MAAM-010513

Amplifier, Driver
40.5 - 43.5 GHz

Rev. V5

Features

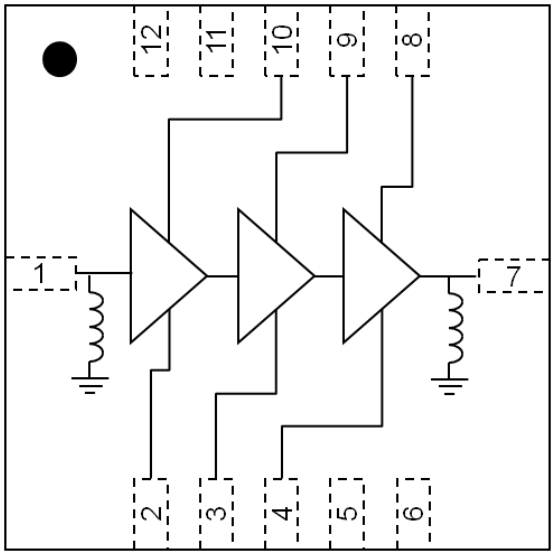
- Gain: 23 dB
- P1dB: 23 dBm
- OIP3: 32 dBm
- Variable Gain with Adjustable Bias
- Lead-Free 5 mm Laminate Package
- RoHS* Compliant and 260°C Reflow Compatible

Description

The MAAM-010513 is a 3-stage driver amplifier with excellent return losses, in a 5 mm laminate package allowing easy assembly. This amplifier product is fully matched to 50 ohms on both the input and output. It can be used as a driver amplifier stage in transmit chains or as an LO buffer amplifier. It is ideally suited for 42 GHz band point-to-point radios.

Each device is 100% RF tested to ensure performance compliance. The part is fabricated using an efficient pHEMT process.

Functional Schematic



Ordering Information

Part Number	Package
MAAM-010513-000000	Bulk Quantity
MAAM-010513-TR0200	200 Piece Reel
MAAM-010513-TR0500	500 Piece Reel
MAAM-010513-001SMB	Sample Evaluation Board

Pin Configuration[1]

Pin No.	Function	Pin No.	Function
1	RF_{IN}	7	RF_{OUT}
2	V_G1	8	V_D3
3	V_G2	9	V_D2
4	V_G3	10	V_D1
5	No Connection	11	No Connection
6	No Connection	12	No Connection
		Paddle[2]	Ground

1. MACOM recommends connecting unused package pins to ground.
2. The exposed pad centered on the package bottom must be connected to RF and DC ground.

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

Electrical Specifications:
Freq: 40.5 - 43.5 GHz, T_A = 25°C, VD = 4 V, ID1 = ID2 = 100 mA, ID3 = 200 mA

Parameter	Units	Min.	Typ.	Max.
Small Signal Gain	dB	19	23	27
Input Return Loss	dB	-	12	-
Output Return Loss	dB	-	15	-
Reverse isolation	dB	-	50	-
Output P1dB	dBm	-	23	-
Output IP3	dBm	27	32	-
Saturated Output Power	dBm	21	25	-
Quiescent Current[3]	mA	-	400	500

3. Adjust V_g between –1.0 and –0.1 V to achieve specified current. Typical 400 mA = 100 (ID1) + 100 (ID2) + 200 (ID3)

Absolute Maximum Ratings [4,5,6]

Parameter	Absolute Max.
Drain Voltage	+4.3 V
Gate Bias Voltage	-1.5V < Vg < 0V
Input Power	+10 dBm
Junction Temperature[7]	150°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +150°C

4. Exceeding any one or combination of these limits may cause permanent damage to this device.
5. MACOM does not recommend sustained operation near these survivability limits.
6. Operating at nominal conditions with $T_J \leq 150°C$ will ensure MTTF > 1 x 10^6 hours.
7. Junction Temperature (T_J) = $T_C + \Theta jc * (V * I)$
   Typical thermal resistance (Θjc) = 26° C/W.
   a) For T_C = 25°C,
   T_J = 67°C @ 4 V, 400 mA
   b) For T_C = 85°C,
   T_J = 127°C @ 4 V, 400 mA

Handling Procedures

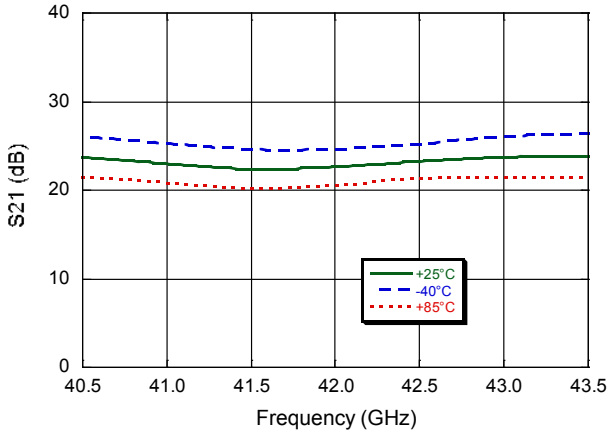
Please observe the following precautions to avoid damage:

Static Sensitivity

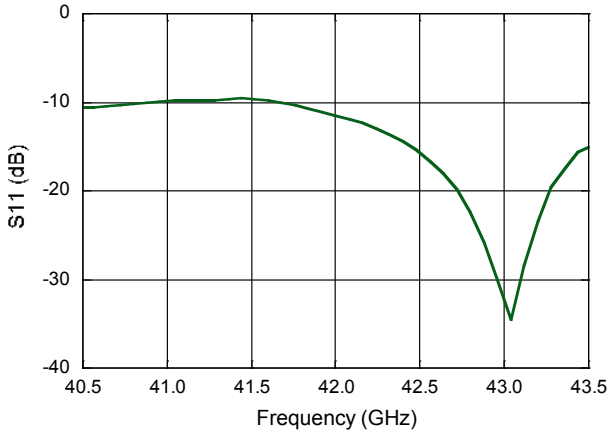
Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these Human Body Model Class 1B and Machine Model Class A devices.

Typical Performance Curves: VD = 4 V, ID1 = ID2 = 100 mA, ID3 = 200 mA, T_A = 25°C

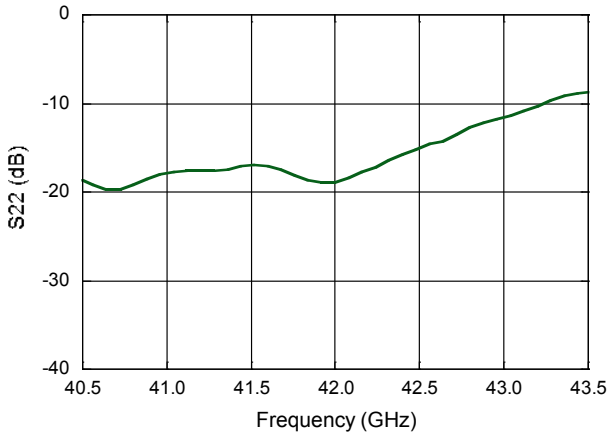
Small Signal Gain



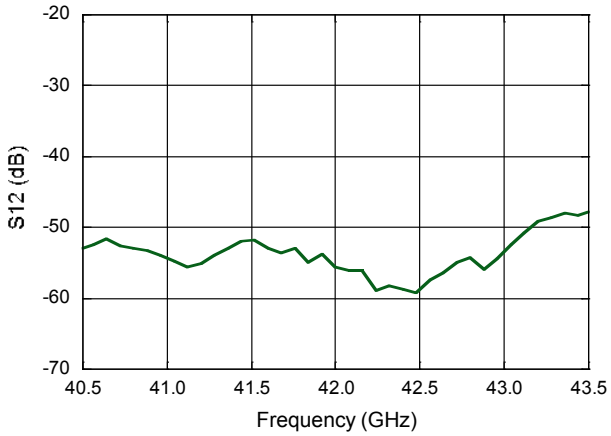
Input Return Loss



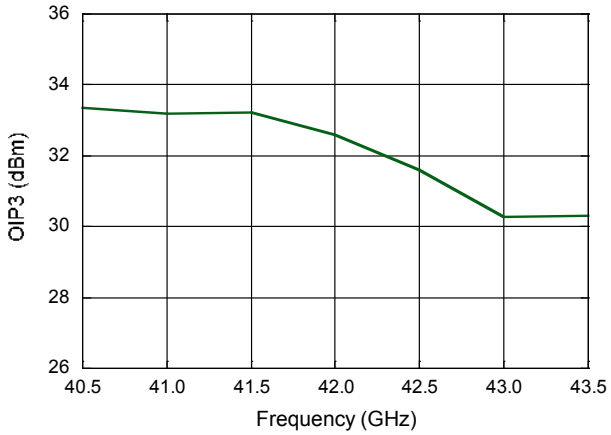
Output Return Loss



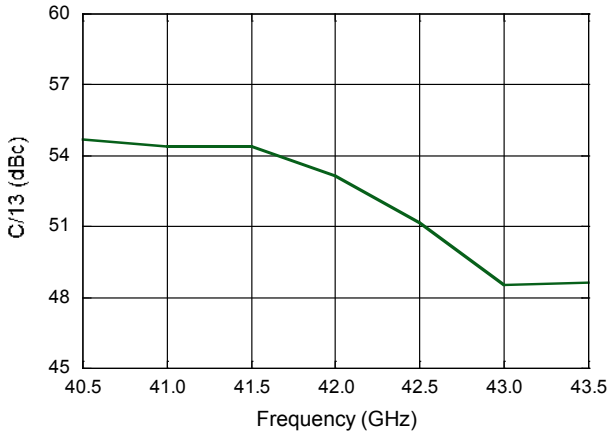
Reverse Isolation



Output IP3 (Pout = 6 dBm SCL)

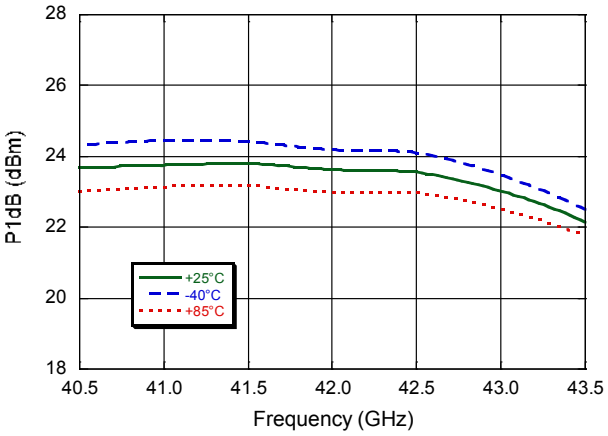


C/I3 (Pout = 6 dBm SCL)

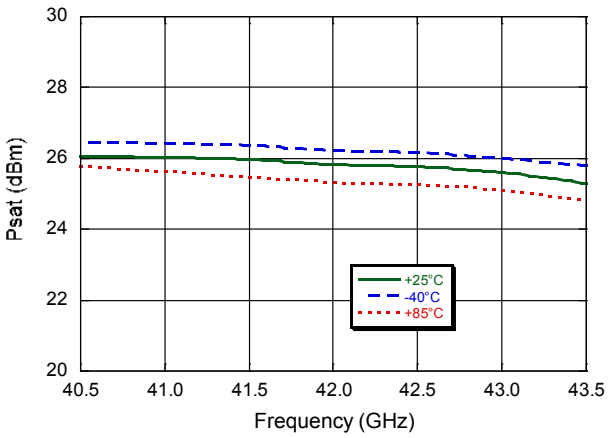


Typical Performance Curves: VD = 4 V, ID1 = ID2 = 100 mA, ID3 = 200 mA, T_A = 25°C

Output P1dB



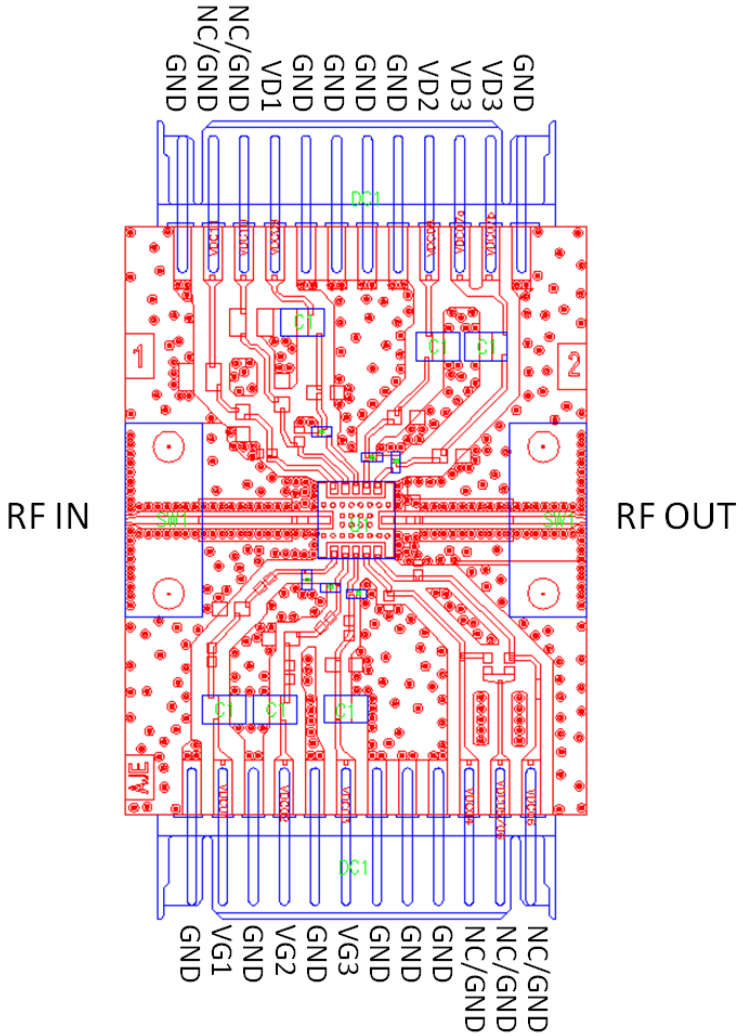
Psat



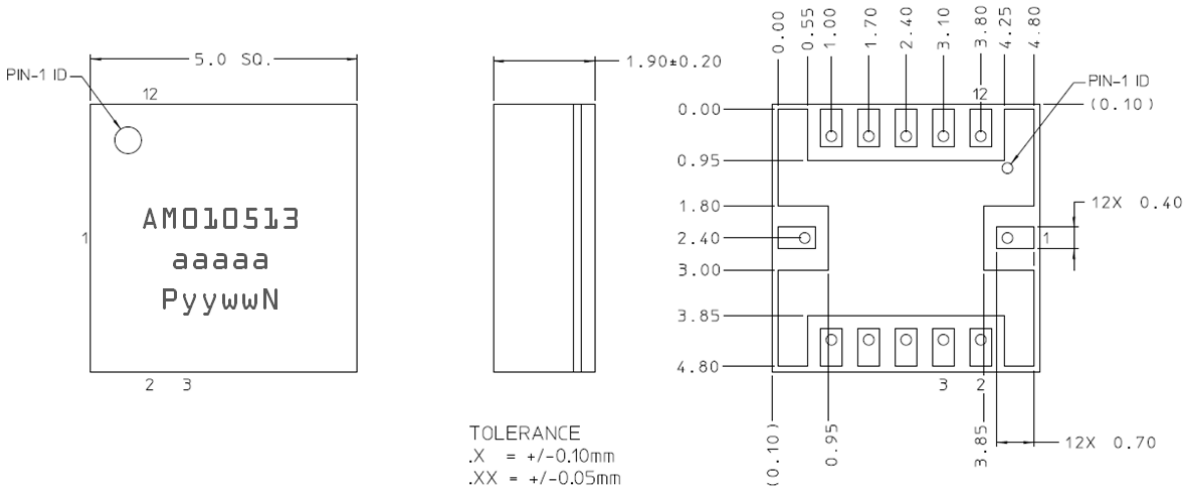
App Note [1] Biasing - It is recommended to bias the amplifier with Vd=4.0 V and IdTOTAL=400 mA. It is also recommended to use active biasing to keep the currents constant as the RF power and temperature vary; this gives the most reproducible results. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage needed to do this is -0.3 V. Typically the gate is protected with Silicon diodes to limit the applied voltage. Also, make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

App Note [2] Bias Arrangement - Each DC pin (Vd and Vg) needs to have DC bypass capacitance (100pF/10nF/1uF) as close to the package as possible.

Recommended Board Layout

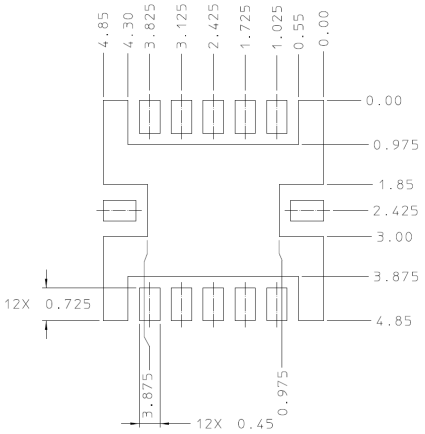


Lead-Free 5 x 5 mm Laminate Package†



Top View | Side View | Bottom View

Recommended Substrate Footprint



All dimensions are in mm.

Markings:
Line 1: MACOM Part Number
Line 2: Lot Wafer Number
Line 3:
P = Philippines (Country of Origin)
yyww: Date Stamp (year-year-week-week)
N = Nickel/Gold plating

† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 3 requirements.

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