MAAP-011246

Power Amplifier, 2 W
27.5 - 31.5 GHz

Rev. V3

Features

- High Gain: 23 dB
- P1dB: 30 dBm
- P_{SAT}: 33 dBm
- IM3 Level: -22 dBc @ P_{OUT} 27 dBm/tone
- Power Added Efficiency: 24% at P_{SAT}
- Lead-Free 5 mm AQFN 32-lead Package
- RoHS* Compliant

Description

The MAAP-011246 is a 2 Watt, 4-stage power amplifier assembled in a lead-free 5 mm 32-lead AQFN plastic package. This power amplifier operates from 27.5 to 31.5 GHz and provides 23 dB of linear gain, 2 W saturated output power and 24% efficiency while biased at 6 V.

The MAAP-011246 can be used as a power amplifier stage or as a driver stage in higher power applications. This device is ideally suited for VSAT and 28 GHz PTP applications.

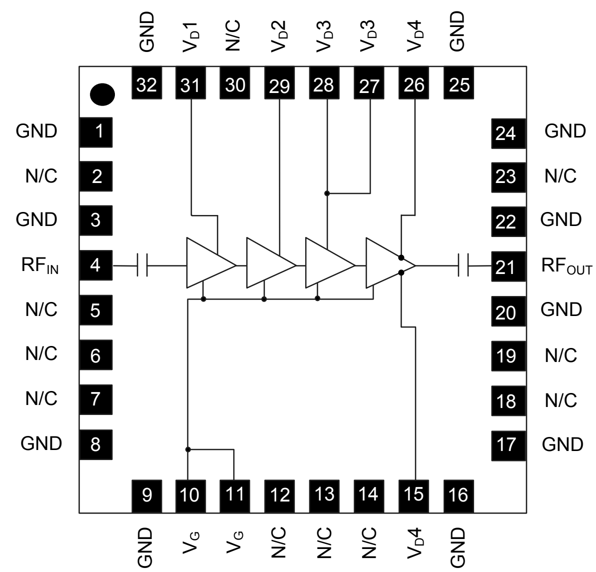
This product is fabricated using a GaAs pHEMT process which features full passivation for enhanced reliability.

Ordering Information[1,2]

Part Number	Package
MAAP-011246-TR0500	500 Piece Reel
MAAP-011246-1SMB	Sample Board

1. Reference Application Note M513 for reel size information.
2. All sample boards include 3 loose parts.

Functional Schematic



Pin Configuration[3]

Pin #	Function	Pin #	Function
1	Ground	20	Ground
2	No Connection	21	RF Output
3	Ground	22	Ground
4	RF Input	23	No Connection
5 - 7	No Connection	24, 25	Ground
8, 9	Ground	26	Drain Voltage 4
10	Gate Voltage	27, 28	Drain Voltage 3
11	Gate Voltage	29	Drain Voltage 2
12 - 14	No Connection	30	No Connection
15	Drain Voltage 4	31	Drain Voltage 1
16, 17	Ground	32	Ground
18, 19	No Connection	Paddle[4]	Ground

3. MACOM recommends connecting all No Connection (N/C) pins to ground.
4. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications: Freq. = 30 GHz, T_A = +25°C, V_D = 6 V, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	P_{IN} = 0 dBm	dB	19	22	—
P_{OUT}	P_{IN} = 15 dBm	dBm	31.5	33	—
IM3 Level	P_{OUT} = 27 dBm / tone	dBc	—	-22	—
Power Added Efficiency	P_{SAT} (P_{IN} = 15 dBm)	%	—	24	—
Input Return Loss	P_{IN} = -20 dBm	dB	—	10	—
Output Return Loss	P_{IN} = -20 dBm	dB	—	14	—
Quiescent Current	I_{DQ} (see bias conditions, page 4)	mA	—	900	—
Current	P_{SAT} (P_{IN} = 15 dBm)	mA	—	1450	—

Maximum Operating Ratings

Parameter	Rating
Input Power	15 dBm
Junction Temperature[5,6]	+160°C
Operating Temperature	-40°C to +85°C

5. Operating at nominal conditions with junction temperature ≤ +160°C will ensure MTTF > 1 x 10^6 hours.
6. Junction Temperature (T_J) = T_C + $Θ_{JC}$ * ((V * I) - (P_{out} - P_{IN}))
   Typical thermal resistance ($Θ_{JC}$) = 8°C/W.
   a) For T_C = +25°C,
   T_J = +79°C @ 6 V, 1.45 A, P_{OUT} = 33.0 dBm, P_{IN} = 15 dBm
   b) For T_C = +85°C,
   T_J = +136°C @ 6 V, 1.34 A, P_{OUT} = 32.4 dBm, P_{IN} = 15 dBm

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

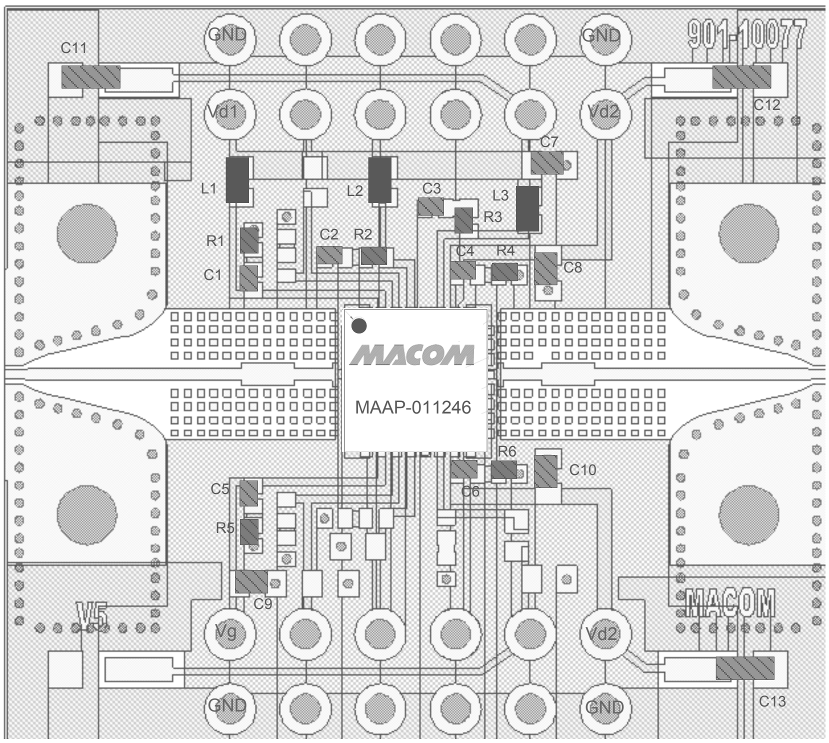
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A devices.

Absolute Maximum Ratings[7,8]

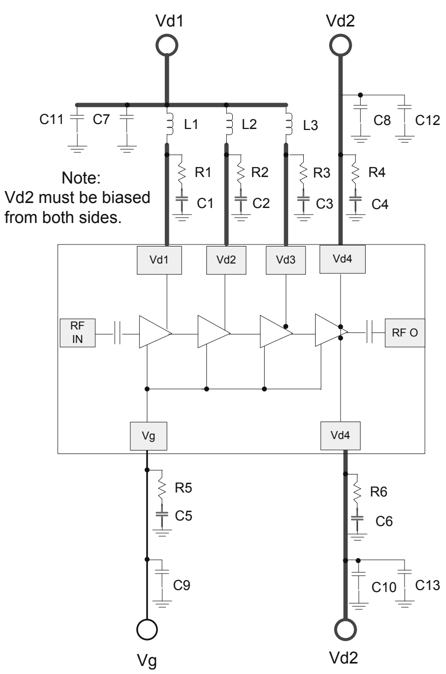
Parameter	Absolute Maximum
Input Power	20 dBm
Drain Voltage	+6.5 V
Gate Voltage	-3 to 0 V
Junction Temperature[9]	+175°C
Storage Temperature	-65°C to +125°C

7. Exceeding any one or combination of these limits may cause permanent damage to this device.
8. MACOM does not recommend sustained operation near these survivability limits.
9. Junction temperature directly effects device MTTF. Junction temperature should be kept as low as possible to maximize lifetime.

Sample Board Layout



Application Schematic



Parts List

Part	Value	Case Style
C1 - C6	0.01 µF	0402
C7 - C10	1 µF	0402
C11 - C13	10 µF	0603
R1 - R6	10 Ω	0402
L1 - L3[10]	600 Ω @ 100 MHz	0603

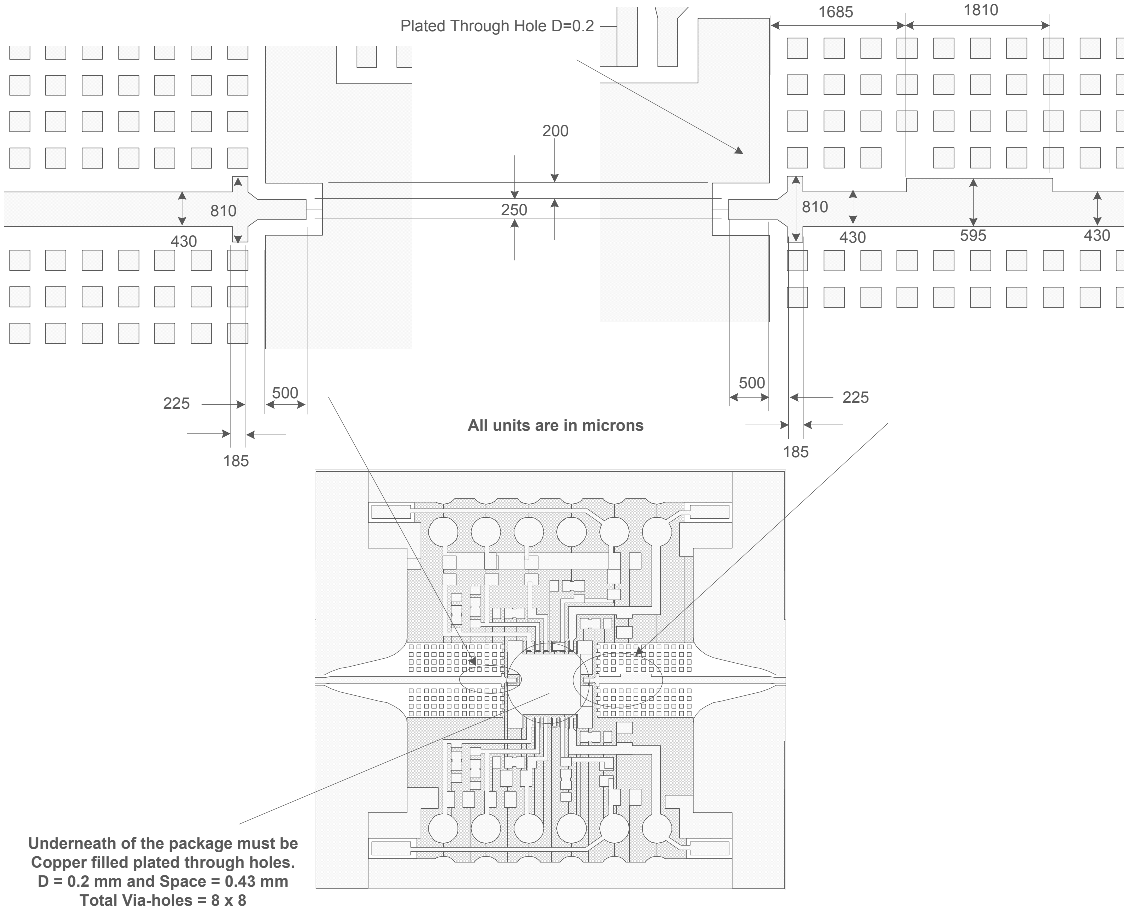
10. L1 - L3 (chip ferrite bead) supplied from Murata, part number BLM18HE601SN1D.

Sample Board Material Specifications

Top Layer: 1/2 oz Copper Cladding, 0.017 mm thickness
Dielectric Layer: Rogers RO4003C 0.203 mm thickness
Bottom Layer: 1/2 oz Copper Cladding, 0.017 mm thickness
Finished overall thickness: 0.238 mm

Recommended PCB Layout Detail:

RF input and output pre-matching circuit patterns are designed to compensate packaging effects. Transmission line dimensions apply to a PCB with 0.203 mm thick Rogers RO4003C laminate dielectric. Performance curves shown in this data sheet were measured with these circuit patterns.



Biasing Conditions

Recommended biasing conditions are V_D = 6 V, I_{DQ} = 900 mA (controlled with V_G). The drain bias voltage range is 3 to 6 V, and the quiescent drain current biasing range is 600 to 1200 mA.

V_G pins 10 and 11 are connected internally; choose either pin for layout convenience. Muting can be accomplished by setting the V_G to the pinched off voltage (V_G = -2 V).

V_D bias must be applied to V_D1, V_D2, V_D3, and V_D4 pins. V_D3 pins 27 and 28 are connected internally: choose either pin for layout convenience. Two V_D4 pins 15 and 26 (not connected internally) are required for current symmetry.

Operating the MAAP-011246

Turn-on

1. Apply V_G (-1.5 V).
2. Apply V_D (6.0 V typical).
3. Set I_{DQ} by adjusting V_G more positive (typically -0.9 to -1.0 V for I_{DQ} = 900 mA).
4. Apply RF_{IN} signal.

Turn-off

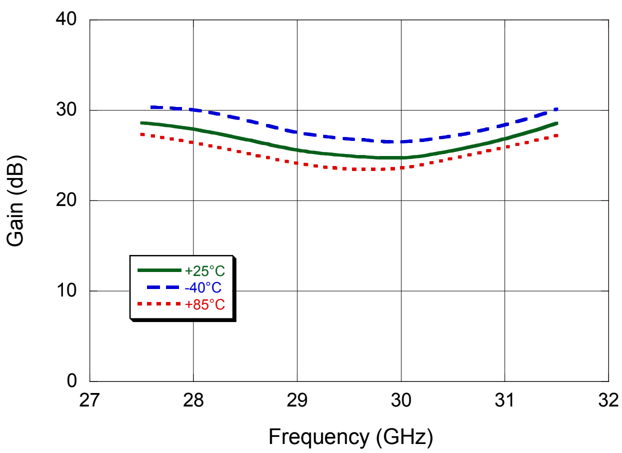
1. Remove RF_{IN} signal.
2. Decrease V_G to -1.5 V.
3. Decrease V_D to 0 V.

Electrical Specifications with the Recommended PCB Layout and bias conditions: Freq. = 27.5 - 29.5 GHz, T_A = +25°C, V_D = 6 V, Z_0 = 50 Ω

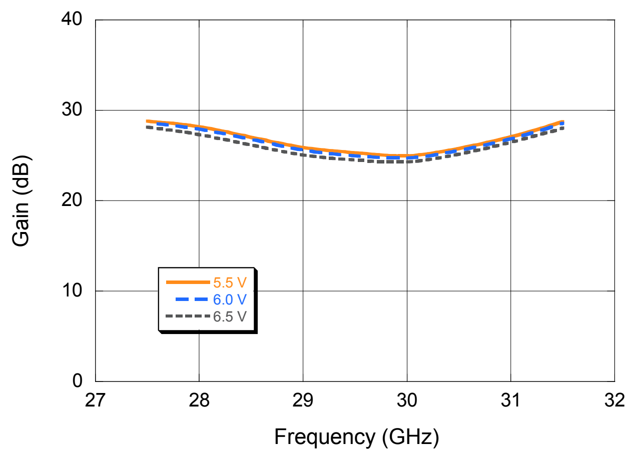
Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	P_{IN} = 0 dBm	dB	19	27	30.5
P_{SAT}		dBm	31.5	33.5	—
IM3 Level	P_{OUT} = 27 dBm / tone	dBc	—	-20	—
Power Added Efficiency	P_{SAT}	%	—	24	—
Input Return Loss	P_{IN} = -20 dBm	dB	—	15	—
Output Return Loss	P_{IN} = -20 dBm	dB	—	13	—
Quiescent Current	I_{DQ} (see bias conditions, page 4)	mA	—	900	—
Current	P_{SAT}	mA	—	1600	—

Typical Performance Curves

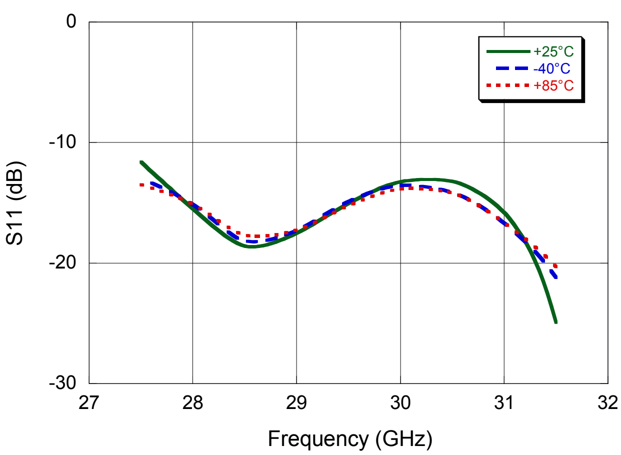
Gain vs. Frequency over Temperature



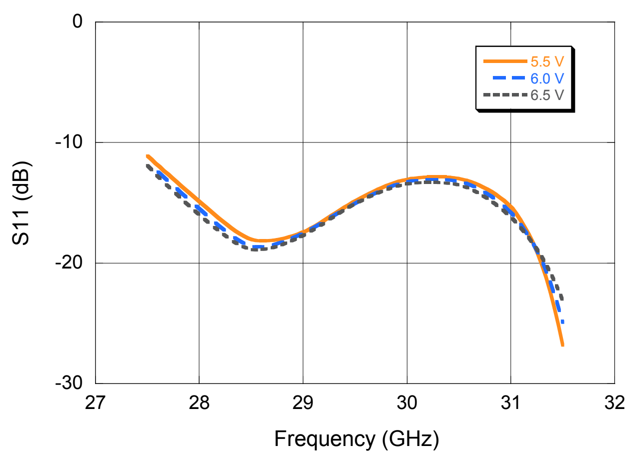
Gain vs. Frequency over Bias Voltage



Input Return Loss vs. Frequency over Temperature

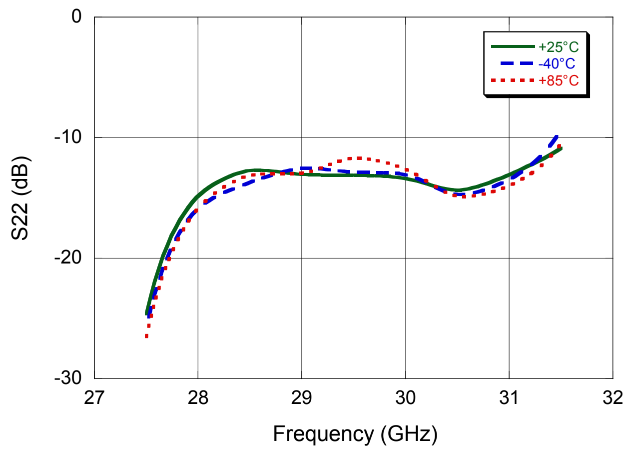


Input Return Loss vs. Frequency over Bias Voltage

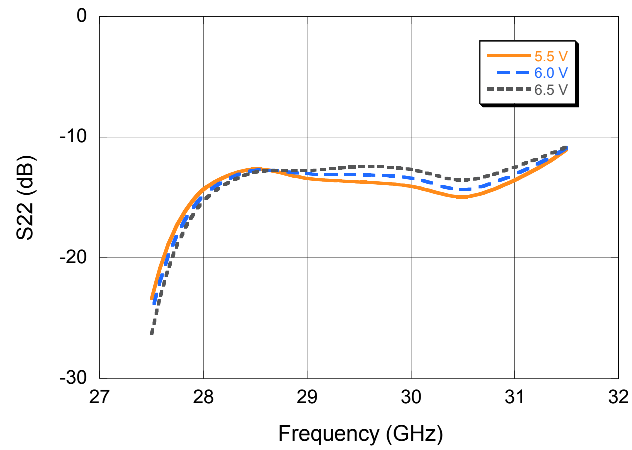


Typical Performance Curves over Temperature

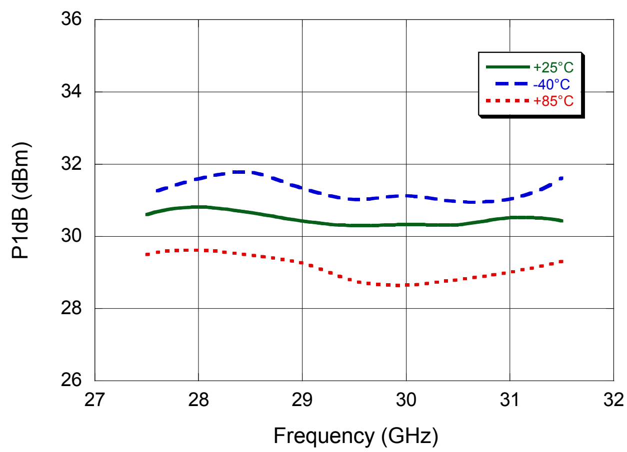
Output Return Loss vs. Frequency over Temperature



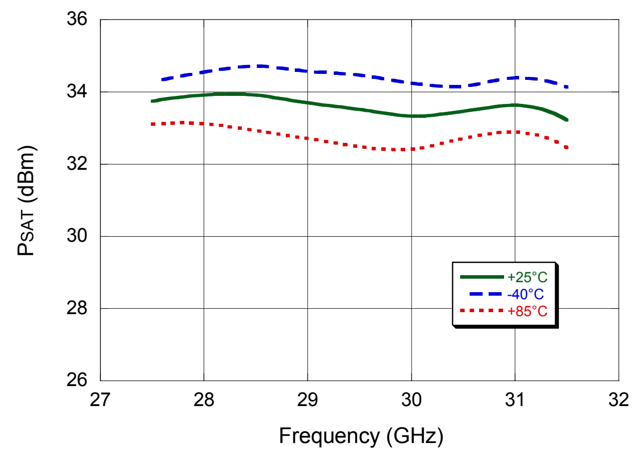
Output Return Loss vs. Frequency over Bias Voltage



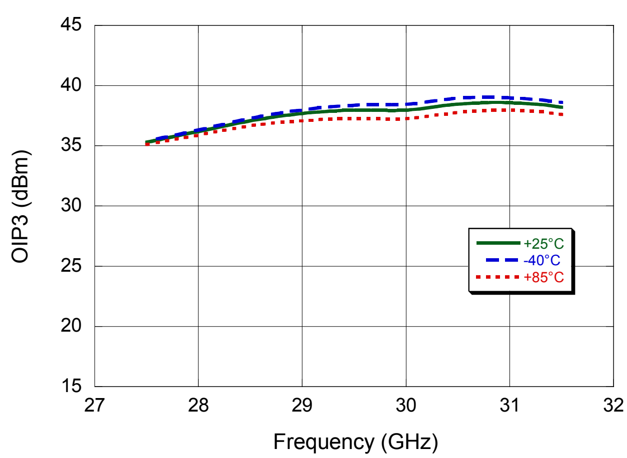
P1dB Output Power vs. Frequency



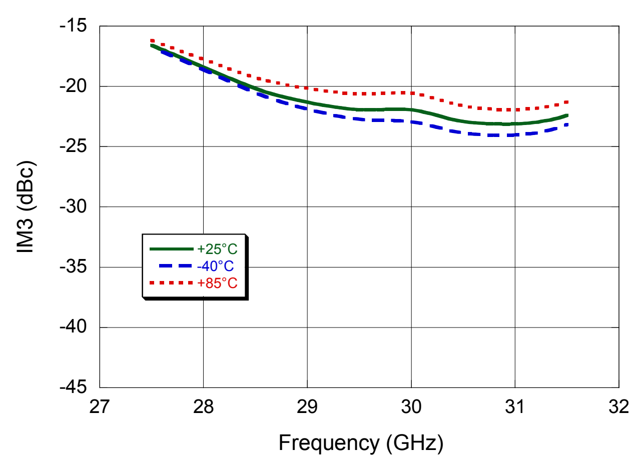
P_{SAT} Output Power vs. Frequency



OIP3 vs. Frequency (P_{OUT} = 27 dBm/tone)

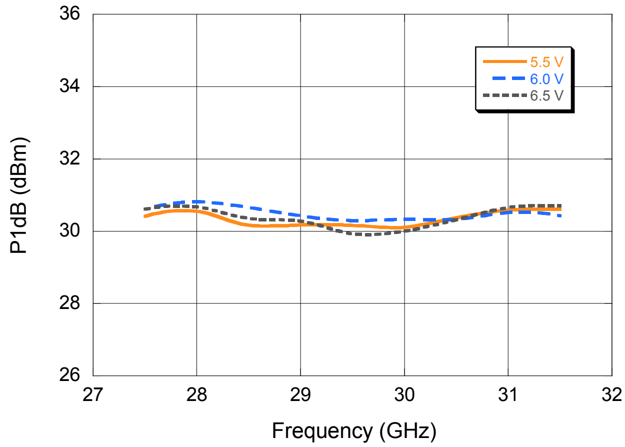


IM3 vs. Frequency (P_{OUT} = 27 dBm/tone)

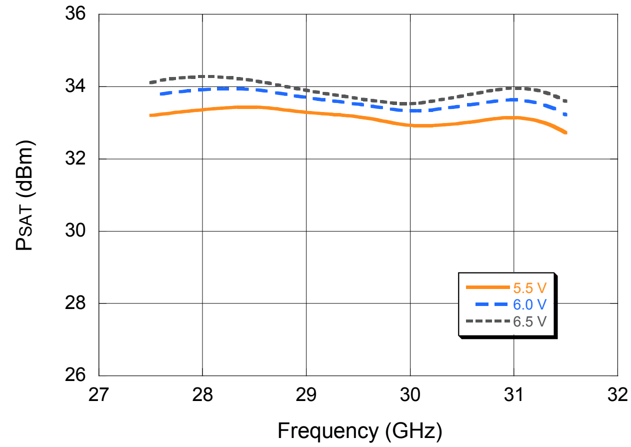


Typical Performance Curves over Bias Voltage

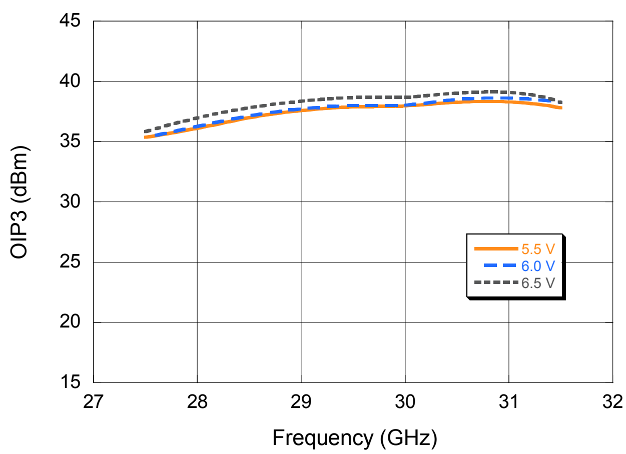
P1dB Output Power vs. Frequency



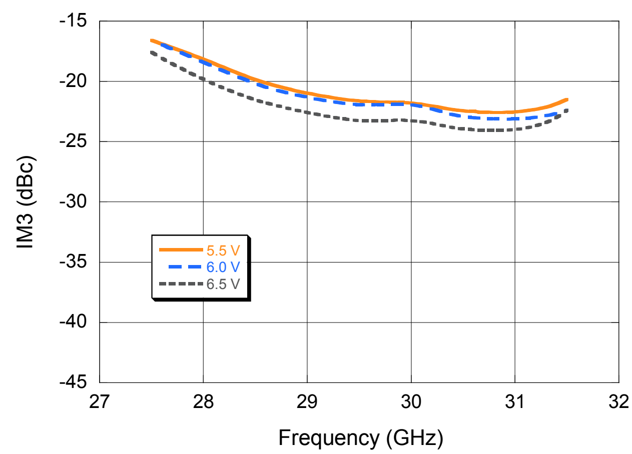
P_{SAT} Output Power vs. Frequency



OIP3 vs. Frequency (P_{OUT} = 27 dBm/tone)

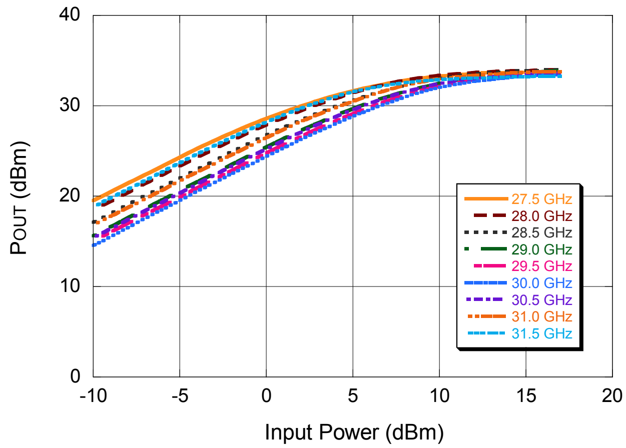


IM3 vs. Frequency (P_{OUT} = 27 dBm/tone)

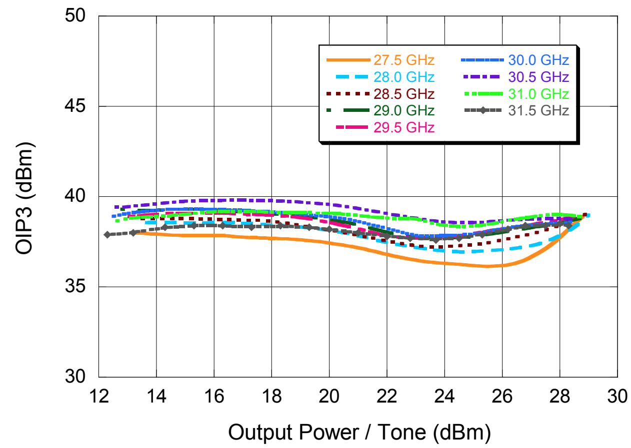


Typical Performance Curves over Frequency

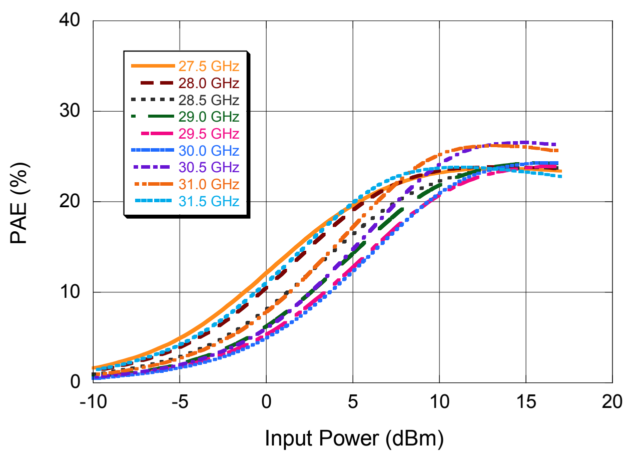
P_{OUT} vs. P_{IN}



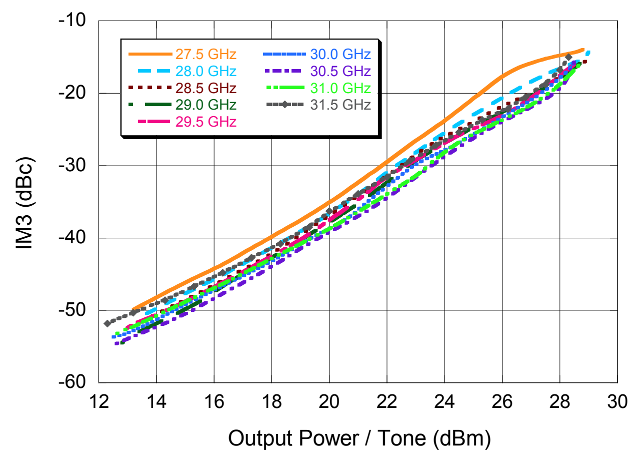
OIP3 vs. P_{OUT} (dBm/tone)



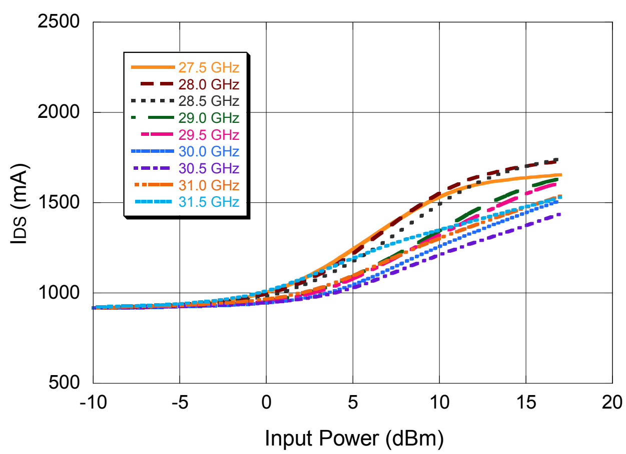
PAE vs. P_{IN}



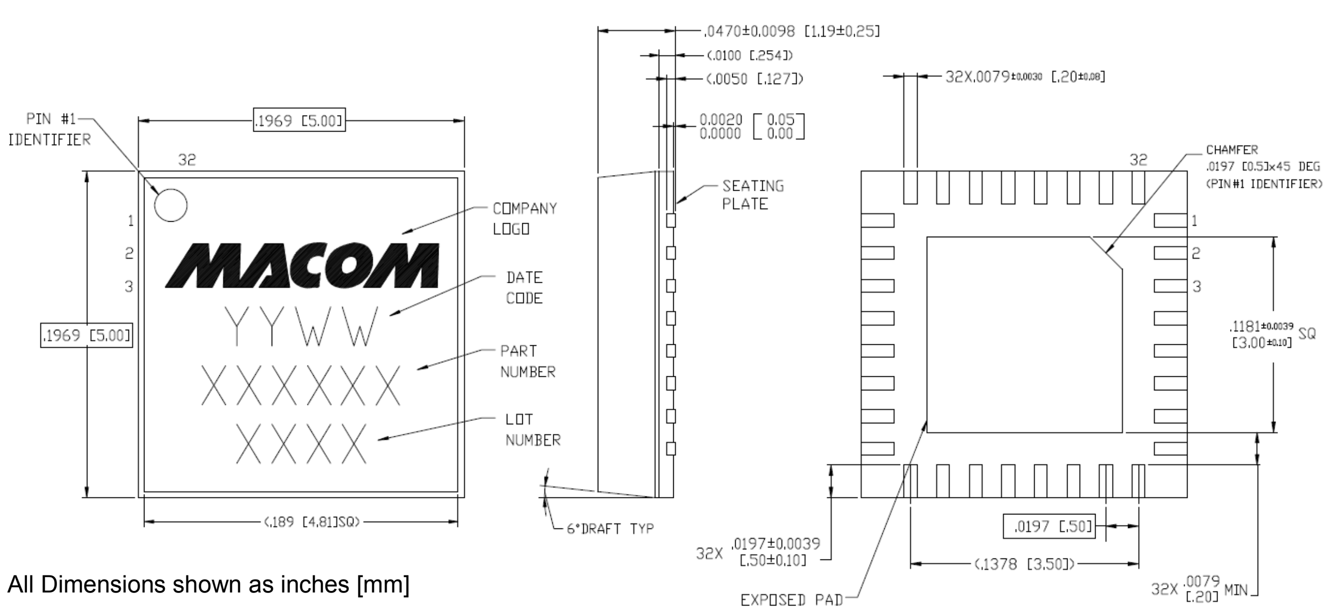
IM3 Level vs. P_{OUT} (dBm/tone)



I_{DS} vs. P_{IN}



Lead-Free 5 mm AQFN 32-Lead†



All Dimensions shown as inches [mm]

† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 3 requirements.
Plating is NiPdAu.