

## Features

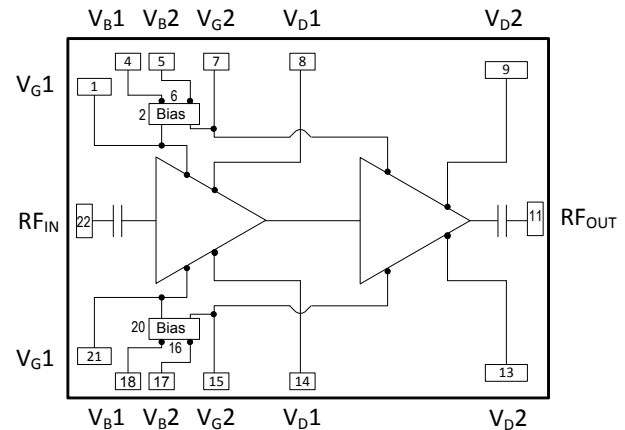
- 12 W X-Band Power Amplifier
- 21 dB Large Signal Gain
- 41 dBm Saturated Pulsed Output Power
- 40% Power Added Efficiency
- On Chip Gate Bias Circuit
- 100% On-wafer DC & RF Power Tested
- 100% Visual Inspection to MIL-STD-833
- Bare Die

## Description

The MAAP-015030-DIE two stage 8.5 - 11.75 GHz GaAs MMIC power amplifier has a saturated pulsed output power of 41 dBm and a large signal gain of 21 dB. The power amplifier can be biased using a direct gate voltage or using an on chip gate bias circuit.

This device is well suited for communication and radar applications.

## Functional Schematic



## Pad Configuration

Pad #	Function	Pad #	Function
1	V <sub>G1</sub>	12	GND
2	Bias Circuit GND	13	V <sub>D2</sub>
3	No Connection	14	V <sub>D1</sub>
4	V <sub>B1</sub>	15	V <sub>G2</sub>
5	V <sub>B2</sub>	16	Bias Circuit GND
6	Bias Circuit GND	17	V <sub>B2</sub>
7	V <sub>G2</sub>	18	V <sub>B1</sub>
8	V <sub>D1</sub>	19	GND
9	V <sub>D2</sub>	20	Bias Circuit GND
10	GND	21	V <sub>G1</sub>
11	RF <sub>OUT</sub>	22	RF <sub>IN</sub>

## Ordering Information

Part Number	Package
MAAP-015030-DIE	Die in Vacuum release gel pack
MAAP-015030-DIEEV1	Direct gate bias sample board
MAAP-015030-DIEEV2	On chip gate bias sample board

\* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

## Power Amplifier, 13 W 8.5 - 11.75 GHz

Rev. V5

### Electrical Specifications:

Freq. = 8.5 - 11.5 GHz,  $T_A = +25^\circ\text{C}$ , Duty Cycle = 5%,  $P_{IN} = 20\text{ dBm}$ ,  $V_G = -0.9\text{ V}$

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain (Large Signal)	8.5 - 11.5 GHz 11.5 - 11.75 GHz	dB	20 19	21	—
Gain	—	dB	—	25	—
Gain Flatness	—	dB	—	1	—
Input Return Loss	—	dB	—	12	—
Output Return Loss	—	dB	—	10	—
Saturated Output Power	8.5 - 11.5 GHz 11.5 - 11.75 GHz	dBm	40 39	41	—
Power Added Efficiency	8.5 - 9.0 GHz 9.0 - 10.0 GHz 10.0 - 11.75 GHz	%	—	35 40 40	—
Drain Bias Voltage	—	V	—	8.0	—
Drain Current	—	A	—	5	5.5

### Absolute Maximum Ratings<sup>1,2</sup>

Parameter	Absolute Maximum
Input Power	23 dBm
Drain Voltage	8.5 V
Gate Voltage	$-2.0\text{ V} < V_G < -0.7\text{ V}$
Bias Voltage	$-6.5\text{ V} < V_B < -4.5\text{ V}$
Drain Current	$< 6.0\text{ A}$
Gate Current	$< 30\text{ mA}$
Operating Temperature	$-40^\circ\text{C}$ to $+85^\circ\text{C}$
Junction Temperature <sup>3,4</sup>	$+175^\circ\text{C}$

- Exceeding any one or combination of these limits may cause permanent damage to this device.
- MACOM does not recommend sustained operation near these survivability limits.
- Operating at nominal conditions with  $T_J \leq +175^\circ\text{C}$  will ensure  $\text{MTTF} > 1 \times 10^6$  hours.
- Junction Temperature ( $T_J$ ) =  $T_A + \Theta_{jc} * (V * I)$   
Typical thermal resistance ( $\Theta_{jc}$ ) =  $5.7^\circ\text{C/W}$ .
  - For  $T_A = 25^\circ\text{C}$ ,  
 $T_J = 175^\circ\text{C}$  @ 8 V, 3.29 A
  - For  $T_A = 85^\circ\text{C}$ ,  
 $T_J = 175^\circ\text{C}$  @ 8 V, 1.97 A

### Handling Procedures

Please observe the following precautions to avoid damage:

### Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

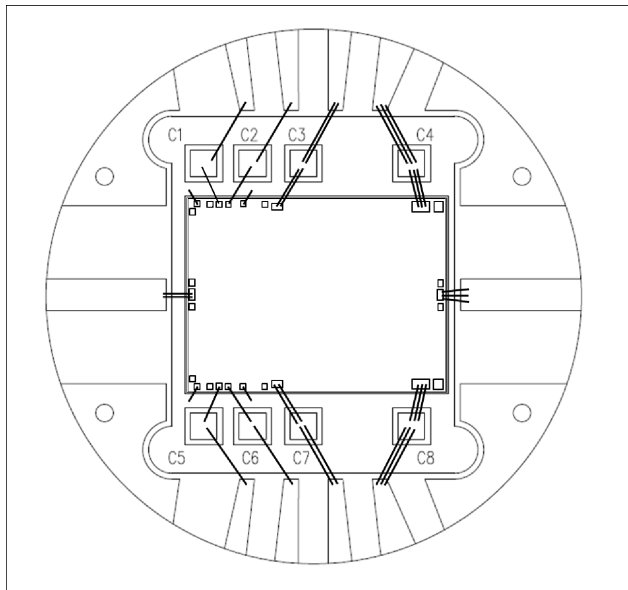
# MAAP-015030-DIE



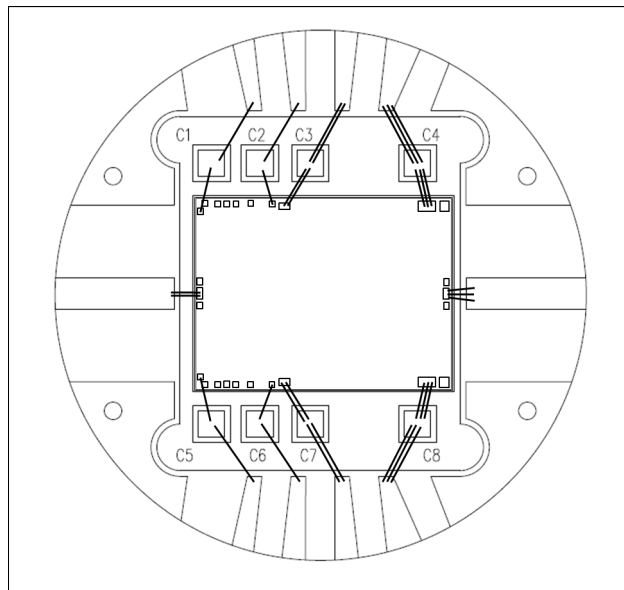
Power Amplifier, 13 W  
8.5 - 11.75 GHz

Rev. V5

## Bonding Diagram - On Chip Bias<sup>5</sup>

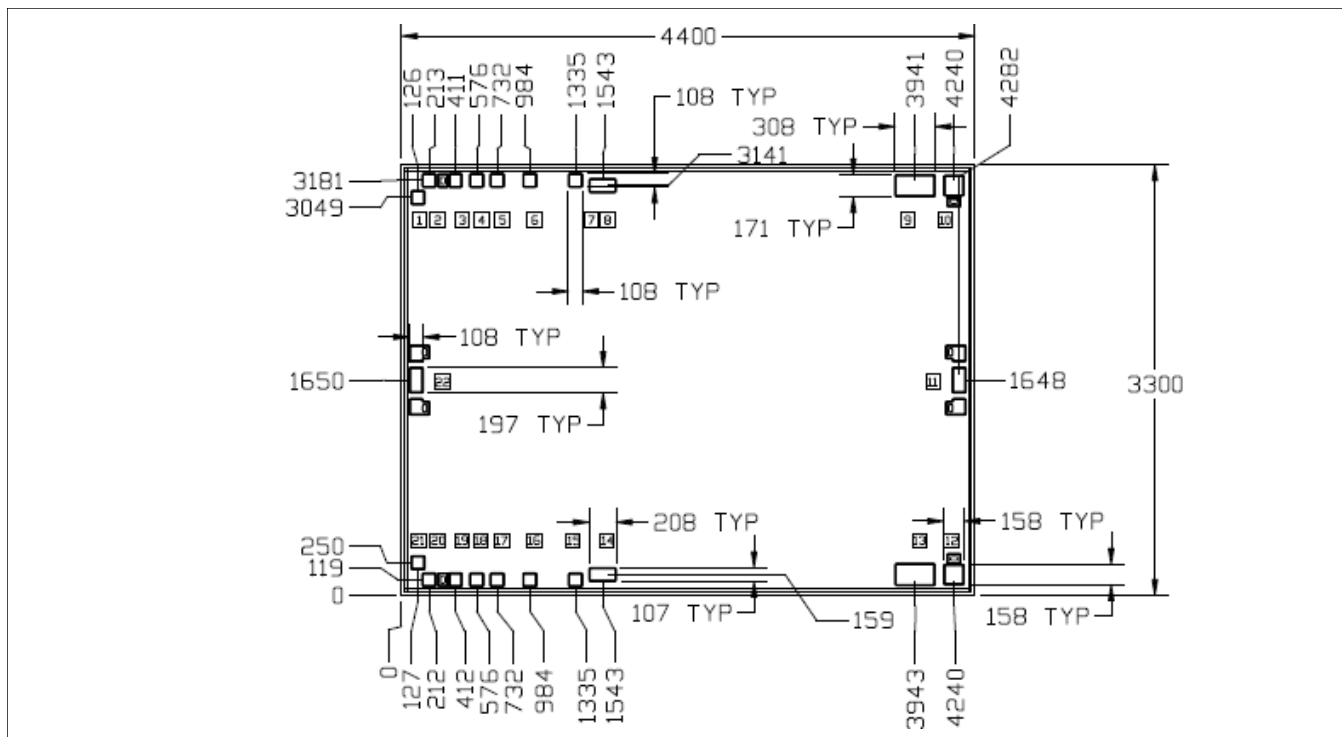


## Bonding Diagram - Direct Gate Bias<sup>5</sup>



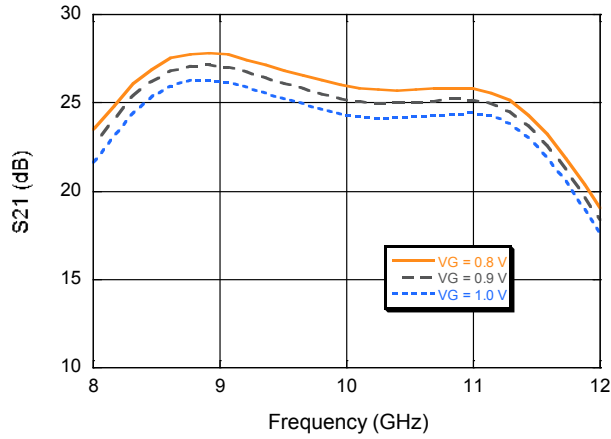
5. Components C1 - C8 are all 100 pF chips.

## MMIC Bare Die

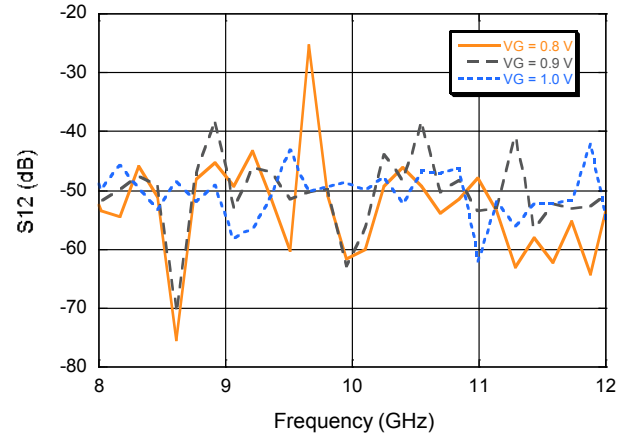


## Typical Performance Curves over Voltage

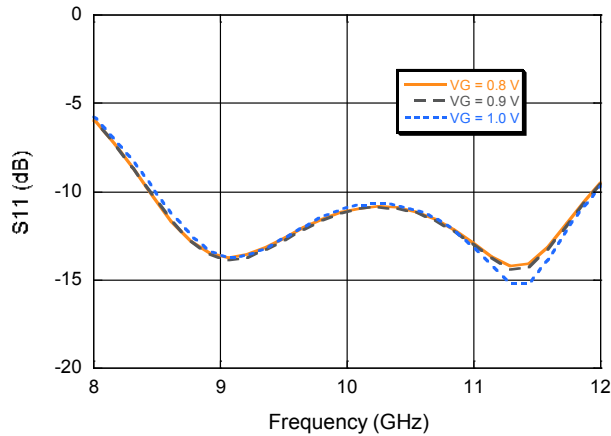
Gain vs. Frequency



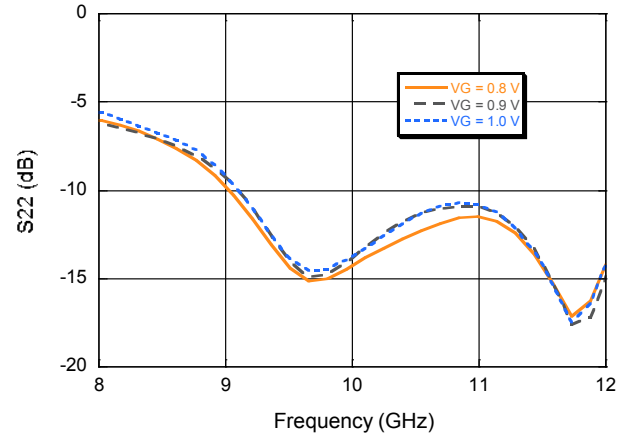
Reverse Isolation vs. Frequency



Input Return Loss vs. Frequency

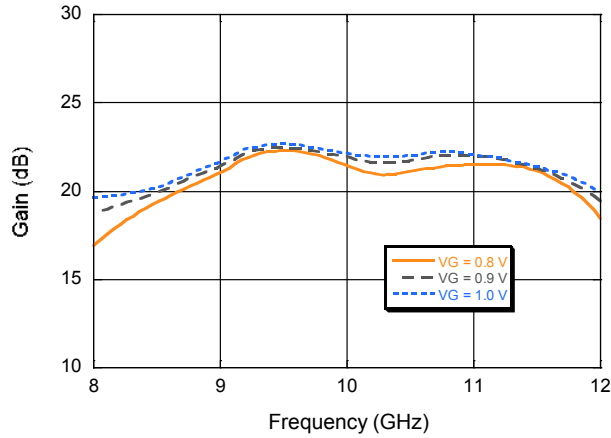


Output Return Loss vs. Frequency

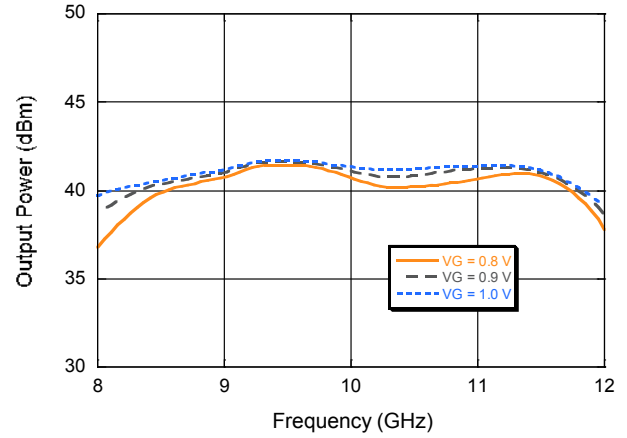


## Typical Performance Curves over Voltage

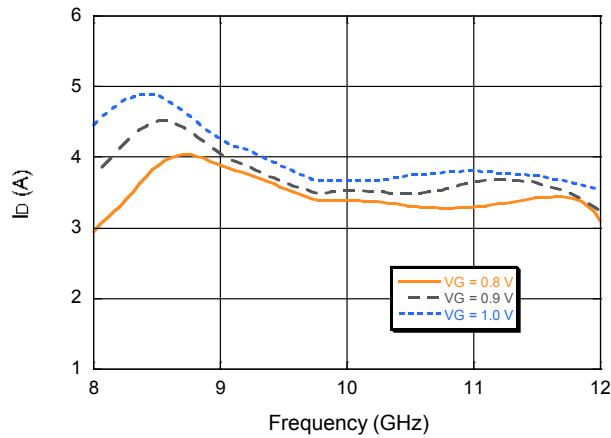
**Gain vs. Frequency**



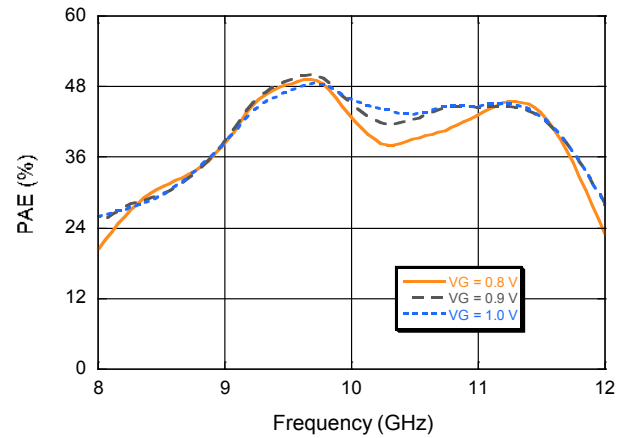
**Output Power vs. Frequency**



**Drain Current vs. Frequency**

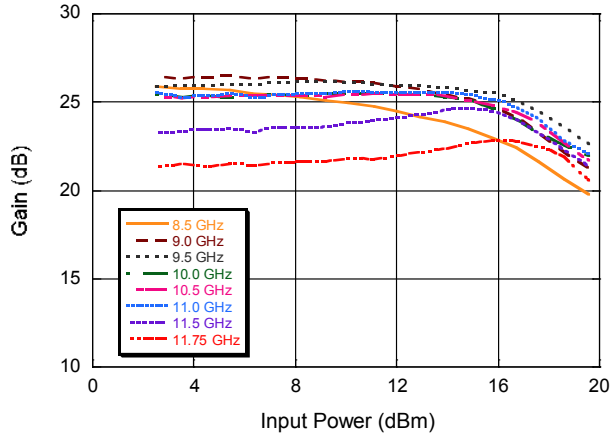


**PAE vs. Frequency**

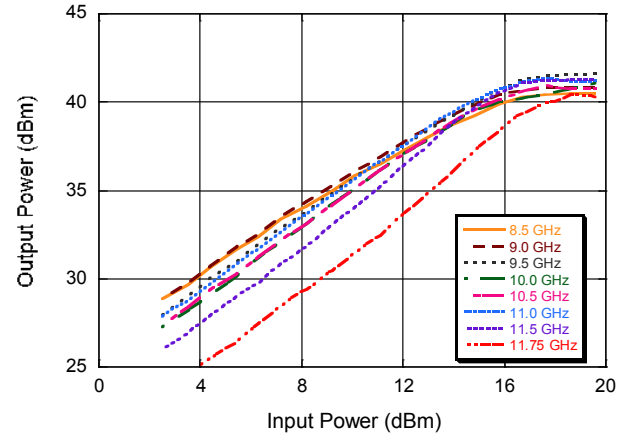


## Typical Performance Curves over Frequency

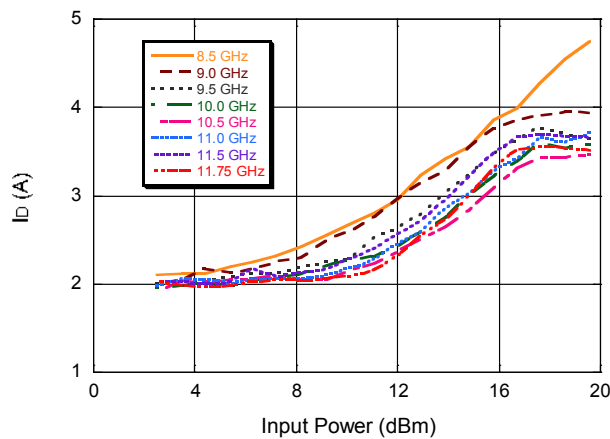
**Gain vs. Input Power**



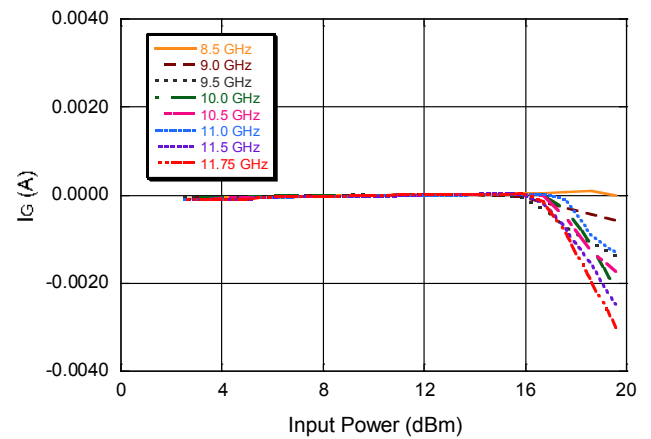
**Output Power vs. Input Power**



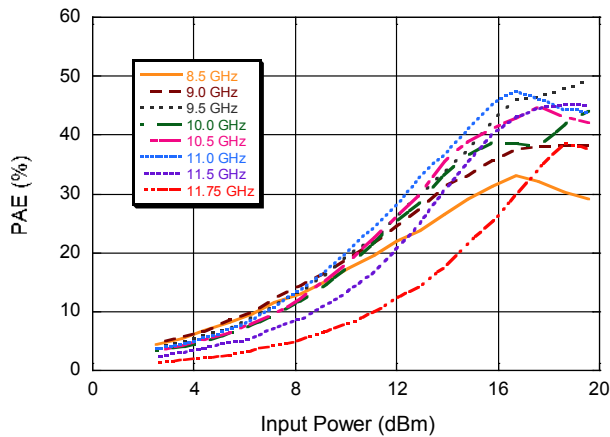
**Drain Current vs. Input Power**



**Gate Current vs. Input Power**

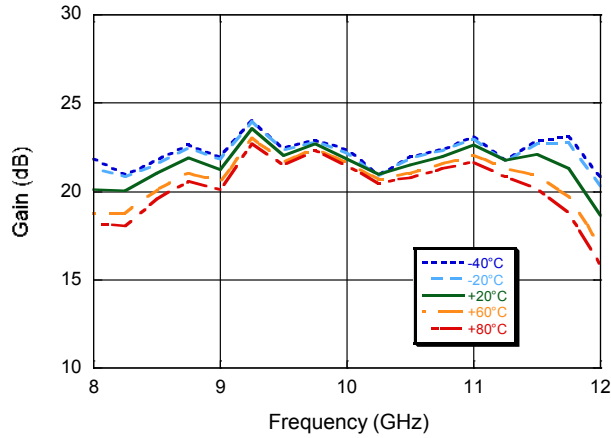


**PAE vs. Input Power**

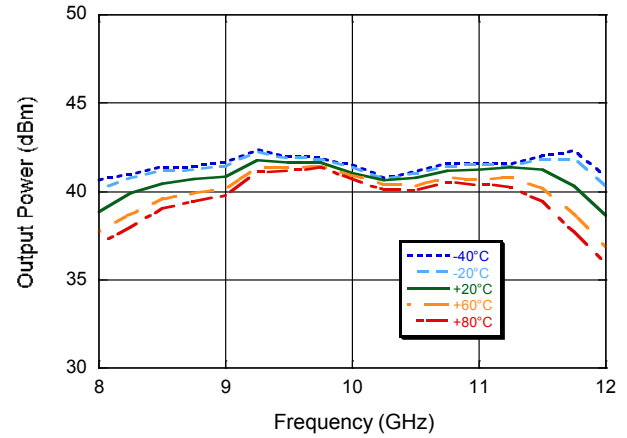


**Typical Performance Curves over Temperature:  $P_{IN} = 19.5$  dBm**

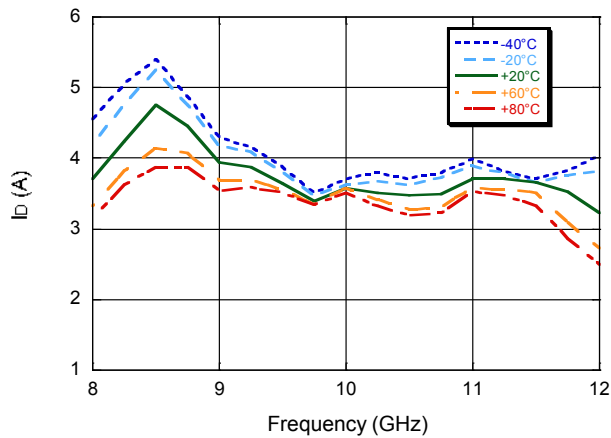
**Gain vs. Frequency**



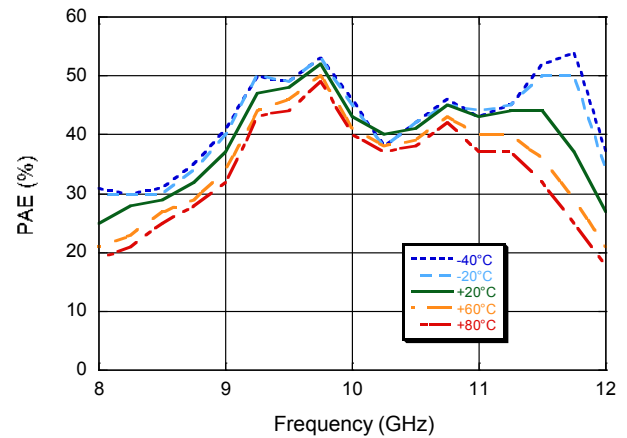
**Output Power vs. Frequency**



**Drain Current vs. Frequency**

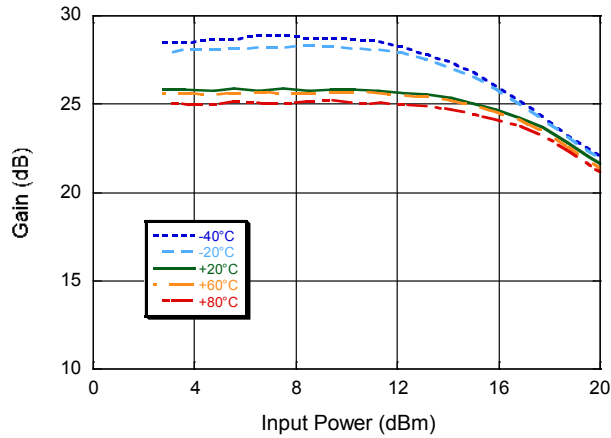


**PAE vs. Frequency**

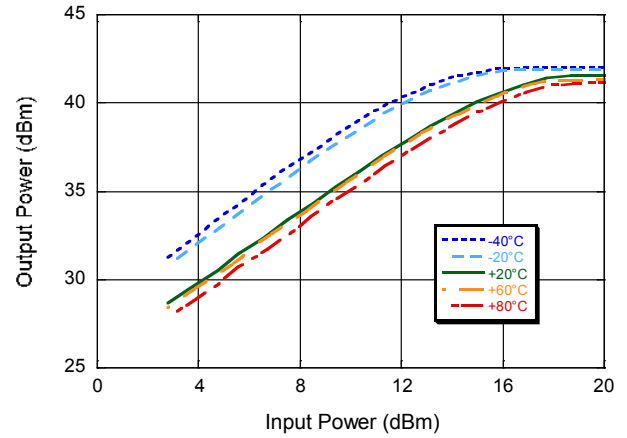


## Typical Performance Curves over Temperature

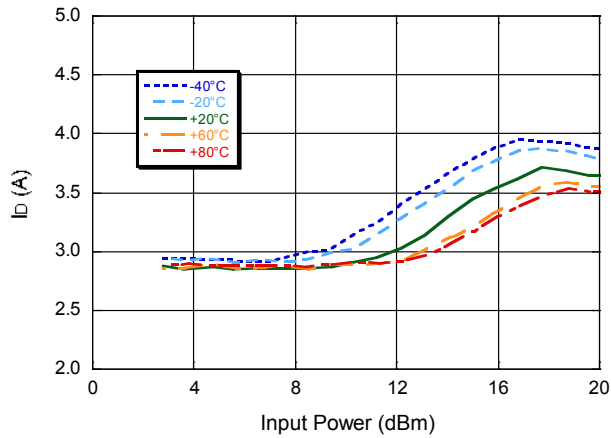
**Gain vs. Input Power**



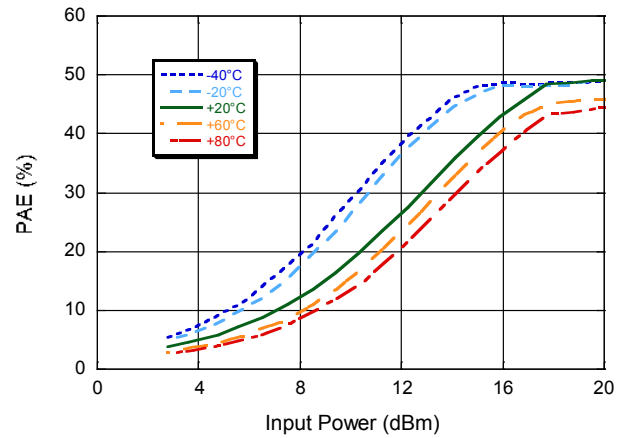
**Output Power vs. Input Power**



**Drain Current vs. Input Power**



**PAE vs. Input Power**





## Applications Section

### Application Notes

#### Note 1 - Biasing

The gate biasing is applied in one of the following:

1. Direct Gate Bias:  $V_{G1}$  &  $V_{G2}$  provide the direct gate bias input to the 2 MMIC stages. This method of biasing allows the user to control the total drain current without the scaling factor provided by the bias circuit. It is recommended that the gate voltage is supplied by both sides of the Die. Optimum performance can be achieved with a -0.9 V operation.
2. Bias Circuit Biasing: Applying -5 V to  $V_{B1}$  &  $V_{B2}$  will typically draw 2A with no further adjustment necessary. Wafer lot variation may result in some devices experiencing higher or lower drain currents than the typical 2 A. It is necessary to connect the Bias Circuit Ground (Pad 2,6,16,20) to ground in order for this bias circuit to function correctly. It is recommended that the bias circuits on both sides of the PA are used.

#### Note 2 - Bias Sequence

When switching on the PA, In each case, the gate bias must be applied before the drain voltage is applied. Both the  $V_{D1}$  and  $V_{D2}$  should be biased from the top and bottom sides of the die.

#### Note 3 - Decoupling Circuits

Each bias pad,  $V_G$  or  $V_B$  and the  $V_{D1}$ ,  $V_{D2}$  must have a decoupling capacitor of 100 pF as close to the device as possible, as is shown in the bonding diagrams. In the case where the bias circuit is used the additional bond wire to ground must be made as short as possible.

#### Note 4 - Pulse Operation

The performance of the MAAP-015030-BD is characterized under pulsed conditions with a duty cycle of 5% consisting of a pulse width of 5  $\mu$ s applied to the drain. Under pulsed conditions the gate is constantly biased using either the on chip bias circuit or using a gate voltage directly applied to the PA. It is recommended that the die is mounted with an adequate thermal solution.

#### Note 5 - CW Operation

The PA is only recommended for CW operation at reduced drain voltages.

## Applications Section

### Handling and Assembly

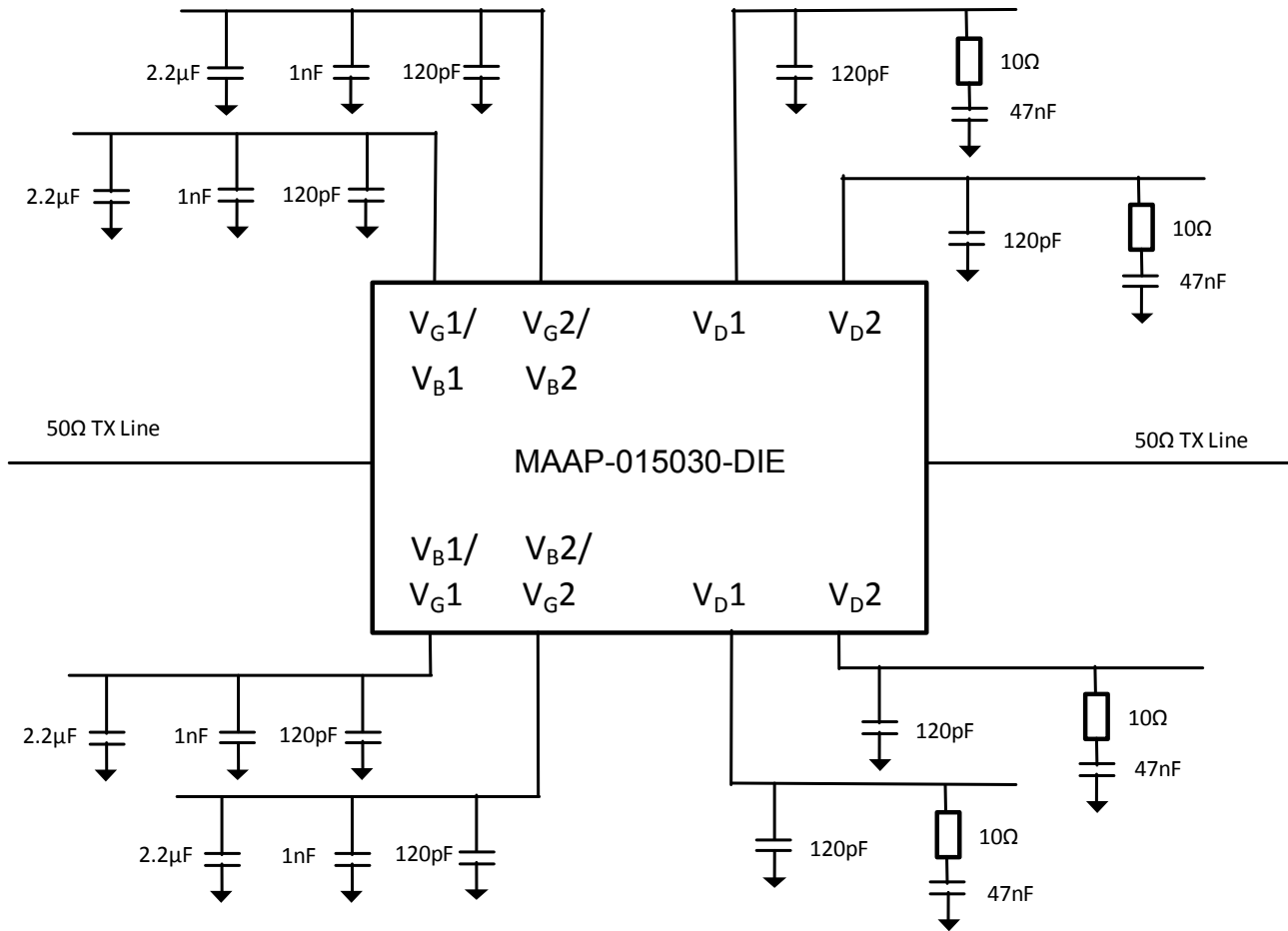
#### Die Attachment

This product is 0.100 mm (0.004") thick and has vias through to the backside to enable grounding to the circuit. Microstrip substrates should be brought as close to the die as possible. The mounting surface should be clean and flat. If using conductive epoxy, recommended epoxies are Tanaka TS3332LD, Die Mat DM6030HK or DM6030HK-Pt cured in a nitrogen atmosphere per manufacturer's cure schedule. Apply epoxy sparingly to avoid getting any on to the top surface of the die. An epoxy fillet should be visible around the total die periphery. For additional information please see the MACOM "Epoxy Specifications for Bare Die" application note. If eutectic mounting is preferred, then a flux-less gold-tin (AuSn) preform, approximately 0.0012 thick, placed between the die and the attachment surface should be used. A die bonder that utilizes a heated collet and provides scrubbing action to ensure total wetting to prevent void formation in a nitrogen atmosphere is recommended. The gold-tin eutectic (80% Au 20% Sn) has a melting point of approximately 280°C (Note: Gold Germanium should be avoided). The work station temperature should be 310°C +/- 10°C. Exposure to these extreme temperatures should be kept to minimum. The collet should be heated, and the die pre-heated to avoid excessive thermal shock. Avoidance of air bridges and force impact are critical during placement.

#### Wire Bonding

Windows in the surface passivation above the bond pads are provided to allow wire bonding to the die's gold bond pads. The recommended wire bonding procedure uses 0.076 mm x 0.013 mm (0.003" x 0.0005") 99.99% pure gold ribbon with 0.5 - 2% elongation to minimize RF port bond inductance. Gold 0.025 mm (0.001") diameter wedge or ball bonds are acceptable for DC Bias connections. Aluminium wire should be avoided. Thermo-compression bonding is recommended though thermo-sonic bonding may be used providing the ultrasonic content of the bond is minimized. Bond force, time and ultrasonic's are all critical parameters. Bonds should be made from the bond pads on the die to the package or substrate. All bonds should be as short as possible.

## Application Circuit



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