## Dual Pair Anti-Parallel Non-Magnetic PIN

$5-400 \mathrm{MHz}$

## Features

- Designed for MRI applications
- Non-Magnetic Surface Mount Package
- Anti-Parallel Self Bias Configuration
- $\mathrm{C}_{\mathrm{T}}=3.0 \mathrm{pF}, \mathrm{R}_{\mathrm{P}}=10 \mathrm{k} \Omega, \mathrm{V}_{\mathrm{B}}=80 \mathrm{~V}$
- > 50 W CW Incident Power Handling @ 400 MHz
- Lead-Free 4 mm 8-lead HQFN Package
- Halogen-Free "Green" Mold Compound
- RoHS* Compliant and $260^{\circ} \mathrm{C}$ Reflow Compatible


## Description

The MADP-011048 acts as a passive switch using silicon PIN diodes in a non-magnetic surface mount package. There are two sets of diode pairs constructed in an anti-parallel configuration that operate from 5 to 400 MHz .

The two pairs of diodes are arranged in an electrically isolated anti-parallel configuration. The diode pair with anode on Pin 1 and cathode on Pin 6 will be referenced as D1 and the diode pair with anode on Pin 5 and cathode on Pin 2 will be referenced as D2.

The MADP-011048 is well suited for MRI passive switching applications. The PIN diodes become a high Q R-C network under small signal and behave as an effective passive rectifier or short circuit under high RF signal to tune and de-tune the resonant MRI tank circuit. The anti-parallel doublet configuration provides efficient power handling.

Ordering Information ${ }^{1,2}$

| Part Number | Package |
| :---: | :---: |
| MADP-011048-TR3000 | 3000 Piece Reel |
| MADP-011048-000SMB | Sample Board |

1. Reference Application Note M513 for reel size information.
2. All sample boards include 5 loose parts.

## Functional Schematic



## Pin Configuration ${ }^{3}$

| Pin No. | Function |
| :---: | :---: |
| 1 | D1 Anode |
| 2 | D2 Cathode |
| 3 | No Connection |
| 4 | No Connection |
| 5 | D2 Anode |
| 6 | D1 Cathode |
| 7 | No Connection |
| 8 | No Connection |
| Paddle $^{4}$ | Ground |

3. MACOM recommends connecting unused package pins to ground.
4. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.
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Electrical Specifications ${ }^{5}$ : $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{Z}_{0}=50 \Omega$

| Parameter | Test Conditions | Units | Min. | Typ. | Max. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Total Capacitance ( $\mathrm{C}_{\mathrm{T}}$ ) | $100 \mathrm{MHz}, 0 \mathrm{~V}$ | pF | - | 3.0 | 4.0 |
| Series Resistance ( $\mathrm{R}_{\mathrm{S}}$ ) | $100 \mathrm{MHz},+10 \mathrm{~mA}$ | $\Omega$ | - | 0.5 | - |
| Parallel Resistance ( $\mathrm{R}_{\mathrm{P}}$ ) | $100 \mathrm{MHz}, 0 \mathrm{~V}$ | $\mathrm{k} \Omega$ | - | 10 | - |
| Reverse Breakdown Voltage | $-10 \mu \mathrm{~A}$ | V | - | 100 | - |
| Forward Voltage | +10 mA | V | - | 0.85 | - |
| Carrier Lifetime | $1 \mathrm{kHz},+10 \mathrm{~mA},-6 \mathrm{~mA}$ | $\mu \mathrm{s}$ | - | 0.2 | - |
| CW Thermal Resistance ( $\Theta_{\mathrm{Jc}}$ ) | (Infinite heat sink at thermal ground plane) | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ | - | 22 | - |
| Insertion Loss | $100 \mathrm{MHz},+10 \mathrm{~mA}$ | dB | - | 0.05 | - |
| Input/output Return Loss | $100 \mathrm{MHz},+10 \mathrm{~mA}$ | dB | - | 30 | - |
| Isolation | $100 \mathrm{MHz}, 0 \mathrm{~V}$ | dB | - | 14 | - |

5. Per diode pair D1 or D2

## Absolute Maximum Ratings ${ }^{6,7}$

| Parameter | Absolute Maximum |
| :---: | :---: |
| CW Incident Power <br> $+50 \mathrm{~mA}, 400 \mathrm{MHz} @ 85^{\circ} \mathrm{C}$ | +51 dBm |
| Reverse Voltage | 80 V |
| $\mathrm{AC}_{\text {RMs }}+$ DC Forward Current <br> (per diode pair D1 or D2) | 3.7 A |
| Power Dissipation <br> (per diode pair D1 or D2) | 4.7 W |
| Junction Temperature ${ }^{8}$ | $+175^{\circ} \mathrm{C}$ |
| Operating Temperature | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| Storage Temperature | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |

6. Exceeding any one or combination of these limits may cause permanent damage to this device.
7. MACOM does not recommend sustained operation near these survivability limits.
8. Operating at nominal conditions with $\mathrm{T}_{\mathrm{J}} \leq+175^{\circ} \mathrm{C}$ will ensure MTTF $>1 \times 10^{6}$ hours.

## Handling Procedures

Please observe the following precautions to avoid damage:

## Static Sensitivity

These devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these class 2 devices.

## Low Power Sample Board (< +20 dBm ${ }^{9}$ )


9. The board is recommended for small signal. For high power operation, heat sink is required.

Parts List: 100-400 MHz

| Part | Value | Case Style |
| :---: | :---: | :---: |
| $\mathrm{C} 1, \mathrm{C} 2, \mathrm{C} 5, \mathrm{C} 6$ | 100 pF | 0402 |
| $\mathrm{C} 3, \mathrm{C} 4, \mathrm{C} 7, \mathrm{C} 8$ | $1 \mu \mathrm{~F}^{10}$ | 0402 |
| Ferrite Bead: <br> FB1,FB2,FB3,FB4 | AC Resistance <br> @ 1000 GHz | 0402 |

10. These values are recommended for $100-400 \mathrm{MHz}$ operation. Increase capacitance to $10 \mu \mathrm{~F}$ for operation below 100 MHz .
11. Recommended part: Murata BLM15HD102SN1

## Application Schematic



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## Typical Performance Curves ${ }^{12}$

Insertion Loss, 10 mA Forward Bias


Insertion Loss, 50 mA Forward Bias


Insertion Loss, 20 mA Forward Bias


Insertion Loss, 100 mA Forward Bias

12. Performance below 100 MHz is limited by sample board bias components.

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## Typical Performance Curves ${ }^{13}$

## Return Loss, 10 mA Forward Bias



Return Loss, 50 mA Forward Bias


## Return Loss, 20 mA Forward Bias



Return Loss, 100 mA Forward Bias

13. Performance below 100 MHz is limited by sample board bias components.

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## Typical Performance Curves ${ }^{14}$

Isolation, 0 V Reverse Bias


Isolation, 40 V Reverse Bias


Isolation, 10 V Reverse Bias


Output Power vs. Incident Power @ 400 MHz CW

14. Performance below 100 MHz is limited by sample board bias components.

## Lead-Free 4 mm 8-Lead HQFN ${ }^{\dagger}$


${ }^{\dagger}$ Reference Application Note S2083 for lead-free solder reflow recommendations. Meets JEDEC moisture sensitivity level 1 requirements.
Plating is $100 \%$ matte tin over copper.

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[^0]:    * Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

