MAXP-37161B

16 Channel, 28 Gbps Crosspoint Switch & Signal Conditioner

Rev V1

Features

- 16-channel Crosspoint Switch with CDR's and Signal Conditioners
- Five-Tap Decision Feedback Equalizer (DFE)
- Adaptive Continuous Time Linear Equalizer (ADCTLE)
- Individual lane LOS (Loss of Signal) detection and squelch
- CDRs support different data rates with a single reference clock
- Integrated Non-Blocking Crosspoint Switches
- Programmable Output Swing with Pre and Post De-Emphasis Levels
- Four Eye Monitors for input jitter diagnostics
- Four PRBS-31 pattern generators and checkers
- Low Power Operation
- Single 1.8 V Power Supply (DV_{DDIO} 3.3V optional for digital interface)
- Extended operating temperature range: -40°C to +85 °C

Applications

- Storage Area Network Switch Fabrics
- Reconfigurable Optical Add-Drop Multiplexer Switch
- Multirate Linecard Redriver & Retimer, Multirate Switch Fabric
- Backplane Signal Conditioning for 100 GE, EDR InfiniBand, 32 G FibreChannel
- Front Panel Retimer for (4x25G) Modules and Copper

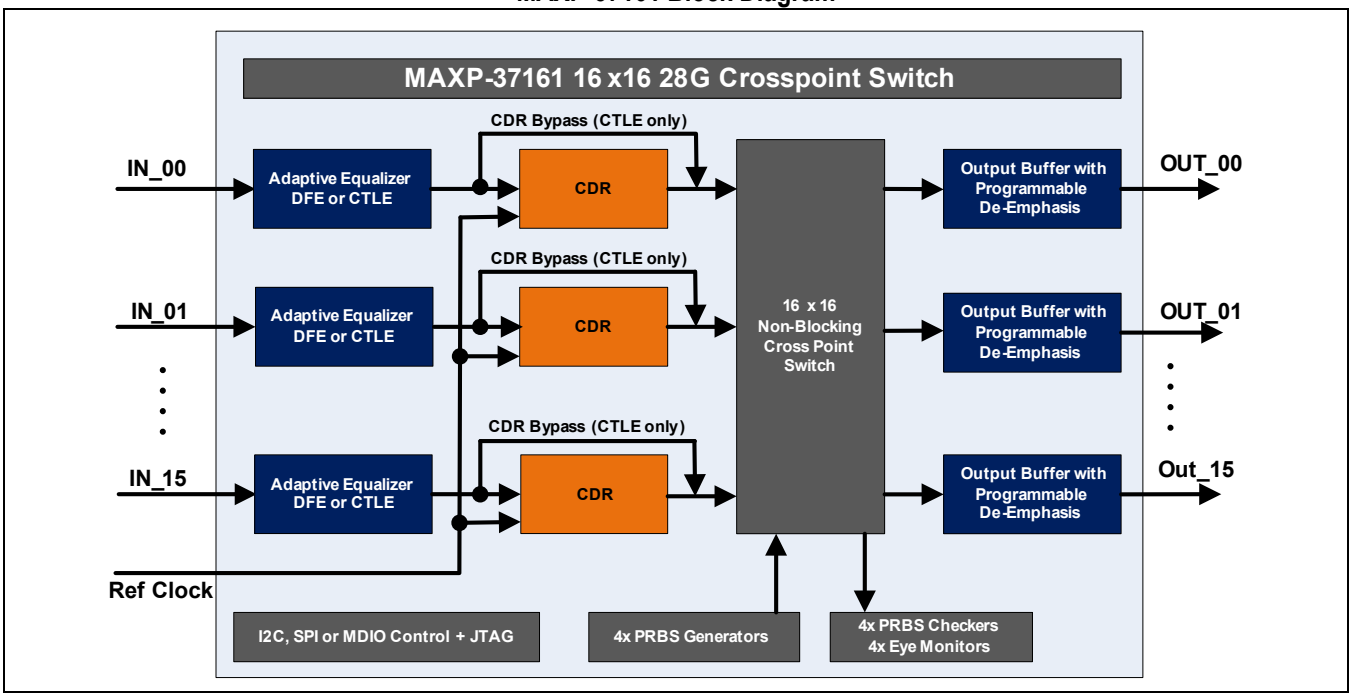
The MAXP-37161 is a highly integrated, low power fully non-blocking crosspoint switch designed to compensate for lossy backplane channels at rates of 100Mbps up to 28.1Gbps. The MAXP-37161 is comprised of a 16-channel crosspoint switch core with CDR's that are able to re-time data rates from 2.4 Gbps up to 28.1 Gbps and thus eliminate residual jitter and provide a clean signal for transmitting to downstream devices.

Each input buffer offers a Decision Feedback Equalization (DFE) or an Adaptive Continuous Time Linear Equalization (ADCTLE) that aids to compensate up to 32 dB of insertion loss at 25.78 Gbps. Each channel can be independently setup to run at different data rates if needed.

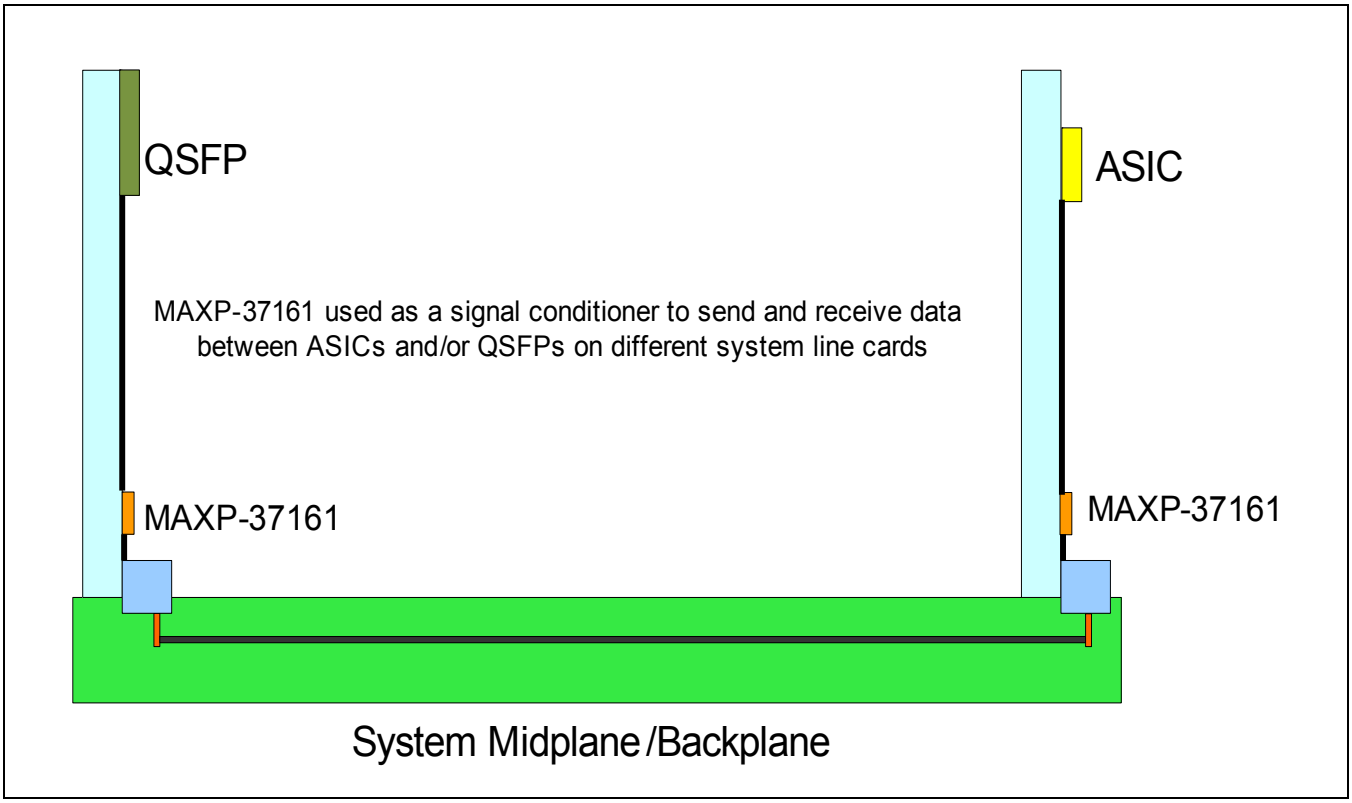
Each output buffer has a three-tap Finite Impulse Response (FIR) filter De-emphasis that help to pre-compensate for channel losses between the MAXP-37161 and any downstream devices. Diagnostic features are also available, including four integrated PRBS generators/checkers and four on-chip eye monitors for in-service link margin evaluation and/or receiver optimization.

The MAXP-37161 can be controlled via a standard two-wire I^2C compatible, four-wire SPI with daisy-chain support and MDIO interface for host control. The MAXP-37161 is packaged in a 196-pin, 15 mm x 15 mm BGA package.

MAXP-37161 Block Diagram



MAXP-37161 Application Diagram



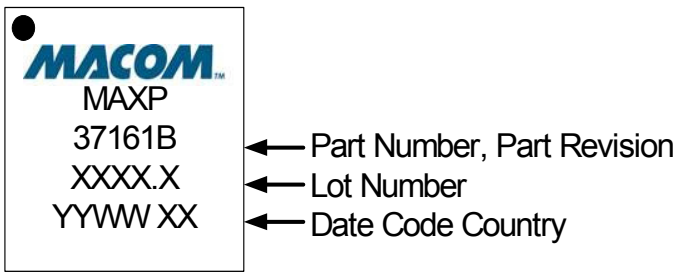
Ordering Information

Part Number	Data Rates Supported	Package	Operating Ambient Temperature
MAXP-37161B	0.1 - 28.1 Gbps	196-pin,15 mm x 15 mm BGA	-40 °C to +85 °C

Revision History

Revision	Level	Date	Description
V1	Release	September 2017	Updated Electrical specifications and typical performance Chapter 1 Updated functional description Chapter 4 Updated register table Chapter 5
V2P	Preliminary	January 2017	Updated Electrical specifications and typical performance Chapter 1 and Chapter 2 Updated functional description Chapter 4 Updated register table Chapter 5
V1P	Preliminary	October 2015	Updated Electrical specifications and typical performance Chapter 1 and Chapter 2 Updated pinout to match Macom's pin naming convention Chapter 3 Updated functional description for digital interfaces Chapter 4 Updated register table Chapter 5
V2A	Advance	April 2015	Adding mechanical info Adding interface detail
V1A	Advance	December 2014	Initial release.

MAXP-37161 Marking Diagram



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1.0 Electrical Characteristics

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
V_{DD}	Core power supply voltage		2.1	V
V_{DDIO}	I/O power supply voltage		3.7	V
V_{IN}	DC input voltage (PCML and CMOS)	V_{SS}-0.5	V_{DD}+0.5	V
T_{STORE}	Storage temperature	-65	150	°C
$V_{ESD, HBM}$	Electrostatic discharge voltage (HBM)	-500	+500	V
$V_{ESD, CDM}$	Electrostatic discharge voltage (CDM)	-2000	+2000	V

Table 1-2. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}	Core power supply voltage	1.71	1.8	1.89	V
V_{DDIO}	I/O power supply voltage	1.71	1.8	3.47	V
T_{CASE}	Operating ambient temperature	-40	25	85	°C
θ_{JC}	Junction to case thermal resistance		0.75		°C/W

NOTES:

Operating temperature at 85 degree C can be achieve with proper cooling recommendations.

Unless noted otherwise, specifications in this section apply to the recommended operation conditions outlined in Table 1-4, Table 1-5, Table 1-6 are PRBS 2^{31} – 1 test pattern at 25.78 Gbps, R_{LOAD} = 100 Ω differential.

Table 1-3. Power Consumption Specifications

Symbol	Parameter			Current (A)		Power (W)	
	Operating Conditions	PRBS Tx/Rx, Eye Monitor	Output Swing (mVppd)	Typical	Max	Typical	Max
PV_{DDIO}	Digital interface at maximum speed. V_{DDIO} = 1.8V.	NA	NA		0.01		0.02
P_{TOTAL}	Standby Mode	NA	NA	0.06	0.09	0.11	0.17
	ADCTLE only, CDR bypassed	Disabled	800	2.6	3.0	4.7	5.7
	ADCTLE + CDR			3.0	3.5	5.3	6.6
	DFE + CDR			3.7	4.4	6.7	8.3
	Maximum power consumption. All channels ON, DFE + CDR, 4x PRBS Generators and 4x Checkers + 4x Eye monitors enabled.	Enabled	800	5.3	6.1	9.5	11.6
			1200	5.4	6.3	9.7	11.8

NOTES:

1. Maximum current and power consumption include a 5% increase on the supply voltage as well as temperature and process variations.

Table 1-4. Input/Output Electrical Characteristics (1 of 2)

Symbol	Parameter		Note	Minimum	Typical	Maximum	Unit
DR	NRZ data rate (CDR enabled)	CDR Enabled		2.4		28.1	Gbps
		CDR bypassed (CTLE only)		0.1		28.1	Gbps
V_{IN}	Differential input swing			200	800	1200	mV_{PPD}
V_{ICM}	Input common-mode voltage			0.3		1.6	V
V_{OUT}	Differential output swing	Range	1	170	800	1200	mV_{PPD}
		800mVppd Setting	1	700	800		mV_{PPD}
		1200mVppd Setting	1	1050	1150		mV_{PPD}
t_R/t_F	Output rise/fall time		2		11	15	ps
V_{OCM}	Output common mode voltage (measured at device pin)					1.9	V
DCD	Output duty cycle distortion	28.10 Gbps				20	mUI
t_{PD}	Propagation delay including lock time	25.78 Gbps				13.0	UI
		28.10 Gbps				13.8	UI
t_{SWITCH}	Crosspoint switch time not including locking time				2		ns
t_{SKEW}	Skew within channels of four lanes					22	ps

Table 1-4. Input/Output Electrical Characteristics (2 of 2)

Symbol	Parameter			Note	Minimum	Typical	Maximum	Unit
J_{TOL}	Input Jitter tolerance		ADCTLE			0.73		UI
			DFE			0.70		UI
t_{DJ}	Output deterministic jitter	10.3125 Gbps	ADCTLE	3, 4		95	180	mUI
		25.78 Gbps	DFE			190	260	
		28.10 Gbps				195	270	
t_{RJ}	Output random jitter	10.3125 Gbps	ADCTLE	3, 4		6.2	7.7	mUIrms
		25.78 Gbps	DFE			9.0	10.5	
		28.10 Gbps				9.9	11.4	
t_{JIT}	Total output jitter	10.3125 Gbps	ADCTLE	3, 4		190	300	mUI
		25.78 Gbps	DFE			330	425	
		28.10 Gbps				365	450	

NOTES:

1. Output swing programming values range is 170mVppd to 1200mVppd. Default value is 800mVppd.
2. Measured with 1" of PCB trace and 16CID pattern using Macom's Evaluation Module (EVM)
3. Jitter settings include 1E-15 BER and maximum equalization settings to compensate for maximum trace insertion loss. Using a PRBS 2^{15} pattern
4. Reference mode

Table 1-5. Reference Clock Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
REF_{FREQ}	Reference clock frequency		100	312.5	878.125	MHz
$REF_{FREQ-TOL}$	Reference clock frequency tolerance		-100		100	ppm
REF_{ACC}	Reference clock frequency accuracy		-100		+100	ppm
REF_{AMP}	Reference clock input amplitude	1	200	800		mV_{PPD}
REF_{PN}	Reference clock phase noise 100 Hz 1kHz 10kHz 100kHz 1MHz >10MHz				 -105 -115 -125 -130 -145 -150	dBC/Hz

NOTES:

1. Reference clock should be AC-coupled on system board to REF_CLK_P/N pins.

Table 1-6. Digital Interface Input/Output Characteristics

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Unit
V_{IH}	Digital Input logic HIGH		0.75 x V_{DDIO}		V_{DDIO}	V
V_{IL}	Digital Input logic LOW			0	0.25 x V_{DDIO}	V
$V_{IH-3STATE}$	Tri-state input logic HIGH		0.85 x V_{DDIO}		V_{DDIO}	V
$V_{IF-3STATE}$	Tri-state input logic FLOAT		0.25 x V_{DDIO}		0.75 x V_{DDIO}	V
$V_{IL-3STATE}$	Tri-state input logic LOW		0		0.15 x V_{DDIO}	V
V_{OH}	Digital Output Logic HIGH	1	0.8 x V_{DDIO}	V_{DDIO}		V
V_{OL}	Digital Output Logic LOW			0	0.15 x V_{DDIO}	V

NOTES:

1. I_{OH} = 4mA, I_{OL} = -4mA.
2. All digital I/Os are 3.3V tolerant. Open drain outputs can pull up to V_{DDIO}. Other outputs are limited to V_{DDIO} +5%

2.0 Typical Performance Characteristics

Unless otherwise noted, typical performance applies for V_{DD} = 1.8 V, 25 °C ambient temperature, 800 mV_{PP} differential input/output data swing, PRBS 2^{31} – 1 data pattern with BER 1E-15.

Figure 2-1. Typical Eye Diagram at 28.05 Gbps, Using DFE

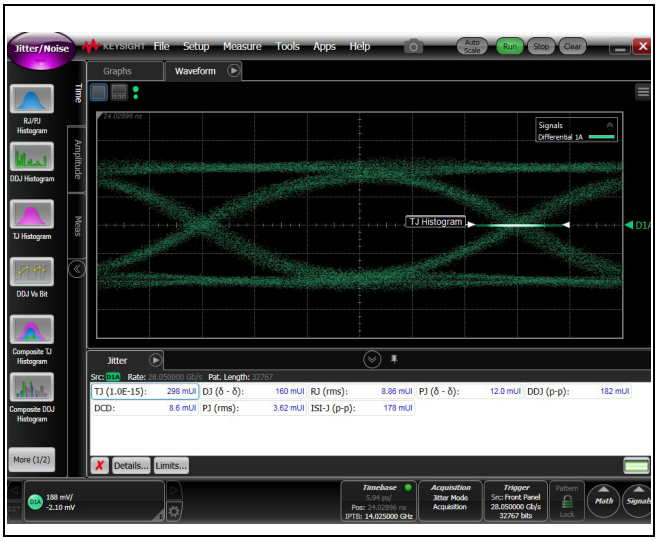


Figure 2-2. Typical Eye Diagram at 14.025 Gbps Using ADCTLE

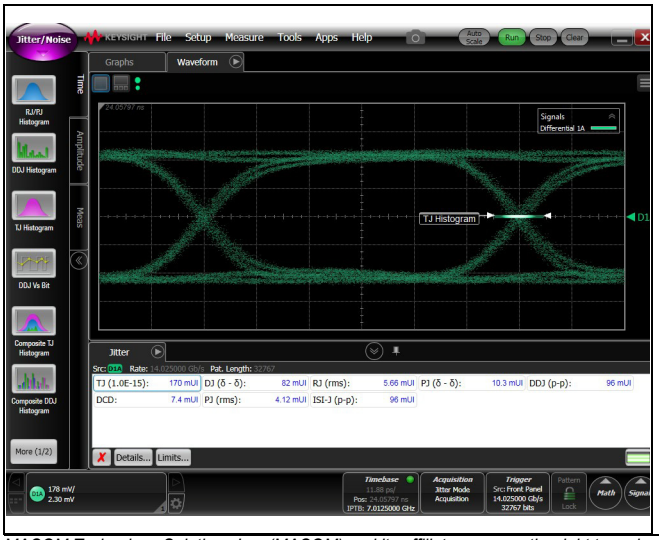


Figure 2-3. Typical Eye Diagram at 25.78 Gbps Using DFE

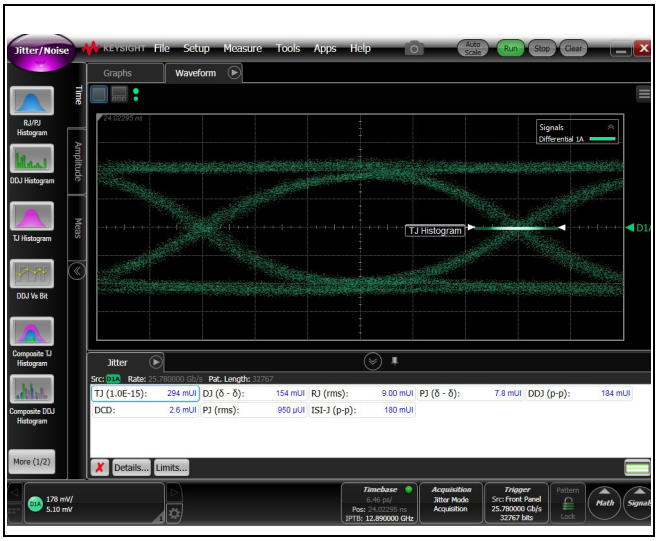
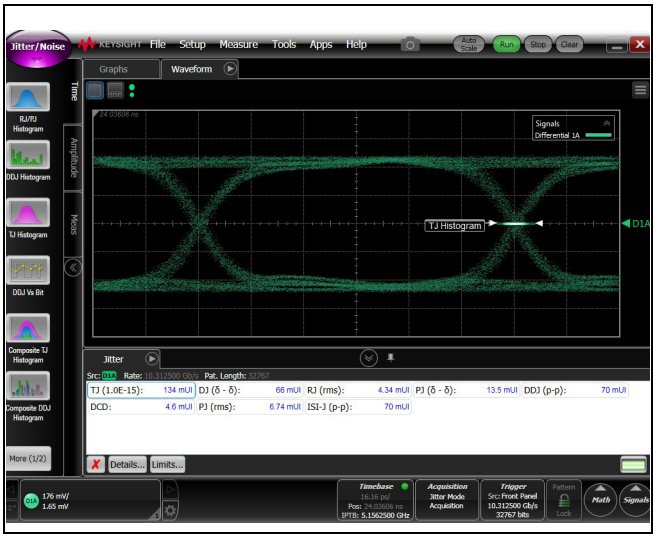


Figure 2-4. Typical Eye Diagram at 10.3125 Gbps Using ADCTLE



3.0 Pinout Diagram, Pin Descriptions, and Package Outline Drawing

Figure 3-1. MAXP-37161 Pinout Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	INP_00	GND	GND	OUTP_00	GND	OUTP_02	GND	OUTP_06	GND	OUTP_07	GND	GND	GND	INP_09
B	INN_00	GND	GND	OUTN_00	GND	OUTN_02	GND	OUTN_06	GND	OUTN_07	GND	GND	GND	INN_09
C	GND	GND	GND	GND	OUTP_01	GND	OUTP_03	GND	OUTP_05	GND	GND	INP_08	GND	GND
D	INP_01	GND	GND	VDD	OUTN_01	VDD	OUTN_03	VDD	OUTN_05	VDD	VDD	INN_08	GND	INP_10
E	INN_01	GND	INP_03	VDD	GND	VDD	GND	OUTP_04	GND	CONFIG0	CONFIG1	GND	GND	INN_10
F	GND	VDD	INN_03	TEST_P	TEST_N	REFCLKP	MF2	OUTN_04	VDD	xRESET	VDD	INP_11	VDD	GND
G	INP_02	VDD	GND	VDD	MF3	REFCLKN	VDDIO	GND	VDD	xALARM	GND	INN_11	GND	INP_13
H	INN_02	GND	INP_04	GND	MF4	VDD	GND	VDDIO	MCLKP	DC_ACB	VDD	GND	VDD	INN_13
J	GND	VDD	INN_04	VDD	xSET	VDD	OUTP_11	MF1	MCLKN	MF0	MF5	INP_12	VDD	GND
K	INP_05	GND	GND	LFIN	LFOUT	GND	OUTN_11	GND	VDD	GND	VDD	INN_12	GND	INP_14
L	INN_05	GND	INP_07	VDD	VDD	OUTP_10	VDD	OUTP_12	VDD	OUTP_14	VDD	GND	GND	INN_14
M	GND	GND	INN_07	GND	GND	OUTN_10	GND	OUTN_12	GND	OUTN_14	GND	GND	GND	GND
O	INP_06	GND	GND	GND	OUTP_08	GND	OUTP_09	GND	OUTP_13	GND	OUTP_15	GND	GND	INP_15
P	INN_06	GND	GND	GND	OUTN_08	GND	OUTN_09	GND	OUTN_13	GND	OUTN_15	GND	GND	INN_15

3.1 Pin Description

Table 3-1. MAXP-37161 16-channel Pinout

Pin Name	Pin Numbers	Pin Type	Pin Function
VDD	D4, D6, D8, D10, D11, E4, E6, F2, F9, F11, F13, G2, G4, G9, H6, H11, H13, J2, J4, J6, J13, K9, K11, L4, L5, L7, L9, L11	Power	Core Voltage Supply (1.8V)
VDDIO	G7, H8	Power	Digital I/O Supply (1.8V up to 3.3V)
VSS	A2, A3, A5, A7, A9, A11, A12, A13, B2, B3, B5, B7, B9, B11, B12, B13, C1, C2, C3, C4, C6, C8, C10, C11, C13, C14, D2, D3, D13, E2, E5, E7, E9, E12, E13, F1, F14, G3, G8, G11, G13, H2, H4, H7, H12, J1, J14, K2, K3, K6, K8, K10, K13, L2, L12, L13, M1, M2, M4, M5, M7, M9, M11, M12, M13, M14, N2, N3, N4, N6, N8, N10, N12, N13, P2, P3, P4, P6, P8, P10, P12, P13	Ground	Device Ground
CONFIG [1:0]	E11, E10	Digital Input Tri-State	Digital Interface selection, (Internal pull- down) LL: I2C interface with EEPROM download HL: I2C interface LF: SPI interface with EEPROM download FL: SPI interface HF: MDIO interface with EEPROM download FH: MDIO interface LH: JTAG interface FF and HH are not used, see Table 4-4
MF0	J10	Digital Input	Multi-Function pins (High-Z) function changes according to digital interface selection using **pin.CONFIG**[1:0] above, see Table 4-4 for more details
MF1	J8	Digital I/O	
MF2	F7	Digital Input	
MF3	G5	Digital I/O	
MF4	H5	Digital Input	
MF5	J11	Digital Input	
xRESET	F10	Digital Input	Master Reset, active low (Internal pull-down)
xSET	J5	Digital Input	Hardware Strobe, (Internal pull-down) Updates the switch configuration depending on the transition: L to H = ISC1 is selected to update ASC H to L = ISC2 is selected to update ASC Software strobe is accessible via **register.xSET_mode**
xALARM	G10	Digital Output	xAlarm output, active low (open drain, external pull-up needed)
DC_ACB	H10	Digital Input Tri-State	High Speed inputs AC or DC coupling selection L = AC Coupling, normal operation F = AC Coupling, device on standby mode H = DC Coupling, normal operation
LFIN	K4	Analog Input	Low Frequency Common-Mode Modulation Input

Table 3-1. MAXP-37161 16-channel Pinout

Pin Name	Pin Numbers	Pin Type	Pin Function
LFOUT	K5	Analog Output	Low Frequency Common-Mode Modulation Output
REFCLKP, REFCLKN	F6, G6	High Speed Input	Reference Clock Inputs Configurable as CMOS or CML via register.**refclk_type**
INP_00, INN_00	A1, B1	High Speed Input	Input Channel 0 Positive/Negative
INP_01, INN_01	D1, E1	High Speed Input	Input Channel 1 Positive/Negative
INP_02, INN_02	G1, H1	High Speed Input	Input Channel 2 Positive/Negative
INP_03, INN_03	E3, F3	High Speed Input	Input Channel 3 Positive/Negative
INP_04, INN_04	H3, J3	High Speed Input	Input Channel 4 Positive/Negative
INP_05, INN_05	K1, L1	High Speed Input	Input Channel 5 Positive/Negative
INP_06, INN_06	N1, P1	High Speed Input	Input Channel 6 Positive/Negative
INP_07, INN_07	L3, M3	High Speed Input	Input Channel 7 Positive/Negative
INP_08, INN_08	C12, D12	High Speed Input	Input Channel 8 Positive/Negative
INP_09, INN_09	A14, B14	High Speed Input	Input Channel 9 Positive/Negative
INP_10, INN_10	D14, E14	High Speed Input	Input Channel 10 Positive/Negative
INP_11, INN_11	F12, G12	High Speed Input	Input Channel 11 Positive/Negative
INP_12, INN_12	J12, K12	High Speed Input	Input Channel 12 Positive/Negative
INP_13, INN_13	G14, H14	High Speed Input	Input Channel 13 Positive/Negative
INP_14, INN_14	K14, L14	High Speed Input	Input Channel 14 Positive/Negative
INP_15, INN_15	N14, P14	High Speed Input	Input Channel 15 Positive/Negative
OUTP_00, OUTN_00	A4, B4	High Speed Output	Output Channel 0 Positive/Negative
OUTP_01, OUTN_01	C5, D5	High Speed Output	Output Channel 1 Positive/Negative
OUTP_02, OUTN_02	A6, B6	High Speed Output	Output Channel 2 Positive/Negative
OUTP_03, OUTN_03	C7, D7	High Speed Output	Output Channel 3 Positive/Negative
OUTP_04, OUTN_04	E8, F8	High Speed Output	Output Channel 4 Positive/Negative
OUTP_05, OUTN_05	C9, D9	High Speed Output	Output Channel 5 Positive/Negative
OUTP_06, OUTN_06	A8, B8	High Speed Output	Output Channel 6 Positive/Negative
OUTP_07, OUTN_07	A10, B10	High Speed Output	Output Channel 7 Positive/Negative
OUTP_08, OUTN_08	N5, P5	High Speed Output	Output Channel 8 Positive/Negative
OUTP_09, OUTN_09	N7, P7	High Speed Output	Output Channel 9 Positive/Negative
OUTP_10, OUTN_10	L6, M6	High Speed Output	Output Channel 10 Positive/Negative
OUTP_11, OUTN_11	J7, K7	High Speed Output	Output Channel 11 Positive/Negative
OUTP_12, OUTN_12	L8, M8	High Speed Output	Output Channel 12 Positive/Negative
OUTP_13, OUTN_13	N9, P9	High Speed Output	Output Channel 13 Positive/Negative

Table 3-1. MAXP-37161 16-channel Pinout

Pin Name	Pin Numbers	Pin Type	Pin Function
OUTP_14, OUTN_14	L10, M10	High Speed Output	Output Channel 14 Positive/Negative
OUTP_15, OUTN_15	N11, P11	High Speed Output	Output Channel 15 Positive/Negative
MCLKP, MCLKN	H9, J9	High Speed Output	Monitor clock differential outputs
TEST0, TEST1	F4, F5	Analog Output	Internal test points, do not connect

1. Pull-up/pull-down resistance is an internal 100 kΩ to DV_{DDIO} or V_{SS}.

3.2 Package Description

The MAXP-37161 is assembled in a 15 x 15 mm BGA package.

Figure 3-2. MAXP-37161 Package Outline Drawing Preliminary (subject to change)

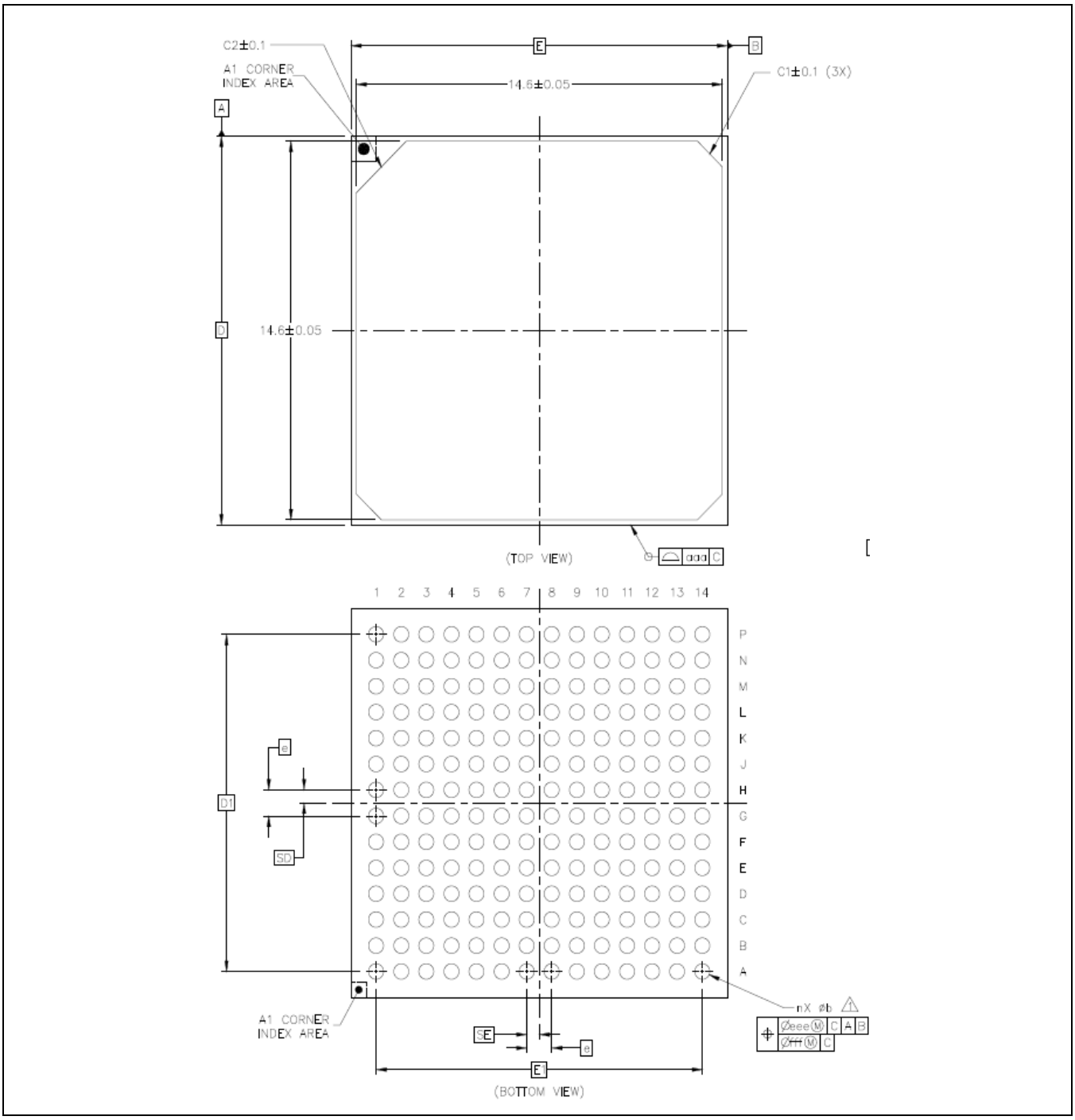
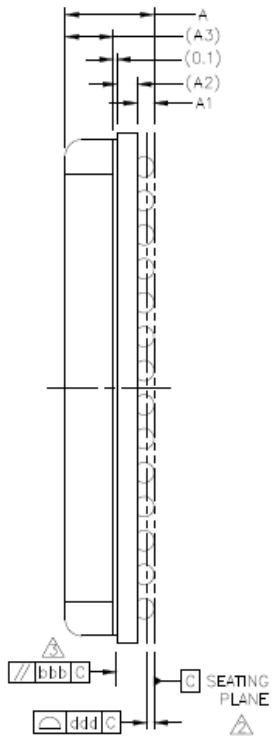


Figure 3-3. MAXP-37161 Package Outline Drawing Preliminary (subject to change)



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	2.88
STAND OFF	A1	0.4	---	0.6
SUBSTRATE THICKNESS	A2		0.62	REF
HEAT SLUG THICKNESS	A3		1.45	REF
BODY SIZE	D		15	BSC
	E		15	BSC
BALL DIAMETER			0.6	
BALL OPENING			0.48	
BALL WIDTH	b	0.5	---	0.7
BALL PITCH	e		1	BSC
BALL COUNT	n		196	
EDGE BALL CENTER TO CENTER	D1		13	BSC
	E1		13	BSC
BODY CENTER TO CONTACT BALL	SD		0.5	BSC
	SE		0.5	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
SUBSTRATE FLATNESS	bbb		0.25	
COPLANARITY	ddd		0.2	
BALL OFFSET (PACKAGE)	eee		0.25	
BALL OFFSET (BALL)	fff		0.1	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

4.0 Functional Description

4.1 General Overview

The MAXP-37161 is a highly integrated, asynchronous 16x16 non-blocking crosspoint switch with signal conditioner designed to compensate for lossy backplane channels at data rates from 2.4Gbps up to 28.1 Gbps.

16 channels divided into 4 slices. Each slice comprise of four receivers, four transmitters, one PRBS generator and one PRBS checker. The non-blocking crosspoint switch configuration is determined by the contents of the Active Switch Configuration (ASC) registers. This register contain the mapping for the source for that particular output. Additionally, there are two Intermediate Switch Configuration (ISC) available that can be loaded into ASC register by a hardware pin.**xSET** or software strobe, thus providing synchronous switching.

Each input buffer has a Decision Feedback Equalization (DFE) or Adaptive Continuous Time Linear Equalization (ADCTLE) are used to compensate up to 32 dB insertion loss at 12.9 GHz / and 30 dB insertion loss at 14 GHz for 25Gbps and 28Gbps applications respectively.

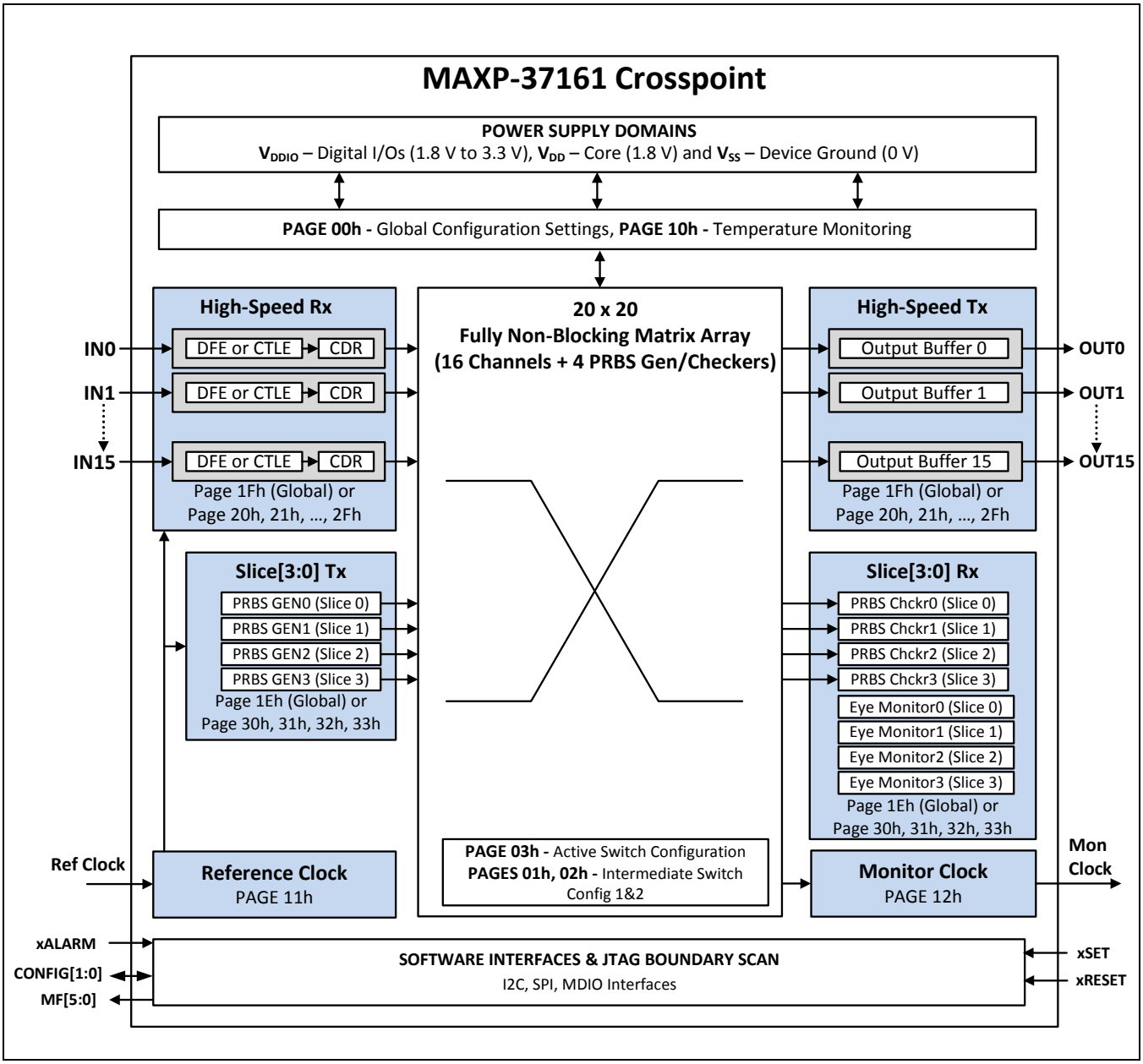
Retiming is used to eliminate any residual jitter and provide a clean signal for transmitting to downstream devices.

Each output buffer has a Three-Tap FIR filter de-emphasis which is used to pre-compensate for channel losses between the MAXP-37161 and downstream devices. In addition, each output buffer can be independently programmed to have up to 1200 mVppd output swing.

The MAXP-37161 supports manual configuration of the input equalizer as well as output driver. Also available are diagnostic features including on-chip eye monitoring, temperature monitoring, and on-chip PRBS generation and checking.

Controlled via a standard two-wire I^2C compatible, four-wire SPI compatible or MDIO interface for host control. The JTAG test interface supports the 1149.6 boundary scan standard (ACJTAG). A functional block diagram of the device is shown in Figure 4-1 below.

Figure 4-1. MAXP-37161 Detailed Functional Block Diagram



4.2 Power Up

4.2.1 Power Supplies

The MAXP-37161 requires two supply voltages, the core power supply V_{DD} = 1.8V and the digital core power V_{DDIO} = 1.8V to 3.3V which offers extended voltage range for flexible interface support.

The power supply for the device should be filtered using typical good practices for PCB design, including using multiple decoupling capacitors with different capacitance values placed close to the device pins, as well as included bulk decoupling capacitors for the power supply.

The MAXP-37161 supports hot plugging for applications where this is needed. When the MAXP-37161 is used in a hot-plug application, the device ground and power connections should be made before any high-speed data connections are made, and the high-speed data connections should be removed before the device power and ground connections are removed. A hardware reset is required after all power supplies are active and stable.

4.2.2 Power Up Sequence

Both V_{DD} and V_{DDIO} can be powered separately or together using a single power supply of 1.8 V (V_{DD} = V_{DDIO}). Although the cross point is designed to support any scenario of power sequencing, it is recommended to power up V_{DDIO} followed by V_{DD} whenever possible.

4.3 High Speed Input Buffers

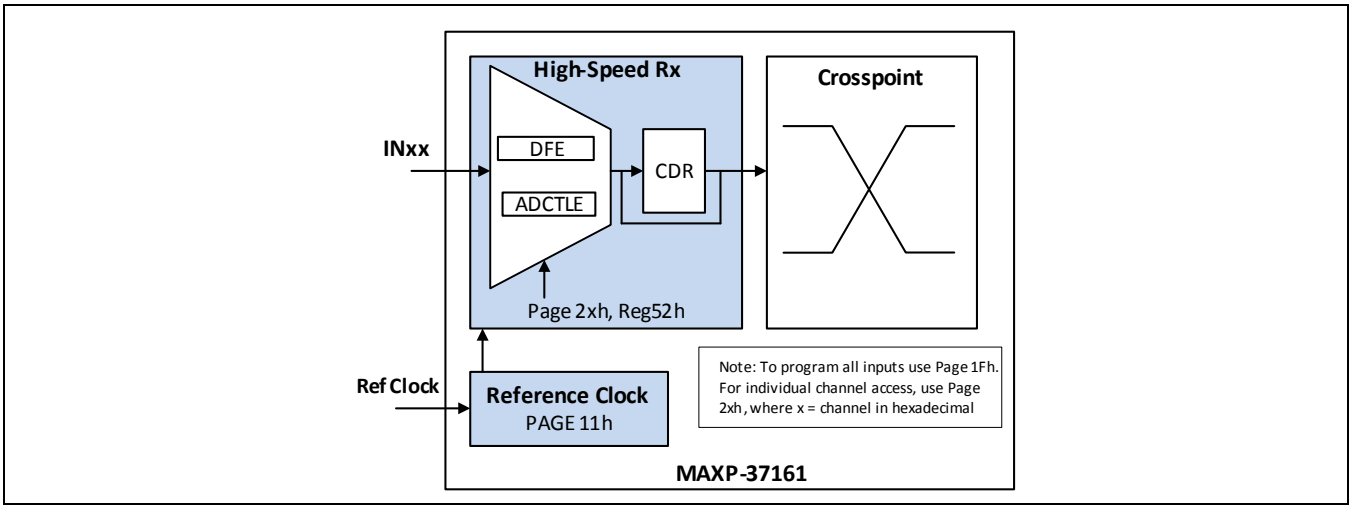
The MAXP-37161 input buffers are high-bandwidth circuits designed to function at data rates from 100Mbps to up to 28.1 G and they include input equalization that was designed to compensate for up to 32 dB of insertion loss at Nyquist frequency of 12.9 GHz for 25Gbps or up to 30 dB of insertion loss at 14 GHz for 28Gbps operation.

Each of the input buffers include on-chip terminations independently of the equalizer selection, they can be AC-coupled or DC-coupled with a wide range of input common mode voltages. If there is a mixture of AC an DC-couple inputs, pin.**DC_ACB** should be set to LOW for AC coupling and for the DC coupled channels, this setting can be overwritten via page 2xh register 92h, bit[6].

Each input channel includes a five-tap DFE (Decision Feedback Equalizer) and a ADCTLE (Adaptive Continuous Time Linear Equalizer) for input equalization. Note that only one equalizer can be used at any given time, either DFE or ADCTLE, but not both.

There are 2 ways to control the input channels: globally and independently. Globally, writing to Page 1Fh will program all 16 inputs, if only one input buffer should be addressed, Pages 20h to 2Fh offer independent programming to each buffer.

Figure 4-2. MAXP-37161 Input Block Diagram



4.3.1 DFE (Decision Feedback Equalizer)

Each input channel includes a five-tap DFE with all of its taps being adaptive. DFE is recommended for data rates higher than 14Gbps because it offers better protection against crosstalk.

Note: If DFE is selected, the CDR cannot be bypassed, the DFE block needs feedback from the CDR to properly work.

After power up or device reset, DFE is selected by default (Page 2xh, register 52h = 00h). There are additional optimization settings after power up that are data rate dependent noted in Table 4-1.

4.3.2 Adaptive CTLE (ADCTLE)

Each input channel includes an ADCTLE (Adaptive Continuous Time Linear Equalizer) for input equalization. The input equalization is fully adaptive, meaning that the equalization coefficients are automatically optimized for each channel. Note that the ADCTLE is recommended for data rates lower than 14Gbps because it consumes less power than the DFE, see Table 1-3 for power consumption.

Note: If ADCTLE is selected, the CDR can be bypassed if desired to save power. For data rates lower than 2.4Gbps, it is recommended to select the ADCTLE with CDR bypassed, this way there will be an active equalization on the incoming signal.

In order to select the ADCTLE, write Page 2xh, register 52h = 40h.

4.3.3 CDR Functionality and Description

The MAXP-37161 includes a CDR for each input channel. The CDR is used to recover the data after equalization and remove any residual jitter after equalization.

After selecting which equalizer to use (DFE or ADCTLE), the correct VCO (Voltage Control Oscillator) and its frequency range should be selected. To lock from 2.4Gbps to 28.1Gbps, the CDR has three VCOs that cover this wide data rate range with help of four dividers as shown Table 4-1, this table also shows the additional CDR optimization registers used (CDR_Reg2 and PLL_Reg2). Notice all the settings on Table 4-1 are data rate dependent.

Table 4-1. MAXP-37161 Data Rate Dependent settings

Data Rate Range (Gbps)	MODE	DFE Optimization		CDR				
	DFE/ADCTLE	DFE Goal	Tap0 Range	VCO Sel	VCO Shift	VCO Divider	CDR_Reg2	PLL_Reg2
	Reg 52h	Reg 15h	Reg 1Ch	Reg 65h	Reg 64h	Reg 62h	Reg 61h	Reg B8h
25.5 - 28.1	00h (DFE)	09h	00h	08h (High)	04h	3Ch (Div1)	00h	47h
22.0 - 25.4		04h	01h	10h (Med)	04h			
19.8 - 21.9					0Ch			
17.3 -19.7		07h		20h (Low)	04h			
14.7 - 17.2					00h			
13.7 - 14.6	40h (ADCTLE)	NA	NA	08h (High)	04h	7Ch (Div2)	20h	40h
12.5 - 13.6					0Ch			
11.3 - 12.4				10h (Med)	04h			
9.9 - 11.2					00h			
8.7 - 9.8				20h (Low)	04h			
7.4 - 8.6					00h			
6.9 - 7.3				08h (High)	04h	BCh (Div4)	30h	
6.25 - 6.8					0Ch			
5.6 - 6.24				10h (Med)	04h			
5.0 - 5.5					00h			
4.3 - 4.9				20h (Low)	04h			
3.7 - 4.2					00h			
3.4 - 3.6				08h (High)	04h	FCh (Div8)		
3.2 - 3.3					0Ch			
2.8 - 3.1				10h (Med)	04h			
2.4 - 2.7					00h			

4.3.3.1 Referenceless Mode

The MAXP-37161 CDRs can be operated in reference-free mode, each CDR is fully independent and can lock to any incoming signal with a data rate from 2.4Gbps up to 28.1 Gbps

NOTES:

- It is strongly recommended to use reference mode until the device is released to production.
- Reference clock is needed for PRBS Generators

4.3.3.2 Reference Mode

The CDRs can operate with a reference clock, in this mode of operation, each CDR uses an integrated PLL that can lock to wide range of frequencies. To enable the reference clock input buffer write Page 11h, reg 00h = 00h and have the reference clock be the source to all slices by writing Page 12h, registers 05h and 06h = 44h. To program PLL to a desired frequency:

1. Select F_{CLOCK}, the reference clock frequency (100 MHz to 312.5 MHz range)
2. Select F_{DATA}, this is the desired frequency for the incoming signal's data rate (2.4GHz to 28.1GHz range)
3. Find the correct VCO (High, Med or Low) and its $VCO_{DIVIDER}$ (1, 2, 4 or 8) for the incoming data rate, Table 4-1
4. Calculate F_{VCO}, $F_{VCO} = F_{DATA} * VCO_{DIVIDER}$
5. Select a reference clock divider ratio, M, between 8 and 511
6. Calculate F_{PFD}, this is the phase and frequency detector $F_{PFD} = F_{CLOCK} / M$
7. Finally, Calculate N, the VCO divider ratio, $N = F_{VCO} / (Divider_{COEFF} * F_{PFD})$. N needs to be rounded off to the closest integer value with a 4 to 4095 range. $Divider_{COEFF}$ = 8 for VCO High and Med and 4 for VCO Low

For an example of a M and N selection we have:

1. F_{CLOCK} = 312.5 MHz
2. F_{DATA} = 10.3125 GHz
3. From Table 4-1, VCO = med and $VCO_{DIVIDER}$ = 2 Table 4-1
4. Then $F_{VCO} = F_{DATA} * VCO_{DIVIDER}$ = 10.3125 GHz * 2 = 20.625 GHz
5. Select a M, **M = 12** which is between 8 and 511
6. Then $F_{PFD} = F_{CLOCK} / M$ = (312.5MHz / 12) = 26.0416 MHz
7. **N =** $F_{VCO} / (Divider_{COEFF} * F_{PFD})$ = 20.625 GHz / (8 * 26.0416 MHz) = **99**

Therefore, for a 10.3125Gbps signal and using a 312.5MHz reference clock the divider coefficients M = 12 and N = 99 should be used. Once the clock divider and VCO divider ratios (M and N) values are calculated, they need to be converted to hexadecimal values and program for each channel Page 2xh registers B5h:B2h.

Notice that given the wide range or M and N values each channel can operate at a different data rate. Table 4-2 offers the recommended M and N values for several different data rates used in the industry.

Table 4-2. MAXP-37161 M and N Dividers for Different Data Rates (1 of 2)

Standard	Industry Standard	Data Rate (Gbps)	Ref Clock (MHz)	VCO	VCO Divider	M	N	Reg B3h:B2h	Reg B5h:B4h
Fibre Channel	32G Fiber Channel Gen6	28.05	312.5	High	1	32	359	0020h	0167h
	16G Fiber Channel Gen5	14.025		High	2	32	359	0020h	0167h
	10G Fiber Channel 66/64 Encoded FEC237	11.6709		Med	2	89	831	0059h	033Fh
	10G Fiber Channel 66/64 Encoded FEC238	11.6218		Med	2	37	344	0025h	0158h
	10G Fiber Channel FEC237	11.318		Med	2	37	335	0025h	014Fh
	10G Fiber Channel FEC235	11.2697		Med	2	63	568	003Fh	0238h
	10G Fiber Channel	10.51875		Med	2	53	446	0035h	01BEh
	8G Fiber Channel	8.5		Low	2	10	136	000Ah	0088h
	4G Fiber Channel	4.25		Low	4	10	136	000Ah	0088h
Ethernet	100G Ethernet	25.78125	312.5	High	1	16	165	0010h	00A5h
	10G Ethernet LAN FEC237	11.0957		Med	2	65	577	0041h	0241h
	10G Ethernet LAN FEC238	11.0491		Med	2	56	495	0038h	01EFh
	10G Ethernet LAN	10.3125		Med	2	12	99	000Ch	0063h
SONET / OTN	10G WAN / OC192 / STM-64 FEC237	10.709225	312.5	Med	2	37	317	0025h	013Dh
	10G WAN / OC192 / STM-64 FEC238	10.6642		Med	2	32	273	0020h	0111h
	10G WAN / OC192 / STM-64	9.95328		Med	2	27	215	001Bh	00D7h
	OC-96	4.97664		Med	4	27	215	001Bh	00D7h
	OC-48 / STM-16	2.488		Med	8	26	207	001Ah	00CFh
Infiniband	EDR	25	312.5	Med	1	12	120	000Ch	0078h
	FDR	14.0625		High	2	12	135	000Ch	0087h
	FDR-10	10.3125		Med	2	12	99	000Ch	0063h
	QDR	10		Med	2	12	96	000Ch	0060h
	DDR	5		Med	4	12	96	000Ch	0060h
	SDR	2.5		Med	8	12	96	000Ch	0060h

Table 4-2. MAXP-37161 M and N Dividers for Different Data Rates (2 of 2)

Standard	Industry Standard	Data Rate (Gbps)	Ref Clock (MHz)	VCO	VCO Divider	M	N	Reg B3h:B2h	Reg B5h:B4h
CPRI	E.238	24.33024	153.6	Med	1	10	198	000Ah	00C6h
	E.119	12.16512		Med	2	10	198	000Ah	00C6h
	E.99	10.1376		Med	2	12	198	000Ch	00C6h
	E.96	9.8304		Low	2	12	384	000Ch	0180h
	E.60	6.144		Med	4	12	240	000Ch	00F0h
	E.48	4.9152		Low		12	384	000Ch	0180h
	E.30	3.072		Med		12	240	000Ch	00F0h
	E.24	2.4576		Low		12	384	000Ch	0180h

Note:

Additional registers are needed to be written to have the optimum performance, namely, VCO Shift (Reg 64h), CDR_Reg2 (Reg 61h) and PLL_Reg2 (Reg62h). See Table 4-1 for more details

4.4 Cross Point Switch Configuration

On power up the crosspoint configuration follows the ASC register (Page 03h) default values, if needed the ASC registers can be programmed by the EEPROM download

There are three methods of changing and/or updating the switch matrix configuration:

- The direct ASC mode. The ASC register contains the current crosspoint configuration. The switch configuration can be changed directly by programming the desired switching path on to Page 03h.
- The hardware strobe mode, using hardware pin.**xSET** and selectively loading one of two pre-determined switching maps (ISC1 or ISC2). ISC1 is selected if pin.**xSET** is toggled from LOW to HIGH, similarly, ISC2 is selected if pin.**xSET** is toggled from HIGH to LOW.
- The software strobe mode, using reg.**swstrobe** (Page 00h, register 03h, bits[5:0] and selectively loading one of two pre-determined switching maps (ICS1 or ICS2) using bit[7].

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4.5 High Speed Output Buffers

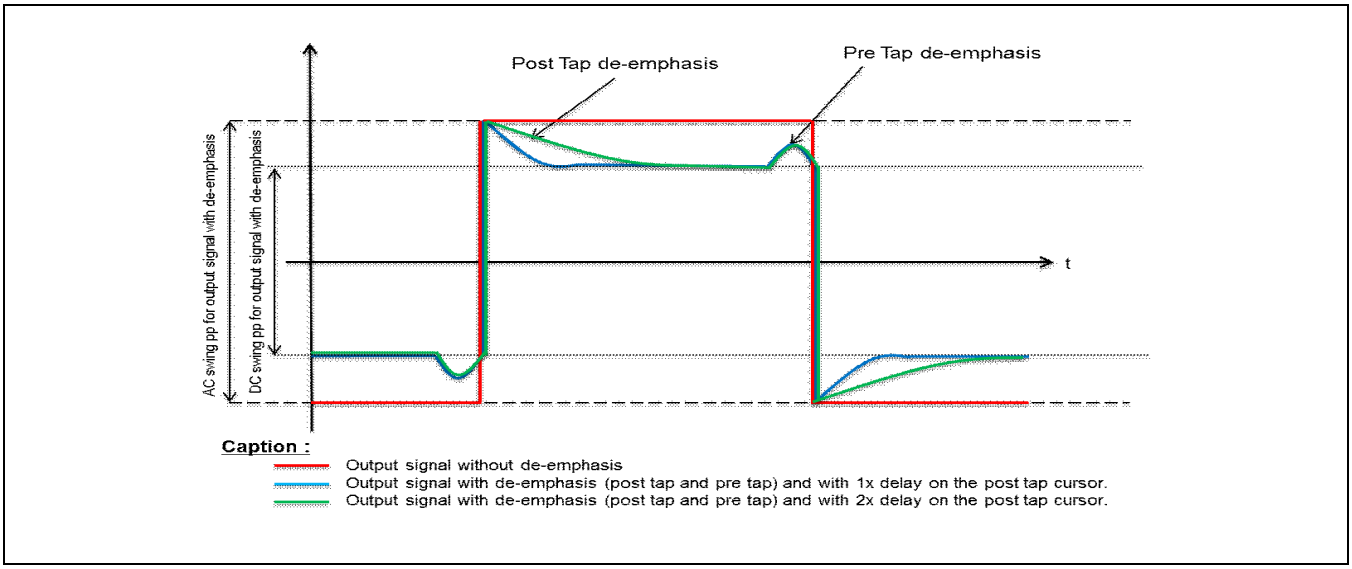
The MAXP-37161 output buffers are high-bandwidth circuits designed to function at data rates up to 28.1 Gbps. The output buffers have programmable settings for swing as well as pre and post tap de-emphasis levels. The output buffers can be individually or globally powered down if desired, and will revert to a high impedance state when disabled.

The MAXP-37161 output drivers are designed with three-tap FIR filter to pre-compensate any channel impairment between MAXP-37161 and downstream devices.

- The main tap output swing is programmable from 170 mV_{PPD} to 1200 mV_{PPD} in 16 mV steps.
- Pre-cursor de-emphasis is programmable from 0 dB to 4 dB in 0.13 dB steps.
- Post-tap de-emphasis is programmable from 0 dB to 12 dB in 0.4 dB steps.

The output buffers are programmed on a per-channel basis and are configured using device registers.

Figure 4-3. De-emphasis Correction



4.6 Diagnostics

There are 2 ways to control the four slices: globally and independently. Globally, writing to Page 1Eh will program all 4 slices, if only one slice should be addressed, Pages 30h to 33h offer independent programming to each slice.

4.6.1 PRBS Generators

There four pattern generators, one per slice. Each generator is capable to have a PRBS-9 or PRBS-31 pattern. Just like the input buffers, the generators have to be programmed with the correct VCO selection (Page 3xh Reg0Ah), VCO divider (Page 3xh Reg08h) and VCO shift (Page 3xh Reg09h) to support a particular data rate. These data rate dependent settings are listed on Table 4-1.

Procedure to start PRBS Gen0 to Output 09, PRBS31 pattern running at 25.78125Gbps:

1. Select the clock source. Page 12h, registers 05h and 06h, write 44h to select the reference clock for all generators.
2. Select the VCO, Page 1Eh, register 0Ah = 08h to select VCO high for all generators.
3. Select the VCO divider, Page 1Eh, register 08h = 00h to select VCO divider by1 for all generators.
4. Select the VCO shift, Page 1Eh, register 09h = 04h to select VCO shift for optimization purposes.
5. Select M and N dividers. For 25.78125Gbps and 312.5MHz Reference Clock, M = 16, N = 165:
   - Page 1Eh, register 00h = 10h. // M divider value
   - Page 1Eh, register 01h = 00h.
   - Page 1Eh, register 02h = A5h. // N divider value
   - Page 1Eh, register 03h = 00h.
6. Select PRBS Gen0 to Output 09, Page 03h, register 09h = 10h.
7. To reset and start pattern generator:
   - Page 30h, register 23h = 18h. // Reset PRBS Gen0
   - Page 30h, register 23h = 18h. // Start PRBS Gen0

Note: In this example, all the PRBS generators were programmed to work at the same data rate using the global slicer control page 1Eh. If different data rates for different generators is needed use pages 30h to 33h instead.

4.6.2 PRBS Checkers

There four PRBS checkers, one per slice. Each checker is capable to track bit errors in a PRBS-31 pattern. Just like the input buffers, the generators have to be programmed with VCO selection (Page 3xh Reg3Ch), VCO divider (Page 3xh Reg3Ah) and VCO shift (Page 3xh Reg3Bh). The PRBS generator and checker share these settings per slice. If a different data rate from the PRBS generator is needed in the checker, use another slice.

Procedure to use PRBS checker1 on Input 09, PRBS31 pattern incoming at 25.78125Gbps:

1. Select the clock source. Page 12h, registers 05h and 06h, write 44h to select the reference clock for all generators.
2. Select reference mode, Page 1Eh, register 42h = 40h for all generators.
3. Select the VCO, Page 1Eh, register 3Ch = 08h to select VCO high for all generators.
4. Select the VCO divider, Page 1Eh, register 3Ah = 00h to select VCO divider by1 for all generators.
5. Select the VCO shift, Page 1Eh, register 3Bh = 04h to select VCO shift for optimization purposes.
6. Select M and N dividers. For 25.78125Gbps and 312.5MHz Reference Clock, M = 16, N = 165:
   - Page 1Eh, register 32h = 10h. // M divider value
   - Page 1Eh, register 33h = 00h.
   - Page 1Eh, register 34h = A5h. // N divider value
   - Page 1Eh, register 35h = 00h.
7. Select Input 09 to PRBS CKR0, Page 03h, register 10h = 09h.
8. To reset checker0:
   - Page 30h, register 43h = 41h. // Reset PRBS Gen0
   - Page 30h, register 43h = 40h. // PRBS Gen0 normal operation
   - Page 30h, register 22h = 7Ah. // PRBS Gen0 counter reset1. Note polarity flip may be needed see bit [2]
   - Page 30h, register 23h = 03h. // PRBS Gen0 counter reset2.
   - Page 30h, register 25h = 07h. // PRBS Gen0 manual delay.
   - Page 30h, register 22h = 0Ah. // Checker starts
9. To read bit errors
   - Page 30h, register 29h. // MSB
   - Page 30h, register 2Ah. // LSB

Note: In this example, all the PRBS checkers were programmed to work at the same data rate using the global slicer control page 1Eh. If different data rates for different generators is needed use pages 30h to 33h instead.

4.6.3 Temperature Monitor

A temperature monitor is included in the MAXP-37161 to give an indication of the internal die temperature. A code can be read from the device registers which gives an indication of the internal die temperature. Since every system has different power dissipation, a temperature calibration is required to have accurate temperature readings.

4.6.3.1 Temperature Monitor Readings

By default, the temperature monitor is already enabled. To read the current temperature, a temperature monitor strobe must be performed first to update the temperature read register.

1. Reset the temperature monitor by writing 1b to Page10h, register00h, bit[5]
2. Strobe or update the temperature reading by writing 1b to Page10h, register00h, bit[6].
3. Read the monitor temperature Page10h, register04h, bit[7:0].

4.6.3.2 Temperature Monitor Alarms

By default, the temperature monitor alarms are also enabled. There are two types of alarms:

1. Temp alarm status, Page10h, register FCh, bit[1]. This bit will stay 0b as long as the temperature read by the device is lower than the alarm threshold high, Page10h, register01h, bit[5:0]. If the temperature crosses this threshold, then Page10h, register FCh, bit[1] = 1b.
2. Temp alarm flag, Page10h, register FCh, bit[0]. This bit will stay 0b as long as there are no changes on the temperature alarm status. This alarm is meant to track changes of temperature crossing the alarm threshold. To clear this alarm, simply write 1b to Page10h, register FCh, bit[0].

4.6.3.3 Temperature Monitor Calibration Procedure

In order to calibrate the temperature monitor, the device has to be placed in standby mode and a thermo couple should be used to measure the case temperature.

Using a forced temperature unit or thermal chamber, set a desired temperature, read both the device temperature monitor and the case temperature as read by the thermo couple. Using a MAXP-37161 Evaluation Module (EVM). The following readings were obtained:

Table 4-3. Temperature Calibration Readings for MAXP-37161 Evaluation Module (EVM)

Forced Case Temp	Temp Monitor Reading		Alarm Threshold Setting	
	hex	decimal	hex	decimal
+25C	5Ch	92	NA	NA
+50C	75h	117	03h	03
+75C	91h	145	0Ah	10
+100C	ACh	172	10h	16
Notes: Additional readings are found in Chapter 5, Page10h, register 01h and register 04h EVM fan was disabled.				

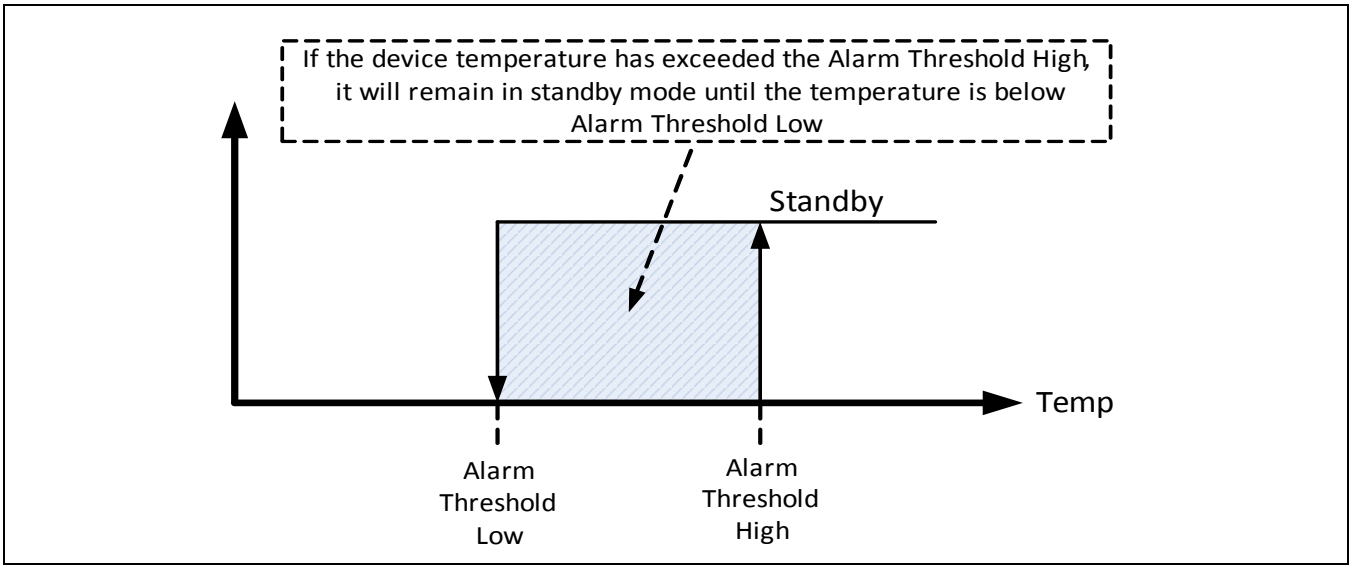
Subtracting the measured temperature from the monitor reading, in average, the monitor temperature offset is ~70C. Therefore, once the system is in normal operation, the device case temperature is approximately equal to the monitor temperature minus 70C for Macom's MAXP-37161 EVM.

For the alarm threshold, as the temperature monitor was calibrated, the temperature alarm status register (page10h, register FCh, bit[1]) was used to determined at what temperature this bit was changing. Table 4-3 reflects those readings.

4.6.3.4 Over Temperature Auto Shutdown

If desired, the MAXP-37161 can be automatically placed in standby mode if the temperature exceeds the alarm threshold high, Page10h register 01h, bit[5:0]. In this mode of operation, the device will remain in standby mode until the temperature falls below the alarm threshold low, Page10h register 08h, bit[5:0]. By default, after power up or device reset, this feature is disabled, to enable the over temperature auto shutdown Page10h register 08h, bit[7] should be set to 1b..

Figure 4-4. Over Temperature Auto Shutdown Operation



4.7 Control Interfaces

The registers of the MAXP-37161 can be configured through different control interfaces:

- I2C or 2-wire serial interface.
- SPI or 4-wire serial interface.
- MDIO or Management Data I/O.

In general, pin.**V_{DDIO}** should share the same power supply as the host controller. The crosspoint supports host controller voltages of 1.8 V, 2.5 V, and 3.3 V. The registers are defined to allow a select number of parameters to be configured individually (per lane or group) or globally. With the global option, selection of a feature will apply to all lanes of the device. If the individual option is selected, then each lane or group can be configured individually. Global configuration is faster but individual configuration allows for more flexibility and customization.

There are two hardware pins - pin.**CONFIG[1:0]** which allow the user to select the control interface and define the function of the multi-functions pins, pin.**MF[5:0]**, as summarized in Table 4-4.

The interface selection is not latched upon the power on reset of the part, or after a hardware reset, and can be changed during operation. This means that assertion of the software reset will not reset the interface selection. The physical logic level of the control interface (and all low-speed digital I/O pins in general) is determined by the supply voltage seen at pin.**V_{DDIO}**.

In the following sections, the pins of the selected interface will be referred to by the assigned name in quotes. For example, pin.**MF0** for the 4-wire interface will be called "**SCLK**".is controlled through an I^2C compatible 2-wire programming interface, SPI compatible 4-wire programming or MDIO interface.

Table 4-4. Digital Interface - Pin Descriptions

Control Pins	Control Selected Interface							Type/Termination
	I2C		SPI		MDIO		JTAG	
	EEPROM	Normal	EEPROM	Normal	EEPROM	Normal		
CONFIG1	LOW	HIGH	LOW	FLOAT	HIGH	FLOAT	LOW	Input / Pull-down[1]
CONFIG0	LOW	LOW	FLOAT	LOW	FLOAT	HIGH	HIGH	Input / Pull-down[1]
MF5	A3		See Note 2		A3			Input / High-Z
MF4	A2				A2		TRSTn	Input / High-Z
MF3	A1		xCS		A1		TDO	I_O / High-Z
MF2	A0		SI		A0		TDI	Input / High-Z
MF1	SDA[3]		SO		MDIO		TMS	I_O / High-Z[3]
MF0	SCL[3]		SCLK		MDC		TCK	Input / High-Z[3]

NOTES:

1. Pull-up/pull-down resistance is an internal 100 kΩ to DV_{DDIO} or V_{SS}.
2. MF[5:4] = 00 EEPROM requires 1 address offset byte. MF[5:4] = 01 = EEPROM requires 2 address offset bytes
3. Needs an external pull-up for I2C interface.

4.7.1 I2C Interface

The two-wire interface supports up to 400 kHz programming modes. The maximum capacitance that the SDA pin can drive when configured as an output is 400 pF @100 kHz and 100 pF @400 kHz. The CMOS I/O are 3.3V tolerant. For details on the register interface, please refer to the I^2C programming bus standard.

Figure 4-5. I2C Bit Operations

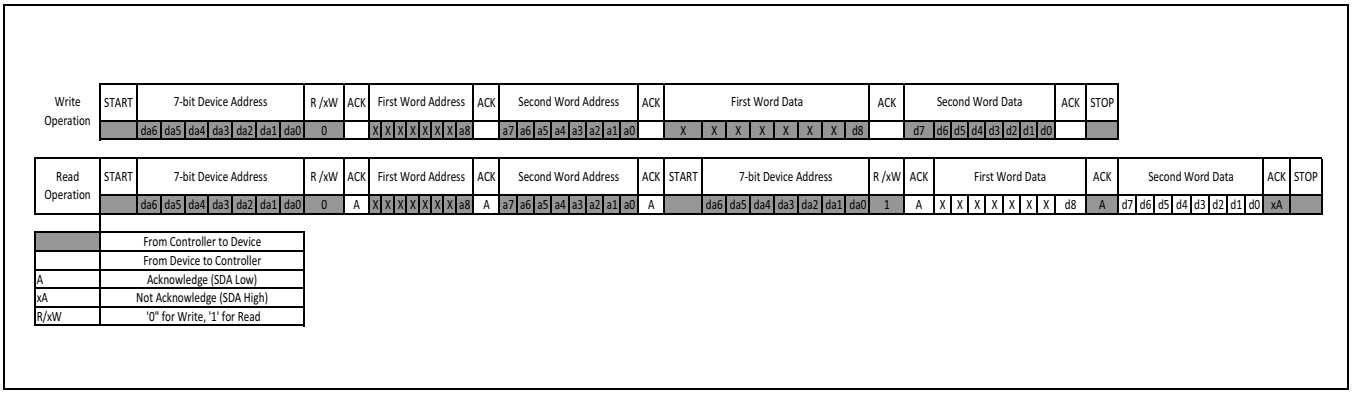
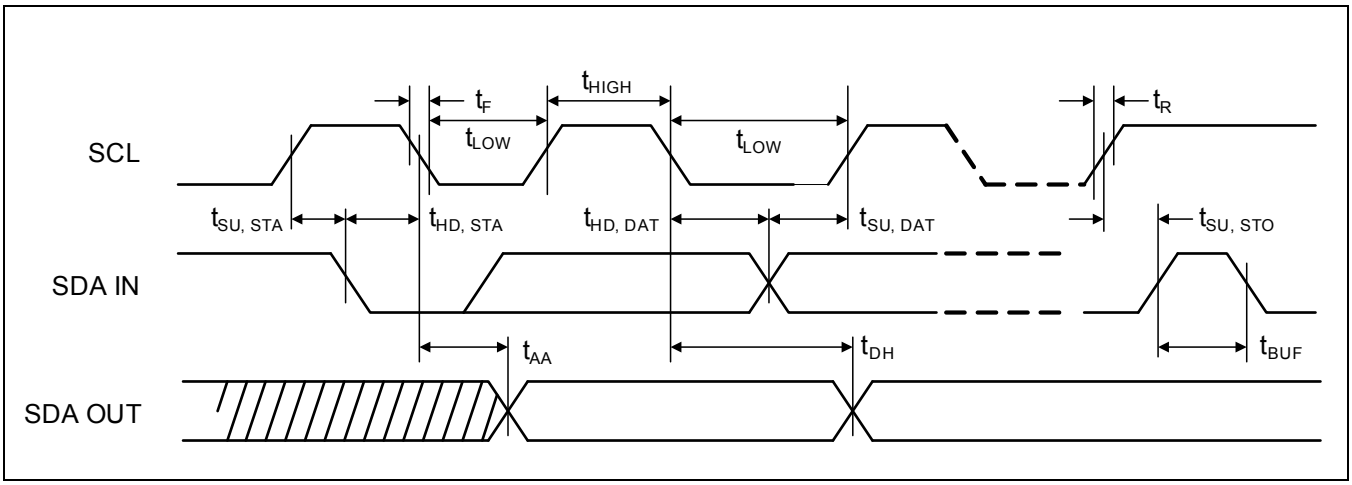


Figure 4-6 illustrates typical waveforms and timing seen at pin.**SCL** and pin.**SDA** for a Read and Write operation.

Figure 4-6. I2C Read and Write Operation Timing Diagram



In I2C Mode, the multi-function pin.**MF[5:2]** are I2C address for the device. Each of these pins can be configured three ways: tied low (0), tied high (1), or left floating (F). The valid addresses are listed in the Table 4-5 below.

Table 4-5. I2C Mode Multi-function Pins

MF[5:2]	I2C Address	MF[5:2]	I2C Address	MF[5:2]	I2C Address	MF[5:2]	I2C Address
FFFF	40h[1]	0F10	68h	11F0	90h	F00F	B8h
0000	40h[2]	0F11	6Ah	11F1	92h	F01F	BAh
0001	42h	0FF0	6Ch	110F	94h	F0FF	BCh
0010	44h	0FF1	6Eh	111F	96h	F100	BEh
0011	46h	0F0F	70h	11FF	98h	F101	C0h
00F0	48h	0F1F	72h	1F00	9Ah	F110	C2h
00F1	4Ah	0FFF	74h	1F01	9Ch	F111	C4h
000F	4Ch	1000	76h	1F10	9Eh	F1F0	C6h
001F	4Eh	1001	78h	1F11	A0h	F1F1	C8h
00FF	50h	1010	7Ah	1FF0	A2h	F10F	CAh
0100	52h	1011	7Ch	1FF1	A4h	F11F	CCh
0101	54h	10F0	7Eh	1F0F	A6h	F1FF	CEh
0110	56h	10F1	80h	1F1F	A8h	FF00	D0h
0111	58h	100F	82h	1FFF	AAh	FF01	D2h
01F0	5Ah	101F	84h	F000	ACh	FF10	D4h
01F1	5Ch	10FF	86h	F001	AEh	FF11	D6h
010F	5Eh	1100	88h	F010	B0h	FFF0	D8h
011F	60h	1101	8Ah	F011	B2h	FF01	DAh
01FF	62h	1110	8Ch	F0F0	B4h	FF0F	DCh
0F00	64h	1111	8Eh	F0F1	B6h	FF1F	DEh
0F01	66h						

Notes:
1. Use this code when EEPROM require 2 address offset bytes
2. Use this code when EEPROM require 1 address offset byte

Table 4-6. I2C Interface Specifications (Standard and Fast Modes)

Timing Symbol	Description		Standard-Fast Mode		Units
			Min	Max	
f_{SCL}	Clock Frequency, SCL		–	400	KHz
t_F	Fall time for both SDA and SCL		–	300	ns
t_R	Rise time for both SDA and SCL		–	300	ns
t_{LOW}	Clock Pulse Width Low		1.3	–	µs
t_{HIGH}	Clock Pulse Width High		0.6	–	µs
t_{AA}	Clock Low to Data Out Valid		0.05	0.9	µs
$t_{HD,STA}$	Start Hold Time		200	–	ns
$t_{SU,STA}$	Start Set-up Time		200	–	ns
$t_{HD,DAT}$	Data In Hold Time		0	–	ns
$t_{SU,DAT}$	Data In Set-up Time		100	–	ns
$t_{SU,STO}$	Stop Set-up Time		200	–	ns
t_{DH}	Data Out Hold Time		50	–	ns
t_{BUF}	Bus free time between a STOP and START condition	Standard Mode	4.7	–	µs
		Fast Mode	1.3	–	µs

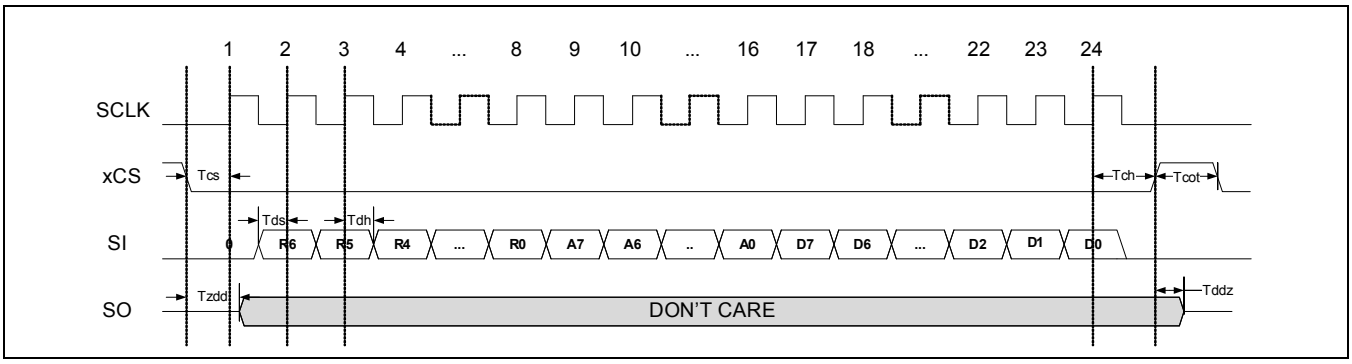
4.7.2 SPI Interface

The SPI interface provides a high-speed means of accessing internal registers. This interface is design to work up to 20MHz.

4.7.2.1 SPI Write

Figure 4-7 illustrates the Serial Write Mode. To initiate the 24-bit long write sequence, **xCS** is driven low before the rising edge of **SCLK.** On each rising edge of the clock, the 24 bits consisting of 1-bit R/xW = 0 for write, 7 reserved bits, ADDR (8-bit) and DATA (8-bit), are latched into the input shift register through **SI**. After the last data bit is sent, **xCS** must be driven high to complete the write operation.

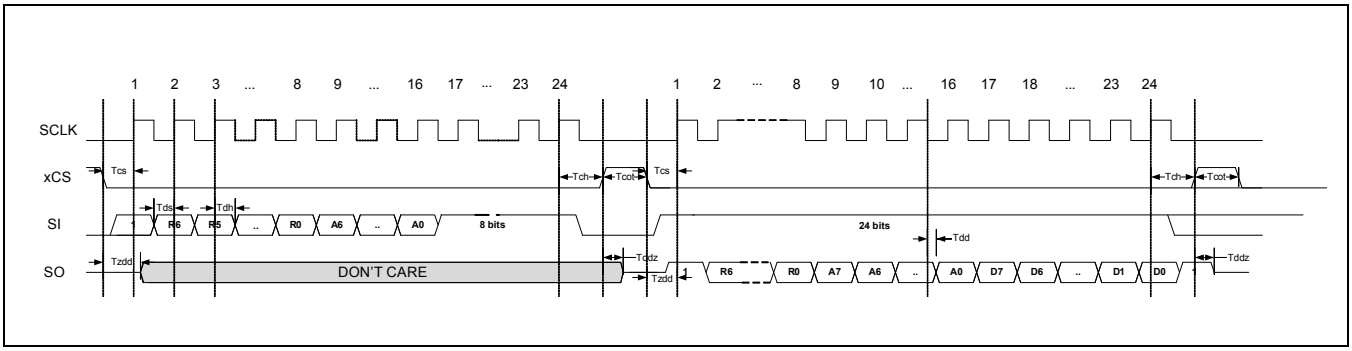
Figure 4-7. SPI Serial WRITE Timing Diagram



4.7.2.2 SPI Read

Figure 4-8 illustrates the Serial Read Mode. To initiate the 48-bit long read sequence, **xCS** is driven low before the rising edge of **SCLK.** On each rising edge of the clock, the first 24 bits consisting of 1-bit R/xW = 1 for read, 7 reserved bits, ADDR (8-bit) and dummy DATA (8 x “1” bits), are latched into the input shift register through **SI**. After the 24th bit is sent, **xCS** must be toggled to start the second part of the operation. The second set of 24 x “1” bits are latched into the input shift register through **SI** while the register address and data requested in the first part of the read transaction are shifted out on **SO** on the failing edge of the clock. Finally, **xCS** must be driven high to complete the read operation.

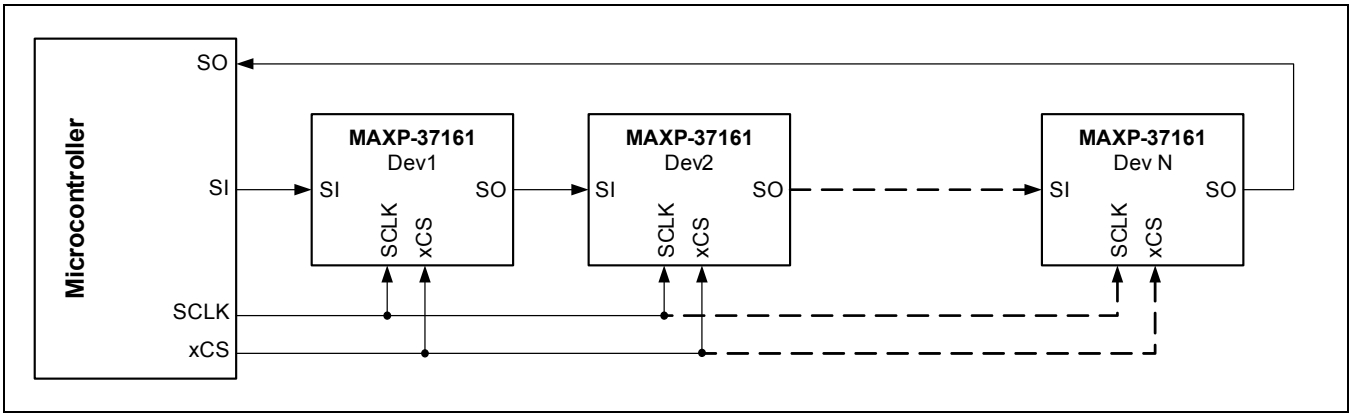
Figure 4-8. SPI Serial READ Timing Diagram



4.7.2.3 SPI Interface Daisy Chain

The SPI interface supports daisy chain for an unlimited number of devices as shown in Figure 4-9. Daisy chain operation provides an architectural advantage in that only one **xCS** and **SCLK** pin is required on the host, as well as one **SO** and one **SI** pin irrespective of the number of devices. The **SO** data of each device shifts into the next device **SI**.

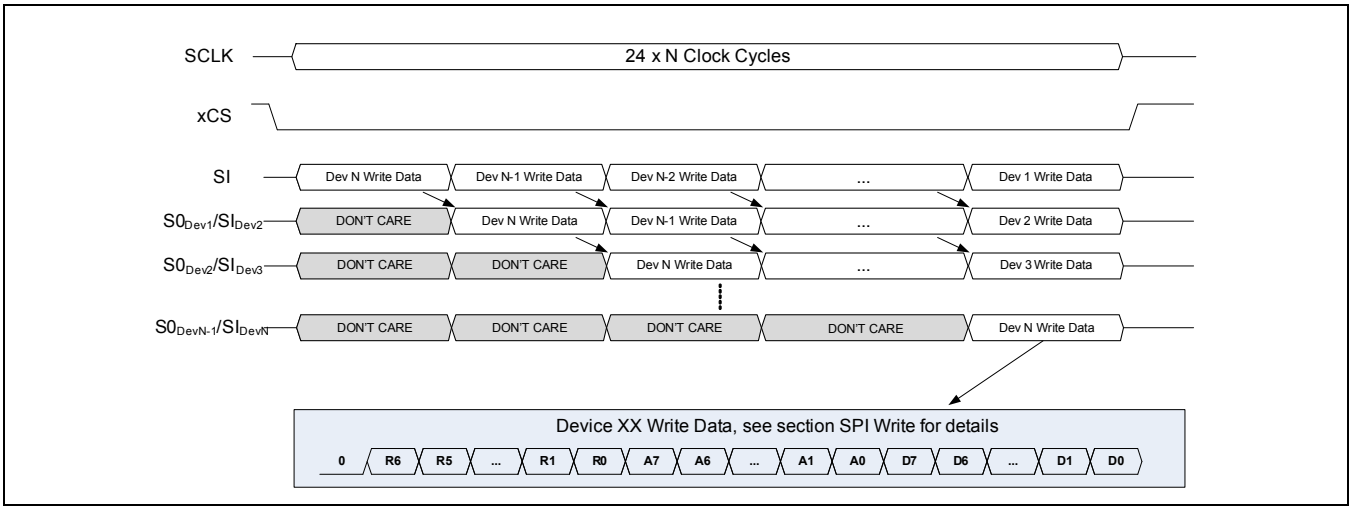
Figure 4-9. SPI Interface, Daisy Chain Configuration



4.7.2.4 SPI Interface Daisy Chain - Write

Figure 4-10 illustrates the SPI write operation for a daisy chain architecture consisting of N devices. To initiate the (24 x N)-bit long write sequence, **xCS** is driven low before the first rising edge of **SCLK.** The difference in the daisy chain configuration is that **xCS** remains low for (24 x N) clock cycles, where the 24-bit write operation block consists of 1-bit R/xW = 0 for write, 7 reserved bits, ADDR (8-bit) and DATA (8-bit) as described in **Section 4.7.2.1**. At the beginning of the last 24-bit block, each device receives the appropriate data to be written on its register table. Finally, **xCS** must be driven high to complete the write operation.

Figure 4-10. 4-wire Serial Interface, Daisy Chain Write Timing Diagram



4.7.2.5 SPI Interface Daisy Chain - Read

Figure 4-11 illustrates the SPI read operation for a daisy chain architecture consisting of N devices. To initiate the (48 x N)-bit long read sequence, **xCS** is driven low before the first rising edge of **SCLK.** The difference in the daisy chain configuration is that **xCS** remains low for (24 x N) clock cycles to send the appropriate read data to each device, where the 16-bit read operation block consists of 1-bit R/xW = 1 for read, 7 reserved bits, ADDR (8-bit) and DATA (8-bit) as described in Section 4.7.2.2.

The second set of (24 x N) "1" bits are latched into the input shift register through **SI** while the register address and data requested in the first part of the read transaction are shifted out on **SO.** Finally, **xCS** must be driven high to complete the write operation.

Figure 4-11. 4-wire Serial Interface, Daisy Chain Read Timing Diagram

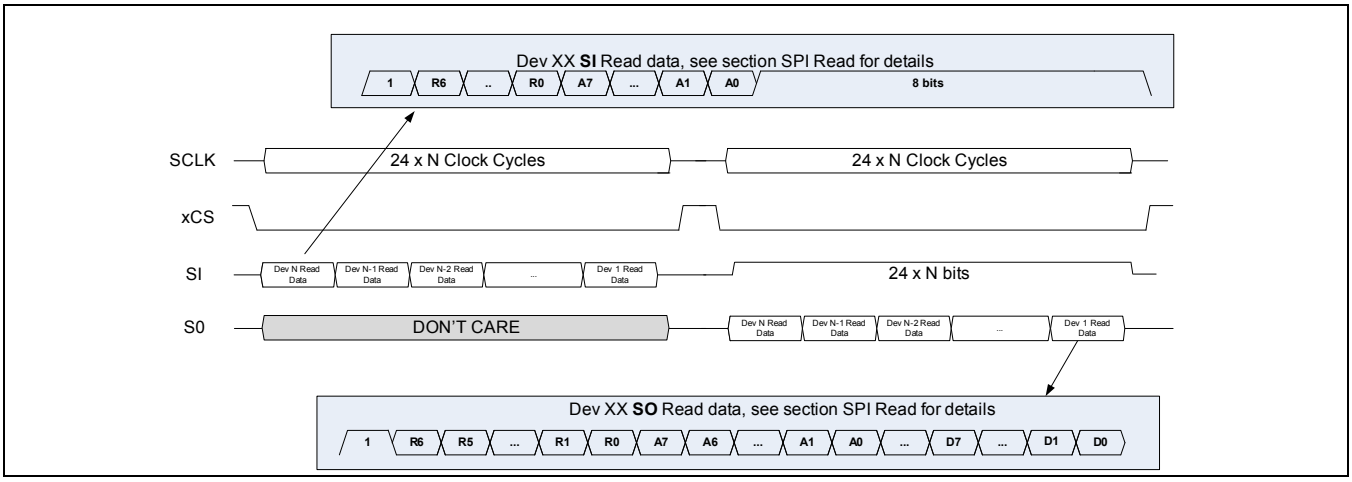


Table 4-7. SPI Interface Specifications

Timing Symbol	Description	Min	Max	Unit
T_{FREQW}	4-Wire clock Frequency	—	20	MHz
T_{DCD}	SCLK pulse width	40	60	%
Tds	SI Data set-up time (SCLK↑).	4	—	ns
Tdh	SI Data hold time (SCLK↑).	4	—	ns
Tcs	xCS set-up time (from xCS↓ to SCLK↑).	14	—	ns
Tch	xCS hold time (from xCS↑ to SCLK↑).	4	—	ns
Tcot	xCS off time (from xCS↑ to xCS↓).	10	—	us
Tzdd	SO Read data output delay, Tri-State to Active (xCS↓)	—	10	ns
Tddz	SO Read data output delay, Active to Tri-State (xCS↑)	—	20	ns
Tdd	SO Read data output delay from SCLK↓	—	15	ns

4.7.3 MDIO Interface

When the MAXP-37161 digital interface is configured to be in MDIO Manageable Devices interface (MMD) controlled by a Station Management Entity (STA), MF[1:0] are mapped to MDIO (Data IO) and MDC (Clock) respectively. Pins MF[5:2] are used to decode the port addresses (PRTAD) for the MMD, see Table 4-8.

Table 4-8. PRTAD Address set by Multi-functions Pins MF[5:2]

MF[5:2]	PRTAD	**MF[5:2]**	PRTAD
0000	00h or 01h	00FF	10h or 11h
0001	02h or 03h	0100	12h or 13h
0010	04h or 05h	0101	14h or 15h
0011	06h or 07h	0110	16h or 17h
00F0	08h or 09h	0111	18h or 19h
00F1	0Ah or 0Bh	01F0	1Ah or 1Bh
000F	0Ch or 0Dh	01F1	1Ch or 1Dh
001F	0Eh or 0Fh	010F	1Eh or 1Fh

This device supports expansion clause 45 of IEEE 802.3ae but does not support clause 22. The frame composition is shown in Table 4-9. After POR, a minimum of three MDC clock cycles is required to get the device "out of reset" before any Read/WRITE operation.

Table 4-9. MDIO — Frame Composition

Operation	**PRE(32)**	**ST(2)**		**OP(2)**		**PRTAD(5)**					**DEVAD(5)**					**TA(2)**		**ADDR/DATA (16 bits)**	**Idle**
	FFFFFFFFh	0	0								*0	0	0	0	1				
Address				0	0											1	0	Driven by STA	z
Write				0	1											1	0	Driven by STA	z
Read				1	1											z	0	Driven by MMD	z
Read + Address				1	0											z	0	Driven by MMD	z

NOTES:

1. **PRE:** 32-bit Preamble sequence of “1’s” on MDIO is required before MMD responds to any transaction.
2. **ST:** 2-bit Start of Frame:, clause 22: 01b and clause 45: 00b (not supporting clause 22).
3. **OP:** 2-bit Opcode. 00b = Address, 01b = Write, 11b = Read, 10b = Read + Address
4. **PRTAD:** 5-bit Port of address, see Table 4-8, more PRTAD’s are supported via EEPROM download..
5. **DEVAD:** 5-bit Device address, *default value is 1Eh (could be changed by optional downloading from external EEPROM or by a STA to register 09h/page0).
6. **TA:** 2-bit Turn Around): “10” in Write cycle. MMD drives TA bits in Read cycle with “z0”.
7. **ADDR/DATA:** 16-bit. All bits are used for writing or reading depending on the value of **OP**
8. **Idle:** MAXP-37161 disables output MDIO pin. STA should also disable its driver and let MDIO pulling high by external pull-up resistor.

The MDIO timing waveforms are shown in Figure 4-12 and the timing specifications are listed in Table 4-10. For further details, please refer to the IEEE Std 802-3-2005 (section 45.3).

Figure 4-12. MDIO Timing

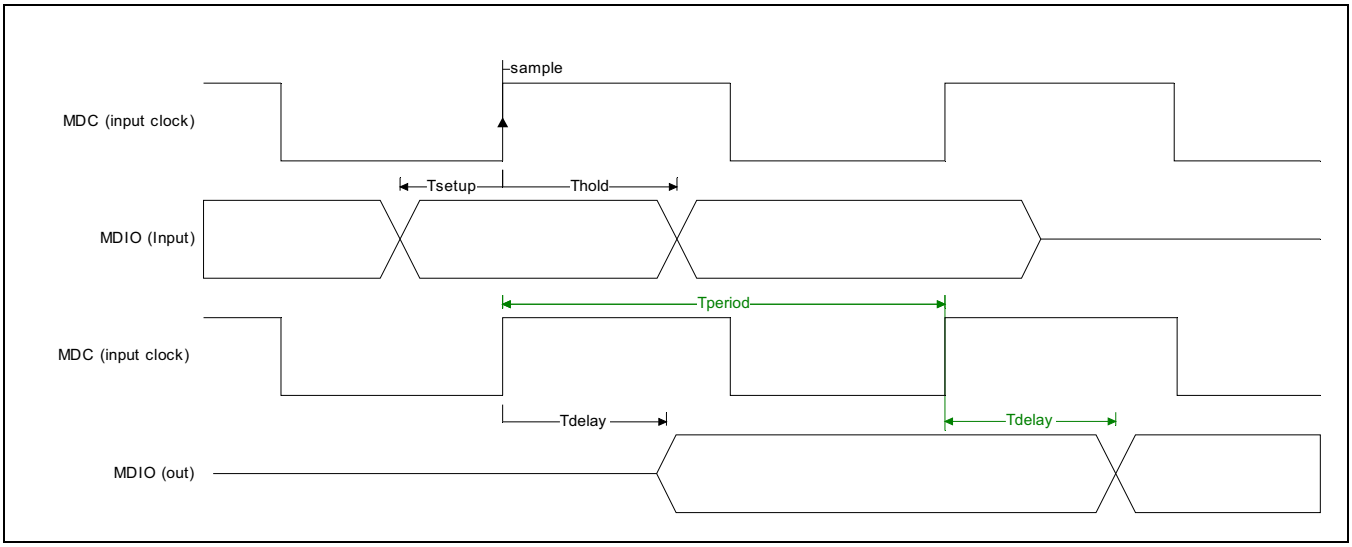


Table 4-10. MDIO Timing Specifications

Symbol	Description	Minimum	Maximum	Unit
T_{setup}	MDIO Set up time to MDC XX	10		ns
T_{hold}	MDIO HOLD time to MDC XX	10		ns
T_{delay}	MDIO delay from MDC XX in reading	0	300	ns
T_{PERIOD}	Period of MDC (2.5MHz max clock)	400		ns
T_{pwl}	MDC minimum Low	160		ns
T_{pwh}	MDC minimum High	160		ns

4.7.4 EEPROM Support

4.7.4.1 EEPROM Download Process

The larger system consists of a number of devices sharing the I2C bus. When EEPROM mode is enabled using the CONFIG[1:0] pins, each device reads initialization data from the EEPROM after power-up. The first device is the one configured to respond to I2C device ID 0100000 (40h) by driving MF[5:2] low. This I2C device ID must be used. The other I2C device IDs need not be in sequence. When EEPROM download is enabled with the I2C interface, all devices on the bus read their bytes in turn as one device enables the next. When EEPROM download is enabled with the SPI interface, it is assumed that only one device is connected to the EEPROM.

The first seven bytes of the EEPROM data compose the header, see Table 4-11. The first byte of the header is the checksum seed. This value is selected so that the 8 LSB of the sum of all header bytes results in 2Eh. The purpose of the checksum is to detect an un-programmed (blank) EEPROM. It can also detect data errors which result from a noisy power supply immediately after power-up. If the computed checksum does not match this value, the header is reloaded. After 512 checksum errors, a failure is declared and no further EEPROM downloading is performed. This allows up to 92ms for things to stabilize after power-up.

Two bytes (byte 2 and 3) of the header contain the number of registers to be programmed. The data following the header is a structure containing the address and value of each register to be initialized. Only the registers indicated by the address fields will be written. Writing to address FFh changes the logical page so that any of the device's registers may be initialized. Even the broadcast page may be used to save time if all channels require the same values. This sparse data structure saves time when only a few registers need to be initialized. When using the sparse data structure, the registers may be configured in any order.

If byte 2 and 3 of the header are zero, then it is assumed that the bytes are stored in the EEPROM in a packed arrangement (no addresses). The packed structure (full download) saves time when initializing most or all registers. When using the packed data structure, all device registers must be included (even if the values are not changed) and the order of the bytes is important.

Byte 4 of the header indicates the device ID of the next master on the bus. Once the first master is finished reading from the EEPROM, it writes control registers in the next master telling it where its data is located in the EEPROM and causing it to begin downloading data. The current master will write to the eeprom_size, eeprom_i2c_device_id, eeprom_address_offset registers of the next master device before setting its eeprom_start to '1'. If the next_i2c_master field is zero, then there is no next master and this master asserts the alarm pin.

Byte 5 of the header indicates the EEPROM I2C address of the next master's data. This information is passed to the next master before it is enabled to download. Some EEPROMS use multiple I2C device IDs in addition to the internal address offset byte(s). This field makes it possible to use these types of EEPROMS. Some systems might have more than one small EEPROM in place of a larger one. This field makes it possible for the initialization data to span multiple EEPROMs.

Bytes 6 and 7 of the header indicate the EEPROM address offset of the next master's data. This information is passed to the next master before it is enabled to download. This field enables the best use of the EEPROM storage since not all devices need to use the same number of bytes. In fact, some devices may use the sparse method and some may use the packed method. All initialization data for all devices can be packed into the front of the EEPROM so that there is space available at the end for other system-related values.

Only one device will master the bus at a time. The host controller must not attempt to master the bus until all devices complete their download. If the EEPROM is not ready when the first master attempts to read from it (NACK), it will retry 512 times before a failure is declared. Similarly, if the next master is not yet ready (NACK), 512

retries will be attempted before a failure is declared. This allows up to 14ms for any differences between devices to be resolved.

Table 4-11. EEPROM Data Format

Section	Sub-Section	Comment
Header	Checksum Seed	1 byte. This value is set such that the sum of the header values will be 2Eh so that a blank EEPROM is detected
	Register Count	2 bytes. The EEPROM can have a full format or a sparse format. When this field is zero, the full download format is used and all device registers are assumed to be in the EEPROM. Any other value indicates that the sparse format is used and that there are <count> number of byte pairs. Each pair consists of an address and data field. Not all registers need be included in the sparse format.
	Next I2C Master	1 byte. This field indicates the I2C device ID of the next master on the bus. If this field is zero, this master is the last to download from the EEPROM.
	Next EEPROM I2C Device ID	1 byte.
	Next EEPROM address offset	2 bytes. This field indicates where the next master's data starts in the EEPROM
Data	Packet or sparse formats	Packet format: data1, data2.... Sparse format: add1, data1, add2, data2 ...

4.7.4.2 EEPROM Package Data Sequence

If the package data format is selected the data download follows the format shown in Table 4-12.

Table 4-12. EEPROM Sequence Description by Register Map

Sequence	Page	Register Addresses	Function	
1	00h	01h - 09h, 10h and 11h	Global Configuration	
2	01h	00h - 13h	Crosspoint	Intermediate Switch Config1
3	02h	00h - 13h		Intermediate Switch Config2
4	03h	00h - 13h		Active Switch Configuration
5	05h	00h		Group Configuration
6	10h	00h - 03h and 07h	Temperature Monitoring	
7	11h	00h	Reference Clock	
8	12h	00h to 06h	Monitor Clock	
9	1Fh	E0h, E6h, E7h, F0h, F1h, F4h, F5h, F6h, F7h, FAh, FBh, FCh, FDh	Broadcast Channel	
10-25	2Fh - 20h	10h to 1Fh, 20h to 24h, 30h, 31h, 32h, 33h, 34h, 35h, 36h, 37h, 40h, 41h, 43h, 44h, 46h, 50h, 51h, 52h, 60h, 61h, 62h, 63h, 64h, 65h, 70h, 71h, 72h, 73h, 74h, 7Eh, 80h, 81h, 83h, 90h, 91h, 92h, 93h, 94h, 95h, 96h, 97h, 98h, A0h, A1h, A2h, B0h, B2h, B3h, B4h, B5h, B6h, B7h, B8h and DDh	Channel [15:0] Control	
26-28	33h -30h	00h to 0Ah, 13h, 22h, 23h, 25h, 26h, 27h, 32h to 3Fh, 40h to 43h, 44h, 50h, 51h, 53h, 54h, DCh, DDh	Slice [3:0] Control	

4.7.4.3 Atmel EEPROM's Supported

Table 4-13 Shows supported EEPROM's from Atmel.

Table 4-13. Atmel EEPROM's Supported

Part Number	# Bytes	Address Bytes	I2C Device ID	Comments
AT24C1024*	131072	2	A0-A2	I2C device ID[1] is pin configurable
AT24C1024B	131072	2	A0-A2	I2C device ID[2:1] is pin configurable
AT24C512	65536	2	A0	I2C device ID[1:0] is pin configurable
AT24C256	32768	2	A0	I2C device ID[1:0] is pin configurable
AT24C128	16384	2	A0	I2C device ID[1:0] is pin configurable
AT24C64	8192	2	A0	I2C device ID[2:0] is pin configurable
AT24C64A*	8192	2	A0	I2C device ID[2:0] is pin configurable
AT24C64C	8192	2	A0	I2C device ID[2:0] is pin configurable
AT24C32	4096	2	A0	I2C device ID[2:0] is pin configurable
AT24C32A*	4096	2	A0	I2C device ID[2:0] is pin configurable
AT24C32C	4096	2	A0	I2C device ID[2:0] is pin configurable
AT24C16*	2048	1	A0-AE	
AT24C16A	2048	1	A0-AE	
AT24C08*	1024	1	A0-A6	I2C device ID[2] is pin configurable
AT24C08A	1024	1	A0-A6	I2C device ID[2] is pin configurable
AT24C04	512	1	A0-A2	I2C device ID[2:1] is pin configurable
AT24C04A	512	1	A0-A2	I2C device ID[2:1] is pin configurable
AT24C02	256	1	A0	I2C device ID[2:0] is pin configurable
AT24C02A	256	1	A0	I2C device ID[2:0] is pin configurable
AT24C01A	128	1	A0	I2C device ID[2:0] is pin configurable
AT34C02*	256	1	A0	I2C device ID[2:0] is pin configurable
AT34C02C	256	1	A0	I2C device ID[2:0] is pin configurable
*Not recommended for new designs				

4.7.5 JTAG Interface

The JTAG test interface support the 1149.6 boundary scan standard (ACJTAG)

Table 4-14. JTAG Mode Multi-function Pin

MF3	MF2	MF1	MF0	MF4
TDO	TDI	TMS	TCK	TRSTn

5.0 Control Registers Map and Descriptions

5.1 Register Map General Overview

The MAXP-37161 has a lot of functions that can be controlled via registers, the register map is divided with several register pages to help distribute these functions as described in Table 5-1.

Table 5-1. Register Map Description Summary

Function		Page	Comment
Global		00h	Use register.**Page** (address FFh) to select other pages.
Crosspoint	Intermediate Switch Config1	01h	ISC1. Serves as memory page1 for the next xSET strobe
	Intermediate Switch Config2	02h	ISC2. Serves as memory page2 for the next xSET strobe
	Active Switch Configuration	03h	Holds the current configuration the crosspoint has.
Temperature Monitoring		10h	
Reference Clock		11h	
Monitor Clock		12h	
Global Channel Control (Rx and Tx)		1Fh	Write to all channels at the same time. Write only.
Individual Channel Control (Rx and Tx)		2Fh - 20h	Channel [15:0] Individual input buffer, CDR and output buffer control
Global Slice Control		1Eh	Write to all slices at the same time. Write only.
Individual Slice Control		33h -30h	Individual Slice [3:0] control, eye monitor, PRBS generator and checker.

NOTES:

- After power up or software reset, the default page in 00h.
- To switch pages, write the desired page number to register FFh, independent of the active page (All pages support register FFh)

Table 5-2 shows the register map for the MAXP-37161. Should any reserved registers or bits need to be written, use with their default value listed. Registers not listed in Table 5-2 are reserved with default value of 00h.

Table 5-2. Register Summary

Page	Add	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
"PAGE 00h, Global Configuration" on page 49												
00h	00h	Checksum seed	checksum								00'h	R
	01h	Gen SW Config	*Reserved*					strobe		standby	00'h	R/W
	02h	*Reserved*	*Reserved (set to default)*								02'h	R/W
	03h	Strobe	icl_sel	xSET_mode	swstrobe						00'h	R/W
	05h	grpchassign	gblch		*group_lane*	*Reserved (set to default)*					20'h	R/W
	06h-07h	*Reserved*	*Reserved (set to default)*								A5'h	R/W
	08h	*Reserved*	*Reserved (set to default)*								12'h	R/W
	10h	*powermode*	*Reserved (set to default)*							smartpwr	00'h	R/W
	11h	*modulation*	*Reserved (set to default)*			en_lf	sel_lf				00'h	R/W
	E0h	Reset	Reset								00'h	R/W
	E1h	CHIPID	chipid								44'h	R
	E2h	*Rev ID*	*revid*								09'h	R
	E3h	*Reserved*	*Reserved (set to default)*								00'h	R
	E4h	*DC_ACB*	*Reserved*	DC_ACB	*Reserved (set to default)*						00'h	R
	E5h	Checksum_calc	checksum_calc								00'h	R
	E6-E7h	*Reserved*	*Reserved (set to default)*								00'h	R/W
	E9h	Eeprom_reg	eeprom_size	eeprom_i2c_addr							50'h	R/W
	EAh	eeprom address1	eeprom_addr1								00'h	R/W
	EBh	eeprom address2	eeprom_addr2								00'h	R/W
	ECh	eeprom	*Reserved (set to default)*				eeprom_fail		eeprom_done	eeprom_start	00'h	R/W
	F0h	LOS Alarm Flag1	CH7 LOS alrm	CH6 LOS alrm	CH5 LOS alrm	CH4 LOS alrm	CH3 LOS alrm	CH2 LOS alrm	CH1 LOS alrm	CH0 LOS alrm	00'h	R/W
	F1h	LOS Alarm Flag2	CH15 LOS alrm	CH14 LOS alrm	CH13 LOS alrm	CH12 LOS alrm	CH11 LOS alrm	CH10 LOS alrm	CH9 LOS alrm	CH8 LOS alrm	00'h	R/W
	F2h	LOS Alarm status1	CH7 LOS stat	CH6 LOS stat	CH5 LOS stat	CH4 LOS stat	CH3 LOS stat	CH2 LOS stat	CH1 LOS stat	CH0 LOS stat	00'h	R
	F3h	LOS Alarm status2	CH15 LOS stat	CH14 LOS stat	CH13 LOS stat	CH12 LOS stat	CH11 LOS stat	CH10 LOS stat	CH9 LOS stat	CH8 LOS stat	00'h	R
	F4h	LOS Alarm mask1	CH7 LOS msk	CH6 LOS msk	CH5 LOS msk	CH4 LOS msk	CH3 LOS msk	CH2 LOS msk	CH1 LOS msk	CH0 LOS msk	00'h	R/W
	F5h	LOS Alarm mask2	CH15 LOS msk	CH14 LOS msk	CH13 LOS msk	CH12 LOS msk	CH11 LOS msk	CH10 LOS msk	CH9 LOS msk	CH8 LOS msk	00'h	R/W
	F6h	LOL Alarm Flag1	CH7 LOL alrm	CH6 LOL alrm	CH5 LOL alrm	CH4 LOL alrm	CH3 LOL alrm	CH2 LOL alrm	CH1 LOL alrm	CH0 LOL alrm	00'h	R/W
	F7h	LOL Alarm Flag2	CH15 LOL alrm	CH14 LOL alrm	CH13 LOL alrm	CH12 LOL alrm	CH11 LOL alrm	CH10 LOL alrm	CH9 LOL alrm	CH8 LOL alrm	00'h	R/W
	F8h	LOL Alarm status1	CH7 LOL stat	CH6 LOL stat	CH5 LOL stat	CH4 LOL stat	CH3 LOL stat	CH2 LOL stat	CH1 LOL stat	CH0 LOL stat	00'h	R
	F9h	LOL Alarm status2	CH15 LOL stat	CH14 LOL stat	CH13 LOL stat	CH12 LOL stat	CH11 LOL stat	CH10 LOL stat	CH9 LOL stat	CH8 LOL stat	00'h	R
	FAh	LOL Alarm mask#1	CH7 LOL msk	CH6 LOL msk	CH5 LOL msk	CH4 LOL msk	CH3 LOL msk	CH2 LOL msk	CH1 LOL msk	CH0 LOL msk	00'h	R/W
	FBh	LOL Alarm mask#2	CH15 LOL msk	CH14 LOL msk	CH13 LOL msk	CH12 LOL msk	CH11 LOL msk	CH10 LOL msk	CH9 LOL msk	CH8 LOL msk	00'h	R/W
	FCh	Other Alarm reg#1	*Reserved*				eeprom alarm	LOR alarm flag	Temp alrm stat	Temp alrm flag	00'h	R/W
	FDh	Other Alarm reg#2	*Reserved*				eeprom mask	LOR mask	Temp stat msk	Temp flag msk	00'h	R/W

Table 5-2. Register Summary

Page	Add	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
"PAGE 03h, Active Switch Configuration (ASC)" on page 69												
01h	00h-0Fh	isc1(M)	1:1 Configuration								HEX(M)	R/W
	10h-13h	isc1_aux	*Reserved (set to default)*			isc1_aux0	isc1_aux1	isc1_aux2	isc1_aux3	isc1_aux_off	1F'h	R/W
02h	00h-0Fh	isc2(M)	Channel 0 Broadcast								00'h	R/W
	10h-13h	isc2_aux	*Reserved (set to default)*			isc2_aux0	isc2_aux1	isc2_aux2	isc2_aux3	isc2_aux_off	1F'h	R/W
03h	00h-0Fh	asc(M)	1:1 Configuration								HEX(M)	R/W
	10h-13h	asc_aux	*Reserved (set to default)*			asc1_aux0	asc1_aux1	asc1_aux2	asc1_aux3	asc1_aux_off	1F'h	R/W
"PAGE 10h, Temperature Monitor" on page 70												
10h	00h	temp reg#1	temp mon pd	temp_strobe	temp_reset	Reserved (set to default)				Disable temp_alarm	00'h	R/W
	01h	temp reg#2	*Reserved (set to default)*		temp alarm threshold high						28'h	R/W
	02h	*Reserved*	*Reserved (set to default)*								00'h	R/W
	03h	*Reserved*	*Reserved (set to default)*								00'h	R/W
	04h	Temp Read	temp read								na	R
	05h	*Reserved*	*Reserved (set to default)*								00'h	R
	06h	*Reserved*	*Reserved (set to default)*								00'h	R
	07h	*Reserved*	*Reserved (set to default)*								00'h	R/W
	08h	*Reserved*	overtemp pd	overtemp flag	overtemp threshold low						1A'h	R/W
	FCh	Temp alarm1	*Reserved*					LOR alarm flag	Temp alarm status	Temp alarm flag	00'h	R/W
	FDh	Temp alarm2	*Reserved*					LOR mask	TEMP status mask	Temp flag mask	00'h	R/W
"PAGE 11h, Reference Clock" on page 75												
11h	00h	Core Bias & refclk reg	refclk los vth		refclk los tc	refclk_type	pd refclk	*Reserved*			08'h	R/W
"PAGE 12h, Monitor Clock" on page 76												
12h	00h	MCLK_ASC	*Reserved*			rclk_asc					1F'h	R/W
	01h	MCLK_ISC1	*Reserved*			rclk_isc1					00'h	R/W
	02h	MCLK_ISC2	*Reserved*			rclk_isc2					00'h	R/W
	03h	MCLK_SW	*Reserved*						rclk_isc_sel	rclk_strobe	00'h	R/W
	04h	MCLK_CTRL	*Reserved*				mclk_swing			mclk_en	00'h	R/W
	05h	MCLK_PRBS0	*Reserved*	mclk_prbs1			*Reserved*	mclk_prbs0			77'h	R/W
	06h	MCLK_PRBS1	*Reserved*	mclk_prbs3			*Reserved*	mclk_prbs2			77'h	R/W
"PAGE 1Fh, Broadcast Control" on page 79												
1Fh	Any	Channel Broadcast	Any								00'h	R/W

Table 5-2. Register Summary

Page	Add	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
"PAGE 20h to 2Fh, Channel [15:0] Rx Control" on page 80												
20h-2Fh	10h	*chan_test*	*Reserved (set to default)*						los_clk_pd	selftest_en	00'h	R/W
	12h	ch powerdown	ch powerdown	*Reserved*							30'h	R/W
	37h	squelch level	*Reserved*						squelch level		00'h	R/W
	51h	FREQ ACQ2	lock detect pd	select FA mode	*Reserved*		vctrl LOL				00'h	R/W
	52h	*smart_power*	set_state			*Reserved (set to default)*				smart_pwr	00'h	R
	53h	FREQ ACQ4	*Reserved*			LOL	*Reserved*	Freq Acq state			00'h	R
	61h	CDR REG2	*Reserved*		CDR CP compensation		*Reserved (set to default)*				00'h	R/W
	62h	CDR REG3	vco div		ictrl_gm_coarse		ictrl_gm_fine				3C'h	R/W
	65h	CDR REG4	*Reserved*	set clk test	sel vco			pd qclk	vco core test	lf_en	08'h	R/W
	80h	LOS REG1	pd los	los test enable	los hyst disable	los force hyst	los hyst level	*Reserved*		never squelch	07'h	R/W
	81h	LOS REG2	low datarate	los time const	los cal restart	force los cal	los threshold				00'h	R/W
	82h	*Reserved*	*Reserved (set to default)*								00'h	R/W
	83h	LOS CAL1	eyemon cal	LOS alarm	los cal valout						00'h	R
	92h	*AFE*	*Reserved)*	dc_ac	*Reserved (set to default)*						00'h	R/W
	A1h	EYEMON_CALVAL	*Reserved*		cal_val_in						00'h	R/W
	A2h	EYEMON_CTRL	*Reserved*		dll_ctrl						00'h	R/W
	B2h	PLL_DIV_M_LSB	pll_div_m_lsb								00'h	R/W
	B3h	PLL_DIV_M_MSB	*Reserved*							pll_div_m_msb	00'h	R/W
	B4h	PLL_DIV_N_LSB	pll_div_n lsb								00'h	R/W
	B5h	PLL_DIV_N_MSB	*Reserved*				pll_div_n msb				00'h	R/W
	B6h	*PLL_REG1*	*Reserved (set to default)*			pll_icp_set					14'h	R/W
	B8h	*PLL_REG2*	*clk_div_64*	pll_rclk_div		*Reserved*		pll_resistor			43'h	R/W
"PAGE 20h to 2Fh, Channel [15:0] Tx Control" on page 89												
20h-2Fh	30h	TX CNTL0	offset enable	force offset mid	force offset min	force offst max	slow slew enable		squelch enable	force mute	80'h	R/W
	31h	*Reserved*	*Reserved (set to default)*								3A'h	R/W
	32h	*Reserved*	*Reserved (set to default)*								1B'h	R/W
	33h	TX post	*Reserved*			post de-emph					00'h	R/W
	34h	TX pre	*Reserved*			pre de-emph					00'h	R/W
	35h	TX swing	*Reserved*		tx swing						28'h	R/W
	36h	TX spare	*Reserved*					tx_en_lf	pd_tx	ch invert	00'h	R/W

Table 5-2. Register Summary

Page	Add	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
"PAGE 30h to 33h, Slice[3:0] Control" on page 91												
30h-33h	00h	GEN PLL DIV M LSB	gen_pll_div_m_lsb								10'h	R/W
	01h	GEN PLL DIV M MSB	*Reserved*							gen_pll_div_m_msb	00'h	R/W
	02h	GEN PLL DIV N LSB	gen_pll_div_n lsb								A5'h	R/W
	03h	GEN PLL DIV N MSB	*Reserved*				gen_pll_div_n msb				00'h	R/W
	04h	GEN PLL REG1	*Reserved (set to default)*				gen_pll_set_icp				14'h	R/W
	06h	*Reserved*	*Reserved (set to default)*								80'h	R/W
	07h	*Reserved*	*Reserved (set to default)*								60'h	R/W
	08h	GEN CDR REG2	gen_vco_div		gen_ictrl_gm_coarse		gen_ictrl_gm_fine				3C'h	R/W
	09h	*Reserved*	*Reserved (set to default)*								04'h	R/W
	0Ah	GEN CDR REG4	*Reserved*		gen_sel_vco			*Reserved*			08'h	R/W
	20h	COUNT EVEN PRBS	PRBS EVEN COUNT								00'h	R
	21h	COUNT ODD PRBS	PRBS ODD COUNT								00'h	R
	22h	PRBS CHKR CNTL0	*Reserved*	prbs chkr_ reset	prbs chkr cnt reset	prbs chkr freeze	prbs chkr_en	prbs chkr polarity	prbs chkr select	*Reserved*	00'h	R/W
	23h	PRBS CNTL1	prbs chkr extn enable	*Reserved*		prbs gen reset	prbs gen en	prbs gen select	prbs chkr cntr extn rst	prbs chkr dly cntl	00'h	R/W
	26h	PRBS CNTL4	*Reserved*				prbs chkr sync error	prbs chkr mode	prbs chkr done	prbs chkr run	00'h	R/W
	27h	PRBS CNTL5	prbs chkr closed eye	prbs chkr anomaly	prbs chkr timer						00'h	R/W
	29h	PRBS CHKR Error LSB	PRBS CHKR Error LSB								00'h	R
	2Ah	PRBS CHKR Error MSB	PRBS CHKR Error MSB								00'h	R
	32h	CHK PLL DIV M LSB	chk_pll_div_m_lsb								10'h	R/W
	33h	CHK PLL DIV M MSB	*Reserved*							chk_pll_div_m_msb	00'h	R/W
	34h	CHK PLL DIV N LSB	chk_pll_div_n lsb								A5'h	R/W
	35h	CHK PLL DIV N MSB	*Reserved*				chk_pll_div_n msb				00'h	R/W
	36h	CHK PLL REG1	*Reserved (set to default)*			chk_pll_set_icp					14'h	R/W
	38h	*Reserved*	*Reserved (set to default)*								13'h	R/W
	39h	*Reserved*	*Reserved (set to default)*								60'h	R/W
	3Ah	CHK CDR REG2	chk_vco_div		chk_ictrl_gm_coarse		chk_ictrl_gm_fine				3C'h	R/W
	3Ch	CHK CDR REG4	*Reserved*		chk_sel_vco			*Reserved*			08'h	R/W
	40h	CHK FREQ ACQ1	lock_de-t_prbs_gen	*Reserved*		chk_lol	*Reserved*	chk_freq_acq_state			00'h	R
	42h	CHK FREQ ACQ2	*Reserved*	chk select FA mode	*Reserved*		chk vctrl LOL				00'h	R/W
	43h	CHK FREQ ACQ3	*chk_set state*			*Reserved (set to default)*					40'h	R

Table 5-2. Register Summary

Page	Add	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
30h-33h	50h	SLICE CTRL	*Reserved (set to default)*							slice_pd	00'h	R/W
	52h	EYEMON_RESULT	*Reserved*		eyemon_result						00'h	R
	53h	EYEMON_CNTL0	*Reserved*	adc_pdb	adc_swing				adc_clk_sel		00'h	R/W
	54h	MON CLK	*Reserved*					mon_clk_sel			00'h	R/W
All	FFh	Page	*Reserved*		page						00'h	R/W

5.2 PAGE 00h, Global Configuration

Page: 00h
Address: 00h
Register Name: Checksum seed
Default Value: 00'h
Description: Checksum seed. EEPROM downloadable.
Set during EEPROM download, this value biases the checksum of the header so that the result will be 3Eh

Bit(s)	Name	Description	Default	Type
[7:0]	checksum	0000 0000b: Set during EEPROM download, this value biases the checksum of the header so that the result will be 3Eh	0000 0000b	R

Page: 00h
Address: 01h
Register Name: Gen SW Config
Default Value: 00'h
Description: Strobe mode selection made with hardware pin or control register. EEPROM downloadable.

Bit(s)	Name	Description	Default	Type
[7:3]	*Reserved*	*Reserved (set to default)*	0 0000b	R/W
[2:1]	strobe	00b: Direct ASC mode. Update switch configuration on each ASC register write. 01b: Strobe pin xSET to change SW config 11b: Strobe control reg to change SW config (ACL regs only written to when this bit=1)	00b	R/W
[0]	standby	0b: Normal operation 1b: Place device in standby	0b	R/W

Page: 00h
Address: 03h
Register Name: Strobe
Default Value: 00'h
Description: Changes switch configuration with strobe to this self-clearing control register. Intermediate switch configuration (ISC) transferred to active switch configuration (ASC) upon strobe. EEPROM downloadable.

Bit(s)	Name	Description	Default	Type
[7]	icl_sel	0b: Sets ISC#1 as the active state to become ACL upon software strobe 1b: Sets ISC#2 as the active state to become ACL upon software strobe	0b	R/W
[6]	xSET_mode	0b: xSET: L->H= select ISC#1 & H->L= ISC#2 as the active state (when Gen SW config reg<1>=0) 1b: xSET: H->L changes active state to either ISC#1 or ISC#2 depending on bit7 above (when Gen SW config reg<4>=0)	0b	R/W
[5:0]	swstrobe	00 0000b: Normal operation 10 1010b: Software strobe, change Active Switch Configuration with ISC 1 or 2.	00 0000b	R/W

Page: 00h
Address: 05h
Register Name: grpchassign
Default Value: 20'h
Description: Global group lane input order assignment register.

Bit(s)	Name	Description	Default	Type
[7:6]	gblch	00b: Set input.grouping{0,1,2,3} to output.grouping{0,1,2,3} 01b: Set input.grouping{0,1,2,3} to output.grouping{3,2,1,0} 10b: Set individual group assignments using the ISC1 & ISC2 (Pages 01h and 02h) 11b: Reserved	00b	R/W
[5]	*group_lane*	0b: Group Mode 1b: Lane Mode	1b	R/W
[4:0]	*Reserved*	*Reserved (set to default)*	0 0000b	R/W

Page: 00h
Address: 10h
Register Name: powermode
Default Value: 00'h
Description: Power mode.

Bit(s)	Name	Description	Default	Type
[7:1]	*Reserved*	*Reserved (set to default)*	0000000b	R/W
[0]	*smartpwr*	0b: Normal operation, smart power enabled 1b: Smart power disabled	0b	R/W

Page: 00h
Address: 11h
Register Name: modulation
Default Value: 00'h
Description: Global group lane input order assignment register.

Bit(s)	Name	Description	Default	Type
[7:5]	*Reserved*	*Reserved (set to default)*	0000b	R/W
[4]	*en_lf*	0b: Normal operation, low frequency cm modulation disabled 1b: Low frequency cm modulation enabled	0b	R/W
[3:0]	sel_lf	00b: Group0 selected for modulation 01b: Group1 selected for modulation 10b: Group2 selected for modulation 11b: Group3 selected for modulation	0000b	R/W

Page: 00h
Address: E0h
Register Name: Reset
Default Value: 00'h
Description: Writing AAh to this register causes all digital logic to reset to its default state including registers (except this one) and digital rtl FSMs.

Bit(s)	Name	Description	Default	Type
[7:0]	Reset	0000 0000b: Normal operation 1010 1010b: Assert reset	0000 0000b	R/W

Page: 00h
Address: E1h
Register Name: CHIPID
Default Value: 44'h
Description: Determines the chip ID code used by the JTAG controller

Bit(s)	Name	Description	Default	Type
[7:0]	chipid	0000 0000b: MAXP-37161, 16 Channel crosspoint	0100 0100b	R

Page: 00h
Address: E2h
Register Name: REVID
Default Value: 09'h
Description: Determines the revision ID code used by the JTAG controller

Bit(s)	Name	Description	Default	Type
[7:0]	revid	MAXP-37161B	0000 1001b	R
		MAXP-37161A	0000 1000b	R

Page: 00h
Address: E4h
Register Name: DC_ACB
Default Value: 00'h
Description: Rx DC or AC status

Bit(s)	Name	Description	Default	Type
[7]	*Reserved*	*Reserved (set to default)*	0b	R
[6]	dc_acb	0b: AC coupling is selected for Rx 1b: DC coupling is selected for Rx	0b	R
[5:0]	*Reserved*	*Reserved (set to default)*	00 0000b	R

Page: 00h
Address: E5h
Register Name: Checksum_calc
Default Value: 00'h
Description: Reports the actual value for the calculated checksum during the EEPROM download

Bit(s)	Name	Description	Default	Type
[7:0]	checksum_calc	0000 0000b: Checksum result	0000 0000b	R

Page: 00h
Address: E9h
Register Name: Eeprom_reg#1
Default Value: 50'h
Description: Indicates roughly how large the EEPROM is <7>, & Indicates the I2C address of the EEPROM <6:0>.

Bit(s)	Name	Description	Default	Type
[7]	eeprom_size	0b: One address offset byte 1b: Two address offset byte	0b	R/W
[6:0]	eeprom_i2c_addr	101 0000b: Indicates the i2c addr of the eeprom 111 1111b: Max address	101 0000b	R/W

Page: 00h
Address: EAh
Register Name: eeprom address#1
Default Value: 00'h
Description: eeprom_addr<7:0>: Indicates where in the EEPROM to find the initialization data for this master

Bit(s)	Name	Description	Default	Type
[7:0]	eeprom_addr1	0000 0000b: EEPROM address<7:0> for master initialization data	0000 0000b	R/W

Page: 00h
Address: EBh
Register Name: eeprom address#2
Default Value: 00'h
Description: eeprom_addr<15:8>: Indicates where in the EEPROM to find the initialization data for this master

Bit(s)	Name	Description	Default	Type
[7:0]	eeprom_addr2	0000 0000b: EEPROM address<15:8> for master initialization data	0000 0000b	R/W

Page: 00h
Address: ECh
Register Name: eeprom
Default Value: 00'h
Description: eeprom download status

Bit(s)	Name	Description	Default	Type
[7:4]	*Reserved*	*Reserved (set to default)*	0000b	R
[3:2]	eeprom_fail	00b: Initialization succeeded 01b: Failure to read EEPROM} 10b: Failure to start next master 11b: Reserved	00b	R
[1]	eeprom_done	0b: Download not completed 1b: Download completed	0b	R/W
[0]	eeprom_start	0b: Download has not started 1b: Download in progress	0b	R/W

Page: 00h
Address: F0h
Register Name: LOS Alarm Flag#1
Default Value: 00'h
Description: Reports whether a LOS alarm has been activated on CH<7:0> since the last time this bit was cleared. Writing a '1' to a bit clears that channel's alarm flag. If any of these bits are high, the alarm output will be asserted.
0 = no alarm has occurred
1 = an alarm has occurred

Bit(s)	Name	Description	Default	Type
[7]	CH7 LOS alarm flag	0b: No alarm asserted for Input CH7 1b: Alarm asserted for Input CH7	0b	R/W
[6]	CH6 LOS alarm flag	0b: No alarm asserted for Input CH6 1b: Alarm asserted for Input CH6	0b	R/W
[5]	CH5 LOS alarm flag	0b: No alarm asserted for Input CH5 1b: Alarm asserted for Input CH5	0b	R/W
[4]	CH4 LOS alarm flag	0b: No alarm asserted for Input CH4 1b: Alarm asserted for Input CH4	0b	R/W
[3]	CH3 LOS alarm flag	0b: No alarm asserted for Input CH3 1b: Alarm asserted for Input CH3	0b	R/W
[2]	CH2 LOS alarm flag	0b: No alarm asserted for Input CH2 1b: Alarm asserted for Input CH2	0b	R/W
[1]	CH1 LOS alarm flag	0b: No alarm asserted for Input CH1 1b: Alarm asserted for Input CH1	0b	R/W
[0]	CH0 LOS alarm flag	0b: No alarm asserted for Input CH0 1b: Alarm asserted for Input CH0	0b	R/W

Page: 00h
Address: F1h
Register Name: LOS Alarm Flag#2
Default Value: 00'h
Description: Reports whether a LOS alarm has been activated on CH<15:8> since the last time this bit was cleared. Writing a '1' to a bit clears that channel's alarm flag. If any of these bits are high, the alarm output will be asserted.
0 = no alarm has occurred
1 = an alarm has occurred

Bit(s)	Name	Description	Default	Type
[7]	CH15 LOS alarm flag	0b: No alarm asserted for Input CH15 1b: Alarm asserted for Input CH15	0b	R/W
[6]	CH14 LOS alarm flag	0b: No alarm asserted for Input CH14 1b: Alarm asserted for Input CH14	0b	R/W
[5]	CH13 LOS alarm flag	0b: No alarm asserted for Input CH13 1b: Alarm asserted for Input CH13	0b	R/W
[4]	CH12 LOS alarm flag	0b: No alarm asserted for Input CH12 1b: Alarm asserted for Input CH12	0b	R/W
[3]	CH11 LOS alarm flag	0b: No alarm asserted for Input CH11 1b: Alarm asserted for Input CH11	0b	R/W
[2]	CH10 LOS alarm flag	0b: No alarm asserted for Input CH10 1b: Alarm asserted for Input CH10	0b	R/W
[1]	CH9 LOS alarm flag	0b: No alarm asserted for Input CH9 1b: Alarm asserted for Input CH9	0b	R/W
[0]	CH8 LOS alarm flag	0b: No alarm asserted for Input CH8 1b: Alarm asserted for Input CH8	0b	R/W

Page: 00h
Address: F2h
Register Name: LOS Alarm status#1
Default Value: 00'h
Description: Reports the live status of each channel<7:0> alarm LOS source
0 = no alarm currently active
1 = an alarm is currently active

Bit(s)	Name	Description	Default	Type
[7]	CH7 LOS alarm status	0b: Alarm active for Input CH7 1b: Alarm inactive for Input CH7	0b	R
[6]	CH6 LOS alarm status	0b: Alarm active for Input CH6 1b: Alarm inactive for Input CH6	0b	R
[5]	CH5 LOS alarm status	0b: Alarm active for Input CH5 1b: Alarm inactive for Input CH5	0b	R
[4]	CH4 LOS alarm status	0b: Alarm active for Input CH4 1b: Alarm inactive for Input CH4	0b	R
[3]	CH3 LOS alarm status	0b: Alarm active for Input CH3 1b: Alarm inactive for Input CH3	0b	R
[2]	CH2 LOS alarm status	0b: Alarm active for Input CH2 1b: Alarm inactive for Input CH2	0b	R
[1]	CH1 LOS alarm status	0b: Alarm active for Input CH1 1b: Alarm inactive for Input CH1	0b	R
[0]	CH0 LOS alarm status	0b: Alarm active for Input CH0 1b: Alarm inactive for Input CH0	0b	R

Page: 00h
Address: F3h
Register Name: LOS Alarm status#2
Default Value: 00'h
Description: Reports the live status of each channel<15:8> alarm LOS source
0 = no alarm currently active
1 = an alarm is currently active

Bit(s)	Name	Description	Default	Type
[7]	CH15 LOS alarm status	0b: Alarm active for Input CH15 1b: Alarm inactive for Input CH15	0b	R
[6]	CH14 LOS alarm status	0b: Alarm active for Input CH14 1b: Alarm inactive for Input CH14	0b	R
[5]	CH13 LOS alarm status	0b: Alarm active for Input CH13 1b: Alarm inactive for Input CH13	0b	R
[4]	CH12 LOS alarm status	0b: Alarm active for Input CH12 1b: Alarm inactive for Input CH12	0b	R
[3]	CH11 LOS alarm status	0b: Alarm active for Input CH11 1b: Alarm inactive for Input CH11	0b	R
[2]	CH10 LOS alarm status	0b: Alarm active for Input CH10 1b: Alarm inactive for Input CH10	0b	R
[1]	CH9 LOS alarm status	0b: Alarm active for Input CH9 1b: Alarm inactive for Input CH9	0b	R
[0]	CH8 LOS alarm status	0b: Alarm active for Input CH8 1b: Alarm inactive for Input CH8	0b	R

Page: 00h
Address: F4h
Register Name: LOS Alarm mask#1
Default Value: 00'h
Description: Enables or masks any combination of channel<7:0> LOS alarms
0 = alarm enabled
1 = alarm masked

Bit(s)	Name	Description	Default	Type
[7]	CH7 LOS alarm mask	0b: Alarm enabled for Input CH7 1b: Alarm masked for Input CH7	0b	R/W
[6]	CH6 LOS alarm mask	0b: Alarm enabled for Input CH6 1b: Alarm masked for Input CH6	0b	R/W
[5]	CH5 LOS alarm mask	0b: Alarm enabled for Input CH5 1b: Alarm masked for Input CH5	0b	R/W
[4]	CH4 LOS alarm mask	0b: Alarm enabled for Input CH4 1b: Alarm masked for Input CH4	0b	R/W
[3]	CH3 LOS alarm mask	0b: Alarm enabled for Input CH3 1b: Alarm masked for Input CH3	0b	R/W
[2]	CH2 LOS alarm mask	0b: Alarm enabled for Input CH2 1b: Alarm maskedfor Input CH2	0b	R/W
[1]	CH1 LOS alarm mask	0b: Alarm enabled for Input CH1 1b: Alarm masked for Input CH1	0b	R/W
[0]	CH0 LOS alarm mask	0b: Alarm enabled for Input CH0 1b: Alarm masked for Input CH0	0b	R/W

Page: 00h
Address: F5h
Register Name: LOS Alarm mask#2
Default Value: 00'h
Description: Enables or masks any combination of channel<15:8> LOS alarms
0 = alarm enabled
1 = alarm masked

Bit(s)	Name	Description	Default	Type
[7]	CH15 LOS alarm mask	0b: Alarm enabled for Input CH15 1b: Alarm masked for Input CH15	0b	R/W
[6]	CH14 LOS alarm mask	0b: Alarm enabled for Input CH14 1b: Alarm masked for Input CH14	0b	R/W
[5]	CH13 LOS alarm mask	0b: Alarm enabled for Input CH13 1b: Alarm masked for Input CH13	0b	R/W
[4]	CH12 LOS alarm mask	0b: Alarm enabled for Input CH12 1b: Alarm masked for Input CH12	0b	R/W
[3]	CH11 LOS alarm mask	0b: Alarm enabled for Input CH11 1b: Alarm masked for Input CH11	0b	R/W
[2]	CH10 LOS alarm mask	0b: Alarm enabled for Input CH10 1b: Alarm masked for Input CH10	0b	R/W
[1]	CH9 LOS alarm mask	0b: Alarm enabled for Input CH9 1b: Alarm masked for Input CH9	0b	R/W
[0]	CH8 LOS alarm mask	0b: Alarm enabled for Input CH8 1b: Alarm masked for Input CH8	0b	R/W

Page: 00h
Address: F6h
Register Name: LOL Alarm Flag#1
Default Value: 00'h
Description: Reports whether a LOL alarm has been activated on CH<7:0> since the last time this bit was cleared. Writing a '1' to a bit clears that channel's alarm flag. If any of these bits are high, the alarm output will be asserted.
0 = no alarm has occurred
1 = an alarm has occurred

Bit(s)	Name	Description	Default	Type
[7]	CH7 LOL alarm flag	0b: No alarm asserted for Input CH7 1b: Alarm asserted for Input CH7	0b	R/W
[6]	CH6 LOL alarm flag	0b: No alarm asserted for Input CH6 1b: Alarm asserted for Input CH6	0b	R/W
[5]	CH5 LOL alarm flag	0b: No alarm asserted for Input CH5 1b: Alarm asserted for Input CH5	0b	R/W
[4]	CH4 LOL alarm flag	0b: No alarm asserted for Input CH4 1b: Alarm asserted for Input CH4	0b	R/W
[3]	CH3 LOL alarm flag	0b: No alarm asserted for Input CH3 1b: Alarm asserted for Input CH3	0b	R/W
[2]	CH2 LOL alarm flag	0b: No alarm asserted for Input CH2 1b: Alarm asserted for Input CH2	0b	R/W
[1]	CH1 LOL alarm flag	0b: No alarm asserted for Input CH1 1b: Alarm asserted for Input CH1	0b	R/W
[0]	CH0 LOL alarm flag	0b: No alarm asserted for Input CH0 1b: Alarm asserted for Input CH0	0b	R/W

Page: 00h
Address: F7h
Register Name: LOL Alarm Flag#2
Default Value: 00'h
Description: Reports whether a LOL alarm has been activated on CH<15:8> since the last time this bit was cleared. Writing a '1' to a bit clears that channel's alarm flag. If any of these bits are high, the alarm output will be asserted.
0 = no alarm has occurred
1 = an alarm has occurred

Bit(s)	Name	Description	Default	Type
[7]	CH15 LOL alarm flag	0b: No alarm asserted for Input CH15 1b: Alarm asserted for Input CH15	0b	R/W
[6]	CH14 LOL alarm flag	0b: No alarm asserted for Input CH14 1b: Alarm asserted for Input CH14	0b	R/W
[5]	CH13 LOL alarm flag	0b: No alarm asserted for Input CH13 1b: Alarm asserted for Input CH13	0b	R/W
[4]	CH12 LOL alarm flag	0b: No alarm asserted for Input CH12 1b: Alarm asserted for Input CH12	0b	R/W
[3]	CH11 LOL alarm flag	0b: No alarm asserted for Input CH11 1b: Alarm asserted for Input CH11	0b	R/W
[2]	CH10 LOL alarm flag	0b: No alarm asserted for Input CH10 1b: Alarm asserted for Input CH10	0b	R/W
[1]	CH9 LOL alarm flag	0b: No alarm asserted for Input CH9 1b: Alarm asserted for Input CH9	0b	R/W
[0]	CH8 LOL alarm flag	0b: No alarm asserted for Input CH8 1b: Alarm asserted for Input CH8	0b	R/W

Page: 00h
Address: F8h
Register Name: LOL Alarm status#1
Default Value: 00'h
Description: Reports the live status of each channel<7:0> alarm LOL source
0 = no alarm currently active
1 = an alarm is currently active

Bit(s)	Name	Description	Default	Type
[7]	CH7 LOL alarm status	0b: Alarm active for Input CH7 1b: Alarm inactive for Input CH7	0b	R
[6]	CH6 LOL alarm status	0b: Alarm active for Input CH6 1b: Alarm inactive for Input CH6	0b	R
[5]	CH5 LOL alarm status	0b: Alarm active for Input CH5 1b: Alarm inactive for Input CH5	0b	R
[4]	CH4 LOL alarm status	0b: Alarm active for Input CH4 1b: Alarm inactive for Input CH4	0b	R
[3]	CH3 LOL alarm status	0b: Alarm active for Input CH3 1b: Alarm inactive for Input CH3	0b	R
[2]	CH2 LOL alarm status	0b: Alarm active for Input CH2 1b: Alarm inactive for Input CH2	0b	R
[1]	CH1 LOL alarm status	0b: Alarm active for Input CH1 1b: Alarm inactive for Input CH1	0b	R
[0]	CH0 LOL alarm status	0b: Alarm active for Input CH0 1b: Alarm inactive for Input CH0	0b	R

Page: 00h
Address: F9h
Register Name: LOL Alarm status#2
Default Value: 00'h
Description: Reports the live status of each channel<15:8> alarm LOL source
0 = no alarm currently active
1 = an alarm is currently active

Bit(s)	Name	Description	Default	Type
[7]	CH15 LOL alarm status	0b: Alarm active for Input CH15 1b: Alarm inactive for Input CH15	0b	R
[6]	CH14 LOL alarm status	0b: Alarm active for Input CH14 1b: Alarm inactive for Input CH14	0b	R
[5]	CH13 LOL alarm status	0b: Alarm active for Input CH13 1b: Alarm inactive for Input CH13	0b	R
[4]	CH12 LOL alarm status	0b: Alarm active for Input CH12 1b: Alarm inactive for Input CH12	0b	R
[3]	CH11 LOL alarm status	0b: Alarm active for Input CH11 1b: Alarm inactive for Input CH11	0b	R
[2]	CH10 LOL alarm status	0b: Alarm active for Input CH10 1b: Alarm inactive for Input CH10	0b	R
[1]	CH9 LOL alarm status	0b: Alarm active for Input CH9 1b: Alarm inactive for Input CH9	0b	R
[0]	CH8 LOL alarm status	0b: Alarm active for Input CH8 1b: Alarm inactive for Input CH8	0b	R

Page: 00h
Address: FAh
Register Name: LOL Alarm mask#1
Default Value: 00'h
Description: Enables or masks any combination of channel<7:0> LOL alarms
0 = alarm enabled
1 = alarm masked

Bit(s)	Name	Description	Default	Type
[7]	CH7 LOL alarm mask	0b: Alarm enabled for Input CH7 1b: Alarm masked for Input CH7	0b	R/W
[6]	CH6 LOL alarm mask	0b: Alarm enabled for Input CH6 1b: Alarm masked for Input CH6	0b	R/W
[5]	CH5 LOL alarm mask	0b: Alarm enabled for Input CH5 1b: Alarm masked for Input CH5	0b	R/W
[4]	CH4 LOL alarm mask	0b: Alarm enabled for Input CH4 1b: Alarm masked for Input CH4	0b	R/W
[3]	CH3 LOL alarm mask	0b: Alarm enabled for Input CH3 1b: Alarm masked for Input CH3	0b	R/W
[2]	CH2 LOL alarm mask	0b: Alarm enabled for Input CH2 1b: Alarm maskedfor Input CH2	0b	R/W
[1]	CH1 LOL alarm mask	0b: Alarm enabled for Input CH1 1b: Alarm masked for Input CH1	0b	R/W
[0]	CH0 LOL alarm mask	0b: Alarm enabled for Input CH0 1b: Alarm masked for Input CH0	0b	R/W

Page: 00h
Address: FBh
Register Name: LOL Alarm mask#2
Default Value: 00'h
Description: Enables or masks any combination of channel<15:8> LOL alarms
0 = alarm enabled
1 = alarm masked

Bit(s)	Name	Description	Default	Type
[7]	CH15 LOL alarm mask	0b: Alarm enabled for Input CH15 1b: Alarm masked for Input CH15	0b	R/W
[6]	CH14 LOL alarm mask	0b: Alarm enabled for Input CH14 1b: Alarm masked for Input CH14	0b	R/W
[5]	CH13 LOL alarm mask	0b: Alarm enabled for Input CH13 1b: Alarm masked for Input CH13	0b	R/W
[4]	CH12 LOL alarm mask	0b: Alarm enabled for Input CH12 1b: Alarm masked for Input CH12	0b	R/W
[3]	CH11 LOL alarm mask	0b: Alarm enabled for Input CH11 1b: Alarm masked for Input CH11	0b	R/W
[2]	CH10 LOL alarm mask	0b: Alarm enabled for Input CH10 1b: Alarm masked for Input CH10	0b	R/W
[1]	CH9 LOL alarm mask	0b: Alarm enabled for Input CH9 1b: Alarm masked for Input CH9	0b	R/W
[0]	CH8 LOL alarm mask	0b: Alarm enabled for Input CH8 1b: Alarm masked for Input CH8	0b	R/W

Page: 00h
Address: FCh
Register Name: Other Alarm reg#1
Default Value: 00'h
Description: eeprom alarm = sticky flag which si asserted when the initialization process termiantes. Writing a "1" to this bit clears the flag
LOR alarm flag = Reports whether a LOR alarm has been activated since the last time this bit was cleared. Writing a '1' to this bit clears this flag.
Temp alarm status = Reports the live status of the temperature alarm source
Temp alarm flag = Reports whether a temperature alarm has been activated since the last time this bit was cleared. Writing a '1' to this bit clears this flag.

Bit(s)	Name	Description	Default	Type
[7:4]	*Reserved*	*Reserved (set to default)*	0000b	R/W
[3]	eeprom alarm	0b: Eeprom alarm asserted 1b: Eeprom alarm cleared	0b	R/W
[2]	LOR alarm flag	0b: No LOR alarm activated 1b: LOR alarm event	0b	R/W
[1]	Temp alarm status	0b: No temp alarm currently active 1b: Temp alarm is currently active	0b	R/W
[0]	Temp alarm flag	0b: No temp alarm has occurred 1b: Temp alarm has occurred	0b	R/W

Page: 00h
Address: FDh
Register Name: Other Alarm reg#2
Default Value: 00'h
Description: eeprom mask = sticky flag which si asserted when the initialization process termiantes. Writing a "1" to this bit clears the flag
LOR mask = Reports whether a LOR alarm has been activated since the last time this bit was cleared. Writing a '1' to this bit clears this flag.
Temp status mask = Reports the live status of the temperature alarm source
Temp flag mask = Reports whether a temperature alarm has been activated since the last time this bit was cleared. Writing a '1' to this bit clears this flag.

Bit(s)	Name	Description	Default	Type
[7:4]	*Reserved*	*Reserved (set to default)*	0000b	R/W
[3]	eeprom mask	0b: Eeprom alarm asserted 1b: Eeprom alarm cleared	0b	R/W
[2]	LOR mask	0b: No LOR alarm activated 1b: LOR alarm event	0b	R/W
[1]	Temp status mask	0b: No temp alarm currently active 1b: Temp alarm is currently active	0b	R/W
[0]	Temp flag mask	0b: No temp alarm has occurred 1b: Temp alarm has occurred	0b	R/W

Page: All
Address: FFh
Register Name: Page
Default Value: 00'h
Description: Page register. Determines the page accessed on subsequent read/writes.

Bit(s)	Name	Description	Default	Type
[7:6]	*Reserved*	*Reserved (set to default)*	00b	R/W
[5:0]	page	00 0000b: Set to page 00h 11 1111b: Set to page 3Fh (slice0-ch0 starts at pg 20h)(1)	00 0000b	R/W

NOTES:

1. Metal changeable.

5.3 PAGE 01h, Intermediate Switch Config1 (ISC1)

Page: 01h
Address: HEX(0 + n*1) n=0...19
00h 01h 02h 03h 04h 05h 06h 07h 08h 09h 0Ah 0Bh 0Ch 0Dh 0Eh 0Fh
Register Name: isc1(M)
Default Value: HEX(M)
Description: M=[0…19]
Intermediate switch configuration #1 (ISC1) state for output lane **M** (lane/lane mode), or group **M**, (group mode).
Writing to this register may cause the switch state to change immediately in an asynchronous manner.
Behavior is dependent on the content of register.**grpchassign** (page.00h, address.05h)

Bit(s)	Name	Description	Default	Type
[7:0]	isc1(M)	0000 0000b: Route input lane/group 0 to output lane/group **M** 0000 0001b: Route input lane/group 1 to output lane/group **M** 0000 0010b: Route input lane/group 2 to output lane/group **M** 0000 0011b: Route input lane/group 3 to output lane/group **M** :: last available group 0000 1110b: Route input lane 14 to output lane **M** 0000 1111b: Route input lane 15 to output lane **M** 1111 1111b: - Disable core output lane **M** and output driver **M**, if register.**misc_ctrl.**bit[2]=0b (default) (page.11h, address.25h)	HEX(M)	R/W

NOTES:

1. The M has 20 (including Auxiliary) valid lane assignments and 4 valid group assignments. Valid addresses are [00h..13h] in lane mode, [00..03h] in group mode.
2. By default this register sets up the crosspoint into a 1:1 configuration if not changed.

Page: 01h
Address: HEX(0 + n*1) n=0...19
10h 11h 12h 13h
Register Name: isc1(M)
Default Value: 1Fh
Description: M=[0…19]
Intermediate switch configuration #1 (ISC1) state for output lane **M** (lane/lane mode), or group **M**, (group mode).
Writing to this register may cause the switch state to change immediately in an asynchronous manner.
Behavior is dependent on the content of register.**grpchassign** (page.00h, address.05h)

Bit(s)	Name	Description	Default	Type
[7:0]	isc1_aux(M)	0001 0000b: Route auxiliary input lane 0 to output lane **M** 0001 0001b: Route auxiliary input lane 1 to output lane **M** 0001 0010b: Route auxiliary input lane 2 to output lane **M** 0001 0011b: Route auxiliary input lane 3 to output lane **M** 1111 1111b: - Disable core output lane **M** and output driver **M**, if register.**misc_ctrl.**bit[2]=0b (default) (page.11h, address.25h)	0001 1111b	R/W

NOTES:

1. The M has 20 (including Auxiliary) valid lane assignments and 4 valid group assignments. Valid addresses are [00h..13h] in lane mode, [00..03h] in group mode.

5.4 PAGE 02h, Intermediate Switch Config2 (ISC2)

Page: 02h
Address: HEX(0 + n*1) n=0...19
00h 01h 02h 03h 04h 05h 06h 07h 08h 09h 0Ah 0Bh 0Ch 0Dh 0Eh 0Fh
Register Name: isc2(M)
Default Value: HEX(M)
Description: M=[0…19]
Intermediate switch configuration #2 (ISC2) state for output lane **M** (lane/lane mode), or group **M**, (group mode).
Writing to this register may cause the switch state to change immediately in an asynchronous manner.
Behavior is dependent on the content of register.**grpchassign** (page.00h, address.05h).

Bit(s)	Name	Description	Default	Type
[7:0]	isc2(M)	0000 0000b: Route input lane/group 0 to output lane/group **M** 0000 0001b: Route input lane/group 1 to output lane/group **M** 0000 0010b: Route input lane/group 2 to output lane/group **M** 0000 0011b: Route input lane/group 3 to output lane/group **M** :: last available group 0000 1110b: Route input lane 14 to output lane **M** 0000 1111b: Route input lane 15 to output lane **M** 1111 1111b: - Disable core output lane **M** and output driver **M**, if register.**misc_ctrl.**bit[2]=0b (default) (page.11h, address.25h)	HEX(M)	R/W

NOTES:

1. The M has 20 (including Auxiliary) valid lane assignments and 4 valid group assignments. Valid addresses are [00h..13h] in lane mode, [00..03h] in group mode.
2. By default this register sets up the crosspoint into a channel 0 broadcast configuration if not changed.

Page: 02h
Address: HEX(0 + n*1) n=0...19
10h 11h 12h 13h
Register Name: isc2(M)
Default Value: 1Fh
Description: M=[0…19]
Intermediate switch configuration #2 (ISC2) state for output lane **M** (lane/lane mode), or group **M**, (group mode).
Writing to this register may cause the switch state to change immediately in an asynchronous manner.
Behavior is dependent on the content of register.**grpchassign** (page.00h, address.05h).

Bit(s)	Name	Description	Default	Type
[7:0]	isc2_aux(M)	0001 0000b: Route auxiliary input lane 0 to output lane **M** 0001 0001b: Route auxiliary input lane 1 to output lane **M** 0001 0010b: Route auxiliary input lane 2 to output lane **M** 0001 0011b: Route auxiliary input lane 3 to output lane **M** 1111 1111b: - Disable core output lane **M** and output driver **M**, if register.**misc_ctrl.**bit[2]=0b (default) (page.11h, address.25h)	0001 1111b	R/W

NOTES:

1. The M has 20 (including Auxiliary) valid lane assignments and 4 valid group assignments. Valid addresses are [00h..13h] in lane mode, [00..03h] in group mode.

5.5 PAGE 03h, Active Switch Configuration (ASC)

Page: 03h
Address: HEX(0 + n*1) n=0...19
00h 01h 02h 03h 04h 05h 06h 07h 08h 09h 0Ah 0Bh 0Ch 0Dh 0Eh 0Fh
Register Name: asc(M)
Default Value: HEX(M)
Description: M=[0…19]
Active switch configuration (ASC) state for output lane **M** (lane/lane mode), or group **M**, (group mode).
Writing to this register may cause the switch state to change immediately in an asynchronous manner.
Behavior is dependent on the content of register.**grpchassign** (page.00h, address.05h).

Bit(s)	Name	Description	Default	Type
[7:0]	asc(M)	0000 0000b: Route input lane/group 0 to output lane/group **M** 0000 0001b: Route input lane/group 1 to output lane/group **M** 0000 0010b: Route input lane/group 2 to output lane/group **M** 0000 0011b: Route input lane/group 3 to output lane/group **M** :: last available group 0000 1110b: Route input lane 14 to output lane **M** 0000 1111b: Route input lane 15 to output lane **M** 1111 1111b: - Disable core output lane **M** and output driver **M**, if register.**misc_ctrl.**bit[2]=0b (default) (page.11h, address.25h)	M mod 4	R/W

NOTES:

1. The M has 20 (including Auxiliary) valid lane assignments and 4 valid group assignments. Valid addresses are [00h..13h] in lane mode, [00..03h] in group mode.
2. After power up or reset, this register sets up the crosspoint into a 1:1 configuration.

Page: 03h
Address: HEX(0 + n*1) n=0...19
10h 11h 12h 13h
Register Name: asc(M)
Default Value: HEX(M)
Description: M=[0…19]
Active switch configuration (ASC) state for output lane **M** (lane/lane mode), or group **M**, (group mode).
Writing to this register may cause the switch state to change immediately in an asynchronous manner.
Behavior is dependent on the content of register.**grpchassign** (page.00h, address.05h).

Bit(s)	Name	Description	Default	Type
[7:0]	asc_aux(M)	0001 0000b: Route auxiliary input lane 0 to output lane **M** 0001 0001b: Route auxiliary input lane 1 to output lane **M** 0001 0010b: Route auxiliary input lane 2 to output lane **M** 0001 0011b: Route auxiliary input lane 3 to output lane **M** 1111 1111b: - Disable core output lane **M** and output driver **M**, if register.**misc_ctrl.**bit[2]=0b (default) (page.11h, address.25h)	0001 1111b	R/W

NOTES:

1. The M has 20 (including Auxiliary) valid lane assignments and 4 valid group assignments. Valid addresses are [00h..13h] in lane mode, [00..03h] in group mode.

5.6 PAGE 10h, Temperature Monitor

Page: 10h
Address: 00h
Register Name: temp reg#1
Default Value: 00'h
Description: Temperature monitor control register to power down the cct, strobe result, reset, and disable the circuit

Bit(s)	Name	Description	Default	Type
[7]	temp mon power down	0b: Temp monitor enable 1b: Temp monitor disable/power down	0b	R/W
[6]	temp_strobe	0b: No strobe to temp monitor 1b: Strobe to temp monitor, updates register temp read (Page10h, reg 04h)	0b	R/W
[5]	temp_reset	0b: Temp monitor normal operation 1b: Temp monitor reset	0b	R/W
[4:1]	Reserved	Reserved, set to default.	0000b	R/W
[0]	Dis temp_alarm	0b: Enable alarm monitor 1b: Disable alarm monitor	0b	R/W

Page: 10h
Address: 01h
Register Name: temp thres high
Default Value: 28'h
Description: Temperature monitor register to adjust the alarm activation high threshold

Bit(s)	Name	Description	Default	Type
[7:6]	Reserved	Reserved, set to default.	00b	R/W
[5:0]	temp alarm threshold high	00h:Threshold high set to +100C 01h:Threshold high set to +45C 02h:Threshold high set to +49C 03h:Threshold high set to +53C 04h:Threshold high set to +56C 05h:Threshold high set to +60C 06h:Threshold high set to +64C 07h:Threshold high set to +67C 08h:Threshold high set to +71C 09h:Threshold high set to +75C 0Ah:Threshold high set to +79C 0Bh:Threshold high set to +82C 0Ch:Threshold high set to +86C 0Dh:Threshold high set to +90C 0Eh:Threshold high set to +93C 0Fh:Threshold high set to +97C 10h:Threshold high set to +101C 11h:Threshold high set to +104C 12h:Threshold high set to +108C 13h:Threshold high set to +112C 14h:Threshold high set to +115C 15h:Threshold high set to +119C 16h:Threshold high set to +123C 17h:Threshold high set to +126C 18h:Threshold high set to +130C ...	10 1000b	R/W

NOTES:

1. These values were taken using Macom's MAXP-37161 Evaluation Module (EVM), system calibration is required for accurate temperature readings.
2. Step Size is about 3.68C
3. Measurements are case temperature, see Section 4.6.3 for calibration procedures.

Page: 10h
Address: 04h
Register Name: Temp Read
Default Value: na
Description: Temperature monitor readback register.

Bit(s)	Name	Description	Default	Type
[7:0]	temp read	... 17h: -40C 1Ch: -35C 21h: -30C ... 5Ch: +25C 61h: +30C 67h: +35C ... 8Ch: +70C 91h: +75C 97h: +80C 9Ch: +85C A1h: +90C A7h: +95C ACh: +100C B1h: +105C B7h: +110C BCh: +115C ...		R

NOTES:

1. Temperature strobe must be performed before reading this register to update the temperature values. See reg_temp_strobe, Page 10h, register 00h, bit[6]
2. These values were taken using Macom's MAXP-37161 Evaluation Module (EVM), system calibration is required for accurate temperature readings.
3. Step Size ~0.93C

Page: 10h
Address: 08h
Register Name: temp thres low
Default Value: 1A'h
Description: Temperature monitor register to adjust the alarm activation low threshold

Bit(s)	Name	Description	Default	Type
[7]	*overtemp pd*	0b: Over temperature power down disabled 1b: Over temperature power down enabled	0b	R
[6]	overtemp flag	0b: Over temperature alarm: Status mode 1b: Over temperature alarm: Flag mode	0b	R
[5:0]	alarm thres low	00h:Threshold high set to +100C 01h:Threshold high set to +45C 02h:Threshold high set to +49C 03h:Threshold high set to +53C 04h:Threshold high set to +56C 05h:Threshold high set to +60C 06h:Threshold high set to +64C 07h:Threshold high set to +67C 08h:Threshold high set to +71C 09h:Threshold high set to +75C 0Ah:Threshold high set to +79C 0Bh:Threshold high set to +82C 0Ch:Threshold high set to +86C 0Dh:Threshold high set to +90C 0Eh:Threshold high set to +93C 0Fh:Threshold high set to +97C 10h:Threshold high set to +101C 11h:Threshold high set to +104C 12h:Threshold high set to +108C 13h:Threshold high set to +112C 14h:Threshold high set to +115C 15h:Threshold high set to +119C 16h:Threshold high set to +123C 17h:Threshold high set to +126C 18h:Threshold high set to +130C ...	01 1010b	R

NOTES:

1. These values were taken using Macom's MAXP-37161 Evaluation Module (EVM), system calibration is required for accurate temperature readings.
2. Step Size is about 3.68C
3. Measurements are case temperature, see Section 4.6.3 for calibration procedures.

Page: 10h
Address: FCh
Register Name: Temp alarm1
Default Value: 00'h
Description: Alarm register to indicate LOR flag and temperature alarm status and flag

Bit(s)	Name	Description	Default	Type
[7:3]	*Reserved*	*Reserved (set to default)*	0 0000b	R/W
[2]	LOR alarm flag	0b: The LOR status has not changed since this bit cleared 1b: LOR status has changed since this bit cleared	0b	R/W
[1]	Temp alarm status	0b: Temperature is below the alarm threshold high, page10h, reg 01h 1b: Temperature is above the alarm threshold high	0b	R/W
[0]	Temp alarm flag	0b: No temperature alarm status has not changed since this bit cleared 1b: Temperature alarm status has changed since this bit cleared	0b	R/W

Page: 10h
Address: FDh
Register Name: Temp alarm2
Default Value: 00'h
Description: Alarm register to set masks for the LOR and temp alarm status and flag

Bit(s)	Name	Description	Default	Type
[7:3]	*Reserved*	*Reserved (set to default)*	0 0000b	R/W
[2]	LOR mask	0b: LOR alarm enabled 1b: LOR alarm masked	0b	R/W
[1]	TEMP status mask	0b: Temp alarm enabled 1b: Temp alarm masked	0b	R/W
[0]	Temp flag mask	0b: Temp sticky alarm enabled 1b: Temp sticky alarm masked	0b	R/W

5.7 PAGE 11h, Reference Clock

Page: 11h
Address: 00h
Register Name: Core Bias & refclk reg
Default Value: 08'h
Description: Reference clock control register to adjust loss-of-refclk (LOR) threshold, time constant, select CMOS or differential refclk, and power down refclk circuitry

Bit(s)	Name	Description	Default	Type
[7:6]	refclk los vth	00b: LOR threshold set to 200mV (1) 01b: LOR threshold set to 100mV 10b: LOR threshold set to 350mV 11b: LOR circuit powered down	00b	R/W
[5]	refclk los tc	0b: LOR activation Time constant set to 5us 1b: LOR activation Time constant set to 10us	0b	R/W
[4]	refclk_type	0b: Input to reference clock is CML compatible 1b: Input to reference clock is CMOS compatible (2)	0b	R/W
[3]	pd refclk	0b: Reference clock enabled 1b: Power down reference clock block	1b	R/W
[2:0]	*Reserved*	*Reserved (set to default)*	000b	R/W

NOTES:

1. REFCLK AMPLITUDE PK-PK DIFFERENTIAL FOR CML AND PK AMPLTUDE FRO CMOS.
2. DISABLES 50OHM INPUT TERMINATION (AC COUPLED FOR BOTH CMOS AND CML).
3. 000=0%,001=+10%,010=+20%,011=+30%, 100=-10%,101=-10%,110=-20%,111=-30%

5.8 PAGE 12h, Monitor Clock

Page: 12h
Address: 00h
Register Name: MCLK_ASC
Default Value: 00'h
Description: Recovered clock xpt ASC register

Bit(s)	Name	Description	Default	Type
[7:5]	*Reserved*	*Reserved (set to default)*	000b	R/W
[4:0]	rclk_asc	0 0000b: Recovered clock set to ch0 on ASC 0 0001b: Recovered clock set to ch1 on ASC ... 0 1111b: Recovered clock set to ch15 on ASC 1 1111b: Recovered clock not selected	1 1111b	R/W

Page: 12h
Address: 01h
Register Name: MCLK_ISC1
Default Value: 00'h
Description: Recovered clock xpt ISC1 register

Bit(s)	Name	Description	Default	Type
[7:5]	*Reserved*	*Reserved (set to default)*	000b	R/W
[4:0]	rclk_isc1	0 0000b: Recovered clock set to ch0 on ISC1 0 0001b: Recovered clock set to ch1 on ISC1 ... 0 1111b: Recovered clock set to ch15 on ISC1	0 0000b	R/W

Page: 12h
Address: 02h
Register Name: MCLK_ISC2
Default Value: 00'h
Description: Recovered clock xpt ISC2 register

Bit(s)	Name	Description	Default	Type
[7:5]	*Reserved*	*Reserved (set to default)*	000b	R/W
[4:0]	rclk_isc2	0 0000b: Recovered clock set to ch0 on ISC2 0 0001b: Recovered clock set to ch1 on ISC2 ... 0 1111b: Recovered clock set to ch15 on ISC2	0 0000b	R/W

Page: 12h
Address: 03h
Register Name: MCLK_SW
Default Value: 00'h
Description: Recovered clock ISC select and software strobe register

Bit(s)	Name	Description	Default	Type
[7:2]	*Reserved*	*Reserved (set to default)*	00 0000b	R/W
[1]	rclk_isc_sel	0b: Rclk sel strobe register: ISC1 1b: Rclk sel strobe register: ISC2	0b	R/W
[0]	rclk_strobe	0b: No strobe 1b: Rclk_strobe (software strobe to update asc register)	0b	R/W

Page: 12h
Address: 04h
Register Name: MCLK_SW
Default Value: 00'h
Description: Recovered clock driver swing control register

Bit(s)	Name	Description	Default	Type
[7:4]	*Reserved*	*Reserved (set to default)*	0000b	R/W
[3:1]	swing_cntl1	000b: Rclk1 swing = 200mV ppd 001b: Rclk1 swing = 400mV ppd 010b: Rclk1 swing = 600mV ppd 011b: Rclk1 swing = 800mV ppd 1xxb: Rclk1 swing =1000mV ppd	000b	R/W
[0]	pd_driver1	0b: Normal operation 1b: Power down recovered clock driver	0b	R/W

Page: 12h
Address: 05h
Register Name: MCLK_PRBS0
Default Value: 77'h
Description: Recovered clock for PRBS Checker 1 and 0

Bit(s)	Name	Description	Default	Type
[7]	*Reserved*	*Reserved (set to default)*	0b	R/W
[6:4]	rclk1_prbs1	000b: PRBS Checker1 selects RCLK from slice0 001b: PRBS Checker1 selects RCLK from slice1 010b: PRBS Checker1 selects RCLK from slice2 011b: PRBS Checker1 selects RCLK from slice3 100b: PRBS Checker1 selects the Reference Clock 101b: Reserved 111b: PRBS Checker1 powered down	111b	R/W
[3]	*Reserved*	*Reserved (set to default)*	0b	R/W
[2:0]	rclk1_prbs0	000b: PRBS Checker0 selects RCLK from slice0 001b: PRBS Checker0 selects RCLK from slice1 010b: PRBS Checker0 selects RCLK from slice2 011b: PRBS Checker0 selects RCLK from slice3 100b: PRBS Checker0 selects the Reference Clock 101b: Reserved 111b: PRBS Checker0 powered down	111b	R/W

Page: 12h
Address: 06h
Register Name: MCLK_PRBS1
Default Value: 77'h
Description: Recovered clock for PRBS Checker 3 and 2

Bit(s)	Name	Description	Default	Type
[7]	*Reserved*	*Reserved (set to default)*	0b	R/W
[6:4]	rclk1_prbs3	000b: PRBS Checker3 selects RCLK from slice0 001b: PRBS Checker3 selects RCLK from slice1 010b: PRBS Checker3 selects RCLK from slice2 011b: PRBS Checker3 selects RCLK from slice3 100b: PRBS Checker3 selects the Reference Clock 101b: Reserved 111b: PRBS Checker3 powered down	111b	R/W
[3]	*Reserved*	*Reserved (set to default)*	0b	R/W
[2:0]	rclk1_prbs2	000b: PRBS Checker2 selects RCLK from slice0 001b: PRBS Checker2 selects RCLK from slice1 010b: PRBS Checker2 selects RCLK from slice2 011b: PRBS Checker2 selects RCLK from slice3 100b: PRBS Checker2 selects the Reference Clock 101b: Reserved 111b: PRBS Checker2 powered down	111b	R/W

5.9 PAGE 1Fh, Broadcast Control

Page: 1Fh
Address: Any
Register Name: Channel Broadcast
Default Value: 00'h
Description: Broadcase page: most of the writeable channel registers (pages 20h-2Fh) can be broadcast written to all channels by writing the corresponding address in page 1Fh. It is not possible to read the broadcast registers since they are actually 16 physical registers.

The following ch addrs are not broadcastable:
20h,21h,22h,23h,24h,25h, 93h, 94h, A0h,A1h,A2h,B6h,B7h,B8h

Bit(s)	Name	Description	Default	Type
[7:0]	Any	0000 0000b: Setting page to 1F, facilitates global write to slice registers	0000 0000b	R/W

5.10 PAGE 20h to 2Fh, Channel [15:0] Rx Control

Page: HEX(32 + n*1) n=0...15
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh
Address: 10h
Register Name: chan_test
Default Value: 00'h
Description: channel self tests

Bit(s)	Name	Description	Default	Type
[7:2]	*Reserved*	*Reserved (set to default)*	00 0000b	R/W
[1]	los_clk_pd	0b: Normal operation 1b: Channel N LOS clock powered down	0b	R/W
[0]	selftest_en	0b: Normal operation 1b: Channel N Self test enabled	0b	R/W

Page: HEX(32 + n*1) n=0...15
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh
Address: 12h
Register Name: ch powerdown
Default Value: 30'h
Description: channel power down

Bit(s)	Name	Description	Default	Type
[7]	ch powerdown	0b: Normal operation 1b: Channel N powered down	0b	R/W
[6:0]	*Reserved*	*Reserved (set to default)*	011 0000b	R/W

Page: HEX(32 + n*1) n=0...15
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh
Address: 37h
Register Name: squelch level
Default Value: 00'h
Description: TX squelch control and channel inversion

Bit(s)	Name	Description	Default	Type
[7:2]	*Reserved*	*Reserved (set to default)*	00 0000b	R/W
[1:0]	squelch level	00b: Channel N, Tx Squelch level set to CM 01b: Reserved 10b: Channel N, Tx Squelch level set to LOW 11b: Channel N, Tx Squelch level set to HIGH	00b	R/W

Page: HEX(32 + n*1) n=0...15
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh
Address: 51h
Register Name: FREQ ACQ2
Default Value: 00'h
Description:

Bit(s)	Name	Description	Default	Type
[7]	lock detect pd	0b: Power down lock detect	0b	R/W
[6]	select FA mode	0b: Select pll mode	0b	R/W
[5:4]	*Reserved*	*Reserved (set to default)*	00b	R/W
[3:0]	vctrl LOL	0b: Lock threshold adjust (1h=min, fh=max)	0b	R/W

NOTES:

1. Adjusts tolerance to input sinusoidal jitter.

Page: HEX(32 + n*1) n=0...15
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh
Address: 52h
Register Name: SMART POWER
Default Value: 00'h
Description:

Bit(s)	Name	Description	Default	Type
[7:5]	set_state	000b: Normal Operation 001b: State machine stops at frequency acquisition state with PLL 010b: State machine stops at phase acquisition state with ADEQ + CDR 011b: State machine stops at phase acquisition state with DFE + CDR 100b: State machine stops at frequency acquisition state with VCO sweep 101b: Force state machine to stop at phase acquisition state with ADEQ + CDR 110b: Force state machine to stop at phase acquisition state with DFE + CDR 111b: Reserved	0b	R/W
[4:1]	*Reserved*	*Reserved (set to default)*	0b	R/W
[0]	smart_pwr	0b: Normal operation, smart power enabled 1b: Channel N smart power disabled	0b	R/W

NOTES:

1. Adjusts tolerance to input sinusoidal jitter.

Page: HEX(32 + n*1) n=0...15
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh
Address: 53h
Register Name: FREQ ACQ4
Default Value: 00'h
Description: Reading the value of the channel state machine

Bit(s)	Name	Description	Default	Type
[7:5]	*Reserved*	*Reserved*	000b	R
[4]	LOL	0b: LOL disabled 1b: LOL enabled	0b	R
[3]	*Reserved*	*Reserved*	0b	R
[2:0]	Freq Acq state	000b: Reset state 001b: FA with PLL 010b: CDR with ADEQ 011b: CDR with DFE 100b: FA with sweeping 101b: Reserved 11xb: Reserved	000b	R

Page: HEX(32 + n*1) n=0...15
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh
Address: 61h
Register Name: CDR REG2
Default Value: 00'h
Description:

Bit(s)	Name	Description	Default	Type
[7:6]	*Reserved*	*Reserved*	00b	R
[5:4]	CDR CP compensation	00b: Charge pump compensation multiplier x1 01b: Charge pump compensation multiplier x2 10b: Charge pump compensation multiplier x0.5 11b: Charge pump compensation multiplier x8	00b	R/W
[3:0]	*Reserved*	*Reserved*	0000b	R

Page: HEX(32 + n*1) n=0...15
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh
Address: 62h
Register Name: CDR REG3
Default Value: 3C'h
Description:

Bit(s)	Name	Description	Default	Type
[7:6]	vco div	00b: Channel N, VCO div1 01b: Channel N, VCO div2 10b: Channel N, VCO div4 11b: Channel N, VCO div8	00b	R/W
[5:4]	ictrl_gm_coarse	00b: Channel N, gm buffer current multiplier x1 01b: Channel N, gm buffer current multiplier x2 10b: Channel N, gm buffer current multiplier x0.5 11b: Channel N, gm buffer current multiplier x0.25	11b	R/W
[3:0]	ictrl_gm_fine	0111b: CDR gm buffer current adjust +20% ... 1111b: CDR gm buffer current adjust -15%)	1100b	R/W

Page: HEX(32 + n*1) n=0...15
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh
Address: 65h
Register Name: CDR REG4
Default Value: 08'h
Description:

Bit(s)	Name	Description	Default	Type
[7]	*Reserved*	*Reserved (set to default)*	0b	R/W
[6]	set clk test	0b: Normal operation 1b: Drive clk/2 to xpt (Slice specific register even if appears on both pages)	0b	R/W
[5:3]	sel vco	000b: Reserved 001b: Channel N, VCO select: High range (24-29G) 010b: Channel N, VCO select: Mid range (19-24G) 100b: Channel N, VCO select: Low range (14-19G) All other reserved	001b	R/W
[2]	pd qclk	0b: Normal operation 1b: Power down of Qclk generation (Slice specific register even if appears on both pages)	0b	R/W
[1]	vco core test	0b: Normal operation 1b: Enable vco core test (Slice specific register even if appears on both pages)	0b	R/W
[0]	*Reserved*	*Reserved (set to default)*	0b	R/W

Page: HEX(32 + n*1) n=0...7
20h 21h 22h 23h 24h 25h 26h 27h

Address: 80h

Register Name: LOS REG1

Default Value: 00'h

Description: Loss of signal control register#1 controling los circuit power down & hysterisis

Bit(s)	Name	Description	Default	Type
[7]	pd los	0b: Normal operation 1b: Power down LOS cct	0b	R/W
[6]	los test enable	0b: Normal operation 1b: Enable LOS test signals to atp	0b	R/W
[5]	los hystresis disable	0b: Normal Operation, LOS hysteresis enabled 1b: hysteresis disabled	0b	R/W
[4]	los force hysteresis	0b: Normal operation 1b: Force LOS hysteresis	0b	R/W
[3]	los hysteresis level	0b: LOS hysteresis 1.5dB 1b: LOS hysteresis 2.5dB	0b	R/W
[2:1]	*Reserved*	*Reserved (set to default)*	00b	R/W
[0]	never squelch	0b: Normal operation 1b: Never squelch	0b	R/W

Page: HEX(32 + n*1) n=0...15
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh
Address: 81h
Register Name: LOS REG2
Default Value: 07'h
Description: Loss of signal control register#2; select data-rate, los time constnat, los calibration, and los threshold adjustment

Bit(s)	Name	Description	Default	Type
[7]	low datarate	0b: LOS configured for high datarate (>14G) 0b: LOS configured for low datarate (<14G)	0b	R/W
[6]	los time constant	0b: LOS time constant 1us, 0b: LOS time constant 5us)	0b	R/W
[5]	los cal restart	0b: Normal operation 1b: Restart los calibration	0b	R/W
[4]	force los cal	0b: Normal operation 1b: Force los calibration	0b	R/W
[3:0]	los threshold	0000b: LOS Threshold 15mV 0001b: LOS Threshold 20mV ... 0111b: LOS Threshold 50mV (default) 1000b: LOS Threshold 60mV ... 1101b: LOS Threshold 120mV 1110b: LOS Threshold 135mV 1111b: LOS Threshold 150mV	0111b	R/W

Page: HEX(32 + n*1) n=0...15
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh
Address: 83h
Register Name: LOS CAL1
Default Value: 00'h
Description:

Bit(s)	Name	Description	Default	Type
[7]	eyemon calibrate	0b: Normal operation 1b: Eye monitoring calibration	0b	R
[6]	LOS alarm	0b: Normal operation 1b: LOS event	0b	R
[5:0]	los cal valout	00 0000b: LOS cal value readout (1)	00 0000b	R

NOTES:

1. Bit<5> is polarity, bit<0> is lsb.

Page: HEX(32 + n*1) n=0...15
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh
Address: 92h
Register Name: AFE
Default Value: 00'h
Description: Rx DC or AC coupling

Bit(s)	Name	Description	Default	Type
[7]	*Reserved*	*Reserved (set to default)*	0b	R
[6]	dc_ac	0b: AC coupling is selected for Rx 1b: DC coupling is selected for Rx	0b	R
[5:0]	*Reserved*	*Reserved (set to default)*	00 0000b	R

Page: HEX(32 + n*1) n=0...15
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh
Address: A1h
Register Name: EYEMON_CALVAL
Default Value: 00'h
Description: Eyemon coarse calibration value

Bit(s)	Name	Description	Default	Type
[7:6]	*Reserved*	*Reserved (set to default)*	00b	R/W
[5:0]	cal_val_in	00 0000b: Eyemon cal delay shift (1)	00 0000b	R/W

NOTES:

1. Coarse dll delay adjustment to be used during calibration to center the fine-tune delay range (32h<5:0>). The rnage on this dac is 4x that of the fine tune.

Page: HEX(32 + n*1) n=0...15
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh
Address: A2h
Register Name: EYEMON_CTRL
Default Value: 00'h
Description: Eyemon phase adjust value

Bit(s)	Name	Description	Default	Type
[7:6]	*Reserved*	*Reserved (set to default)*	00b	R/W
[5:0]	dll_ctrl	00 0000b: Eyemon phase adjust value (1)	00 0000b	R/W

NOTES:

1. Fine phase adjustment to be used (after successful calibration) to step through phases for eye build-up. Range is ~1.3UI.

Page: HEX(32 + n*1) n=0...15
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh
Address: B2h
Register Name: PLL_DIV_M_LSB
Default Value: 00'h
Description:

Bit(s)	Name	Description	Default	Type
[7:0]	pll_div_m_lsb	0000 0000b: PLL div by m (LSB)	0000 0000b	R/W

NOTES:

1. *00H & 01h are both equal divide-by-1 ratios (div0=div1), 02h,03h,04,05h,05h,06h,07h are reserved. Next valid divide ratio is 08h=div8.*
2. Ideally set o/p of divider to 1MHz in FA mode for good accuracy (e.g. for a 100MHz refck, div-ratio=100).

Page: HEX(32 + n*1) n=0...15
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh
Address: B3h
Register Name: PLL_DIV_M_MSB
Default Value: 00'h
Description:

Bit(s)	Name	Description	Default	Type
[7:1]	*Reserved*	*Reserved (set to default)*	000 0000b	R/W
[0]	pll_div_m_msb	0b: PLL div by m (MSB)	0b	R/W

NOTES:

1. *00H & 01h are both equal divide-by-1 ratios (div0=div1), 02h,03h,04,05h,05h,06h,07h are reserved. Next valid divide ratio is 08h=div8.*
2. Ideally set o/p of divider to 1MHz in FA mode for good accuracy (e.g. for a 100MHz refck, div-ratio=100).

Page: HEX(32 + n*1) n=0...15
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh
Address: B4h
Register Name: PLL_DIV_N_LSB
Default Value: 00'h
Description: PLL N divider value<7:0>

Bit(s)	Name	Description	Default	Type
[7:0]	pll_div_n lsb	0000 0000b: PLL div by n (LSB)	0000 0000b	R/W

NOTES:

1. PLL feedback divider. Frequency at PFD is fvco/(8*n).

Page: HEX(32 + n*1) n=0...15
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh
Address: B5h
Register Name: PLL_DIV_N_MSB
Default Value: 00'h
Description: PLL N divider value<11:8>

Bit(s)	Name	Description	Default	Type
[7:4]	*Reserved*	*Reserved (set to default)*	0000b	R/W
[3:0]	pll_div_n msb	0000b: PLL div by n (MSB)	0000b	R/W

NOTES:

1. PLL feedback divider. Frequency at PFD is fvco/(8*n).

Page: HEX(32 + n*1) n=0...15
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh
Address: B6h
Register Name: PLL_REG1
Default Value: 00'h
Description: PLL control1

Bit(s)	Name	Description	Default	Type
[7:5]	*Reserved*	*Reserved (set to default)*	000b	R
[4:0]	pll_icp_set	0 0000b: icp set to ... 1 1111b: icp set to	0 0000b	R

Page: HEX(32 + n*1) n=0...15
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh
Address: B8h
Register Name: PLL_REG2
Default Value: 43'h
Description: PLL control2

Bit(s)	Name	Description	Default	Type
[7]	*clk_div_64*	0b: Normal Operation 1b: PLL output buffer enabled	0b	R
[6:5]	pll_rclk_div	00b: Monitor clock frequency div1 01b: Monitor clock frequency div16 10b: Monitor clock frequency div32 11b: Monitor clock frequency div64	10b	R
[4:3]	*Reserved*	*Reserved (set to default)*	00b	R
[2:0]	*pll_ressistor*	000b: resistor set to ... 111b: resistor set to	011b	R

5.11 PAGE 20h to 2Fh, Channel [15:0] Tx Control

Page: HEX(32 + n*1) n=0...15
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh
Address: 30h
Register Name: TX CNTL0
Default Value: 80'h
Description: TX slew & squelch control

Bit(s)	Name	Description	Default	Type
[7]	offset enable	0b: Disable tx offset automatic cancellation 0b: Enable tx offset automatic cancellation	1b	R/W
[6]	force offset mid	0b: Force offset cancellation to mid point (1,2)	0b	R/W
[5]	force offset min	0b: Force offset cancellation to lowest point (1,2)	0b	R/W
[4]	force offset max	0b: Force offset cancellation to max point (1,2)	0b	R/W
[3]	slow slew enable2	0b: Enable slow slew option2	0b	R/W
[2]	slow slew enable1	0b: Enable slow slew option1	0b	R/W
[1]	squelch enable	0b: Enable squelch (4)	0b	R/W
[0]	force mute	0b: Force mute	0b	R/W

NOTES:

1. Bit7, offset enable must be set to "1" for this control to be effective. These coarse programmabilty bits over-ride the automatic offset cancellation.
2. Only one of these bits <6:4> can be active at a time, otherwise an invalid state results.
3. Enable1 providing ~2x slew degradation compared to enable2. Both bits can be active together.
4. Enables squelching to CM in the event of a force_mute (bit<0>) and a LOS/OOB event, the never_squelch bit (36h<1>) must be inactive during a los/oob squelch to CM. If squelching to hi/lo in event of oob/los/jtag this bit should be set to 0, and squelch_lvl is set appropriately to 10b or 11b (36h<3:2>).

Page: HEX(32 + n*1) n=0...15
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh
Address: 33h
Register Name: TX post
Default Value: 00'h
Description: TX post-cursor de-emphasis setting

Bit(s)	Name	Description	Default	Type
[7:5]	*Reserved*	*Reserved (set to default)*	000b	R/W
[4:0]	post de-emph	0 0000b: Post cursor de-emphasis magnitude (1)	0 0000b	R/W

NOTES:

1. 1LSB= 2.4% magnitude change in peak-to-settled value; DAC straight binary decode. 0h=0dB, 1f=12dB.

Page: HEX(32 + n*1) n=0...15
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh
Address: 34h
Register Name: TX pre
Default Value: 00'h
Description: TX pre-cursor de-emphasis setting

Bit(s)	Name	Description	Default	Type
[7:5]	*Reserved*	*Reserved (set to default)*	000b	R/W
[4:0]	pre de-emph	0 0000b: Pre cursor de-emphasis magnitude min (1)	0 0000b	R/W

NOTES:

1. 1LSB= 1.2% magnitude change in peak-to-settled value; DAC straight binary decode. 0h=0dB, 1f=4dB.

Page: HEX(32 + n*1) n=0...15
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh
Address: 35h
Register Name: TX swing
Default Value: 28'h
Description: TX output swing magnitude setting

Bit(s)	Name	Description	Default	Type
[7:6]	*Reserved*	*Reserved (set to default)*	00b	R/W
[5:0]	tx swing	10 1000b: Tx swing magnitude (1)	10 1000b	R/W

NOTES:

1. 1LSB=16mV; Range = 170mV to 1200mV ppd; DAC straight binary decode. Default is 800mV.

Page: HEX(32 + n*1) n=0...15
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh
Address: 36h
Register Name: TX spare
Default Value: 00'h
Description: TX squelch control and channel inversion

Bit(s)	Name	Description	Default	Type
[7:2]	*Reserved*	*Reserved (set to default)*	00 0000b	R/W
[1]	pd_tx	0b: Power down tx buffer	0b	R/W
[0]	ch invert	0b: Invert polarity of channel	0b	R/W

5.12 PAGE 30h to 33h, Slice[3:0] Control

Page: HEX(96 + n*1) n=0...3
30h 31h 32h 33h
Address: 00h
Register Name: GEN PLL DIV M LSB
Default Value: 10'h
Description:

Bit(s)	Name	Description	Default	Type
[7:0]	gen_pll_div_m_lsb	0000 0000b: PLL div by m (LSB)	0001 0000b	R/W

NOTES:

1. *00H & 01h are both equal divide-by-1 ratios (div0=div1), 02h,03h,04,05h,05h,06h,07h are reserved. Next valid divide ratio is 08h=div8.*
2. Ideally set o/p of divider to 1MHz in FA mode for good accuracy (e.g. for a 100MHz refck, div-ratio=100).

Page: HEX(96 + n*1) n=0...3
30h 31h 32h 33h
Address: 01h
Register Name: GEN PLL DIV M MSB
Default Value: 00'h
Description:

Bit(s)	Name	Description	Default	Type
[7:1]	*Reserved*	*Reserved (set to default)*	000 0000b	R/W
[0]	gen_pll_div_m_msb	0b: PLL div by m (MSB)	0b	R/W

NOTES:

1. *00H & 01h are both equal divide-by-1 ratios (div0=div1), 02h,03h,04,05h,05h,06h,07h are reserved. Next valid divide ratio is 08h=div8.*
2. Ideally set o/p of divider to 1MHz in FA mode for good accuracy (e.g. for a 100MHz refck, div-ratio=100).

Page: HEX(96 + n*1) n=0...3
30h 31h 32h 33h
Address: 02h
Register Name: GEN PLL DIV N LSB
Default Value: A5'h
Description: PLL N divider value<7:0>

Bit(s)	Name	Description	Default	Type
[7:0]	gen_pll_div_n lsb	0000 0000b: PLL div by n (LSB)	1010 0101b	R/W

NOTES:

1. PLL feedback divider. Frequency at PFD is fvco/(8*n).

Page: HEX(96 + n*1) n=0...3
30h 31h 32h 33h
Address: 03h
Register Name: GEN PLL DIV N MSB
Default Value: 00'h
Description: PLL N divider value<11:8>

Bit(s)	Name	Description	Default	Type
[7:4]	*Reserved*	*Reserved (set to default)*	0000b	R/W
[3:0]	gen_pll_div_n msb	0000b: PLL div by n (MSB)	0000b	R/W

NOTES:

1. PLL feedback divider. Frequency at PFD is fvco/(8*n).

Page: HEX(96 + n*1) n=0...3
30h 31h 32h 33h
Address: 04h
Register Name: GEN PLL REG1
Default Value: 00'h
Description: PLL Control

Bit(s)	Name	Description	Default	Type
[7:4]	*Reserved*	*Reserved (set to default)*	0000b	R/W
[3:0]	gen_pll_div_n msb	0000b: PLL set icp	0000b	R/W

Page: HEX(96 + n*1) n=0...3
30h 31h 32h 33h
Address: 08h
Register Name: GEN CDR REG2
Default Value: 3C'h
Description:

Bit(s)	Name	Description	Default	Type
[7:6]	gen_vco_div	00b: Per ch VCO div ratio value (1)	00b	R/W
[5:4]	gen_ictrl_gm_coarse	00b: CDR gm buffer current multiplier (00b=x1, 01b=x2, 10b=x0.5, 11b=x8)	11b	R/W
[3:0]	gen_ictrl_gm_fine	0000b: CDR gm buffer current adjust (7h=+20%, fh=-15%)	1100b	R/W

NOTES:

1. 0 (Div by 1), 1 (div by 2), 2 (div by 4), 3 (div by 8).

Page: HEX(96 + n*1) n=0...3
30h 31h 32h 33h
Address: 0Ah
Register Name: GEN CDR REG4
Default Value: 08'h
Description:

Bit(s)	Name	Description	Default	Type
[7:6]	*Reserved*	*Reserved (set to default)*	0b	R/W
[5:3]	gen_sel_vco	000b: Reserved 001b: Aux Channel N, VCO select: High range (24-29G) 010b: Aux Channel N, VCO select: Mid range (19-24G) 100b: Aux Channel N, VCO select: Low range (14-19G) All other reserved	001b	R/W
[2:0]	*Reserved*	*Reserved (set to default)*	0b	R/W

Page: HEX(96 + n*1) n=0...3
30h 31h 32h 33h
Address: 20h
Register Name: COUNT EVEN PRBS
Default Value: 00'h
Description: Error counter for all even bits in PRBS Checker

Bit(s)	Name	Description	Default	Type
[7:0]	PRBS EVEN COUNT	0000 0000b: PRBS EVEN MIN COUNT 1111 1111b: PRBS EVEN MAX COUNT	0000 0000b	R

Page: HEX(96 + n*1) n=0...3
30h 31h 32h 33h
Address: 21h
Register Name: COUNT ODD PRBS
Default Value: 00'h
Description: Error counter for all odd bits in PRBS Checker

Bit(s)	Name	Description	Default	Type
[7:0]	PRBS ODD COUNT	0000 0000b: PRBS ODD MIN COUNT 1111 1111b: PRBS ODD MAX COUNT	0000 0000b	R

Page: HEX(96 + n*1) n=0...3
30h 31h 32h 33h
Address: 22h
Register Name: PRBS CHKR CNTL0
Default Value: 00'h
Description: PRBS checker control register0

Bit(s)	Name	Description	Default	Type
[7]	*Reserved*	*Reserved*	0b	R
[5]	prbs chkr reset	0b: PRBS checker reset 1b: Counter is reset	0b	R/W
[5]	prbs chkr cnt reset	0b: Counter is not reset 1b: Counter is reset	0b	R/W
[4]	prbs chkr freeze	0b: No suspension to counting 1b: Suspends counting	0b	R/W
[3]	prbs chkr_en	0b: Prbs chkr en 1b: Prbs chkr disable	0b	R/W
[2]	prbs chkr polarity	0b: Prbs chkr polarity not changed 1b: Prbs chkr polarity flip	0b	R/W
[1]	prbs chkr select	0b: LFSR mode=0 open loop out of sync 1b: Closed loop in sync	0b	R/W
[0]	*Reserved*	*Reserved (set to default)*	0b	R/W

Page: HEX(96 + n*1) n=0...3
30h 31h 32h 33h
Address: 23h
Register Name: PRBS CNTL1
Default Value: 00'h
Description: PRBS checker & generator control register

Bit(s)	Name	Description	Default	Type
[7]	prbs chkr extn enable	0b: Counter reset extended one clk cycle 1b: No extension to counter reset	0b	R/W
[6:5]	*Reserved*	*Reserved (set to default)*	00b	R/W
[4]	prbs gen reset	0b: Prbs gen & chkr not reset 1b: Prbs gen & chkr reset	0b	R/W
[3]	prbs gen en	0b: Prbs gen disabled 1b: Prbs gen enabled	0b	R/W
[2]	prbs gen select	0b: Prbs31 pattern selected 1b: Prbs9 pattern selected	0b	R/W
[1]	prbs chkr cntr extn rst	0b: Counter normal operation 1b: Counter is reset (and extended if <7> active)	0b	R/W
[0]	prbs chkr dly cntl	0b: Select fsm delay adjust (24h[3:0]) 1b: Select manual cntl (25h[3:0])	0b	R/W

Page: HEX(96 + n*1) n=0...3
30h 31h 32h 33h
Address: 26h
Register Name: PRBS CNTL4
Default Value: 00'h
Description: PRBS checker sync error indication, mode selection, & status indication.

Bit(s)	Name	Description	Default	Type
[7:4]	*Reserved*	*Reserved (set to default)*	0000b	R/W
[3]	prbs chkr sync error	0b: Sync valid 1b: Receiver unable to maintain sync	0b	R
[2]	prbs chkr mode	0b: Delay calibration 1b: Error measurement	0b	R/W
[1]	prbs chkr done	0b: Fsm running or disabled 1b: Fsm process is complete	0b	R
[0]	prbs chkr run	0b: Cancel current process and enable manual interface mode 1b: Change from 0 to 1 starts the process selected by "prbs chkr mode"	0b	R/W

Page: HEX(96 + n*1) n=0...3
30h 31h 32h 33h
Address: 27h
Register Name: PRBS CNTL5
Default Value: 00'h
Description: PRBS checker problem indication and runtime selection

Bit(s)	Name	Description	Default	Type
[7]	prbs chkr closed eye	0b: Error free window found in delay cal mode 1b: No error free point exists in delay cal mode	0b	R
[6]	prbs chkr anomaly	0b: Indicates normal result 1b: Indicates presence of unexpected result	0b	R
[5:0]	prbs chkr timer	00 0000b: Controls amount of time used to measure prbs errors (00h=66ns, max 38h=152yrs) 11 1000b: Max amount of time to measure prbs errors	00 0000b	R/W

Page: HEX(96 + n*1) n=0...3
30h 31h 32h 33h
Address: 29h
Register Name: PRBS CHKR Error LSB
Default Value: 00'h
Description: PRBS checker error count (LSB)

Bit(s)	Name	Description	Default	Type
[7:0]	PRBS CHKR Error LSB	0000 0000b: Reports number of errors measured at the FSM adj point 1111 1111b: Max number of errors measured at the FSM adj point	0000 0000b	R

Page: HEX(96 + n*1) n=0...3
30h 31h 32h 33h
Address: 2Ah
Register Name: PRBS CHKR Error MSB
Default Value: 00'h
Description: PRBS checker error count (MSB)

Bit(s)	Name	Description	Default	Type
[7:0]	PRBS CHKR Error MSB	0000 0000b: Reports number of errors measured at the FSM adj point 1111 1111b: Max number of errors measured at the FSM adj point	0000 0000b	R

Page: HEX(96 + n*1) n=0...3
30h 31h 32h 33h
Address: 32h
Register Name: CHK PLL DIV M LSB
Default Value: 10'h
Description:

Bit(s)	Name	Description	Default	Type
[7:0]	chk_pll_div_m_lsb	0000 0000b: PLL div by m (LSB)	0001 0000b	R/W

NOTES:

1. *00H & 01h are both equal divide-by-1 ratios (div0=div1), 02h,03h,04,05h,05h,06h,07h are reserved. Next valid divide ratio is 08h=div8.*
2. Ideally set o/p of divider to 1MHz in FA mode for good accuracy (e.g. for a 100MHz refck, div-ratio=100).

Page: HEX(96 + n*1) n=0...3
30h 31h 32h 33h
Address: 33h
Register Name: CHK PLL DIV M MSB
Default Value: 00'h
Description:

Bit(s)	Name	Description	Default	Type
[7:1]	*Reserved*	*Reserved (set to default)*	000 0000b	R/W
[0]	chk_pll_div_m_msb	0b: PLL div by m (MSB)	0b	R/W

NOTES:

1. *00H & 01h are both equal divide-by-1 ratios (div0=div1), 02h,03h,04,05h,05h,06h,07h are reserved. Next valid divide ratio is 08h=div8.*
2. Ideally set o/p of divider to 1MHz in FA mode for good accuracy (e.g. for a 100MHz refck, div-ratio=100).

Page: HEX(96 + n*1) n=0...3
30h 31h 32h 33h
Address: 34h
Register Name: CHK PLL DIV N LSB
Default Value: A5'h
Description: PLL N divider value<7:0>

Bit(s)	Name	Description	Default	Type
[7:0]	chk_pll_div_n lsb	0000 0000b: PLL div by n (LSB)	1010 0101b	R/W

NOTES:

1. PLL feedback divider. Frequency at PFD is fvco/(8*n).

Page: HEX(96 + n*1) n=0...3
30h 31h 32h 33h
Address: 35h
Register Name: CHK PLL DIV N MSB
Default Value: 00'h
Description: PLL N divider value<11:8>

Bit(s)	Name	Description	Default	Type
[7:4]	*Reserved*	*Reserved (set to default)*	0000b	R/W
[3:0]	chk_pll_div_n msb	0000b: PLL div by n (MSB)	0000b	R/W

NOTES:

1. PLL feedback divider. Frequency at PFD is fvco/(8*n).

Page: HEX(96 + n*1) n=0...3
30h 31h 32h 33h
Address: 36h
Register Name: CHK PLL REG1
Default Value: 00'h
Description: CHK PLL control

Bit(s)	Name	Description	Default	Type
[7:5]	*Reserved*	*Reserved (set to default)*	000b	R/W
[4:0]	chk_pll_icp_set	0 0000b: icp set to ... 1 1111b: icp set to	0000b	R/W

Page: HEX(96 + n*1) n=0...3
30h 31h 32h 33h
Address: 3Ah
Register Name: CHK CDR REG2
Default Value: 3C'h
Description:

Bit(s)	Name	Description	Default	Type
[7:6]	chk_vco_div	00b: Per ch VCO div ratio value (1)	00b	R/W
[5:4]	chk_ictrl_gm_coarse	00b: CDR gm buffer current multiplier (00b=x1, 01b=x2, 10b=x0.5, 11b=x8)	11b	R/W
[3:0]	chk_ictrl_gm_fine	0000b: CDR gm buffer current adjust (7h=+20%, fh=-15%)	1100b	R/W

NOTES:

1. 0 (Div by 1), 1 (div by 2), 2 (div by 4), 3 (div by 8).

Page: HEX(96 + n*1) n=0...3
30h 31h 32h 33h
Address: 3Ch
Register Name: CHK CDR REG4
Default Value: 08'h
Description:

Bit(s)	Name	Description	Default	Type
[7:6]	*Reserved*	*Reserved (set to default)*	00b	R/W
[5:3]	chk_sel_vco	000b: Reserved 001b: PRBS Checker N, VCO select: High range (24-29G) 010b: PRBS Checkerl N, VCO select: Mid range (19-24G) 100b: PRBS Checkerl N, VCO select: Low range (14-19G) All other reserved	001b	R/W
[2:0]	*Reserved*	*Reserved (set to default)*	000b	R/W

Page: HEX(96 + n*1) n=0...3
30h 31h 32h 33h
Address: 40h
Register Name: CHK FREQ ACQ1
Default Value: 00'h
Description: Reading the value of the channel state machine

Bit(s)	Name	Description	Default	Type
[7]	lock_det_prbs_gen	0b: PRBS Gen PLL lock detect	0b	R
[6:5]	*Reserved*	*Reserved*	00b	R
[4]	chk_lol	1b: Lol active	0b	R
[3]	*Reserved*	*Reserved*	0b	R
[2:0]	chk_freq_acq_state	000b: State (0h=reset state, 01h=FA with PLL, 02h=CDR with ADEQ, 03h=CDR with DFE, 04h=FA with sweeping)	000b	R

Page: HEX(96 + n*1) n=0...3
30h 31h 32h 33h
Address: 42h
Register Name: CHK FREQ ACQ2
Default Value: 00'h
Description:

Bit(s)	Name	Description	Default	Type
[7]	*Reserved*	*Reserved (set to default)*	0b	R/W
[6]	chk select FA mode	0b: Select pll mode	0b	R/W
[5:4]	*Reserved*	*Reserved (set to default)*	00b	R/W
[3:0]	chk vctrl LOL	0000b: Lock threshold adjust (1h=min, fh=max)	0000b	R/W

NOTES:

1. Adjusts tolerance to input sinusoidal jitter.

Page: HEX(96 + n*1) n=0...3
30h 31h 32h 33h
Address: 43h
Register Name: CHK FREQ ACQ3
Default Value: 40'h
Description:

Bit(s)	Name	Description	Default	Type
[7:5]	*chk_set state*	000b: PRBS Checker N, state set to ... 000b: PRBS Checker N, state set to	010b	R/W
[4:0]	*Reserved*	*Reserved (set to default)*	0 0000b	R/W

Page: HEX(96 + n*1) n=0...3
30h 31h 32h 33h
Address: 50h
Register Name: SLICE CTRL
Default Value: 00'h
Description:

Bit(s)	Name	Description	Default	Type
[7:1]	*Reserved*	*Reserved (set to default)*	000 0000b	R/W
[0]	*Reserved*	0b: Normal operation 1b: Slice N powered down	0b	R/W

Page: HEX(96 + n*1) n=0...3
30h 31h 32h 33h
Address: 52h
Register Name: EYEMON_RESULT
Default Value: 00'h
Description: eye monitor result for selected RX channel

Bit(s)	Name	Description	Default	Type
[7:6]	*Reserved*	*Reserved*	00b	R
[5:0]	eyemon_result	00 0000b: Eyemon result min code 11 1111b: Eyemon result max code	00 0000b	R

NOTES:

1. Page33=result for slices 0,1,2, & 3; page32=result for slices 4,5,6, & 7.

Page: HEX(96 + n*1) n=0...3
30h 31h 32h 33h
Address: 53h
Register Name: EYEMON_CNTL0
Default Value: 00'h
Description: EYEMON shared sampler control0 - sampler enable<4>

Bit(s)	Name	Description	Default	Type
[7]	*Reserved*	*Reserved (set to default)*	000b	R/W
[6]	adc_pdb	0b: Normal operation - ADC sampler powered down	0b	R/W
[5:2]	adc_swing	00b: Adc input swing (2)	00b	R/W
[1:0]	adc_clk_sel	00b: Adc tempco (3)	00b	R/W

NOTES:

1. Page33=control for slices 0,1,2, & 3; page32=control for slices 4,5,6, & 7;.
2. Adc range adjusted for this expected swing. 00=232mVppd, 01=266mVppd, 10= 302mVppd, 11=336mVppd.
3. Adc tempco adjustment in ppm: 00 = 145, 01=240, 10=340, 11=520ppm. ADC ref ladder employs large salicided ploy R's.

Page: HEX(96 + n*1) n=0...3
30h 31h 32h 33h
Address: 54h
Register Name: MON_CLK
Default Value: 00'h
Description: Monitor clock input selection

Bit(s)	Name	Description	Default	Type
[7:3]	*Reserved*	*Reserved (set to default)*	0 0000b	R/W
[2:0]	mon_clk_sel	000b: Monitor clock input is Rx0 001b: Monitor clock input is Rx1 010b: Monitor clock input is Rx2 011b: Monitor clock input is Rx3 100b: Monitor clock input is PRBS Gen 101b: Monitor clock input is PRBS Checker 11xb: Reserved	000b	R/W

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