

Microwave Power Silicon Bipolar Transistor 5.0 W, 960–1215 MHz, 28V

Rev. V1

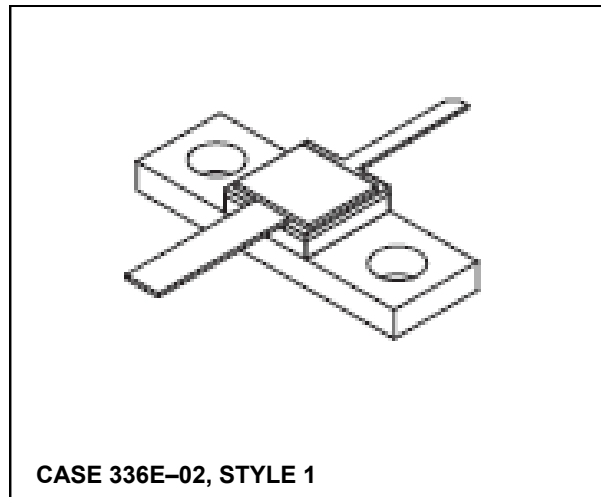
Features

- Guaranteed performance @1.215GHz, 28Vdc
- Output power: 5.0W CW
- Minimum gain = 8.5dB, 10.3dB (Typ.)
- RF performance curves for 28 Vdc and 36 Vdc operation
- 100% tested for load mismatch at all phase angles with 10:1 VSWR
- Hermetically sealed industry standard package
- Silicon nitride passivated
- Gold metallized, emitter ballasted for long life and resistance to metal migration
- Internal input matching for broadband operation

Description and Applications

Designed for CW and long-pulsed common base amplifier applications, such as JTIDS and Mode S, in the 0.96 to 1.215 GHz frequency range with high overall duty cycles.

Product Image



Maximum Ratings

| | Symbol | Value | |
|--|-----------|-------------|------------------------------|
| Collector–Emitter Voltage | V_{CES} | 55 | Vdc |
| Collector–Base Voltage | V_{CBO} | 55 | Vdc |
| Emitter–Base Voltage | V_{EBO} | 3.5 | Vdc |
| Collector Current — Continuous (1) | I_C | 1.25 | mAdc |
| Total Device Dissipation @ $T_A = 25^\circ\text{C}$ (1) Derate above 25°C | P_D | 25 143 | Watt mW/ $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | –65 to +200 | $^\circ\text{C}$ |
| Junction Temperature | T_J | 200 | $^\circ\text{C}$ |

THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|--|-----------------|-----|--------------------|
| Thermal Resistance, Junction to Case (2) | $R_{\theta JC}$ | 7.0 | $^\circ\text{C/W}$ |

NOTES:

1. These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.
2. Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

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ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | |
|---|---------------|-----|---|-----|-----|
| Collector–Emitter Breakdown Voltage ($I_C = 25\text{ mAdc}$, $V_{BE} = 0$) | $V_{(BR)CES}$ | 55 | — | — | Vdc |
| Collector–Base Breakdown Voltage ($I_C = 25\text{ mAdc}$, $I_E = 0$) | $V_{(BR)CBO}$ | 55 | — | — | Vdc |
| Emitter–Base Breakdown Voltage ($I_E = 0.5\text{ mAdc}$, $I_C = 0$) | $V_{(BR)EBO}$ | 3.5 | — | — | Vdc |
| Collector Cutoff Current ($V_{CB} = 28\text{ Vdc}$, $I_E = 0$) | I_{CBO} | — | — | 1.0 | mA |

ON CHARACTERISTICS

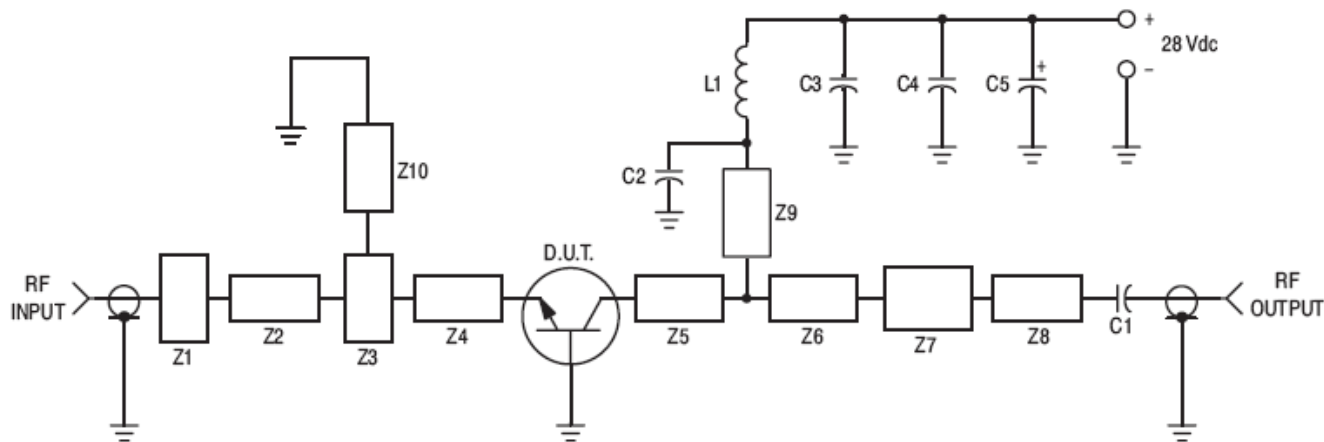
| | | | | | |
|---|----------|----|---|-----|---|
| DC Current Gain ($I_C = 500\text{ mAdc}$, $V_{CE} = 5.0\text{ Vdc}$) | h_{FE} | 20 | — | 100 | — |
|---|----------|----|---|-----|---|

DYNAMIC CHARACTERISTICS

| | | | | | |
|--|----------|---|-----|----|----|
| Output Capacitance ($V_{CB} = 28\text{ Vdc}$, $I_E = 0$, $f = 1.0\text{ MHz}$) | C_{ob} | — | 7.0 | 10 | pF |
|--|----------|---|-----|----|----|

FUNCTIONAL TESTS

| | | | | | |
|---|----------|--------------------------------|------|---|----|
| Common–Base Amplifier Power Gain ($V_{CC} = 28\text{ Vdc}$, $P_{out} = 5.0\text{ W}$, $f = 1215\text{ MHz}$) | G_{PB} | 8.5 | 10.3 | — | dB |
| Collector Efficiency ($V_{CC} = 28\text{ Vdc}$, $P_{out} = 5.0\text{ W}$, $f = 1215\text{ MHz}$) | η | 45 | 55 | — | % |
| Load Mismatch ($V_{CC} = 28\text{ Vdc}$, $P_{out} = 5.0\text{ W}$, $f = 1215\text{ MHz}$, VSWR = 10:1 All Phase Angles) | ψ | No Degradation in Output Power | | | |



C1, C2, C3 — 220 pF 100 mil Chip Capacitor
 C4 — 0.1 μF
 C5 — 47 $\mu\text{F}/50\text{ V}$ Electrolytic
 L1 — 3 turn #18 AWG, 1/8" ID, 0.18" Long

Z1–Z10 — Microstrip, see details below
 Board Material — 0.030" Glass Teflon,
 2.0 oz. Copper, $\epsilon_r = 2.55$

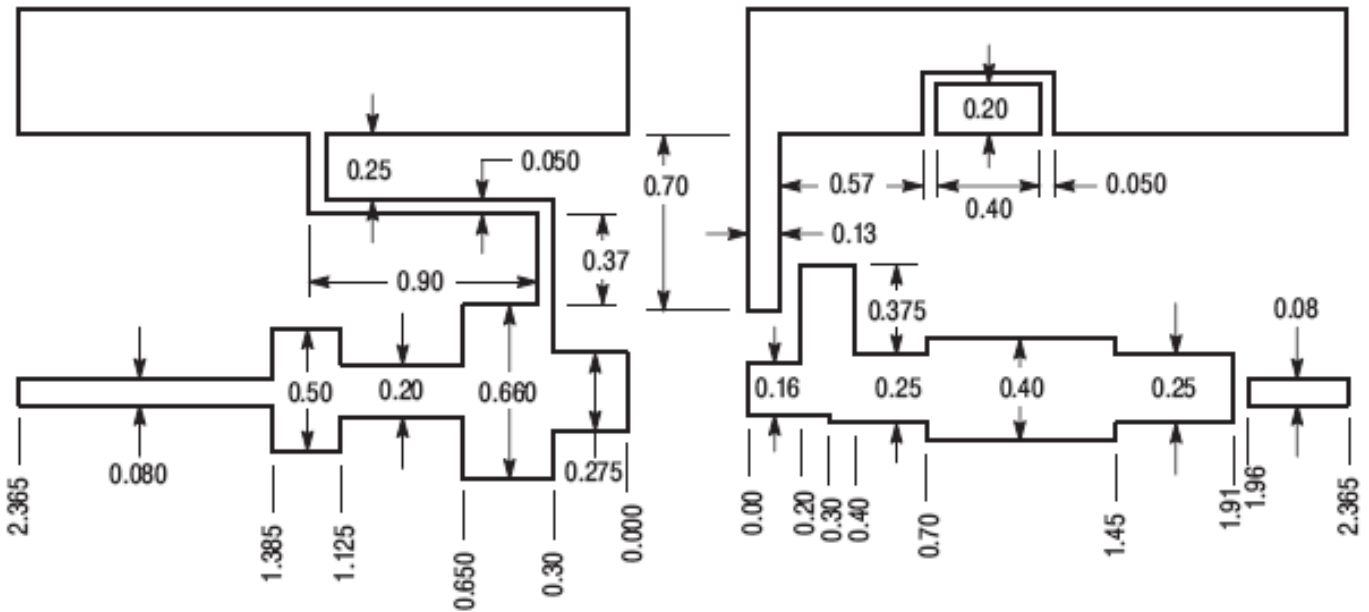


Figure 1. Test Circuit

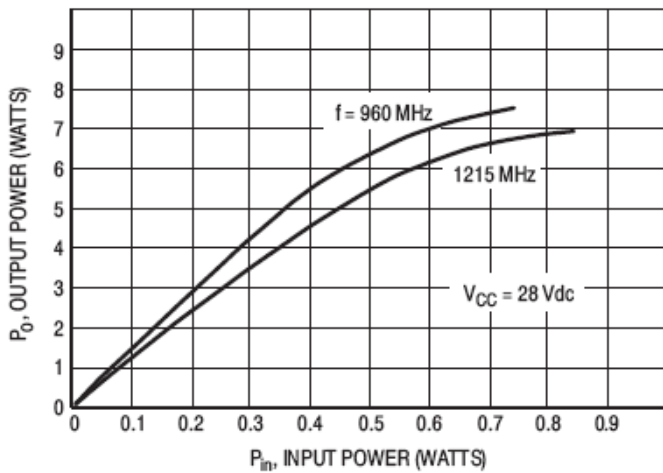


Figure 2. Output Power versus Input Power

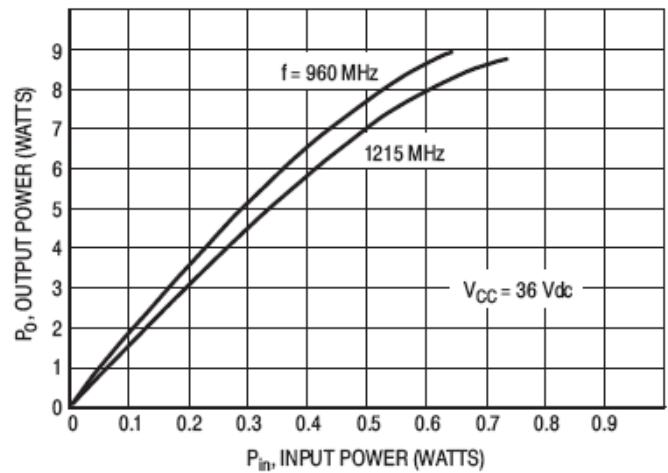
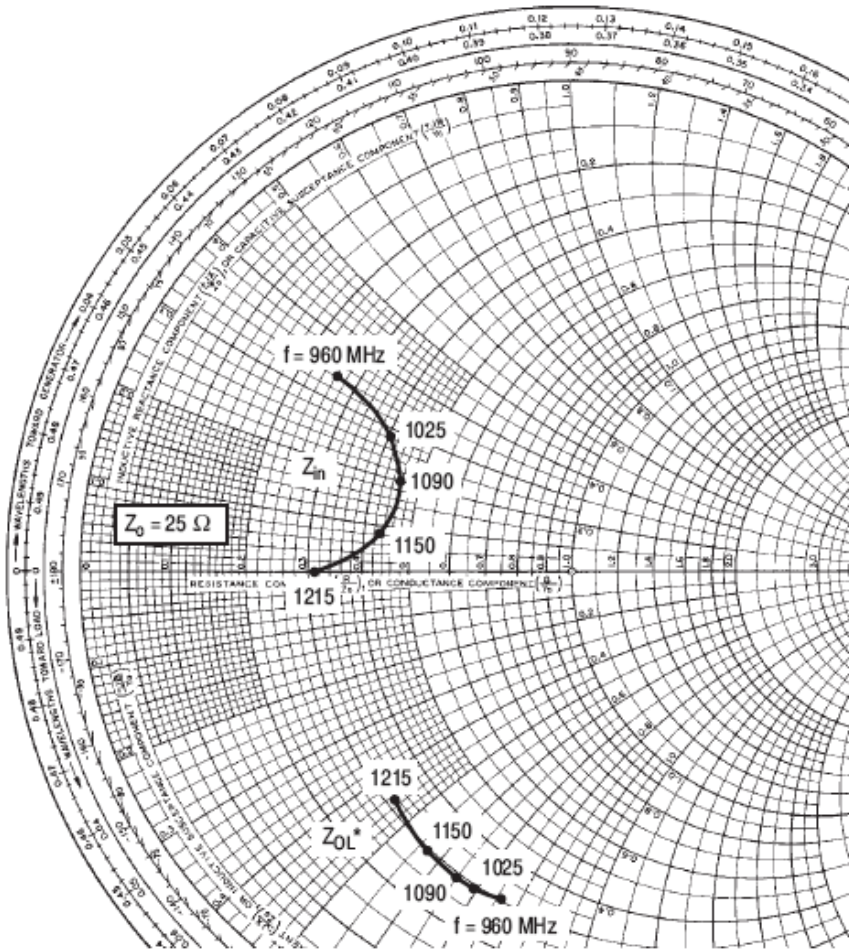


Figure 3. Output Power versus Input Power



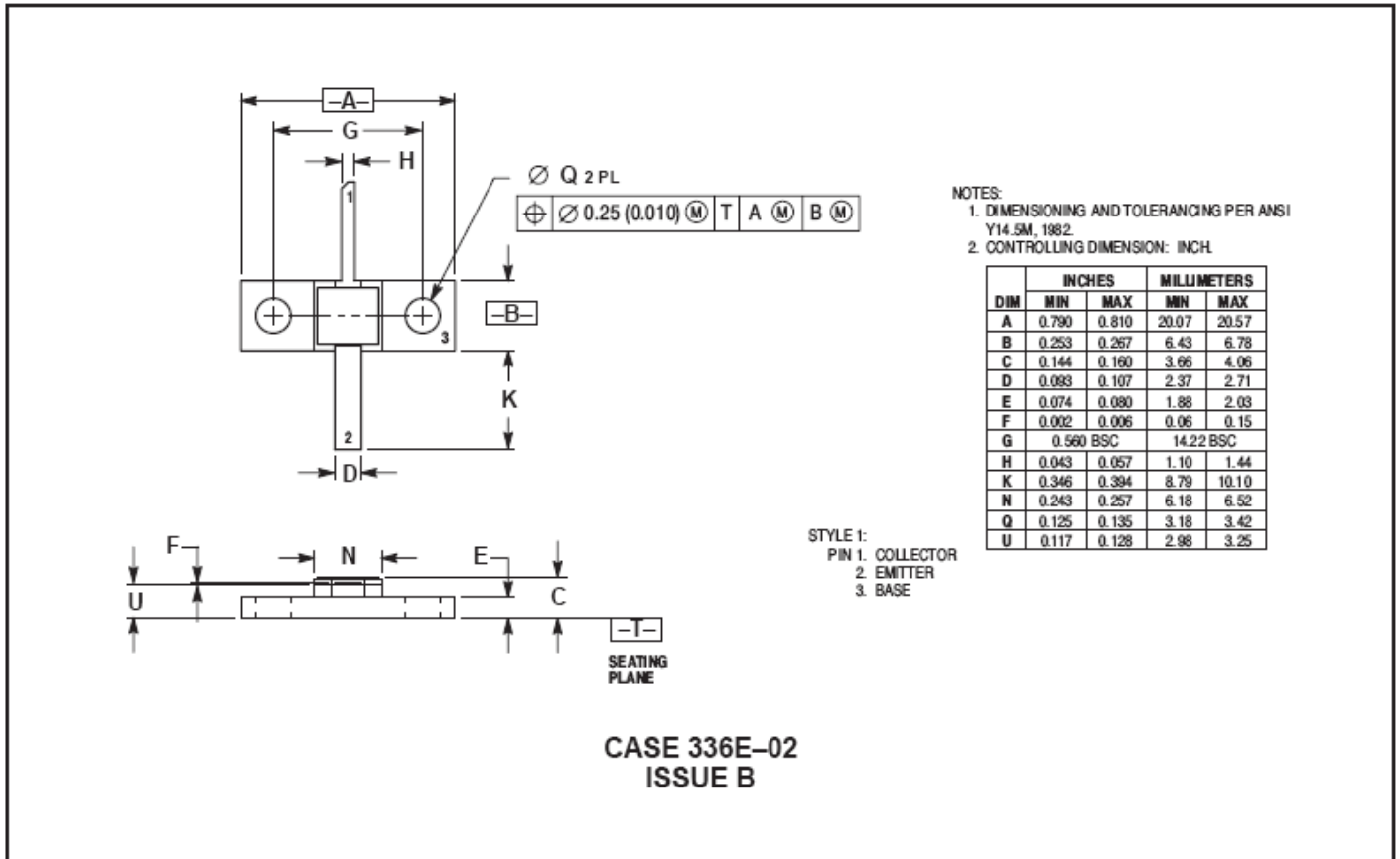
$P_{out} = 5\text{ W}, V_{CC} = 28\text{ V}$

| f MHz | Z_{in} OHMS | Z_{OL}^* OHMS |
|----------|------------------|--------------------|
| 960 | 6.5 + j8.5 | 7.4 - j18.9 |
| 1025 | 10.0 + j7.0 | 7.2 - j17.4 |
| 1090 | 11.2 + j4.9 | 7.1 - j16.3 |
| 1150 | 10.8 + j2.0 | 7.15 - j14.3 |
| 1215 | 7.8 + j0.0 | 7.8 - j11.2 |

Z_{OL}^* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 4. Series Equivalent Input/Output Impedances

PACKAGE DIMENSIONS



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