

Features

- Integrates Image Reject (Balanced) Mixer, LO Buffer, LO Doubler and RF Buffer
- 7 dB Conversion Gain (USB)
- -25 dBm (2x) LO Leakage (at RF Port)
- 26 dBm OIP3
- Variable Gain with Adjustable Bias
- Lead-Free 4mm 24-lead QFN Package
- 100% RF and DC Testing
- RoHS* Compliant and 260°C Reflow Compatible

Description

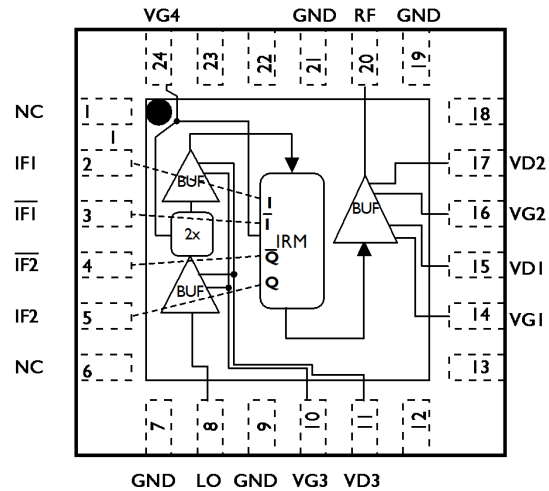
The XU1019-QH is a 37.0-40.0 GHz GaAs MMIC Integrated up-converter that has a typical conversion gain of 7 dB, and an image rejection of greater than 15 dBc. It has been optimized for USB operation. The device includes a LO doubler and buffer, and can be tuned to give 2xLO leakage of less than -25 dBm. Variable gain regulation can be achieved by adjusting the bias, with turn-down trajectories optimized to maintain linearity and minimal 2xLO leakage over the gain control range. At full gain, an OIP3 of 26 dBm is typical.

The device comes in an RoHS compliant 4x4mm QFN surface mount package offering excellent RF and thermal properties. Typical application for this device are as an up-converter stage in a linear 38 GHz radio transmit lineup. This device has been designed for use in 38 GHz Point-to-Point Microwave Radio applications.

Ordering Information

Part Number	Package
XU1019-QH-0G00	bulk quantity
XU1019-QH-0G0T	tape and reel
XU1019-QH-EV1	evaluation module

Functional Schematic



Pin Configuration ¹

Pin No.	Function	Pin No.	Function
1	Not Connected	13	Not Connected
2	IF1 Input	14	Gate 1 Bias
3	IF1* Input	15	Drain 1 Bias
4	IF2* Input	16	Gate 2 Bias
5	IF2 Input	17	Drain 2 Bias
6	Not Connected	18	Not Connected
7	GND	19	GND
8	LO Input	20	RF Output
9	GND	21	GND
10	Gate 3 Bias	22	Not Connected
11	Drain 3 Bias	23	Not Connected
12	Not Connected	24	Gate 4 Bias

1. The exposed pad centered on the package bottom must be connected to RF and DC ground.

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

Up Converter 37.0 - 40.0 GHz

Rev. V2

Electrical Specifications: (Ambient Temperature T = +25°C)

Parameter	Units	Min.	Typ.	Max.
Frequency Range (RF)	GHz	37.0	-	40.0
Frequency Range (LO) ²	GHz	16.75	-	20.0
Frequency Range (IF)	GHz	DC	-	3.5
LO Input Power (P _{lo})	dBm	0	-	6.0
Conversion Gain	dB	5.0	7.0	9.0
Image Rejection	dBc	15	-	-
Output IP3 (OIP3)	dBm	23.0	26.0	-
Spurious (2xLO) [tuned]	dBm	-25	-	-
Spurious (1xLO)	dBm	-45	-	-
Noise Figure (NF)	dB	-	18.5	-
Input Return Loss (IF port)	dB	-	7.0	-
Output Return Loss (RF Port)	dBm	-	7.0	-
LO Return Loss	dB	-	7.0	-
Drain Bias Voltage (V _{d1,2,3})	V	-	4.0	4.0
Drain Current (I _{d1})	mA	-	120	150
Drain Current (I _{d2})	mA	-	120	150
Drain Current (I _{d3})	mA	110	150	180
Gate Voltage (V _{g4})	V	-	-3	-
Gate Current (I _{g4})	mA	-	7	-

2. LO frequency range limits the performance characteristics to USB only.

Absolute Maximum Ratings

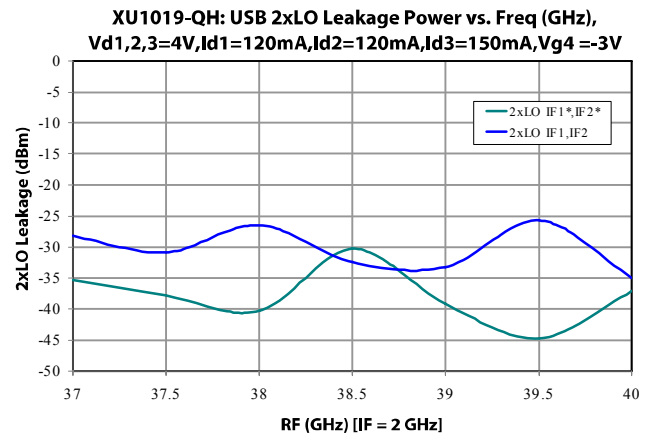
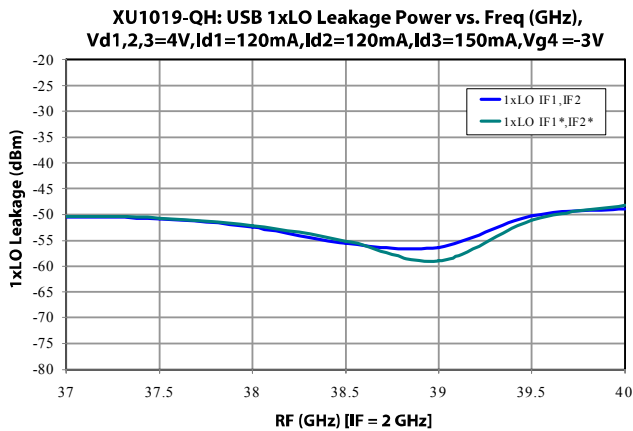
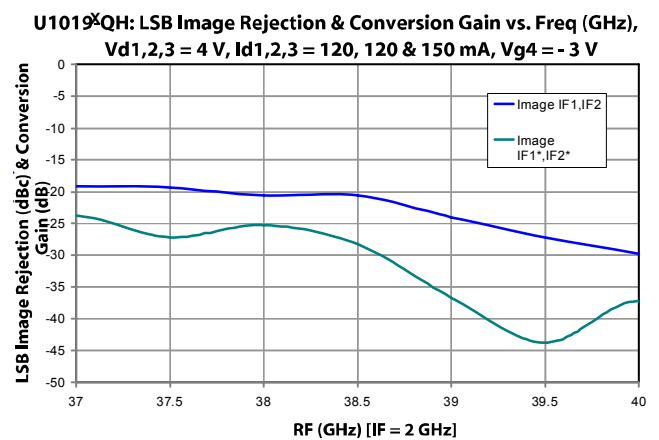
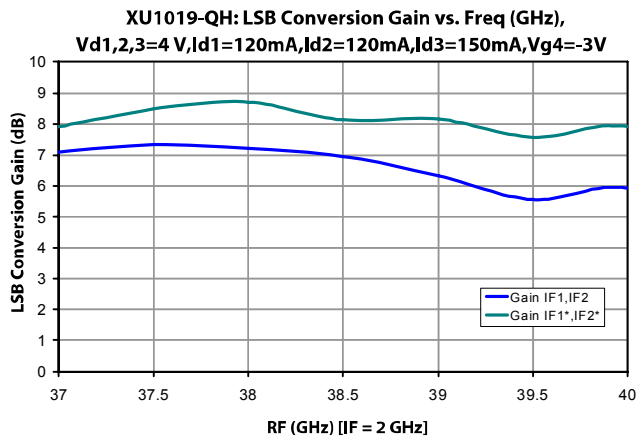
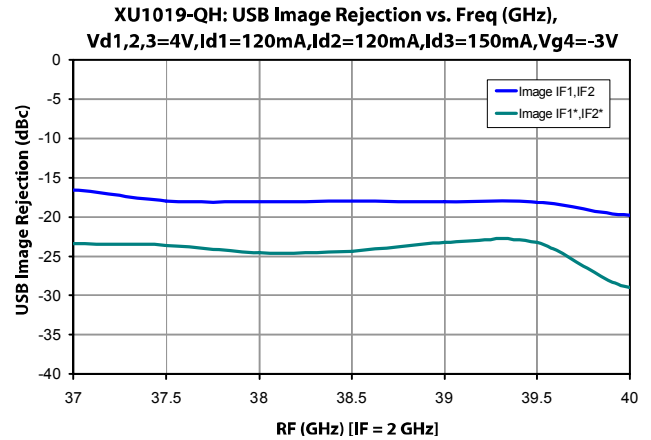
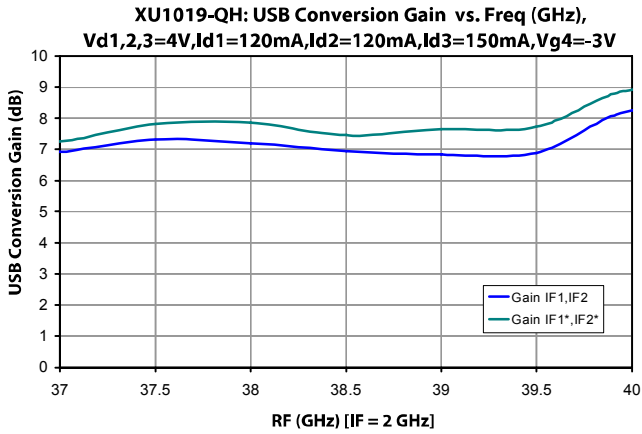
Parameter	Absolute Max.
Supply Voltage (V _{d1,2,3})	+4.3 V
Drain Current (I _{d1+2+3})	480 mA
Gate Bias Voltage (V _{g1,2,3})	1.5V < V _g < 0V
Gate Bias Voltage (V _{g4})	-4.0 V min.
Input Power (P _{in})	+10 dBm
LO Input Power (LO _{in})	+13 dBm
Storage Temperature (T _{stg})	-65°C to +165°C
Operating Temperature (T _a)	-55°C to +85°C
Operating Junction/Channel Temp	150°C
Mounting Temperature	See solder reflow profile
ESD Min. - Machine Model (MM)	Class A
ESD Min. - Human Body Model (HBM)	Class 1A
MSL Level	MSL3

2

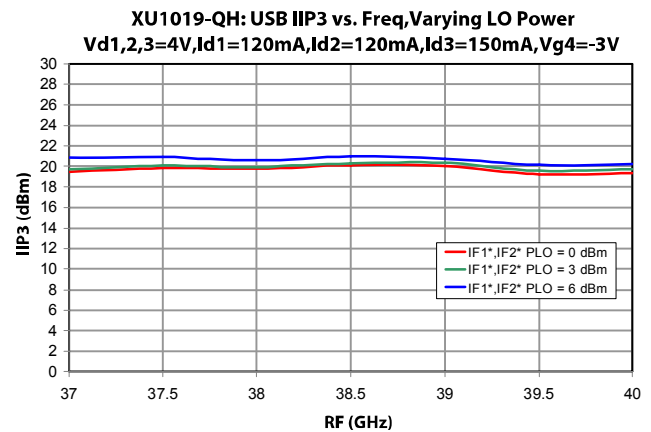
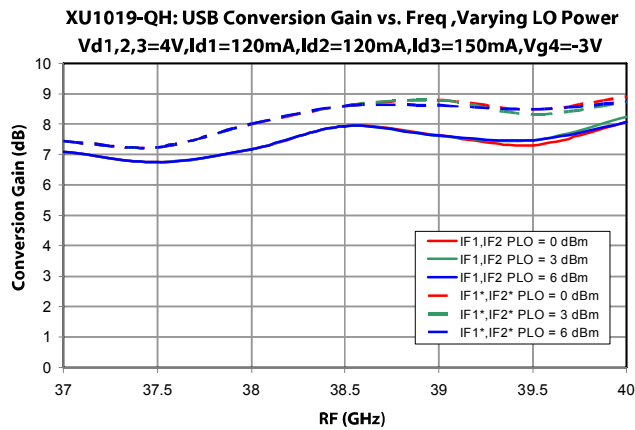
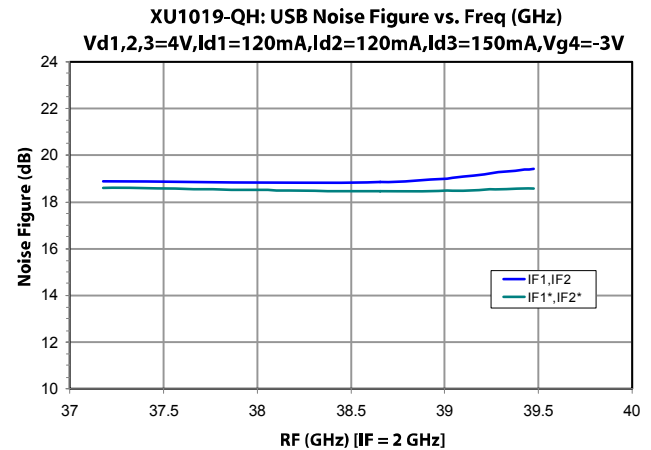
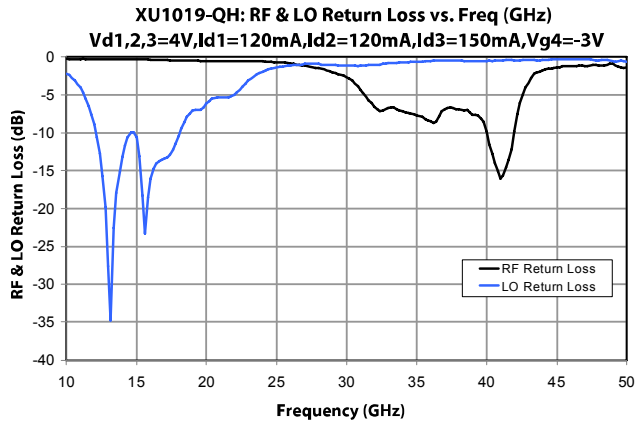
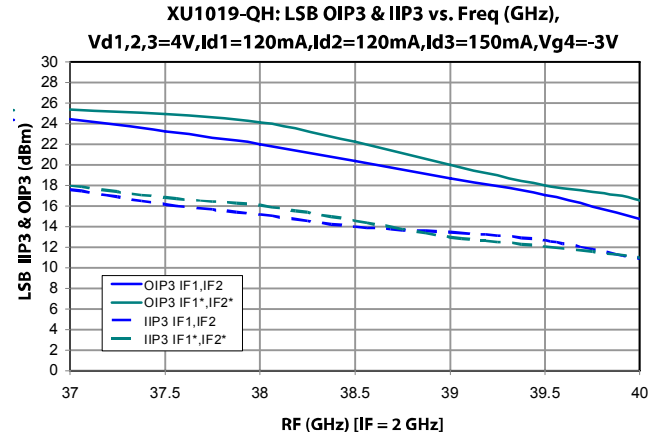
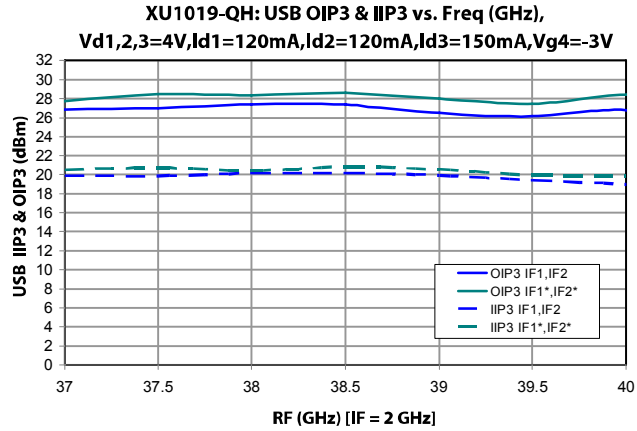
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Typical Performance Curves

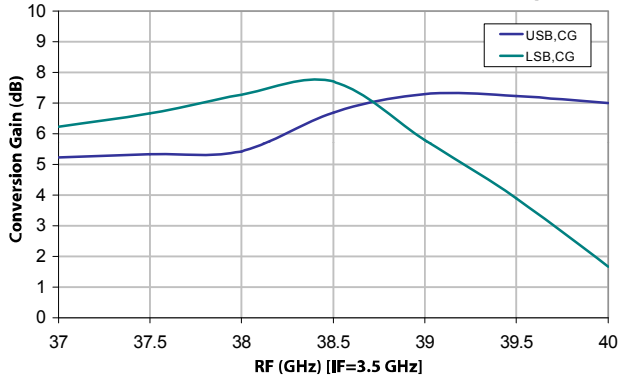


Typical Performance Curves (cont.)

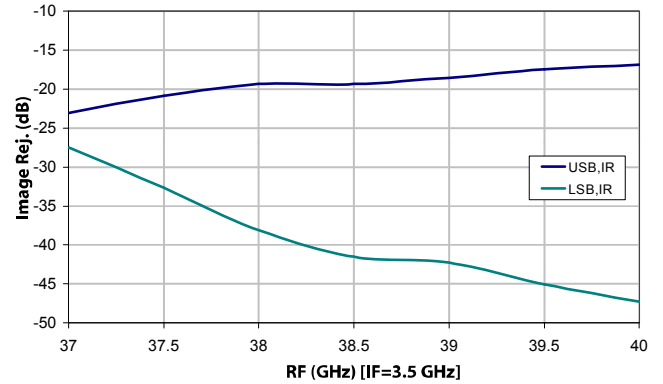


Typical Performance Curves (cont.)

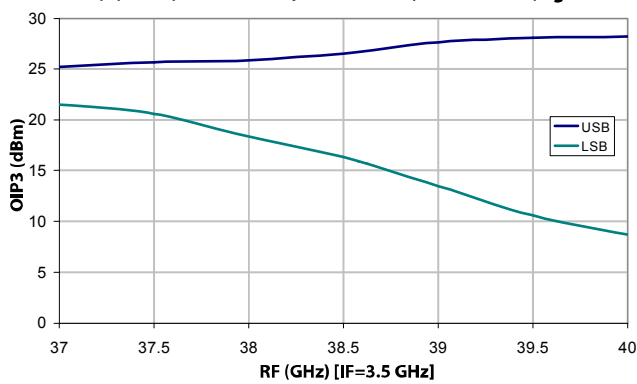
XU1019-QH: Conversion Gain vs Freq, Pscl=0 dBm, IF1/IF2 used
Vd1,2,3=4V; Id1=120 mA, Id2=120 mA, Id3=150 mA, Vg4=-3V



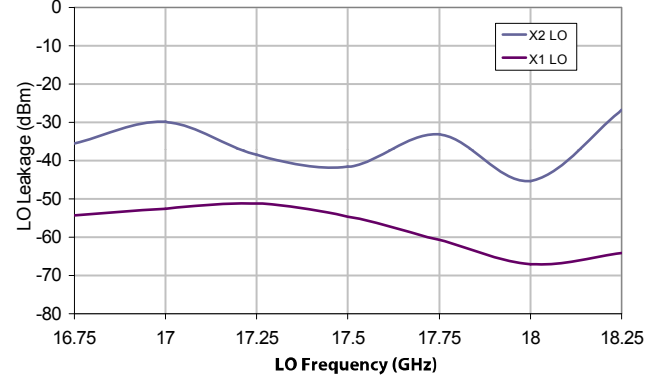
XU1019-QH: Image Rejection vs Freq, Pscl=0 dBm, IF1/IF2 used
Vd1,2,3=4V; Id1=120 mA, Id2=120 mA, Id3=150 mA, Vg4=-3V



XU1019-QH: OIP3 vs Freq, Pscl=0 dBm, IF1/IF2 used
Vd1,2,3=4V; Id1=120 mA, Id2=120 mA, Id3=150 mA, Vg4=-3V

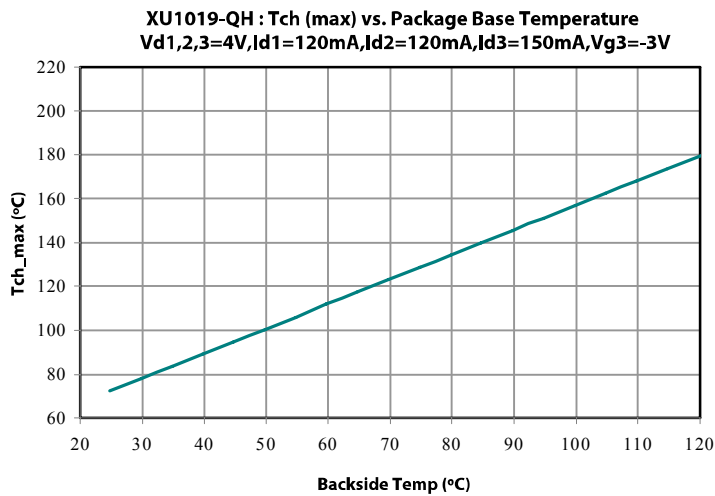
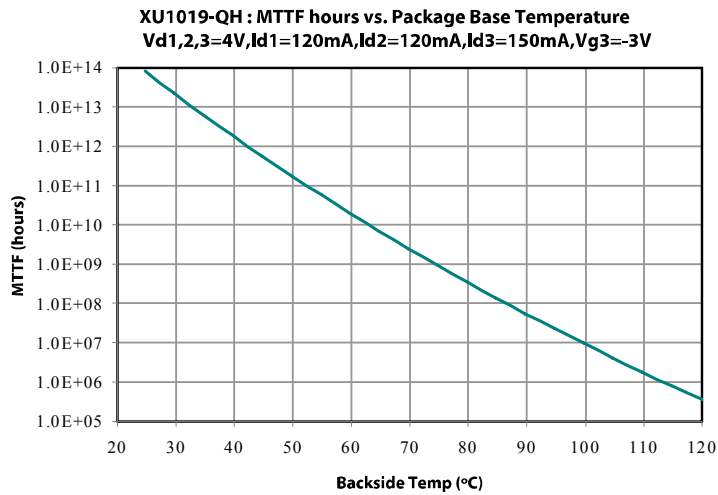


XU1019-QH: (USB) LO Leakage vs LO Freq, Plo=3 dBm
Vd1,2,3=4V; Id1=120 mA, Id2=120 mA, Id3=150 mA, Vg4=-3V



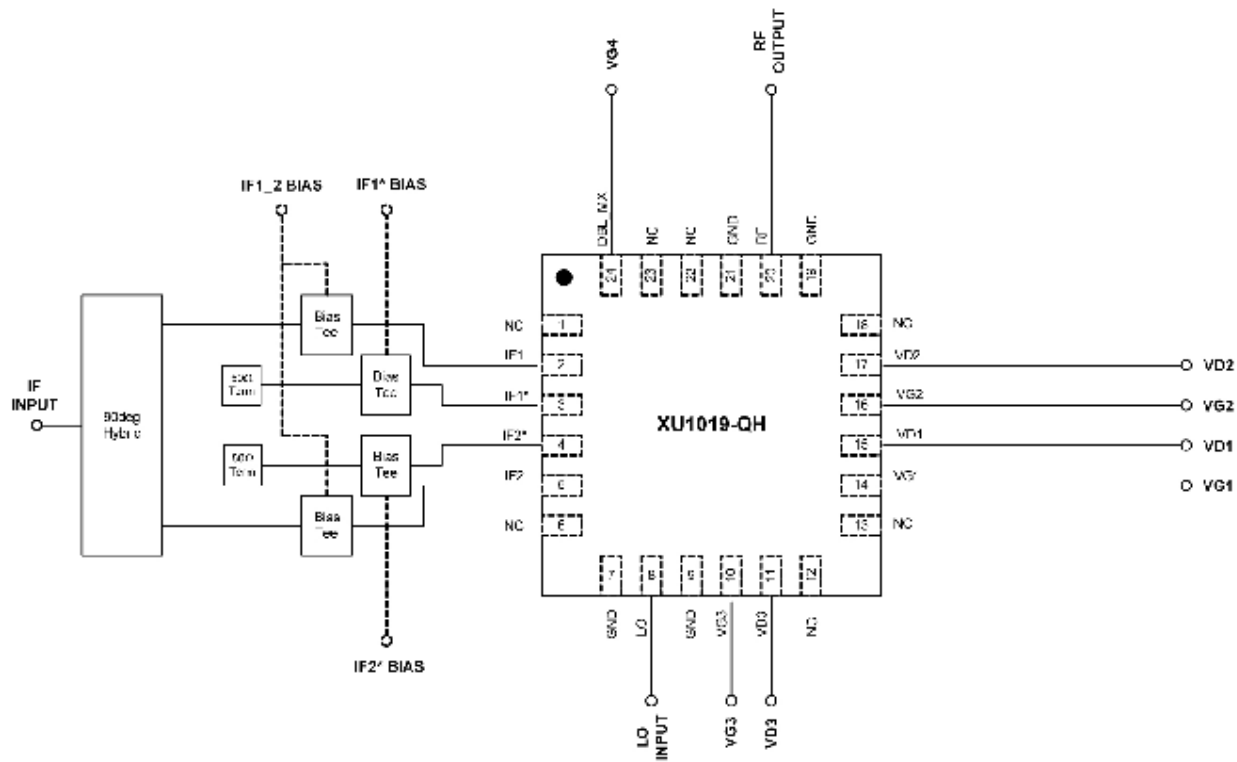
MTTF

These numbers were calculated based on accelerated life test information and thermal model analysis received from the fabricating foundry.



App Note [1] Biasing - As shown in the Pin Designations table, the device is operated by biasing Vd1, Vd2, and Vd3 at 4.0 V. The corresponding drain currents are set to 120 mA, 120 mA, and 150 mA respectively. Vg4 requires a fixed voltage bias of nominally -3 V. It is recommended to use active bias on Vg1, Vg2, Vg3 to keep the currents in Vd1, Vd2, and Vd3 constant, in order to maintain the best performance over temperature. Depending on the supply voltages available and the power dissipation constraints, the bias circuits may include a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply to sense the current. Make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

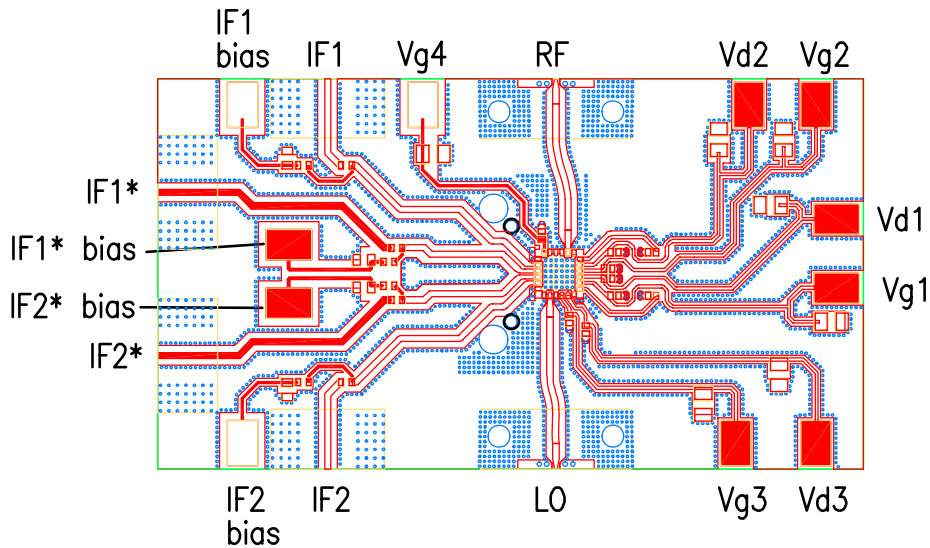
App Note [2] IF1/IF2 versus IF1*/IF2* - The IF input to the typical configuration is through a 90deg hybrid coupler. The hybrid splits the IF input into inphase and quadrature phase components. These two signals enter the XU1019-QH on either the IF1/IF2 pair, or the IF1*/IF2* complimentary pair. Which ever pair are not used must be terminated into 50 Ω. There are subtle differences between the performance when using the main IF ports (IF1,IF2) versus the complimentary ports (IF1*, IF2*) which are shown in the preceding performance curves. For highest gain, best image rejection and lowest noise figure, the complimentary ports (IF1*, IF2*) should be used.



Typical Configuration

App Note [3] Board Layout - As shown in the recommended board layout, it is recommended to provide 100 pF decoupling capacitors as close to the bias pins as possible. Additional 10 nF and 1 μ F on each of the bias lines are recommended placed a distance further away.

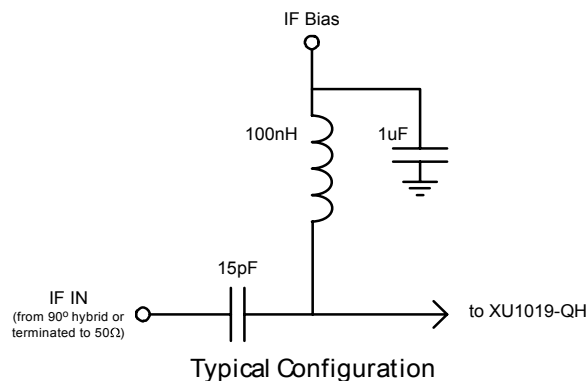
Recommended Board Layout



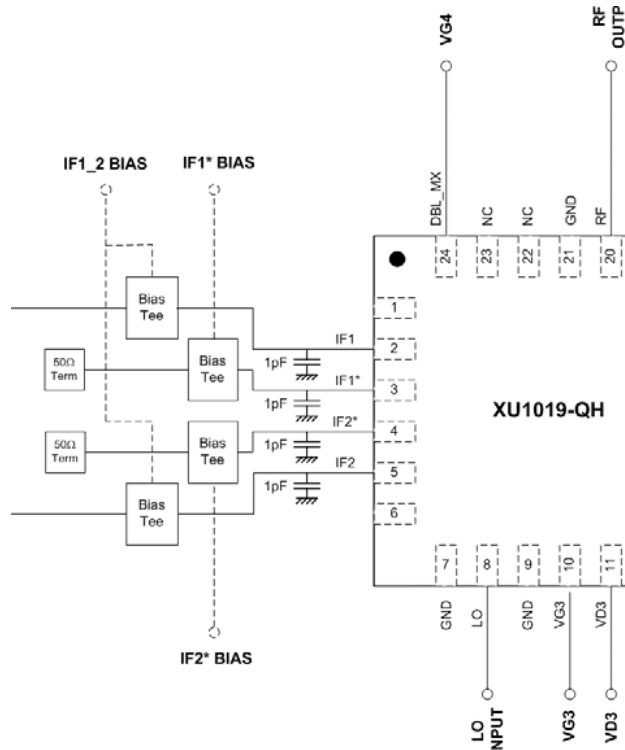
App Note [4] IF Bias - To obtain optimum 2xLO leakage performance, tuning is achieved by adjusting the DC bias on each of the IF inputs (IF1, IF2, IF1*, IF2*). DC bias is implemented by adding simple bias tees to each of the four IF ports. The diagram below shows a typical bias tee design used.

If the IF1 and IF2 ports are used for the IF input, the IF1* and IF2* ports are DC biased and terminated into 50 Ω . A typical tuning arrangement is to apply a fixed 0.3 V DC bias to both the used IF input ports (i.e. IF1,IF2 or IF1*,IF2*). The remaining two IF ports which have been terminated to 50 Ω tuning independently for minimum 2xLO leakage.

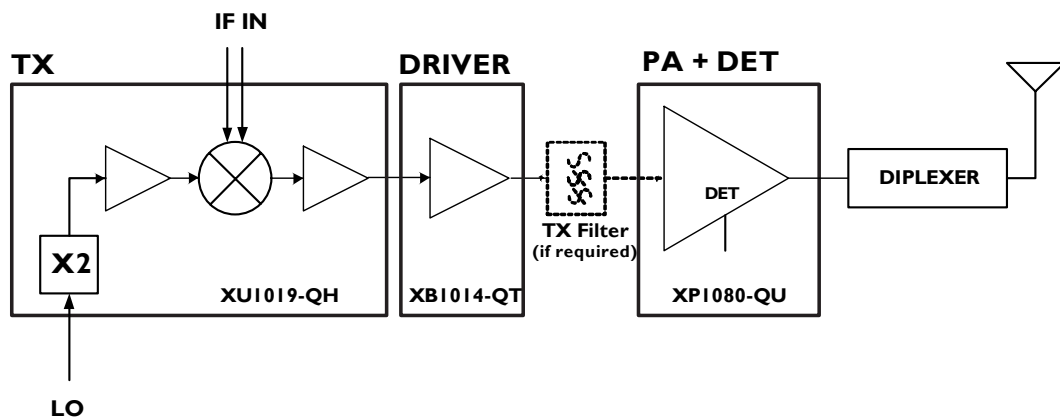
For minimum 2xLO leakage in a system, it may be necessary to correct the IF DC bias for different frequency and temperature conditions. This can be implemented by calibration and offset tables stored in memory, and used to control IF bias over all practical conditions.



App Note [5] Extended IF Frequency Range - If using the XU1019-QH using IF frequencies greater than 2 GHz, conversion gain roll-off can be minimized by placing 1pF capacitors on each of the four IF ports. The capacitors should be placed close to the package, between the bias tees and the package.



Typical Application



Lead-Free 4 mm 24-Lead PQFN†

TOP VIEW

Pin 1 Dot By marking

xxxxxyy
aaaaa
cyywpp

BOTTOM VIEW

.35 X .35 CHAMFER

MARKINGS:
PIN 1/BOM REV/Pb FREE SYM
MIMIX PART/MODEL NO.
WAFER LOT NUMBER
DATE CODE

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

NOTES:
1. DIMENSIONS ARE IN MM.

	MIN	TYP	MAX
A	0.80	0.90	1.00
A3	0.20 REF		
b	0.20	0.25	0.30
K	0.20	-	-
D	4.00 BSC		
E	4.00 BSC		
e	0.50		
D2	2.45	2.60	2.75
E2	2.45	2.60	2.75
L	0.20	0.30	0.40

1. VIEWS ARE NOT TO SCALE: USE DIMENSIONS AND TABLE.

† Reference Application Note S2083 for lead-free solder reflow recommendations.
Plating is 100% matte tin over copper.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

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