MXM1120

Digital Hall Sensor

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Ver. 2.4

This document is subject to change without notice

1. Overview

MXM1120 is the digital Hall sensor in measuring the intensity of the magnetic flux through selecting options of the various sensitivity with the low power consumption providing a built-in 10 bits ADC digital output. It can also detect the open/close state for many applications by one or multiple external magnets. This sensor is comprised of a Hall element, an offset cancellation circuitry, a programmable gain amplifier, a 10-bits low power ADC, and control logic in a single chip. The adjustment of the open/close state threshold values, the magnetic polarity, and the operation period can be programmed through I2C interface. The software package supports to convert the magnetic strength into the angle or distance by detecting intensity of flux between the external magnet and the sensing element. Because the small WLCSP and SOP package, the low current consumption, and the stable performance, Our MXM1120 can be used in the hand set and consumer electronics and any other industries. One of the typical applications in the smart phone is the lid opening angle measurement system.

◆ **Functions:**

- Magnetometer device for magnets on external equipment
- Built-in analog to digital converter for magnetometer data outputs
- 10/8-bits selectable data outputs for each built-in Hall element
- I2C bus interface:
  - Standard mode and fast mode compliant with Philips I2C specification Ver.2.1
- Interrupt function: When magnetic intensity level sensed is higher than upper threshold level or lower than lower threshold level, interrupt signal is generated through INTB PAD.
- Configurable magnetic sensitivity level and measurable range, for example;
  - High sensitivity mode: ±2.5mT (typically) at 5uT/LSB (10bit)
  - High dynamic range mode: ±40.8mT (typically) at 80uT/LSB (10bit)
- Built-in oscillator for internal clock source
- Power on Reset circuit

◆ **Operating temperature:**

- -30°C to +85°C

◆ **Operating supply voltage:**

- Analog power supply (VDD): +2.7V to +3.6V (3.0V typical)
- Digital Interface supply (VID): +1.65V to VDD (1.8V typical)

◆ **Current consumption:**

- Power-down mode: 1 µA typically
- Normal operating mode: 18µA typically at 10 Hz operating frequency (OPF[2:0] = “001”)

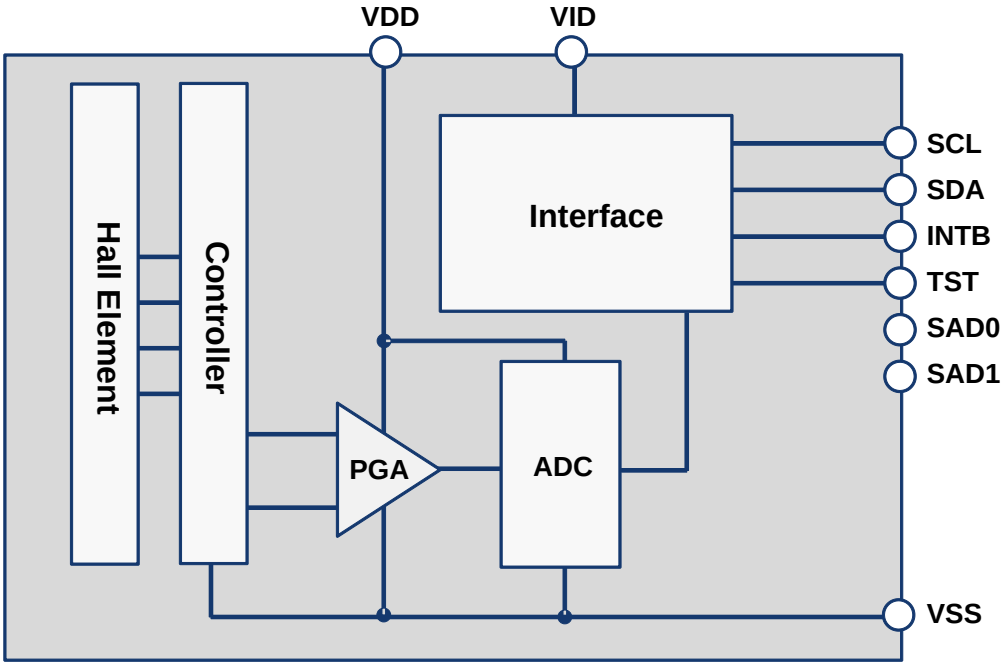
◆ **Package:**

- MXM1120 9-pin WL-CSP (BGA): 1.33 mm × 1.33 mm × 0.5 mm (typically)

2. Table of Contents

3. Circuit Configuration

3.1. Block Diagram



3.2. Pin Function

WLCSP Pin No.	Pin Name	I/O	Power level	Type	Function
B1	SDA	I/O	VID	CMOS	Control data input/output pin Input: Schmidt trigger, Output: Open drain
A2	VDD	-	-	Power	Internal block power supply pin
B2	SCL	I	VID	CMOS	Control data clock input pin Input: Schmidt trigger
B3	VSS	-	-	Power	Ground pin
A3	SAD1	I	VDD	CMOS	Slave address 1 input pin Connect to VSS or VDD (not VID)
C3	INTB	O	VID	CMOS	When detected magnetic flux density meets specific threshold level, INTB become low level during specific duration. (“L” active)
C2	VID	-	-	Power	Interface block power supply pin
C1	TST	I	VDD	CMOS	Test purpose only Should be connected to GND.
A1	SAD0	I	VDD	CMOS	Slave address 0 input pin Connect to VSS or VDD (not VID)

4. Overall Characteristics

4.1. Absolute Maximum Ratings

VSS = 0 V

Parameter	Symbol	Min.	Max.	Unit
Power supply voltage (VDD, VID)	V+	-0.3	+4.3	V
Input voltage	VIN	-0.3	(V+)+0.3	V
Input current	IIN	-	± 10	mA
Storage temperature	TST	-40	+125	°C

(Note 1) If the device is used in conditions exceeding these values, the device may be destroyed. Normal operations are not guaranteed in such exceeding conditions.

4.2. Recommended Operating Conditions

VSS = 0 V

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	Ta	-30		+85	°C
Power supply voltage (VDD)	Vdd	2.7	3.0	3.6	V
Power supply voltage (VID)	Vid	1.65		Vdd	V

4.3. Electrical Characteristics

The following conditions is applied unless otherwise noted:
Vdd=2.7V to 3.6V, Vid=1.65V to Vdd, Temperature range=-30°C to 85°C

4.3.1. DC Characteristics

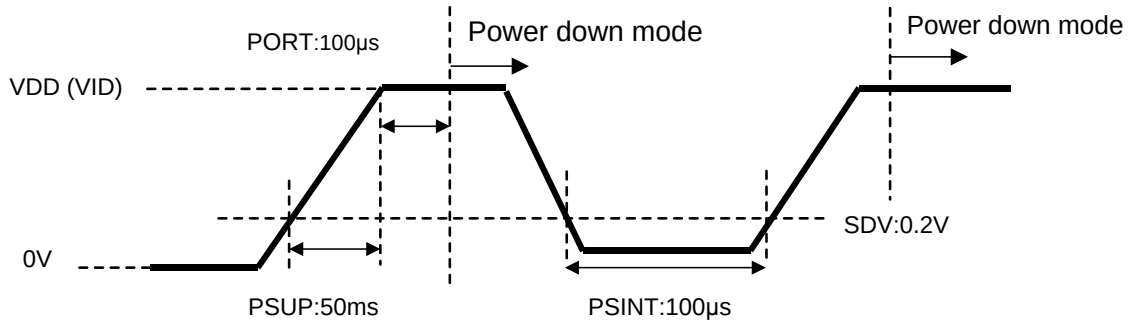
Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level input voltage 1	VHI1	SCL SDA		80%Vid		Vid+0.5	V
Low level input voltage 1	VIL1			-0.5		20%Vid	V
High level input voltage 2	VHI2	SAD0 SAD1		80%Vdd			
Low level input voltage 2	VIL2					20%Vdd	
Input current 1	IIN1	SCL SDA	Vin=VSS or Vid	-10		+10	µA
Input current 2	IIN2	SAD0 SAD1	Vin=VSS or Vdd	-10		+10	µA
Input current 3	IIN3	TST	Vin= VSS			+10	µA
Hysteresis input voltage (Note 2)	VHS	SCL SDA	Vid>2V	5%Vid			V
			Vid<2V	10%Vid			V
Low level output voltage 1 (Note 3)(Note 4)	VOL1	SDA	IOL≤3mA Vid ≥ 2V			0.4	V
			IOL≤3mA Vid <2V			20%Vid	V
Current consumption (Note 5)	IDD1	VDD VID	Power-down mode Vdd=Vid=3.0V		0.1	1	µA
	IDD2		Normal operating (Note 6)		18	30	µA

(Note 2) Schmitt trigger input (reference value for design)
(Note 3) Maximum load capacitance: 400pF (capacitive load of each bus line applied to the I2C bus interface)
(Note 4) Output is open-drain. Connect a pull-up resistor externally.
(Note 5) Without any resistance load
(Note 6) OPF[2:0] = “001” condition (operating frequency 10Hz)

4.3.2. AC Characteristics

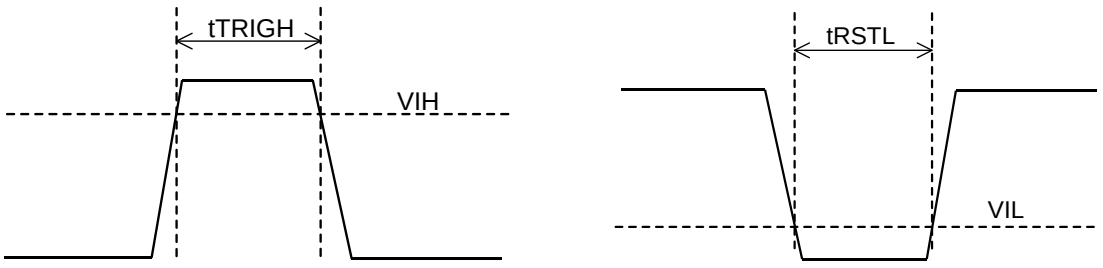
Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Power supply rise time (Note 7)	PSUP	VDD VID	Period of time that VDD (VID) changes from 0.2V to Vdd (Vid). (Note 8)			50	ms
POR completion time (Note 7)	PORT		Period of time after PSUP to Power-down mode (Note 8)			100	µs
Power supply turn off voltage	SDV	VDD VID	Turn off voltage to enable POR to restart (Note 8)			0.2	V
Power supply turn on interval (Note 7)	PSINT	VDD VID	Period of time that voltage lower than SDV needed to be kept to enable POR to restart (Note 8)	100			µs
Wait time before mode setting	Twat			100			µs

(Note 7) Reference value for design
(Note 8) When POR circuit detects the rise of VDD voltage, it resets internal circuits and initializes the registers. After reset, MXM1120 transits to power-down mode



Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Effective pulse width of trigger input	tTRIGH	TRG		200			ns
Effective frequency of trigger input (Note 9)	tTRIGf	TRG				100	Hz
Effective pulse width of trigger input (“L”)	tRSTL	RSTN		200			ns

(Note 9) The time from the end of the measurement to the next trigger input is 1.3ms.



4.3.3. IC Output Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Measurement data output bit	DBIT	BIT = “0”	-	10	-	bit
		BIT = “1”	-	8	-	
Time for measurement	TSM	Single measurement mode		420	500	usec
Magnetic sensor sensitivity (Note 11)	BSE	Tc=25℃, VDD = 3.0V, BIT= “0”,	-7%	(Note 10)	+7%	(Note 10)

(Note 10) Refer to chapter 7.2.2. INTSRS.
(Note 11) Magnetic sensitivity range and resolution are just reference values for design because they depend on the measurement environment.
This min/max range includes process variation and IC output fluctuation due to operating noise.

4.3.4. I²C Bus Interface

I2C bus interface is compliant with standard mode and fast mode. Standard/fast mode is selected automatically by fSCL.

(1) Standard mode

fSCL≤100kHz

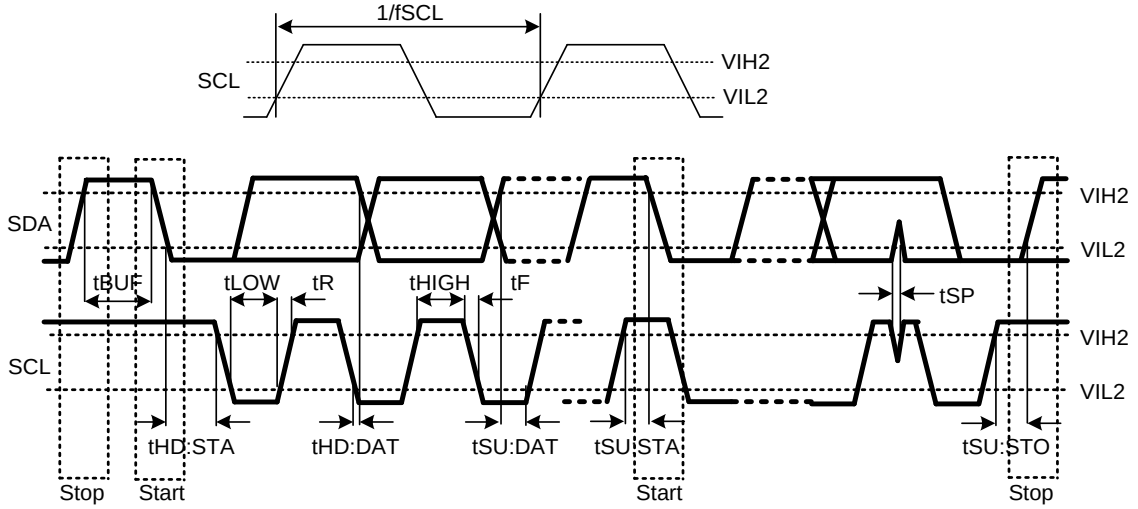
Symbol	Parameter	Min.	Typ.	Max.	Unit
fSCL	SCL clock frequency			100	kHz
tHIGH	SCL clock "High" time	4.0			μs
tLOW	SCL clock "Low" time	4.7			μs
tR	SDA and SCL rise time			1.0	μs
tF	SDA and SCL fall time			0.3	μs
tHD:STA	Start Condition hold time	4.0			μs
tSU:STA	Start Condition setup time	4.7			μs
tHD:DAT	SDA hold time (vs. SCL falling edge)	0			μs
tSU:DAT	SDA setup time (vs. SCL rising edge)	250			ns
tSU:STO	Stop Condition setup time	4.0			μs
tBUF	Bus free time	4.7			μs

(2) Fast mode

100kHz<fSCL≤400kHz

Symbol	Parameter	Min.	Typ.	Max.	Unit
fSCL	SCL clock frequency			400	kHz
tHIGH	SCL clock "High" time	0.6			μs
tLOW	SCL clock "Low" time	1.3			μs
tR	SDA and SCL rise time			0.3	μs
tF	SDA and SCL fall time			0.3	μs
tHD:STA	Start Condition hold time	0.6			μs
tSU:STA	Start Condition setup time	0.6			μs
tHD:DAT	SDA hold time (vs. SCL falling edge)	0			μs
tSU:DAT	SDA setup time (vs. SCL rising edge)	100			ns
tSU:STO	Stop Condition setup time	0.6			μs
tBUF	Bus free time	1.3			μs
tSP	Noise suppression pulse width			50	μs

[I²C bus interface timing]



5. Functional Explanation

5.1. Power States

When VDD and VID are turned on, all registers in MXM1120 are initialized by POR circuit and MXM1120 transits to power-down mode.

All the states in the table below can be set, although the transition from state 2 to state 3 and the transition from state 3 to state 2 are prohibited.

State	VDD	VID	Power state
1	OFF (0V)	OFF (0V)	OFF (0V). It doesn't affect external interface. Digital input pins except SCL and SDA pin should be fixed to "L" (0V).
2	OFF (0V)	1.65V to 3.6V	OFF (0V). It doesn't affect external interface.
3	2.7V to 3.6V	OFF (0V)	OFF (0V). It doesn't affect external interface. Digital input pins except SCL and SDA pin should be fixed to "L" (0V).
4	2.7V to 3.6V	1.65V to Vdd	ON

5.2. Reset Functions

When the power is on, it is always maintained at Vid≤Vdd.
Power-On Reset (POR) works until Vdd reaches the effective operation voltage (about 1.4V: reference value for design) on power-on sequence. After POR is deactivated, all registers are initialized and transits to power down mode.

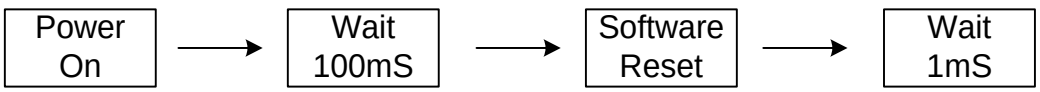
When Vdd=2.7 ~ 3.6V, POR circuit is active.

MXM1120 has two types of reset;

(1) Power on reset (POR):
When Vdd rise is detected, POR circuit operates, and MXM1120 is reset.
(2) Soft reset:
MXM1120 is reset by setting SRST bit. When SRST bit set to "1", fuse ROM value is automatically loaded..

When MXM1120 is reset, all registers are initialized and MXM1120 transits to power-down mode.

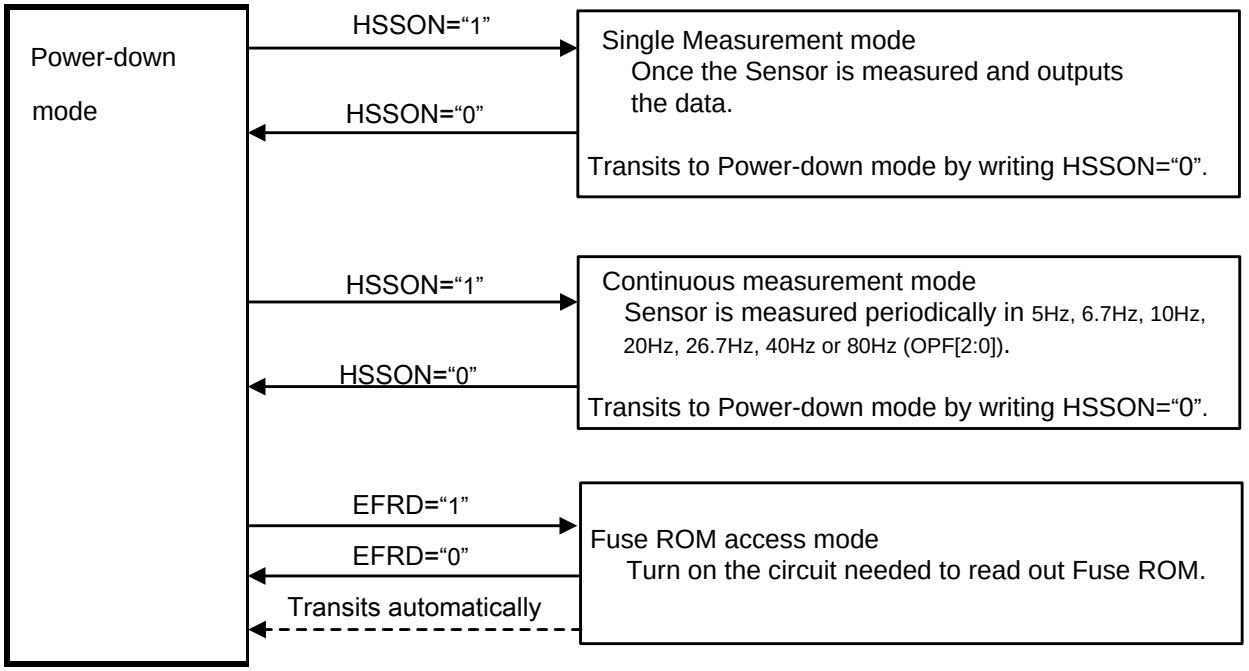
5.2.1. Power on Sequence



5.3. Operation Modes

MXM1120 has the following four operation modes:

(1) Power-down mode
(2) Single measurement mode
(3) Continuous measurement mode
(4) Fuse ROM access mode



When power is turned on, MXM1120 is in power-down mode. When a specified value is set to HSSON, MXM1120 transits to the specified mode and starts operation. When user wants to change operation mode, transit to power-down mode first and then transit to other modes. After power-down mode is set, at least 100us(Twat) is needed before setting another mode

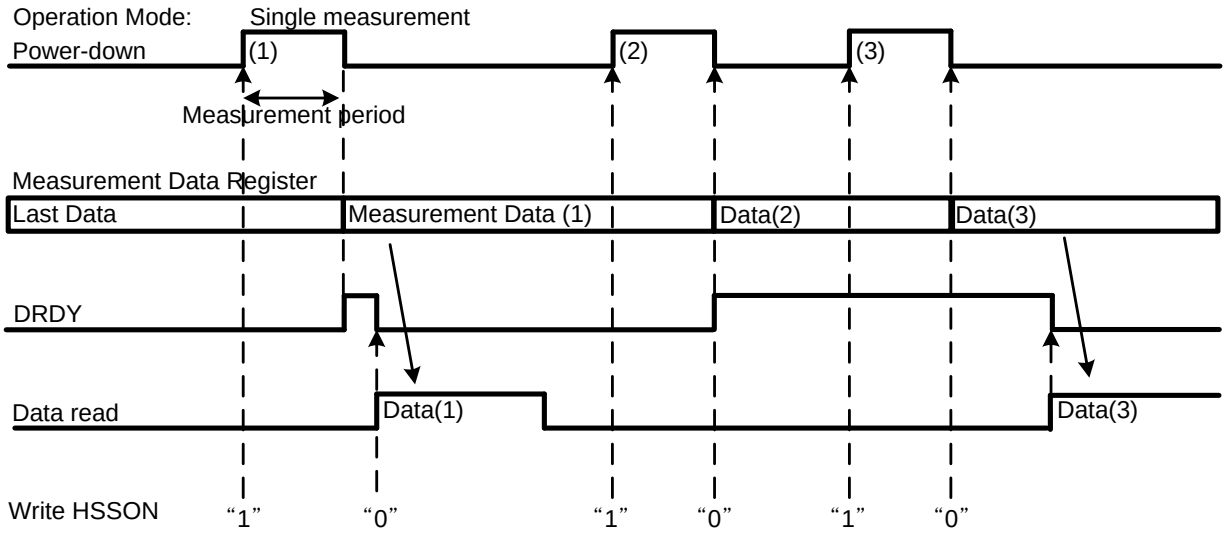
5.4. Description of Each Operation Mode

5.4.1. Power-down Mode

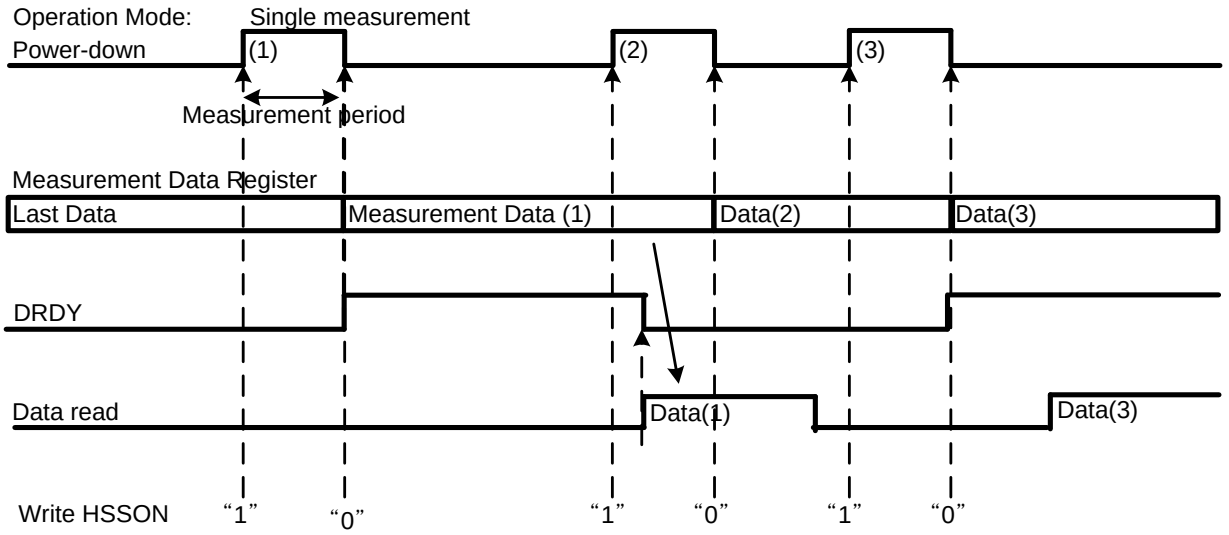
Almost power of all internal circuits is turned off. All registers are accessible in power-down mode.
However, embedded OTP data cannot be read correctly. Data stored in read/write registers remains. They can be reset by soft reset.

5.4.2. Single Measurement Mode

When single measurement mode (HSSON="1") is set, sensor is measured, and after sensor measurement and signal processing is finished, measurement data is stored to HS[9:0] data registers (HSL to HSH). DRDY bit in ST1 register turns to "1". This is called "Data Ready". When any of HS[9:0] data registers (HSL to HSH) is read, DRDY bit turns to "0". While sensor is being measured (in measurement period), measurement data registers (HSL ~ HSH) keep the previous data. Therefore, it is possible to read out data even during measurement. Data during measurement period are kept previous data. It must be set to power-down mode(HSSON="0"), after measurement data reading is finished.



Single measurement mode: when data is read out of measurement period

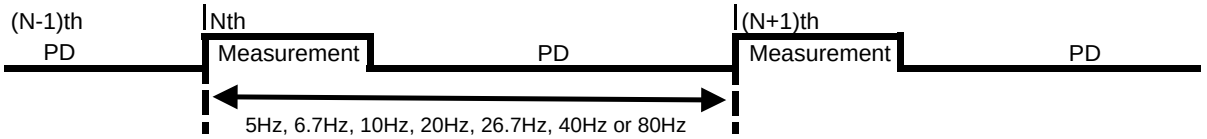


Single measurement mode: when data read started during measurement period

5.4.3. Continuous Measurement Mode

When continuous measurement mode (HSSON="1" and OPF[2:0]="XXX") is set, sensor is measured periodically at 5Hz, 6.7Hz, 10Hz, 20Hz, 26.7Hz, 40Hz and 80Hz respectively. When sensor measurement and signal processing is finished, measurement data is stored to measurement data registers (HSL ~ HSH) and all circuits except for the minimum circuit required for counting cycle length are turned off (PD). When the next measurement timing comes, MXM1120 wakes up automatically from PD and starts measurement again.
Continuous measurement mode ends when power-down mode (HSSON="0") is set. It repeats measurement until power-down mode is set.
When continuous measurement mode is set again while MXM1120 is already in continuous measurement mode, a new measurement starts.

OPF[2]	OPF[1]	OPF[0]	Frequence [Hz]
0	0	0	20.0
0	0	1	10.0
0	1	0	6.7
0	1	1	5.0
1	0	0	80.0
1	0	1	40.0
1	1	0	26.7
1	1	1	20.0



5.4.3.1. Data Ready

When measurement data is stored and ready to be read, DRDY bit in ST1 register turns to "1". This is called "Data Ready". DRDY pin is in the same state as DRDY bit. When measurement is performed correctly, MXM1120 becomes Data Ready on transition to PD after measurement.

5.4.4. Normal Read Sequence

(1) Check whether it is Data Ready or not, by any of the following method.
- Polling DRDY bit of ST1 register

When Data Ready, proceed to the next step.

(2) Read ST1 register
DRDY: Shows Data Ready or not. "0" indicates Data not Ready, and "1" means Data Ready.

(3) Read measurement data
Must read the ST1, HSL and HSH register with multiple byte read mode. If reading the ST1, HSL and HSH register with one-byte read mode, measurement data is not protected.

5.4.5. Embedded OTP Access Mode

OTP access mode is used to read embedded OTP data.
Sensitivity adjustment data are stored in embedded OTP.
Set OTP access mode (EFRD="1") before reading OTP data.
When OTP access mode is set, circuits required for reading fuse ROM are turned on.
After reading fuse ROM data, set power-down mode (EFRD="0") before transition to another mode.

6. Serial Interface

6.1. I²C Bus Interface

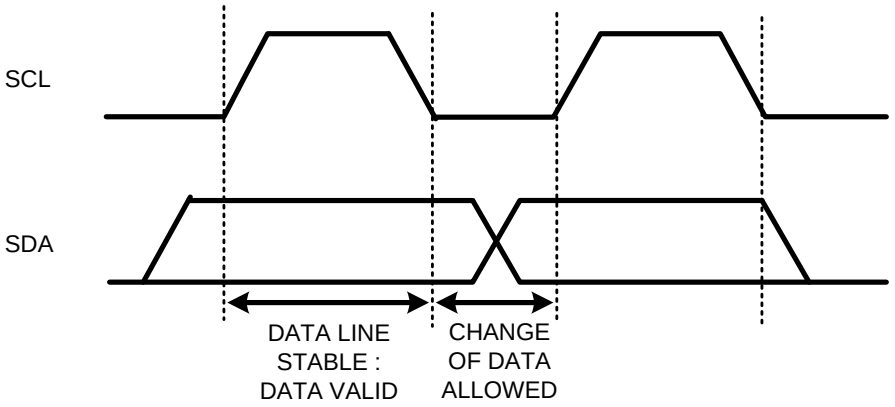
The I²C bus interface of MXM1120 supports standard mode (100 kHz max.) and fast mode (400 kHz max.).

6.1.1. Data Transfer

To access MXM1120 on the bus, generate a start condition first.
Next, transmit a one-byte slave address including a device address. At this time, MXM1120 compares the slave address with its own address. If these addresses match, MXM1120 generates an acknowledgement, and then executes READ or WRITE instruction. At the end of instruction execution, generate a stop condition.

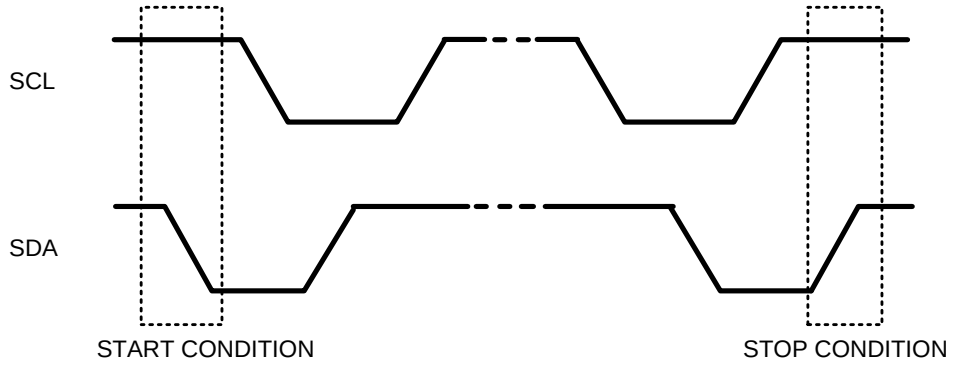
6.1.1.1. Change of Data

Data change on the SDA line must be made during "Low" period of the clock on the SCL line. When the clock signal on the SCL line is "High", the state of the SDA line must be stable. (Data on the SDA line can be changed only when the clock signal on the SCL line is "Low".)
During the SCL line is "High", the state of data on the SDA line is changed only when a start condition or a stop condition is generated.



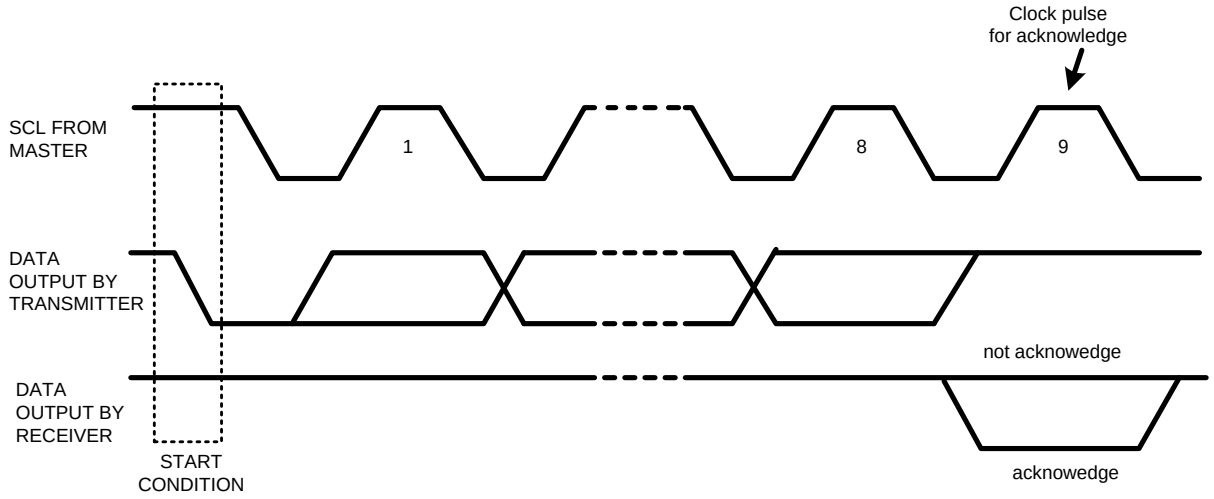
6.1.1.2. Start/Stop Condition

If the SDA line is driven to "Low" from "High" when the SCL line is "High", a start condition is generated.
Every instruction starts with a start condition.
If the SDA line is driven to "High" from "Low" when the SCL line is "High", a stop condition is generated.
Every instruction stops with a stop condition.



6.1.1.3. Acknowledge

The IC that is transmitting data releases the SDA line (in the "High" state) after sending 1-byte data.
The IC that receives the data drives the SDA line to "Low" on the next clock pulse. This operation is referred as acknowledge. With this operation, whether data has been transferred successfully can be checked.
MXM1120 generates an acknowledge after reception of a start condition and slave address.
When a WRITE instruction is executed, MXM1120 generates an acknowledge after all bytes are received.
When a READ instruction is executed, MXM1120 generates an acknowledge then transfers the data stored at the specified address. Next, MXM1120 releases the SDA line then monitors the SDA line. If a master IC generates an acknowledge instead of a stop condition, MXM1120 transmits the 8bit data stored at the next address. If no acknowledge is generated, MXM1120 stops data transmission.



6.1.1.4. Slave Address

The slave address of MXM1120 can be selected from the following list by setting SAD0/1 pin. When SAD pin is fixed to VSS, the corresponding slave address bit is “0”. When SAD pin is fixed to VDD, the corresponding slave address bit is “1”..

SAD1	SAD0	Slave Address	MXM1120
0	0	0CH	O
0	1	0DH	O
1	0	0EH	O
1	1	0FH	O

MSB LSB

0	0	0	1	1	SAD1	SAD0	R/W

The first byte including a slave address is transmitted after a start condition, and an IC to be accessed is selected from the ICs on the bus according to the slave address.
When a slave address is transferred, the IC whose device address matches the transferred slave address generates an acknowledge, and then executes an instruction. The 8th bit (least significant bit) of the first byte is a R/W bit.
When the R/W bit is set to "1", READ instruction is executed. When the R/W bit is set to "0", WRITE instruction is executed.

6.1.2. WRITE Instruction

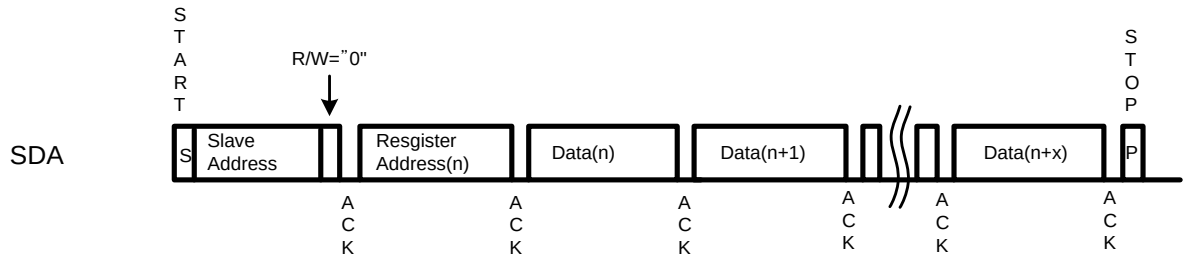
When the R/W bit is set to "0", MXM1120 performs write operation.
In write operation, MXM1120 generates an acknowledge after receiving a start condition and the first byte (slave address) then receives the second byte. The second byte is used to specify the address of an internal control register and is based on the MSB-first configuration.

MSB							LSB
A7	A6	A5	A4	A3	A2	A1	A0

After receiving the second byte (register address), MXM1120 generates an acknowledge then receives the third byte. The third and the following bytes represent control data. Control data consists of 8 bits and is based on the MSB-first configuration. MXM1120 generates an acknowledge after all bytes are received. Data transfer always stops with a stop condition generated by the master.

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

MXM1120 can write multiple bytes of data at a time.
After reception of the third byte (control data), MXM1120 generates an acknowledge then receives the next data.
If additional data is received instead of a stop condition after receiving one byte of data, the address counter inside the LSI chip is automatically incremented and the data is written at the next address.
The address is incremented from 10H to 1CH or from 20H to22H. When the address is in 10H~1CH, the address goes back to 10H after 10CH. When the address is in 20H~22H, the address goes back to 20H after 22H.
Actual data is written only to Read/Write registers.

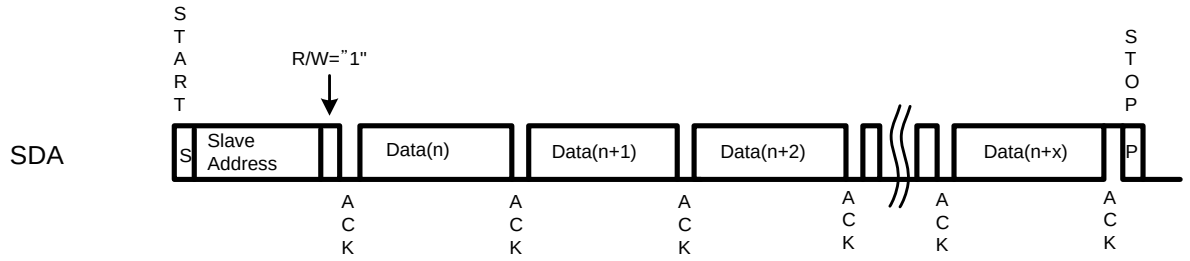


6.1.3. READ Instruction

When the R/W bit is set to "1", MXM1120 performs read operation.
If a master IC generates an acknowledge instead of a stop condition after MXM1120 transfers the data at a specified address, the data at the next address can be read.
Address can be 10H~1CH and/or 20H~22H.When address is counted up to 1CH in 10H~1CH, the next address returns to 10H. When address is counted up to 22H in 20H~22H, the next address returns to 20H.
MXM1120 supports one byte read and multiple bytes read.

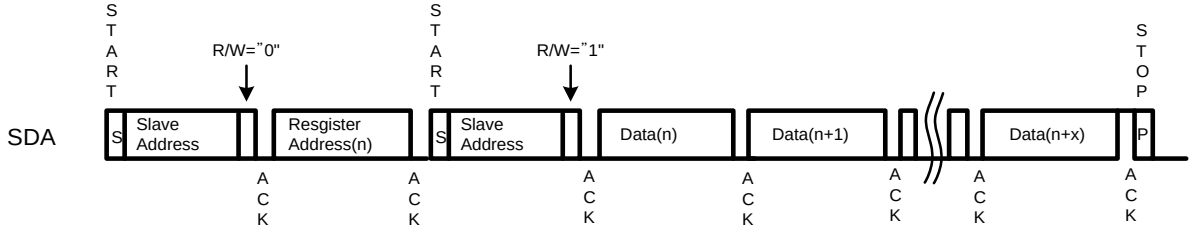
6.1.3.1. One Byte READ

MXM1120 has an address counter inside the LSI chip. In the current address read operation, the data at an address specified by this counter is read.
The internal address counter holds the next address of the most recently accessed address.
For example, if the most recently accessed (for READ instruction) address is "n", and the current address read operation is attempted, the data at address "n+1" is read.
In one byte read operation, MXM1120 generates an acknowledge after receiving a slave address for READ instruction (R/W bit="1"). Next, MXM1120 transfers the data specified by the internal address counter starting with the next clock pulse, and then increments the internal counter by one. If the master IC generates a stop condition instead of an acknowledge after MXM1120 transmits one byte of data, the read operation stops.



6.1.3.2. Multiple Byte READ

By multiple byte read operation, data at an arbitrary address can be read.
The multiple byte read operation requires executing WRITE instruction as dummy before a slave address for the READ instruction (R/W bit="1") is transmitted. In random read operation, a start condition is first generated, then a slave address for the WRITE instruction (R/W bit="0") and a read address are transmitted sequentially.
After MXM1120 generates an acknowledge in response to this address transmission, a start condition and a slave address for the READ instruction (R/W bit="1") are generated again. MXM1120 generates an acknowledge in response to this slave address transmission. Next, MXM1120 transfers the data at a specified address, and then increments the internal address counter by one. If the master IC generates a stop condition instead of an acknowledge after data is transferred, the read operation stops.



7. Registers

7.1. Register Map

Address	Name	Mode	D7	D6	D5	D4	D3	D2	D1	D0	Default
00H	PERSINT	Write / Read	PERS[3:0]				0	0	0	INTCLR	41H
01H	INTSRS	Write / Read	INTON	0	0	INT_TYP	0	SRS[2:0]			82H
02H	LTHL	Write / Read	LTH7	LTH6	LTH5	LTH4	LTH3	LTH2	LTH1	LTH0	00H
03H	LTHH	Write / Read	LTH9	LTH8	0	0	0	0	0	0	00H
04H	HTHL	Write / Read	HTH7	HTH6	HTH5	HTH4	HTH3	HTH2	HTH1	HTH0	40H
05H	HTHH	Write / Read	HTH9	HTH8	0	0	0	0	0	0	00H
06H	I2CDIS	Write / Read	I2CDIS[7:0]								00H
07H	SRST	Write / Read	0	0	0	0	0	0	0	SRST	00H
08H	OPMODE	Write / Read	0	OPF[2:0]			EFRD	0	BIT	HSSON	00H
09H	DID	Read	1	0	0	1	1	1	0	0	9CH
0AH	INFO	Read	INFO7	INFO6	INFO5	INFO4	INFO3	INFO2	INFO1	INFO0	XXH
10H	ST1	Read	0	0	0	INTM	0	0	BITM	DRDY	00H
11H	HSL	Read	HS7	HS6	HS5	HS4	HS3	HS2	HS1	HS0	00H
12H	HSH	Read	HS9	HS8	0	0	0	0	0	0	00H

When VDD is turned on, POR function works and all registers of MXM1120 are initialized regardless of VID status. To write data to, or read data from, register, VID must be on.

7.2. Detailed Description of Registers

7.2.1. PERSINT: Interrupt time

Address	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	PERSINT	PERS[3:0]							INTCLR

PERS[3:0]:

Interrupt PAD (INTB) transits from low to high level after consecutive interrupt events occur more than PERS[3:0] times. This function is to reject abnormal interrupt events (noise).
For example, if PERS[3:0] = “0100”, then four consecutive events must be detected during four consecutive measurement cycles. Similarly if PERS[3:0] = “1000”, then 8 consecutive interrupt events must be detected.
If no interrupt event is detected for intervening measurement time, then the count is reset to zero.

PERS[3]	PERS[2]	PERS[1]	PERS[0]	Interrupt count
0	0	0	0	not use
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

INTCLR:

"0": Interrupt events counting is enabled.
"1": Interrupt count is cleared.

7.2.2. INTSRS: Sensitivity (gain control)

Address	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	INTSRS	INTON	0	0	INT_TYP	0	SRS[2:0]		

INTON: Interrupt mode on/off selection

"0" : interrupt mode off

"1" : interrupt mode on

INT_TYP: Interrupt type selection

"0" : (LTH[9:0] > HS[9:0]) or (HTH[9:0] < HS[9:0])

"1" : (LTH[9:0] < HS[9:0]) and (HTH[9:0] > HS[9:0])

SRS[2:0]:

Sensitivity range and resolution is adjusted with SRS[2:0].

BIT = 0 : 10bit

SRS[2]	SRS[1]	SRS[0]	Measuring range (±mT)	Resolution (mT/LSB)
0	0	0	40.8	0.08
0	0	1	20.4	0.04
0	1	0	10.2	0.02
0	1	1	5.1	0.01
1	0	0	2.55	0.005
1	0	1	10.2	0.02
1	1	0	10.2	0.02
1	1	1	10.2	0.02

BIT = 1 : 8bit

SRS[2]	SRS[1]	SRS[0]	Measuring range (±mT)	Resolution (mT/LSB)
0	0	0	40.8	0.32
0	0	1	20.4	0.16
0	1	0	10.2	0.08
0	1	1	5.1	0.04
1	0	0	2.55	0.02
1	0	1	10.2	0.08
1	1	0	10.2	0.08
1	1	1	10.2	0.08

7.2.3. LTH / HTH : Lower and upper threshold level

Address	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	LTHL	LTH7	LTH6	LTH5	LTH4	LTH3	LTH2	LTH1	LTH0
03H	LTHH	LTH9	LTH8	0	0	0	0	0	0
04H	HTHL	HTH7	HTH6	HTH5	HTH4	HTH3	HTH2	HTH1	HTH0
05H	HTHH	HTH9	HTH8	0	0	0	0	0	0

LTH[9:0] / HTH[9:0]:

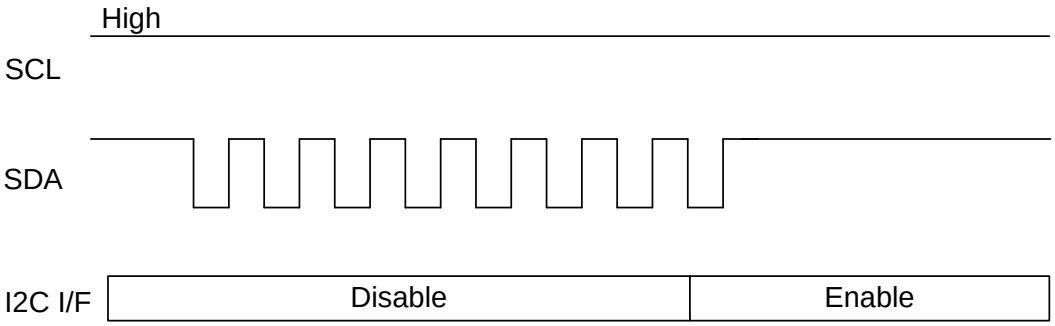
Lower and upper threshold levels for interrupt function are defined with LTH[9:0] and HTH[9:0] respectively.
The interrupt upper and lower threshold levels set the window limits that are used to trigger an interrupt.
The values are in signed digit format and negative threshold setting is available.

7.2.4. I2CDIS : I2C interface disable

Address	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	I2CDIS	I2CDIS[7:0]							

I2CDIS[7:0]:

This register disables I2C bus interface. I2C bus interface is enabled as default. To disable I2C bus interface, write "00110111" to I2CDIS register, then I2C bus interface is disabled. Once I2C bus interface is disabled, it is impossible to write other value to I2CDIS register. To enable I2C bus interface, reset MXM1120 or SDA pin toggle 8 times in a row as below.



7.2.5. SRST : Software reset

Address	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	SRST	0	0	0	0	0	0	0	SRST

SRST:

If you want to reset the IC, set SRST = "1".
When SRST = "1", all registers are initialized. After reset, SRST bit turns to "0" automatically

7.2.6. OPMODE : Operation mode selection

Address	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	OPMODE	0	OPF[2:0]			EFRD	0	BIT	HSSON

OPF[2:0]:

Operating frequency mode is set by OPF[2:0].

Power consumption increases proportional to operating frequency.

OPF[2]	OPF[1]	OPF[0]	Period (msec)	Frequency (Hz)
0	0	0	50	20
0	0	1	100	10
0	1	0	150	6.7
0	1	1	200	5
1	0	0	12.5	80
1	0	1	25	40
1	1	0	37.5	26.7
1	1	1	50	20

EFRD:

Embedded OTP access mode

"0": Previous OTP data is kept

"1": New OTP data is read automatically

BIT:

ADC output data width selection

"0": 10bits

"1": 8bits

HSSON:

Device power down mode

"0": Power down mode

"1": Normal operation

7.2.7. DID : Device ID

Address	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	DID	1	0	0	1	1	1	0	0

DID[7:0]:

Device ID of MXM1120. It is described in one byte and fixed value; 9CH.

7.2.8. INFO : Device information

Address	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	INFO	INFO7	INFO6	INFO5	INFO4	INFO3	INFO2	INFO1	INFO0

INFO[7:0]:
Device information is described in one byte and fixed value.

7.2.9. ST1 : Status data

Address	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
10H	ST1	0	0	0	INTM	0	0	BITM	DRDY

INTM:
Status for interrupt (mirroring for INTB)

BITM:
Status for ADC output data width (mirroring for BIT)

DRDY:
Status for data ready. DRDY bit turns to “1” when measured data is ready to output.

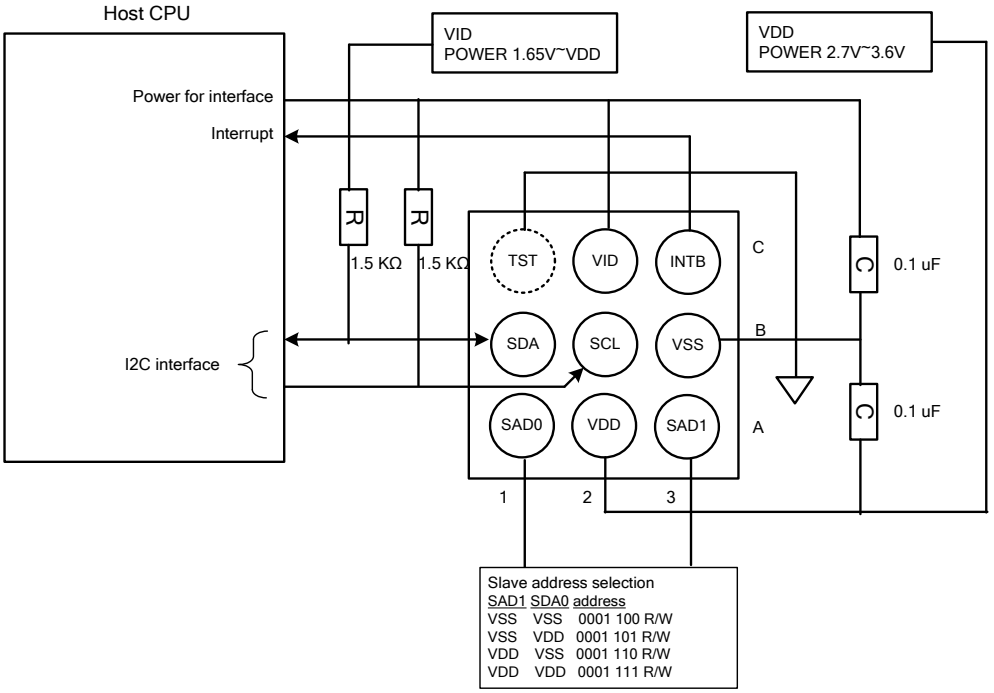
7.2.10. HS : Measured data output

Address	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
11H	HSL	HS7	HS6	HS5	HS4	HS3	HS2	HS1	HS0
12H	HSH	HS9	HS8	0	0	0	0	0	0

HS[9:0]:
The measured data of the magnetic sensor. The data is stored in two's complement and Little Endian format.
Measurement range of sensor is -512 ~ +511 in decimal in 10-bit output, and -128 ~ +127 in 8-bit output.

Measurement data (HS[9:0])		
Two's complement	Hex	Decimal
8-bit output		
00 0111 1111	07F	127
|	|	|
00 0000 0001	001	1
00 0000 0000	000	0
11 1111 1111	3FF	-1
|	|	|
11 1000 0000	380	-128
10-bit output		
01 1111 1111	1FF	511
|	|	|
00 0000 0001	001	1
00 0000 0000	000	0
11 1111 1111	3FF	-1
|	|	|
10 0000 0000	200	-512

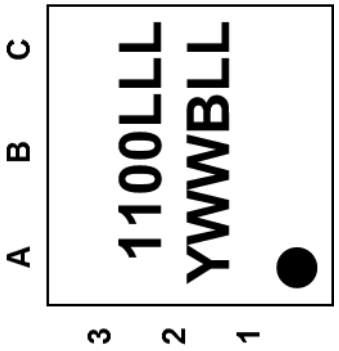
8. Application Note



9. Package

9.1. Marking

- Product name : 1100
- LLLLL : Lot traceability code (5digits)
- Y : Year code (1 digit)
- WW : Work week code (2 digits)
- B : Revision code (1 digit)
- Pin 1 mark : Left bottom alignment



< Top view>

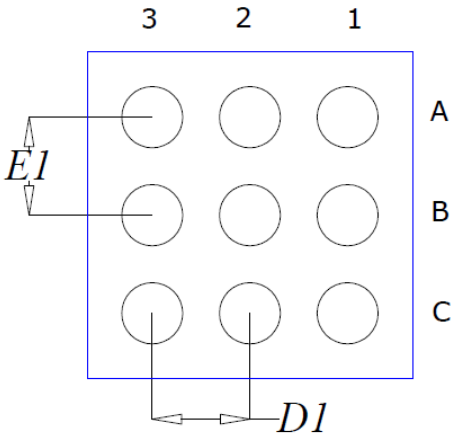
9.2. Pin Assignment

Pin number	3	2	1
C	INTB	VID	TST
B	VSS	SCL	SDA
A	SAD1	VDD	SAD0

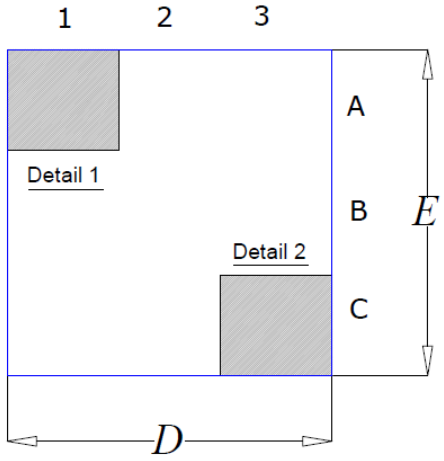
< Top View>

9.3. Outline Dimensions

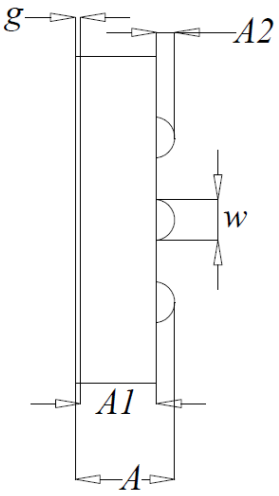
Bottom view (Bump side up)



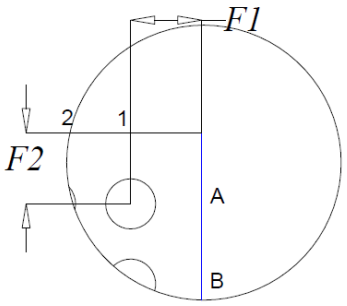
Top view (Bump side down)



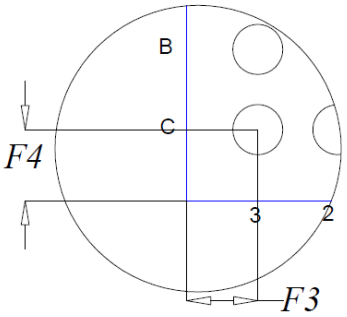
Side view



Detail 1



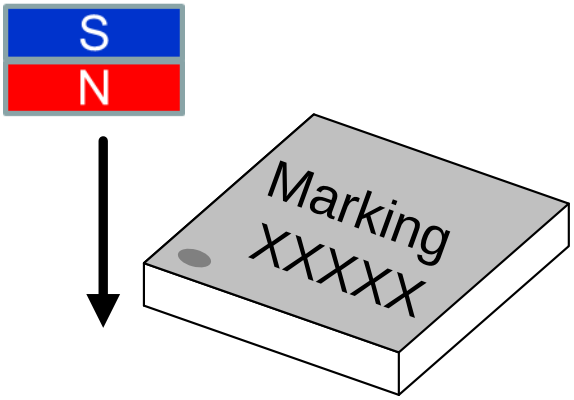
Detail 2



Symbol	Dimension [mm]				Symbol	Dimension [mm]			
	Min	Nom.	Max	Note		Min	Nom.	Max	Note
A	0.491	0.530	0.569	±0.039	F1	0.265			Ball center to die edge
A1	0.375	0.395	0.415	±0.020	F2	0.265			Ball center to die edge
A2	0.094	0.110	0.126	±0.016	F3	0.265			Ball center to die edge
D	1.290	1.330	1.370	±0.040	F4	0.265			Ball center to die edge
E	1.290	1.330	1.370	±0.040	g	0.022	0.025	0.028	±0.003
D1	0.400			-	w	0.235	0.240	0.245	±0.005
E1	0.400			-					

10. Relationship between the Magnetic Field and Output Code

The measurement data increases as the magnetic flux density increases in the arrow directions.



Z (HS[9:0])

11. Revision History

0.00	2013-07-24	- First edition
1.00	2013-10-01	- Correction: 4.2 Recommended operationg condition change. - Correction: 8. Application note. Pull up resister 2.2KΩ → 1.5KΩ
1.01	2013-11-18	- Correction: 3.1 Block Diagram. (DRDY→TST)
1.10	2013-12-04	- Addition: 9.1 Marking
2.00	2014-02-13	- Modification: 7.2.2 SRS register setting (3bit → 2bit) - Modification: 7.2.3 LTH/HTH format (unsigned → signed) - Modification: 7.2.6 OPF register setting (2bit → 3bit) - Addition: 7.2.2 INT_TYP selection bit - Addition: 5.3 Operation mode - Addition: 5.4 Description of Each Operation Mode
2.1	2014-03-07	- Modification: 3.2 Pin function (TST power VID → VDD) - Addition: 4.1 Absolute maximum ratings (Input current max 10mA) - Addition: 4.3 Electrical characteristics (Dynamic current VDD max) - Addition: 4.3.3 IC output characteristics (sensitivity min - max) - Modification: 7.2.4 I2CDIS methods
2.2	2014-04-11	- Modification : 5.2.1 Power on sequence (wait 10ms → wait 100ms)
2.3	2015-01-16	- Modification : 1. Overview - Modification : 4.3.3. IC output characteristics. Sensitivity min, max changed - Remove : 7.1 Register map ASA register (10H) - Modification : 7.2.2 INTSRS. SRS[2:0] table update - Remove : 7.2.9 ASA register
2.4	2015-01-29	- Modification : 9.1 Marking : rotate drawing to 90 degree left. - Modification : 9.3 Outline Dimensions

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