



# SLP18N50C / SLF18N50C

## 500V N-Channel MOSFET

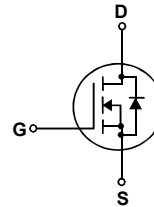
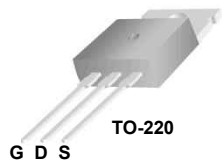
SLP18N50C / SLF18N50C

### General Description

This Power MOSFET is produced using Maple semi's advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

### Features

- 18A, 500V,  $R_{DS(on)typ.} = 236m\Omega @ V_{GS} = 10V$
- Low gate charge ( typical 69nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



### Absolute Maximum Ratings

$T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	SLP18N50C	SLF18N50C	Units
$V_{DSS}$	Drain-Source Voltage	500		V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	18.0	18.0 *	A
		10.8	10.8 *	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	64	64 *	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$		V
EAS	Single Pulsed Avalanche Energy (Note 2)	371		mJ
$I_{AR}$	Avalanche Current (Note 1)	18		A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	22.93		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5		V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	229	41	W
		1.83	0.33	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		$^\circ\text{C}$

\* Drain current limited by maximum junction temperature.

### Thermal Characteristics

Symbol	Parameter	SLP18N50C	SLF18N50C	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.54	3.04	$^\circ\text{C}/\text{W}$
$R_{\theta JS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	--	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	$^\circ\text{C}/\text{W}$

**Electrical Characteristics**T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	500	--	--	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	--	0.5	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V	--	--	1	μA
		V <sub>DS</sub> = 400 V, T <sub>C</sub> = 125°C	--	--	10	μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V	--	--	-100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	3.0	--	5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 9 A	--	236	283	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 9 A (Note 4)	--	12	--	S
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	--	3053	--	pF
C <sub>oss</sub>	Output Capacitance		--	335	--	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	21	--	pF
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 250 V, I <sub>D</sub> = 18 A, R <sub>G</sub> = 25 Ω (Note 4, 5)	--	48.5	--	ns
t <sub>r</sub>	Turn-On Rise Time		--	43.5	--	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	261	--	ns
t <sub>f</sub>	Turn-Off Fall Time		--	70.5	--	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 400 V, I <sub>D</sub> = 18 A, V <sub>GS</sub> = 10 V (Note 4, 5)	--	69	--	nC
Q <sub>gs</sub>	Gate-Source Charge		--	16.5	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	31.2	--	nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	18	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	72	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 18 A	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 18 A,	--	452	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge	di <sub>F</sub> / dt = 100 A/μs (Note 4)	--	6.2	--	μC

**Notes:**

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 2.0mH, I<sub>AS</sub> = 18A, V<sub>DD</sub> = 50V, R<sub>G</sub> = 25Ω, Starting T<sub>J</sub> = 25°C
3. I<sub>SD</sub> ≤ 18A, di/dt ≤ 100A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, Starting T<sub>J</sub> = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

### Typical Characteristics

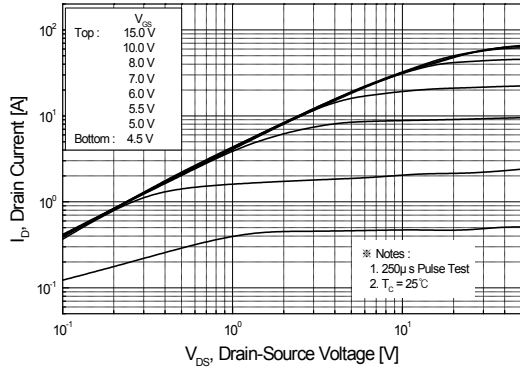


Figure 1. On-Region Characteristics

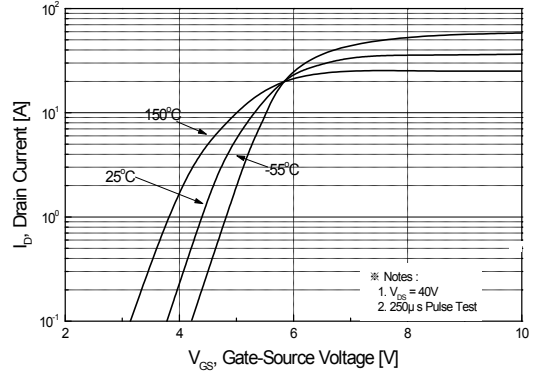


Figure 2. Transfer Characteristics

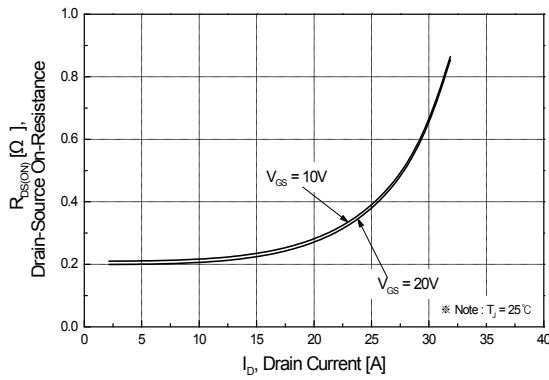


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

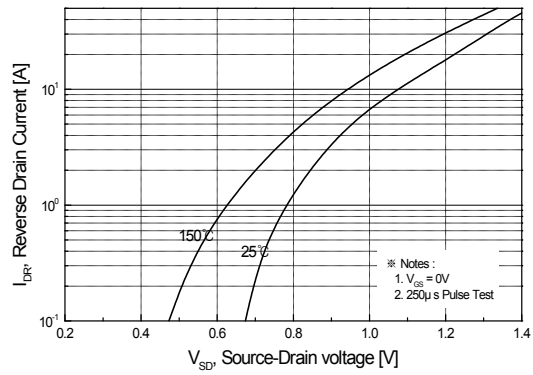


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

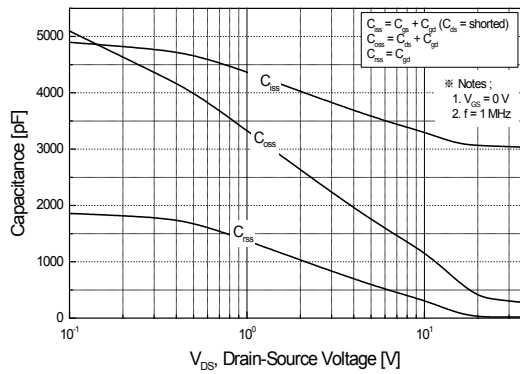


Figure 5. Capacitance Characteristics

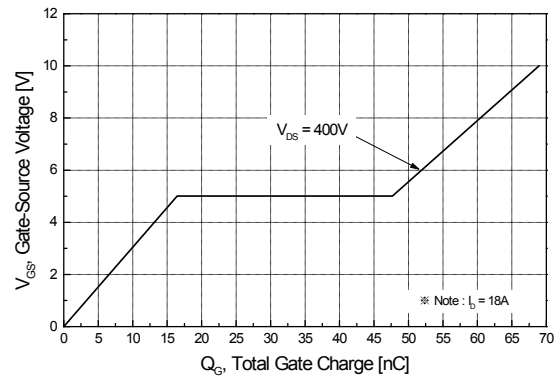


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

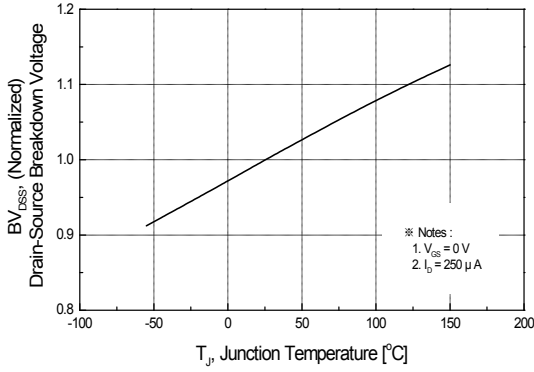


Figure 7. Breakdown Voltage Variation vs Temperature

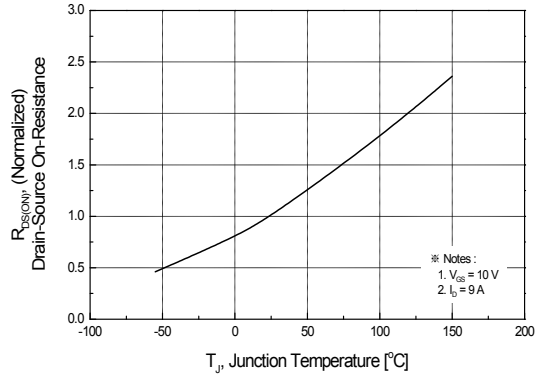


Figure 8. On-Resistance Variation vs Temperature

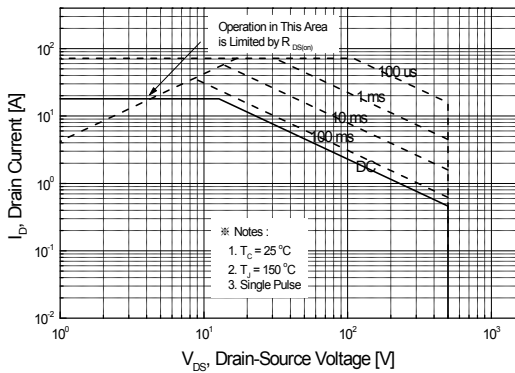


Figure 9-1. Maximum Safe Operating Area for SLP18N50C

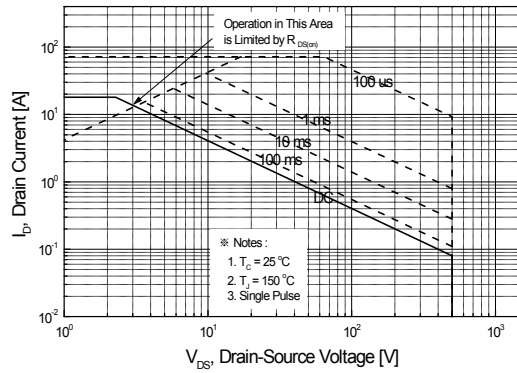


Figure 9-2. Maximum Safe Operating Area for SLF18N50C

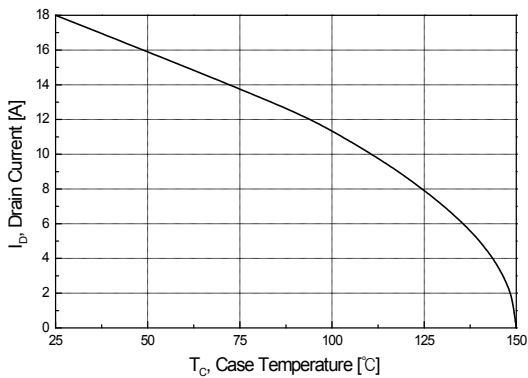


Figure 10. Maximum Drain Current vs Case Temperature

Typical Characteristics (Continued)

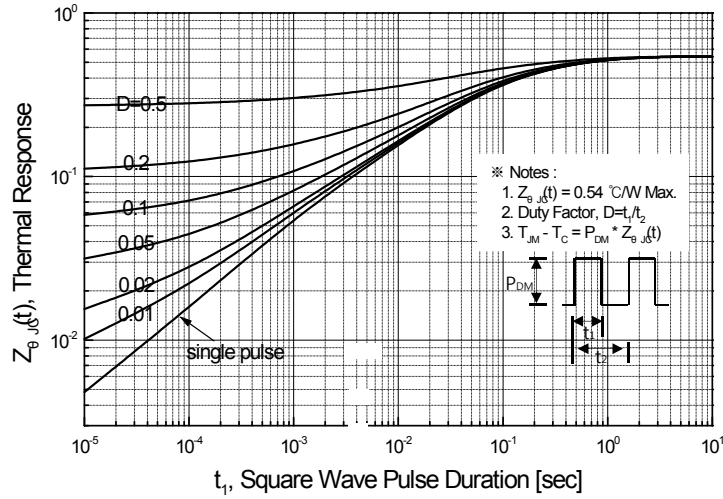


Figure 11-1. Transient Thermal Response Curve for SLP18N50C

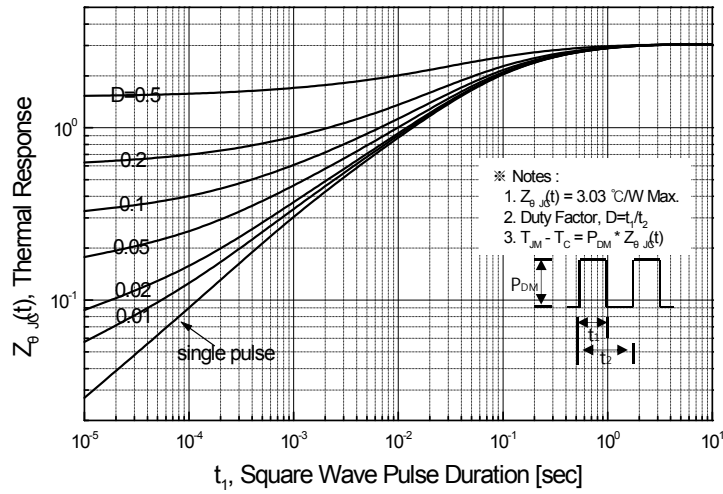
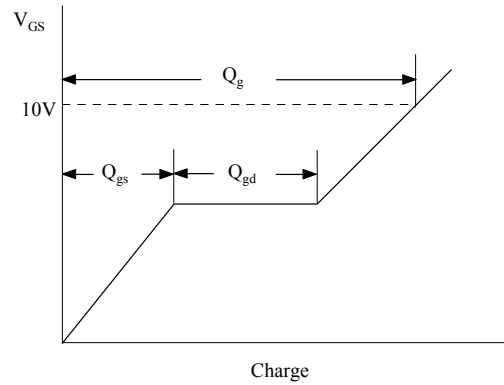
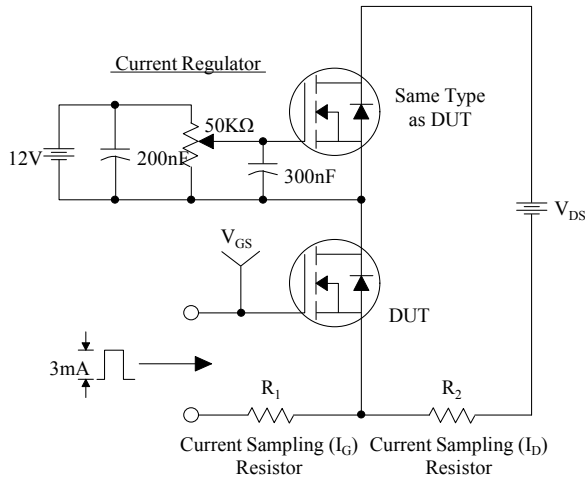
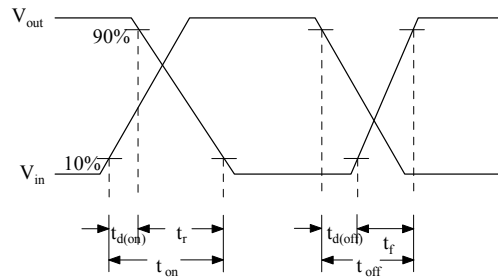
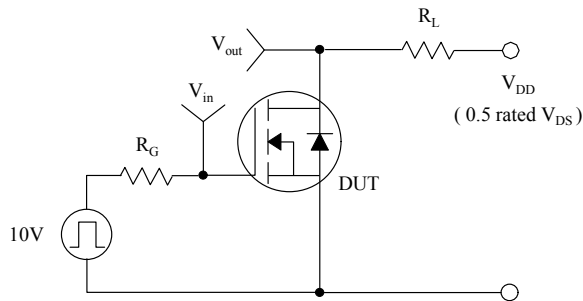


Figure 11-2. Transient Thermal Response Curve for SLF18N50C

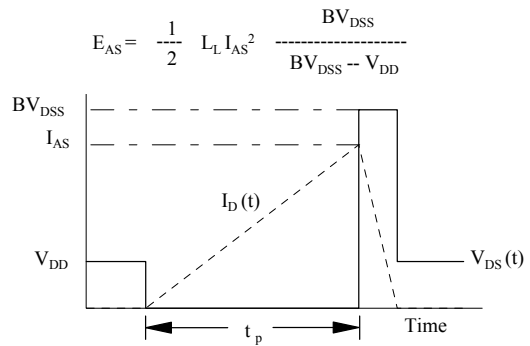
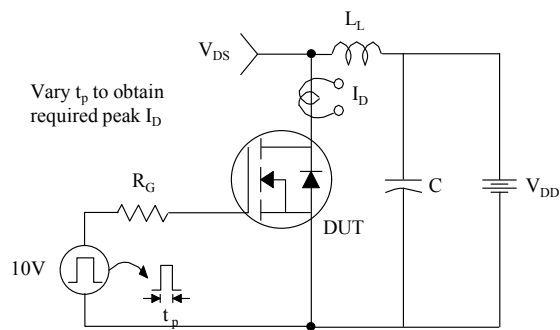
### Gate Charge Test Circuit & Waveform



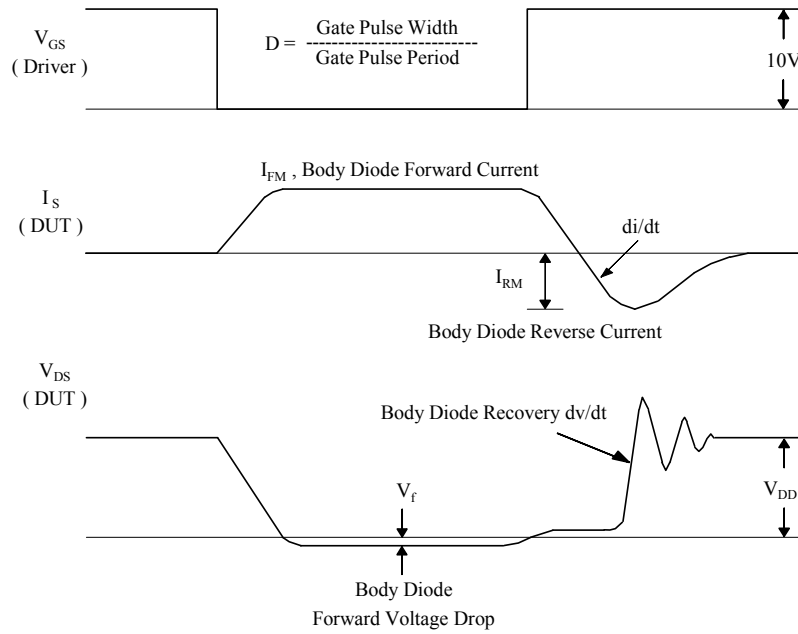
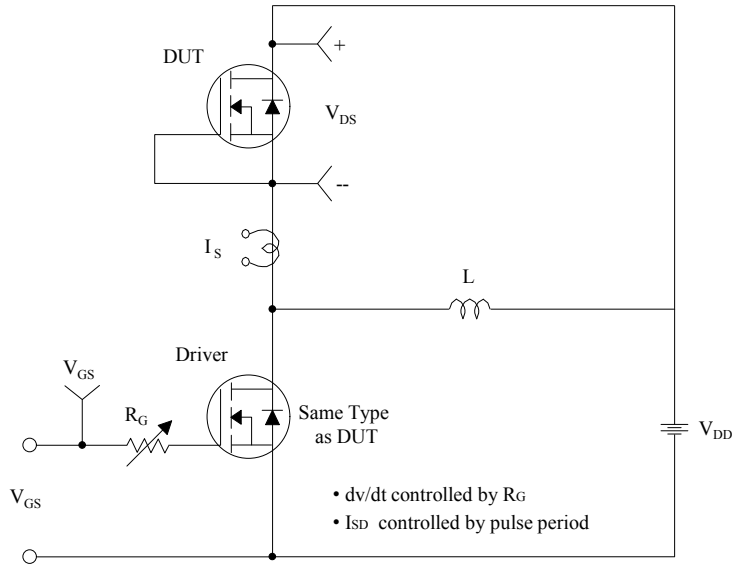
### Resistive Switching Test Circuit & Waveforms



### Unclamped Inductive Switching Test Circuit & Waveforms



### Peak Diode Recovery dv/dt Test Circuit & Waveforms



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