

# SLP5N65S/SLF5N65S

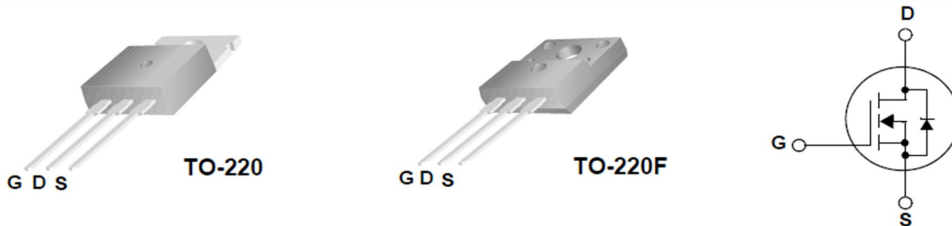
## 650V N-Channel MOSFET

### General Description

This Power MOSFET is produced using Maple semi's advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

### Features

- 4.5A, 650V,  $R_{DS(on)Max} = 2.5\Omega @ V_{GS} = 10V$
- Low gate charge ( typical 13nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



### Absolute Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	SLP5N65S	SLF5N65S	Units
$V_{DSS}$	Drain-Source Voltage	650		V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ C$ )	4.5		A
	- Continuous ( $T_C = 100^\circ C$ )	2.4		A
$I_{DM}$	Drain Current - Pulsed (Note 1)	16		A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$		V
EAS	Single Pulsed Avalanche Energy (Note 2)	113		mJ
$I_{AR}$	Avalanche Current (Note 1)	4.5		A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	3.5		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5.5		V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ C$ )	106	36	W
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150		$^\circ C$
$T_L$	Maximum lead temperature for soldering purposes,	300		$^\circ C$
	1/8" from case for 5 seconds			

### Thermal Characteristics

Symbol	Parameter	Max.		Units
		SLP5N65S	SLF5N65S	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.20	3.47	$^\circ C/W$
$R_{\theta JS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	--	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	$^\circ C/W$

## Electrical Characteristics

$T_C = 25^\circ \text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \text{ }\mu\text{A}$	650	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.6	--	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 650 \text{ V}, V_{GS} = 0 \text{ V}$	--	--	10	$\mu\text{A}$
		$V_{DS} = 520 \text{ V}, T_C = 125^\circ\text{C}$	--	--	50	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30 \text{ V}, V_{DS} = 0 \text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30 \text{ V}, V_{DS} = 0 \text{ V}$	--	--	-100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \text{ }\mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 2.0 \text{ A}$	--	2.0	2.5	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40 \text{ V}, I_D = 2.0 \text{ A}$ (Note 4)	--	2.5	--	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}, f = 1.0 \text{ MHz}$	--	600	--	pF
$C_{oss}$	Output Capacitance		--	53.8	--	pF
$C_{riss}$	Reverse Transfer Capacitance		--	3.2	--	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 100 \text{ V}, I_D = 2.0 \text{ A}, R_G = 25 \Omega$ (Note 4, 5)	--	30	--	ns
$t_r$	Turn-On Rise Time		--	10	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	60	--	ns
$t_f$	Turn-Off Fall Time		--	50	--	ns
$Q_g$	Total Gate Charge		$V_{DS} = 100 \text{ V}, I_D = 3.0 \text{ A}, V_{GS} = 10 \text{ V}$ (Note 4, 5)	--	13	--
$Q_{gs}$	Gate-Source Charge	--		3.6	--	nC
$Q_{gd}$	Gate-Drain Charge	--		2	--	nC

### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	4.0	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	16	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 4.0 \text{ A}$	--	--	1.4	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_S = 4.0 \text{ A}$ ,	--	230	--	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F / dt = 100 \text{ A}/\mu\text{s}$ (Note 4)	--	1.6	--	$\mu\text{C}$

#### Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $I_{AS} = 4.0 \text{ A}, L = 15 \text{ mH}, V_{DD} = 50 \text{ V}, R_G = 25 \Omega$ , Starting  $T_J = 25^\circ \text{C}$
3.  $I_{SD} \leq 4.0 \text{ A}, di/dt \leq 200 \text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ \text{C}$
4. Pulse Test : Pulse width  $\leq 300 \mu\text{s}$ , Duty cycle  $\leq 2\%$
5. Essentially independent of operating temperature

### Typical Characteristics

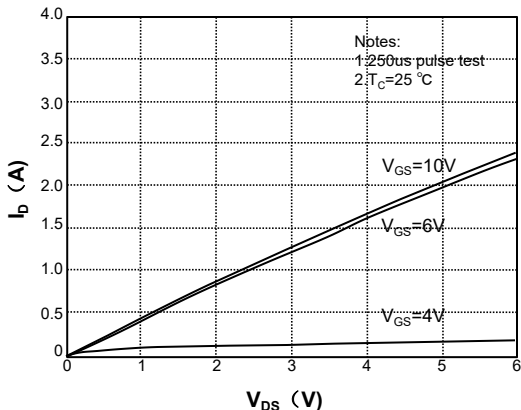


Figure 1. Typical Output Characteristics

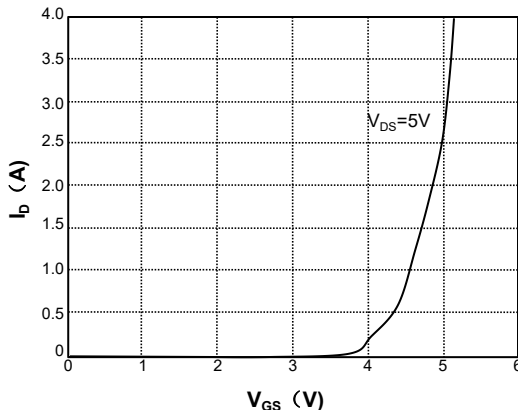


Figure 2. Transfer Characteristics

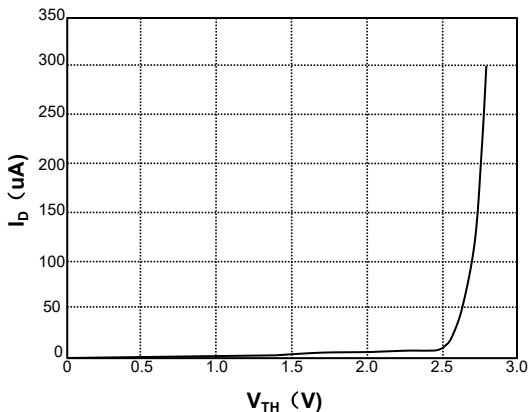


Figure 3. Drain Current VS Gate Threshold Voltage

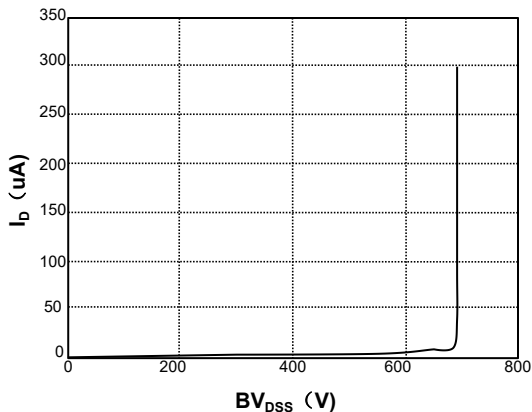


Figure 4. Drain Current VS DS Breakdown Voltage

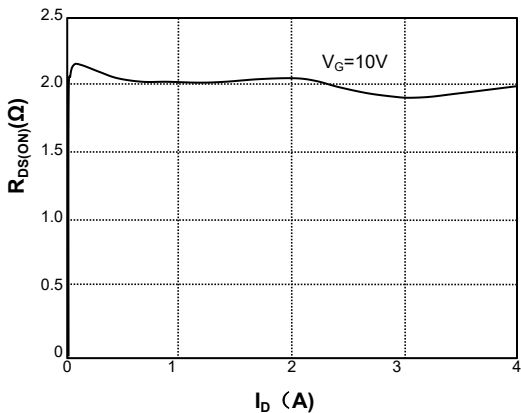


Figure 5.  $R_{DS(ON)}$  VS Drain Current

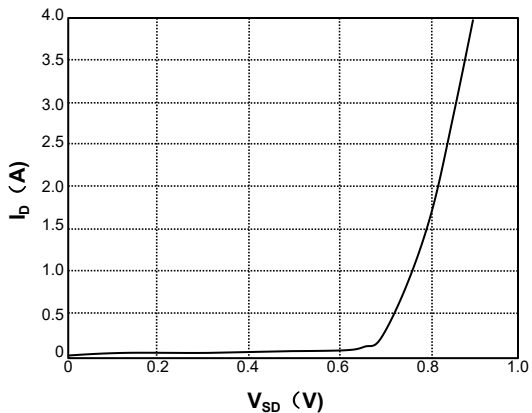


Figure 6. Drain Current vs Source Drain Voltage,  $V_{SD}$

## Typical Characteristics (Continued)

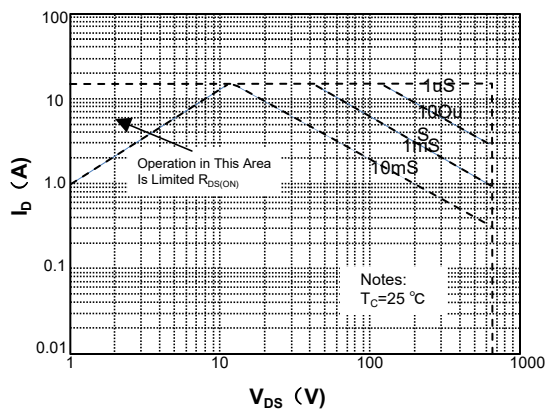
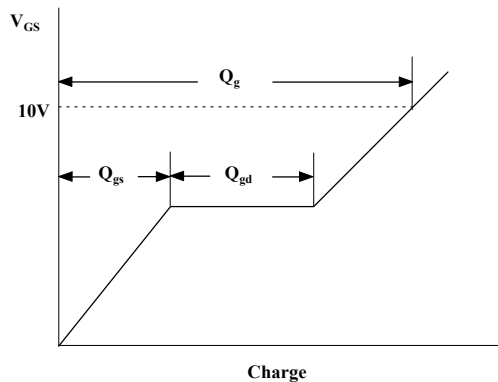
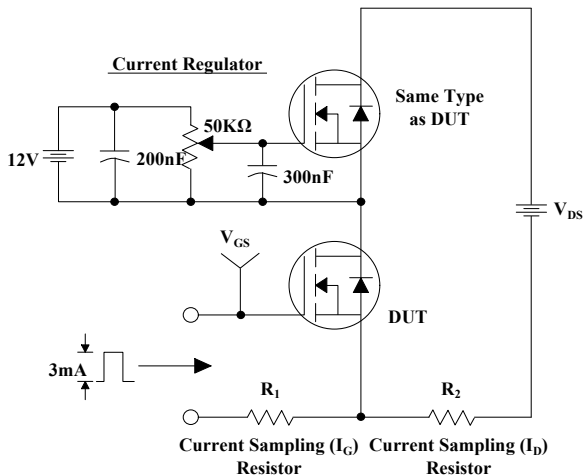
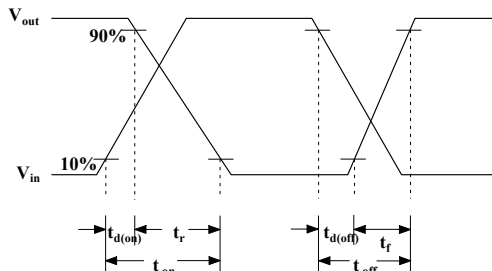
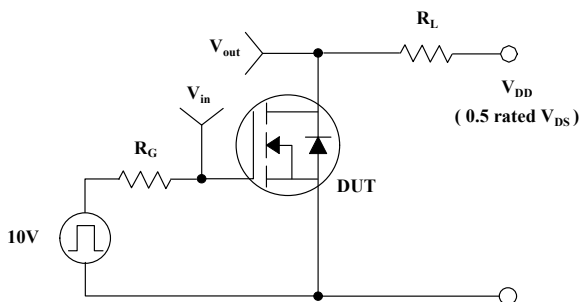


Figure 6. Maximum Safe Operating Area

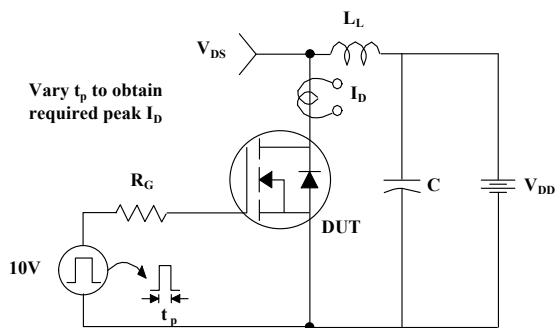
### Gate Charge Test Circuit & Waveform



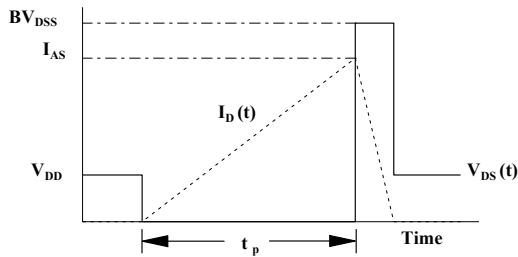
### Resistive Switching Test Circuit & Waveforms



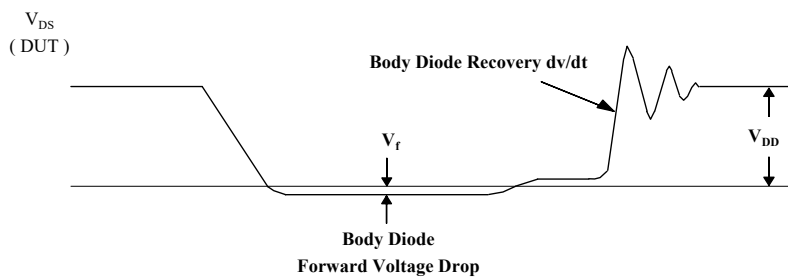
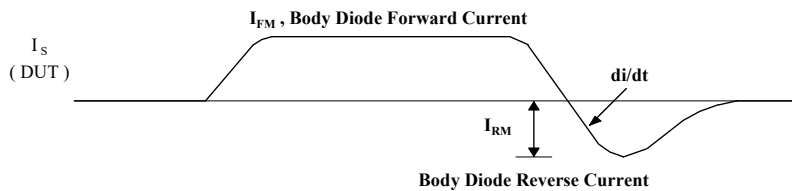
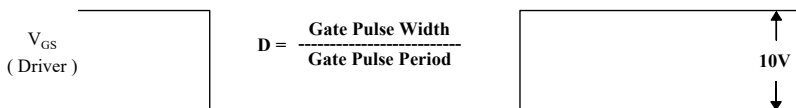
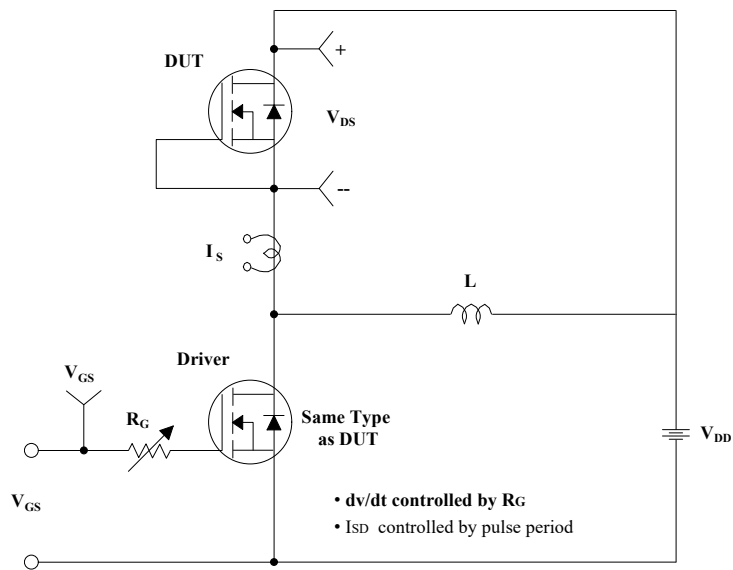
### Unclamped Inductive Switching Test Circuit & Waveforms



$$E_{AS} = \frac{1}{2} L_L I_{AS}^2 - \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



## Peak Diode Recovery dv/dt Test Circuit & Waveforms



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