

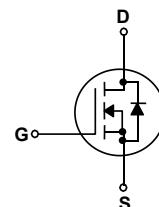
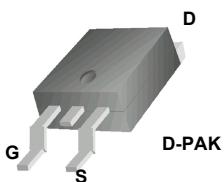
# SLD70R900S2 / SLF70R900S2 700V N-Channel Power MOSFET

## General Description

This Power MOSFET is produced using Maple semi's advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology

## Features

- 5A, 700V,  $R_{DS(on)}$  typ. =  $0.8\Omega$ @ $V_{GS} = 10\text{ V}$
- Extended Safe Operating Area
- Ease of Parallelizing
- Fast Switching
- 100% avalanche tested
- 100% Single Pulse avalanche energy Test



## Absolute Maximum Ratings

Symbol	Parameter	SLF70R900S2	SLD70R900S2	Units
$V_{DSS}$	Drain-to-Source Breakdown Voltage	700		V
$I_D$	Drain Current - Continuous ( $T_c = 25^\circ\text{C}$ )	5		A
	Drain Current - Continuous ( $T_c = 100^\circ\text{C}$ )	3.2		A
$I_{DM}$	Drain Current - Pulsed	18		A
$V_{GS}$	Gate-Source Voltage	$\pm 30$		V
$P_{tot}$	Power Dissipation ( $T_c = 25^\circ\text{C}$ )	24	58	W
$T_J$	Operating Junction Temperature Range	-55 to +150		°C
EAS	Single Pulsed Avalanche Energy (Note 2)	180		mJ

## Electrical Characteristics @ $T_J=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{DS}$	Drain-source Voltage	$V_{GS} = 0\text{V}$ , $I_D = 250\mu\text{A}$	700			V
$R_{DS(on)}$	Static Drain-to-Source on-Resistance	$V_{GS} = 10\text{V}$ , $I_D = 20\text{A}$		0.8	0.9	Ω
$V_{GS(th)}$	Gated Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 250\mu\text{A}$	2.0	3.0	4.0	V

IDSS	Zero Gate Voltage Drain Current	VDS=100V, VGS = 0V			1.0	µA
IGSS(F)	Gated Body Leakage Current	VGS = +30V,			100	nA
IGSS(R)	Gated Body Leakage Current	VGS = -30V,			-100	nA
Ciss	Input Capacitance	VGS =0V, VDS=25V, f=1.0MHZ	360			pF
Coss	Output Capacitance		21			pF
Crss	Reverse Transfer Capacitance		1.9			pF
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =560V I <sub>D</sub> =5A V <sub>GS</sub> =10V	19.2			nC
Q <sub>qs</sub>	Gate-Source Charge		2.45			nC
Q <sub>qd</sub>	Gate-Drain Charge		11.7			nC
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DD</sub> =350V,I <sub>D</sub> =5A V <sub>GS</sub> =10V,R <sub>G</sub> =24Ω	9.47			nS
t <sub>r</sub>	Turn-on Rise Time		26.3			nS
t <sub>d(off)</sub>	Turn-off Delay Time		57.9			nS
t <sub>f</sub>	Turn-off Fall Time		25.7			nS

## Source-Drain Diode Maximum Ratings and Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I <sub>SD</sub>	S-D Current(Body Diode)				5	A
I <sub>SDM</sub>	Pulsed S-D Current(Body Diode)				18.0	A
VSD	Diode Forward Voltage	VGS =0V, IDS=5A			1.4	V
t <sub>rr</sub>	Reverse Recovery Time	T <sub>J</sub> =25°C,I <sub>F</sub> =5A di/dt=100 A/us	305			nS
Q <sub>rr</sub>	Reverse Recovery Charge		2.3			nC

\*Pulse Test: Pulse Width≤300µs, Duty Cycle≤2%

## Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case		5.21	°C/W
R <sub>θJA</sub>	Junction-to-Ambient		62.5	°C/W

### Notes:

- Repetitive Rating : Pulse width limited by maximum junction temperature
- L = 79mH, IAS = 2.0A, VDD =100V, RG = 25Ω, Starting TJ = 25° C
- ISD 5.0A, di/dt 100A/us, VDD BVDSS, Starting TJ = 25° C
- Pulse Test : Pulse width 300us, Duty cycle 2%
- Essentially independent of operating temperature

## Typical Characteristics

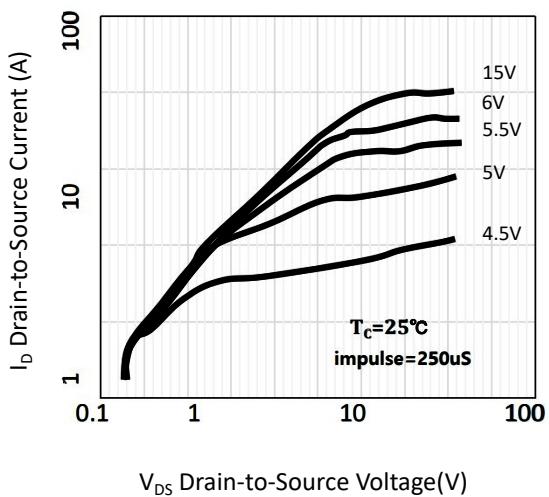


Figure 1. Typical Output Characteristics

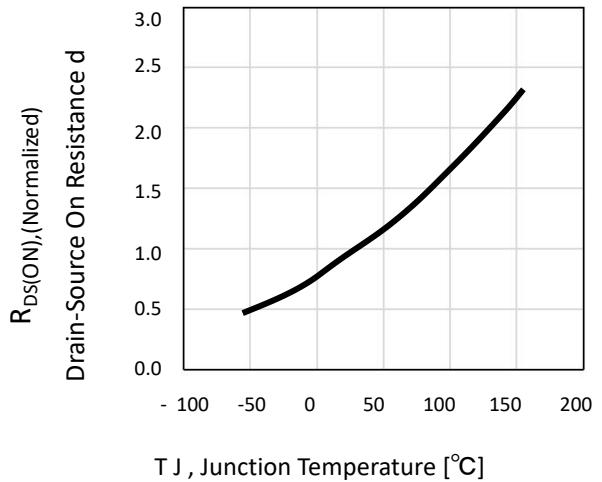


Figure 2. Typical Output Characteristics

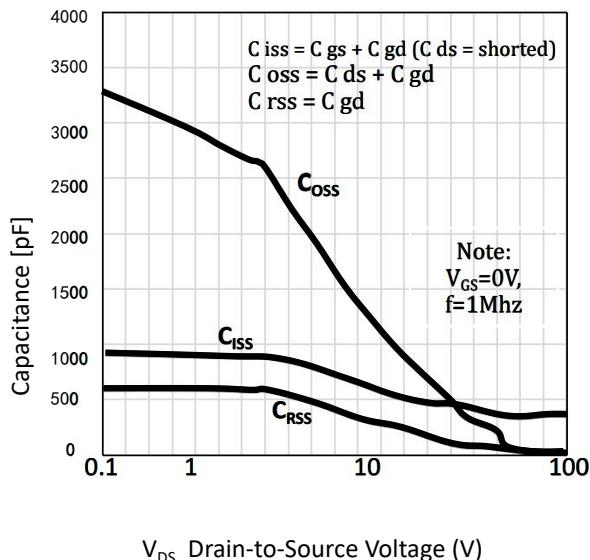


Figure 3. Typical Capacitance Vs Drain-Source Voltage

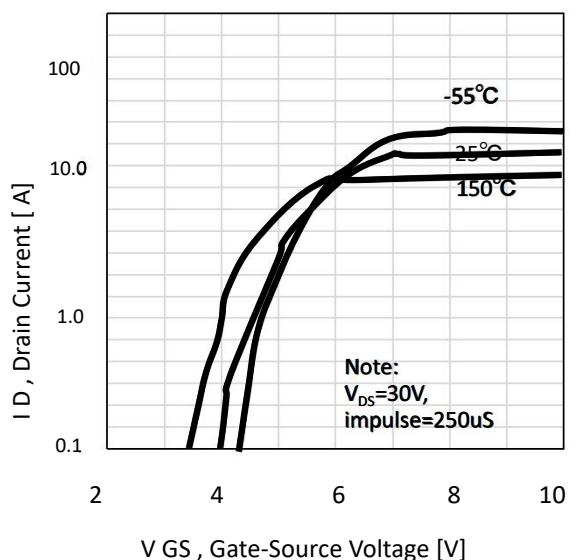
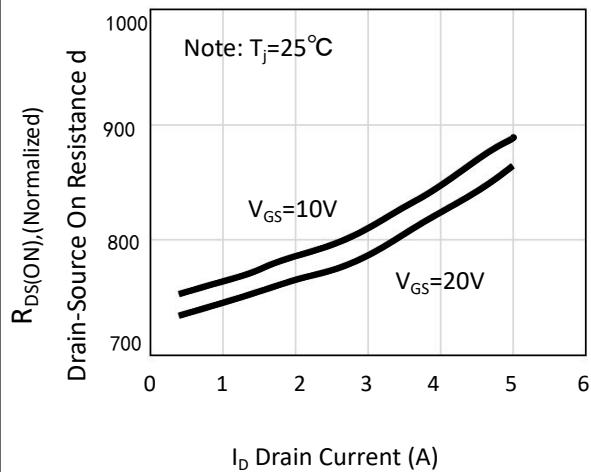
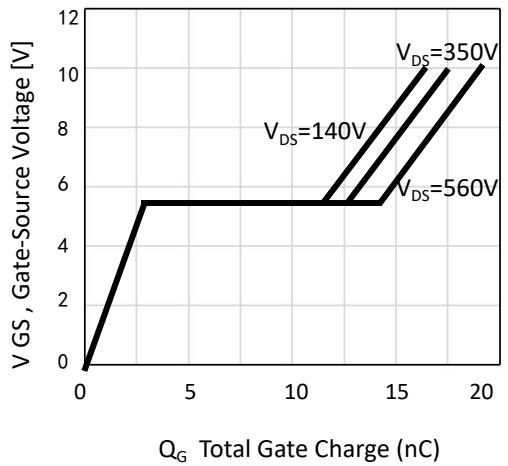
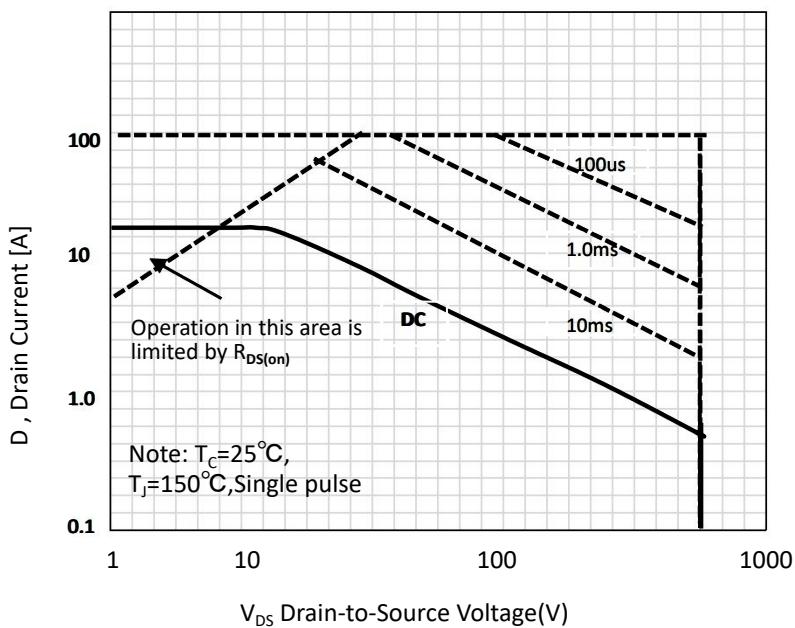
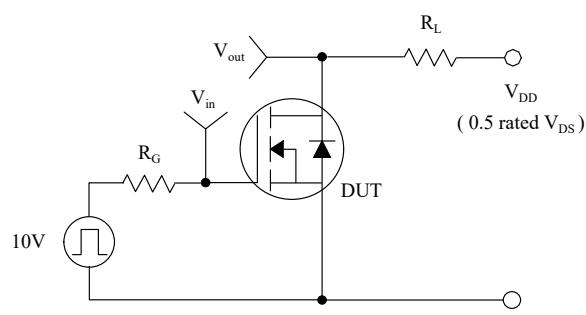
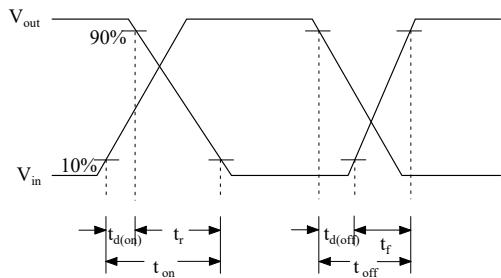
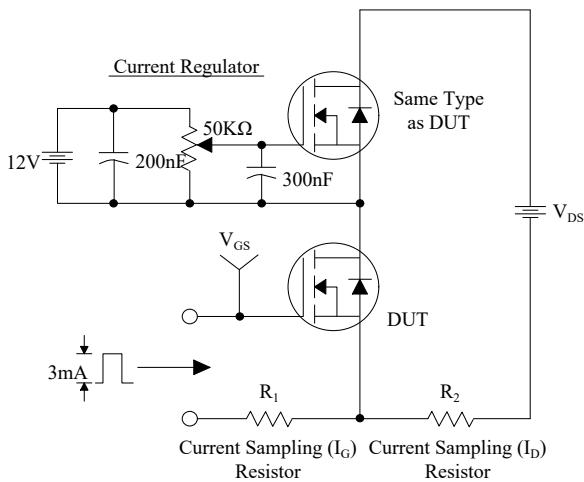
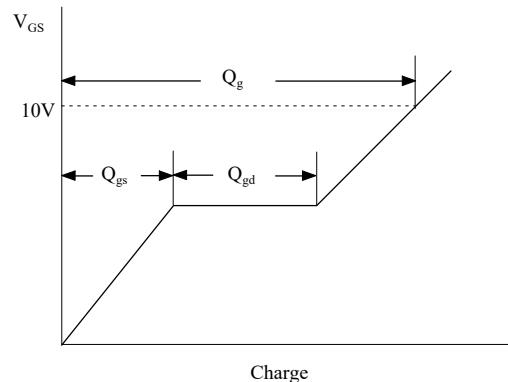
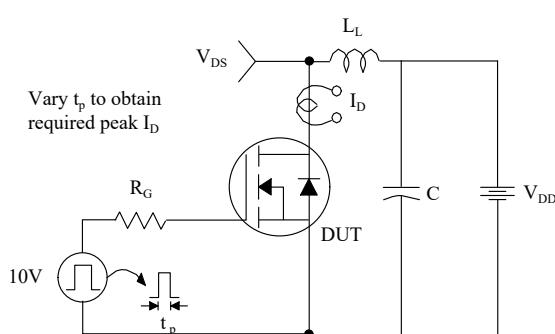
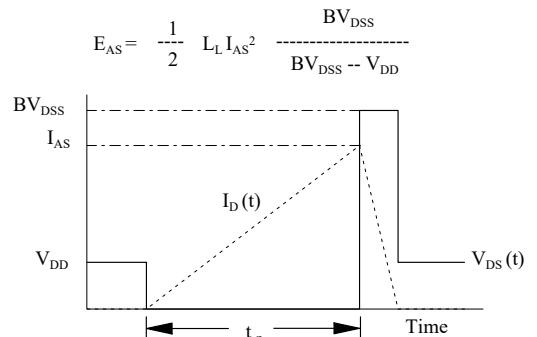


Figure 4. On-Resistance Vs Drain Current

**Figure 5.**  $R_{DS(ON)}$  Vs Drain Current , Gate-Source Voltage**Figure 6.** Typical Gate Charge Vs Gate-Source Voltage**Figure 7.** Maximum Safe Operating Area

**Figure 8 a.** Switching Time Test Circuit**Figure 8 b.** Switching Time Waveforms**Figure 9 a.** Gate Charge Test Circuit**Figure 9 b.** Basic Gate Charge Waveforms**Figure 10 a.** Unclamped Inductive Switching Test Circuit**Figure 10 b.** Switching Test Waveforms

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