

SLD750U / SLF750U

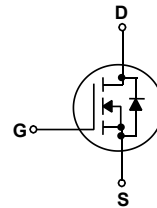
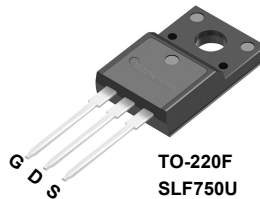
430V N-Channel MOSFET

General Description

This Power MOSFET is produced using Maple semi's advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

Features

- N-Channel:430V 11A
 $R_{DS(on)Typ}=0.54\Omega@V_{GS} = 10 V$
- Very Low On-resistance RDS(ON)
- LowCrss
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Absolute Maximum Ratings

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	SLD750U / SLF750U		Units
V_{DSS}	Drain-Source Voltage	430		V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$) - Continuous ($T_C = 100^\circ\text{C}$)	11		A
		6.7		A
I_{DM}	Drain Current - Pulsed (Note 1)	33		A
V_{GSS}	Gate-Source Voltage	± 30		V
E_{AS}	Single Pulsed Avalanche Energy	437		mJ
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	-	35	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	-	3.57	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		$^\circ\text{C}$

* Drain current limited by maximum junction temperature.

Package Marking

Part Number	Top Marking	Package	Packing Method	MOQ	QTY
SLD750U	SLP750U	TO-252	Tape	2500	25000
SLF750U	SLF750U	TO-220F	Tube	1000	5000

Electrical Characteristics

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	430	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
		$V_{DS} = 340\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	-	4	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 5.5\text{ A}$	--	0.54	0.62	Ω

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	835	-	pF
C_{oss}	Output Capacitance		--	98	-	pF
C_{rss}	Reverse Transfer Capacitance		--	3.85	-	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DS} = 210\text{ V},$ $R_G = 25\Omega, I_D = 5.5\text{ A}$	--	19	--	ns
t_r	Turn-On Rise Time		--	70	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	70	--	ns
t_f	Turn-Off Fall Time		--	27	--	ns
Q_g	Total Gate Charge	$V_{DS} = 210\text{ V}, I_D = 5.5\text{ A},$ $V_{GS} = 10\text{ V}$	--	23	--	nC
Q_{gs}	Gate-Source Charge		--	5.4	--	nC
Q_{gd}	Gate-Drain Charge		--	5	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	11	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	33	A
V_{SD}	Drain to Source Diode Forward Voltage, $V_{GS} = 0\text{ V}, I_{SD} = 11\text{ A}, T_J = 25^\circ\text{C}$	--	--	1.4	V
t_{rr}	Reverse Recovery Time & $T_J = 25^\circ\text{C}, I_F = 5.5\text{ A } di/dt = 100\text{ A}/\mu\text{s}$	--	410	-	nS
Q_{rr}	Reverse Recovery Charge & $T_J = 25^\circ\text{C}, I_F = 5.5\text{ A } di/dt = 100\text{ A}/\mu\text{s}$	--	7	-	nC

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. EAS condition: $T_J = 25^\circ\text{C}, V_{DD} = 50\text{ V}, V_G = 10\text{ V}, R_G = 25\Omega,$
3. Pulse Test: Pulse Widths $\leq 300\mu\text{s}$, Duty Cycles $\leq 0.5\%$

N- Channel Typical Characteristics

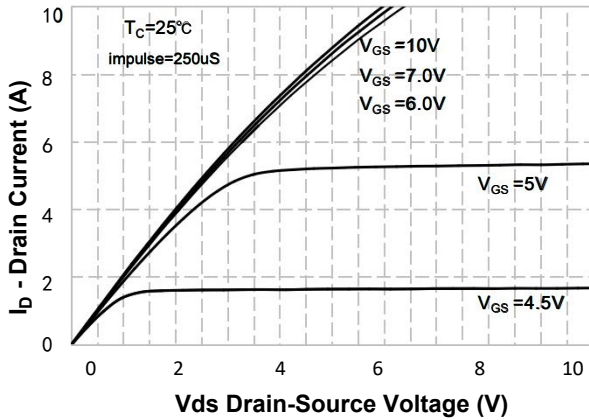


Figure 1. On-Region Characteristics

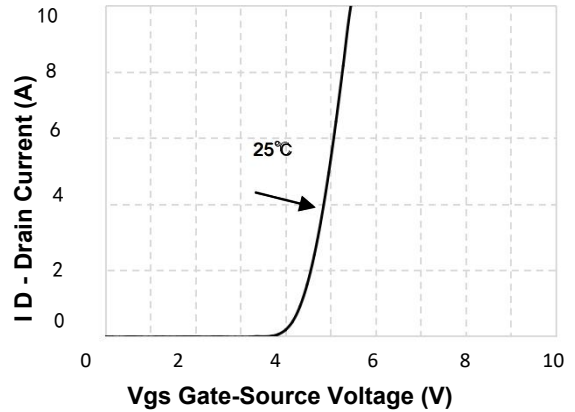


Figure 2. Transfer Characteristics

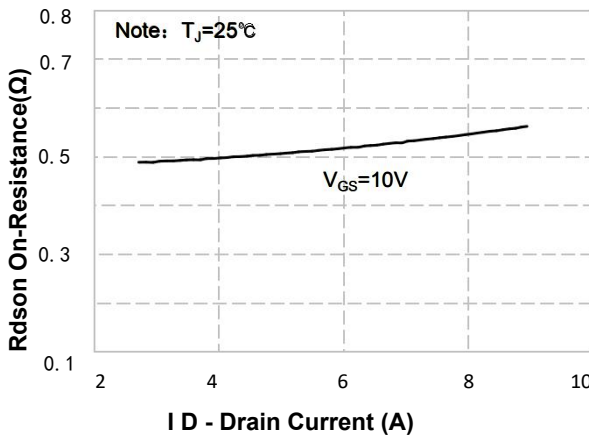


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

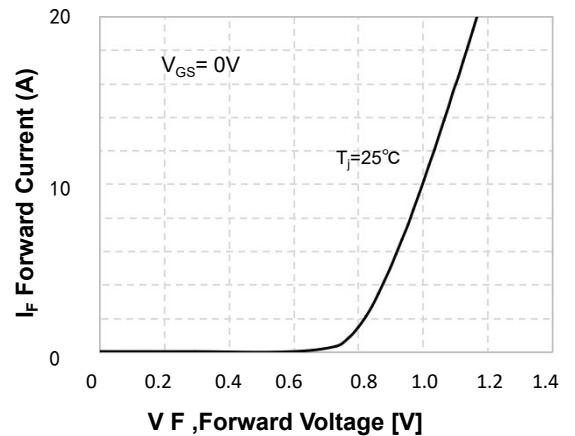


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

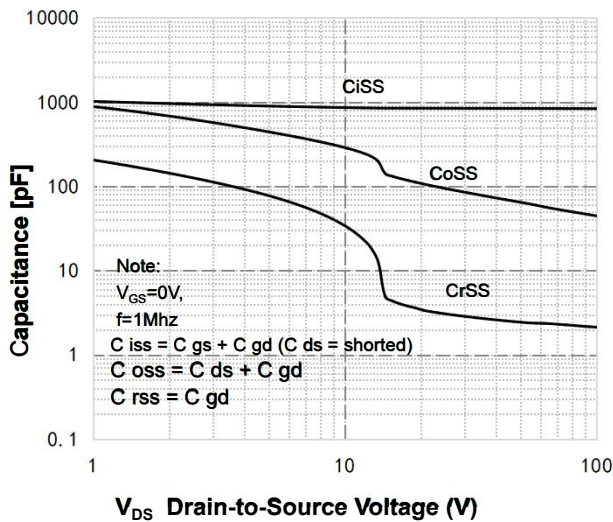


Figure 5. Capacitance Characteristics

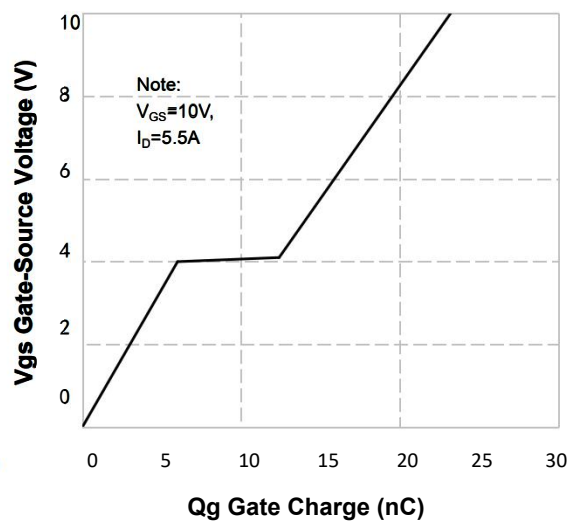


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

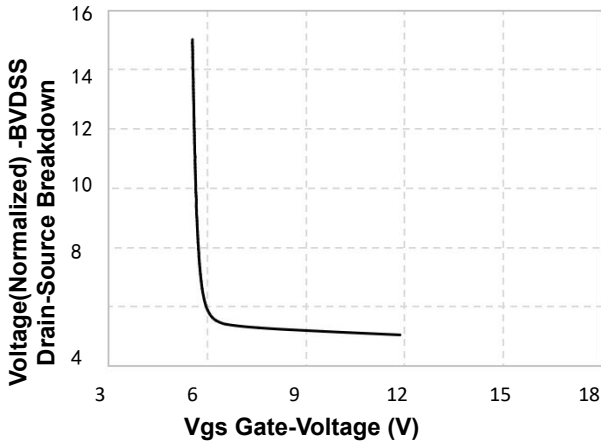


Figure 7. Breakdown Voltage Variation vs Gate-Voltage

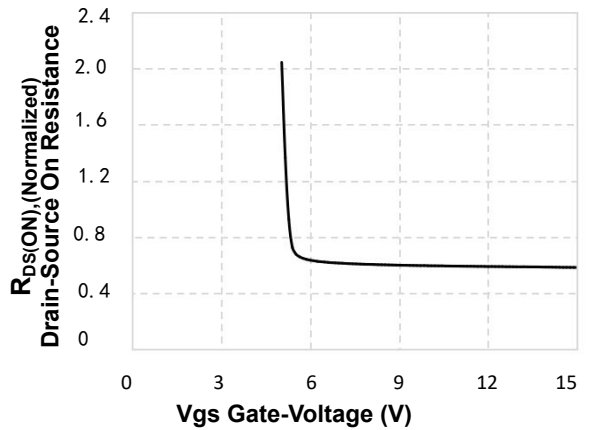


Figure 8. On-Resistance Variation vs Gate-Voltage

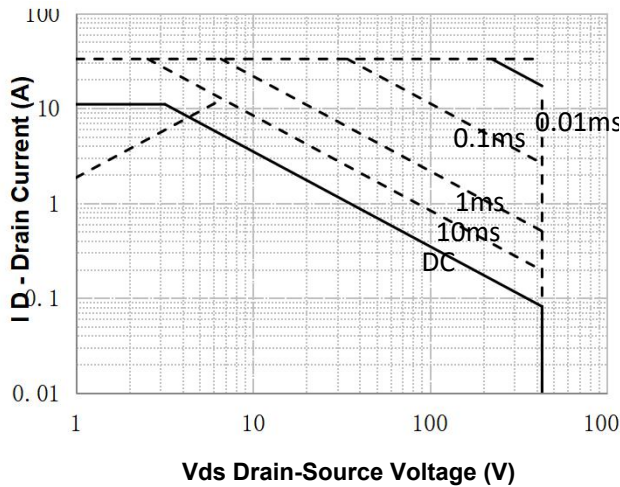


Figure 9. Maximum Safe Operating Area

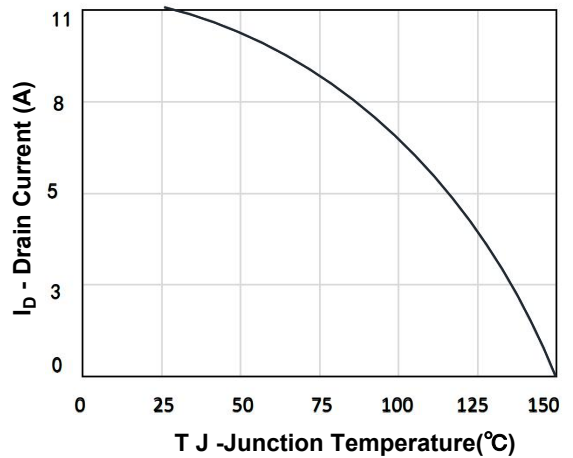


Figure 10. Maximum Drain Current vs Case Temperature

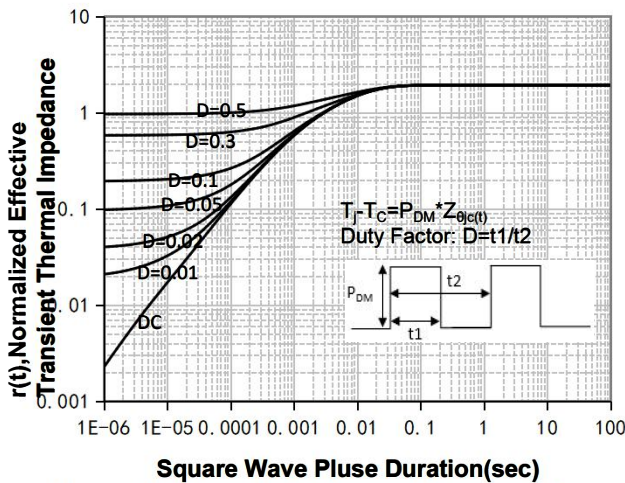
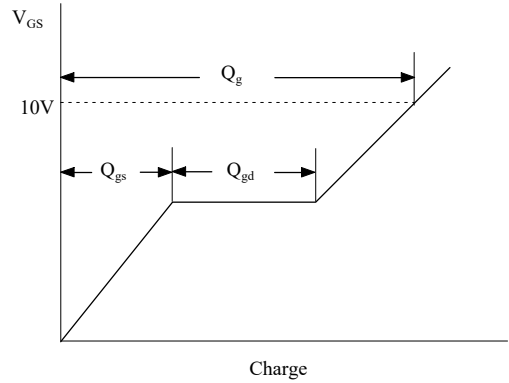
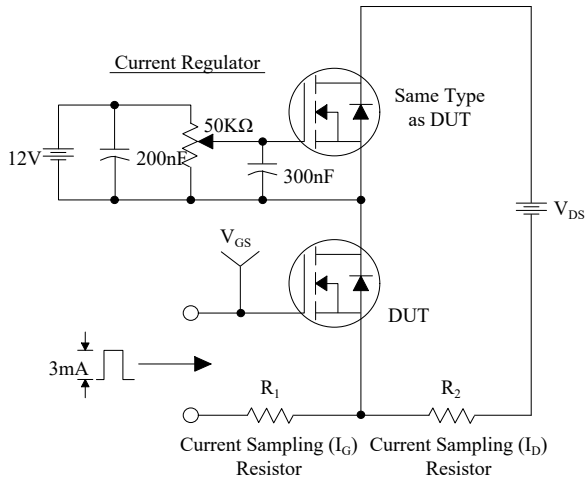
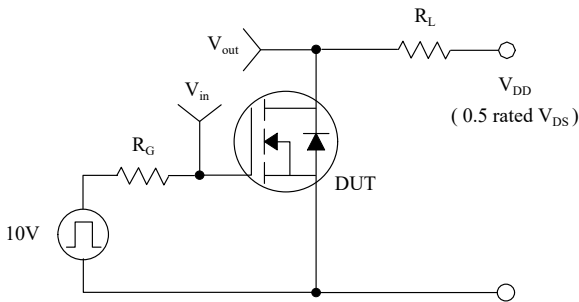


Figure 11. Transient Thermal Response Curve

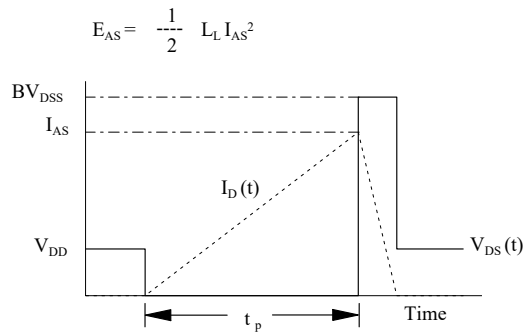
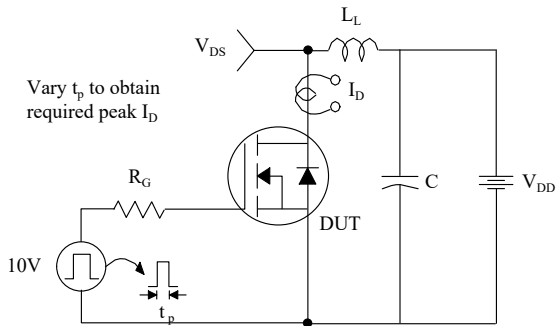
Gate Charge Test Circuit & Waveform



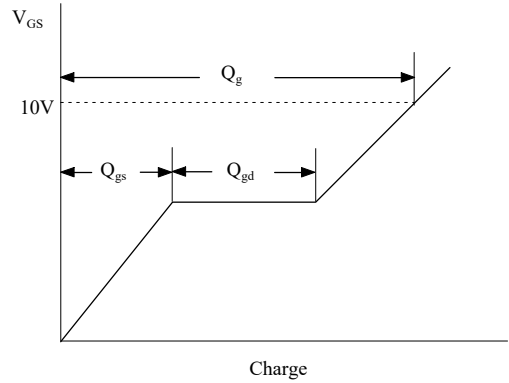
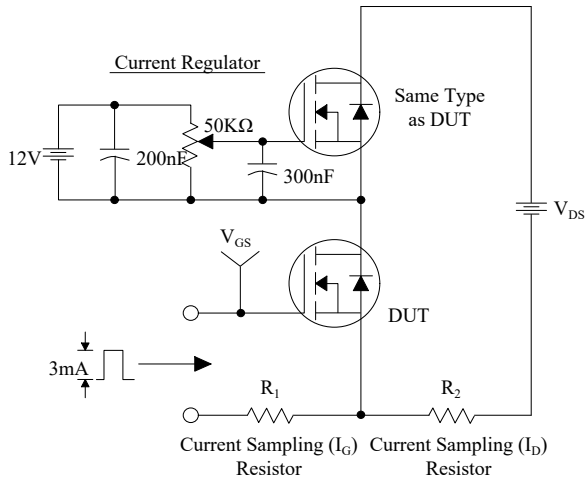
Resistive Switching Test Circuit & Waveforms



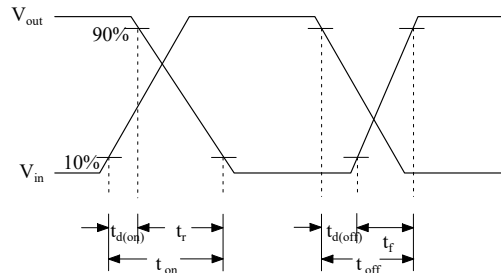
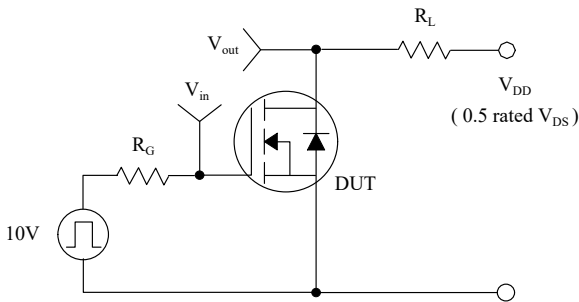
Unclamped Inductive Switching Test Circuit & Waveforms



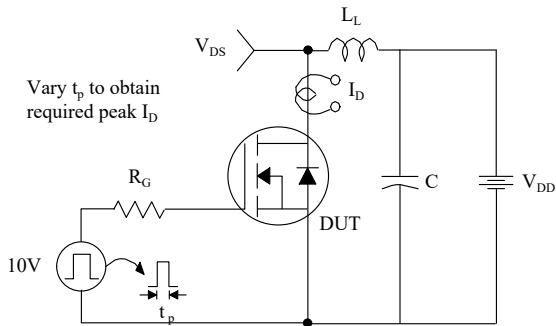
Gate Charge Test Circuit & Waveform



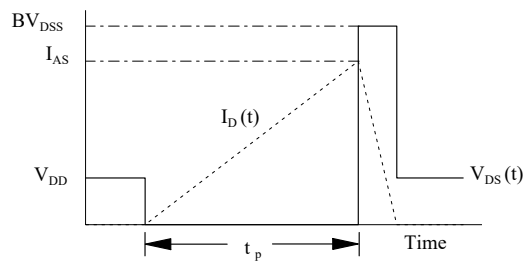
Resistive Switching Test Circuit & Waveforms



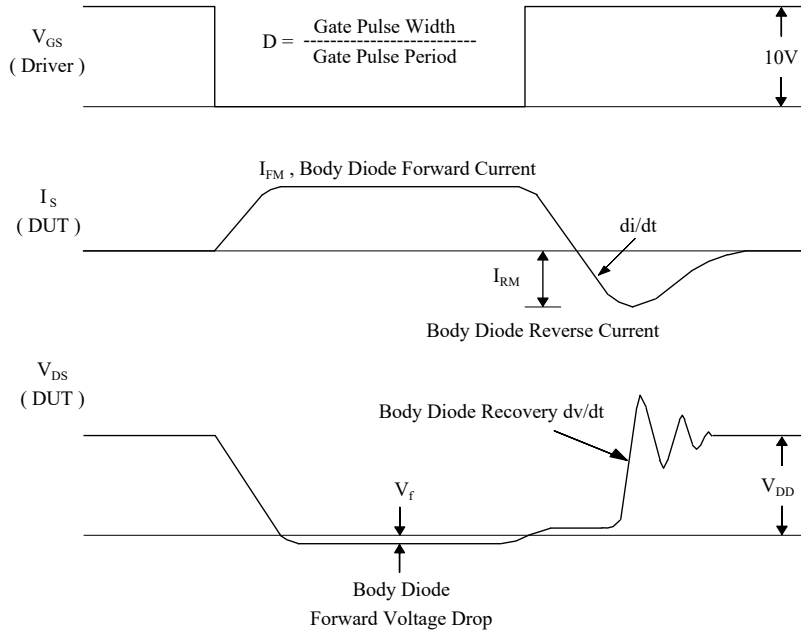
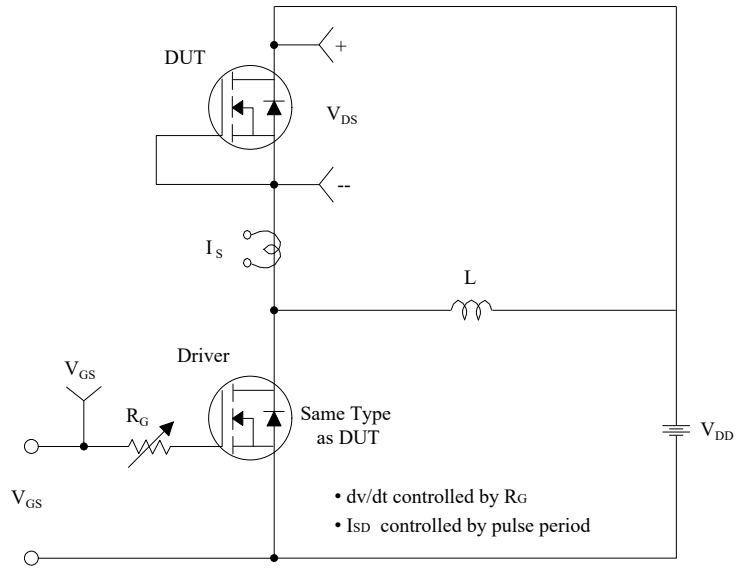
Unclamped Inductive Switching Test Circuit & Waveforms



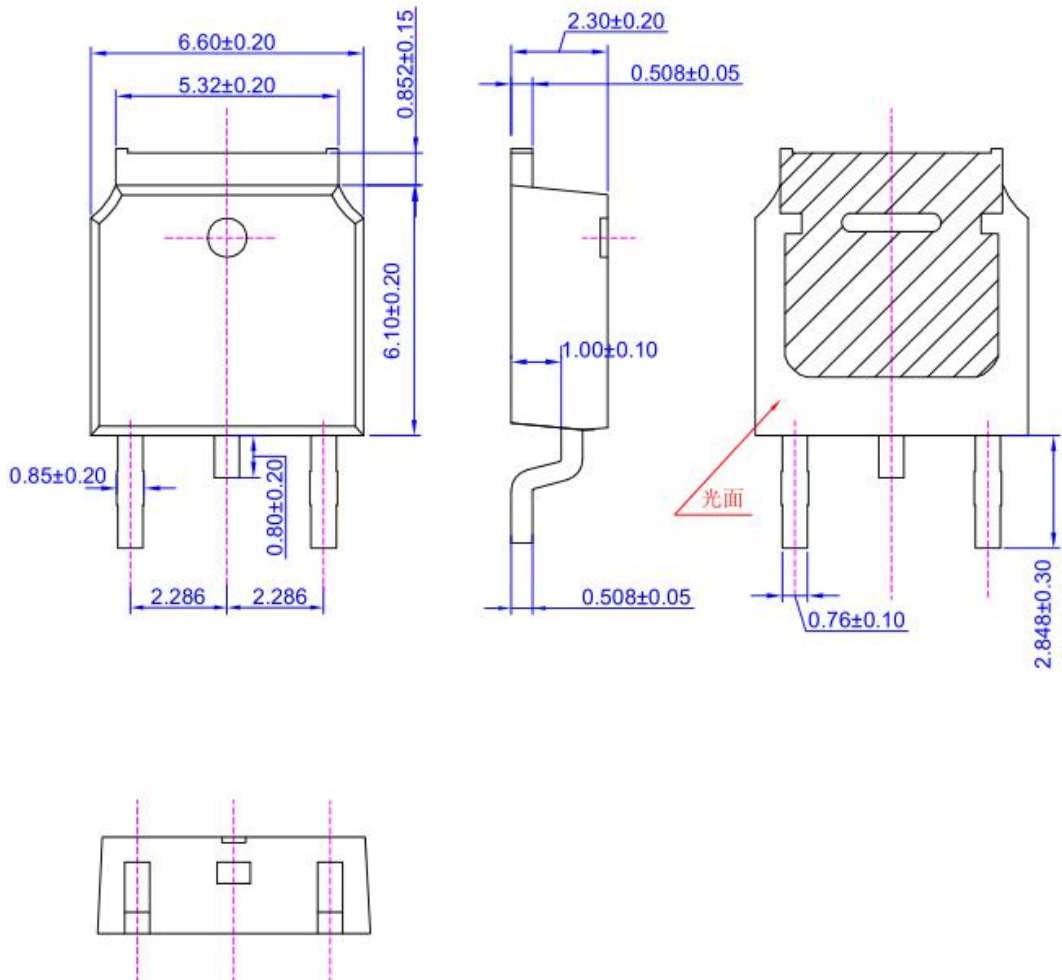
$$E_{AS} = \frac{1}{2} L_L I_{AS}^2$$



Peak Diode Recovery dv/dt Test Circuit & Waveforms



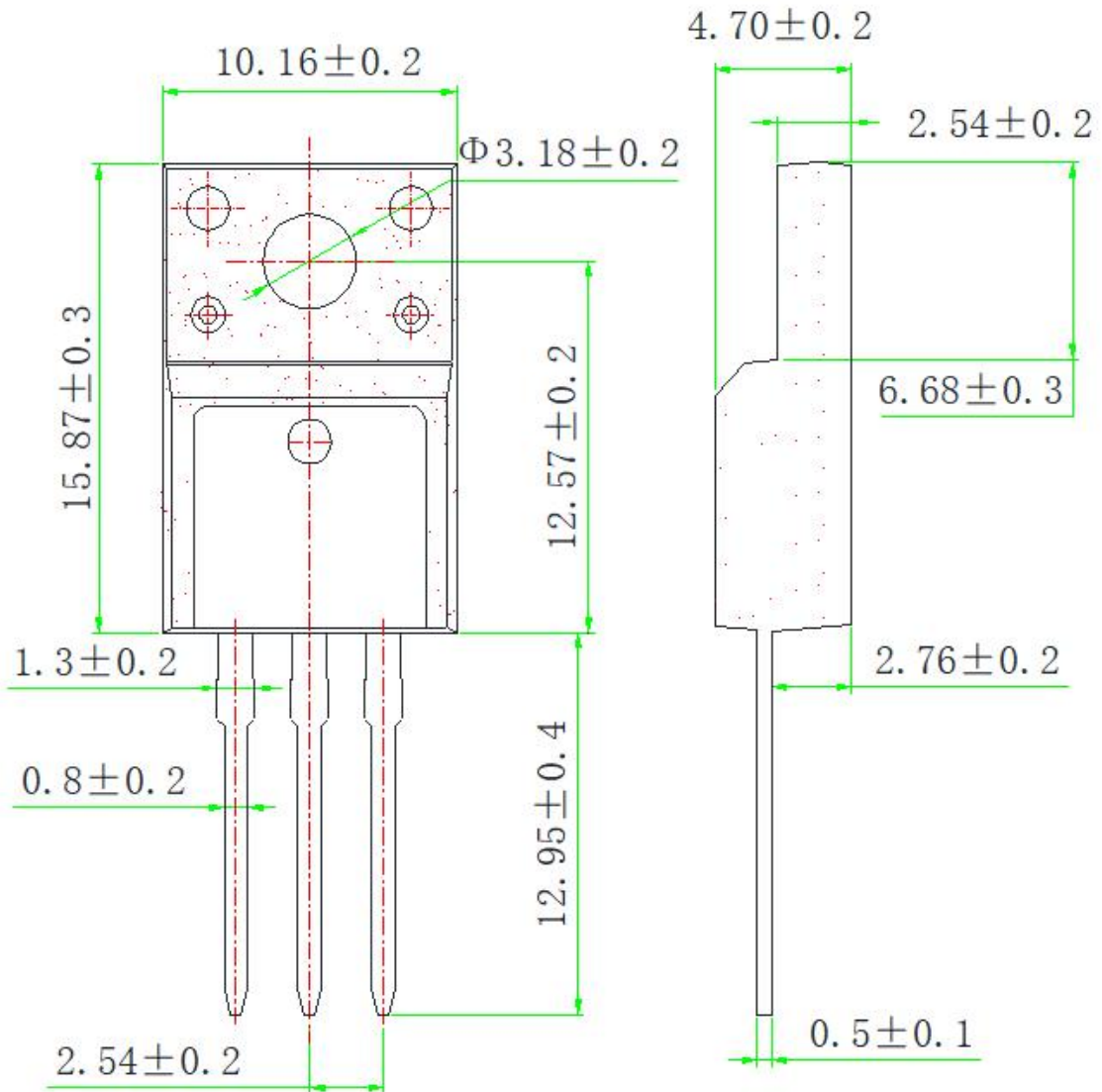
TO-252 OUTLINE



NOTE:

1. The plastic package is not marked as smooth surface $Ra=0.1$; Subglossy surface $Ra=0.8$
2. Undeclared tolerance ± 0.25 , Unmarked fillet $R_{max}=0.25$

TO-220F OUTLINE



Note: Distance from top pinhole to colloid surface 0.8 ± 0.15 mm

NAME	TO-220F OUTLINE	UNIT	mm	DESIGNED	Shawn Chen	THIRD ANGLE SYSTEM
DWGNO		PAGE	1 OF 1	CHECKED		
VERSION	Ver1.0	ISSUE DATE		APPROVED		

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