



SLP8N65C/SLF8N65C 650V N-Channel MOSFET

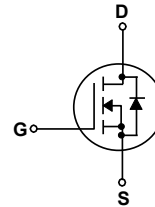
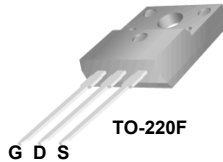
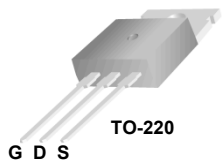
SLP8N65C / SLF8N65C

General Description

This Power MOSFET is produced using Maple semi's advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

Features

- 7.5A, 650V, $R_{DS(on) typ.} = 1.2\Omega @ V_{GS} = 10V$
- Low gate charge (typical 29nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Absolute Maximum Ratings T_C = 25°C unless otherwise noted

| Symbol | Parameter | SLP8N65C | SLF8N65C | Units |
|-----------------------------------|---|-------------|----------|-------|
| V _{DSS} | Drain-Source Voltage | 650 | | V |
| I _D | Drain Current - Continuous (T _C = 25°C) - Continuous (T _C = 100°C) | 7.5 | 7.5 * | A |
| | | 4.5 | 4.5 * | A |
| I _{DM} | Drain Current - Pulsed (Note 1) | 30 | 30 * | A |
| V _{GSS} | Gate-Source Voltage | ±30 | | V |
| E _{AS} | Single Pulsed Avalanche Energy (Note 2) | 230 | | mJ |
| I _{AR} | Avalanche Current (Note 1) | 7.5 | | A |
| E _{AR} | Repetitive Avalanche Energy (Note 1) | 21 | | mJ |
| dv/dt | Peak Diode Recovery dv/dt (Note 3) | 4.5 | | V/ns |
| P _D | Power Dissipation (T _C = 25°C) - Derate above 25°C | 210 | 40 | W |
| | | 1.68 | 0.32 | W/°C |
| T _J , T _{STG} | Operating and Storage Temperature Range | -55 to +150 | | °C |
| T _L | Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds | 300 | | °C |

* Drain current limited by maximum junction temperature.

Thermal Characteristics

| Symbol | Parameter | SLP8N65C | SLF8N65C | Units |
|------------------|---|----------|----------|-------|
| R _{θJC} | Thermal Resistance, Junction-to-Case | 0.6 | 3.1 | °C/W |
| R _{θJS} | Thermal Resistance, Case-to-Sink Typ. | 0.5 | -- | °C/W |
| R _{θJA} | Thermal Resistance, Junction-to-Ambient | 62.5 | 62.5 | °C/W |

Electrical CharacteristicsT_C = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|--------------------------------------|---|---|-----|-----|------|-------|
| Off Characteristics | | | | | | |
| BV _{DSS} | Drain-Source Breakdown Voltage | V _{GS} = 0 V, I _D = 250 μA | 650 | -- | -- | V |
| ΔBV _{DSS} / ΔT _J | Breakdown Voltage Temperature Coefficient | I _D = 250 μA, Referenced to 25°C | -- | 0.7 | -- | V/°C |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} = 650 V, V _{GS} = 0 V | -- | -- | 1 | μA |
| | | V _{DS} = 520 V, T _C = 125°C | -- | -- | 10 | μA |
| I _{GSSF} | Gate-Body Leakage Current, Forward | V _{GS} = 30 V, V _{DS} = 0 V | -- | -- | 100 | nA |
| I _{GSSR} | Gate-Body Leakage Current, Reverse | V _{GS} = -30 V, V _{DS} = 0 V | -- | -- | -100 | nA |

On Characteristics

| | | | | | | |
|---------------------|-----------------------------------|---|-----|-----|-----|---|
| V _{GS(th)} | Gate Threshold Voltage | V _{DS} = V _{GS} , I _D = 250 μA | 2.0 | -- | 4.0 | V |
| R _{DS(on)} | Static Drain-Source On-Resistance | V _{GS} = 10 V, I _D = 3.75 A | -- | 1.2 | 1.4 | Ω |
| g _{FS} | Forward Transconductance | V _{DS} = 40 V, I _D = 3.75 A (Note 4) | -- | 7.5 | -- | S |

Dynamic Characteristics

| | | | | | | |
|------------------|------------------------------|---|----|------|----|----|
| C _{iss} | Input Capacitance | V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz | -- | 1000 | -- | pF |
| C _{oss} | Output Capacitance | | -- | 110 | -- | pF |
| C _{rss} | Reverse Transfer Capacitance | | -- | 12 | -- | pF |

Switching Characteristics

| | | | | | | |
|---------------------|---------------------|---|----|------|----|----|
| t _{d(on)} | Turn-On Delay Time | V _{DD} = 325 V, I _D = 7.5 A, R _G = 25 Ω (Note 4, 5) | -- | 20 | -- | ns |
| t _r | Turn-On Rise Time | | -- | 50 | -- | ns |
| t _{d(off)} | Turn-Off Delay Time | | -- | 80 | -- | ns |
| t _f | Turn-Off Fall Time | | -- | 70 | -- | ns |
| Q _g | Total Gate Charge | V _{DS} = 520 V, I _D = 7.5 A, V _{GS} = 10 V (Note 4, 5) | -- | 29 | -- | nC |
| Q _{gs} | Gate-Source Charge | | -- | 4.7 | -- | nC |
| Q _{gd} | Gate-Drain Charge | | -- | 12.5 | -- | nC |

Drain-Source Diode Characteristics and Maximum Ratings

| | | | | | | |
|-----------------|---|--|----|-----|-----|----|
| I _S | Maximum Continuous Drain-Source Diode Forward Current | -- | -- | 7.5 | A | |
| I _{SM} | Maximum Pulsed Drain-Source Diode Forward Current | -- | -- | 30 | A | |
| V _{SD} | Drain-Source Diode Forward Voltage | V _{GS} = 0 V, I _S = 7.5 A | -- | -- | 1.4 | V |
| t _{rr} | Reverse Recovery Time | V _{GS} = 0 V, I _S = 7.5 A, | -- | 350 | -- | ns |
| Q _{rr} | Reverse Recovery Charge | di _F / dt = 100 A/us (Note 4) | -- | 3.3 | -- | μC |

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 8mH, I_{AS} = 7.5A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
3. I_{SD} ≤ 7A, di/dt ≤ 200A/us, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300us, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

Typical Characteristics

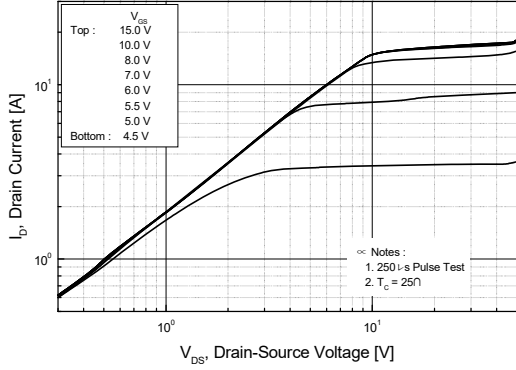


Figure 1. On-Region Characteristics

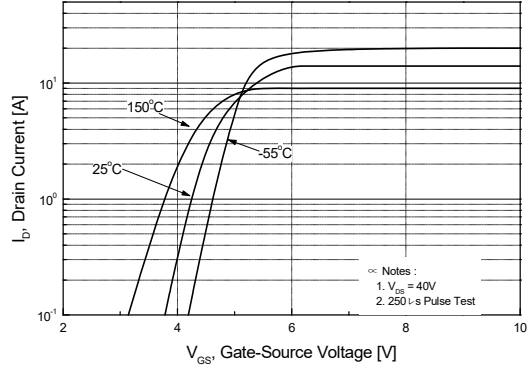


Figure 2. Transfer Characteristics

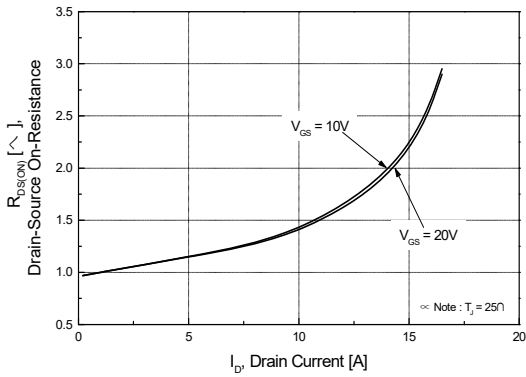


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

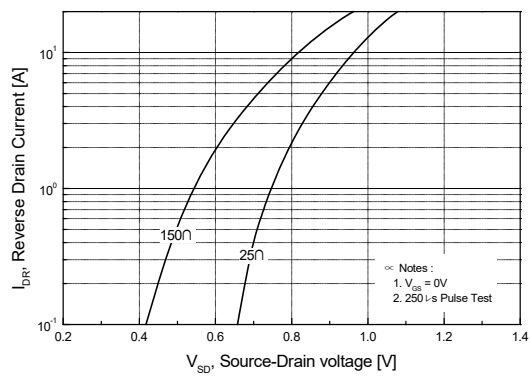


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

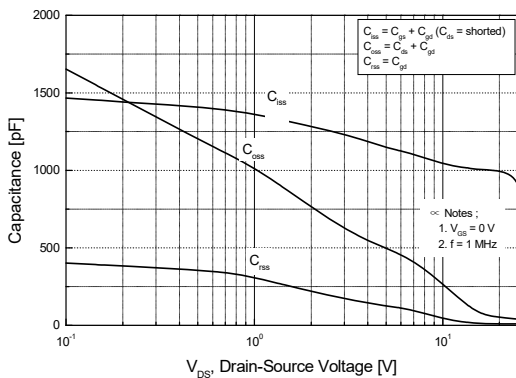


Figure 5. Capacitance Characteristics

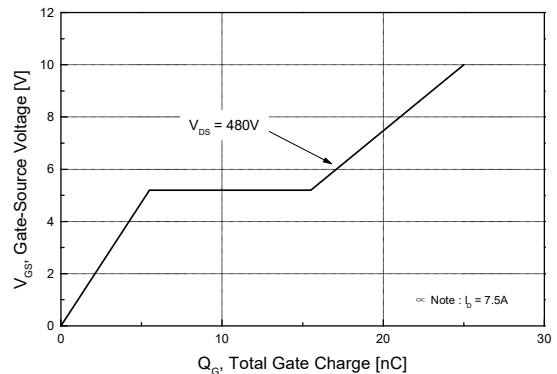


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

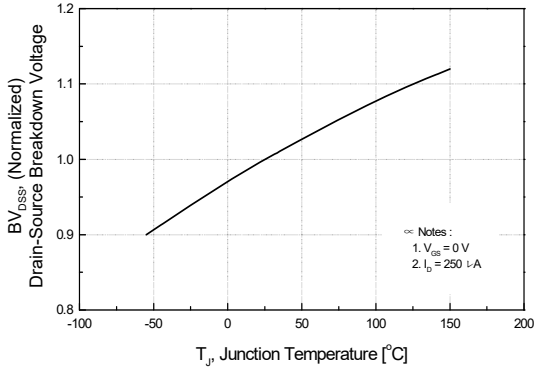


Figure 7. Breakdown Voltage Variation vs Temperature

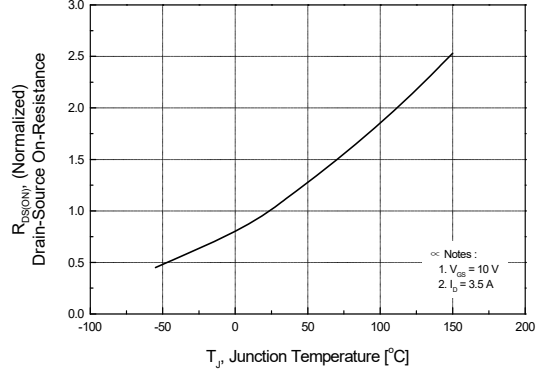


Figure 8. On-Resistance Variation vs Temperature

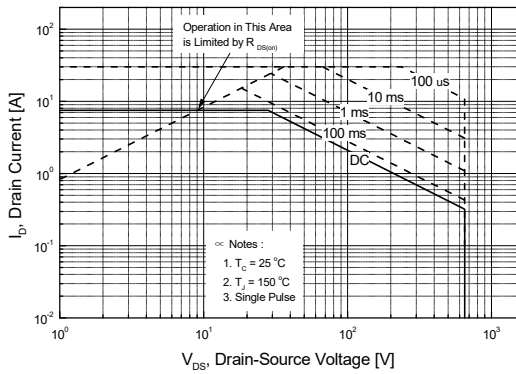


Figure 9-1. Maximum Safe Operating Area for SLP8N65C

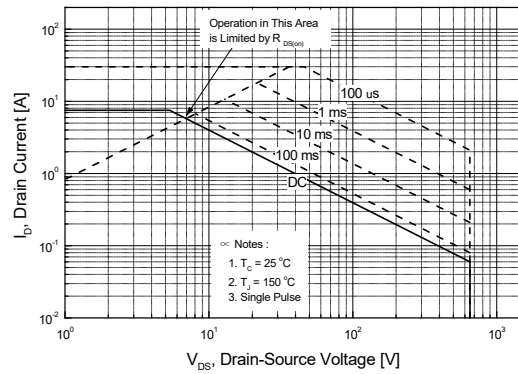


Figure 9-2. Maximum Safe Operating Area for SLF8N65C

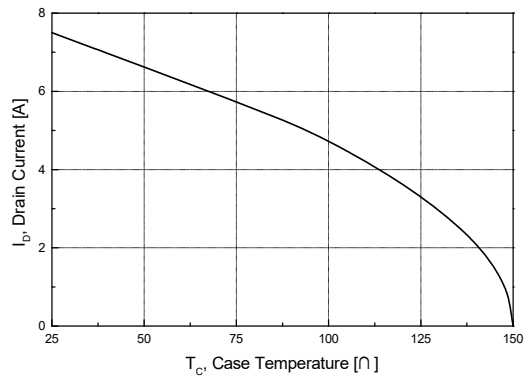


Figure 10. Maximum Drain Current vs Case Temperature

Typical Characteristics (Continued)

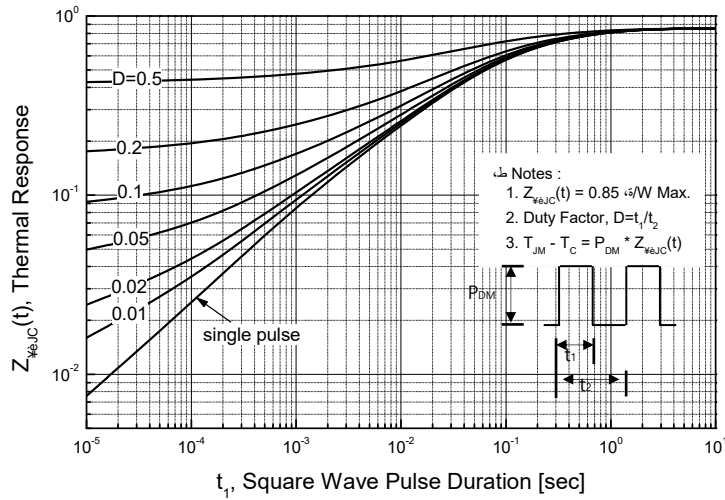


Figure 11-1. Transient Thermal Response Curve for SLP8N65C

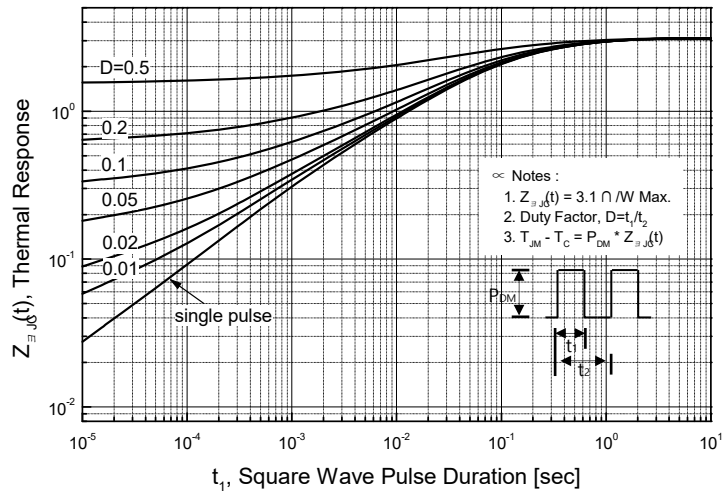
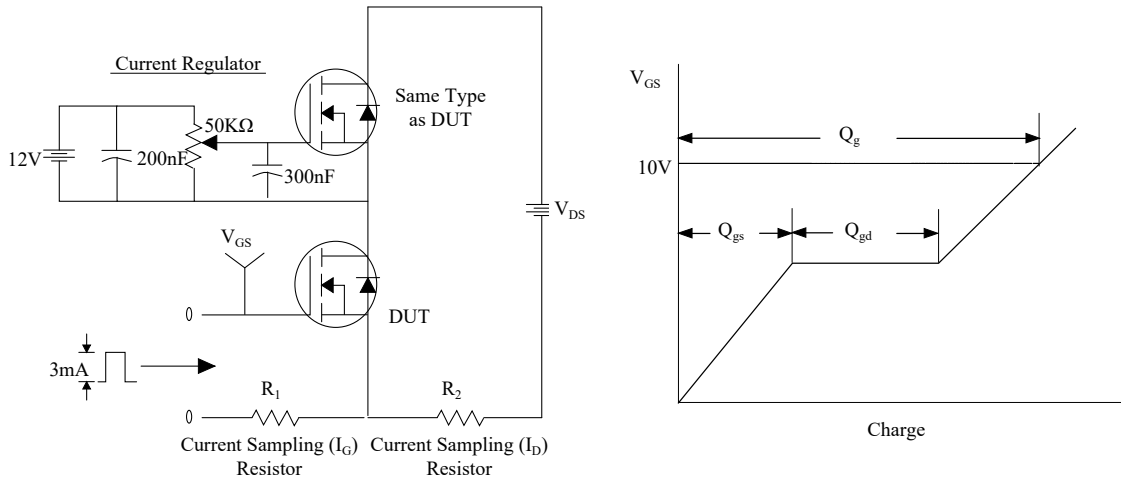
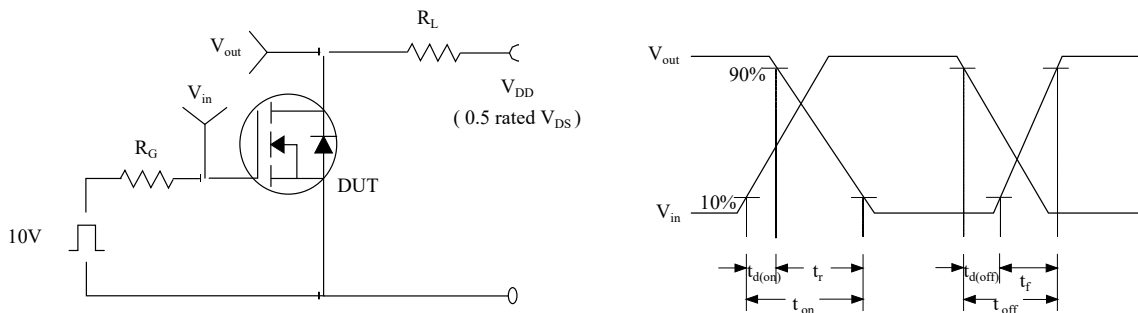


Figure 11-2. Transient Thermal Response Curve for SLF8N65C

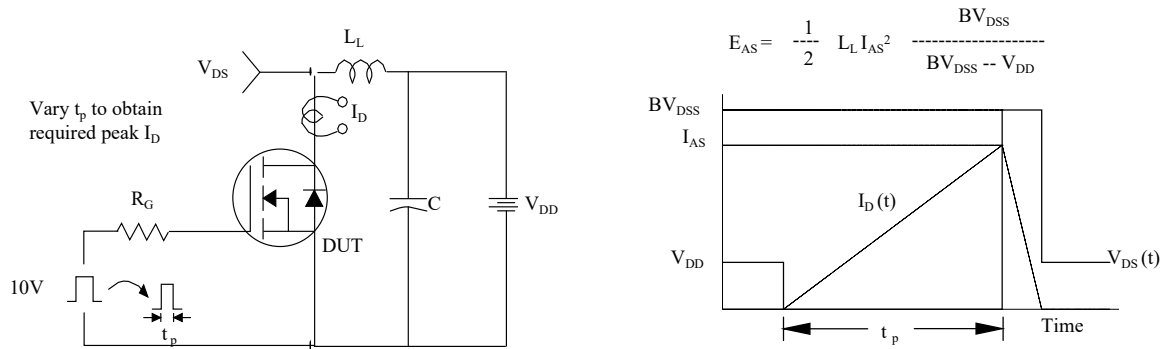
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

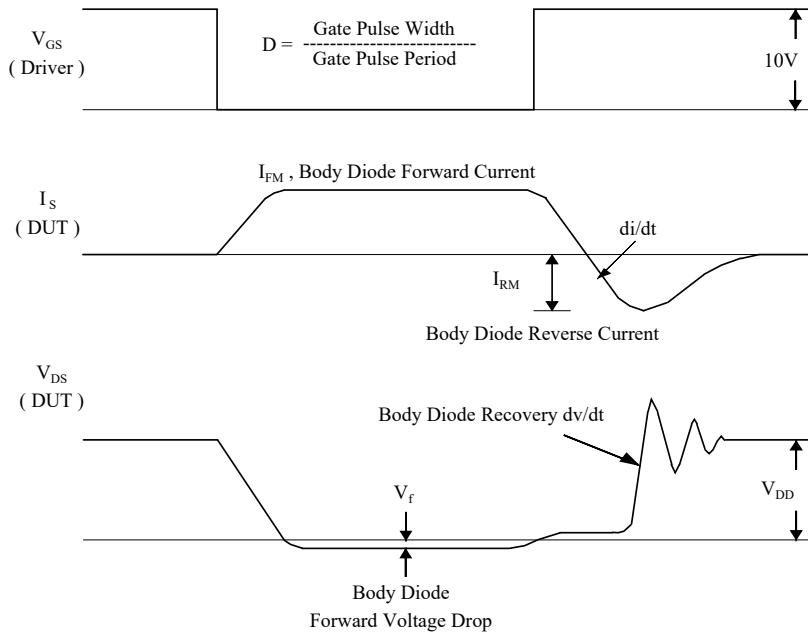
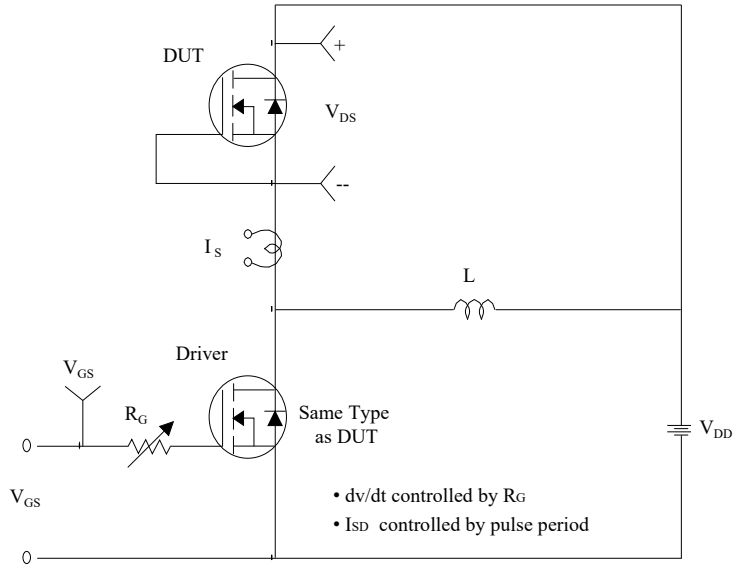


Unclamped Inductive Switching Test Circuit & Waveforms



$$E_{AS} = \frac{1}{2} L_L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

Peak Diode Recovery dv/dt Test Circuit & Waveforms



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