Marvell® Alaska® 88E1111

Integrated 10/100/1000 Ultra Gigabit Ethernet Transceiver

Datasheet

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PRODUCT OVERVIEW

The Alaska® Ultra 88E1111 Gigabit Ethernet Transceiver is a physical layer device for Ethernet 1000BASE-T, 100BASE-TX, and 10BASE-T applications. It is manufactured using standard digital CMOS process and contains all the active circuitry required to implement the physical layer functions to transmit and receive data on standard CAT 5 unshielded twisted pair.

The 88E1111 device incorporates the Marvell Virtual Cable Tester® (VCT™) feature, which uses Time Domain Reflectometry (TDR) technology for the remote identification of potential cable malfunctions, thus reducing equipment returns and service calls. Using VCT, the Alaska 88E1111 device detects and reports potential cabling issues such as pair swaps, pair polarity and excessive pair skew. The device will also detect cable opens, shorts or any impedance mismatch in the cable and report accurately within one meter the distance to the fault.

The 88E1111 device supports the Gigabit Media Independent Interface (GMII), Reduced GMII (RGMII), Serial Gigabit Media Independent Interface (SGMII), the Ten-Bit Interface (TBI), and Reduced TBI (RTBI) for direct connection to a MAC/Switch port.

The 88E1111 device incorporates an optional 1.25 GHz SERDES (Serializer/Deserializer). The serial interface may be connected directly to a fiber-optic transceiver for 1000BASE-T/1000BASE-X media conversion applications. Additionally, the 88E1111 device may be used to implement 1000BASE-T Gigabit Interface Converter (GBIC) or Small Form Factor Pluggable (SFP) modules.

The 88E1111 device uses advanced mixed-signal processing to perform equalization, echo and crosstalk cancellation, data recovery, and error correction at a gigabit per second data rate. The device achieves robust performance in noisy environments with very low power dissipation.

The 88E1111 device is offered in three different package options including a 117-Pin TFBGA, a 96-pin aQFN featuring a body size of only 9 x 9 mm, and a 128 PQFP package.

Features

- 10/100/1000BASE-T IEEE 802.3 compliant
- Supports GMII, TBI, reduced pin count GMII (RGMII), reduced pin count TBI (RTBI), and serial GMII (SGMII) interfaces
- Integrated 1.25 GHz SERDES for 1000BASE-X fiber applications
- Four RGMII timing modes
- Energy Detect and Energy Detect+ low power modes
- Three loopback modes for diagnostics
- "Downshift" mode for two-pair cable installations
- Fully integrated digital adaptive equalizers, echo cancellers, and crosstalk cancellers
- Advanced digital baseline wander correction
- Automatic MDI/MDIX crossover at all speeds of operation
- Automatic polarity correction
- IEEE 802.3u compliant Auto-Negotiation
- Software programmable LED modes including LED testing
- Automatic detection of fiber or copper operation
- Supports IEEE 1149.1 JTAG
- Two-Wire Serial Interface (TWSI) and MDC/MDIO
- CRC checker, packet counter
- Packet generation
- Virtual Cable Tester (VCT)

- Auto-Calibration for MAC Interface outputs
- Requires only two supplies: 2.5V and 1.0V (with 1.2V option for the 1.0V supply)
- I/Os are 3.3V tolerant
- Low power dissipation Pave = 0.75W
- 117-Pin TFBGA, 96-Pin aQFN, and 128 PQFP package options (NOTE: The 96-Pin BCC package is obsolete and is no longer available. The 96-Pin aQFN package is a pin compatible replacement for the 96-Pin BCC package. See Product Change Notification 1210066 and Table 186 for details.)
- 117-Pin TFBGA and 96-Pin aQFN packages available in Commercial or Industrial grade
- RoHS 6/6 compliant packages available

Figure 1: 88E1111 Device used in Copper Application

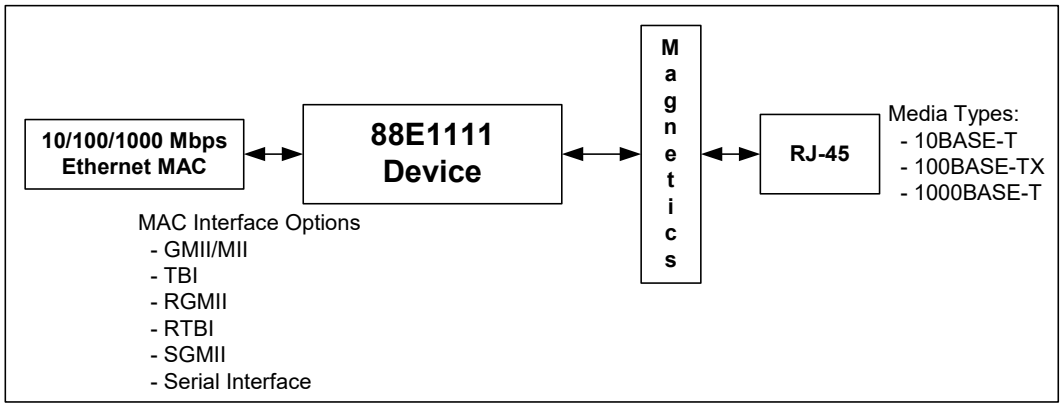


Figure 2: 88E1111 Device used in Fiber Application

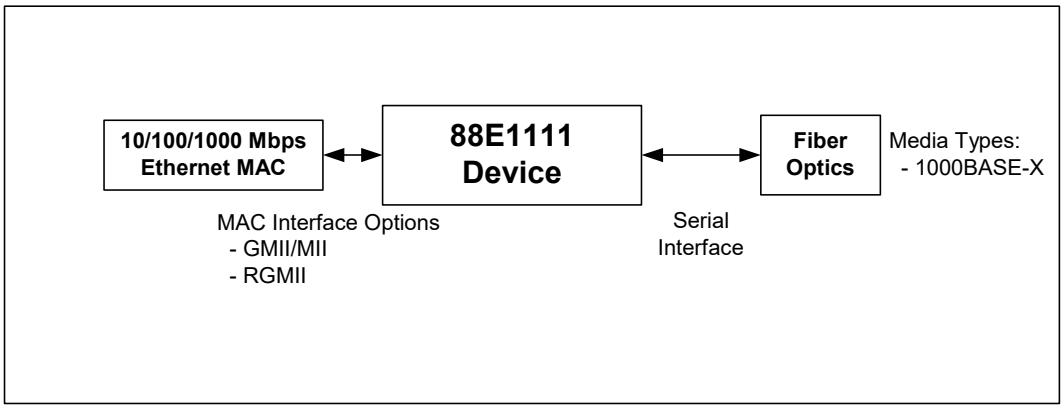
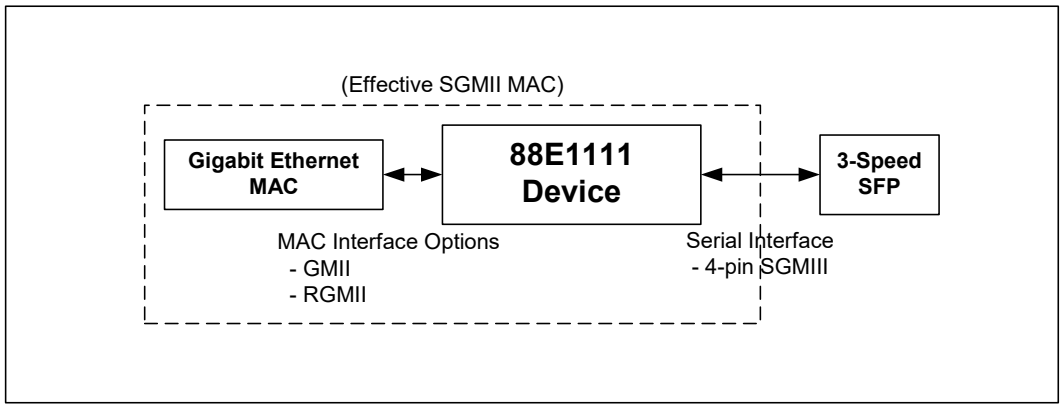


Figure 3: 88E1111 RGMII/GMII MAC to SGMII MAC Conversion



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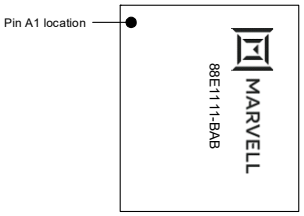
The 88E1111 device is a 10/100/1000BASE-T/1000BASE-X Gigabit Ethernet transceiver.

1.1 117-Pin TFBGA Package

Figure 4: 88E1111 Device 117-Pin TFBGA Package (Top View)

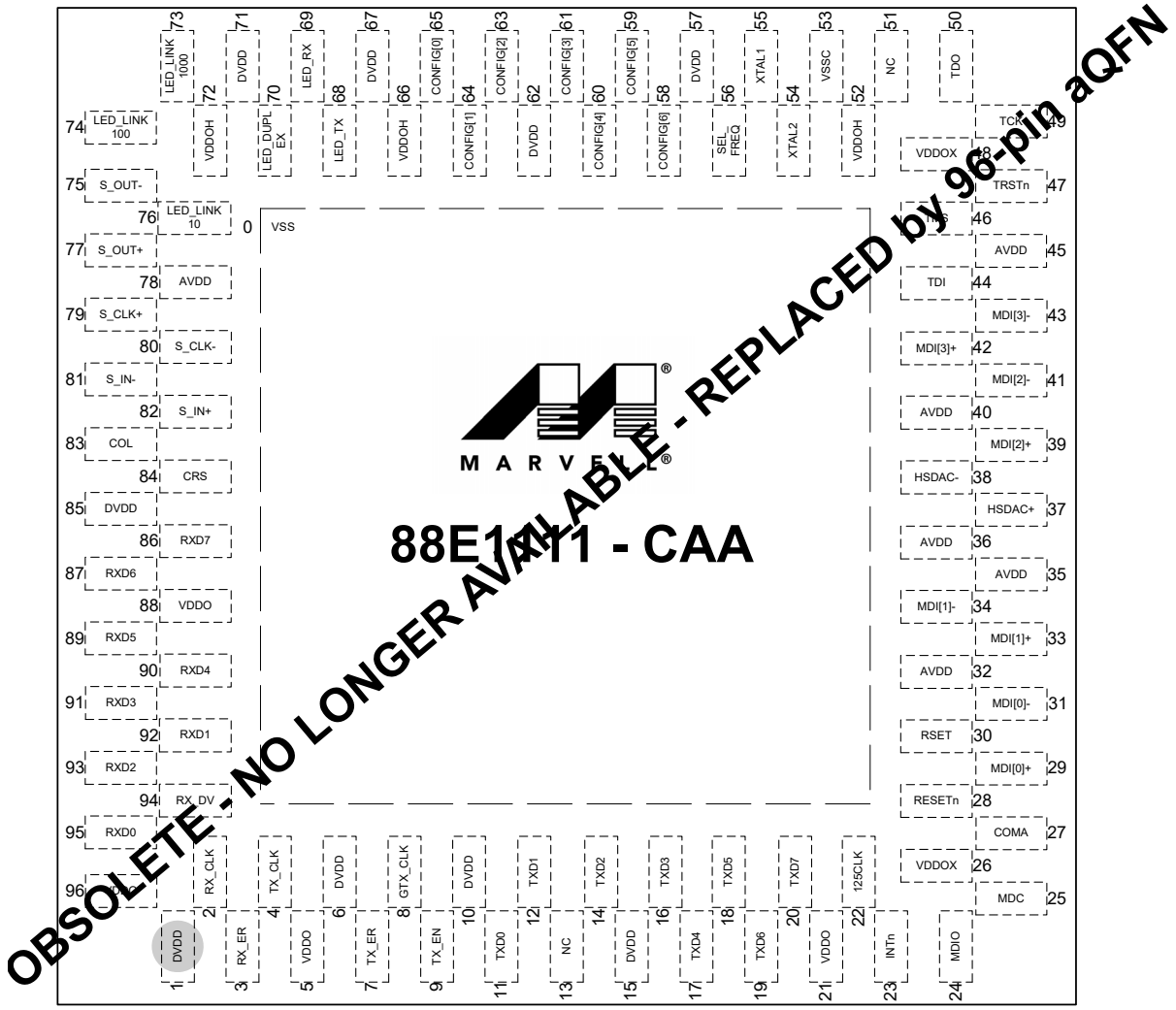
	1	2	3	4	5	6	7	8	9	
A	RXD5	RXD6	S_IN+	S_IN-	S_CLK+	S_CLK-	S_OUT+	S_OUT-	LED_ LINK1000	A
B	RX_DV	RXD0	RXD3	VDDO	CRS	COL	AVDD	LED_ LINK100	VDDOH	B
C	RX_CLK	VDDO	RXD2	RXD4	RXD7	DVDD	DVDD	LED_ LINK10	LED_RX	C
D	TX_CLK	RX_ER	RXD1	VSS	VSS	VSS	DVDD	CONFIG[0]	LED_TX	D
E	TX_EN	GTX_CLK	DVDD	VSS	VSS	VSS	DVDD	LED_ DUPLEX	CONFIG[1]	E
F	TXD0	TX_ER	DVDD	VSS	VSS	VSS	VDDOH	CONFIG[2]	CONFIG[4]	F
G	NC	TXD1	TXD2	VSS	VSS	VSS	CONFIG[3]	CONFIG[6]	CONFIG[5]	G
H	TXD4	TXD3	TXD5	VSS	VSS	VSS	VSSC	SEL_ FREQ	XTAL1	H
J	TXD6	TXD7	DVDD	VSS	VSS	VSS	DVDD	VDDOH	XTAL2	J
K	VDDO	125CLK	RESETn	VSS	VSS	VSS	NC	TDO	VDDOX	K
L	INTn	VDDOX	MDC	COMA	VSS	VSS	TDI	TMS	TCK	L
M	MDIO	RSET	AVDD	AVDD	HSDAC+	HSDAC-	AVDD	AVDD	TRSTn	M
N	MDI[0]+	MDI[0]-	MDI[1]+	MDI[1]-	AVDD	MDI[2]+	MDI[2]-	MDI[3]+	MDI[3]-	N
	1	2	3	4	5	6	7	8	9	

Figure 5: Pin A1 Location



1.2 96-Pin aQFN Package

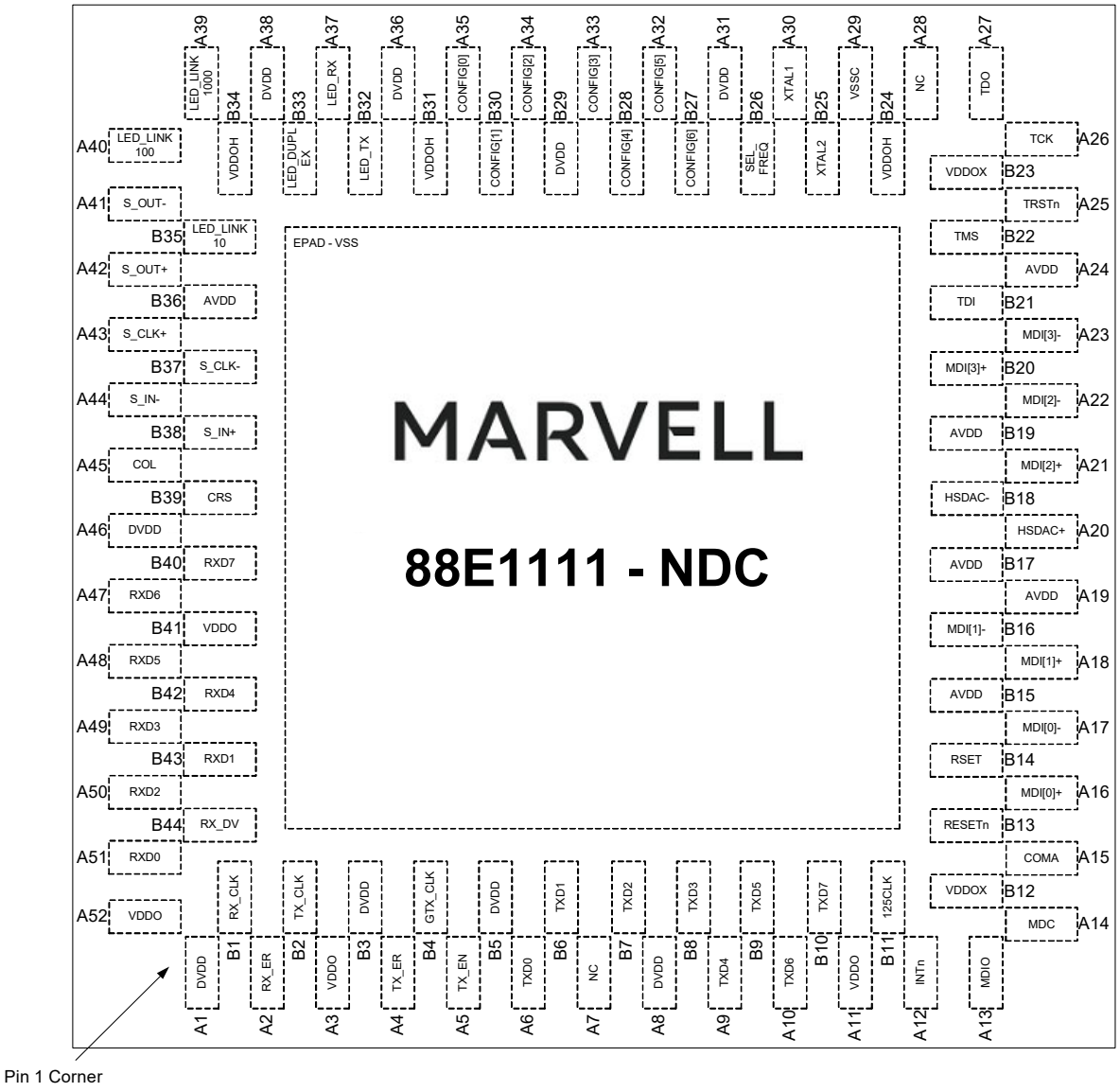
Figure 6: 88E1111 Device 96-Pin BCC Package (Top View) - (OBSOLETE - No Longer Available - Replaced by 96-Pin aQFN Package)



Note

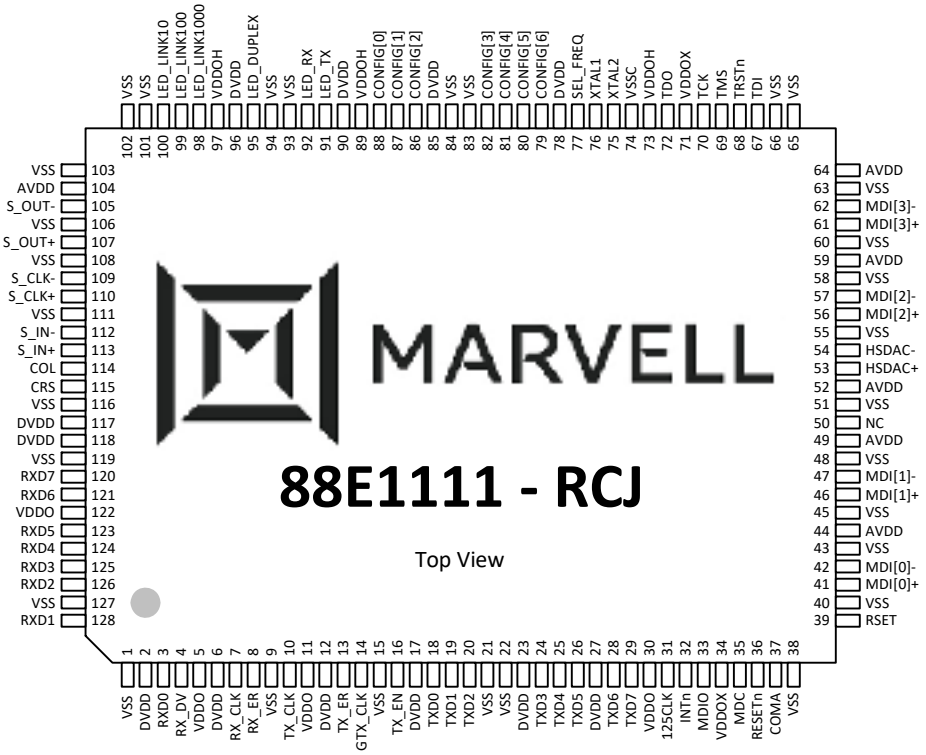
The 96-Pin aQFN package is a pin compatible replacement for the 96-Pin BCC package. See Product Change Notification 1210066 and Table 186 for details.

Figure 7: 88E1111 Device 96-Pin aQFN Package (Top View)



1.3 128-Pin PQFP Package

Figure 8: 88E1111 Device 128-Pin PQFP Package (Top View)



1.4 Pin Description

Table 1: Pin Type Definitions

Pin Type	Definition
H	Input with hysteresis
I/O	Input and output
I	Input only
O	Output only
PU	Internal pull-up
PD	Internal pull-down
D	Open drain output
Z	Tri-state output
mA	DC sink capability

Table 2: Media Dependent Interface

117-TFBGA Pin #	96-aQFN Pin #	128-PQFP Pin #	Pin Name	Pin Type	Description
N1 N2	A16 A17	41 42	MDI[0]+ MDI[0]-	I/O, D	Media Dependent Interface[0]. In 1000BASE-T mode in MDI configuration, MDI[0]± correspond to BI_DA±. In MDIX configuration, MDI[0]± correspond to BI_DB±. In 100BASE-TX and 10BASE-T modes in MDI configuration, MDI[0]± are used for the transmit pair. In MDIX configuration, MDI[0]± are used for the receive pair. MDI[0]± should be tied to ground if not used. See Section 2.17 "MDI/MDIX Crossover" on page 102.
N3 N4	A18 B16	46 47	MDI[1]+ MDI[1]-	I/O, D	Media Dependent Interface[1]. In 1000BASE-T mode in MDI configuration, MDI[1]± correspond to BI_DB±. In MDIX configuration, MDI[1]± correspond to BI_DA±. In 100BASE-TX and 10BASE-T modes in MDI configuration, MDI[1]± are used for the receive pair. In MDIX configuration, MDI[1]± are used for the transmit pair. MDI[1]± should be tied to ground if not used. See Section 2.17 "MDI/MDIX Crossover" on page 102.

Table 2: Media Dependent Interface (Continued)

117-TFBGA Pin #	96-aQFN Pin #	128-PQFP Pin #	Pin Name	Pin Type	Description
N6 N7	A21 A22	56 57	MDI[2]+ MDI[2]-	I/O, D	Media Dependent Interface[2]. In 1000BASE-T mode in MDI configuration, MDI[2]± correspond to BI_DC±. In MDIX configuration, MDI[2]± corresponds to BI_DD±. In 100BASE-TX and 10BASE-T modes, MDI[2]± are not used. MDI[2]± should be tied to ground if not used. See Section 2.17 "MDI/MDIX Crossover" on page 102.
N8 N9	B20 A23	61 62	MDI[3]+ MDI[3]-	I/O, D	Media Dependent Interface[3]. In 1000BASE-T mode in MDI configuration, MDI[3]± correspond to BI_DD±. In MDIX configuration, MDI[3]± correspond to BI_DC±. In 100BASE-TX and 10BASE-T modes, MDI[3]± are not used. MDI[3]± should be tied to ground if not used. See Section 2.17 "MDI/MDIX Crossover" on page 102.

The GMII interface supports both 1000BASE-T and 1000BASE-X modes of operation. The GMII interface pins are also used for the TBI interface. See Table 4 for TBI pin definitions. The MAC interface pins are 3.3V tolerant. See Section 4.5.1, “Digital Pins,” on page 193 for details.

Table 3: GMII/MII Interfaces

117-TFBGA Pin #	96-aQFN Pin #	128-PQFP Pin #	Pin Name	Pin Type	Description
E2	B4	14	GTX_CLK	I	GMII Transmit Clock. GTX_CLK provides a 125 MHz clock reference for TX_EN, TX_ER, and TXD[7:0]. This clock can be stopped when the device is in 10/100BASE-T modes, and also during Auto-Negotiation.
D1	B2	10	TX_CLK	O, Z	MII Transmit Clock. TX_CLK provides a 25 MHz clock reference for TX_EN, TX_ER, and TXD[3:0] in 100BASE-TX mode, and a 2.5 MHz clock reference in 10BASE-T mode. TX_CLK provides a 25 MHz, 2.5 MHz, or 0 MHz clock during 1000 Mbps Good Link, Auto-Negotiation, and Link Lost states depending on the setting of register 20.6:4. The 2.5 MHz clock is the default rate, which may be programmed to another frequency by writing to register 20.6:4.
E1	A5	16	TX_EN	I	GMII and MII Transmit Enable. In GMII/MII mode when TX_EN is asserted, data on TXD[7:0] along with TX_ER is encoded and transmitted onto the cable. TX_EN is synchronous to GTX_CLK, and synchronous to TX_CLK in 100BASE-TX and 10BASE-T modes.
F2	A4	13	TX_ER	I	GMII and MII Transmit Error. In GMII/MII mode when TX_ER and TX_EN are both asserted, the transmit error symbol is transmitted onto the cable. When TX_ER is asserted with TX_EN deasserted, carrier extension symbol is transmitted onto the cable. TX_ER is synchronous to GTX_CLK, and synchronous to TX_CLK in 100BASE-TX and 10BASE-T modes.

Table 3: GMII/MII Interfaces (Continued)

117-TFBGA Pin #	96-aQFN Pin #	128-PQFP Pin #	Pin Name	Pin Type	Description
J2 J1 H3 H1 H2 G3 G2 F1	B10 A10 B9 A9 B8 B7 B6 A6	29 28 26 25 24 20 19 18	TXD[7] TXD[6] TXD[5] TXD[4] TXD[3]/TXD[3] TXD[2]/TXD[2] TXD[1]/TXD[1] TXD[0]/TXD[0]	I	GMII and MII Transmit Data. In GMII mode, TXD[7:0] present the data byte to be transmitted onto the cable in 1000BASE-T mode. In MII mode, TXD[3:0] present the data nibble to be transmitted onto the cable in 100BASE-TX and 10BASE-T modes. TXD[7:4] are ignored in these modes, but should be driven either high or low. These pins must not float. TXD[7:0] are synchronous to GTX_CLK, and synchronous to TX_CLK in 100BASE-TX and 10BASE-T modes. Inputs TXD[7:4] should be tied low if not used (e.g., RGMII mode).
C1	B1	7	RX_CLK	O, Z	GMII and MII Receive Clock. RX_CLK provides a 125 MHz clock reference for RX_DV, RX_ER, and RXD[7:0] in 1000BASE-T mode, a 25 MHz clock reference in 100BASE-TX mode, and a 2.5 MHz clock reference in 10BASE-T mode. TX_TCLK comes from the RX_CLK pins used in jitter testing. Refer to Register 9 for jitter test modes.
B1	B44	4	RX_DV	O, Z	GMII and MII Receive Data Valid. When RX_DV is asserted, data received on the cable is decoded and presented on RXD[7:0] and RX_ER. RX_DV is synchronous to RX_CLK.
D2	A2	8	RX_ER	O, Z	GMII and MII Receive Error. When RX_ER and RX_DV are both asserted, the signals indicate an error symbol is detected on the cable. When RX_ER is asserted with RX_DV de-asserted, a false carrier or carrier extension symbol is detected on the cable. RX_ER is synchronous to RX_CLK.
C5 A2 A1 C4 B3 C3 D3 B2	B40 A47 A48 B42 A49 A50 B43 A51	120 121 123 124 125 126 128 3	RXD[7] RXD[6] RXD[5] RXD[4] RXD[3]/RXD[3] RXD[2]/RXD[2] RXD[1]/RXD[1] RXD[0]/RXD[0]	O, Z	GMII and MII Receive Data. Symbols received on the cable are decoded and presented on RXD[7:0] in 1000BASE-T mode. In MII mode, RXD[3:0] are used in 100BASE-TX and 10BASE-T modes. In MII mode, RXD[7:4] are driven low. RXD[7:0] is synchronous to RX_CLK.

Table 3: GMII/MII Interfaces (Continued)

117-TFBGA Pin #	96-aQFN Pin #	128-PQFP Pin #	Pin Name	Pin Type	Description
B5	B39	115	CRS	O, Z	GMII and MII Carrier Sense. CRS asserts when the receive medium is non-idle. In half-duplex mode, CRS is also asserted during transmission. CRS assertion during half-duplex transmit can be disabled by programming register 16.11 to 0. CRS is asynchronous to RX_CLK, GTX_CLK, and TX_CLK.
B6	A45	114	COL	O, Z	GMII and MII Collision. In 10/100/1000BASE-T full-duplex modes, COL is always low. In 10/100/1000BASE-T half-duplex modes, COL asserts only when both the transmit and receive media are non-idle. In 10BASE-T half-duplex mode, COL is asserted to indicate signal quality error (SQE). SQE can be disabled by clearing register 16.2 to zero. COL is asynchronous to RX_CLK, GTX_CLK, and TX_CLK.

The TBI interface supports 1000BASE-T mode of operation. The TBI interface uses the same pins as the GMII interface. The MAC interface pins are 3.3V tolerant. See “Digital Pins” on page 193 for details.

Table 4: TBI Interface

117-TFBGA Pin #	96-aQFN Pin #	128-PQFP Pin #	Pin Name	Pin Type	Description
E2	B4	14	GTX_CLK/ TBI_TXCLK	I	TBI Transmit Clock. In TBI mode, GTX_CLK is used as TBI_TXCLK. TBI_TXCLK is a 125 MHz transmit clock. TBI_TXCLK provides a 125 MHz clock reference for TX_EN, TX_ER, and TXD[7:0].
D1	B2	10	TX_CLK/RCLK1	O, Z	TBI 62.5 MHz Receive Clock- even code group. In TBI mode, TX_CLK is used as RCLK1.
J2 J1 H3 H1 H2 G3 G2 F1	B10 A10 B9 A9 B8 B7 B6 A6	29 28 26 25 24 20 19 18	TXD[7] TXD[6] TXD[5] TXD[4] TXD[3] TXD[2] TXD[1] TXD[0]	I	TBI Transmit Data. TXD[7:0] presents the data byte to be transmitted onto the cable. TXD[9:0] are synchronous to GTX_CLK. Inputs TXD[7:4] should be tied low if not used (e.g., RTBI mode).
E1	A5	16	TX_EN/ TXD8	I	TBI Transmit Data. In TBI mode, TX_EN is used as TXD8. TXD[9:0] are synchronous to GTX_CLK.
F2	A4	13	TX_ER/ TXD9	I	TBI Transmit Data. In TBI mode, TX_ER is used as TXD9. TXD[9:0] are synchronous to GTX_CLK. TX_ER should be tied low if not used (e.g., RTBI mode).
C1	B1	7	RX_CLK/ RCLK0	O, Z	TBI 62.5 MHz Receive Clock- odd code group. In the TBI mode, RX_CLK is used as RCLK0.
C5 A2 A1 C4 B3 C3 D3 B2	B40 A47 A48 B42 A49 A50 B43 A51	120 121 123 124 125 126 128 3	RXD[7] RXD[6] RXD[5] RXD[4] RXD[3] RXD[2] RXD[1] RXD[0]	O, Z	TBI Receive Data code group [7:0]. In the TBI mode, RXD[7:0] present the data byte to be transmitted to the MAC. Symbols received on the cable are decoded and presented on RXD[7:0]. RXD[7:0] are synchronous to RCLK0 and RCLK1.
B1	B44	4	RX_DV/ RXD8	O, Z	TBI Receive Data code group bit 8. In the TBI mode, RX_DV is used as RXD8. RXD[9:0] are synchronous to RCLK0 and RCLK1.
D2	A2	8	RX_ER/ RXD9	O, Z	TBI Receive Data code group bit 9. In the TBI mode, RX_ER is used as RXD9. RXD[9:0] are synchronous to RCLK0 and RCLK1.

Table 4: TBI Interface (Continued)

117-TFBGA Pin #	96-aQFN Pin #	128-PQFP Pin #	Pin Name	Pin Type	Description
B5	B39	115	CRS/ COMMA	O, Z	TBI Valid Comma Detect. In the TBI mode, CRS is used as COMMA.
B6	A45	114	COL/LPBK	I	TBI Mode Loopback. In the TBI mode, COL is used to indicate loopback on the TBI. When a "0 - 1" transition is sampled on this pin, bit 0.14 is set to 1. When a "1 - 0" is sampled on this pin, bit 0.14 is reset to 0. If this feature is not used, the COL pin should be driven low on the board. This pin should not be left floating in TBI mode.

The RGMII interface supports 10/100/1000BASE-T and 1000BASE-X modes of operation.The RGMII interface pins are also used for the RTBI interface. See Table 6 for RTBI pin definitions. The MAC interface pins are 3.3V tolerant. See"Digital Pins" on page 193 for details.

Table 5: RGMII Interface

117-TFBGA Pin #	96-aQFN Pin #	128-PQFP Pin #	Pin Name	Pin Type	Description
E2	B4	14	GTX_CLK/ TXC	I	RGMII Transmit Clock provides a 125 MHz, 25 MHz, or 2.5 MHz reference clock with ± 50 ppm tolerance depending on speed. In RGMII mode, GTX_CLK is used as TXC.
H2 G3 G2 F1	B8 B7 B6 A6	24 20 19 18	TXD[3]/TD[3] TXD[2]/TD[2] TXD[1]/TD[1] TXD[0]/TD[0]	I	RGMII Transmit Data. In RGMII mode, TXD[3:0] are used as TD[3:0]. In RGMII mode, TXD[3:0] run at double data rate with bits [3:0] presented on the rising edge of GTX_CLK, and bits [7:4] presented on the falling edge of GTX_CLK. In this mode, TXD[7:4] are ignored. In RGMII 10/100BASE-T modes, the transmit data nibble is presented on TXD[3:0] on the rising edge of GTX_CLK.
E1	A5	16	TX_EN/ TX_CTL	I	RGMII Transmit Control. In RGMII mode, TX_EN is used as TX_CTL. TX_EN is presented on the rising edge of GTX_CLK. A logical derivative of TX_EN and TX_ER is presented on the falling edge of GTX_CLK.
C1	B1	7	RX_CLK/ RXC	O, Z	RGMII Receive Clock provides a 125 MHz, 25 MHz, or 2.5 MHz reference clock with ± 50 ppm tolerance derived from the received data stream depending on speed. In RGMII mode, RX_CLK is used as RXC.
B1	B44	4	RX_DV/ RX_CTL	O, Z	RGMII Receive Control. In RGMII mode, RX_DV is used as RX_CTL. RX_DV is presented on the rising edge of RX_CLK. A logical derivative of RX_DV and RX_ER is presented on the falling edge of RX_CLK.
B3 C3 D3 B2	A49 A50 B43 A51	125 126 128 3	RXD[3]/RD[3] RXD[2]/RD[2] RXD[1]/RD[1] RXD[0]/RD[0]	O, Z	RGMII Receive Data. In RGMII mode, RXD[3:0] are used as RD[3:0]. In RGMII mode, RXD[3:0] run at double data rate with bits [3:0] presented on the rising edge of RX_CLK, and bits [7:4] presented on the falling edge of RX_CLK. In this mode, RXD[7:4] are ignored. In RGMII 10/100BASE-T modes, the receive data nibble is presented on RXD[3:0] on the rising edge of RX_CLK. RXD[3:0] are synchronous to RX_CLK.

The RTBI interface supports 1000BASE-T mode of operation. The RTBI interface uses the same pins as the RGMII interface. The MAC interface pins are 3.3V tolerant. See "Digital Pins" on page 193 for details.

Table 6: RTBI Interface

117-TFBGA Pin #	96-aQFN Pin #	128-PQFP Pin #	Pin Name	Pin Type	Description
E2	B4	14	GTX_CLK/ TXC	I	RGMII Transmit Clock provides a 125 MHz reference clock with ± 50 ppm tolerance. In RTBI mode, GTX_CLK is used as TXC.
H2 G3 G2 F1	B8 B7 B6 A6	24 20 19 18	TXD[3]/TD[3] TXD[2]/TD[2] TXD[1]/TD[1] TXD[0]/TD[0]	I	RTBI Transmit Data. In RTBI mode, TXD[3:0] are used as TD[3:0]. TD[3:0] run at double data rate with bits [3:0] presented on the rising edge of GTX_CLK, and bits [8:5] presented on the falling edge of GTX_CLK. In this mode, TXD[7:4] are ignored.
E1	A5	16	TX_EN/ TD4_TD9	I	RTBI Transmit Data. In RTBI mode, TX_EN is used as TD4_TD9. TD4_TD9 runs at a double data rate with bit 4 presented on the rising edge of GTX_CLK, and bit 9 presented on the falling edge of GTX_CLK.
C1	B1	7	RX_CLK/ RXC	O, Z	RTBI Receive Clock provides a 125 MHz reference clock with ± 50 ppm tolerance derived from the received data stream. In RTBI mode, RX_CLK is used as RXC.
B3 C3 D3 B2	91 A50 B43 A51	125 126 128 3	RXD[3]/RD[3] RXD[2]/RD[2] RXD[1]/RD[1] RXD[0]/RD[0]	O, Z	RTBI Receive Data. In RTBI mode, RXD[3:0] are used as RD[3:0]. RD[3:0] runs at double data rate with bits [3:0] presented on the rising edge of RX_CLK, and bits [8:5] presented on the falling edge of RX_CLK. In this mode, RXD[7:4] are ignored.
B1	B44	4	RX_DV/ RD4_RD9	O, Z	RTBI Receive Data. In RTBI mode, RX_DV is used as RD4_RD9. RD4_RD9 runs at a double data rate with bit 4 presented on the rising edge of RX_CLK, and bit 9 presented on the falling edge of RX_CLK.

Table 7: SGMII Interface

117-TFBGA Pin #	96-aQFN Pin #	128-PQFP Pin #	Pin Name	Pin Type	Description
A3 A4	B38 A44	113 112	S_IN+ S_IN-	I	SGMII Transmit Data. 1.25 GBaud input - Positive and Negative. Input impedance on the S_IN± pins may be programmed for 50 ohm or 75 ohm impedance by setting register 26.6. The input impedance default setting is determined by the 75/50 OHM configuration pin. See Section 2.4 "Hardware Configuration" on page 68.
A5 A6	A43 B37	110 109	S_CLK+ S_CLK-	I/O	SGMII 625 MHz Receive Clock. For Serial Interface modes (HWCFG_MODE[3:0] = 1x00) the S_CLK± pins become Signal Detect± (SD±) inputs.
A7 A8	A42 A41	107 105	S_OUT+ S_OUT-	O, Z	SGMII Receive Data. 1.25 GBaud output - Positive and Negative. Output impedance on the S_OUT± pins may be programmed for 50 ohm or 75 ohm impedance by setting register 26.5. Output amplitude can be adjusted via register 26.2:0. The output impedance default setting is determined by the 75/50 OHM configuration pin. See Section 2.4 "Hardware Configuration" on page 68.

Table 8: 1.25 GHz Serial High Speed Interface

117-TFBGA Pin #	96-aQFN Pin #	128-PQFP Pin #	Pin Name	Pin Type	Description
A3 A4	B38 A44	113 112	S_IN+ S_IN-	I	1.25 GHz input - Positive and Negative. When this interface is used as a MAC interface, the MAC transmitter's positive output connects to the S_IN+. The MAC transmitter's negative output connects to the S_IN-. When this interface is used as a fiber interface, the fiber-optic transceiver's positive output connects to the S_IN+. The fiber-optic transceiver's negative output connects to the S_IN-. Input impedance on the S_IN± pins may be programmed for 50 ohm or 75 ohm impedance by setting register 26.6. The input impedance default setting is determined by the 75/50 OHM configuration pin. See Section 2.4 "Hardware Configuration" on page 68.
A5 A6	A43 B37	110 109	S_CLK+/SD+ S_CLK-/SD-	I	Signal Detect input. For Serial Interface modes the S_CLK± pins become Signal Detect± (SD±) inputs.
A7 A8	A42 A41	107 105	S_OUT+ S_OUT-	O, Z	1.25 GHz output – Positive and Negative. When this interface is used as a MAC interface, S_OUT+ connects to the MAC receiver's positive input. S_OUT- connects to the MAC receiver's negative input. When this interface is used as a fiber interface, S_OUT+ connects to the fiber-optic transceiver's positive input. S_OUT- connects to the fiber-optic transceiver's negative input. Output impedance on the S_OUT± pins may be programmed for 50 ohm or 75 ohm impedance by setting register 26.5. Output amplitude can be adjusted via register 26.2:0. The output impedance default setting is determined by the 75/50 OHM configuration pin. See Section 2.4 "Hardware Configuration" on page 68.
B3	A49	125	RXD[3]	O, Z	Serial MAC interface Copper Link Status[1] connection. 1 = Copper link up 0 = Copper link down See "Serial MAC Interface" on page 61 for details.

Table 8: 1.25 GHz Serial High Speed Interface (Continued)

117-TFBGA Pin #	96-aQFN Pin #	128-PQFP Pin #	Pin Name	Pin Type	Description
C3	A50	126	RXD[2]	O, Z	Serial MAC interface Copper Link Status[0] connection. 1 = Copper link down 0 = Copper link up See “Serial MAC Interface” on page 61 for details.
D3	B43	128	RXD[1]	O, Z	Serial MAC interface PHY_SIGDET[1] connection. 1 = S_OUT± valid code groups according to clause 36. 0 = S_OUT± invalid See “Serial MAC Interface” on page 61 for details.
B2	A51	3	RXD[0]	O, Z	Serial MAC interface PHY_SIGDET[0] connection. 1 = S_OUT± invalid 0 = S_OUT± valid code groups according to clause 36 See “Serial MAC Interface” on page 61 for details.

Table 9: Management Interface and Interrupt

117-TFBGA Pin #	96-aQFN Pin #	128-PQFP Pin #	Pin Name	Pin Type	Description
L3	A14	35	MDC	I 3.3V Tolerant	MDC is the management data clock reference for the serial management interface. A continuous clock stream is not expected. The maximum frequency supported is 8.3 MHz.
M1	A13	33	MDIO	I/O 3.3V Tolerant	MDIO is the management data. MDIO transfers management data in and out of the device synchronously to MDC. This pin requires a pull-up resistor in a range from 1.5 kohm to 10 kohm.
L1	A12	32	INTn	D	The polarity of the INTn pin may be programmed at hardware reset by setting the INT_POL bit. Polarity: 0 = Active High 1 = Active Low See Section 2.4 "Hardware Configuration" on page 68. See Section 2.9.3 "Programming Interrupts" on page 83.

Table 10: Two-Wire Serial Interface

117-TFBGA Pin #	96-aQFN Pin #	128-PQFP Pin #	Pin Name	Pin Type	Description
L3	A14	35	MDC/SCL	I	Two-Wire Serial Interface (TWSI) serial clock line. When the 88E1111 device is connected to the bus, MDC connects to the serial clock line (SCL). Data is input on the rising edge of SCL, and output on the falling edge. See Section 2.10 "Two-wire Serial Interface" on page 84.
M1	A13	33	MDIO/SDA	I/O	TWSI serial data line. When the 88E1111 device is connected to the bus, MDIO connects to the serial data line (SDA). This pin is open-drain and may be wire-ORed with any number of open-drain devices. See Section 2.10 "Two-wire Serial Interface" on page 84.

Table 11: JTAG Interface

117-TFBGA Pin #	96-aQFN Pin #	128-PQFP Pin #	Pin Type	Pin Name	Description
L7	B21	67	TDI	I, PU	Boundary scan test data input. TDI contains an internal 150 kohm pull-up resistor.
L8	B22	69	TMS	I, PU	Boundary scan test mode select input. TMS contains an internal 150 kohm pull-up resistor.
L9	A26	70	TCK	I, PU	Boundary scan test clock input. TCK contains an internal 150 kohm pull-up resistor.
M9	A25	68	TRSTn	I, PU	Boundary scan test reset input. Active low. TRSTn contains an internal 150 kohm pull-up resistor as per the 1149.1 specification. After power up, the JTAG state machine should be reset by applying a low signal on this pin, or by keeping TMS high and applying 5 TCK pulses, or by pulling this pin low by a 4.7 kohm resistor.
K8	A27	72	TDO	O, Z	Boundary scan test data output.

Table 12: Clock/Configuration/Reset/I/O

117-TFBGA Pin #	96-aQFN Pin #	128-PQFP Pin #	Pin Name	Pin Type	Description
K2	B11	31	125CLK	O	Clock 125. A generic 125 MHz clock reference generated for use on the MAC device. This output can be disabled via DIS_125 through the CONFIG[3] pin.
D8	A35	88	CONFIG[0]	I	CONFIG[0] pin configures PHY_ADR[2:0] bits of the physical address. Each LED pin is hardwired to a constant value. The values associated to the CONFIG[0] pin are latched at the de-assertion of hardware reset. CONFIG[0] pin must be tied to one of the pins shown in Table 32 based on the configuration options selected. They should not be left floating. For the Two-Wire Serial Interface (TWSI) device address, the lower 5 bits, which are PHYADR[4:0], are latched during hardware reset, and the device address bits [6:5] are fixed at ‘10’. See Section 2.4 "Hardware Configuration" on page 68.
E9	B30	87	CONFIG[1]	I	CONFIG[1] pin configures PHY_ADR[4:3] and ENA_PAUSE options. Each LED pin is hardwired to a constant value. The values associated to the CONFIG[1] pin are latched at the de-assertion of hardware reset. CONFIG[1] pin must be tied to one of the pins shown in Table 32 based on the configuration options selected. They should not be left floating. For the TWSI device address, the lower 5 bits, which are PHYADR[4:0], are latched during hardware reset, and the device address bits [6:5] are fixed at ‘10’. See Section 2.4 "Hardware Configuration" on page 68.
F8	A34	86	CONFIG[2]	I	CONFIG[2] pin configures ANEG[3:1] bits. Each LED pin is hardwired to a constant value. The values associated to the CONFIG[2] pin are latched at the de-assertion of hardware reset. CONFIG[2] pin must be tied to one of the pins shown in Table 32 based on the configuration options selected. They should not be left floating. See Section 2.4 "Hardware Configuration" on page 68.

Table 12: Clock/Configuration/Reset/I/O (Continued)

117-TFBGA Pin #	96-aQFN Pin #	128-PQFP Pin #	Pin Name	Pin Type	Description
G7	A33	82	CONFIG[3]	I	CONFIG[3] pin configures ANEG[0], ENA_XC, and DIS_125 options. Each LED pin is hardwired to a constant value. The values associated to the CONFIG[3] pin are latched at the de-assertion of hardware reset. CONFIG[3] pin must be tied to one of the pins shown in Table 32 based on the configuration options selected. They should not be left floating. See Section 2.4 "Hardware Configuration" on page 68.
F9	B28	81	CONFIG[4]	I	CONFIG[4] pin configures HWCFG_MODE[2:0] options. See Section 2.4 "Hardware Configuration" on page 68.
G9	A32	80	CONFIG[5]	I	CONFIG[5] pin configures DIS_FC, DIS_SLEEP, and HWCFG_MODE[3] options. See Section 2.4 "Hardware Configuration" on page 68.
G8	B27	79	CONFIG[6]	I	CONFIG[6] pin configures SEL_TWSI, INT_POL, and 75/50 OHM options. See Section 2.4 "Hardware Configuration" on page 68.
H8	B26	77	SEL_FREQ		Frequency Selection for XTAL1 input NC = Selects 25 MHz clock input. Tied low = Selects 125 MHz clock input. Internally divided to 25 MHz. SEL_FREQ is internally pulled up.
H9	A30	76	XTAL1	I	Reference Clock. 25 MHz ± 50 ppm or 125 MHz ± 50 ppm oscillator input. PLL clocks are not recommended, see "XTAL1 Input Clock Timing" on page 204 for details.
J9	B25	75	XTAL2	0	Reference Clock. 25 MHz ± 50 ppm tolerance crystal reference. When the XTAL2 pin is not connected, it should be left floating. There is no option for a 125 MHz crystal. See "Crystal Oscillator" Application Note for details.

Table 12: Clock/Configuration/Reset/I/O (Continued)

117-TFBGA Pin #	96-aQFN Pin #	128-PQFP Pin #	Pin Name	Pin Type	Description
K3	B13	36	RESETn	I	Hardware reset. Active low. XTAL1 must be active for a minimum of 10 clock cycles before the rising edge of RESETn. RESETn must be pulled high for normal operation.
L4	A15	37	COMA	I	COMA disables all active circuitry to draw absolute minimum power. The COMA power mode can be activated by asserting high on the COMA pin. To deactivate the COMA power mode, tie the COMA pin low. Upon deactivating COMA mode, the 88E1111 device will continue normal operation. The COMA power mode cannot be enabled as long as hardware reset is enabled. In COMA mode, the PHY cannot wake up on its own by detecting activity on the CAT 5 cable.

Table 13: Test

117-TFBGA Pin #	96-aQFN Pin #	128-PQFP Pin #	Pin Name	Pin Type	Description
M5 M6	A20 B18	53 54	HSDAC+ HSDAC-	Analog PD	Test pins. These pins should be left floating but brought out for probing.

Table 14: Control and Reference

117-TFBGA Pin #	96-aQFN Pin #	128-PQFP Pin #	Pin Name	Pin Type	Description
M2	B14	39	RSET	Analog I	Constant voltage reference. External 5.0 kohm 1% resistor connection to VSS required for each pin.

Table 15: Power & Ground

117-TFBGA Pin #	96-aQFN Pin #	128-PQFP Pin #	Pin Name	Pin Type	Description
B7 M3 M4 M7 M8 N5	B15 A19 B17 B19 A24 B36	44 49 52 59 64 104	AVDD	Power	Analog Power. 2.5V.
C6 C7 D7 E3 E7 F3 J3 J7	A1 B3 B5 A8 A31 B29 A36 A38 A46	2 6 12 17 23 27 78 85 90 96 117 118	DVDD	Power	Digital Power. 1.0V (Instead of 1.0V, 1.2V can be used).
B9 F7 J8	B24 B31 B34	73 89 97	VDDOH	Power	2.5V Power Supply for LED and CONFIG pins.
K9 L2	B12 B23	34 71	VDDOX	Power	2.5V Supply for the MDC/MDIO, INTn, 125CLK, RESETn, JTAG pin Power.
B4 C2 K1	A3 A11 B41 A52	5 11 30 122	VDDO	Power	2.5V I/O supply for the MAC interface pins.

Table 15: Power & Ground (Continued)

117-TFBGA Pin #	96-aQFN Pin #	128-PQFP Pin #	Pin Name	Pin Type	Description
D4 D5 D6 E4 E5 E6 F4 F5 F6 G4 G5 G6 H4 H5 H6 J4 J5 J6 K4 K5 K6 L5 L6	EPAD	1 9 15 21 22 38 40 43 45 48 51 55 58 60 63 65 66 83 84 93 94 101 102 103 106 108 111 116 119 127	VSS	GND	Global ground
H7	A29	74	VSSC	GND	Ground reference for XTAL1 and XTAL2 pins. This pin must be connected to the ground.
G1 K7	A7 A28	50	NC	NC	No connect. Do not connect these pins to anything

1.5 I/O State at Various Test or Reset Modes

Table 16: I/O State at Various Test or Reset Modes

Pin(s)	Isolate	Loopback or Normal operation	Software Reset	Hardware Reset	Power Down	Coma	Power Down and Isolate
MDI[3:0]±	Active	Active	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state
TX_CLK	Tri-state	Active	Reg. 16.3 state 0 = Low 1 = Active	Low	Reg. 16.3 state 0 = Low 1 = Active	Reg. 16.3 state 0 = Low 0 = Static but can be either high or low	Tri-state
RXD[0], RXD[2]	Tri-state	Active	High	High	High	High	Tri-state
RXD[7:3,1], RX_DV, RX_ER, CRS	Tri-state	Active	Low	Low	Low	Low	Tri-state
COL	Tri-state	TBI mode - input else -active	Tri-state	Tri-state	TBI mode - input else - low	TBI mode - input else - low	Tri-state
RX_CLK	Tri-state	Active	Reg. 16.3 state 0 = Low 1 = Active	Low	Reg. 16.3 state 0 = Low 1 = Active	Reg. 16.3 state 0 = Low 0 = Static but can be either high or low	Tri-state
S_CLK± S_OUT±	Active	Active	Tri-state	Tri-state	Reg. 16.3 state 0 = Tri-state 1 = Active	Tri-state	Active
MDIO	Active	Active	Active	Tri-state	Active	Tri-state	Active
INT	Active	Active	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state
LED_***	Active	Active	High	High	High	High	High
TDO	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state	Active	Tri-state
125CLK	Reg. 16.4 state 0 = Toggle 1 = Low	Reg. 16.4 state 0 = Toggle 1 = Low	Reg. 16.4 state 0 = Toggle 1 = Low	Toggle	Reg. 16.4 state 0 = Toggle 1 = Low	Reg. 16.3 state 0 = Static but can be either high or low 0 = Low	Reg. 16.4 state 0 = Toggle 1 = Low

1.6 117-Pin TFBGA Pin Assignment List - Alphabetical by Signal Name

Table 17: 117-Pin TFBGA Pin Assignment List - Alphabetical by Signal Name

Pin #	Pin Name	Pin #	Pin Name
K2	125CLK	A9	LED_LINK1000
B7	AVDD	C9	LED_RX
M3	AVDD	D9	LED_TX
M4	AVDD	L3	MDC
M7	AVDD	N2	MDI[0]-
M8	AVDD	N1	MDI[0]+
N5	AVDD	N4	MDI[1]-
B6	COL	N3	MDI[1]+
L4	COMA	N7	MDI[2]-
D8	CONFIG[0]	N6	MDI[2]+
E9	CONFIG[1]	N9	MDI[3]-
F8	CONFIG[2]	N8	MDI[3]+
G7	CONFIG[3]	M1	MDIO
F9	CONFIG[4]	G1	NC
G9	CONFIG[5]	K7	NC
G8	CONFIG[6]	K3	RESETn
B5	CRS	M2	RSET
C6	DVDD	B2	RXD0
C7	DVDD	D3	RXD1
D7	DVDD	C3	RXD2
E3	DVDD	B3	RXD3
E7	DVDD	C4	RXD4
F3	DVDD	A1	RXD5
J3	DVDD	A2	RXD6
J7	DVDD	C5	RXD7
E2	GTX_CLK	C1	RX_CLK
M6	HSDAC-	B1	RX_DV
M5	HSDAC+	D2	RX_ER
L1	INTn	A6	S_CLK-
E8	LED_DUPLEX	A5	S_CLK+
C8	LED_LINK10	A4	S_IN-
B8	LED_LINK100	A3	S_IN+
A8	S_OUT-	D4	VSS
A7	S_OUT+	D5	VSS
H8	SEL_FREQ	D6	VSS

Table 17: 117-Pin TFBGA Pin Assignment List - Alphabetical by Signal Name (Continued)

Pin #	Pin Name	Pin #	Pin Name
L9	TCK	E4	VSS
L7	TDI	E5	VSS
K8	TDO	E6	VSS
L8	TMS	F4	VSS
M9	TRSTn	F5	VSS
F1	TXD0	F6	VSS
G2	TXD1	G4	VSS
G3	TXD2	G5	VSS
H2	TXD3	G6	VSS
H1	TXD4	H4	VSS
H3	TXD5	H5	VSS
J1	TXD6	H6	VSS
J2	TXD7	J4	VSS
D1	TX_CLK	J5	VSS
E1	TX_EN	J6	VSS
F2	TX_ER	K4	VSS
B4	VDDO	K5	VSS
C2	VDDO	K6	VSS
K1	VDDO	L5	VSS
B9	VDDOH	L6	VSS
F7	VDDOH	H7	VSSC
J8	VDDOH	H9	XTAL1
K9	VDDOX	J9	XTAL2
L2	VDDOX		

1.7 96-Pin aQFN Pin Assignment List - Alphabetical by Signal Name

Table 18: 96-Pin aQFN Pin Assignment List - Alphabetical by Signal Name

NOTE: The 96-pin BCC package is obsolete and is no longer available. The 96-Pin aQFN package is a pin compatible replacement for the 96-Pin BCC package.

96- Pin BCC Pin #	96- Pin aQFN Pin #	Pin Name	96- Pin BCC Pin #	96- Pin aQFN Pin #	Pin Name
22	B11	125CLK	74	A40	LED_LINK100
32	B15	AVDD	73	A39	LED_LINK1000
35	A19	AVDD	69	A37	LED_RX
36	B17	AVDD	68	B32	LED_TX
40	B19	AVDD	25	A14	MDC
45	A24	AVDD	31	A17	MDI[0]-
78	B36	AVDD	29	A16	MDI[0]+
83	A45	COL	34	B16	MDI[1]-
27	A15	COMA	33	A18	MDI[1]+
65	A35	CONFIG[0]	41	A22	MDI[2]-
64	B30	CONFIG[1]	39	A21	MDI[2]+
63	A34	CONFIG[2]	43	A23	MDI[3]-
61	A33	CONFIG[3]	42	B20	MDI[3]+
60	B28	CONFIG[4]	24	A13	MDIO
59	A32	CONFIG[5]	13	A7	NC
58	B27	CONFIG[6]	51	A28	NC
84	B39	CRS	28	B13	RESETn
1	A1	DVDD	30	B14	RSET
6	B3	DVDD	95	A51	RXD0
10	B5	DVDD	92	B43	RXD1
15	A8	DVDD	93	A50	RXD2
57	A31	DVDD	91	A49	RXD3
62	B29	DVDD	90	B42	RXD4
67	A36	DVDD	89	A48	RXD5
71	A38	DVDD	87	A47	RXD6
85	A46	DVDD	86	B40	RXD7
8	B4	GTX_CLK	2	B1	RX_CLK
38	B18	HSDAC-	94	B44	RX_DV
37	A20	HSDAC+	3	A2	RX_ER
23	A12	INTn	80	B37	S_CLK-
70	B33	LED_DUPLEX	79	A43	S_CLK+
76	B35	LED_LINK10	81	A44	S_IN-

Table 18: 96-Pin aQFN Pin Assignment List - Alphabetical by Signal Name (Continued)

NOTE: The 96-pin BCC package is obsolete and is no longer available. The 96-Pin aQFN package is a pin compatible replacement for the 96-Pin BCC package.

96- Pin BCC Pin #	96- Pin aQFN Pin #	Pin Name	96- Pin BCC Pin #	96- Pin aQFN Pin #	Pin Name
82	B38	S_IN+	4	B2	TX_CLK
75	A41	S_OUT-	9	A5	TX_EN
77	A42	S_OUT+	7	A4	TX_ER
56	B26	SEL_FREQ	5	A3	VDDO
49	A26	TCK	21	A11	VDDO
44	B21	TDI	88	B41	VDDO
50	A27	TDO	96	A52	VDDO
46	B22	TMS	52	B24	VDDOH
47	A25	TRSTn	66	B31	VDDOH
11	A6	TXD0	72	B34	VDDOH
12	B6	TXD1	26	B12	VDDOX
14	B7	TXD2	48	B23	VDDOX
16	B8	TXD3	EPAD	EPAD	VSS
17	A9	TXD4	53	A29	VSSC
18	B9	TXD5	55	A30	XTAL1
19	A10	TXD6	54	B25	XTAL2
20	B10	TXD7			

1.8 128-Pin PQFP Pin Assignment List - Alphabetical by Signal Name

Table 19: 128-Pin PQFP Pin Assignment List - Alphabetical by Signal Name

Pin #	Pin Name	Pin #	Pin Name
31	125CLK	32	INTn
44	AVDD	95	LED_DUPLEX
49	AVDD	100	LED_LINK10
52	AVDD	99	LED_LINK100
59	AVDD	98	LED_LINK1000
64	AVDD	92	LED_RX
104	AVDD	91	LED_TX
114	COL	35	MDC
37	COMA	41	MDI[0]+
88	CONFIG[0]	42	MDI[0]-
87	CONFIG[1]	46	MDI[1]+
86	CONFIG[2]	47	MDI[1]-
82	CONFIG[3]	56	MDI[2]+
81	CONFIG[4]	57	MDI[2]-
80	CONFIG[5]	61	MDI[3]+
79	CONFIG[6]	62	MDI[3]-
115	CRS	33	MDIO
2	DVDD	50	NC
6	DVDD	36	RESETn
12	DVDD	39	RSET
17	DVDD	7	RX_CLK
23	DVDD	4	RX_DV
27	DVDD	8	RX_ER
78	DVDD	3	RXD0
85	DVDD	128	RXD1
90	DVDD	126	RXD2
96	DVDD	125	RXD3
117	DVDD	124	RXD4
118	DVDD	123	RXD5
14	GTX_CLK	121	RXD6
53	HSDAC+	120	RXD7
54	HSDAC-	110	S_CLK+
109	S_CLK-	9	VSS
113	S_IN+	15	VSS
112	S_IN-	21	VSS

Table 19: 128-Pin PQFP Pin Assignment List - Alphabetical by Signal Name (Continued)

Pin #	Pin Name	Pin #	Pin Name
107	S_OUT+	22	VSS
105	S_OUT-	38	VSS
77	SEL_FREQ	40	VSS
70	TCK	43	VSS
67	TDI	45	VSS
72	TDO	48	VSS
69	TMS	51	VSS
68	TRSTn	55	VSS
10	TX_CLK	58	VSS
16	TX_EN	60	VSS
13	TX_ER	63	VSS
18	TXD0	65	VSS
19	TXD1	66	VSS
20	TXD2	83	VSS
24	TXD3	84	VSS
25	TXD4	93	VSS
26	TXD5	94	VSS
28	TXD6	101	VSS
29	TXD7	102	VSS
5	VDDO	103	VSS
11	VDDO	106	VSS
30	VDDO	108	VSS
122	VDDO	111	VSS
73	VDDOH	116	VSS
89	VDDOH	119	VSS
97	VDDOH	127	VSS
34	VDDOX	74	VSSC
71	VDDOX	76	XTAL1
1	VSS	75	XTAL2

2 Functional Description

The 88E1111 device is a 10/100/1000BASE-T/1000BASE-X Gigabit Ethernet transceiver.

Figure 9: 88E1111 Device Functional Block Diagram

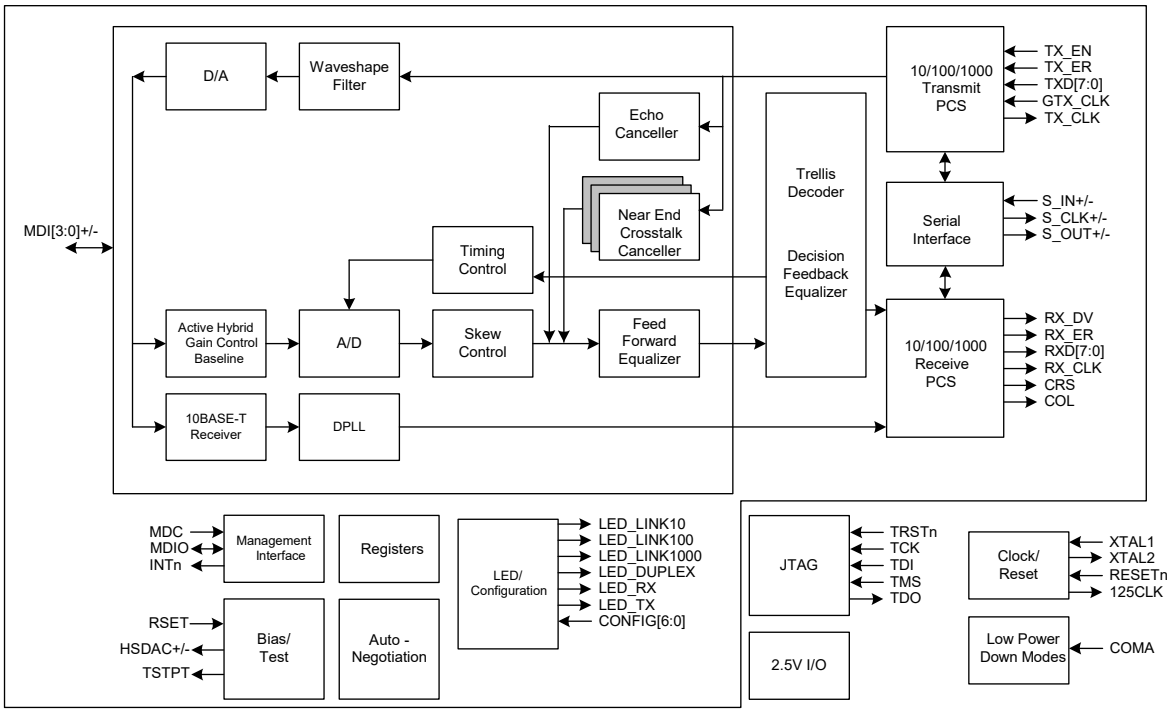


Figure shows the functional block diagram of the 88E1111 device. The transmitter and transmit PCS and PMA blocks are more fully described on Section 2.6.1 "Transmit Side Network Interface" on page 74. The receiver and receive PCS and PMA blocks are more fully described on Section 2.6.3 "Receive Side Network Interface" on page 74.

2.1 88E1111 Device Interface Description

The 88E1111 device supports a number of digital interfaces that support both copper and fiber-optic media. Refer to the connection diagrams further in this section.

2.1.1 Media Interface

2.1.1.1 Copper Interface

The copper interface consists of the MDI[3:0]± pins that connect to the physical media for 1000BASE-T, 100BASE-TX, and 10BASE-T modes of operation. The MDI pins should be terminated externally with 100 ohm differential impedance and connected to an RJ-45 connector through magnetics.

The CAT 5 UTP interface requires 100 ohm differential external terminations. See the "Alaska® Ultra Reference Design Schematics" for details.

2.1.1.2 Fiber Interface

Fiber cable connects to the fiber transceiver. The fiber transceiver is connected via the serial interface pins to the PHY device. The PHY device is then connected to the MAC through the GMII or RGMII interfaces. The serial interface consists of the S_IN±, S_OUT±, and SD± pins.

The input and output buffers of the SERDES interface are internally terminated by programmable 75/50 ohm impedance. The 75/50 OHM configuration bit can be used to select the input or output impedance. Refer to registers 26.5 or 26.6 in Table 102, “Extended PHY Specific Control 2 Register,” on page 172 for details. No external termination is required. The SERDES I/Os are Current Mode Logic (CML) buffers. CML I/Os can be used to connect to other components with PECL or LVDS I/Os. See the “Reference Design Schematics” and "Fiber Interface" application note for details.

Figure 10: CML I/Os

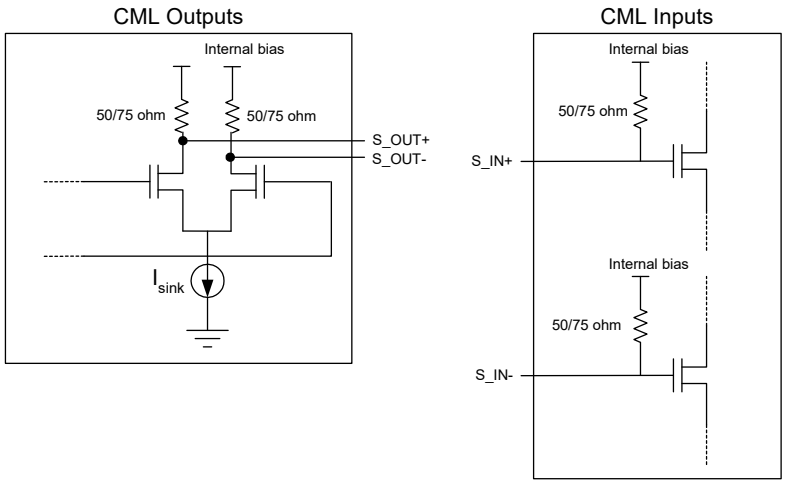


Table 20: Serial Interface Mapping for Fiber Transceiver

88E1111 Device	Description
S_OUT±	1.25 Gbaud transmit output - Positive and Negative
S_IN±	1.25 Gbaud receive input - Positive and Negative
SD±	Signal Detect input from Fiber Transceiver

Signal Detect Input for Fiber Mode

The fiber transceiver's signal detect outputs are typically directly connected to the MAC and there are no signal detect inputs to the PHY (e.g. SERDES PHY). In this case, the 88E1111 PHYs will default to signal detect always being good. If it is desired to use the signal detect output of the fiber transceiver as an input to the 88E1111 device, then the signal detect status will be determined by monitoring the signal detect inputs. To allow this mode of operation, Register 26.7 should be set to 1. One example of why the signal detect input might be needed is to prevent the LEDs from falsely indicating receive or transmit activity based on noise received on the S_IN± inputs when Auto-Negotiation is disabled and no fiber cable is connected.

2.1.2 MAC Interface

The MAC interface supports GMII/MII, RGMII/Modified MII, SGMII, and serial interface connections. These interfaces connect to a 10/100/1000 Mbps Media Access Controller (MAC).

Table 21: 88E1111 Device MAC Interface Pins

88E1111 Device Pins
GTX_CLK
TX_CLK
TX_ER
TX_EN
TXD[7:0]
RX_CLK
RX_ER
RX_DV
RXD[7:0]
CRS
COL
S_IN±
S_CLK±
S_OUT±

2.2 MAC Interfaces

The following sections describes the 88E1111 device MAC Interfaces in detail.

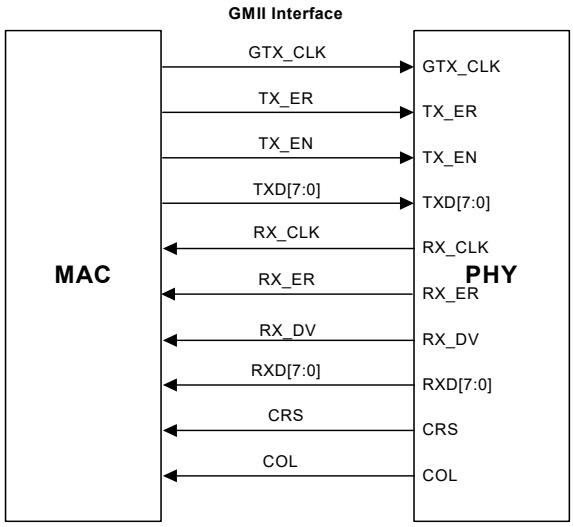
2.2.1 Gigabit Media Independent Interface (GMII/MII)

Table 22 indicates the signal mapping of the 88E1111 device to the GMII interface. MII signaling to support 100BASE-TX and 10BASE-T modes is implemented by sharing pins of the GMII interface. The GMII/MII interface to copper interface is selected by setting the HWCFG_MODE[3:0] to'1111'. The GMII to fiber interface is selected by setting the HWCFG_MODE[3:0] bits to'0111'.

Table 22: GMII/MII Signal Mapping

88E1111 Device Pins	GMII	MII
GTX_CLK	GTX_CLK	-
TX_CLK	-	TX_CLK
TX_ER	TX_ER	TX_ER
TX_EN	TX_EN	TX_EN
TXD[7:0]	TXD[7:0]	TXD[3:0]
RX_CLK	RX_CLK	RX_CLK
RX_ER	RX_ER	RX_ER
RX_DV	RX_DV	RX_DV
RXD[7:0]	RXD[7:0]	RXD[3:0]
CRS	CRS	CRS
COL	COL	COL

Figure 11: GMII Signal Diagram

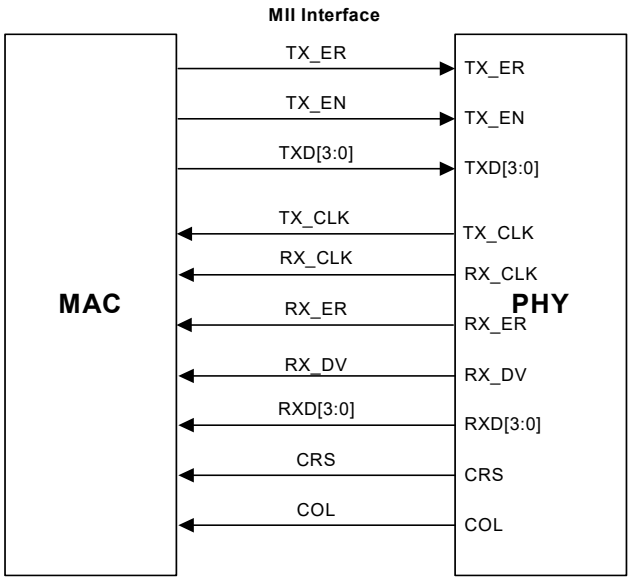


The GMII and MII interfaces are fully compliant to IEEE 802.3 clauses 35 and 22, respectively. The GMII and MII interfaces are enabled by hardware configuration bits HWCFG_MODE[3:0] that are latched at the end of hardware reset. Refer to Section 2.4 "Hardware Configuration" on page 68.

In 1000BASE-T mode, when the GMII interface is selected, a 125 MHz transmit clock is expected on GTX_CLK. Although not part of the GMII interface, TX_CLK is still available and can source 25 MHz, 2.5 MHz, or 0 MHz clock depending on the setting of register 20.6:4; and RX_CLK sources the 125 MHz receive clock. TXD[7:0] and RXD[7:0] signals are used.

In the 100BASE-TX and 10BASE-T modes, when the MII mode is selected, both TX_CLK and RX_CLK source 25 MHz or 2.5 MHz, respectively. TXD[3:0] and RXD[3:0] signals are used. GTX_CLK and TXD[7:4] signals must be pulled high or low and must not be left floating. RXD[7:4] pins are driven low.

Figure 12: MII Signal Diagram



Note During the transition from one speed to another, a dead time for a maximum duration of 1.5 clock cycles may occur on RX_CLK and TX_CLK to insure a glitch-free clock.

In GMII mode, Register 20.15 is the register bit used to block carrier extension.

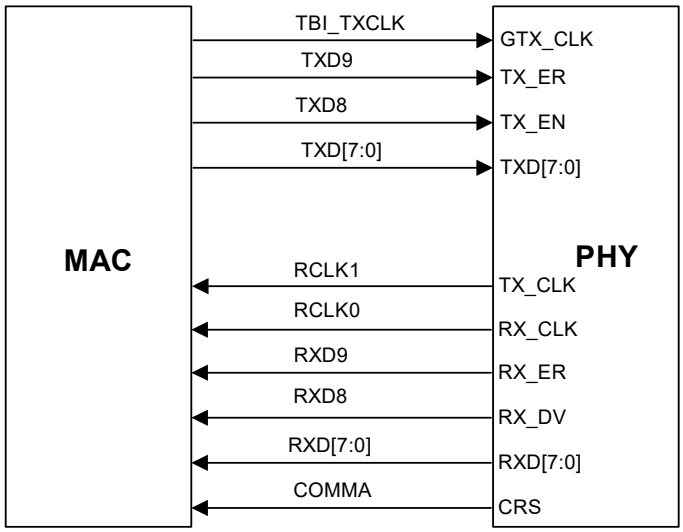
2.2.2 Ten-Bit Interface

The TBI interface pin mapping is shown below. This interface supports 1000 Mbps mode of operation. The TBI to copper interface is selected by setting HWCFG_MODE[3:0] bits to '1101'.

Table 23: TBI Interface Pin Mapping

88E1111 Device Pin Name	TBI Spec Pin Name	Description
GTX_CLK	TBI_TXCLK	125 MHz transmit clock
TX_CLK	RCLK1	62.5 MHz receive clock - even code group
TX_ER	TXD9	Transmit code group bit 9
TX_EN	TXD8	Transmit code group bit 8
TXD[7:0]	TXD[7:0]	Transmit code group bit 7 to 0
RX_CLK	RCLK0	62.5 MHz receive clock - odd code group
RX_ER	RXD9	Receive code group 9
RX_DV	RXD8	Receive code group 8
RXD[7:0]	RXD[7:0]	Receive code group 7 to 0
CRS	COMMA	Valid comma detected

Figure 13: TBI Signal Diagram



In 1000BASE-T mode, the 10-bit interface (TBI) can be used instead of the GMII. An additional layer of encoding and decoding is performed in the data paths, which results in additional latency through the transceiver.

On the receive side, the 88E1111 presents the encoded 1000BASE-X PMA 10-bit receive code group, and the code group is output through the GMII output pins. On the transmit side, the 88E1111 device accepts the PMA 10-bit transmit code-group at the GMII input pins.

Any special symbols such as 1000BASE-X Auto-Negotiation link code words are ignored and treated as idle symbols. For more details on 1000BASE-X, refer to IEEE 802.3 clause 36.

2.2.2.1 TBI to Copper Mode

In 1000BASE-T mode (HWCFG_MODE[3:0] bits to ‘1101’), the TBI can be used instead of the GMII. An additional layer of encoding and decoding is performed in the data paths, which results in additional latency through the transceiver.

In the TBI to copper mode, the PHY will not send to the MAC any received data from the copper cable, if the MAC is not sending valid idles or valid data to the PHY.

2.2.3 Reduced Pin Count GMII (RGMII)

The 88E1111 device supports the RGMII specification (Version 1.2a, 9/22/2000, version 2.0, 04/2002 - note that the 88E1111 device does not support HSTL, but does support the timing specified in RGMII version 2.0). Various other RGMII timing modes, with different clock to data timing, can be programmed by setting 20.1 and 20.7 described in Table 95 on page 165. See "RGMII/RTBI Delay Timing for different RGMII/RTBI timing modes" on Page 213 for timing details. This interface reduces the interconnection between the MAC and the PHY to 12 pins. Data paths and associated control signals are reduced, and control signals are multiplexed together.

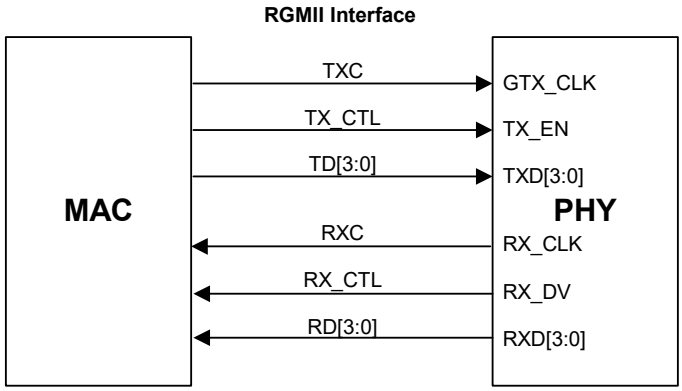
The RGMII to copper mode is selected by setting HWCFG_MODE[3:0] bits to '1011'. Transmit and receive clocks operate at 125 MHz, 25 MHz, and 2.5 MHz depending on the speed selected. The RGMII to fiber is selected by setting HWCFG_MODE[3:0] bits to '0011'.

When the RGMII mode is selected, transmit control (TX_CTL) is presented on both clock edges of GTX_CLK (TXC). Receive control (RX_CTL) is presented on both clock edges of RX_CLK (RXC).

Table 24: RGMII Signal Mapping

88E1111 Device Pin Name	RGMII Spec Pin Name	Description
GTX_CLK	TXC	125 MHz, 25 MHz, or 2.5 MHz transmit clock with ±50 ppm tolerance based on the selected speed.
TX_EN	TX_CTL	Transmit Control Signals. TX_EN is encoded on the rising edge of GTX_CLK, TX_ER XORed with TX_EN is encoded on the falling edge of GTX_CLK.
TXD[3:0]	TD[3:0]	Transmit Data. In 1000BASE-T and 1000BASE-X modes, TXD[3:0] are presented on both edges of GTX_CLK. In 100BASE-TX and 10BASE-T modes, TXD[3:0] are presented on the rising edge of GTX_CLK.
RX_CLK	RXC	125 MHz, 25 MHz, or 2.5 MHz receive clock ± 50 ppm tolerance derived from the received data stream and based on the selected speed.
RX_DV	RX_CTL	Receive Control Signals. RX_DV is encoded on the rising edge of RX_CLK, RX_ER XORed with RX_DV is encoded on the falling edge of RX_CLK.
RXD[3:0]	RD[3:0]	Receive Data. In 1000BASE-T and 1000BASE-X modes, RXD[3:0] are presented on both edges of RX_CLK. In 100BASE-TX and 10BASE-T modes, RXD[3:0] are presented on the rising edge of RX_CLK.

Figure 14: RGMII Signal Diagram



2.2.3.1 10/100 Mbps Functionality

This interface can be used to implement 10/100 Mbps Ethernet Media Independent Interface (MII) by reducing the clock rate to 25 MHz for 100 Mbps operation, and 2.5 MHz for 10 Mbps. The GTX_CLK (TXC) signal is always generated by the MAC, and the RX_CLK (RXC) signal is generated by the PHY.

During packet reception, RX_CLK may be stretched on either the positive or negative pulse to accommodate the transition from the free running clock to a data synchronous clock domain. When the speed of the PHY changes, a similar stretching of the positive or negative pulse is allowed. No glitching of the clocks is allowed during speed transitions.

The MAC must hold TX_EN (TX_CTL) low until the MAC has ensured that TX_EN (TX_CTL) is operating at the same speed as the PHY.

2.2.3.2 TX_ER and RX_ER Coding

See the RGMII Specifications for definitions of RX_CTL, TX_CTL, and in band status coding.

In RGMII mode, Register 20.15 is the register bit used to block carrier extension.

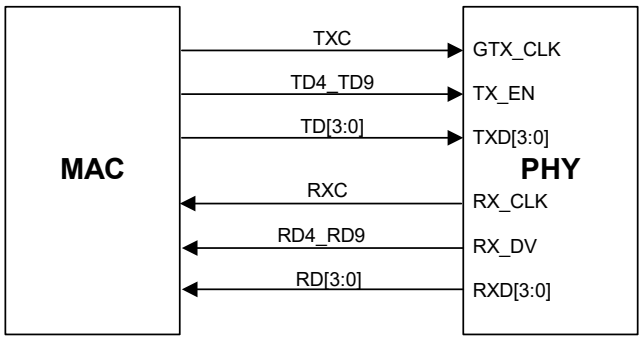
2.2.4 Reduced Pin Count TBI (RTBI)

The 88E1111 device supports RTBI. The RTBI interface pin mapping is shown below. This interface supports 1000 Mbps mode of operation. The RTBI to copper interface is selected by setting HWCFG_MODE[3:0] bits to '1001'.

Table 25: RTBI Signal Mapping

88E1111 Device Pin Name	RTBI Spec Pin Name	Description
GTX_CLK	TXC	125 MHz transmit clock ± 50 ppm tolerance.
TX_EN	TD4_TD9	Transmit - Code Group bits 4 and 9. TX_EN presents bit 4 on the rising edge of GTX_CLK and bit 9 on the falling edge of GTX_CLK.
TXD[3:0]	TD[3:0]	Transmit - Code Group bits 0 to 3 and 5 to 8. TXD[3:0] runs at a double data rate with bits [3:0] presented on the rising edge of GTX_CLK and bits [8:5] on the falling edge of GTX_CLK.
RX_CLK	RXC	125 MHz receive clock ±50 ppm tolerance.
RX_DV	RD4_RD9	Receive Data - Code Group bits 4 and 9. RX_DV presents bit 4 of the 10-bit Code Group on the rising edge of RX_CLK, and bit 9 on the falling edge of RX_CLK.
RXD[3:0]	RD[3:0]	Receive Data. RD[3:0] run at a double data rate with bits [3:0] presented on the rising edge of RX_CLK, and bits [8:5] on the falling edge of RX_CLK.

Figure 15: RTBI Signal Diagram



2.2.5 SGMII Interface

The 88E1111 device supports the SGMII Rev. 1.7 interface to copper. This interface supports 10, 100, and 1000 Mbps modes of operation. The 88E1111 device does not need a TXCLK input as it recovers this clock from input data. This feature has the advantage of reducing pin count, the number of traces on the board, as well as EMI and noise generation.

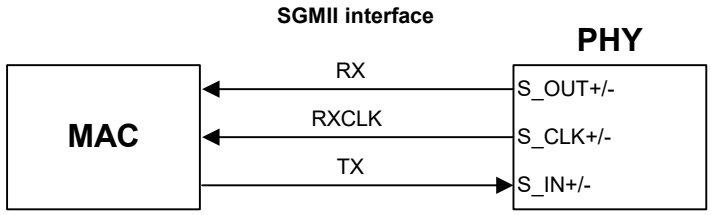
On the receive side, 2 modes of operation: one with a receive clock supplied to the MAC, and one without. The serial interface with clock is selected by setting HWCFG_MODE[3:0] bits to '0000'. The serial interface without clock is selected by setting HWCFG_MODE[3:0] bits to '0100'. The receive clock is required for MACs that do not have clock recovery capability. The SGMII signal mapping is shown in Table 26.

For SGMII mode, if the bypass logic brings up the fiber link, copper auto-negotiation will restart and advertise only gigabit speed.

Table 26: SGMII Serial Interface Pin Mapping

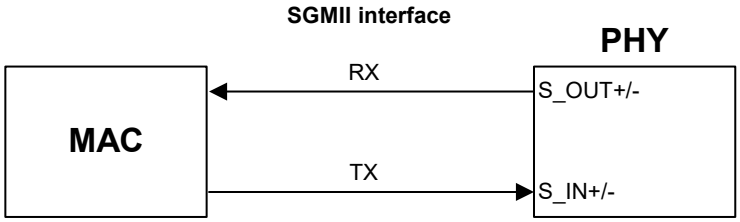
88E1111 Device Pin Name	SGMII Specification Pin Name	Description
S_OUT±	RX	1.25 Gbaud receive output - Positive and Negative
S_CLK±	RXCLK	625 MHz receive clock
S_IN±	TX	1.25 Gbaud transmit input - Positive and Negative

Figure 16: SGMII with Receive Reference Clock



A receive reference clock is available on the S_CLK± pins. This reference clock is for implementing SGMII for MACs without receive clock recovery.

Figure 17: SGMII without Receive Reference Clock



S_CLK± pins can be disabled to save power for MACs with clock recovery capability.

2.2.6 Serial MAC Interface

The serial MAC interface is selected by setting HWCFG_MODE[3:0] bits to ‘1000’ or ‘1100’.The serial interface signal mapping is shown in Table 27.

Two signals (RXD[0] and RXD[1]) function as signal detect outputs. These pins are asserted when the signal on the S_OUT± pins is valid.

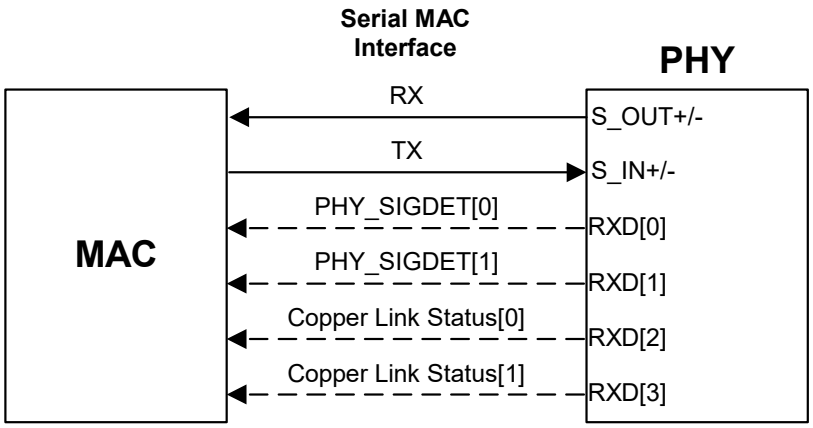
The PHY_SIGDET pins are valid in serial interface to copper modes. Note that RXD[0] and RXD[1] only indicate that the Alaska® Ultra device is outputting a clean signal on the S_OUT± pins. This is independent of whether the copper link status is up or down.

The signals RXD[2] and RXD[3] give the real time link status of the copper side. These signals can be used as signal detect.

Table 27: Serial MAC Interface Pin Mapping

88E1111 Device Pin Name	Serial MAC	Description
S_OUT±	RX	1.25 Gbaud transmit output - Positive and Negative
S_IN±	TX	1.25 Gbaud receive input - Positive and Negative
RXD[0]	PHY_SIGDET[0]	1 = S_OUT± invalid 0 = S_OUT ± valid code groups according to clause 36
RXD[1]	PHY_SIGDET[1]	1 = S_OUT± valid code groups according to clause 36 0 = S_OUT ± invalid
RXD[2]	Copper Link Status [0]	1 = Copper link down 0 = Copper link up
RXD[3]	Copper Link Status [1]	1 = Copper link up 0 = Copper link down

Figure 18: Serial MAC Interface



2.3 88E1111 Device Modes of Operation

Table 28 shows data rates supported by each interface.

Table 28: Data Rates Supported through each Interface

MAC Interface	10BASE-T	100BASE-TX	1000BASE-T	Fiber
GMII			HWCFG_MODE[3:0] 1111	HWCFG_-MODE[3:0] 0111
MII	HWCFG_-MODE[3:0] 1111	HWCFG_-MODE[3:0] 1111		
TBI			HWCFG_MODE[3:0] 1101	
RGMII	HWCFG_MODE[3:0] 1011	HWCFG_MODE[3:0] 1011	HWCFG_MODE[3:0] 1011	HWCFG_MODE[3:0] 0011
RTBI			HWCFG_MODE[3:0] 1001	
SGMII[1]	HWCFG_-MODE[3:0] 0000 or 0100	HWCFG_MODE[3:0] 0000 or 0100	HWCFG_MODE[3:0] 0000 or 0100	
Serial Interface[2]			HWCFG_MODE[3:0] 1000 or 1100	

1. Two SGMII modes are available: 1) with clock and SGMII Auto-Negotiation on, and 2) without clock and SGMII Auto-Negotiation on.
2. Two 1000BASE-X modes are available for the 88E1111 device: 1) legacy 88E1000S without 1000BASE-X Auto-Negotiation without clock, and 2) with 1000BASE-X Auto-Negotiation without clock (GBIC mode).

Table 29: Special Operation Modes

Modes[1]	Hardware Configuration Setting
GMII - SGMII	HWCFG_MODE[3:0] = 1110
RGMII-SGMII	HWCFG_MODE[3:0] = 0110

1. These modes are used for converting GMII/RGMII MAC interfaces to SGMII MAC interface.

2.3.1 Modes of Operation for Copper Media

The 88E1111 device supports various modes of operation for connection to copper media. Figure 19 displays the MAC interfaces for copper modes of operation

Figure 19: MAC to Copper Connection

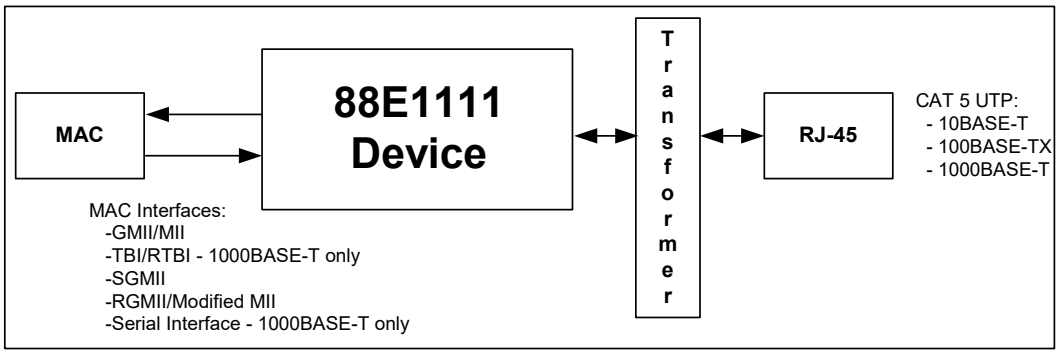


Table 30 shows the mode to select MAC interfaces connecting to copper media.

Table 30: Mode Selection for MAC Interfaces for Copper Media

HWCFG_MODE[3:0]	Description
1111	GMII/MII to Copper
1101	TBI to Copper
1011	RGMII to Copper
1001	RTBI to Copper
0000	SGMII with clock to Copper
0100	SGMII without clock to Copper
1000	1000BASE-X with Auto-Negotiation to Copper
1100	1000BASE-X without Auto-Negotiation to Copper

2.3.1.1 GMII/MII to Copper Mode

The GMII/MII to copper mode is selected by setting HWCFG_MODE[3:0] bits to ‘1111’.

2.3.1.2 TBI to Copper Mode

The TBI to copper mode is selected by setting HWCFG_MODE[3:0] bits to ‘1101’.

2.3.1.3 RGMII to Copper Mode

The RGMII to copper mode is selected by setting HWCFG_MODE[3:0] bits to ‘1011’.

2.3.1.4 RTBI to Copper Mode

The RTBI to copper mode is selected by setting HWCFG_MODE[3:0] bits to ‘1001’.

2.3.1.5 SGMII to Copper Modes

There are two SGMII to copper modes, SGMII with clock, and SGMII without clock.

The SGMII with clock to copper mode is selected by setting HWCFG_MODE[3:0] bits to ‘0000’. The SGMII without clock to copper mode is selected by setting HWCFG_MODE[3:0] bits to ‘0100’.

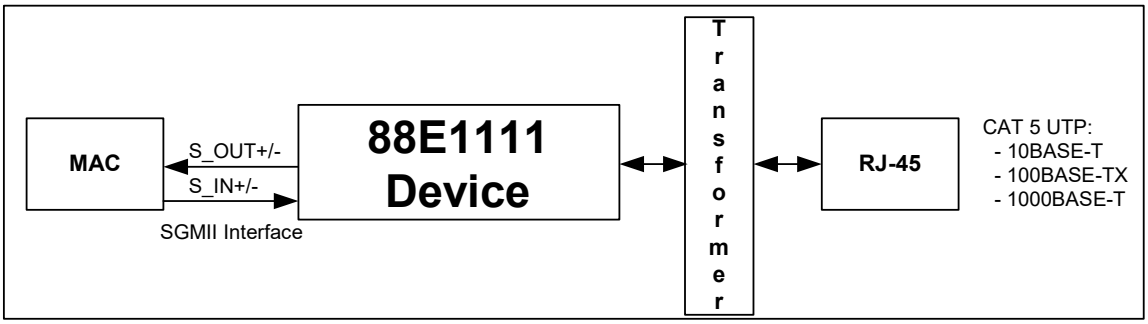
When the copper interface is running in 1000BASE-T mode, the serial 1.25 GHz SGMII encoding is identical to that found in 1000BASE-X.

In 100BASE-TX and 10BASE-T modes, the SGMII interface still runs at 1.25 GHz using 1000BASE-X encoding. However, each byte of data in the packet is repeated 10 or 100 times, respectively. The synchronizing FIFOs are automatically enabled in these modes for both the transmit and receive paths.

The SGMII interface implements a modified 1000BASE-X Auto-Negotiation to indicate link, duplex, and speed to the MAC. The result of the Auto-Negotiation exchange on the copper side is encoded onto the serial interface via the modified Auto-Negotiation so that multi-port devices can adjust to the correct operating speed.

Figure 20 is an example of an 88E1111 device using the SGMII interface.

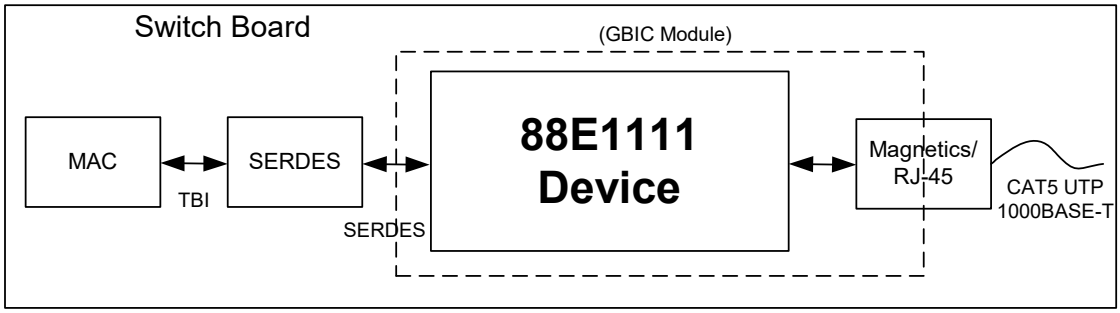
Figure 20: SGMII Interface



2.3.1.6 Serial Interface (SERDES) to Copper Modes

The GBIC mode is selected by setting HWCFG_MODE[3:0] bits to ‘1000’. Figure 21 is an example of the device used for a GBIC application.The GBIC/SERDES interface supports 1000 Mbps operation only.

Figure 21: Typical GBIC Application



The 1000BASE-X Auto-Negotiation information received from the MAC is used by the PHY to control what abilities the PHY advertises on the copper side. For example, if the MAC advertises only full-duplex, but the PHY is configured to advertise both full-duplex and half-duplex, the PHY only advertises full-duplex. The advertise register settings or the configuration pin strap option settings are not modified, although what is advertised on the line is now different.

After the copper Auto-Negotiation is complete, the copper side Auto-Negotiation results are sent to the MAC using 1000BASE-X Auto-Negotiation. For example, the link partner's abilities such as flow control and duplex are indicated to the MAC. The MAC, based on this information, will determine the mode of operation.

This Auto-Negotiation mechanism is different from the SGMII modified 1000BASE-X Auto-Negotiation. In SGMII mode, the Auto-Negotiation is completely done by the PHY. The PHY only reports the results of the Auto-Negotiation such as speed and duplex, as well as link status to the MAC. The only way the MAC can control Auto-Negotiation in SGMII mode is by register writes using the MDC/MDIO interface.

There is also a legacy GBIC mode that does not support 1000BASE-X Auto-Negotiation. The legacy GBIC mode is selected by setting HWCFG_MODE[3:0] to'1100'. This legacy mode is currently used in the first generation of the Marvell® Alaska® PHYs. Changing from GBIC mode to HWCFG_MODE[3:0] '1100' (1000BASE-X without Clock without 1000BASE-X Auto-Neg to copper) does not disable serial interface Auto-Negotiation. A register write of zero to Register 0_1.12 is necessary when switching from GBIC mode to HWCFG_MODE[3:0] '1100'.

In HWCFG_MODE[3:0] '0000', '0100', '1000', and '1100', RXD[1:0] outputs are used as signal detect to indicate when the fiber transmitter is transmitting valid data (when the 88E1111 device is powered up and not being reset). See Table 35 for connection details.

In HWCFG_MODE[3:0] '0000', '0100', '1000', and '1100', RXD[3:2] can be used to indicate the copper link status. In this mode the LED_LINK10, LED_LINK100, and LED_LINK1000 pins cannot be used to indicate copper link status because the LED_LINK10, LED_LINK100, and LED_LINK1000 toggle during configuration. The RXD[3:2] pins must strictly indicate copper link status and not mirror the LED output. The link status will be real time status.

The definition of RXD[2] is 1 = Copper link down, 0 = Copper link up. The definition of RXD[3] is 0 = Copper link down, 1 = Copper link up.

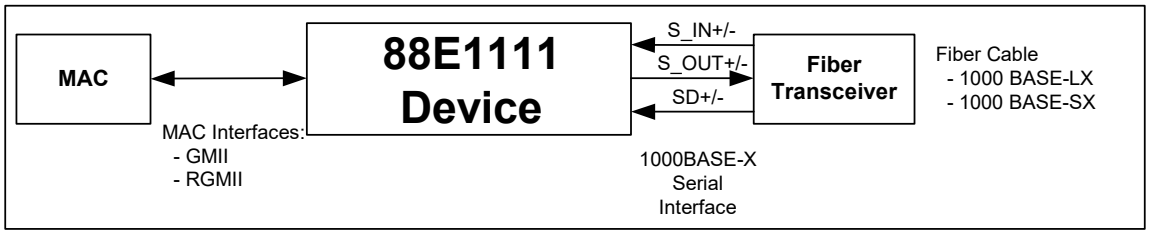
Note that during hardware reset it is undetermined whether the PHY will be configured in fiber or copper mode.

See Table 27 for connection details.

2.3.2 Modes of Operation for Fiber Media

Figure 22 displays the MAC interfaces for fiber modes of operation.

Figure 22: MAC to Fiber Connection



There are two modes of fiber operation. Table 31 shows the mode to select digital interfaces connecting to fiber media.

Table 31: Mode Selection for MAC Interfaces for Fiber Media

HWCFG_ MODE[3:0]	Description
0111	GMII to Fiber
0011	RGMII to Fiber

2.3.2.1 GMII to Fiber Mode

The GMII to fiber mode is selected by setting the HWCFG_MODE bits to ’0111’. When GMII is connected to the MAC and the serial interface is connected to a fiber transceiver, only the 1000 Mbps mode is active.

On the transmit and receive sides, data is converted and sent to and from the serial interface. This mode supports 1000BASE-X Auto-Negotiation.

2.3.2.2 RGMII to Fiber Mode

The RGMII to fiber mode is selected by setting the HWCFG_MODE bits to ’0011’. In RGMII to fiber mode, 1000 Mbps Auto-Negotiation is used.

2.3.3 GMII/MII to SGMII and RGMII to SGMII Mode

The 88E1111 device supports both GMII/MII to SGMII mode and RGMII to SGMII mode. GMII/MII to SGMII mode is selected by setting the HWCFG_MODE bits to ’1110’, and RGMII to SGMII mode is selected by setting the HWCFG_MODE bits to ’0110’. The GMII/MII and RGMII to SGMII mode supports all three speeds (10/100/1000). The SGMII behaves as if it were the SGMII on the MAC side of the interface.

In the case of Auto-Negotiation enable, the SGMII Auto-Negotiation information (speed, duplex and link) received from the PHY is used to determine the mode of operation. The speed and duplex of GMII/MII and RGMII will be adjusted accordingly when SGMII Auto-Negotiation is completed. In GMII/MII and RGMII to SGMII modes, link is defined to be up and the corresponding speed LED will be active when Auto-Negotiation is complete and the PHY SGMII partner’s link is up. In RGMII to SGMII mode this link up condition will be shown in the in-band status.

In the case of Auto-Negotiation disable, the speed and duplex is determined by Register 20.5:4 for speed and Register 0_1_8 for duplex. (20.5:4 = 00 selects 10 Mbps, 01 selects 100 Mbps, 10 selects 1000 Mbps.) In GMII/MII and RGMII to SGMII modes, the link is defined to be up when valid idles are received.

The transmit and receive FIFOs are enabled in both modes. S_CLK± is enabled by default.

2.3.4 Mode Switching

The operating mode selected at power up may be changed by writing to Register 27.3:0 with the new mode as indicated on Table 35. Any mode change must be followed by a software reset. Operation may begin in the new mode when the software reset is completed. There are additional register changes required that are not automatically completed for some mode changes. These are summarized below:

- When switching from a mode that is only capable of 1000 Mbps to a 10/100 Mbps mode, the copper Register 4 must be set with the appropriate 10/100 Mbps advertisement.
- When switching from RGMII to SGMII mode to RGMII to fiber mode, Register 4 must be set to advertise the proper 1000BASE-X capabilities; otherwise, the 1000BASE-X will not come up.
- 0_1.12 must be appropriately set when changing between a serial interface to copper mode that uses Auto-Negotiation (HWCFG_MODE bits set to’1000’ or’0x00’) and one that doesn't (HWCFG_MODE bits set to ’1100’). This is not done automatically.
- Register 27.12 must be reprogrammed when changing between modes that use Serial Interface Auto-Negotiation bypass mode (HWCFG_MODE bits set to ’1000’, ’0011’ or ’0111’) and those that do not (HWCFG_MODE bits set to ’0x00’).
- When changing MAC interfaces for auto selection, the mode programmed must always be the copper mode (as with the power up mode).

2.4 Hardware Configuration

Configuration options like physical address, PHY operating mode, Auto-Negotiation, MDI crossover (ENA_XC), and physical connection type are configured by using the configuration pins

CONFIG[6:0] pins must be tied to one of the pins shown in Table 32 based on the configuration options selected. They should not be left floating.

Note Configuration options can be overwritten by register writes, with the exception of the PHY addresses. Configuration options are specified by tying the CONFIG[6:0] pins to the LED output, VDDO, or VSS pins. The LED output, VDDO, and VSS pins are encoded to the values shown in Table 32.

Table 32: Pin to Constant Mapping

Pin	Bit[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

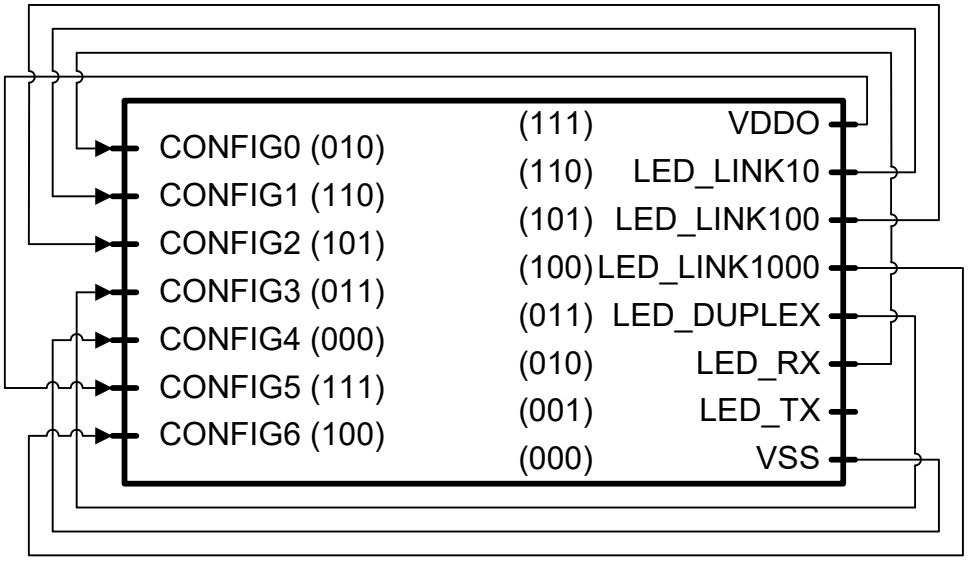
The encoded values of the LED output tied to the CONFIG[6:0] pins are latched at the de-assertion of the RESETn pin. The 88E1111 device configuration options associated to each configuration pin are shown in Table 34.

Figure 23 illustrates a common configuration connection that will enable the conditions listed in Table 33.

Table 33: CONFIG Pin Connection Example

Pin	LED Pin Connection	Hardware Configuration Bit Setting	Configuration
CONFIG0	LED_RX	010	PHY Address bit [2:0] = 010
CONFIG1	LED_LINK10	110	Enable Pause, PHY address bit[4:3] = 10
CONFIG2	LED_LINK100	101	Auto-Neg advertise 1000BASE-T only, prefer master
CONFIG3	LED_DUPLEX	011	Enable MDI crossover, disable 125CLK
CONFIG4	VSS	000	1000BASE-X without clock with 1000BASE-X Auto-Neg to copper (GBIC)
CONFIG5	VDDO	111	Disable fiber/copper Auto-detect, Disable sleep
CONFIG6	LED_LINK1000	100	Select TWSI interface, INT signal active high, 50 ohm SERDES (SFP application)

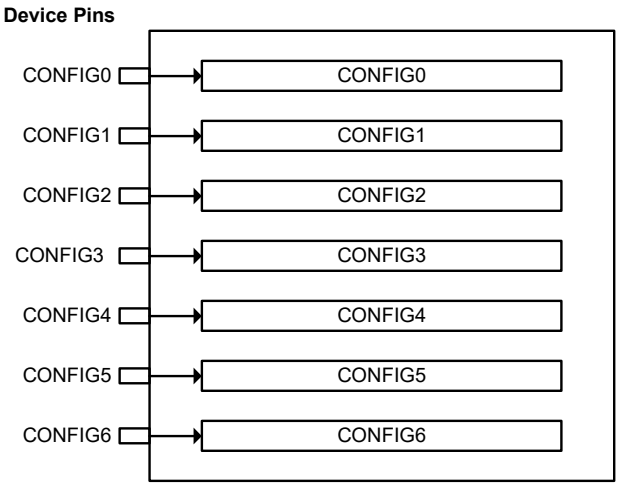
Figure 23: Configuration Connection Example



2.4.1 88E1111 Device Configuration Description

For the 88E1111 device, the encoded values of the LED output tied to the CONFIG[6:0] pins are latched at the de-assertion of the RESETn pin. The CONFIG[6:0] inputs come out to the corresponding CONFIG pins. See Figure 24 for details.

Figure 24: 88E1111 Device Configuration Input



The 88E1111 device configuration options associated to each configuration pin are shown in Table 34.

Table 34: 88E1111 Device Pin to Configuration Bit Mapping

Pin	Bit[2]	Bit[1]	Bit[0]
CONFIG0	PHYADR[2][1]	PHYADR[1][1]	PHYADR[0][1]
CONFIG1	ENA_PAUSE	PHYADR[4][1]	PHYADR[3][1]
CONFIG2	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG3	ANEG[0]	ENA_XC	DIS_125
CONFIG4	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]
CONFIG5	DIS_FC	DIS_SLEEP	HWCFG_MODE[3]
CONFIG6	SEL_TWSI	INT_POL	75/50 OHM

1. For the TWSI device address, the lower 5 bits (PHYADR[4:0]), are latched during hardware reset, and the device address bits ([6:5]) are fixed at '10'.

Refer to Table 35 for a detailed description of the 88E1111 device configuration options.

Table 35: 88E1111 Device Configuration Register Definitions

Configuration	Description
PHYADR[4:0]	PHY Address. PHY Address in MDC/MDIO mode Lower 5 address bits are used in bi-directional data transfer mode
ENA_PAUSE	Enable Pause. 0 = Default register 4.11:10 to 00 - copper 1 = Default register 4.11:10 to 11 - copper 0 = Default register 4.8:7 to 00 - fiber 1 = Default register 4.8:7 to 11 - fiber
ANEG[3:0]	Auto-Negotiation Configuration for copper modes. ANEG[3:0] determines whether Auto-Negotiation should be turned on, Master/Slave preference, and the speed and duplex at which to run. ANEG [3:2] also determines duplex advertised in 1000BASE-X mode. 0000 = Forced 10BASE-T half-duplex 0001 = Forced 10BASE-T full-duplex 0010 = Forced 100BASE-TX half-duplex 0011 = Forced 100BASE-TX full-duplex 0100 = Auto-Neg, advertise only 1000BASE-T half-duplex, forced Master 0101 = Auto-Neg, advertise only 1000BASE-T half-duplex, forced Slave 0110 = Auto-Neg, advertise only 1000BASE-T half-duplex, preferred Master 0111 = Auto-Neg, advertise only 1000BASE-T half-duplex, preferred Slave 1000 = Auto-Neg, advertise only 1000BASE-T full-duplex, forced Master 1001 = Auto-Neg, advertise only 1000BASE-T full-duplex, forced Slave 1010 = Auto-Neg, advertise only 1000BASE-T full-duplex, preferred Master 1011 = Auto-Neg, advertise only 1000BASE-T full-duplex, preferred Slave 1100 = Auto-Neg, advertise all capabilities, forced Master 1101 = Auto-Neg, advertise all capabilities, forced Slave 1110 = Auto-Neg, advertise all capabilities, prefer Master 1111 = Auto-Neg, advertise all capabilities, prefer Slave
ANEG[3:2]	Auto-Negotiation Configuration for fiber modes. ANEG[3:2] determines whether Auto-Negotiation should be turned on, and the speed and duplex at which to run. 01 = Forced 1000BASE-X half-duplex 10 = Forced 1000BASE-X full-duplex 11 = Auto-Negotiation enabled, 1000BASE-X full-duplex/Auto-Negotiation enabled, 1000BASE-X half-duplex[1]

1. For Auto-Negotiation, half-duplex, set ANEG[3:2] = 11 AND change to half-duplex by disabling full-duplex in Register bit 0.8, and by disabling full-duplex advertisement in Register bit 4.5.

Table 35: 88E1111 Device Configuration Register Definition (Continued)

Configuration	Description
ENA_XC	Enable Crossover. ENA_XC selects whether the MDI crossover function is enabled. If the MDI crossover function is disabled, then the device assumes the MDI configuration. 0 = Disable 1 = Enable
DIS_125	Disable 125MHz clock. 0 = Enable 125CLK 1 = Disable 125CLK
HWCFG MODE[3:0]	Hardware Configuration Mode. HWCFG_MODE[3:0] specifies the operating mode of the 88E1111 device. Modes 0001, 0101, 1001, 1101, 0111, 1111, 0011, and 1011 can be overridden if the automatic selection of the copper/fiber interface is enabled (e.g. if GMII to copper is selected but the PHY detects energy on the fiber lines, the mode will become GMII to fiber if DIS_FC = 0). 0000 = SGMII with Clock with SGMII Auto-Neg to copper 0100 = SGMII without Clock with SGMII Auto-Neg to copper 1000 = 1000BASE-X without Clock with 1000BASE-X Auto-Neg to copper (GBIC) 1100 = 1000BASE-X without Clock without 1000BASE-X Auto-Neg to copper 0001 = Reserved 0101 = Reserved 1001 = RTBI to copper 1101 = TBI to copper 0010 = Reserved 0110 = RGMII to SGMII 1010 = Reserved 1110 = GMII to SGMII 0011 = RGMII to Fiber 0111 = GMII to Fiber 1011 = RGMII to copper 1111 = GMII to copper
DIS_FC	Disable fiber/copper interface. DIS_FC is used to enable or disable the automatic selection of the fiber/copper interface. (The PHY automatically switches between the fiber and copper interface based on energy detected on those lines, and if Auto-Negotiation is complete.) 0 = Enable fiber/copper auto selection 1 = Disable fiber/copper auto selection
DIS_SLEEP	Energy detect. DIS_SLEEP is used to enable or disable energy detect. 0 = Enable energy detect 1 = Disable energy detect

Table 35: 88E1111 Device Configuration Register Definitions (Continued)

Configuration	Description
SEL_TWSI	Interface select. SEL_TWSI selects whether the MDC/MDIO interface or the Two-Wire Serial Interface (TWSI) is enabled. 0 = Select MDC/MDIO interface 1 = Select Two-Wire Serial Interface
INT_POL	Interrupt polarity 0 = INTn signal is active HIGH 1 = INTn signal is active LOW
75/50 OHM	Termination resistance. Selects default value 50 Ω or 75 Ω fiber (or SGMII) input or output impedance. Refer to Register 26.6 and 26.5 for details. 0 = 50 ohm termination for fiber 1 = 75 ohm termination for fiber

2.5 Synchronizing FIFO

The 88E1111 device controls transmit and receive synchronizing FIFOs to reconcile frequency differences between the clocks in all MAC interfaces, the serial interface, the management interface, and internal clocks. The depth of the transmit and receive FIFOs can be independently programmed by programming register bits 16.15:12. See the "Alaska® Ultra FAQs" for details on how to calculate required FIFO depth and the details of the different clocks used for transmit and receive in each mode of operation.

The FIFO depths can be increased in length by programming Register 16.15:12 to support longer frames. The 88E1111 device can handle jumbo frame sizes up to 10 Kbytes with up to ± 150 PPM clock jitter. The deeper the FIFO depth, the higher the latency will be.

Table 36 shows when transmit and receive FIFOS are enabled or disabled for each mode.

Table 36: FIFO Enable/Disable based on the Mode Selected

Mode of Operation	10BASE-T		100BASE-T		1000BASE-T		1000BASE-X	
	TX FIFO	RX FIFO	TX FIFO	RX FIFO	TX FIFO	RX FIFO	TX FIFO	RX FIFO
GMII/MII	Off	Off	Off	Off	On	Off	On	On
TBI	-	-	-	-	On	On	-	-
RGMII/Modified MII	On	Off	On	Off	On	Off	On	On
RTBI	-	-	-	-	On	On	-	-
SGMII	On	On	On	On	On	On	-	-
Serial Interface[1]	-	-	-	-	On	On	-	-

1. Two 1000BASE-X modes are available for the 88E1111 device: 1) legacy 88E1000S without 1000BASE-X Auto-Negotiation without clock, and 2) with 1000BASE-X Auto-Negotiation without clock (GBIC mode).

2.6 Copper Media Transmit and Receive Functions

The transmit and receive paths for the 88E1111 device are described in the following sections.

2.6.1 Transmit Side Network Interface

2.6.1.1 Multi-mode TX Digital to Analog Converter

The 88E1111 device incorporates a multi-mode transmit DAC to generate filtered 4D PAM 5, MLT3, or Manchester coded symbols. The transmit DAC performs signal wave shaping to reduce EMI. The transmit DAC is designed for very low parasitic loading capacitances to improve the return loss requirement, which allows the use of low cost transformers.

2.6.1.2 Slew Rate Control and Waveshaping

In 1000BASE-T mode, partial response filtering and slew rate control is used to minimize high frequency EMI. In 100BASE-TX mode, slew rate control is used to minimize high frequency EMI. In 10BASE-T mode, the output waveform is pre-equalized via a digital filter.

2.6.2 Encoder

2.6.2.1 1000BASE-T

In 1000BASE-T mode, the transmit data bytes are scrambled to 9-bit symbols and encoded into 4D PAM 5 symbols. Upon initialization, the initial scrambling seed is determined by the PHY address. This prevents multiple 88E1111 device from outputting the same sequence during idle, which helps to reduce EMI.

2.6.2.2 100BASE-TX

In 100BASE-TX mode, the transmit data stream is 4B/5B encoded, serialized, and scrambled. Upon initialization, the initial scrambling seed is determined by the PHY address. This prevents multiple 88E1111 device from outputting the same sequence during idle, which helps to reduce EMI.

2.6.2.3 10BASE-T

In 10BASE-T mode, the transmit data is serialized and converted to Manchester encoding.

2.6.3 Receive Side Network Interface

2.6.3.1 Analog to Digital Converter

The 88E1111 device incorporates an advanced high speed ADC on each receive channel with greater resolution than the ADC used in the reference model of the 802.3ab standard committee. Higher resolution ADC results in better SNR, and therefore, lower error rates. Patented architectures and design techniques result in high differential and integral linearity, high power supply noise rejection, and low metastability error rate. The ADC samples the input signal at 125 MHz.

2.6.3.2 Active Hybrid

The 88E1111 device employs a sophisticated on-chip hybrid to substantially reduce the near-end echo, which is the super-imposed transmit signal on the receive signal. The hybrid minimizes the echo to reduce the precision requirement of the digital echo canceller. The on-chip hybrid allows both the transmitter and receiver to use the same transformer for coupling to the twisted pair cable, which reduces the cost of the overall system.

2.6.3.3 Echo Canceller

Residual echo not removed by the hybrid and echo due to patch cord impedance mismatch, patch panel discontinuity, and variations in cable impedance along the twisted pair cable result in drastic SNR degradation on the receive signal. The 88E1111 device employs a fully developed digital echo canceller to adjust for echo impairments from more than 100 meters of cable. The echo canceller is fully adaptive to compensate for the time varying nature of channel conditions.

2.6.3.4 NEXT Canceller

The 1000BASE-T physical layer uses all 4 pairs of wires to transmit data to reduce the baud rate requirement to only 125 MHz. This results in significant high frequency crosstalk between adjacent pairs of cable in the same bundle. The 88E1111 device employs 3 parallel NEXT cancellers on each receive channel to cancel any high frequency crosstalk induced by the adjacent 3 transmitters. A fully adaptive digital filter is used to compensate for the time varying nature of channel conditions.

2.6.3.5 Baseline Wander Canceller

Baseline wander is more problematic in the 1000BASE-T environment than in the traditional 100BASE-TX environment due to the DC baseline shift in both the transmit and receive signals. The 88E1111 device employs an advanced baseline wander cancellation circuit to automatically compensate for this DC shift. It minimizes the effect of DC baseline shift on the overall error rate.

2.6.3.6 Digital Adaptive Equalizer

The digital adaptive equalizer removes inter-symbol interference at the receiver. The digital adaptive equalizer takes unequalized signals from ADC output and uses a combination of feedforward equalizer (FFE) and decision feedback equalizer (DFE) for the best-optimized signal-to-noise (SNR) ratio.

2.6.3.7 Digital Phase Lock Loop

In 1000BASE-T mode, the slave transmitter must use the exact receive clock frequency it sees on the receive signal. Any slight long-term frequency phase jitter (frequency drift) on the receive signal must be tracked and duplicated by the slave transmitter; otherwise, the receivers of both the slave and master physical layer devices have difficulty canceling the echo and NEXT components. In the 88E1111 device, an advanced DPLL is used to recover and track the clock timing information from the receive signal. This DPLL has very low long-term phase jitter of its own, thereby maximizing the achievable SNR.

2.6.3.8 Link Monitor

The link monitor is responsible for determining if link is established with a link partner. In 10BASE-T mode, link monitor function is performed by detecting the presence of valid link pulses (NLPs) on the MDI± pins.

In 100BASE-TX and 1000BASE-T modes, link is established by scrambled idles.

If Force Link Good register 16.10 is set high, the link is forced to be good and the link monitor is bypassed for 100BASE-TX and 10BASE-T modes. In the 1000BASE-T mode, register 16.10 has no effect.

2.6.3.9 Signal Detection

In 1000BASE-T mode, signal detection is based on whether the local receiver has acquired lock to the incoming data stream.

In 100BASE-TX mode, the signal detection function is based on the receive signal energy detected on the MDI± pins that is continuously qualified by the squelch detect circuit, and the local receiver acquiring lock.

2.6.4 Decoder

2.6.4.1 1000BASE-T

In 1000BASE-T mode, the receive idle stream is analyzed so that the scrambler seed, the skew among the 4 pairs, the pair swap order, and the polarity of the pairs can be accounted for. Once calibrated, the 4D PAM 5 symbols are converted to 9-bit symbols that are then descrambled into 8-bit data values. If the descrambler loses lock for any reason, the link is brought down and calibration is restarted after the completion of Auto-Negotiation.

2.6.4.2 100BASE-TX

In 100BASE-TX mode, the receive data stream is recovered and converted to NRZ. The NRZ stream is descrambled and aligned to the symbol boundaries. The aligned data is then parallelized and 5B/4B decoded. The receiver does not attempt to decode the data stream unless the scrambler is locked. The descrambler “locks” to the *scrambler* state after detecting a sufficient number of consecutive idle code-groups. Once locked, the descrambler continuously monitors the data stream to make sure that it has not lost synchronization. The descrambler is always forced into the *unlocked* state when a link failure condition is detected, or when insufficient idle symbols are detected.

2.6.4.3 10BASE-T

In 10BASE-T mode, the recovered 10BASE-T signal is decoded from Manchester to NRZ, and then aligned. The alignment is necessary to insure that the start of frame delimiter (SFD) is aligned to the nibble boundary.

2.7 Power Supplies

The 88E1111 device requires 2 power supplies: 2.5V, and 1.0V. 1.2V can be used instead of 1.0V, if it is available on the board. For the I/O pins, there are three separate groupings: VDDO, VDDOH, VDDOX.

2.7.1 VDDO

VDDO is used for the MAC interface I/O pins[1] only. There is one supply option for VDDO: 2.5V

2.7.2 VDDOH

VDDOH is used for the LED[2], CONFIG[3], XTAL1, XTAL2, and SEL_FREQ pin power. VDDOH supports 2.5V.

2.7.3 VDDOX

VDDOX is used for MDC/MDIO/INTn/125CLK/RESETn/JTAG[4] pin power. This supply supports 2.5V. These pins have a fixed input threshold that is a function of supply voltage. This flexibility in supply voltage allows the user not to use any level shifters.

For the 88E1111 device internal logic, there are two separate supplies: AVDD and DVDD.

2.7.4 AVDD

AVDD is used for the analog high digital logic. AVDD is used as the 2.5V analog supply.

2.7.5 DVDD

DVDD is used for the digital logic. DVDD is the 1.0V digital supply. 1.2V can be used instead of 1.0V if 1.0V supply is not available. If the 1.2V option is used, refer to the current consumption values shown in "Current Consumption DVDD (1.2V)" on page 192.

1. GTX_CLK, TX_CLK, TX_EN, TX_ER, TXD[7:0], RX_CLK, RX_DV, RX_ER, RXD[7:0], CRS, and COL.
2. LED_LINK10, LED_LINK100, LED_LINK1000, LED_DUPLEX, LED_RX, and LED_TX.
3. CONFIG[4:0], GCONFIG0, GCONFIG1.
4. TDI, TMS, TCK, TRSTn, and TDO.

2.8 Power Management

The 88E1111 device supports several advanced power management modes that conserve power.

2.8.1 Low Power Modes

Four low power modes are supported in the 88E1111 device.

- COMA
- IEEE 22.2.4.1.5 compliant power down
- Energy Detect (Mode 1)
- Energy Detect+™ (Mode 2)

The COMA (deep sleep) mode disables all the active circuitry to draw absolute minimum power.

IEEE 22.2.4.1.5 power down compliance allows for the PHY to be placed in a low-power consumption state by register control.

Energy Detect (Mode 1) allows the 88E1111 device to wake up when energy is detected on the wire.

Energy Detect+™ (Mode 2) is identical to Mode 1 with the additional capability to wake up a link partner. In Mode 2, the 10BASE-T link pulses are sent once every second while listening for energy on the line.

Details of each mode are described below.

2.8.2 Enabling Low Power Modes

The 88E1111 device has one pin dedicated to support the low power modes.

- The COMA pin is a direct input from the MAC. It can be used to put the PHY into or out of the COMA mode. Refer to the Signal Description for COMA pin details.
- The CONFIG3 pin is sampled during power-on reset, and is used to select between normal modes of operation and the energy detect low power down modes. The default mode is Mode 2 when DIS_SLEEP is 0. See Section 2.4 "Hardware Configuration" on page 68.

Low power modes are also register programmable. Register 16.9:8 allows the user to select between Mode 1 and Mode 2. When the low power modes are not selected, Register 0.11 may be used. If during the energy detect modes, the PHY wakes up and starts operating at a normal mode, Register 16.9:8 settings are retained. When the link is lost and energy is no longer detected, the 88E1111 device returns to the mode stored in Register 16.9:8.

Table 37: Low Power Mode Activation

Power Mode	How to Activate Mode
COMA (Deep Sleep)	Dedicated pin to activate - COMA (see Table 12 for COMA pin details).
IEEE Power down	Register 0.11 write
Energy Detect	Configuration option & Register 16.9:8 write

2.8.3 Low Power Operating Modes

2.8.3.1 COMA Mode

The COMA mode can be activated by asserting "high" on the COMA pin. In the COMA mode, all the PHY functions including transmit, receive, and serial management interface are completely disabled. No circuitry is running, and all the internal clocks are stopped. The 125 MHz output clock is disabled as well. This mode is for applications that require absolute minimum power.

COMA mode can be deactivated by de-asserting "high" on the COMA pin only. Since the serial management interface is disabled during this mode, read or write to registers is not possible in COMA mode. Moreover, since all the active circuitry is disabled during this mode, the energy detect function is disabled. Upon exiting COMA mode a hardware reset must be completed for the 88E1111 device to resume normal operation. The COMA low power mode cannot be enabled as long as hardware reset is enabled.

In the COMA mode, the PHY cannot wake up on its own by detecting activity on the CAT 5 cable.

2.8.3.2 IEEE Power Down Mode

The standard IEEE power down mode is entered by setting Register 0.11 equal to one. In this mode, the PHY does not respond to any MAC interface signals except the MDC/MDIO. It also does not respond to any activity on the CAT 5 cable.

In this power down mode, the PHY cannot wake up on its own by detecting activity on the CAT 5 cable. It can only wake up by setting Register 0.11 to 0.

2.8.3.3 Energy Detect Power Down Modes

The 88E1111 device can be placed in energy detect power down modes by selecting either of the two energy detect modes. Both modes enable the PHY to wake up on its own by detecting activity on the CAT 5 cable.

In order to exit these modes of operation, bits 9:8 must be set to 00, and there must be a software reset. See Register 16.9:8 in the 3 "Register Description" on page 121.

2.8.3.4 Energy Detect (Mode 1)

In Mode 1, only the signal detection circuitry and serial management interface are active. If the PHY detects energy on the line, it starts to Auto-Negotiate sending FLPs for 5 seconds. If at the end of 5 seconds the Auto-Negotiation is not completed, then the PHY stops sending FLPs and goes back to monitoring receive energy. If Auto-Negotiation is completed, then the PHY goes into normal 10/100/1000 Mbps operation. If during normal operation the link is lost, the PHY will re-start Auto-Negotiation. If no energy is detected after 5 seconds, the PHY goes back to monitoring receive energy.

2.8.3.5 Energy Detect +^{TM} (Mode 2)

In Mode 2, the PHY sends out a single 10 Mbps NLP (Normal Link Pulse) every one second. Except for this difference, Mode 2 is identical to Mode 1 operation. If the 88E1111 device is in Mode 1, it cannot wake up a connected device; therefore, the connected device must be transmitting NLPs, or either device must be woken up through register access. If the 88E1111 device is in Mode 2, then it can wake a connected device. The default mode of operation is Mode 2 when DIS_SLEEP is 0.

2.8.3.6 Normal 10/100/1000 Mbps Operation

Normal 10/100/1000 Mbps operation can be entered by either using a configuration option or a register write during energy detect modes.

2.8.4 125CLK and MAC Interface Effect on Low Power Modes

In some applications, the 125CLK or the clocks on the MAC interface must run continuously regardless of the state of the PHY. Additional power will be required to keep these clocks running during low power states.

If absolute minimal power consumption is required during the IEEE power down mode or the Energy Detect modes, then Register 16.4 should be set to 1 to disable the toggling of 125CLK, and Register 16.3 should be set to 0 to allow the MAC interface to power down. Note that for these settings to take effect a software reset must be issued.

2.9 Management Interface

The management interface provides access to the internal registers via the MDC and MDIO pins and is compliant with IEEE 802.3u clause 22. MDC is the management data clock input and, it can run from DC to a maximum rate of 8.3 MHz. At high MDIO fanouts the maximum rate may be decreased depending on the output loading. MDIO is the management data input/output and is a bi-directional signal that runs synchronously to MDC.

The MDIO pin requires a pull-up resistor in a range from 1.5 kohm to 10 kohm that pulls the MDIO high during the idle and turnaround.

PHY address is configured during the hardware reset sequence. Refer to Section 2.4 "Hardware Configuration" on page 68 for more information on how to configure PHY addresses.

Typical read and write operations on the management interface are shown in Figure 25 and Figure 26. All the required serial management registers are implemented as well as several optional registers. A description of the registers can be found in the Register Description.

Figure 25: Typical MDC/MDIO Read Operation

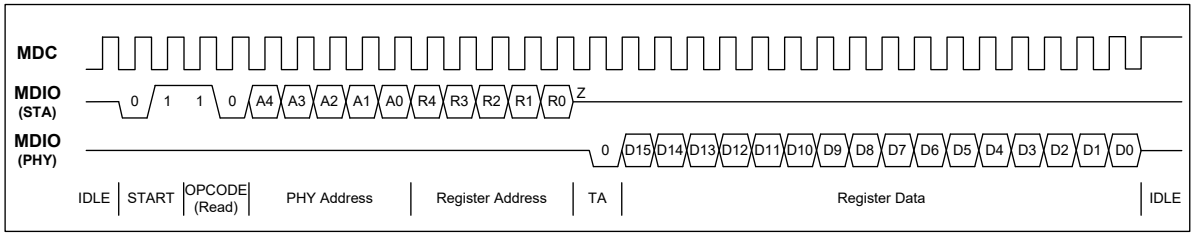


Figure 26: Typical MDC/MDIO Write Operation

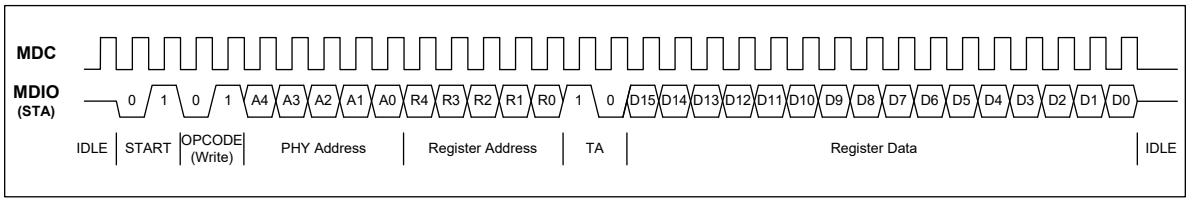


Table 38 is an example of a read operation.

Table 38: Serial Management Interface Protocol

32-Bit Preamble	Start of Frame	OpCode Read = 10 Write = 01	5-Bit PHY Device Address	5-Bit PHY Register Address (MSB)	2-Bit Turn around Read = z0 Write = 10	16-Bit Data Field	Idle
11111111	01	10	01100	00000	z0	0001001100000000	11111111

2.9.1 Extended Register Access

MDC/MDIO protocol only supports 32 registers. Since the 88E1111 device has more than 32 registers, a paging scheme is used to address more than 32 registers. The different pages might be accessed automatically based on the operating mode or they can be selected by setting bit in other registers. For example, Register 29 sets the applicable page of Register 30. Register 22 is used to select the different pages of various registers. See 3 "Register Description" on page 121 for details.

2.9.2 Preamble Suppression

The 88E1111 device is permanently programmed for preamble suppression. A minimum of one idle bit is required between operations.

2.9.3 Programming Interrupts

In the 88E1111 device, the polarity of the interrupt pin is programmable through the hardware configuration option INT_POL. The interrupt function drives high or low based on the INT_POL setting and when register 18 is enabled for an interrupt event and an interrupt is detected. This function minimizes the need for polling via the serial management interface. An external pull-up resistor is used when the INTn pin is active low. and a pull-down resistor is used when the INTn pin is active high.

Table 39 shows the interrupts that may be programmed.

Table 39: Programmable Interrupts

Register Address	Programmable Interrupts
18.15	Auto-Negotiation Error Interrupt Enable
18.14	Speed Changed Interrupt Enable
18.13	Duplex Changed Interrupt Enable
18.12	Page Received Interrupt Enable
18.11	Auto-Negotiation Completed Interrupt Enable
18.10	Link Status Changed Interrupt Enable
18.9	Symbol Error Interrupt Enable
18.8	False Carrier Interrupt Enable
18.7	FIFO Over/Underflow Interrupt Enable
18.6	MDI Crossover Changed Interrupt Enable
18.5	Downshift Interrupt Enable
18.4	Energy Detect Interrupt Enable
18.3	Reserved
18.2	DTE Power Detection Status Changed Interrupt Enable
18.1	Polarity Changed Interrupt Enable
18.0	Jabber Interrupt Enable

Register 18 determines whether the INTn pin is asserted when an interrupt event occurs. Register 19 reports interrupt status. When an interrupt event occurs, the corresponding bit in register 19 is set and remains set until register 19 is read via the serial management interface. When interrupt enable bits are not set in register 18, interrupt status bits in register 19 are still set when the corresponding interrupt events occur. However, the INTn pin is not asserted.

The INTn pin is asserted as long as one interrupt status bit is set in register 19 with its corresponding interrupt enable bit set in register 18.

To de-assert the INTn pin

- Clear register 19 via a management read
- Disable the interrupt enable by writing register 18

2.10 Two-wire Serial Interface

The 88E1111 device supports a Two-wire Serial Interface (TWSI). The TWSI operates with a serial data line (SDA) and a serial clock line (SCL). The bus interface is enabled through CONFIG6 bit 2, and, during data transfer, the MDC/MDIO pins are utilized as the bus interface connections. For the TWSI device address, the lower 5 bits (PHYADR[4:0]), are latched during hardware reset, and the device address bits ([6:5]) are fixed at '10'. The SDA is a bi-directional line, while the SCL line is not. SDA requires a 1.5 kohm pull-up resistor. The 88E1111 device operates as the Slave port of the bus interface, and all references to Slave refer to the 88E1111 device.

The 88E1111 device will be available for read/write operations 5 ms after hardware reset.

Table 40 indicates the pin mapping of the 88E1111 device to the TWSI.

Table 40: 88E1111 device to Two-Wire Serial Interface Signal Mapping

88E1111 Device Pins	100/400 Kbps Mode	Description
MDIO	SDA	Serial data line
MDC	SCL	Serial clock line

The 88E1111 device TWSI features are:

- 7-bit device address/8-bit data transfers
- 100 Kbps mode
- 400 Kbps mode

Multiple devices using the TWSI can share and lump up the MDC and MDIO lines, and are pulled up with a resistor ranging from 4.5 kohm to 10 kohm.

The 88E1111 device will be available for read/write operations 5 ms after hardware reset.

2.10.1 Bus Operation

The Master generates one clock pulse for each data bit transferred. The high or low state of the data line can only change when the clock signal on the SCL line is low. A high to low transition on the SDA line while SCL is high defines a Start. A low to high transition on the SDA line while the SCL is high defines a Stop. Start (S), Repeated Start (Sr), and Stop (P) conditions are always generated by the Master. Acknowledge (A) and Not Acknowledge ($\overline{A}$) can be generated by either the Slave or Master.

The Master continuously monitors for Start and Stop conditions. Whenever a Stop is detected, the 88E1111 device goes into standby mode, and the current operation is cancelled. The Slave recovers from this error condition, and waits for the next transfer to begin.

Data transfer with Acknowledge is always obligatory. The receiver must pull down the SDA line during the Acknowledge clock pulse so that it remains stable low during the high period of this clock pulse.

If the Slave does not Acknowledge the device address, but some time later in the transfer cannot receive any more data bytes, the Master must abort the transfer. This is indicated by the Slave generating the Not Acknowledge on the first byte to follow. The Slave device then leaves the data line high, and the Master must generate a Stop or a Repeated Start condition. When the Slave is transmitting data on the bus and the Master responds with a Not Acknowledge, the Slave must receive a Stop or a Repeated Start condition. If neither is received, it is an error condition. The Slave recovers from this error condition and waits for the next transfer to begin.

The bus interface is also active in power down mode. (See Section 2.8 "Power Management" on page 78 for power down mode details.) Whenever the Slave is addressed by the Master, the 88E1111 device comes out of power down mode if it is in power down mode. Read and Write operations are detailed in the following section.

2.10.2 Read and Write Operations

Write operations require an 8-bit Slave address followed by the register address and Acknowledgement. The Slave address is 7 bits long followed by an eighth bit. The first bit of a data transfer is the most significant bit (MSb). The eighth bit is the least significant bit (LSb), which is a direction bit (R/W) - Read = 1, Write = 0). Read operations are executed the same way as Write operations with the exception that the R/W bit is set to one.

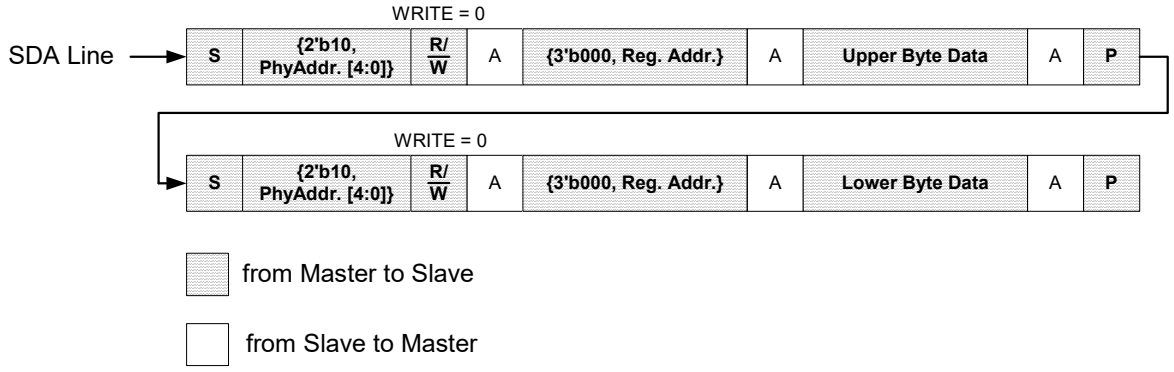
A complete byte write operation includes the upper and lower bytes. The upper byte is written first, followed by the lower byte.

The register address counter maintains the last address accessed during the last read or write operation, incremented by one. The address remains valid between operations as long as chip power is maintained. The register limit is 32 registers. Once the counter reaches the lower byte of register 31, it rolls over to the upper byte of register 0.

2.10.2.1 Random Write

For random writes, both the upper byte and lower byte must be written to the Slave before the data is written to the addressed register.

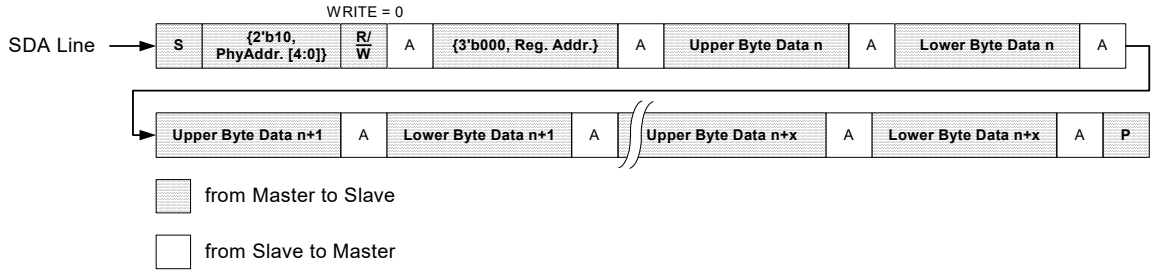
Figure 27: Random Write Operation



2.10.2.2 Sequential Write

A sequential write is started by a random address write. After the register address is received by the Slave, the Slave responds with an Acknowledge. The Slave generates an Acknowledge as long as the Master does not generate a Stop. In sequential write, only the even transfer of bytes is accepted by the 88E1111 device. If the last byte is odd, it is held internally by the Slave, but is not written to the Slave register.

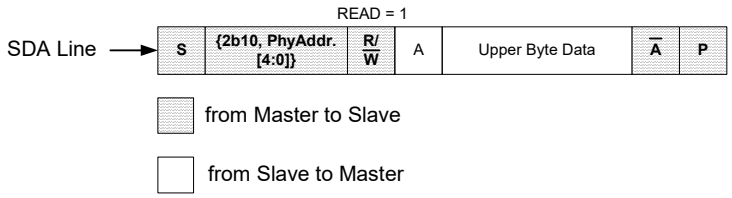
Figure 28: Sequential Write Operation



2.10.2.3 Current Address Read

A current address read is used to read the data at the current register address. A Start begins a current address read and resets the Slave to synchronize with the Master.

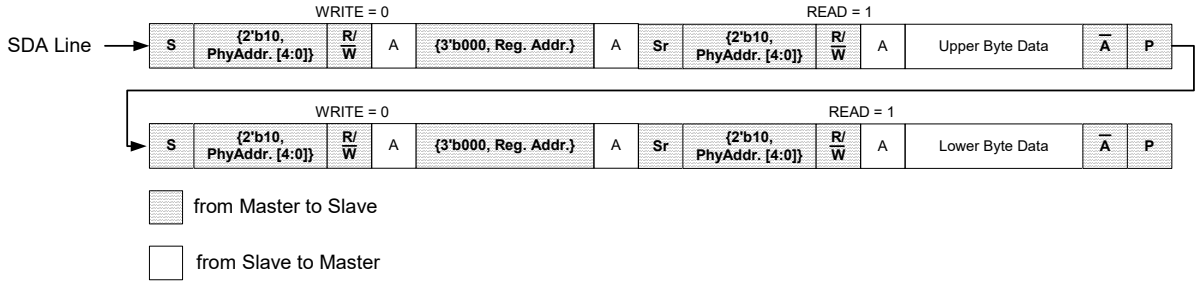
Figure 29: Current Address Read



2.10.2.4 Random Read

A random read is used to access any particular register. A “dummy” byte write is required to load in the data word address. When the device address and the data word address are Acknowledged, another Start condition must be generated. Figure 30 is an example of a random read.

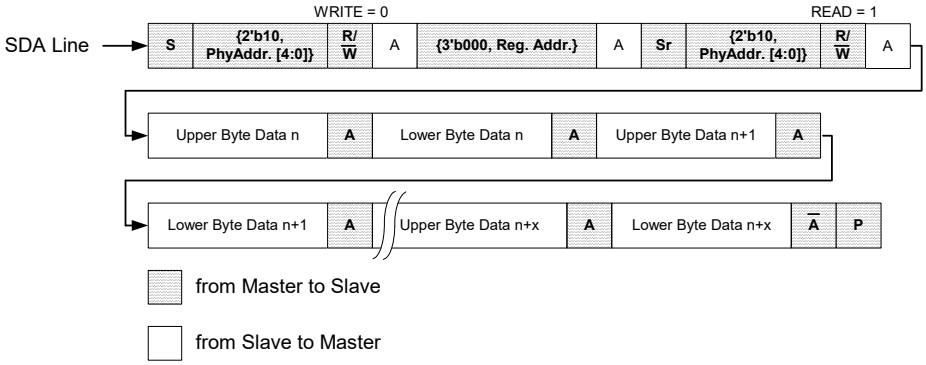
Figure 30: Random Read Operation



2.10.2.5 Sequential Read

A sequential read is used to read particular registers in their address order. A sequential read is initiated by either a current or random address read. After the Master receives the register data, it responds with an Acknowledge. As long as the Slave receives an Acknowledge, register data continues to be read incrementally. The sequential read operation is stopped when the Master does not respond with a zero, but does generate a Stop condition. Figure 31 is an example of a sequential read started by a random read.

Figure 31: Sequential Read Operation



2.11 Auto-Negotiation

The 88E1111 device supports 5 types of Auto-Negotiation.

- 10/100/1000BASE-T Copper Auto-Negotiation. (IEEE 802.3 Clauses 28 and 40)
- 1000BASE-X Auto-Negotiation (IEEE 802.3 Clause 37)
- SGMII Auto-Negotiation (CISCO specification)
- GBIC Mode Auto-Negotiation (Marvell patent)
- Auto Media Select Auto-Negotiation

Auto-Negotiation provides a mechanism for transferring information from the local station to the link partner to establish speed, duplex, and Master/Slave preference during a link session.

Auto-Negotiation for 1000BASE-X supports 1000 Mbps operation only.

Auto-Negotiation is initiated upon any of the following conditions:

- Power up reset
- Hardware reset
- Software reset (Register 0.15)
- Restart Auto-Negotiation (Register 0.9)
- Transition from power down to power up (Register 0.11)
- The link goes down

The option to select 10/100/1000BASE-T or 1000BASE-X Auto-Negotiation is determined by hardware configuration settings at RESETn and based on the digital interface being used.

The following sections describe each of the Auto-Negotiation modes in detail.

2.11.1 10/100/1000BASE-T Auto-Negotiation

The 10/100/1000BASE-T Auto-Negotiation (AN) is based on Clause 28 and 40 of the IEEE802.3 specification. It is used to negotiate speed, duplex, and flow control over CAT5 UTP cable. Once Auto-Negotiation is initiated, the 88E1111 device determines whether or not the remote device has Auto-Negotiation capability. If so, the 88E1111 device and the remote device negotiate the speed and duplex with which to operate.

If the remote device does not have Auto-Negotiation capability, the 88E1111 device uses the parallel detect function to determine the speed of the remote device for 100BASE-TX and 10BASE-T modes. If link is established based on the parallel detect function, then it is required to establish link at half-duplex mode only. Refer to IEEE 802.3 clauses 28 and 40 for a full description of Auto-Negotiation.

After hardware reset, 10/100/1000BASE-T Auto-Negotiation can be enabled and disabled via Register 0.12. Auto MDI/MDIX and Auto-Negotiation may be disabled and enabled independently. When Auto-Negotiation is disabled, the speed and duplex can be set via registers 0.13, 0.6, and 0.8 respectively. When Auto-Negotiation is enabled the abilities that are advertised can be changed via registers 4 and 9.

Auto-Negotiation options are configured using the CONFIG[2] pins, or by registers. See Section 2.4 "Hardware Configuration" on page 68 for more information.

Upon the de-assertion of hardware reset the 88E1111 device can be configured to have Auto-Negotiation enabled for all capabilities (1000BASE-T, 100BASE-TX, or 10BASE-T modes), or the device may be configured to operate in either 1000BASE-T, 100BASE-TX, or 10BASE-T modes.

Auto-Negotiation can also be configured via registers 0, 4, and 9. Changes to registers 0.12, 0.13, 0.6 and 0.8 do not take effect unless one of the following takes place:

- Software reset (Register 0.15)
- Restart Auto-Negotiation (Register 0.9)
- Transition from power down to power up (Register 0.11)
- The link goes down

To enable or disable Auto-Negotiation, Register 0.12 should be changed simultaneously with either Register 0.15 or 0.9. For example, to disable Auto-Negotiation and force 10BASE-T half-duplex mode, Register 0 should be written with 0x8000.

Registers 4 and 9 are internally latched once every time the Auto-Negotiation enters the Ability Detect state in the arbitration state machine. Hence, a write into Register 4 or 9 has no effect once the 88E1111 device begins to transmit Fast Link Pulses (FLPs).This guarantees that sequences of FLPs transmitted are consistent with one another.

Register 7 is treated in a similar way as registers 4 and 9 during additional next page exchanges.

If Auto-Media detect is enabled, Register 22.0 must be set to zero to view the copper auto-negotiation registers.

If 1000BASE-T mode is advertised, then the 88E1111 device automatically sends the appropriate next pages to advertise the capability and negotiate master/slave mode of operation. If the user does not wish to transmit additional next pages, then the next page bit (Register 4.15) can be set to zero, and the user needs to take no further action.

If next pages in addition to the ones required for 1000BASE-T are needed, then the user can set Register 4.15 to one, and send and receive additional next pages via registers 7 and 8, respectively.

Note that 1000BASE-T next page exchanges are automatically handled by the 88E1111 device without user intervention, regardless of whether or not additional next pages are sent.

Once the 88E1111 device completes Auto-Negotiation, it updates the various status in registers 1, 5, 6, and 10. Speed, duplex, page received, and Auto-Negotiation completed status are also available in registers 17 and 19. See 3 "Register Description" on page 121 for details.

2.11.2 1000BASE-X Auto-Negotiation

1000BASE-X Auto-Negotiation is defined in Clause 37 of the IEEE802.3 specification. It is used to auto-negotiate duplex and flow control over fiber cable. Registers 0, 4, 5, 6, and 15 are used to enable AN, advertise capabilities, determine link partner's capabilities, show AN status, and show the duplex mode of operation respectively.

- If HWCFG_MODE[3:0] = 0011 or 0111, Register 0_1.12 determines whether 1000BASE-X Auto-Negotiation is on or off.
- Register 4.5 and 4.6 control 1000BASE-X full-duplex and half-duplex advertisement, respectively. Bits 4.8:7 advertise flow control capabilities.
- Register 5.5 and 5.6 show link partner 1000BASE-X full-duplex/half-duplex capability.
- Register 15.14 and 15.15 show duplex status of the 88E1111 device.

If Auto-Media detect is enabled, Register 22.0 must be set to one to view the fiber auto-negotiation registers.

The 88E1111 device supports Next Page option for 1000BASE-X Auto-Negotiation when the GMII or RGMII interface are used. The 88E1111 device supports Next Pages per IEEE Clause 27 (fiber Auto-Negotiation) in the following modes:

- GMII to 1000BASE-X
- GMII to Auto-Media detection
- RGMII to 1000BASE-X
- RGMII to Auto-Media detection

Register 7 of the fiber pages is used to transmit Next Pages, and register 8 of the fiber pages is used to store the received Next Pages. The Next Page exchange occurs with software intervention. The user must set the fiber bank (Page 1) Register 4.15 to enable fiber Next Page exchange. Each Next Page received in the registers should be read before a new Next Page to be transmitted is loaded in Register 7.

2.11.3 SGMII Auto-Negotiation

SGMII is a de facto standard designed by CISCO. SGMII uses 1000BASE-X coding to send data as well as Auto-Negotiation information between the PHY and the MAC. However, the contents of the SGMII Auto-Negotiation are different than the 1000BASE-X Auto-Negotiation. See the "CISCO SGMII Specification" and the "MAC Interfaces and Auto-Negotiation" application note for further details. For 1000BASE-X operation, registers 4 and 5 are updated.

The 88E1111 device supports SGMII interface with and without Auto-Negotiation. If SGMII mode is selected, Auto-Negotiation can be enabled or disabled by writing to Register 0_1.12 (fiber bank) followed by a soft reset. If SGMII Auto-Negotiation is disabled, (0_1.12 = 0) the MAC interface link, speed, and duplex status (determined by the copper side) cannot be conveyed to the MAC from the PHY. The user must program the MAC with this information in some other way (e.g., by reading PHY registers for link, speed, and duplex status). When SGMII Auto-Negotiation is disabled in GMII/RGMII to SGMII mode, the speed of operation is determined by Register 20.5:4.

2.11.4 GBIC Mode Auto-Negotiation

GBIC Auto-Negotiation is a Marvell® proprietary feature which translates 1000BASE-X Auto-Negotiation from the MAC side to and from 10/100/1000BASE-T Auto-Negotiation on the copper side. See Section 2.3.1.6 "Serial Interface (SERDES) to Copper Modes" on page 64 for details. If GBIC mode is selected, Auto-Negotiation can be enabled and disabled by writing to Register fiber Register 0_1.12 followed by a soft reset. The GBIC mode Auto-Negotiation can also be enabled/disabled by hardware configuration strap options.

2.11.5 Auto-Media Detect Auto-Negotiation

The 88E1111 device supports two separate media interfaces: fiber interface and copper interface. It can monitor both interfaces simultaneously and establish link with whatever media is connected. In this mode of operation, the 88E1111 device simultaneously carries both 1000BASE-X and 10/100/1000BASE-T Auto-Negotiation in its two media interfaces. The first media to complete Auto-Negotiation and link up will be enabled and the other media will be powered down to save power.

Auto-Negotiation registers 4 and 5 have dual functionality. If the media of operation is copper, then they represent the 10/100/1000BASE-T Auto-Negotiation advertised capabilities and link partner's capabilities respectively. If the media of operation is fiber, they contain the 1000BASE-X Auto-Negotiation information. When Auto-Media detect is enabled, either register set can be read or written to by selecting Register 22.7:0.

2.11.6 Serial Interface Auto-Negotiation Bypass Mode

The IEEE standard Auto-Negotiation state machine, per the 802.3X Clause 37 1000BASE-X, requires that both link partners support Auto-Negotiation before link is established. If one link partner implements the Auto-Negotiation function and the other does not, two-way communication is not possible unless Auto-Negotiation is manually disabled and both sides are configured to work in the same operational modes. To solve this problem, the 88E1111 device implements the Serial Interface Auto-Negotiation Bypass Mode. The functional details of the Serial Interface Auto-Negotiation Bypass Mode for GMII/RGMII, SGMII, and GBIC modes are described in Table 41: "Serial Interface Auto-Negotiation in GMII/RGMII, SGMII, and GBIC modes" on page 91. Registers 0.12 and 27.12 must be set to 1 for the Serial Interface Auto Negotiation Bypass Mode to operate.

Note

For the GMII/RGMII and GBIC modes, Register 27.12 = 1 by default, indicating the 88E1111 device automatically enters Serial Interface Auto Negotiation Bypass Mode by default and bypasses Auto-Negotiation after 200 ms if Serial Interface Auto-Negotiation is unsuccessful.

Table 41: Serial Interface Auto-Negotiation in GMII/RGMII, SGMII, and GBIC modes

Mode	HWCFG_ MODE[3:0]	Reg. 27.12 Default Value at H/W Reset	Reg. 27.11 Status	Bypass Timer	Action Taken if Link Up due to bypass
GMII/ RGMII	0111 = GMII to fiber 0011 = RGMII to fiber	1	If Serial Interface-Aneg Enabled (0_1.12 = 1) and serial interface link is up (17.10 = 1) and: 27.11 = 1 - Link up due to bypass 27.11 = 0 - Link up due to standard Auto-Negotiation	200 ms	Full-duplex and pause bits are set to Register 4 advertised values.
SGMII	0000 = SGMII to copper with clock 0100 = SGMII to copper without clock	0	If Serial Interface-Aneg Enabled (0_1.12) and serial interface link is up (17.10 = 1) and: 27.11 = 1 - Link up due to bypass 27.11 = 0 - Link up due to standard Auto-Negotiation	200 ms	Copper Auto-Negotiation restarted with: Full-duplex =1 Half-duplex = 1 Pause = 00 Speed = 1000 Mbps only
GBIC	1000	1	N/A	200 ms (timer starts after cop-per link is up)	Copper Auto-Negotiation NOT restarted and the pause value is the copper Auto-Negotiation resolu-tion value.

The Serial Interface Auto-Negotiation discussion herein applies to the fiber side when in GMII/RGMII to fiber mode (Register 0_1.12=1), and to the MAC or serial interface side in the SGMII to copper (Register 0_1.12 =1) or in the GBIC mode (Register 0_1.12 =1). When entering the state “Ability_Detect”, a bypass timer begins to count down from an initial value of approximately 200 ms. If the 88E1111 device receives idles during the 200 ms, the 88E1111 device will interpret that the other side is “alive” but cannot send configuration codes to perform Auto-Negotiation. After 200 ms, the state machine will move to a new state called “Bypass_Link_Up” in which the 88E1111 device assumes a link-up status and the operational mode is set to the value listed under the “Action Taken if Link Up due to bypass” column of Table 41. The Serial Interface Auto-Negotiation Bypass Mode is performed if the ability_match is not asserted for the bypass timer duration. In the case where the Serial Interface Auto-Negotiation Bypass is performed, the 88E1111 device will report the bypass status via Register 27.11 together with Register 17_1.10 stating link change. Register 27.11 and 17_1.10 indicate whether the link was resumed due to standard Auto-Negotiation or bypass.

2.12 Fiber/Copper Auto-Selection

The 88E1111 device has a patented feature to automatically detect and switch between fiber and copper cable connections. The 88E1111 device monitors the signals of the serial interface lines and the MDI lines. If a fiber optic cable is plugged in, the 88E1111 device will adjust itself to be in fiber mode. If an RJ-45 cable is plugged in, the 88E1111 device will adjust itself to be in copper mode. If both cables are connected then the first media to establish link will be enabled. The media which is not enabled will turn off to save power. If the link on the first media is lost, then the inactive media will be powered up, and both media will once again start searching for link.

Depending on the media selected, the internal Auto-Negotiation register bits will reflect the copper or fiber modes. In this case, registers 1, 4, 5, 6, 17, and 19 are affected. Register 27 and Register 22 are used for the control and status of Fiber/Copper Auto-Selection. Refer to Table 103, “Extended PHY Specific Status Register,” on page 174 for details.

Fiber/Copper Auto-Selection can be enabled by either hardware configuration strap options or by register writes. For configuration strap options see Section 2.4 "Hardware Configuration" on page 68. The configuration strap option for enabling/disabling this feature can be overwritten by writing the desired bit value to Register 27.15 followed by a software reset. Once a media is selected, register access is automatically updated to that media’s registers. To disable this, set Register 27.9 = 1.

Fiber/Copper Auto-Selection requires that the configuration strap option for the MAC/media interface should be set for copper. For example, if the MAC interface is GMII, then GMII to copper mode of operation should be strapped. This can be done by setting the HWFG_MODE [3:0] = 1111. Similarly, for modes other than the GMII, the media selection should be strapped to copper. If it is required to change the mode of operation to GMII to fiber, then the Fiber/Copper Auto-Selection should be disabled by writing to Register 27.15=1. Selection of fiber or copper can be performed through software by using Register 27.3:0.

If Fiber/Copper Auto-Selection is selected, then the ANEG [3:0] strap option bits select not only the Auto-Negotiation options for the copper 10/100/1000BASE-T Auto-Negotiation, but they also affect the Fiber 1000BASE-X Auto-Negotiation.

ANEG [3:2] has to be equal to 11 to allow Fiber Auto-Negotiation to operate; however, this will also specify 10/100BASE-T capabilities for the copper side Auto-Negotiation. To not advertise 10/100BASE-T capabilities, re-program Register 4 page 0.

Fiber-copper Auto-Selection described above is not available in “Energy Detect” sleep mode. See Page 78 for a description of Energy Detect sleep mode.

When doing MAC interface loopback testing, disable auto-selection by setting Register 27.15 = 1. Loopback is enabled by setting Register 0.14 = 1.

2.12.1 Preferred Media for Fiber/Copper Auto-Selection

The 88E1111 device can be programmed to give one media priority over the other. In other words if the non-preferred media establishes link first and subsequently energy is detected on the preferred media, the PHY will drop link on the non-preferred media for 4 seconds and give the preferred media a chance to establish link. Register 26.11:10 selects the preferred media.

- 00 = Link with the first media to establish link
- 01 = Prefer fiber media
- 10 = Prefer copper media

The determination of when to switch from one media to another can also be managed under software instead of being done automatically. Register 26.11:10 can be set to 00 to not give any media any preference. The software then polls register 17_0.4 and 17_1.4 to see if energy is detected is detected on the copper or fiber media respectively. If link is already up for one media but the second media indicate energy is being detected via register 17_0.4 or 17_1.4 then the management software has the option of setting 26.11:10 to prefer the second media when it is ready. Once link is established on the second media register 26.11:10 can then be set back to 00.

Registers 19_0.4 and 19_1.4 are sticky bits that report when the energy detect on the copper or fiber media respectively has changed.

If there is a preference for one medium and it is selected, then the Energy Detect status for the other medium has no meaning. Hence, if the user wants to be able to monitor the Energy Detect status for the other medium, the preference bits in Register 26 should not be set.

Fiber media activity is determined by the Signal Detect pins (SD±). The user must program the 88E1111 device to use the external Signal Detect in Register 26.7.

2.13 Downshift Feature

Without the downshift feature enabled, connecting between two Gigabit link partners requires a four-pair RJ-45 cable to establish 10, 100, or 1000 Mbps link. However, there are existing cables that have only two-pairs, which are used to connect 10 Mbps and 100 Mbps Ethernet PHYs. With the availability of only pairs 1, 2 and 3,6, Gigabit link partners can Auto-Negotiate to 1000 Mbps, but fail to link. The Gigabit PHY will repeatedly go through the Auto-Negotiation but fail 1000 Mbps link and never try to link at 10 Mbps or 100 Mbps.

With the Marvell® downshift feature enabled, the 88E1111 device is able to Auto-Negotiate with another Gigabit link partner using cable pairs 1,2 and 3,6 to downshift and link at 10 Mbps or 100 Mbps, whichever is the next highest advertised speed common between the two Gigabit PHYs.

In the case of a three pair cable (additional pair 4,5 or 7,8 - but not both) the same downshift function for two-pair cables applies.

By default, the downshift feature is turned off. Refer to Register 20.11:8 which describe how to enable this feature and how to control the downshift algorithm parameters.

To enable the downshift feature, the following registers must be set:

- Register 20.8 = 1 - enables downshift
- Register 20.11:9 - sets the number of link attempts before downshifting

2.14. TRR Byte Stuff Blocking Feature

The TRR byte stuffing block feature is enabled by setting Register bit 20.15 to ’1’, plus a soft reset. By default this feature is disabled (Register 20.15 = 0).

2.14.1 TRR Byte Stuff Blocking in the Receive Direction

Link partners with TBI based MACs or SERDES based MACs may transmit with the extra \R\ after the \T\R\, forming the \T\R\R\ at the end of a good frame. In the RGMII or GMII modes, reception of such frames causes the RX_ER to assert one bit time after RX_DV goes low. This is normal behavior, but some MACs may discard this frame type. In the receive direction, enabling the TRR byte stuff blocking (20.15 = ‘1’) will prevent the RX_ER from asserting after the RX_DV goes low at the end of frame.

Blocking of the TRR byte stuffing in the receive direction is available for the following modes:

- RGMII to copper
- RGMII to fiber
- RGMII to SGMII
- GMII to copper
- GMII to fiber
- GMII to SGMII

2.14.2 TRR Byte Stuff Blocking in the Transmit Direction

TBI based MACs or SERDES based MACs connected to the PHY may transmit with the \T\R\R\ at the end of a frame. Enabling the TRR byte stuff blocking (20.15 = ‘1’) in the 88E1111 device will prevent the extra \R\ to be transmitted, thus only the \T\R\ at the end of the transmit frame.

Blocking of the TRR byte stuffing in the transmit direction is available for the following modes:

- SGMII to copper
- Fiber to copper

2.15 Loopback Modes

2.15.1 MAC Interface Loopback

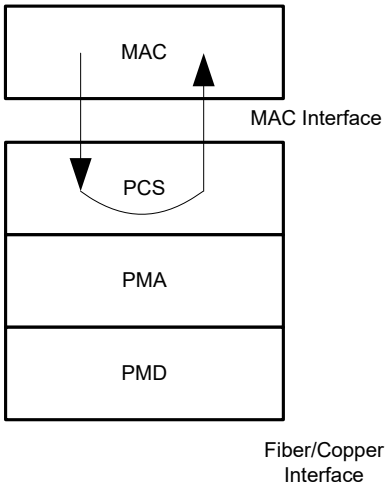
The functionality, timing, and signal integrity of the MAC interface can be tested by placing the Alaska® Ultra device in MAC interface loopback mode. This can be accomplished by setting Register 0.14 = 1. In loopback mode, the data received from the MAC is not transmitted out on the media interface. Instead, the data is looped back and sent to the MAC. For copper media, during loopback, link will be lost and packets will not be received. When performing a Register 0.14 MAC Interface loopback during a mode that uses copper medium, the copper receiver will be powered down, link will not come up and any data received will not be transferred. Idles will be transmitted out the copper transmitter.

If while auto-negotiating and loopback is enabled, FLP Auto-Negotiation codes will be transmitted. If in forced 10BASE-T mode and loopback is enabled, 10BASE-T idle link pulses will be transmitted on the copper side. If in forced 100BASE-T mode and loopback is enabled, 100BASE-T idles will be transmitted on the copper side.

When performing a Register 0.14 loopback during a mode that uses the fiber medium, the fiber transceiver will be powered up and sync status will be up if valid code groups are received. Any data received from the MAC will not be transmitted on the cable. Idles will be transmitted out the fiber transmitter.

The following sections describe the loopback speed determination for GMII/MII mode to copper, RGMII to copper, and SGMII to copper.

Figure 32: MAC Interface Loopback Diagram



2.15.1.1 Loopback when Auto-Negotiation is Enabled

If Auto-Negotiation is enabled, and link is down, the speed is determined by Register 20.6:4. A software update is required to update Register 20.6:4. Loopback can then be enabled by setting Register 0.14 = 1. For example, when Auto-Negotiation is enabled, write:

Register 20.6:4 = ’101’	MAC interface speed is set to 100 Mbps
Register 0.15 = 1	Software reset. Need to update Register 20.6:4 setting.
Register 0.14 = 1	Enable loopback

2.15.1.2 Loopback when Auto-Negotiation is Disabled

If in forced speed mode, (Auto-Negotiation is disabled), the speed is determined by setting Registers 0.6 and 0.13. A software update is required to update 0.6 and 0.13. Loopback can then be enabled by setting Register 0.14 = 1. For example, when Auto-Negotiation is disabled (MAC interface speed forced to 100 Mbps), write:

Register 0.13 = 1 Register 0.6 = 0	MAC interface speed is set to 100 Mbps
Register 0.15 = 1	Software reset. Need to update Registers 0.13 and 0.6 settings.
(e.g., Register 0 = 0xa100)	
Loopback bit setting 0x6100	
Register 0.14 = 1	Enable loopback

2.15.1.3 GBIC and SGMII Mode Loopback

For GBIC and SGMII modes, loopback may be performed as long as serial interface Auto-Negotiation is disabled.

For example, starting with a strap option of GBIC mode (HWCFG_MODE [3:0] = 1000) perform the following register writes.

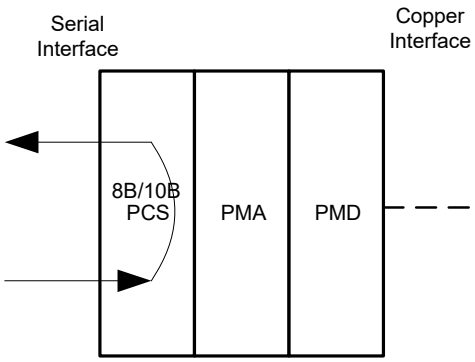
22.7:0 = 0x01	Select fiber register banks of the PHY.
Register 0.12 = 0 and 0.15 = 1	Disable Fiber Auto-Negotiation and apply soft reset.
Register 0.14 = 1	Enable loopback

To return to normal operation, perform the following register writes.

Register 0.14 = 0	Disable loopback
Register 0.12 = 1 and 0.15 = 1	Enable SERDES (or SGMII) Auto-Negotiation and apply soft reset.
22.7:0 = 0x00	Select copper register banks of the PHY.

For media converter and GBIC/SFP applications, the serial interface is treated as a MAC interface for loopback purposes.

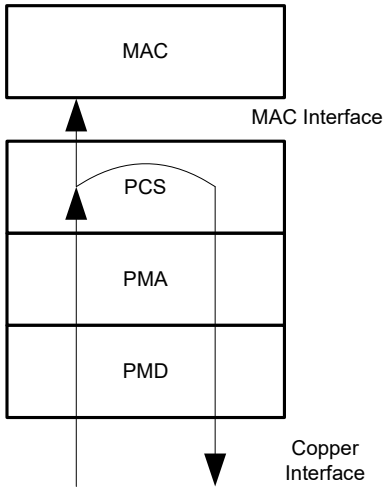
Figure 33: GBIC Loopback



2.15.2 Copper Line Loopback

Line loopback allows a link partner to send frames into the 88E1111 device to test the transmit and receive data path. Frames from a link partner into the PHY, before reaching the MAC interface pins, are looped back and sent out on the copper line. They are also sent to the MAC. The packets received from the MAC are ignored during copper line loopback. Refer to Figure 34. This allows the link partner to receive its own frames.

Figure 34: Line Loopback Data Path



Before enabling the line loopback feature, the PHY must first establish link to another PHY link partner. If Auto-Negotiation is enabled, both link partners should advertise the same speed and full-duplex. If Auto-Negotiation is disabled, both link partners need to be forced to the same speed and full-duplex. Once link is established, enable the line loopback mode by writing to Register 20.14.

- 20.14 = 1 (Enable line loopback)
- 20.14 = 0 (Disables line loopback)

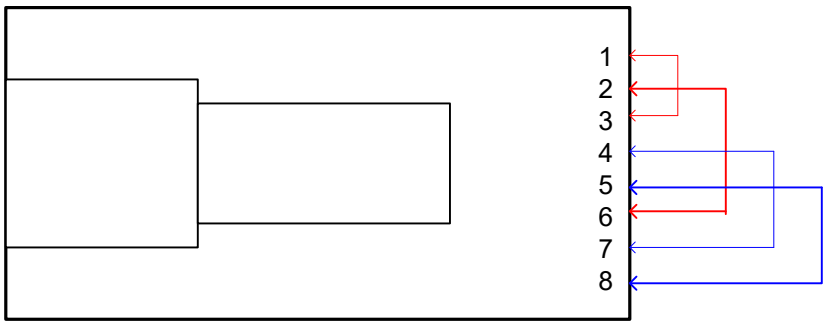
2.15.3 External 1000 Mbps Loopback

For production testing, an external loopback stub allows testing of the complete data path for 10/100/1000 Mbps modes. For 10/100 Mbps modes, the loopback test requires no register writes. For 1000 Mbps mode, a series of register writes will setup the PHY for external 1000 Mbps loopback. All modes require an external loopback stub. See the following sections and Figure 35 for details.

2.15.3.1 Loopback Stub

The loopback stub consists of a plastic RJ-45 header, connecting RJ-45 pair 1,2 to pair 3,6 and connecting pair 4,5 to pair 7,8, as seen in Figure 36.

Figure 35: Loopback Stub (Top View with Tab up)



2.15.3.2 Enabling 1000 Mbps Stub Loopback

To enable the 1000 Mbps Stub Loopback mode, write to the following registers:

Register 18 = 0x0000 (disable all interrupts)

Register 9.12:11 = '11' (force Master, e.g. reg9: 0x1B00)

Register 0.15 = '1' (e.g. reg: 0x9140, to perform softreset)

Register 29 = 0x0007 (points to page 7 of Register 30)

Register 30.3 = '1' (e.g. reg 30: 0x0808)

Register 29 = 0x0010 (points to page 16 of Register 30)

Register 30.1 = '1' (e.g. reg30: 0x0042)

Register 29 = 0x0012 (points to page 18 of Register 30)

Register 30.0 = '1' (e.g. reg30: 0x8901)

2.15.3.3 Disabling 1000 Mbps Stub Loopback

To disable the Gigabit Stub Loopback mode, restore the default settings to the related registers above.

Note Register 29 is a pointer to hidden registers.

Register 9.12:11 = Restore original values (e.g. reg9: 0x0300)

Register 0.15 = '1' (e.g. reg: 0x9140, to perform softreset)

Register 29 = 0x0007 (points to page 7 of Register 30)

Register 30.3 = '0' (e.g. reg 30: 0x0800)

Register 29 = 0x0010 (points page 16 of Register 30)

Register 30.1 = '0' (e.g. reg30: 0x0040)

Register 29 = 0x0012 (points to page 18 of Register 30)

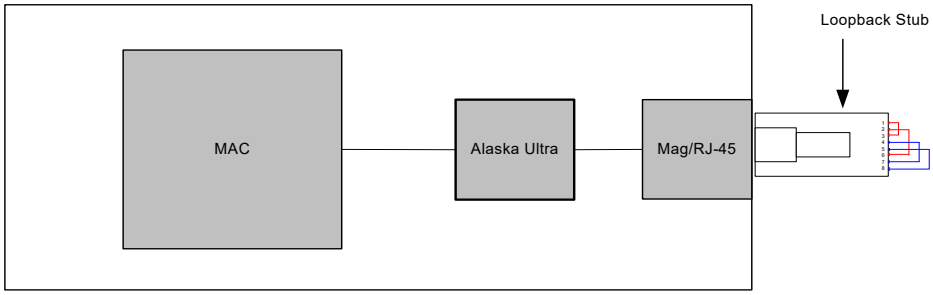
Register 30.0 = '0' (e.g. reg30: 0x8900)

Register 18 = Restore desired interrupts

2.15.3.4 External Gigabit Loopback Test Setup

The external loopback test setup requires the presence of a MAC that will originate the frames to be sent out through the PHY. Instead of a normal RJ-45 cable, the loopback stubs allows the PHY to self-link at 1000 Mbps. It also allows the actual external loopback. See Figure 36. The MAC should see the same packets it sent, looped back to it.

Figure 36: Test Setup for 10/100/1000 Mbps Modes using an External Loopback Stub



2.16 Virtual Cable Tester® (VCT™) Feature

The 88E1111 device Virtual Cable Tester® feature uses Time Domain Reflectometry (TDR) to determine the quality of the cables, connectors, and terminations. Some of the possible problems that can be diagnosed include opens, shorts, cable impedance mismatch, bad connectors, termination mismatch, and bad magnetics.

The 88E1111 device transmits a signal of known amplitude (+1V) down each of the four pairs of an attached cable. It will conduct the cable diagnostic test on each pair, testing the MDI[0], MDI[1], MDI[2], and MDI[3] pairs sequentially. The transmitted signal will continue down the cable until it reflects off of a cable imperfection. The magnitude of the reflection and the time it takes for the reflection to come back are shown in register 28.12:8 and 28.7:0 respectively.

Using the information from register 28, the distance to the problem location and the type of problem can be determined. For example, the time it takes for the reflection to come back, can be converted to distance using table on register 28 (Table 103). The polarity and magnitude of the reflection together with the distance will indicate the type of discontinuity. For example, a +1V reflection will indicate an open close to the PHY and a -1V reflection will indicate a short close to the PHY.

Register 22 is used to select which MDI pair has its results shown in Register 28.

If the cable is properly terminated and there are no discontinuities, then there will be no reflections. If there are no reflections cable length can not be determined by TDR methods. Instead, if there is good link then DSP algorithms are used to determine cable length as indicated by register 17.9:7.

When the cable diagnostic feature is activated by setting Register 28.15=1, a pre-determined amount of time elapses before a test pulse is transmitted. This is to ensure that the link partner loses link, so that it stops sending 1000BASE-T or 100BASE-TX idles or 10 Mbit data packets. This is necessary to be able to perform the TDR test. The TDR test can be performed either when there is no link partner or when the link partner is Auto-Negotiating or sending 10 Mbit idle link pulses. If the 88E1111 device receives a continuous signal for 125 ms, it will declare test failure because it cannot start the TDR test. In the test fail case, the received data is not valid. The results of the test are also summarized in register bit 28.14:13.

- 11 = Test fail (The TDR test could not be run for reasons explained above)
- 00 = valid test, normal cable (no short or open in cable)
- 10 = valid test, open in cable (Impedance > 333 ohms)
- 01 = valid test, short in cable (Impedance < 33 ohms)

The definition for shorts and opens is arbitrary and the user can define it in anyway they desire using the information in register 28. The impedance mismatch at the location of the discontinuity could also be calculated knowing the magnitude of the reflection. Refer to the App Note "Virtual Cable Tester -- How to use TDR results" for details.

When 1000BASE-T link is established, additional information about the cable can be established. Page 4 Register 28 summarizes the pair skew among the four pairs of cables.

Page 5 Register 28.3:0 report the polarity on each pair of cables, and bits 5:4 report which channel is connected to which pair of wires.

The contents on page 4 and page 5 Register 28 are only valid if Page 5 Register 28.6 is set to 1.

2.17 MDI/MDIX Crossover

The 88E1111 device automatically determines whether or not it needs to cross over between pairs as shown in Table 42 so that an external crossover cable is not required. If the 88E1111 device interoperates with a device that cannot automatically correct for crossover, the 88E1111 device makes the necessary adjustment prior to commencing Auto-Negotiation. If the 88E1111device interoperates with a device that implements MDI/MDIX crossover, a random algorithm as described in IEEE 802.3 clause 40.4.4 determines which device performs the crossover.

When the 88E1111 device interoperates with legacy 10BASE-T devices that do not implement Auto-Negotiation, the 88E1111 device follows the same algorithm as described above since link pulses are present. However, when interoperating with legacy 100BASE-TX devices that do not implement Auto-Negotiation (i.e. link pulses are not present), the 88E1111 device uses signal detect to determine whether or not to crossover.

The auto MDI/MDIX crossover function can be disabled via register 16.6:5.

The 88E1111 device is set to MDI mode by default. See ENA_XC in Hardware Configuration and register 16.6:5.

The pin mapping in MDI and MDIX modes is shown in Table 42.

Table 42: Media Dependent Interface Pin Mapping

Pin	MDI			MDIX		
	1000BASE-T	100BASE-TX	10BASE-T	1000BASE-T	100BASE-TX	10BASE-T
MDI[0]±	BI_DA±	TX±	TX±	BI_DB±	RX±	RX±
MDI[1]±	BI_DB±	RX±	RX±	BI_DA±	TX±	TX±
MDI[2]±	BI_DC±	unused	unused	BI_DD±	unused	unused
MDI[3]±	BI_DD±	unused	unused	BI_DC±	unused	unused

Note Table 42 assumes no crossover on PCB.

The MDI/MDIX status is indicated by Register 17.6. This bit indicates whether the receive pairs (3,6) and (1,2) are crossed over. In 1000BASE-T operation, the 88E1111 device can correct for crossover between pairs (4,5) and (7,8) as shown in the table above. However, this is not indicated by Register 17.6.

See Register 28 page 5 bits 5:4 for crossover status of all pairs.

2.18 Polarity Correction

The 88E1111 device automatically corrects polarity errors on the receive pairs in 1000BASE-T and 10BASE-T modes. In 100BASE-TX mode, the polarity does not matter.

In 1000BASE-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the descrambler is locked, the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

In 10BASE-T mode, polarity errors are corrected based on the detection of validly spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10BASE-T link is up. The polarity becomes unlocked when link is down.

The polarity correction status is indicated by Register 17.1. This bit indicates whether the receive pair (3,6) is polarity reversed in MDI mode of operation. In MDIX mode of operation, the receive pair is (1,2) and Register 17.1 indicates whether this pair is polarity reversed. Although all pairs are corrected for receive polarity reversal, Register 17.1 only indicates polarity reversal on the pairs described above. See Register 28 page 5 bits 3:0 for polarity status on each of the four pairs.

2.19 Data Terminal Equipment (DTE) Detect

The 88E1111 device supports the Data Terminal Equipment (DTE) power function. The DTE power function is used to detect if a link partner requires power supplied by the 88E1111 device.

The DTE power function can be enabled by writing to Register 20.2, followed by a software reset. When DTE is enabled, the 88E1111 device will first monitor for any activity transmitted by the link partner. If the link partner is active, then the link partner has power and power from the 88E1111 device is not required. If there is no activity coming from the link partner, DTE power engages, and special pulses are sent to detect if the link partner requires DTE power. If the link partner has a low pass filter (or similar fixture) installed, the link partner will be detected as requiring DTE power.

The detection of the DTE power requirement can be reported to the 88E1111 device in two ways.

- The DTE power status register (Register 27.4) immediately comes up as soon as link partner is detected as a device requiring DTE power. The 88E1111 device will continually poll this register to detect if the link partner requires DTE power.
- If the DTE power status change interrupt is enabled (Register 18.2), an interrupt can be generated if a DTE powered device is detected. The 88E1111 device will then read the DTE power status changed (Register 19.2) and the DTE power status register (Register 27.4).

If a link partner that requires DTE power is unplugged, the DTE power status (Register 27.4) will drop after a user controlled delay (default is 20 seconds - Register 27.8:5) to avoid DTE power status register drop during the link partner powering up (for most applications), since the low pass filter (or similar fixture) is removed during power up. If DTE power status drop is desired to be reported immediately, write Register 27.8:5 to 4'b0000.

For further DTE Detect details, refer to the "DTE Detect Application Note".

A detailed description of the register bits used for DTE power detection for the 88E1111 device is shown in Table 43.

Table 43: Registers for DTE Power

Register	Description
20.2 - Enable power over Ethernet detection	0 = Disable DTE detect 1 = Enable DTE detect A soft reset is required to enable this feature (0.15=1) HW reset: 0 SW reset: Update
27.4 - Power over Ethernet detection status	0 = Do not need power 1 = Need power HW reset: 0 SW reset: 0
18.2 - Power over Ethernet detection state changed interrupt enable	0 = Disable 1 = Enable HW reset: 0 SW reset: retain
19.2 Power over Ethernet detection state changed interrupt	0 = No change 1 = Changed HW reset: 0 SW reset: 0
27.8:5 DTE detect status drop	Once the PHY no longer detects that the link partner filter, the PHY will wait a period of time before clearing the power over Ethernet detection status bit (27.4). The wait time is 5 seconds multiplied by the value of these bits. Example: (5 * 0x4 = 20 seconds) Default at HW reset: 0x4 At SW reset: retain

2.20 Automatic and Manual Impedance Calibration

2.20.1 MAC Interface Calibration Circuit

The auto calibration is available for the MAC interface I/Os. The PHY runs the automatic calibration circuit with a 45 ohm impedance target by default after hardware reset. Other impedance targets are available by changing the impedance target and restarting the auto calibration through register writes. Individual NMOS and PMOS output transistors could be controlled for 22 to 55 ohm targets in various increments.

Manual NMOS and PMOS settings are available if the automatic calibration is not desired. If the PCB traces are different from 50 ohms, the output impedance of the MAC interface I/O buffers can be programmed to match the trace impedance. Users can adjust the NMOS and PMOS driver output strengths to perfectly match the transmission line impedance and eliminate reflections completely.

2.20.2 MAC Interface Calibration Register Definitions

If Register 29 = 0x0003, then Register 30 is defined as follows:

Table 44: Register 30 Page 3 - MAC Interface Calibration Definitions

Reg bit	Function	Setting description	Mode	HW Reset	SW Reset
15	Restart Calibration	0 = Normal 1 = Restart Bit 15 is a self-clearing register. Calibration will start once the register is cleared.	R/W	0	Retain
14	Calibration Complete	0 = Calibration in progress 1 = Calibration complete	RO	0	Retain
13	Reserved	0	R/W	0	Retain
12:8	PMOS Value	00000 = All fingers off 11111 = All fingers on The automatic calibrated values are stored here after calibration completes. Once the LATCH bit is set to 1, the new calibration value is written. The automatic calibrated value is lost.	R/W	Auto calibrated value	Retain
7	Reserved	0	R/W	0	Retain
6	Latch	1 = Latch in new value. This bit self clears. (Used for manual settings)	R/W, SC	0	Retain
5	PMOS/NMOS select	0 = NMOS value is written when LATCH is set to 1 1 = PMOS value is written when LATCH is set to 1	R/W	0	Retain

Table 44: Register 30 Page 3 - MAC Interface Calibration Definitions

Reg bit	Function	Setting description	Mode	HW Reset	SW Reset
4:0	NMOS Value	00000 = All fingers off 11111 = All fingers on The automatic calibrated values are stored here after calibration completes. Once the LATCH bit is set to 1, the new calibration value is written. The automatic calibrated value is lost.	R/W	Auto calibrated value	Retain

Table 45: Miscellaneous Control
Page 18, Register 30

Bits	Field	Description	Mode	HW Rst	SW Rst
15:12	Reserved	These bits must be read and left unchanged when performing a write.	RW	0x8	Retain
11:9	Calibration PMOS Target Impedance	000 = 52 ohm 001 = 45 ohm 010 = 36 ohm 011 = 32 ohm 100 = 30 ohm 101 = 25 ohm 110 = 24 ohm 111 = 22 ohm	RW	0x1	Retain
8:6	Calibration NMOS Target Impedance	000 = 56 ohm 001 = 43 ohm 010 = 39 ohm 011 = 33 ohm 100 = 29 ohm 101 = 27 ohm 110 = 24 ohm 111 = 23 ohm	RW	0x1	Retain
5:2	Packet Generator	Bit 5: 1 = Packet generation enable, 0 = Disable Bit 4: 0 = Random, 1 = 0x5a (packet pattern select) Bit 3: 0 = 64 byte, 1 = 1518 byte (packet length select) Bit 2: 1 = Generate error packet, 0 = No error	RW	0x00	Retain
1	Reserved	These bits must be read and left unchanged when performing a write.	RW	0x00	Retain
0	Turn off NEXT Canceller	0 = Enable NEXT 1 = Disable NEXT	RW	0x0	Retain

2.20.3 Changing Auto Calibration Targets

The PHY runs the automatic calibration circuit with a 45 ohm impedance target by default after hardware reset. Other impedance targets are available by changing the impedance target and restarting the auto calibration through register writes.

To change the auto calibration targets, write to the following registers:

Write to register 29 = 0x0012

Write to register 30, bit 11:9 = ppp (write new PMOS Target value)

Write to register 30, bit 8:6 = nnn (write new NMOS Target value)

Write to register 29 = 0x0003

Write to register 30 = 0x8000 (Restarts the auto calibration with the new target)

Example: To set the approximate 55 ohm auto calibration target, write the following:

Reg29 = 0x0012

Reg30, bit 11:9 = '000' and bit 18:6 = '000'

Reg29 = 0x0003

Reg30 = 0x8000

2.20.4 Manual Settings to The Calibration Registers

To use manual calibration, write to the following registers:

Write to register 29 = 0x0003

Write to register 30 = b'000P PPPP 011N NNNN -- adjusts PMOS strength

Write to register 30 = b'000P PPPP 010N NNNN -- adjusts NMOS strength

Where PPPPP is the 5 bit value for the PMOS strength.

Where NNNNN is the 5 bit value for the NMOS strength.

The value of PPPPP or NNNNN will depend on your board. The '11111' value enables all fingers for maximum drive strength, for minimum impedance. The '00000' value turns all fingers off for minimum drive strength, for maximum impedance. Use a scope to monitor the RX_CLK pin close to the destination. Start with the default auto-calibrated value and move in each direction to see how it affects signal integrity on your board.

Example: The automatic calibration has a 50 ohm target, but if the GMII trace impedance on board was 60 ohms, you see reflections from a scope capture taken at the destination. See Figure 39. After manual calibration, you see that the reflections are eliminated in Figure 40.

Figure 37 and Figure 38 display the trend line for 2.5V PMOS and NMOS impedance settings.

Note

The trend lines displayed in Figure 37 and Figure 38 use nominal values and may vary in production.

Figure 37: PMOS Output Impedance (2.5V) Trend Line

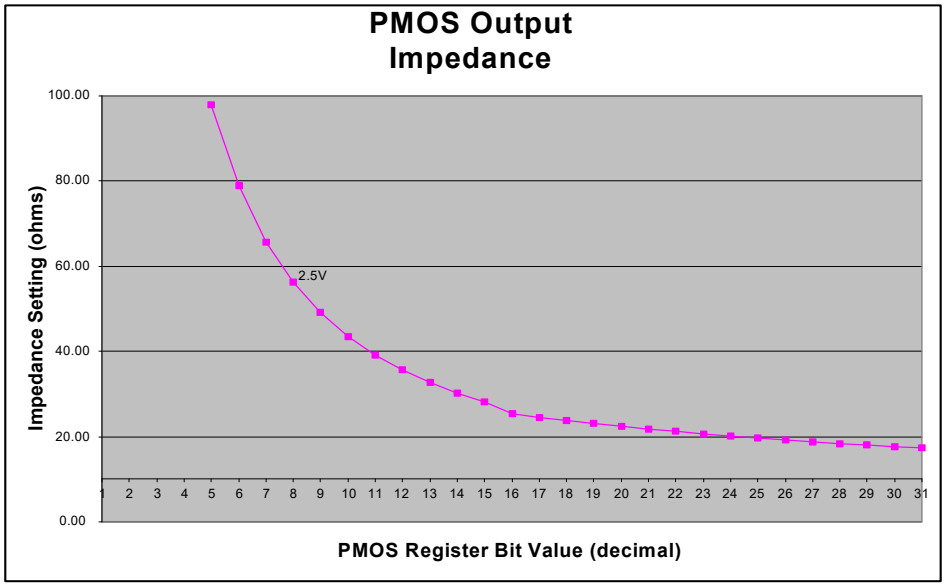
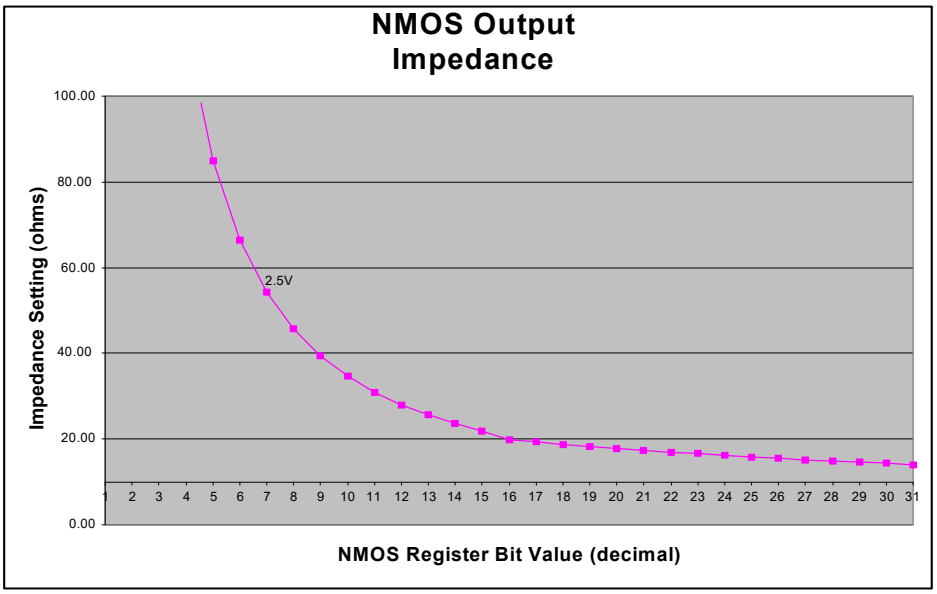


Figure 38: NMOS Output Impedance (2.5V) Trend Line



Example: The automatic calibration has a 50 ohm target, but if the GMII trace impedance on board was 60 ohms, you see reflections from a scope capture taken at the destination. Refer to Figure 39. After manual calibration, you see that the reflections are eliminated as in Figure 40.

Figure 39: Signal Reflections, using the 50 ohm Setting, 60 ohm line

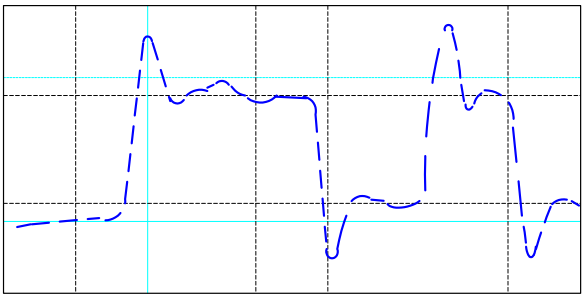
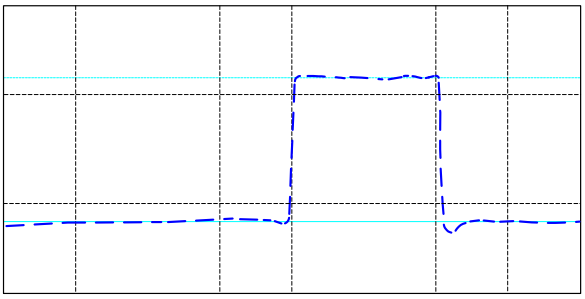


Figure 40: Clean signal after manual calibration for the 60 ohm



2.21 Packet Generator

The 88E1111 device contains a very simple packet generator. When enabled the transmit data from the MAC is ignored. Link should be established first prior to enabling the packet generator. The generator will generate packets at the speed of the established link.

Once enabled, fixed length packet of 64 or 1518 byte frame (including CRC) will be transmitted continuously separated by 12 bytes of IPG. The preamble length will be 8 bytes. The payload of the frame is either a fixed 5A, A5, 5A, A5 pattern or a pseudo random pattern. A correct IEEE CRC is appended to the end of the frame. An error packet can also be generated.

The registers are as follows:

If Register 30 page 18:

Bit 5: 1 = Packet generation enable, 0 = disable

Bit 4: 0 = Random, 1 = 0x5a (packet pattern select)

Bit 3: 0 = 64 byte, 1 = 1518 byte (packet length select)

Bit 2: 1 = Generate error packet, 0 = no error

2.22 CRC Error Counter and Frame Counter

The CRC counter and frame counters, normally found in MACs, are available in the 88E1111 device. The error counter and frame counter features are enabled through register writes and each counter is stored in eight register bits.

2.22.1 Enabling The CRC Error Counter and Frame Counter

2.22.1.1 Enabling Counters

Write to the following registers will enable both counters.

Register 29: 0x0010 (points to page 16 of Register 30)

Register 30.0 = 1 (enables both CRC error and frame counter)

2.22.1.2 Disabling and Clearing Counters

Write to the following register will disable and clear both counters.

Register 29: 0x0010 (points to page 16 of Register 30)

Register 30.0 = 0 (disable and clear CRC error and frame counter)

2.22.1.3 Reading Counter Contents

To read the CRC counter and frame counter, write to the following registers.

Register 29: 0x000C (points to page 12 of Register 30)

Register 30: bits 15:8 (Frame count is stored in these bits), bits 7:0 (CRC error count is stored in these bits)

The counter does not clear on a read command. To clear the CRC error counter, disable and enable the counters. See Page 12 of Register 30 for details.

2.22.1.4 Copper versus Fiber CRC Checking and Packet Counting

CRC error checking is done on the received packets and not on transmitted packets. Packet counting is done on the packets received from the media.

In GMII/RGMII to fiber modes, CRC checking will check for errors in packets received from the fiber media.

In media converter, GBIC and SFP applications, the CRC checking is done only on the packets received from the copper media.

In GMII/RGMII/TBI/RTBI/SGMII to copper modes, the CRC checking is done on the packets received from the copper media.

2.23 LED Interface

The LED interface consists of 6 pins: LED_LINK10, LED_LINK100, LED_LINK1000, LED_DUPLEX, LED_RX, and LED_TX. The LEDs can either be controlled by the PHY or controlled manually, independent of the state of the PHY. Manual control is achieved by writing to Register 25. Any one of the LEDs can be controlled independently of the other LEDs (i.e. one LED can be externally controlled while another LED can be controlled by the state of the PHY).

2.23.1 Manual LED Control

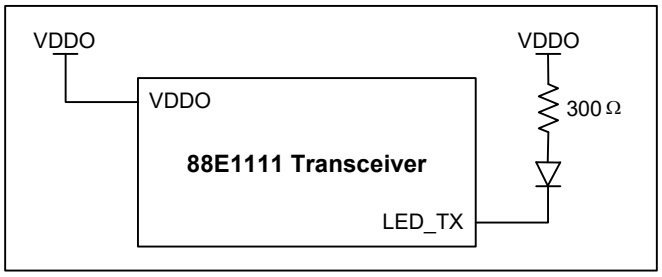
Independent of the state of the PHY, any of the LEDs can be turned on, off, or made to blink at variable rates. This can be achieved by writing 11, 10, or 01 respectively to the register 25 bits [11:0], which control manual LED operation for each of the six LEDs. This eliminates the need for driving LEDs manually from the MAC or the CPU. If LEDs are driven from the CPU located at the back of the board, the LED lines crossing the entire board will pick up noise. This noise will cause EMI issues. Also, the PCB layout will be more difficult due to the additional lines routed across the board.

2.23.1.1 LED Connections

The LEDs can be used either in single LED mode, or bi-color LED mode.

Single LED connection is shown in Figure 41 below. The LED outputs are low active. The positive terminal of the LED should be pulled up to VDDO with a 300 ohm pull-up resistor. The negative terminal should be tied to the LED pin.

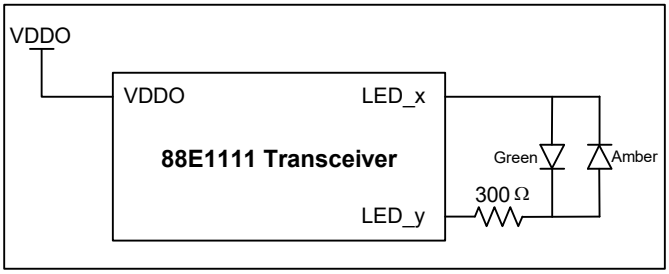
Figure 41: Single LED Connection



The bi-color LED connection in shown in Figure 42. Any two LED output pins can be chosen to implement the desired bi-color functionality. The LED functionality of the individual LED pins is described in the following sections. The LED pins and modes should be chosen such that the combined functionality of the individual LEDs will give the desired bi-color LED behavior. For example, if it is desired to have the green LED to indicate 100 Mbps speed, while the amber LED indicates 1000 Mbps speed, the following connections should be made.

- LED_LINK1000 tied to the negative terminal of the amber colored LED (LED_x).
- LED_LINK100 tied to the negative terminal of the green colored LED (LED_y).

Figure 42: Bi-Color LED Connection



2.23.2 LED Functionality

If the LEDs are controlled by the PHY, then the activity of the LEDs is determined by the state of the PHY. Each LED can be programmed to indicate various PHY states, with variable blink rate. There are four modes of link LED operation when the LEDs are controlled by the state of the PHY.

- Register 24.5:3 = 000 (Direct LED mode)
- Register 24.5:3 = 001, 010, 011, 100, 111 (Combined LED modes. There are three different combined LED modes as described below.)

2.23.2.1 Direct Drive Link LED Mode

When register 24.5:3 = ‘000’, LED output is in direct drive LED mode.

Table 46: LED_LINK Control for Register 24.5:3 = ‘000’ (Default)

88E1111 Device Pins	LED Output Level
LED_LINK10	Low = 10 Link Up High = 10 Link Down
LED_LINK100	Low = 100 Link Up High = 100 Link Down
LED_LINK1000	Low = 1000 Link Up High = 1000 Link Down

2.23.2.2 Combined Link LED Modes

There are three combined link LED modes.When register 24.5:3 = ‘011’, LED output is shown in Table 47.

Table 47: LED_Link Control Register 24.5:3 = 011

88E1111 Device Pins			Selected Speed	Link Status
LED_LINK1000	LED_LINK100	LED_LINK10		
High	High	High	Any Speed	Link down
High	High	Low	10 Mbps	Link up
High	Low	High	100 Mbps	Link up
Low	High	High	1000BASE-T (slave)	Link up
Low	High	Low	1000BASE-T (master)	Link up
Low	High	High	1000BASE-X	Link up

When register 24.5:3 = ‘001’, LED output is shown in Table 48. In this mode, LED_LINK1000 pin is used as a global link indicator.

Table 48: LED_Link Control for Register 24.5:3 = ‘001’

88E1111 Device Pins			Selected Speed	Link Status
LED_LINK1000	LED_LINK100	LED_LINK10		
Low	Low	Low	1000 Mbps	Link up
Low	Low	High	100 Mbps	Link up
Low	High	Low	10 Mbps	Link up
High	High	High	Any speed	Link down

When register 24.5:3 = ‘010’, LED output is shown in Table 49.

Table 49: LED_LINK Control for Register 24.5:3 = ‘010’

88E1111 Device Pins			Selected Speed	Link Status
LED_LINK1000	LED_LINK100	LED_LINK10		
Low	High	Low	1000 Mbps	Link up
High	Low	Low	100 Mbps	Link up
High	High	Low	10 Mbps	Link up
High	High	High	Any speed	Link Down

When register 24.5:3 = ‘100’, LED output is shown in Table 50.

Table 50: LED_LINK Control for Register 24.5:3 = ‘100’

88E1111 Device Pins			Selected Speed	Link Status
LED_LINK1000	LED_LINK100	LED_LINK10		
Low	High	High	1000 Mbps Link AND not in GMII/RGMII to 1000BASE-X mode	Link up
High	Low	High	100 Mbps	Link up
High	High	Low	10 Mbps	Link up
High	High	High	Any speed	Link Down

When register 24.5:3 = ‘111’, LED output is shown in Table 51.

Table 51: LED_LINK Control for Register 24.5:3 = ‘111’

88E1111 Device Pins			Selected Speed	Link Status
LED_LINK1000	LED_LINK100	LED_LINK10		
Low	Low	High	1000 Mbps Link (1000BASE-X)	Link
Low	High	Low	1000 Mbps Link (Master)	Link up
Low	High	High	1000 Mbps Link (Slave)	Link up
High	Low	High	100 Mbps	Link up
High	High	Low	10 Mbps	Link up
High	High	High	Any speed	Link Down

2.23.2.3 Duplex, RX, and TX LEDs

The LED outputs for the LED_DUPLEX, and LED_TX pins are programmed by setting the bits in the LED Control register. There are eight LED programming combinations available.

The tables below shows the LED Control register bit settings and the corresponding functionality of the LED_DUPLEX, and LED_TX LEDs.

Table 52: LED Output for LED_DUPLEX pins

Register 24.2	Register 24.7	LED_DUPLEX pin LED Indication
0	0	Low = Full-duplex High = Half-duplex Blink = Collision
1	0	Low = Full-duplex High = Half-duplex
0	1	Low = Fiber link up High = Fiber lin down
1	1	Reserved

Table 53: LED outputs for LED_RX pins

Register 24.1	LED_RX pin LED Indication
0	Receive Activity Low = Receiving High = Not Receiving
1	Receive Activity/Link Low = Link Up High = Link Down Blink = Receiving

Table 54: LED outputs for LED_TX pins

Register 24.6	Register 24.0	LED_TX pin LED Indication
0	0	Low = Transmitting High = Not Transmitting
0	1	Low = Link Up High = Link Down BLINK = Transmitting or Receiving
1	0	LOW = Transmitting or Receiving HIGH = Not Transmitting or Receiving
1	1	HIGH = Not Transmitting or Receiving BLINK = Transmitting or Receiving

2.23.2.4 LED Pulse Stretching and Blink Rate

Some of the statuses can be pulse-stretched. Pulse stretching is necessary, because the duration of these status events may be too short to be observable on the LEDs. The pulse-stretch duration can be programmed via register 24.14:12. The default pulse-stretch duration is set to 170 to 340 ms. The pulse-stretch duration applies only to the applicable LEDs as described next.

Pulse stretching only applies to Duplex pin in Collision mode, or LED_RX and LED_TX pins (not applicable to Link, Speed, and Duplex signals).

Some of the statuses indicate multiple events by blinking LEDs. The blink period can be programmed via register 24.10:8. The default blink period is set to 84 ms. Blink rate only applies to Duplex pin in Collision mode, LED_RX and LED_TX pins (not applicable to Link, Speed, and Duplex signals). The Blink rate defines the frequency at which an LED blink

2.24 IEEE 1149.1 Controller

The IEEE 1149.1 standard defines a test access port and boundary-scan architecture for digital integrated circuits and for the digital portions of mixed analog/digital integrated circuits.

The standard provides a solution for testing assembled printed circuit boards and other products based on highly complex digital integrated circuits and high-density surface-mounting assembly techniques.

The 88E1111 device implements 5 basic instructions: bypass, sample/preload, extest, clamp, HIGH-Z, and ID CODE. Upon reset, ID_CODE instruction is selected. The instruction opcodes are shown in Table 55.

Table 55: TAP Controller Op Codes

Instruction	OpCode
EXTEST	00000000
SAMPLE/PRELOAD	00000001
CLAMP	00000010
HIGH-Z	00000011
BYPASS	11111111
ID CODE	00000100

The 88E1111 device reserves 5 pins called the Test Access Port (TAP) to provide test accessTest Mode Select Input (TMS), Test Clock Input (TCK), Test Data Input (TDI), and Test Data Output (TDO), and Test Reset Input (TRSTn). To ensure race-free operation all input and output data is synchronous to the test clock (TCK). TAP input signals (TMS and TDI) are clocked into the test logic on the rising edge of TCK, while output signal (TDO) is clocked on the falling edge. For additional details refer to the IEEE 1149.1 Boundary Scan Architecture document.

2.24.1 Bypass Instruction

The bypass instruction uses the bypass register. The bypass register contains a single shift-register stage and is used to provide a minimum length serial path between the TDI and TDO pins of the 88E1111 device. This allows rapid movement of test data to and from other testable devices in the system.

2.24.2 Sample/Preload Instruction

The sample/preload instruction allows scanning of the boundary-scan register without causing interference to the normal operation of the 88E1111 device. Two functions are performed when this instruction is selected: sample and preload.

Sample allows a snapshot to be taken of the data flowing from the system pins to the on-chip test logic or vice versa, without interfering with normal operation. The snapshot is taken on the rising edge of TCK in the *Capture-DR* controller state, and the data can be viewed by shifting through the component's TDO output.

While sampling and shifting data out through TDO for observation, preload allows an initial data pattern to be shifted in through TDI and to be placed at the latched parallel output of the boundary-scan register cells that are connected to system output pins. This ensures that known data is driven through the system output pins upon entering the extest instruction. Without preload, indeterminate data would be driven until the first scan sequence is complete. The shifting of data for the sample and preload phases can occur simultaneously. While data capture is being shifted out, the preload data can be shifted in.

2.25 88E1111 Device Boundary Scan Chain Order

Table 56: Boundary Scan Chain Order

One scan chain is available for the 88E1111 device.

Pin	I/O
RESETn	Input
125CLK	Output
CONFIG[6]	Input
CONFIG[5]	Input
COMA	Input
TXD7	Input
TXD6	Input
TXD5	Input
TXD4	Input
TXD3	Input
TXD2	Input
TXD1	Input
TXD0	Input
TX_EN	Input
GTX_CLK	Input
TX_ER	Input
TX_CLK	Output
CRS	Output
COL_IN	Input
COL_OUT	Output
COL_OEN	Output enable for COL
RX_ER	Output
RX_CLK	Output
RX_DV	Output
RXD0	Output
RXD1	Output
RXD2	Output
RXD3	Output
RXD4	Output
RXD5	Output
RXD6	Output
RXD7	Output
G_OEN	Output enable for TX_CLK, CRS, COL, RX_ER, RX_DV, RXD[7:0], RX_CLK
MDC	Input
MDIO	Input

Table 56: Boundary Scan Chain Order (Continued)
One scan chain is available for the 88E1111 device.

Pin	I/O
MDIO	Output
MDIO_EN	Output enable for MDIO
INTn	Output
INTn_EN	Output enable for INTn
LED_LINK10	Output
LED_LINK100	Output
LED_LINK1000	Output
LED_DUPLEX	Output
LED_RX	Output
LED_TX	Output
LED_OEN	Output enable for LED
CONFIG[0]	Input
CONFIG[1]	Input
CONFIG[2]	Input
CONFIG[3]	Input
CONFIG[4]	Input

2.25.1 Extest Instruction

The extest instruction allows circuitry external to the 88E1111 device (typically the board interconnections) to be tested. Prior to executing the extest instruction, the first test stimulus to be applied is shifted into the boundary-scan registers using the sample/preload instruction. Thus, when the change to the extest instruction takes place, known data is driven immediately from the 88E1111 device to its external connections.

2.25.2 The Clamp Instruction

The clamp instruction allows the state of the signals driven from component pins to be determined from the boundary-scan register while the bypass register is selected as the serial path between TDI and TDO. The signals driven from the component pins will not change while the clamp instruction is selected.

2.25.3 The HIGH-Z Instruction

The HIGH-Z instruction places the component in a state in which all of its system logic outputs are placed in an inactive drive state (e.g., high impedance). In this state, an in-circuit test system may drive signals onto the connections normally driven by a component output without incurring the risk of damage to the component.

2.25.4 ID CODE Instruction

The ID CODE contains the manufacturer identity, part and version.

Table 57: ID CODE

Version	Part Number	Manufacturer Identity	
Bit 31 to 28	Bit 27 to 12	Bit 11 to 1	0
0000	0000 0000 0000 0000	001 1110 1001	1

3 Register Description

The IEEE defines only 32 registers address space for the PHY. In order to extend the number of registers address space available a paging mechanism is used. For register address 0 to 21, and 23 to 28 register 22 bits 7 to 0 are used to specify the page. For registers 30 and 31 register 29 bits 5:0 are used to specify the page. There is no paging for registers 22 and 29.

In this document, the short hand used to specify the registers take the form register_page.bit:bit, register_page.bit, register.bit:bit, or register.bit.

For example:

Register 0 page 1 bits 5 to 2 is specified as 0_1.5:2.

Register 0 page 1 bits 5 is specified as 0_1.5.

Register 2 bit 3 to 0 is specified as 2.3:0.

Note that In this context the setting of the page register (register 22) has no effect.

Register 2 bit 3 is specified as 2.3.

Note that in order for the paging mechanism to work correctly register 22.15 must be set to 0 to disable the automatic medium register selection.

Figure 43: Register Map Summary

Register Address	Page Address: Page 0 (Copper)	Page Address: Page 1 (Fiber)
0	Control Register	Control Register
1	Status Register	Status Register
2	PHY Identifier	
3	PHY Identifier	
4	Auto-Neg Advertisement Register	Auto-Neg Advertisement Register
5	Link Partner Ability Register	Link Partner Ability Register
6	Auto-Neg Expansion Register	Auto-Neg Expansion Register
7	Next Page Transmit Register	Next Page Transmit Register
8	Link Partner Next Page Register	Link Partner Next Page Register
9	1000BASE-T Control Register	
10	1000BASE-T Status Register	
11	Reserved Register	
12	Reserved Register	
13	Reserved Register	
14	Reserved Register	
15	Extended Status Register	
16	PHY Specific Control Register	
17	PHY Specific Status Register	PHY Specific Status Register
18	Interrupt Enable Register	Interrupt Enable Register
19	Interrupt Status Register	Interrupt Status Register
20	Extended PHY Specific Control Register	
21	Receive Error Counter Register	
22	Extended Address Register	
23	Global Status Register	
24	LED Control Register	
25	Manual LED Override Register	
26	Extended PHY Specific Control 2 Register	
27	Extended PHY Specific Status Register	
28	MDI[0:3] Virtual Cable Tester™ Status (Pages 0-3); 1000BASE-T Pair Skew (Page 4); 100BASE-T Pair, 1000BASE-T Pair Swap and Polarity (Page 5)	
29	Extended Address	
30	Calibration Override (Page 3); Force Gigabit (Page7); Class A (Page 11); CRC Checker result (Page 12); Test Enable Control (Page 16); Miscellaneous Control (Page 18)	
31	Reserved Register	

Table 58: Register Map

Register Name	Register Address	Table and Page
Control Register - Copper	Page 0, Register 0	Table 59, p. 125
Control Register - Fiber	Page 1, Register 0	Table 60, p. 130
Status Register - Copper	Page 0, Register 1	Table 61, p. 133
Status Register - Fiber	Page 1, Register 1	Table 62, p. 135
PHY Identifier	Page Any, Register 2	Table 63, p. 136
PHY Identifier	Page Any, Register 3	Table 64, p. 136
Auto-Negotiation Advertisement Register - Copper	Page 0, Register 4	Table 65, p. 137
Auto-Negotiation Advertisement Register - Fiber (GMII/RGMII Mode)	Page 1, Register 4	Table 66, p. 141
Auto-Negotiation Advertisement Register - (SGMII to Copper Modes) (Mode = 0x00)	Page 1, Register 4	Table 67, p. 143
Auto-Negotiation Advertisement Register - Fiber (SGMII to R-GMII Modes) (Mode = x110)	Page 1, Register 4	Table 68, p. 143
Auto-Negotiation Advertisement Register - Fiber (GBIC Mode) (Mode = 1000)	Page 1, Register 4	Table 69, p. 144
Link Partner Ability Register - Base Page, Copper	Page 0, Register 5	Table 70, p. 144
Link Partner Ability Register - Base Page, Fiber (RGMII or GMII Modes)	Page 1, Register 5	Table 71, p. 146
Link Partner Ability Register - Base Page, Fiber (SGMII to Copper Modes) (Mode = 0x00)	Page 1, Register 5	Table 72, p. 147
Link Partner Ability Register - Base Page, Fiber (SGMII to R-GMII Modes) (Mode = x110)	Page 1, Register 5	Table 73, p. 147
Link Partner Ability Register - Base Page, Fiber (GBIC Mode) (Mode = 1000)	Page 1, Register 5	Table 74, p. 148
Auto-Negotiation Expansion Register - Copper	Page 0, Register 6	Table 75, p. 148
Auto-Negotiation Expansion Register - Fiber	Page 1, Register 6	Table 76, p. 149
Next Page Transmit Register - Copper	Page 0, Register 7	Table 77, p. 150
Next Page Transmit Register - Fiber	Page 1, Register 7	Table 78, p. 150
Link Partner Next Page Register - Copper	Page 0, Register 8	Table 79, p. 151
Link Partner Next Page Register - Fiber	Page 1, Register 8	Table 80, p. 151
1000BASE-T Control Register	Page 0, Register 9	Table 81, p. 152
1000BASE-T Status Register	Page 0, Register 10	Table 82, p. 154
Reserved Registers	Page Any, Register 11	Table 83, p. 155
Reserved Registers	Page Any, Register 12	Table 84, p. 155
Reserved Registers	Page Any, Register 13	Table 85, p. 155
Reserved Registers	Page Any, Register 14	Table 86, p. 155
Extended Status Register	Page Any, Register 15	Table 87, p. 156
PHY Specific Control Register	Page Any, Register 16	Table 88, p. 157
PHY Specific Status Register - Copper	Page 0, Register 17	Table 89, p. 159
PHY Specific Status Register - Fiber	Page 1, Register 17	Table 90, p. 160
Interrupt Enable Register	Page 0, Register 18	Table 91, p. 161
Interrupt Enable Register - Fiber	Page 1, Register 18	Table 92, p. 162

Table 58: Register Map (Continued)

Register Name	Register Address	Table and Page
Interrupt Status Register	Page 0, Register 19	Table 93, p. 163
Interrupt Status Register	Page 1, Register 19	Table 94, p. 164
Extended PHY Specific Control Register	Page Any, Register 20	Table 95, p. 165
Receive Error Counter Register	Page Any, Register 21	Table 96, p. 167
Extended Address	Page Any, Register 22	Table 97, p. 168
Global Status Register	Page Any, Register 23	Table 99, p. 170
LED Control Register	Page Any, Register 24	Table 100, p. 170
Manual LED Override Register	Page Any, Register 25	Table 101, p. 171
Extended PHY Specific Control 2 Register	Page Any, Register 26	Table 102, p. 172
Extended PHY Specific Status Register	Page Any, Register 27	Table 103, p. 174
MDI[0] Virtual Cable Tester® Status Register, Page 0	Page 0, Register 28	Table 104, p. 176
MDI[1] Virtual Cable Tester® Status Register, Page 1	Page 1, Register 28	Table 105, p. 176
MDI[2] Virtual Cable Tester® Status Register, Page 2	Page 2, Register 28	Table 106, p. 177
MDI[3] Virtual Cable Tester® Status Register, Page 3	Page 3, Register 28	Table 107, p. 177
1000 BASE-T Pair Skew Register, Page 4	Page 4, Register 28	Table 108, p. 178
1000 BASE-T Pair Swap and Polarity, Page 5	Page 5, Register 28	Table 109, p. 179
Extended Address	Page Any, Register 29	Table 110, p. 179
Extended Registers	Pages 3, 7, 11, 12, 16, and 18 of Register 30	Table 114, p. 181
Reserved Registers	Page Any, Register 31	Table 117, p. 182

Table 59: Control Register - Copper
Page 0, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reset	R/W, SC	0x0	SC	PHY Software Reset. Writing a 1 to this bit causes the PHY state machines to be reset. When the reset operation is done, this bit is cleared to 0 automatically. The reset occurs immediately. This bit is identical to 0_1.15. 1 = PHY reset 0 = Normal operation
14	Loopback	R/W	0x0	0x0	When loopback is activated, the transmitter data presented on TXD is looped back to RXD internally. Link is broken when loopback is enabled. Loopback speed is determined by the mode the device is in Registers 20.6:4. In TBI Mode, this bit is set when the COL pin samples a rising edge after the RESET pin is deasserted. It is reset when the COL pin samples a falling edge. In all Copper modes, the loopback speed is determined by Register 20[6:4] if copper Auto-Negotiation is enabled. If copper Auto-Negotiation is disabled, the loopback speed is determined by speed set in register 0.6 and 0.13 In GMII or RGMII to Fiber Modes the loopback speed is set to 1000 Mbps. In SGMII to GMII or RGMII Modes, the loopback speed is set to SGMII Link partner advertised speed (which is the SGMII Link partners Copper Link speed) if fiber Auto-Negotiation is enabled.' If fiber Auto-Negotiation is disabled, the loopback speed is set from register 20 bits [6:4] Register bit 0.15 must be cleared to 0 before enabling loopback. This bit is identical to 0_1.14. 1 = Enable Loopback 0 = Disable Loopback

Table 59: Control Register - Copper (Continued)
Page 0, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
13	Speed Select (LSB)	R/W	See Descr	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0.15) Power down (Register 0.11) transitions from power down to normal operation. Upon hardware reset this bit defaults as follows: ANEG[3:0] HWCFG_MODE[3:0] Bit 0_0.13 001x 0x00 1 001x 1x11 1 001x 1x10 1 001x 0110 1 all other configurations 0 A write to this register bit will have no effect if MODE[3:0] (either HWCF_MODE or Reg27[3:0] after a software reset) is one of the following: 1x0x, 01x1, 001x In these modes the bit will always be 0. Bit 6, 13 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps

Table 59: Control Register - Copper (Continued)
Page 0, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
12	Auto-Negotiation Enable	R/W	See Descr	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Power down (Register 0.11) transitions from power down to normal operation. When Auto-Negotiation is enabled (0.12 = 1), the speed, duplex, and pause capabilities are advertised in Register 4 and Register 9. If the Auto-Negotiation is disabled (0.12 = 0), then the speed and duplex capabilities take on the settings of register bits 0.13, 0.6, and 0.8. If Register 0_0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0_0.13 and 0_0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0_0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0_0.8 is set to 0. Registers 4_0.8:5 and 9_0.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. Upon hardware reset this bit defaults as follows: ANEG[3:2] Bit 0.12 11 1 all other configurations 0 1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process
11	Power Down	R/W	See Descr	0x0	When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (0.15) and Restart Auto-Negotiation (0_0.9) are not set by the user. IEEE power down shuts down the chip except for the MAC interface if 16.3 is set to 1. If 16.3 is set to 0, then the MAC interface also shuts down. Power down also has no effect on the 125CLK output if 16.4 is set to 0. This bit is identical to 1_0.11. 1 = Power down 0 = Normal operation
10	Isolate	R/W	0x0	0x0	The GMII/MII/TBI output pins are tristated when this bit is set to 1. The GMII/MII/TBI inputs are ignored. This bit is identical to 0_1.10. 1 = Isolate 0 = Normal operation

Table 59: Control Register - Copper (Continued)
Page 0, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
9	Restart Copper Auto-Negotiation	R/W, SC	0x0	SC	Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit (0_0.9) is set. Restart Auto-Negotiation bit should be used when the Auto-Neg bit (0.12) is enabled. 1 = Restart Auto-Negotiation Process 0 = Normal operation
8	Copper Duplex Mode	R/W	See Descr	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0.15) Power down (Register 0.11) transitions from power down to normal operation Upon hardware reset this bit defaults as follows: ANEG[3:0] Bit 0_0.8 00x1 1 1xxx 1 all other configurations 0 1 = Full-duplex 0 = Half-duplex
7	Collision Test	R/W	0x0	0x0	Setting this bit to 1 will cause the COL pin to assert whenever the TX_EN pin is asserted. This bit is identical to 0_1.7. 1 = Enable COL signal test 0 = Disable COL signal test
6	Speed Selection (MSB)	R/W	See Descr	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Power down (Register 0.11) transitions from power down to normal operation Upon hardware reset this bit defaults as follows: ANEG[3:0] HWCFG_MODE[3:0] Bit 0_0.6 1xxx xxxx 1 x1xx xxxx 1 xxxx xx01 1 xxxx 1x00 1 xxxx 0x11 1 xxxx 0010 1 all other configurations 0 bit 6, 13 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps

Table 59: Control Register - Copper (Continued)
Page 0, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
5:0	Reserved				These bits must be read and left unchanged when performing a write.

Table 60: Control Register - Fiber
Page 1, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reset	R/W	0x0	SC	PHY Software Reset. Writing a 1 to this bit causes the PHY state machines to be reset. When the reset operation is done, this bit is cleared to 0 automatically. The reset occurs immediately. This bit is identical to 0_0.15. 1 = PHY reset 0 = Normal operation
14	Loopback	R/W	0x0	0x0	When loopback is activated, the transmitter data presented on TXD is looped back to RXD internally. Link is broken when loopback is enabled. Loopback speed is determined by the mode the device is in Registers 20.6:4. In all Copper modes, the loopback speed is determined by Register 20[6:4] if copper Auto-Negotiation is enabled. If copper Auto-Negotiation is disabled, the loopback speed is determined by speed set in register 0.6 and 0.13 In GMII or RGMII to Fiber Modes the loopback speed is set to 1000Mbps In SGMII to GMII or RGMII Modes, the loopback speed is set to SGMII Link partner advertised speed (which is the SGMII Link partners Copper Link speed) if fiber Auto-Negotiation is enabled. If fiber Auto-Negotiation is disabled, the loopback speed is set from register 20 bits [6:4] This bit is identical to 0_0.14. 1 = Enable Loopback 0 = Disable Loopback
13	Speed Select (LSB)	RO	Always 0	Always 0	bit 6,13 10 = 1000 Mbps

Table 60: Control Register - Fiber (Continued)
Page 1, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
12	Auto-Negotiation Enable	R/W	See Descr	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0.11) transitions from power down to normal operation Fiber link goes down. This bit enables Auto-Negotiation on the fiber interface in all configurations where the serdes is used. Upon hardware reset this bit defaults as follows: MODE [3:0] ANEG[3:2] Bit 0.12 x000 xx 1 x110 xx 1 0100 xx 1 xx11 11 1 all other configurations 0 When this bit gets set/reset, Auto-Negotiation is restarted (bit 1.0.9 is set to 1) 1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process
11	Power Down	R/W	See Descr	0x0	When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (0.15) and Restart Auto-Negotiation (0_1.9) are not set by the user. IEEE power down shuts down the chip except for the MAC interface if 16.3 is set to 1. If 16.3 is set to 0, then the MAC interface also shuts down. Power down also has no effect on the 125CLK output if 16.4 is set to 0. This bit is identical to 0_0.11. 1 = Power down 0 = Normal operation
10	Isolate	R/W	0x0	0x0	The GMII/MII output pins are tristated when this bit is set to 1. The GMII/MIII inputs are ignored. This bit is identical to 0_0.10. 1 = Isolate 0 = Normal operation
9	Restart Fiber Auto-Negotiation	R/W, SC	0x0	SC	Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit (0_1.9) is set. The bit is set when Auto-Negotiation is Enabled or Disabled in 1.0.12 1 = Restart Auto-Negotiation Process 0 = Normal operation

Table 60: Control Register - Fiber (Continued)
Page 1, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
8	Fiber Duplex Mode	R/W	See Descr	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0.11) transitions from power down to normal operation Upon hardware reset this bit defaults as follows: ANEG[3:0] Bit 0_1.8 00x1 1 1xxx 1 all other configurations 0 1 = Full-duplex 0 = Half-duplex
7	Collision Test	R/W	0x0	0x0	Setting this bit to 1 will cause the COL pin to assert whenever the TX_EN pin is asserted. This bit is identical to 0_0.7. 1 = Enable COL signal test 0 = Disable COL signal test
6	Speed Selection (MSB)	RO	Always 1	Always 1	bit 6, 13 10 = 1000 Mbps
5:0	Reserved				These bits must be read and left unchanged when performing a write.

Table 61: Status Register - Copper
Page 0, Register 1

Bits	Field	Mode	HW Rst	SW Rst	Description
15	100BASE-T4	RO	Always 0	Always 0	100BASE-T4. This protocol is not available. 0 = PHY not able to perform 100BASE-T4
14	100BASE-X Full-Duplex	RO	See Descr	See Descr	Upon hardware reset this bit defaults as follows: HWCFG_MODE[3:0] Bit 1.14 xx01 0 1x00 0 0x11 0 xx00 0 all other configurations 1 Upon software reset this bit defaults as follows: HWCFG_MODE[3:0] Bit 1.14 xx01 0 1x00 0 0x11 0 all other configurations 1 1 = PHY able to perform full-duplex 100BASE-X 0 = PHY not able to perform full-duplex 100BASE-X
13	100BASE-X Half-Duplex	RO	See Descr	See Descr	Upon hardware reset this bit defaults as follows: HWCFG_MODE[3:0] Bit 1.13 xx01 0 1x00 0 0x11 0 xx00 0 all other configurations 1 Upon software reset this bit defaults as follows: HWCFG_MODE[3:0] Bit 1.13 xx01 0 1x00 0 0x11 0 all other configurations 1 1 = PHY able to perform half-duplex 100BASE-X 0 = PHY able to perform half-duplex 100BASE-X
12	10 Mbps Full-Duplex	RO	See Descr	See Descr	Upon hardware reset this bit defaults as follows: HWCFG_MODE[3:0] Bit 1.12 xx01 0 1x00 0 0x11 0 xx00 0 all other configurations 1 Upon software reset this bit defaults as follows: HWCFG_MODE[3:0] Bit 1.12 xx01 0 1x00 0 0x11 0 all other configurations 1 1 = PHY able to perform full-duplex 10BASE-T 0 = PHY not able to perform full-duplex 10BASE-T

Table 61: Status Register - Copper (Continued)
Page 0, Register 1

Bits	Field	Mode	HW Rst	SW Rst	Description
11	10 Mbps Half-Duplex	RO	See Descr	See Descr	Upon hardware reset this bit defaults as follows: HWCFG_MODE[3:0] Bit 1.11 xx01 0 1x00 0 0x11 0 xx00 0 all other configurations 1 Upon software reset this bit defaults as follows: HWCFG_MODE[3:0] Bit 1.11 xx01 0 1x00 0 0x11 0 all other configurations 1 1 = PHY able to perform half-duplex 10BASE-T 0 = PHY not able to perform half-duplex 10BASE-T
10	100BASE-T2 Full-Duplex	RO	Always 0	Always 0	This protocol is not available. 0 = PHY not able to perform full-duplex
9	100BASE-T2 Half-Duplex	RO	Always 0	Always 0	This protocol is not available. 0 = PHY not able to perform half-duplex
8	Extended Status	RO	Always 1	Always 1	1 = Extended status information in Register 15
7	Reserved				This bit must be read and left unchanged when performing a write.
6	MF Preamble Suppression	RO	Always 1	Always 1	1 = PHY accepts management frames with preamble suppressed
5	Copper Auto-Negotiation Complete	RO	0x0	0x0	1 = Auto-Negotiation process complete 0 = Auto-Negotiation process not complete
4	Copper Remote Fault	RO,LH	0x0	0x0	Remote Fault bit is only supported in 1000BASE-T mode. 1 = Remote fault condition detected 0 = Remote fault condition not detected
3	Auto-Negotiation Ability	RO	Always 1	Always 1	1 = PHY able to perform Auto-Negotiation
2	Copper Link Status	RO,LL	0x0	0x0	This register bit indicates whether link was lost since the last read. For the current link status, either read this register back-to-back or read Register 17_0.10 Link Real Time. 1 = Link is up 0 = Link is down
1	Jabber Detect	RO,LH	0x0	0x0	1 = Jabber condition detected 0 = Jabber condition not detected
0	Extended Capability	RO	Always 1	Always 1	1 = Extended register capabilities

Table 62: Status Register - Fiber
Page 1, Register 1

Bits	Field	Mode	HW Rst	SW Rst	Description
15	100BASE-T4	RO	Always 0	Always 0	100BASE-T4. This protocol is not available. 0 = PHY not able to perform 100BASE-T4
14	100BASE-X Full-Duplex	RO	Always 0	Always 0	0 = PHY not able to perform full-duplex 100BASE-X
13	100BASE-X Half-Duplex	RO	Always 0	Always 0	0 = PHY not able to perform full-duplex 100BASE-X
12	10 Mb/s Full Duplex	RO	Always 0	Always 0	0 = PHY not able to perform full-duplex 10BASE-T
11	10 Mbps Half-Duplex	RO	Always 0	Always 0	0 = PHY not able to perform half-duplex 10BASE-T
10	100BASE-T2 Full-Duplex	RO	Always 0	Always 0	This protocol is not available. 0 = PHY not able to perform full-duplex
9	100BASE-T2 Half-Duplex	RO	Always 0	Always 0	This protocol is not available. 0 = PHY not able to perform half-duplex
8	Extended Status	RO	Always 1	Always 1	1 = Extended status information in Register 15
7	Reserved				This bit must be read and left unchanged when performing a write.
6	MF Preamble Suppression	RO	Always 1	Always 1	1 = PHY accepts management frames with preamble suppressed
5	Fiber Auto-Negotiation Complete	RO	0x0	0x0	1 = Auto-Negotiation process complete 0 = Auto-Negotiation process not complete Bit is not set when link is up due of Fiber Auto-Negotiation Bypass or if Auto-Negotiation is disabled.
4	Fiber Remote Fault	RO,LH	0x0	0x0	1 = Remote fault condition detected 0 = Remote fault condition not detected This bit is always 0 in SGMII to Copper and SGMII to GMII or RGMII Modes.
3	Auto-Negotiation Ability	RO	Always 1	Always 1	1 = PHY able to perform Auto-Negotiation
2	Fiber Link Status	RO,LL	0x0	0x0	This register bit indicates when link was lost since the last read. For the current link status, either read this register back-to-back or read Register 17_1.10 Link Real Time. 1 = Link is up 0 = Link is down
1	Reserved				This bit must be read and left unchanged when performing a write.
0	Extended Capability	RO	Always 1	Always 1	1 = Extended register capabilities

Table 63: PHY Identifier
Page Any, Register 2

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bits 3:18	RO	0x0141	0x0141	Marvell® OUI is 0x005043 0000 0000 0101 0000 0100 0011 ^ ^ bit 1.....bit 24 Register 2.[15:0] show bits 3 to 18 of the OUI. 0000000101000001 ^ ^ bit 3.....bit18

Table 64: PHY Identifier
Page Any, Register 3

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	OUI LSb	RO	Always 000011	0x00	Organizationally Unique Identifier bits 19:24 000011 ^.....^ bit 19..bit24
9:4	Model Number	RO	Always 001100	0x00	Model Number 88E1111 = 001100
3:0	Revision Number	RO	See Descr	See Descr	Rev Number Contact Marvell® FAEs for information on the device revision number.

Table 65: Auto-Negotiation Advertisement Register - Copper
Page 0, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	Retain	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down If 1000BASE-T is advertised then the required next pages are automatically transmitted. Register 4_0.15 should be set to 0 if no additional next pages are needed. If 4_0.15 is set to 1, then Register 7_0 should be programmed with the desired value and 7_0 will be sent when 7_0.15 = 1. In GBIC mode, a Write to this register is inconsequential. 1 = Advertise 0 = Not advertised
14	Ack	RO	Always 0	Always 0	Must be 0.
13	Remote Fault	R/W	0x0	Retain	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down In GBIC mode, a Write to this register is inconsequential. 1 = Set Remote Fault bit 0 = Do not set Remote Fault bit
12	Reserved	R/W	0x0	Retain	This bit must be read and left unchanged when performing a write.
11	Asymmetric Pause	R/W	See Descr	Retain	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down In GBIC mode, a Write to this register is inconsequential. Upon hardware reset this bit defaults as follows: ENA_PAUSE Bit 4_0.11 0 0 1 1 1 = Asymmetric Pause 0 = No asymmetric Pause

Table 65: Auto-Negotiation Advertisement Register - Copper (Continued)
Page 0, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
10	Pause	R/W	See Descr	Retain	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down In GBIC mode, a Write to this register is inconsequential. Upon hardware reset, this bit defaults as follows: ENA_PAUSE Bit 4_0.10 0 0 1 1 1 = MAC PAUSE implemented 0 = MAC PAUSE not implemented
9	100BASE-T4	R/W	0x0	0x0	0 = Not capable of 100BASE-T4
8	100BASE-TX Full-Duplex	R/W	See Descr	Retain	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down In GBIC mode, a Write to this register is inconsequential. If register 0_0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0_0.13 and 0_0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0_0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0_0.8 set to 0. Registers 4_0.8:5 and 9_0.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. Upon hardware reset this bit defaults as follows: ANEG[3:0] HWCFG_MODE[3:0] Bit 4_0.8 0011 0x00 1 0011 1x11 1 11xx 0x00 1 11xx 1x11 1 all other configurations 0 1 = Advertise 0 = Not advertised

Table 65: Auto-Negotiation Advertisement Register - Copper (Continued)
Page 0, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
7	100BASE-TX Half-Duplex	R/W	See Descr	Retain	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down In GBIC mode, a Write to this register is inconsequential. If register 0_0.12 is set to 0 and speed is manually forced to 1000 Mbps in registers 0_0.13 and 0_0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if Register 0_0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0_0.8 set to 0. Registers 4_0.8:5 and 9_0.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. Upon hardware reset this bit defaults as follows: ANEG[3:0] HWCFG_MODE[3:0] Bit 4_0.7 0010 0x00 1 0010 1x11 1 11xx 0x00 1 11xx 1x11 1 all other configurations 0 1 = Advertise 0 = Not advertised
6	10BASE-TX Full-Duplex	R/W	See Descr	Retain	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down In GBIC mode, a Write to this register is inconsequential. If Register 0_0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0_0.13 and 0_0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if Register 0_0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0_0.8 set to 0. Registers 4_0.8:5 and 9_0.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. Upon hardware reset this bit defaults as follows: ANEG[3:0] HWCFG_MODE[3:0] Bit 4_0.6 0001 0x00 1 0001 1x11 1 11xx 0x00 1 11xx 1x11 1 all other configurations 0 1 = Advertise 0 = Not advertised

Table 65: Auto-Negotiation Advertisement Register - Copper (Continued)
Page 0, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
5	10BASE-TX Half-Duplex	R/W	See Descr	Retain	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down In GBIC mode, a Write to this register is inconsequential. If Register 0_0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0_0.13 and 0_0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if Register 0_0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0_0.8 set to 0. Registers 4_0.8:5 and 9_0.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. Upon hardware reset this bit defaults as follows: ANEG[3:0] HWCFG_MODE[3:0] Bit 4_0.5 0000 0x00 1 0000 1x11 1 11xx 0x00 1 11xx 1x11 1 all other configurations 0 1 = Advertise 0 = Not advertised
4:0	Selector Field	R/W	Always 00001	Always 00001	Selector Field mode 00001 = 802.3

Table 66: Auto-Negotiation Advertisement Register - Fiber (GMII/RGMII Mode)
Page 1, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	Retain	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down 1 = Advertise 0 = Not advertised
14	Reserved				This bit must be read and left unchanged when performing a write.
13:12	Remote Fault 2 RemoteFault 1	R/W	0x0	Retain	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0.15) Re-start Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down Device has no ability to detect remote fault. 00 = No error, link OK (default) 01 = Link Failure 10 = Offline 11 = Auto-Negotiation Error
11:9	Reserved				These bits must be read and left unchanged when performing a write.
8:7	Pause	R/W	See Descr	Retain	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0.15) Re-start Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down Upon hardware reset, this bit defaults as follows: ENA_PAUSE Bits 4_1.8:7 0 00 1 11 00 = No PAUSE 01 = Symmetric PAUSE 10 = Asymmetric PAUSE toward link partner 11 = Both Symmetric PAUSE and Asymmetric PAUSE toward local device.

Table 66: Auto-Negotiation Advertisement Register - Fiber (GMII/RGMII Mode) (Continued)
Page 1, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
6	1000BASE-X Half-Duplex	R/W	See Descr	Retain	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0.15) Re-start Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down Upon hardware reset this bit defaults as follows: ANEG[3:0] Bit 4_1.6 x1xx 1 all other configurations 0 1 = Advertise 0 = Not advertised
5	1000BASE-X Full-Duplex	R/W	See Descr	Retain	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0.15) Re-start Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down Upon hardware reset this bit defaults as follows: ANEG[3:0] Bit 4_1.5 1xxx 1 all other configurations 0 1 = Advertise 0 = Not advertised
4:0	Reserved				These bits must be read and left unchanged when performing a write.

Table 67: Auto-Negotiation Advertisement Register - (SGMII to Copper Modes) (Mode = 0x00)
Page 1, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Copper Link Status	RO	0x0	0x0	0 = Link is Not up on the Copper Interface 1 = Link is UP on the Copper Interface
14	Reserved				This bit must be read and left unchanged when performing a write.
13	Reserved				This bit must be read and left unchanged when performing a write.
12	Copper Duplex Status	RO	0x0	0x0	0 = Copper Interface Resolved to Half-duplex 1 = Copper Interface Resolved to Full-duplex
11:10	Copper Speed[1:0]	RO	0x0	0x0	00 = Copper Interface speed is 10 Mbps 01 = Copper Interface speed is 100 Mbps 10 = Copper Interface speed is 1000 Mbps 11 = Reserved
9:0	Reserved				These bits must be read and left unchanged when performing a write.

Table 68: Auto-Negotiation Advertisement Register - Fiber (SGMII to R-GMII Modes) (Mode = x110)
Page 1, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Reserved				These bits must be read and left unchanged when performing a write.

Table 69: Auto-Negotiation Advertisement Register - Fiber (GBIC Mode) (Mode = 1000)
Page 1, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
15:9	Reserved				These bits must be read and left unchanged when performing a write.
8:7	Pause	RO	Always 00	Always 00	Pause Status as Indicated by the Link Partner on the Copper Interface 00 = No PAUSE 01 = Symmetric PAUSE 10 = Asymmetric PAUSE toward link partner 11 = Both Symmetric PAUSE and Asymmetric PAUSE toward local device.
6	1000BASE-X Half-Duplex	RO	Always 00	Always 00	Copper Link Partners Half-duplex Status' 1 = Half-duplex Capable 0 = Half-duplex Incapable
5	1000BASE-X Full-Duplex	RO	Always 00	Always 00	Copper Link Partners Full-duplex Status' 1 = Full-duplex Capable 0 = Full-duplex Incapable
4:0	Reserved				These bits must be read and left unchanged when performing a write.

Table 70: Link Partner Ability Register - Base Page, Copper
Page 0, Register 5

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received. Received Code Word Bit 15 1 = Link partner capable of next page 0 = Link partner not capable of next page
14	Acknowledge	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page receives Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link Partner has not received link code word
13	Remote Fault	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received. Remote Fault Received Code Word Bit 13 1 = Link partner detected remote fault 0 = Link partner has not detected remote fault
12	Technology Ability Field	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 12

Table 70: Link Partner Ability Register - Base Page, Copper (Continued)
Page 0, Register 5

Bits	Field	Mode	HW Rst	SW Rst	Description
11	Asymetric Pause	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received. Received Code Word Bit 11 1 = Link partner requests asymmetric pause 0 = Link partner does not request asymmetric pause
10	Pause Capable	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received. Received Code Word Bit 10 1 = Link partner is capable of symmetric pause operation 0 = Link partner is not capable of symmetric pause operation
9	100BASE-T4 Capability	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received. Received Code Word Bit 9 1 = Link partner is 100BASE-T4 capable 0 = Link partner is not 100BASE-T4 capable
8	100BASE-TX Full-Duplex Capability	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received. Received Code Word Bit 8 1 = Link partner is 100BASE-TX full-duplex capable 0 = Link partner is not 100BASE-TX full-duplex capable
7	100BASE-TX Half-Duplex Capability	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received. Received Code Word Bit 7 1 = Link partner is 100BASE-TX half-duplex capable 0 = Link partner is not 100BASE-TX half-duplex capable
6	10BASE-T Full-Duplex Capability	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received. Received Code Word Bit 6 1 = Link partner is 10BASE-T full-duplex capable 0 = Link partner is not 10BASE-T full-duplex capable
5	10BASE-T Half-Duplex Capability	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received. Received Code Word Bit 5 1 = Link partner is 10BASE-T half-duplex capable 0 = Link partner is not 10BASE-T half-duplex capable
4:0	Selector Field	RO	0x00	0x00	Register bit is cleared when link goes down and loaded when a base page is received. Selector Field Received Code Word Bit 4:0

Table 71: Link Partner Ability Register - Base Page, Fiber (RGMII or GMII Modes)
Page 1, Register 5

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 15 1 = Link partner capable of next page 0 = Link partner not capable of next page
14	Acknowledge	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received. Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner has not received link code word
13:12	Remote Fault 2 Remote Fault 1	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received. Received Code Word Bit 13:12 00 = No error, link OK (default) 01 = Link Failure 10 = Offline 11 = Auto-Negotiation Error
11:9	Reserved				These bits must be read and left unchanged when performing a write.
8:7	Asymetric Pause	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received. Received Code Word Bit 8:7 00 = No PAUSE 01 = Symmetric PAUSE 10 = Asymmetric PAUSE toward link partner 11 = Both Symmetric PAUSE and Asymmetric PAUSE toward local device.
6	1000BASE-X Half-Duplex	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received. Received Code Word bit 6 1 = Link partner capable of 1000BASE-X half-duplex. 0 = Link partner not capable of 1000BASE-X half-duplex.
5	1000BASE-X Full-Duplex	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received. Received Code Word bit 5 1 = Link partner capable of 1000BASE-X full-duplex. 0 = Link partner not capable of 1000BASE-X full-duplex.
4:0	Reserved				These bits must be read and left unchanged when performing a write.

Table 72: Link Partner Ability Register - Base Page, Fiber (SGMII to Copper Modes) (Mode = 0x00)
Page 1, Register 5

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved				This bit must be read and left unchanged when performing a write.
14	Acknowledge	RO	0x0	0x0	Acknowledge Register bit is cleared when link goes down and loaded when a base page is received. Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner has not received link code word
13:0	Reserved				These bits must be read and left unchanged when performing a write.

Table 73: Link Partner Ability Register - Base Page, Fiber (SGMII to R-GMII Modes) (Mode = x110)
Page 1, Register 5

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Copper Link	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 15 1 = Copper Link is up on the link partner 0 = Copper Link is not up on the link partner
14	Acknowledge	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner has not received link code word
13	Reserved				This bit must be read and left unchanged when performing a write.
12	Copper Duplex Status	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 12 1 = Copper Interface on the Link Partner is capable of Full-duplex 0 = Copper Interface on the link partner is capable of Half-duplex
11:10	Copper Speed Status	RO	0x0	0x0	Register bits are cleared when link goes down and loaded when a base page is received Received Code Word Bit 11:10 00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps 11 = Reserved
9:0	Reserved				These bits must be read and left unchanged when performing a write.

Table 74: Link Partner Ability Register - Base Page, Fiber (GBIC Mode) (Mode = 1000)
Page 1, Register 5

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved				This bit must be read and left unchanged when performing a write.
14	Acknowledge	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner has not received link code word
13:9	Reserved				These bits must be read and left unchanged when performing a write.
8:7	Asymetric Pause	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 8:7 00 = No PAUSE 01 = Symmetric PAUSE 10 = Asymmetric PAUSE toward link partner 11 = Both Symmetric PAUSE and Asymmetric PAUSE toward local device.
6	1000BASE-X Half-Duplex	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word bit 6 1 = Link partner capable of 1000BASE-T half-duplex. 0 = Link partner not capable of 1000BASE-T half-duplex.
5	1000BASE-X Full-Duplex	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word bit 5 1 = Link partner capable of 1000BASE-T full-duplex. 0 = Link partner not capable of 1000BASE-T full-duplex.
4:0	Reserved				These bits must be read and left unchanged when performing a write.

Table 75: Auto-Negotiation Expansion Register - Copper
Page 0, Register 6

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved				These bits must be read and left unchanged when performing a write.
4	Parallel Detection Fault	RO,LH	0x0	0x0	6_0.3 is set when a base page is received and the received link control word has bit 15 set to 1. The bit is cleared when link goes down. 1 = A fault has been detected via the Parallel Detection function 0 = A fault has not been detected via the Parallel Detection function

Table 75: Auto-Negotiation Expansion Register - Copper
Page 0, Register 6

Bits	Field	Mode	HW Rst	SW Rst	Description
3	Link Partner Next page Able	RO	0x0	0x0	Register 6_0.3 is not valid until the Auto-Negotiation complete bit (Reg 1_0.5) indicates completed. 1 = Link Partner is Next Page able 0 = Link Partner is not Next Page able
2	Local Next Page Able	RO	Always 1	Always 1	1 = Local Device is Next Page able
1	Page Received	RO, LH	0x0	0x0	Register 6_0.1 is set when a valid page is received. 1 = A New Page has been received 0 = A New Page has not been received
0	Link Partner Auto-Negotiation Able	RO	0x0	0x0	This bit is set when the device receives 3 matching FLP bursts and the Auto-Negotiation is enabled in register 0.0.12 1 = Link Partner is Auto-Negotiation able 0 = Link Partner is not Auto-Negotiation able

Table 76: Auto-Negotiation Expansion Register - Fiber
Page 1, Register 6

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved				These bits must be read and left unchanged when performing a write.
3	Link Partner Next page Able	RO	0x0	0x0	In SGMII to Copper, SGMII to RGMII, GBIC and Legacy GBIC Modes this bit is always 0. In all the other modes register 6_1.3 is set when a base page is received and the received link control word has bit 15 set to 1. The bit is cleared when link goes down. 1 = Link Partner is Next Page able 0 = Link Partner is not Next Page able
2	Local Next Page Able	RO	Always 1	Always 1	1 = Local Device is Next Page able
1	Page Received	RO, LH	0x0	0x0	Register 6_1.1 is set when a valid page is received. 1 = A New Page has been received 0 = A New Page has not been received
0	Link Partner Auto-Negotiation Able	RO	0x0	0x0	This bit is set when there is sync status, the fiber receiver has received 3 non-zero matching valid configuration code groups and Auto-Negotiation is enabled in register 1.0.12 1 = Link Partner is Auto-Negotiation able 0 = Link Partner is not Auto-Negotiation able

Table 77: Next Page Transmit Register - Copper
Page 0, Register 7

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	0x0	A write to register 7_0 implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded. Transmit Code Word Bit 15
14	Reserved				This bit must be read and left unchanged when performing a write.
13	Message Page Mode	R/W	0x1	0x1	Transmit Code Word Bit 13
12	Acknowledge2	R/W	0x0	0x0	Transmit Code Word Bit 12
11	Toggle	RO	0x0	0x0	Transmit Code Word Bit 11. This bit is internally set to the opposite value each time a page is received
10:0	Message/ Unformatted Field	R/W	0x001	0x001	Transmit Code Word Bit 10:0

Table 78: Next Page Transmit Register - Fiber
Page 1, Register 7

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	0x0	A write to register 7_1 implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded. Transmit Code Word Bit 15
14	Reserved				This bit must be read and left unchanged when performing a write.
13	Message Page Mode	R/W	0x1	0x1	Transmit Code Word Bit 13
12	Acknowledge2	R/W	0x0	0x0	Transmit Code Word Bit 12
11	Toggle	RO	0x0	0x0	Transmit Code Word Bit 11. This bit is internally set to the opposite value each time a page is received.
10:0	Message/ Unformatted Field	R/W	0x001	0x001	Transmit Code Word Bit 10:0

Table 79: Link Partner Next Page Register - Copper
Page 0, Register 8

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	The register is loaded only when a next page is received from the link partner. It is cleared each time the link goes down. Received Code Word Bit 15
14	Acknowledge	RO	0x0	0x0	Received Code Word Bit 14
13	Message Page	RO	0x0	0x0	Received Code Word Bit 13
12	Acknowledge2	RO	0x0	0x0	Received Code Word Bit 12
11	Toggle	RO	0x0	0x0	Received Code Word Bit 11
10:0	Message/ Unformatted Field	RO	0x000	0x000	Received Code Word Bit 10:0

Table 80: Link Partner Next Page Register - Fiber
Page 1, Register 8

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	The register is loaded only when a next page is received from the link partner. It is cleared each time the link goes down. Received Code Word Bit 15
14	Acknowledge	RO	0x0	0x0	Received Code Word Bit 14
13	Message Page	RO	0x0	0x0	Received Code Word Bit 13
12	Acknowledge2	RO	0x0	0x0	Received Code Word Bit 12
11	Toggle	RO	0x0	0x0	Received Code Word Bit 11
10:0	Message/ Unformatted Field	RO	0x000	0x000	Received Code Word Bit 10:0

Table 81: 1000BASE-T Control Register
Page 0, Register 9

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	Test Mode	R/W	0x0	Retain	After exiting the test mode, hardware reset or software reset (Register 0.15) should be issued to ensure normal operation. A restart of Auto-Negotiation will clear these bits. 000 = Normal Mode 001 = Test Mode 1 - Transmit Waveform Test 010 = Test Mode 2 - Transmit Jitter Test (MASTER mode) 011 = Test Mode 3 - Transmit Jitter Test (SLAVE mode) 100 = Test Mode 4 - Transmit Distortion Test 101, 110, 111 = Reserved The transmitting clock which is synchronous to the test data is sourcing from the RX_CLK pin for jitter testing in test modes 2 and 3.
12	MASTER/ SLAVE Manual Configu-ration Enable	R/W	See Descr	Retain	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down Upon hardware reset this bit defaults as follows: ANEG[3:0] Bit 9_0.12 xx1x 0 all other configurations 1 1 = Manual MASTER/SLAVE configuration 0 = Automatic MASTER/SLAVE configuration
11	MASTER/ SLAVE Configuration Value	R/W	See Descr	Retain	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down Register 9_0.11 is ignored if Register 9_0.12 is equal to 0. Upon hardware reset this bit defaults as follows: ANEG[3:0] Bit 9_0.11 xxx1 0 all other configurations 1 1 = Manual configure as MASTER 0 = Manual configure as SLAVE

Table 81: 1000BASE-T Control Register (Continued)
Page 0, Register 9

Bits	Field	Mode	HW Rst	SW Rst	Description
10	Port Type	R/W	See Descr	Retain	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down Register 9_0.10 is ignored if Register 9_0.12 is equal to 1. Upon hardware reset this bit defaults as follows: ANEG[3:0] Bit 9_0.10 xxx1 0 all other configurations 1 1 = Prefer multi-port device (MASTER) 0 = Prefer single port device (SLAVE)
9	1000BASE-T Full-Duplex	R/W	See Descr	Retain	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down Upon hardware reset this bit defaults as follows: ANEG[3:0] Bit 9_0.9 1xxx 1 all other configurations 0 1 = Advertise 0 = Not advertised
8	1000BASE-T Half-Duplex	R/W	See Descr	Retain	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down Upon hardware reset this bit defaults as follows: ANEG[3:0] Bit 9_0.8 x1xx 1 all other configurations 0 1 = Advertise 0 = Not advertised
7:0	Reserved				These bits must be read and left unchanged when performing a write.

Table 82: 1000BASE-T Status Register
Page 0, Register 10

Bits	Field	Mode	HW Rst	SW Rst	Description
15	MASTER/ SLAVE Configuration Fault	RO,LH	0x0	0x0	This register bit will clear on read and restart autoneg It is set to 0 when Auto-Negotiation is off 1 = MASTER/SLAVE configuration fault detected 0 = No MASTER/SLAVE configuration fault detected
14	MASTER/ SLAVE Configuration Resolution	RO	0x0	0x0	1 = Local PHY configuration resolved to MASTER 0 = Local PHY configuration resolved to SLAVE
13	Local Receiver Status	RO	0x0	0x0	1 = Local Receiver OK 0 = Local Receiver is Not OK
12	Remote Receiver Status	RO	0x0	0x0	1 = Remote Receiver OK 0 = Remote Receiver Not OK
11	Link Partner 1000BASE-T Full-Duplex Capability	RO	0x0	0x0	1 = Link Partner is capable of 1000BASE-T full-duplex 0 = Link Partner is not capable of 1000BASE-T full-duplex
10	Link Partner 1000BASE-T Half-Duplex Capability	RO	0x0	0x0	1 = Link Partner is capable of 1000BASE-T half-duplex 0 = Link Partner is not capable of 1000BASE-T half-duplex
9:8	Reserved				These bits must be read and left unchanged when performing a write.
7:0	Idle Error Count	RO, SC	0x00	0x00	MSB of Idle Error Counter These register bits report the idle error count since the last time this register was read. The counter pegs at 11111111 and will not roll over.

Table 83: Reserved Registers
Page Any, Register 11

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Reserved				These bits must be read and left unchanged when performing a write.

Table 84: Reserved Registers
Page Any, Register 12

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Reserved				These bits must be read and left unchanged when performing a write.

Table 85: Reserved Registers
Page Any, Register 13

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Reserved				These bits must be read and left unchanged when performing a write.

Table 86: Reserved Registers
Page Any, Register 14

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Reserved				These bits must be read and left unchanged when performing a write.

Table 87: Extended Status Register
Page Any, Register 15

Bits	Field	Mode	HW Rst	SW Rst	Description
15	1000BASE-X Full-Duplex	RO	See Descr	See Descr	This bit is set to 1 when mode is one of these: 0011, 0110, 0111, 1000 This bit is also set to 1 if auto fiber/copper mode is on when mode is one of these: 1001, 1011, 1101, 1111 Any other mode/auto-fiber-copper combination, this bit is set to 0 1 = 1000 BASE-X full-duplex capable 0 = Not 1000 BASE-X full-duplex capable
14	1000BASE-X Half-Duplex	RO	See Descr	See Descr	This bit is set to 1 when mode is one of these: 0011, 0110, 0111, 1000 This bit is also set to 1 if auto fiber/copper mode is on when mode is one of these: 1001, 1011, 1101, 1111 Any other mode/auto-fiber-copper combination, this bit is set to 0 1 = 1000 BASE-X half-duplex capable 0 = Not 1000 BASE-X half-duplex capable
13	1000BASE-T Full-Duplex	RO	See Descr	See Descr	This bit is set to 1 when mode is one of these: 0000, 0100, 1000, 1001, 1011, 1101, 1111 Any other mode, this bit is set to 0 1 = 1000BASE-T full-duplex capable 0 = Not 1000BASE-T full-duplex capable
12	1000BASE-T Half-Duplex	RO	See Descr	See Descr	This bit is set to 1 when mode is one of these: 0000, 0100, 1000, 1001, 1011, 1101, 1111 Any other mode, this bit is set to 0 1 = 1000BASE-T half-duplex capable 0 = Not 1000BASE-T half-duplex capable
11:0	Reserved				These bits must be read and left unchanged when performing a write.

Table 88: PHY Specific Control Register
Page Any, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Transmit FIFO Depth	R/W	0x0	Retain	See "Synchronizing FIFO" on page 73 to determine when the transmit FIFO is enabled. 1000BASE-T 10/100BASE-T 00 = ± 16 Bits 00 = ± 8 Bits 01 = ± 24 Bits 01 = ± 12 Bits 10 = ± 32 Bits 10 = ± 16 Bits 11 = ± 40 Bits 11 = ± 20 Bits
13:12	Receive FIFO Depth	R/W	0x0	Retain	See "Synchronizing FIFO" on page 73 to determine when the transmit FIFO is enabled. 1000BASE-T 10/100BASE-T 00 = ± 16 Bits 00 = ± 8 Bits 01 = ± 24 Bits 01 = ± 12 Bits 10 = ± 32 Bits 10 = ± 16 Bits 11 = ± 40 Bits 11 = ± 20 Bits
11	Assert CRS on Transmit	R/W	0x0	Retain	This bit has no effect in full-duplex. 1 = Assert on transmit 0 = Never assert on transmit
10	Force Link Good	R/W	0x0	Retain	If link is forced to be good, the link state machine is bypassed and the link is always up. In 1000BASE-T mode this has no effect. 1 = Force link good 0 = Normal operation
9:8	Energy Detect	R/W	See Descr	Update	Upon hardware reset this bit defaults as follows DIS_SLEEP Bits 16.9:8 0 11 1 00 0x = Off 10 = Sense only on Receive (Energy Detect) 11 = Sense and periodically transmit NLP (Energy Detect+™)
7	Enable Extended Distance	R/W	0x0	Retain	When using cable exceeding 100m, the 10BASE-T receive threshold must be lowered in order to detect incoming signals. 1 = Lower 10BASE-T receive threshold 0 = Normal 10BASE-T receive threshold

Table 88: PHY Specific Control Register (Continued)
Page Any, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
6:5	MDI Crossover Mode	R/W	See Descr	Update	Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. Upon hardware reset this bit defaults as follows ENA_XC ANEG[3:0] Bits 16.6:5 1 1xxx 11 1 x1xx 11 0 xxxx 01(for multiple port device) 0 xxxx 00(for single port device) x 00xx 01(for multiple port device) x 00xx 00(for single port device) 00 = Manual MDI configuration 01 = Manual MDIX configuration 10 = Reserved 11 = Enable automatic crossover for all modes
4	Disable 125CLK	R/W	See Descr	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. Upon hardware reset this bit defaults as follows DIS_125 Bit 16.4 0 0 1 1 1 = 125CLK low 0 = 125CLK toggle
3	MAC Interface Power Down	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. This bit determines whether MAC interface powers down when Register 0.11 is used to power down the device or when the PHY enters the energy detect state. In modes 0111 or 0011 RX_CLK will not toggle when in Power Down mode. 1 = Always power up 0 = Can power down
2	SQE test	R/W	0x0	Retain	SQE Test is automatically disabled in full-duplex mode regardless of the state of Register 16.2. 1 = SQE test enabled 0 = SQE test disabled
1	Polarity Reversal	R/W	0x0	Retain	If polarity is disabled, then the polarity is forced to be normal in 10BASE-T. 1 = Polarity Reversal Disabled 0 = Polarity Reversal Enabled
0	Disable Jabber	R/W	0x0	Retain	Jabber has effect only in 10BASE-T half-duplex mode. 1 = Disable jabber function 0 = Enable jabber function

Table 89: PHY Specific Status Register - Copper
Page 0, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Speed	RO	0x0	Retain	These status bits are valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
13	Duplex	RO	0x0	Retain	This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Full-duplex 0 = Half-duplex
12	Page Received	RO, LH	0x0	0x0	1 = Page received 0 = Page not received
11	Speed and Duplex Resolved	RO	0x0	0x0	When Auto-Negotiation is not enabled 17_0.11 = 1. 1 = Resolved 0 = Not resolved (If bit 27.11 is 1, then this bit will be 0.)
10	Link (real time)	RO	0x0	0x0	1 = Link up 0 = Link down
9:7	Cable Length (1000 mode only)	RO	0x0	0x0	Cable length measurement is only a rough estimate. Actual value depends on the attenuation of the cable, output levels of the remote transceiver, connector impedance, etc. 000 = < 50m 001 = 50 - 80m 010 = 80 - 110m 011 = 110 - 140m 100 = greater than 140m A new improved DSP based cable length estimation is also available as described in the application note: “VCT™ – Cable Status Extended Features Plus How to Use TDR Results For Gigabit PHYs.”
6	MDI Crossover Status	RO	0x0	0x0	This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. This bit is 0 or 1 depending on what is written to 16.6:5 in manual configuration mode. Register 16.6:5 are updated with software reset. 1 = MDIX 0 = MDI
5	Downshift Status	RO	0x0	0x0	1 = Downshift 0 = No Downshift

Table 89: PHY Specific Status Register - Copper (Continued)
Page 0, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
4	Copper Energy Detect Status	RO	0x0	0x0	The PHY will go into sleep mode if it does not detect energy for six seconds. The PHY will start in active mode after six seconds once power-up, hardware or software reset is complete. 1 = Sleep 0 = Active
3	Transmit Pause Enabled	RO	0x0	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Transmit pause enabled 0 = Transmit pause disable
2	Receive Pause Enabled	RO	0x0	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Receive pause enabled 0 = Receive pause disabled
1	Polarity (real time)	RO	0x0	0x0	1 = Reversed 0 = Normal
0	Jabber (real time)	RO	0x0	retain	1 = Jabber 0 = No jabber

Table 90: PHY Specific Status Register - Fiber
Page 1, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Speed	RO	0x0	Retain	These status bits are valid only after resolved bit 17_1.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
13	Duplex	RO	0x0	Retain	This status bit is valid only after resolved bit 17_1.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Full-duplex 0 = Half-duplex
12	Page Received	RO, LH	0x0	0x0	1 = Page received 0 = Page not received

Table 90: PHY Specific Status Register - Fiber (Continued)
Page 1, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
11	Speed and Duplex Resolved	RO	0x0	0x0	When Auto-Negotiation is not enabled or mode is 0001 or 0101 17_1.11 = 1. 1 = Resolved 0 = Not resolved If bit 27.11 is 1, then this bit will be 0.
10	Link (real time)	RO	0x0	0x0	1 = Link up 0 = Link down
9:5	Reserved				These bits must be read and left unchanged when performing a write.
4	Fiber Energy Detect Status	RO	0x1	0x1	1 = No energy detected 0 = Energy Detected
3	Transmit Pause Enabled	RO	0x0	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17_1.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Transmit pause enabled 0 = Transmit pause disable
2	Receive Pause Enabled	RO	0x0	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17_1.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Receive pause enabled 0 = Receive pause disabled
1:0	Reserved				These bits must be read and left unchanged when performing a write.

Table 91: Interrupt Enable Register[1]
Page 0, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Auto-Negotiation Error Interrupt Enable	R/W	0	Retain	1 = Interrupt enable 0 = Interrupt disable
14	Speed Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
13	Duplex Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
12	Page Received Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable

Table 91: Interrupt Enable Register[1] (Continued)
Page 0, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
11	Auto-Negotiation Completed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
10	Link Status Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
9	Symbol Error Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
8	False Carrier Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
7	FIFO Over/ Underflow Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
6	MDI Crossover Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
5	Downshift Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
4	Energy Detect Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
3	Reserved				This bit must be read and left unchanged when performing a write.
2	DTE power detection status changed interrupt enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
1	Polarity Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
0	Jabber Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable

1. Interrupts should only be enabled during normal operation (not in test modes, power down, etc.).

Table 92: Interrupt Enable Register[1] - Fiber
Page 1, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved				This bit must be read and left unchanged when performing a write.
14	Speed Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable

Table 92: Interrupt Enable Register[1] - Fiber (Continued)
Page 1, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
13	Duplex Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
12	Page Received Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
11	Auto-Negotiation Completed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
10	Link Status Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
9	Symbol Error Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
8	False Carrier Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
7	FIFO Over/ Underflow Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
6:5	Reserved				These bits must be read and left unchanged when performing a write.
4	Fiber Energy Detect Interrupt Enable	R/W	0x0	Retain	This bit only has effect when auto-media detect is enabled or mode is 0000, 0110 or 1110. 1 = Interrupt enable 0 = Interrupt disable
3:0	Reserved				These bits must be read and left unchanged when performing a write.

1. Interrupts should only be enabled during normal operation (not in test modes, power down, etc.).

Table 93: Interrupt Status Register
Page 0, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Auto-Negotiation Error	RO, LH	0	0	An error is said to occur if MASTER/SLAVE does not resolve, parallel detect fault, no common HCD, or link does not come up after negotiation is completed. 1 = Auto-Negotiation 0 = No Auto-Negotiation
14	Speed Changed	RO,LH	0x0	0x0	1 = Speed changed 0 = Speed not changed
13	Duplex Changed	RO,LH	0x0	0x0	1 = Duplex changed 0 = Duplex not changed
12	Page Received	RO,LH	0x0	0x0	1 = Page received 0 = Page not received

Table 93: Interrupt Status Register (Continued)
Page 0, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
11	Auto-Negotiation Completed	RO,LH	0x0	0x0	1 = Auto-Negotiation completed 0 = Auto-Negotiation not completed
10	Link Status Changed	RO,LH	0x0	0x0	1 = Link status changed 0 = Link status not changed
9	Symbol Error	RO,LH	0x0	0x0	1 = Symbol error 0 = No symbol error
8	False Carrier	RO,LH	0x0	0x0	Does not apply for 1000Mbs. 1 = False carrier 0 = No false carrier
7	FIFO Over/ Underflow	RO,LH	0x0	0x0	1 = Over/Underflow Error 0 = No FIFO Error
6	MDI Crossover Changed	RO,LH	0x0	0x0	1 = Crossover changed 0 = Crossover not changed
5	Downshift Interrupt	RO,LH	0x0	0x0	1 = Downshift detected 0 = No down shift
4	Energy Detect Changed	RO,LH	0x0	0x0	1 = Bit 17.4 (Sleep state status) changed0 = Bit 17.4 (Sleep state status) did not change
3	Reserved				This bit must be read and left unchanged when performing a write.
2	DTE power detection status changed interrupt	RO,LH	0x0	0x0	1 = DTE power detection status changed 0 = No DTE power detection status change detected
1	Polarity Changed	RO,LH	0x0	0x0	1 = Polarity Changed 0 = Polarity not changed
0	Jabber	RO,LH	0x0	0x0	1 = Jabber 0 = No jabber

Table 94: Interrupt Status Register
Page 1, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved				This bit must be read and left unchanged when performing a write.
14	Speed Changed	RO,LH	0x0	0x0	1 = Speed changed 0 = Speed not changed
13	Duplex Changed	RO,LH	0x0	0x0	1 = Duplex changed 0 = Duplex not changed
12	Page Received	RO,LH	0x0	0x0	1 = Page received 0 = Page not received

Table 94: Interrupt Status Register
Page 1, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
11	Auto-Negotiation Completed	RO,LH	0x0	0x0	1 = Auto-Negotiation completed 0 = Auto-Negotiation not completed
10	Link Status Changed	RO,LH	0x0	0x0	1 = Link status changed 0 = Link status not changed
9	Symbol Error	RO,LH	0x0	0x0	1 = Symbol error 0 = No symbol error
8	False Carrier	RO,LH	0x0	0x0	1 = False carrier 0 = No false carrier
7	FIFO Over/ Underflow	RO,LH	0x0	0x0	1 = Over/Underflow Error 0 = No FIFO Error
6:5	Reserved				These bits must be read and left unchanged when performing a write.
4	Fiber Energy Detect Changed	RO	0x0	0x0	Fiber Energy Detect changed has effect only when mode is 0000, 0110 or 1110. 1 = Fiber Energy Detect state changed 0 = No Fiber Energy Detect state change detected
3:0	Reserved				These bits must be read and left unchanged when performing a write.

Table 95: Extended PHY Specific Control Register
Page Any, Register 20

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Block Carrier Extension Bit	R/W	0x0	Update	Applies to the following modes in receive direction 1011,0011,0110,1111,0111 and 1110 Applies to the following modes in transmit direction 0000,0100,1000 and 1100 1 = Enable Block Carrier Extension 0 = Disable Block Carrier Extension Refer to the White Paper TRR Byte Stuffing and MACs for details.
14	Line Loopback	R/W	0x0	0x0	1 = Enable Line Loopback 0 = Normal Operation
13	Reserved				This bit must be read and left unchanged when performing a write.
12	Disable Link Pulses	R/W	0x0	0x0	1 = Disable Link Pulse 0 = Enable Link Pulse

Table 95: Extended PHY Specific Control Register (Continued)
Page Any, Register 20

Bits	Field	Mode	HW Rst	SW Rst	Description
11:9	Downshift counter	R/W	0x6	Update	Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by software reset to take effect. 1x, 2x, ...8x is the number of times the PHY attempts to establish Gigabit link before the PHY downshifts to the next highest speed. 000 = 1x 100 = 5x 001 = 2x 101 = 6x 010 = 3x 110 = 7x 011 = 4x 111 = 8x Note: Bit 9 is set to 0 when mode is one of these: 0010, 0011, 0111, 1000, 1001, 1100 or 1101.
8	Downshift Enable	R/W	0x0	Update	Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by software reset to take effect. This bit is set to 0 when mode is one of these: 0010, 0011, 0111, 1000, 1001, 1100 or 1101. 0 = Disable downshift. 1 = Enable downshift.
7	RGMII Receive Timing Control	R/W	0x0	Update	Changes to this bit are disruptive to the normal operation; hence, any change to this register must be followed by software reset to take effect. 1 = Add delay to RX_CLK for RXD Outputs. See"RGMII/RTBI Delay Timing for different RGMII/RTBI Modes" on page 213.
6:4	Default MAC interface speed (Bits 5:4 also determine the speed of operation in GMII/RGMII to SGMII mode when SGMII Auto-Negotiation is disabled.)	R/W	0x6	Update	Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by software reset to take effect. MAC Interface Speed during Link down while Auto-Negotiation is enabled. Bit Speed TX_CLK speed -link down TX_CLK speed - 1000BASE-T link 000 = 10 Mbps 2.5 MHz 0 MHz 001 = 100 Mbps 25 MHz 0 MHz 01X = 1000 Mbps 0 MHz 0 MHz 100 = 10 Mbps 2.5 MHz 2.5 MHz 101 = 100 Mbps 25 MHz 25 MHz 110 = 1000 Mbps 2.5 MHz 2.5 MHz 111 = 1000 Mbps 25 MHz 25 MHz Note: Bit 5 is set to 1 when mode is one of these: 0010, 0011, 0111, 1000, 1001, 1100 or 1101.
3	Reserved				This bit must be read and left unchanged when performing a write.
2	DTE detect enable	R/W	0x0	Update	1 = Enable DTE detection 0 = Disable DTE detection

Table 95: Extended PHY Specific Control Register (Continued)
Page Any, Register 20

Bits	Field	Mode	HW Rst	SW Rst	Description
1	RGMII Transmit Timing Control	R/W	0x0	Update	Changes to this bit are disruptive to the normal operation; hence, any change to this register must be followed by software reset to take effect. 1 = Add delay to GTX_CLK for TXD Outputs. See"RGMII/RTBI Delay Timing for different RGMII/RTBI Modes" on page 213.
0	Reserved	R/W	0x0	Retain	This bit must be read and left unchanged when performing a write.

Table 96: Receive Error Counter Register
Page Any, Register 21

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Receive Error Count	RO, LH	0x0000	Retain	Counter will peg at 0xFFFF and will not roll over. Both False carrier and symbol errors are reported. The following modes of operation have the receive errors reported from Fiber media. 0011,0111,0110 and 1110. Copper media receive errors are reported in the remaining modes of operation.

Table 97: Extended Address
Page Any, Register 22

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved				These bits must be read and left unchanged when performing a write.
7:0	Page select for registers 0 to 28	R/W	0x00	Retain	Register bits 22.7:0 are used for fiber/copper register identity selection. 0x00 = Selects copper banks of registers 0, 1, 4, 5, 6, 7, 8, 17, 18, 19. 0x01 = Selects fiber banks of registers 0, 1, 4, 5, 6, 7, 8, 17, 18, 19. At the same time register 22.7:0 also selects the VCT™ pair for results to be read from register 28. 0x03 = MDI pair 3 0x02 = MDI pair 2 0x01 = MDI pair 1 0x00 = MDI pair 0 See Table 98 for details. Reg22[7:0] = 01 when Reg27[3:0] is either 0110, 1110, 0011 or 0111 and Reg22[7:0] = 00 when Reg27[3:0] is either 1001, 1101, 1011, 1111 and reg27[15] = 1. When modes is either 0000, 0010, 0100, 1000, 1010, or 1100 and Reg27[15] = 0 and Reg27[9] = 0 then Reg22[7:0] will be 0x00 or 0x01 depends on if the phy is resolved to fiber or copper. If Reg27[15] or Reg27[9] = 1, writing 0x01 to Reg22[7:0] for Fiber registers banks accesses and writing 00 to Reg22[7:0] for Copper registers banks accesses.

Table 98: Register 22[7:0] values for page 0 and 1 of Registers 0, 1, 4, 5, 6, 7, 8, 17, 19

MODE[3:0]	DIS_FC (reg27.15)	Default Bits 22.7:0 No Link	Default Bits 22.7:0 Link Up	Registers Bank Accesses Copper=page 0 Fiber=page1	Disable/ Enable Automatic Medium Register Selection (Reg27.9)	Updates 22.7:0
0000 - SGMII with Clock with SGMII Auto-Neg to Copper	x	"00000000"	"00000000"	Copper/SGMII	x	N/A
0100 - SGMII without Clock with SGMII Auto-Neg to Copper	x	"00000000"	"00000000"	Copper/SGMII	x	N/A
1000 - GBIC	x	"00000000"	"00000000"	Copper/fiber	x	N/A
1100 - 1000BASE-X without Auto-Neg to Copper	x	"00000000"	"00000000"	Copper/fiber	x	N/A
1001 - RTBI to Copper	1	"00000000"	"00000000"	Copper Only	x	N/A
1101 - TBI to Copper	1	"00000000"	"00000000"	Copper Only	x	N/A
0110 - RGMII to SGMII	x	"00000000"	"00000000"	Fiber Only	x	N/A
1110 - GMII to SGMII	x	"00000000"	"00000000"	Fiber Only	x	N/A
0011 - RGMII to Fiber	x	"00000000"	"00000000"	Fiber Only	x	N/A
0111 - GMII to Fiber	x	"00000000"	"00000000"	Fiber Only	x	N/A
1011 - RGMII to Copper	1	"00000000"	"00000000"	Copper Only	x	N/A
1011 - RGMII with Auto-Selection (Resolved to Copper)	0	"00000000"	"00000000"	Copper/fiber	0	Yes
1011 - RGMII with Auto-Selection (Resolved to Fiber)	0	"00000000"	"00000001"	Copper/fiber	1	No
1111 - GMII to Copper	1	"00000000"	"00000000"	Copper Only	x	N/A
1111 - GMII with Auto-Selection (Resolved to Copper)	0	"00000000"	"00000000"	Copper/fiber	0	Yes
1111 - GMII with Auto-Selection (Resolved to Fiber)	0	"00000000"	"00000001"	Copper/fiber	1	No

When mode is 0x01, 0x11, or x110, only fiber registers can be accessed. A write to Register 22 bits[7:0] will not change the pointer to Copper register banks. Similarly, a read from Register 22 bits[7:0] = 0x00 has no indication that copper registers are accessible.

When mode is 1x01 or 1x11 with DIS_FC = 0, both copper or fiber registers are accessible. Register 22 bits[7:0] = 0x00 when the MAC is resolved to Copper and 0x01 when the MAC is resolved to fiber. Register 22 bits[7:0] can be programmed to select copper or fiber register banks. If Disable/Enable Automatic Medium Register Selection bit (Register27.9) = 0, it means that the Register 22 bits[7:0] pointer must be updated which media is to be used. Register 22 bits[7:0] can still be written to to change the pointer to access the other bank.

Table 99: Global Status Register
Page Any, Register 23

Bits	Field	Mode	HW Rst	SW Rst	Description
23.15:1	Reserved				These bits must be read and left unchanged when performing a write.
23.0	Port 0 Interrupt	RO	0	0	1 = Interrupt on Port 0 = No Interrupt on Port Bit will stay high until active interrupts bits cleared on a read of register 19 of the corresponding port.

Table 100: LED Control Register
Page Any, Register 24

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Disable LED	R/W	0x0	Retain	1 = Disable 0 = Enable
14:12	Pulse stretch duration	R/W	0x4	Retain	000 = No pulse stretching 001 = 21 ms to 42ms 010 = 42 ms to 84ms 011 = 84 ms to 170ms 100 = 170 ms to 340ms 101 = 340 ms to 670ms 110 = 670 ms to 1.3s 111 = 1.3s to 2.7s
11	Force Interrupt	R/W	0x0	Retain	1 = Force INTn pin to assert 0 = Normal operation
10:8	Blink Rate	R/W	0x1	Retain	000 = 42 ms 001 = 84 ms 010 = 170 ms 011 = 340 ms 100 = 670 ms 101 to 111 = Reserved
7	LED Duplex Control	R/W	0x0	Retain	See Bit 2
6	LED_TX Control (LSB)	R/W	0x0	Retain	bit 0,6 See section 2.23.2.3 for more details 00 = Transmit activity - solid on 01 = Transmit or receive activity - solid on 10 = Link and no activity - solid on. Transmit or receive activity - blink 11 = Transmit or receive activity - blink
5:3	LED_LINK Control	R/W	0x0	Retain	000 = Direct LED mode 011 = Master/Slave LED mode 001, 010, 100, 111, all other values = See Section 2.23.2.2 "Combined Link LED Modes" on page 113

Table 100: LED Control Register (Continued)
Page Any, Register 24

Bits	Field	Mode	HW Rst	SW Rst	Description
2	LED_ DUPLEX Control	R/W	0x0	Retain	Bit 7,2 - LED DUPLEX Behavior 00 -- Low = Full-duplex, High = Half-duplex, Blink = Collision 01 -- Low = Full-duplex, High = Half-duplex 10 -- Low = Fiber Link Up, High = Fiber Link Down 11 -- Reserved
1	LED_RX Control	R/W	0x0	Retain	See section 2.23.2.3 for more information. 1 = Receive activity/Link 0 = Receive activity
0	LED_TX control (MSB)	R/W	0x0	Retain	See bit 6

Table 101: Manual LED Override Register
Page Any, Register 25

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	SGMII Auto-Negotiation Timer	R/W	0x0	Retain	00 = 1.6 to 2.0 ms 01 = 0.50 to 0.60 us 10 = 0.98 to 1.2 us 11 = 2.1 to 2.3 us
13:12	Reserved				These bits must be read and left unchanged when performing a write.
11:10	LED_ DUPLEX	R/W	0x0	Retain	LED "Off" means LED pin output equals high. LED "On" means LED pin output equals low. 00 = Normal 01 = Blink 10 = LED Off 11 = LED On
9:8	LED_ LINK10	R/W	0x0	Retain	LED "Off" means LED pin output equals high. LED "On" means LED pin output equals low. 00 = Normal 01 = Blink 10 = LED Off 11 = LED On
7:6	LED_ LINK100	R/W	0x0	Retain	LED "Off" means LED pin output equals high. LED "On" means LED pin output equals low. 00 = Normal 01 = Blink 10 = LED Off 11 = LED On
5:4	LED_ LINK1000	R/W	0x0	Retain	LED "Off" means LED pin output equals high. LED "On" means LED pin output equals low. 00 = Normal 01 = Blink 10 = LED Off 11 = LED On

Table 101: Manual LED Override Register (Continued)
Page Any, Register 25

Bits	Field	Mode	HW Rst	SW Rst	Description
3:2	LED_RX	R/W	0x0	Retain	LED "Off" means LED pin output equals high. LED "On" means LED pin output equals low. 00 = Normal 01 = Blink 10 = LED Off 11 = LED On
1:0	LED_TX	R/W	0x0	Retain	LED "Off" means LED pin output equals high. LED "On" means LED pin output equals low. 00 = Normal 01 = Blink 10 = LED Off 11 = LED On

Table 102: Extended PHY Specific Control 2 Register
Page Any, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved				This bit must be read and left unchanged when performing a write.
14	FCT PLL loop Bandwidth control	R/W	0x0	Retain	1 = PLL bandwidth 2.2 Mhz 0 = PLL bandwidth 1.1 Mhz
13	FCT transmitter pre-emphasis Control	R/W	0x0	Retain	1 = High pre-emphasis mode 0 = Low pre-emphasis mode
12	Reserved	R/W	0x0	Retain	Reserved
11:10	Autoselect pre-ferred media	R/W	0x0	Retain	00 = No Preference for Media 01 = Preferred Fiber Medium 10 = Preferred Copper Medium 11 = Reserved
9:8	SERDES pattern generation	R/W	0x0	Retain	When the fiber interface is enabled reg26[9:8] will control the pattern transmitted by the SERDES. Fixed square wave pattern can be generated so jitter can be measured. 0x = normal operation 10 = Generate K28.7 symbols (alternating five 0s and five 1s) 11 = generate D21.5 symbols (alternating 0s and 1s)
7	Enable External Fiber Signal Detect Input	R/W	See Descr	Update	Changes to this bit are disruptive to the normal operation; hence, any changes to these registers must be followed by a software reset to take effect. 1 = Use external hardware pins for signal detect 0 = Force signal detect to be good

Table 102: Extended PHY Specific Control 2 Register (Continued)
Page Any, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
6	Fiber Input Impedance	R/W	See Descr	Update	Changes to this bit are disruptive to the normal operation; hence, any changes to these registers must be followed by software reset to take effect. Upon hardware reset this bit defaults as follows: 75/50 OHM bit 26.6 0 0 1 1 1 = 75 ohm 0 = 50 ohm
5	Fiber Output Impedance	R/W	See Descr	Update	Changes to this bit are disruptive to the normal operation; hence, any changes to these registers must be followed by software reset to take effect. Upon hardware reset this bit defaults as follows: 75/50 OHM Bit 26.5 0 0 1 1 1 = 75 ohm 0 = 50 ohm
4	Fiber Mode Clock Enable	R/W	See Descr	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. Upon hardware reset this bit defaults as follows: HWCFG_MODE[3:0] Bit 26.4 0000 1 0110 1 1110 1 all other configurations 0 1 = Power up TC± drivers to use as output clock 0 = Power down TC± drivers and use TC± as differential signal detect pins To enable fiber mode clock by writing this bit to 0, chip needs to be in one of the following modes: 0010,0011,0111,0110,1110,xx00
3	Reserved				This bit must be read and left unchanged when performing a write.

Table 102: Extended PHY Specific Control 2 Register (Continued)
Page Any, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
2:0	Fiber Output Amplitude (100 ohm differential load) Fiber Output Amplitude (150 ohm differential load)	R/W R/W	010 010	Retain Retain	0.50V - 1.20V = Differential voltage peak-to-peak measured with 100 ohm differential load. 000 = 0.50V 001 = 0.60V 010 = 0.70V 011 = 0.80V 100 = 0.90V 101 = 1.00V 110 = 1.10V 111 = 1.20V 0.62V - 1.32V = Differential voltage peak-to-peak measured with 150 ohm differential load. 000 = 0.62V 001 = 0.72V 010 = 0.82V 011 = 0.92V 100 = 1.02V 101 = 1.12V 110 = 1.22V 111 = 1.32V

Table 103: Extended PHY Specific Status Register
Page Any, Register 27

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Fiber/Copper Auto Selection Disable	R/W	See Descr	Update	Changes to this bit are disruptive to the normal operation; hence, any changes to these registers must be followed by software reset to take effect. Upon hardware reset this bit defaults as follows: DIS_FC Bit 27.15 0 0 1 1 1 = Disable fiber/copper auto-selection 0 = Enable fiber/copper auto-selection
14	Reserved				This bit must be read and left unchanged when performing a write.
13	Fiber/Copper resolution	RO	0x0	Retain	Register 27.13 indicates the resolution of the Fiber/Copper Auto Detection. This bit is valid only when link is up. 1 = Fiber link 0 = Copper link
12	Serial Interface Auto-Negotiation bypass enable	R/W	See Descr	Update	Changes to this bit are disruptive to the normal operation; hence, any changes to these registers must be followed by software reset to take effect. The default value for Register 12 =1 for the following modes: 0111 = GMII to fiber 0011 = RGMII to fiber 1000 = GBIC mode

Table 103: Extended PHY Specific Status Register (Continued)
Page Any, Register 27

Bits	Field	Mode	HW Rst	SW Rst	Description
11	Serial Interface Auto-Negotiation bypass status	RO	0x0	Retain	For SGMII mode, if the bypass logic brings up the serial interface link, copper Auto-Negotiation will restart and advertise only gigabit speed. If this bit is 1, then bit 17_1.11 will be 0. 1 = Serial interface link came up because bypass mode timer timed out and fiber Auto-Negotiation was bypassed. 0 = Serial interface link came up because regular fiber Auto-Negotiation completed.
10	Interrupt Polarity	R/W	See Descr	Update	Changes to this bit are disruptive to the normal operation; hence, any changes to these registers must be followed by software reset to take effect. Default takes the value of INT_POL. 1 = INT active low 0 = INT active high
9	Disable/Enable Automatic Medium Register Selection	R/W	0x0	Retain	1 = Disable automatic medium register selection 0 = Enable automatic medium register selection
8:5	DTE detect status drop hysteresis	R/W	0x4	Retain	0000: report immediately 0001: report 5s after DTE power status drop ... 1111: report 75s after DTE power status drop
4	DTE power status	RO	0x0	Retain	1 = Link partner needs DTE power 0 = Link partner does not need DTE power
3:0	HWCFG_ MODE	R/W	See Descr	Update	Changes to these bits are disruptive to the normal operation; hence, any changes to these registers must be followed by software reset to take effect. Upon hardware reset Register 27.3:0 defaults to the value in HWCFG_MODE[3:0]. 0000 = SGMII with Clock with SGMII Auto-Neg to copper 0100 = SGMII without Clock with SGMII Auto-Neg to copper 1000 = 1000BASE-X without Clock with 1000BASE-X Auto-Neg to copper (GBIC) 1100 = 1000BASE-X without Clock without 1000BASE-X Auto-Neg to copper 0001 = Reserved 0101 = Reserved 1001 = RTBI to Copper 1101 = TBI to copper 0010 = Reserved 0110 = RGMII to SGMII 1010 = Reserved 1110 = GMII to SGMII 0011 = RGMII to Fiber 0111 = GMII to Fiber 1011 = RGMII/Modified MII to Copper 1111 = GMII to copper

Table 104: MDI[0] Virtual Cable Tester® Status Register, Page 0
Page 0, Register 28

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Run VCT™ Test	R/W, SC	0x0	Retain	1 = Run VCT test = VCT test completed 0
14:13	Status	RO	0x0	Retain	MDI[0] ± VCT™ test result 00 = Valid test, normal cable (no short or open in cable) 01 = Valid test, short in cable (Impedance < 33 ohms) 10 = Valid test, open in cable (Impedance greater than 330 ohms) 11 = Test Fail
12:8	Amplitude	RO	0x00	Retain	Amplitude of reflection on pair MDI[0]±.These amplitude bits range from 0x07 to 0x1F. 0x1F = Maximum positive amplitude (+1) 0x10 = Zero amplitude 0x00 = Maximum negative amplitude (-1)
7:0	Distance	RO	0x00	Retain	Approximate distance (± 1m) to the open/short location on Pair MDI[0]±, measured at nominal conditions (room temperature and typical VDDs). Refer to the "VCT™ How to Use TDR Results" application note for distance to fault details.

Table 105: MDI[1] Virtual Cable Tester® Status Register, Page 1
Page 1, Register 28

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Disable waiting period	R/W	0x0	Retain	1 = Start VCT without waiting to bring link down 0 = Wait for link down before starting VCT test
14:13	Status	RO	0x0	Retain	MDI[1] ± VCT test result 00 = Valid test, normal cable (no short or open in cable) 01 = Valid test, short in cable (Impedance < 33 ohms) 10 = Valid test, open in cable (Impedence greater than 330 ohms) 11 = Test Fail
12:8	Amplitude	RO	0x00	Retain	Amplitude of reflection on pair MDI[1]±.These amplitude bits range from 0x07 to 0x1F. 0x1F = Maximum positive amplitude (+1) 0x10 = Zero amplitude 0x00 = Maximum negative amplitude (-1)
7:0	Distance	RO	0x00	Retain	Approximate distance (± 1m) to the open/short location on Pair MDI[1]±, measured at nominal conditions (room temperature and typical VDDs). Refer to the "VCT How to Use TDR Results" application note for distance to fault details.

Table 106: MDI[2] Virtual Cable Tester® Status Register, Page 2

Page 2, Register 28

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved				This bit must be read and left unchanged when performing a write.
14:13	Status	RO	0x0	Retain	MDI[2] ± VCT™ test result 00 = Valid test, normal cable (no short or open in cable) 01 = Valid test, short in cable (Impedance < 33 ohms) 10 = Valid test, open in cable (Impedance greater than 330 ohms) 11 = Test Fail
12:8	Amplitude	RO	0x00	Retain	Amplitude of reflection on pair MDI[2]±.These amplitude bits range from 0x07 to 0x1F. 0x1F = Maximum positive amplitude (+1) 0x10 = Zero amplitude 0x00 = Maximum negative amplitude (-1)
7:0	Distance	RO	0x00	Retain	Approximate distance (± 1m) to the open/short location on Pair MDI[2]±, measured at nominal conditions (room temperature and typical VDDs). Refer to the "VCT How to Use TDR Results" application note for distance to fault details.

Table 107: MDI[3] Virtual Cable Tester® Status Register, Page 3

Page 3, Register 28

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved				This bit must be read and left unchanged when performing a write.
14:13	Status	RO	0x0	Retain	MDI[3] ± VCT test result 00 = Valid test, normal cable (no short or open in cable) 01 = Valid test, short in cable (Impedance < 33 ohms) 10 = Valid test, open in cable (Impedance greater than 330 ohms) 11 = Test Fail
12:8	Amplitude	RO	0x00	Retain	Amplitude of reflection on pair MDI[3]±.These amplitude bits range from 0x07 to 0x1F. 0x1F = Maximum positive amplitude (+1) 0x10 = Zero amplitude 0x00 = Maximum negative amplitude (-1)
7:0	Distance	RO	0x00	Retain	Approximate distance (± 1m) to the open/short location on Pair MDI[3]±, measured at nominal conditions (room temperature and typical VDDs). Refer to the "VCT How to Use TDR Results" application note for distance to fault details.

Note Page 0-3 reg 28{14:0] are valid after the completion of VCT™ (Page 0, bit 28.15 is 0).

Table 108: 1000 BASE-T Pair Skew Register, Page 4
Page 4, Register 28

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Pair 7,8 (MDI[3]±)	RO	0x0	0x0	Skew = Bit value x 8 ns. Value is correct to within ± 8ns.
11:8	Pair 4,5 (MDI[2]±)	RO	0x0	0x0	Skew = Bit value x 8 ns. Value is correct to within ± 8ns.
7:4	Pair 3,6 (MDI[1]±)	RO	0x0	0x0	Skew = Bit value x 8 ns. Value is correct to within ± 8ns.
3:0	Pair 1,2 (MDI[0]±)	RO	0x0	0x0	Skew = Bit value x 8 ns. Value is correct to within ± 8ns. The contents of 28_4.15:0 are valid only if Register 28_5.6 = 1

Table 109: 1000 BASE-T Pair Swap and Polarity, Page 5

Page 5, Register 28

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved				These bits must be read and left unchanged when performing a write.
6	Register 28_4 and 28_5 are valid	RO	0x0	0x0	1= Valid 0 = Invalid
5	C, D Crossover	RO	0x0	0x0	1 = Channel C received on MDI[2]± Channel D received on MDI[3]± 0 = Channel D received on MDI[2]± Channel C received on MDI[3]±
4	A, B Crossover	RO	0x0	0x0	1 = Channel A received on MDI[0]± Channel B received on MDI[1]± 0 = Channel B received on MDI[0]± Channel A received on MDI[1]±
3	Pair 7,8 (MDI[3]±) Polarity	RO	0x0	0x0	1 = Negative 0 = Positive
2	Pair 4,5 (MDI[2]±) Polarity	RO	0x0	0x0	1 = Negative 0 = Positive
1	Pair 3,6 (MDI[1]±) Polarity	RO	0x0	0x0	1 = Negative 0 = Positive
0	Pair 1,2 (MDI[0]±) Polarity	RO	0x0	0x0	1 = Negative 0 = Positive The contents of 28_5.15:0 are valid only if Register 28_5.6 = 1

Table 110: Extended Address

Page Any, Register 29

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved				These bits must be read and left unchanged when performing a write.
4:0	Page select	R/W	0x00	Retain	00000 = No register 30 page access or Page 0 of register 30 00011 = Select Page 3 of register 30 00111 = Select Page 7 of register 30 01100 = Select Page 12 of register 30 10000 = Select Page 16 of register 30 10010 = Select Page 18 or register 30

Table 111: Calibration Override
Page 3, Register 30

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Restart Calibration	R/W, SC	0x0	Retain	Calibration will start once bit 15 is set to 1. 0 = Normal 1 = Restart
14	Calibration Complete	RO	0x0	Retain	Calibration is done once bit 14 becomes 1. 0 = Not done 1 = Done
13	Reserved				This bit must be read and left unchanged when performing a write.
12:8	PMOS Value	R/W	See Descr	Retain	00000 = All fingers off 11111 = All fingers on Register reflects on the calibrated value after hardware reset.
7	Reserved				This bit must be read and left unchanged when performing a write.
6	LATCH	R/W, SC	0x0	Retain	1 = Latch in new value Once LATCH is set to 1 the new calibration value is written into the I/O pad. The automatic calibrated value is lost.
5	PMOS/NMOS Select	R/W	0x0	Retain	1 = PMOS 0 = NMOS If select set to 1 the PMOS value is written into when LATCH is set to 1. If select set to 0 the NMOS value is written into when LATCH is set to 0.
4:0	NMOS value	R/W	See Descr	Retain	00000 = All fingers off 11111 = All fingers on Register reflects on the calibrated value after hardware reset.

Table 112: Force Gigabit Mode
Page 7, Register 30

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved				These bits must be read and left unchanged when performing a write.
3	Force Gigabit Mode	R/W	0	Retain	The Force Gigabit Mode bit is used for the Gigabit stub loopback mode. See Section 2.15.3.2 "Enabling 1000 Mbps Stub Loopback" on page 99 for details. 1 = Forced Gigabit 0 = Not forced
2:0	Reserved				These bits must be read and left unchanged when performing a write.

Table 113: Transmitter Type
Page 11, Register 30

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Transmitter Type	R/W	0	Retain	1 = Class A 0 = Class B
14:0	Reserved				These bits must be read and left unchanged when performing a write.

Table 114: CRC checker result
Page 12, Register 30

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Frame count	RO	0x00	Retain	Frame count is stored in these bits. 00000000 = No frame counted 11111111 = Maximum number of frames counted The counter does not clear on a read command. To clear the CRC error counter, disable the crc_checker (Register 30_16.15 = 0).
7:0	CRC error count	RO	0x00	Retain	Error counter is stored in these bits. 00000000 = No frame counted 11111111 = Maximum number of frame counted The counter does not clear on a read command. To clear the CRC error counter, disable the crc_checker (Register 30_16.15 = 0).

Table 115: Test Enable Control
Page 16, Register 30

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved				These bits must be read and left unchanged when performing a write.

Table 115: Test Enable Control
Page 16, Register 30

Bits	Field	Mode	HW Rst	SW Rst	Description
1	Enable Gigabit Stub Loopback	R/W	0x0	Retain	1 = Enable Gigabit Stub loopback 0 = Normal operation
0	Enable CRC checker	R/W	0x0	Retain	1 = Enable CRC checker 0 = Disable CRC checker, clear frame counter and CRC error counter (Register 30_1215:0 = 0x0000)

Table 116: Miscellaneous Control
Page 18, Register 30

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	RW	0x8	Retain	These bits must be read and left unchanged when performing a write.
11:9	Calibration PMOS Target Impedance	RW	0x1	Retain	000 = 52 ohm 001 = 45 ohm 010 = 36 ohm 011 = 32 ohm 100 = 30 ohm 101 = 25 ohm 110 = 24 ohm 111 = 22 ohm
8:6	Calibration NMOS Target Impedance	RW	0x1	Retain	000 = 56 ohm 001 = 43 ohm 010 = 39 ohm 011 = 33 ohm 100 = 29 ohm 101 = 27 ohm 110 = 24 ohm 111 = 23 ohm
5:2	Packet Generator	RW	0x00	Retain	Bit 5: 1 = Packet generation enable, 0 = Disable Bit 4: 0 = Random, 1 = 0x5a (packet pattern select) Bit 3: 0 = 64 byte, 1 = 1518 byte (packet length select) Bit 2: 1 = Generate error packet, 0 = No error
1	Reserved	RW	0x00	Retain	These bits must be read and left unchanged when performing a write.
0	Turn off NEXT Canceller	RW	0x0	Retain	0 = Enable NEXT 1 = Disable NEXT

Table 117: Reserved Registers
Page Any, Register 31

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Reserved				These bits must be read and left unchanged when performing a write.

4 Electrical Specifications

4.1 Absolute Maximum Ratings

Table 118: Absolute Maximum Ratings

Stresses above those listed in Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Symbol	Parameter	Min	Typ	Max	Units
A_{VDD}	Power Supply Voltage on VDDA with respect to VSS	-0.5		2.75	V
D_{VDD}	Power Supply Voltage on DVDD with respect to VSS	-0.5		1.32	V
V_{DDO}	Power Supply Voltage on VDDO with respect to VSS	-0.5		2.75	V
V_{PIN}	Voltage applied to any input pin	-0.5		3.6	V
$T_{STORAGE}$	Storage temperature	-55		+125[1]	°C

1. 125 °C is only used as bake temperature for not more than 24 hours. Long term storage (e.g weeks or longer) should be kept at 85 °C or lower.

4.2 Recommended Operating Conditions

Table 119: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
A_{VDD}	AVDD supply[1]	For AVDD	2.37	2.5	2.63	V
D_{VDD}	DVDD supply	For DVDD	0.95	1.0[2]	1.05	V
V_{DDO}	VDDO supply	For VDDO, VDDOH, VDDOX	2.37	2.5	2.63	V
RSET	Internal bias reference	Resistor connected to V_{SS}		5000 ± 1% Tolerance		Ω
T_A	Ambient operating temperature	Commercial Parts	0		70[3]	°C
		Industrial Parts[4]	-40		85	°C
T_J	Maximum junction temperature				125[3]	°C

1. Although VDDOH, VDDOX, and VDDO can operate over a wide range, only the voltage ranges specified are tested and guaranteed.
2. Instead of 1.0V, 1.2V can be used.
3. Refer to White Paper on "TJ Thermal Calculations" for more information.
4. Industrial part numbers have an "I" following the commercial part numbers. See Section 6.1 "Part Order Numbering" on page 247.

4.3 Package Thermal Information

4.3.1 Thermal Conditions for 117-Pin TFBGA Package

Table 120: Thermal Conditions for 117-Pin TFBGA Package

Symbol	Parameter	Condition	Min	Typ	Max	Units
θ_{JA}	Thermal resistance - junction to ambient of the 88E1111 device 117-Pin TFBGA package $\theta_{JA} = (T_J - T_A)/ P$ P = Total Power Dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		38.30		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		33.90		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		32.00		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		30.90		°C/W
ψ_{JT}	Thermal characteristic parameter[1] - junction to top center of the 88E1111 device 117-Pin TFBGA package $\psi_{JT} = (T_J - T_c)/P.$ P = Total Power Dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		0.27		°C/W
θ_{JC}	Thermal resistance[1] - junction to case of the 88E1111 device 117-Pin TFBGA package $\theta_{JC} = (T_J - T_C)/ P_{Top}$ P_{Top} = Power Dissipation from the top of the package	JEDEC with no air flow		10.10		°C/W
θ_{JB}	Thermal resistance[1] - junction to board of the 88E1111 device 117-Pin TFBGA package $\theta_{JB} = (T_J - T_B)/ P_{bottom}$ P_{bottom} = power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow		31.10		°C/W

1. Refer to white paper on TJ Thermal Calculations for more information.

4.3.2 Thermal Conditions for 96-Pin aQFN Package

Table 121: Thermal Conditions for 96-Pin aQFN Package

Symbol	Parameter	Condition	96-Pin BCC and 96-Pin aQFN Packages			Units
			Min	Typ	Max	
θ_{JA}	Thermal resistance - junction to ambient of the 88E1111 device 96-Pin BCC and 96-Pin aQFN package $\theta_{JA} = (T_J - T_A)/ P$ P = Total Power Dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		25.00		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		23.60		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		20.90		°C/W
ψ_{JT}	Thermal characteristic parameter[1] - junction to top center of the 88E1111 device 96-Pin BCC and 96-Pin aQFN package $\psi_{JT} = (T_J - T_c)/P.$ P = Total Power Dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		1.3		°C/W
θ_{JC}	Thermal resistance[1] - junction to case of the 88E1111 device 96-Pin BCC and 96-Pin aQFN package $\theta_{JC} = (T_J - T_C)/ P_{Top}$ P_{Top} = Power Dissipation from the top of the package	JEDEC with no air flow		20.50		°C/W
θ_{JB}	Thermal resistance[1] - junction to board of the 88E1111 device 96-Pin BCC and 96-Pin aQFN package $\theta_{JB} = (T_J - T_B)/ P_{bottom}$ P_{bottom} = power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow		9.60		°C/W

1. Refer to white paper on TJ Thermal Calculations for more information.

Note

The 96-Pin aQFN package is a pin compatible replacement for the 96-Pin BCC package. See Product Change Notification 1210066 and Table 186 for details.

4.3.3 Thermal Conditions for 128-Pin PQFP Package

Table 122: Thermal Conditions for 128-Pin PQFP Package

Symbol	Parameter	Condition	Min	Typ	Max	Units
θ_{JA}	Thermal resistance - junction to ambient of the 88E1111 device 128-Pin PQFP package $\theta_{JA} = (T_J - T_A)/ P$ P = Total Power Dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		34.50		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		31.50		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		30.20		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		29.50		°C/W
ψ_{JT}	Thermal characteristic parameter[1] - junction to top center of the device 128-Pin PQFP package $\psi_{JT} = (T_J - T_C)/P.$ P = Total Power Dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		3.22		°C/W
θ_{JC}	Thermal resistance[1] - junction to case of the 88E1111 device 128-Pin PQFP package $\theta_{JC} = (T_J - T_C)/ P_{Top}$ P_{Top} = Power Dissipation from the top of the package	JEDEC with no air flow		17.40		°C/W
θ_{JB}	Thermal resistance[1] - junction to board of the 88E1111 device 128-Pin PQFP package $\theta_{JB} = (T_J - T_B)/ P_{bottom}$ P_{bottom} = power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow		26.60		°C/W

1. Refer to white paper on TJ Thermal Calculations for more information.

4.4 DC Electrical Characteristics

4.4.1 Current Consumption AVDD

Table 123: Current Consumption AVDD

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ[1]	Max	Units
I_{AVDD}	2.5V Power to analog core	AV_{DD}	GMII/RGMII/TBI/RTBI over 1000BASE-T with traffic		160		mA
			SERDES/SGMII over 1000BASE-T with traffic		210		mA
			SERDES/SGMII over 100BASE-TX with traffic		117		mA
			SERDES/SGMII over 10BASE-T with traffic		100		mA
			GMII/RGMII over SGMII or GMII/RGMII over 1000BASE-X with traffic		9		mA
			RGMII/MII over 100BASE-TX with traffic		70		mA
			RGMII/MII over 10BASE-T with traffic		52		mA
			COMA		0		mA
			Sleep (Energy Detect and Energy Detect+™)		17		mA
			Power Down		13		mA

1. The values listed are typical values with six LEDs per port and Auto-Negotiation on.

4.4.2 Current Consumption VDDO, VDDOX, VDDOH

Table 124: Current Consumption VDDO, VDDOX, VDDOH

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ[1]	Max	Units
I_{VDDO}	2.5V Power to outputs	V_{DDO}, V_{DDOX}, V_{DDOH}	GMII/RGMII/TBI/RTBI over 1000BASE-T with traffic		37		mA
			SERDES/SGMII over 1000BASE-T with traffic		15		mA
			SERDES/SGMII over 100BASE-TX with traffic		15		mA
			SERDES/SGMII over 10BASE-T with traffic		15		mA
			GMII/RGMII over SGMII or GMII/RGMII over 1000BASE-X with traffic		39		mA
			RGMII/MII over 100BASE-TX with traffic		10		mA
			RGMII/MII over 10BASE-T with traffic		8		mA
			COMA		0		mA
			Sleep (Energy Detect and Energy Detect+™)		19		mA
			Power Down		9		mA

1. The values listed are typical values with six LEDs per port and Auto-Negotiation on.

4.4.3 Current Consumption Center_Tap

Table 125: Current Consumption Center_Tap
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ[1]	Max	Units
I_{CENTER_TAP}	2.5V Power to center tap	External Magnetics Center Tap Pin	GMII/RGMII/TBI/RTBI over 1000BASE-T with traffic (CLASS B Drivers used)		92.5		mA
			GMII/RGMII/TBI/RTBI over 1000BASE-T with traffic (CLASS A Drivers used)		184		mA
			SERDES/SGMII over 1000BASE-T with traffic		95		mA
			SERDES/SGMII over 100BASE-TX with traffic		25		mA
			SERDES/SGMII over 10BASE-T with traffic		68		mA
			RGMII/MII over 100BASE-TX with traffic		26		mA
			RGMII/MII over 10BASE-T with traffic		75		mA
			COMA		0		mA
			Sleep (Energy Detect and Energy Detect+™)		0		mA
			Power Down		0		mA

1. The values listed are typical values with six LEDs per port and Auto-Negotiation on.

4.4.4 Current Consumption DVDD (1.0V)

Table 126: Current Consumption DVDD (1.0V)
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ[1]	Max	Units
I_{DVDD}	1.0V Power to digital core	DV_{DD}	GMII/RGMII/TBI/RTBI over 1000BASE-T with traffic		205		mA
			SERDES/SGMII over 1000BASE-T with traffic		207		mA
			SERDES/SGMII over 100BASE-TX with traffic		32		mA
			SERDES/SGMII over 10BASE-T with traffic		18		mA
			GMII/RGMII over SGMII or GMII/RGMII over 1000BASE-X with traffic		20		mA
			RGMII/MII over 100BASE-TX with traffic		28		mA
			RGMII/MII over 10BASE-T with traffic		14		mA
			COMA		6		mA
			Sleep (Energy Detect and Energy Detect+™)		8		mA
			Power Down		8		mA

1. The values listed are typical values with six LEDs per port and Auto-Negotiation on.

4.4.5 Current Consumption DVDD (1.2V)

Table 127: Current Consumption DVDD (1.2V)
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ[1]	Max	Units
I_{DVDD}	1.2V Power to digital core	DV_{DD}	GMII/RGMII/TBI/RTBI over 1000BASE-T with traffic		250		mA
			SERDES/SGMII over 1000BASE-T with traffic		253		mA
			SERDES/SGMII over 100BASE-TX with traffic		40		mA
			SERDES/SGMII over 10BASE-T with traffic		22		mA
			GMII/RGMII over SGMII or GMII/RGMII over 1000BASE-X with traffic		25		mA
			RGMII/MII over 100BASE-TX with traffic		35		mA
			RGMII/MII over 10BASE-T with traffic		17		mA
			COMA		8		mA
			Sleep (Energy Detect and Energy Detect+™)		10		mA
			Power Down		10		mA

1. The values listed are typical values with six LEDs per port and Auto-Negotiation on.

4.5 DC Operating Conditions

4.5.1 Digital Pins

4.5.1.1 VDDOH

Table 128: VDDOH

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins[1]	Condition	Min	Typ	Max	Units
VIH_ VDDOH	Input high voltage VDDOH	All digital inputs on VDDOH	VDDOH = 2.5V	2.0		3.47	V
VIL_ VDDOH	Input low voltage VDDOH	All digital inputs on VDDOH	VDDOH = 2.5V	-0.3		0.8	V
VOH_ VDDOH	High level output voltage VDDOH	All digital outputs on VDDOH	IOH = -4 mA	VDDOH - 0.2V			V
VOL_ VDDOH	Low level output voltage VDDOH	All digital outputs on VDDOH except LED	IOL = 4 mA			0.2	V
VOL_LED	Low level output voltage LED	All digital LED outputs	IOL = 8 mA			0.2	V

1. VDDOH supplies CONFIG[4:0], GCONFIG0, GCONFIG1, SEL_FREQ, XTAL1, XTAL2, LED_LINK10, LED_LINK100, LED_LINK1000, LED_DUPLEX, LED_RX, LED_TX. Although VDDOH requires 2.5V, these digital input pins are 3.3V tolerant.

4.5.1.2 VDDOX

Table 129: VDDOX

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins[1]	Condition	Min	Typ	Max	Units
VIH_ VDDOX	Input high voltage VDDOX	All digital inputs on VDDOX	VDDOX = 2.5V	2.0		3.47	V
VIL_ VDDOX	Input low voltage VDDOX	All digital inputs on VDDOX	VDDOX = 2.5V	-0.3		0.8	V
VOH_ VDDOX	High level output voltage VDDOX	All digital outputs on VDDOX	IOH = -4 mA VDDOX = 2.5V	VDDOX - 0.2V			V
VOL_ VDDOX	Low level output voltage VDDOX	All digital outputs on VDDOX	IOL = 4 mA VDDOX = 2.5V			0.4	V

1. VDDOX supplies RESET, COMA, MDC, MDIO, CLK125, INT, TDI, TMS, TCK, TRSTn, TDO. Although VDDOX requires 2.5V, these digital input pins are 3.3V tolerant.

4.5.1.3 VDDO

Table 130: VDDO

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins[1]	Condition	Min	Typ	Max	Units
VIH_ VDDO	Input high voltage VDDO	All digital inputs on VDDO	VDDO = 2.5V	1.7[2]		3.47	V
VIL_ VDDO	Input low voltage VDDO	All digital inputs on VDDO	VDDO = 2.5V	-0.3		0.8	V
VOH_ VDDO	High level output voltage VDDO	All digital outputs on VDDO	IOH = -4 mA	VDDO - 0.2V			V
VOL_ VDDO	Low level output voltage VDDO	All digital outputs on VDDO except LED	IOL = 4 mA			0.2	V

1. VDDO supplies GTX_CLK, TX_CLK, TX_EN, TX_ER, TXD[7:0], RX_CLK, RX_DV, RX_ER, RXD[7:0], CRS, and COL. The input pins that are listed are 3.3V tolerant.
2. The VIH values in this DC table are not to be confused with the VIH values in the AC table. See IEEE Clause 35 GMII interface description for details.

4.5.1.4 MISC

Table 131: MISC

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
IILK	Input leakage current	With internal pull-up resistor				+10[1] -50	uA
		All others without resistor				±10	uA
CIN	Input capacitance	All pins				5	pF

1. "+" is current into pin, "-" is current out of pin.

4.5.2 Internal Resistor Description

Table 132: Internal Resistor Description

117-Pin TFBGA Pin #	96-Pin BCC Pin #	128-Pin PQFP Pin #	Pin Name	Resistor
L7	44	67	TDI	150 kohm Internal pull-up
L8	46	69	TMS	150 kohm Internal pull-up
L9	49	70	TCK	150 kohm Internal pull-up
M9	47	68	TRSTn	150 kohm Internal pull-up
H8	56	77	SEL_FREQ	Internal pull-up
			Others	none

4.6 IEEE DC Transceiver Parameters

Table 133: IEEE DC Transceiver Parameters

IEEE tests are typically based on template and cannot simply be specified by a number. For an exact description of the template and the test conditions, refer to the IEEE specifications.
-- 10BASE-T IEEE 802.3 Clause 14
-- 100BASE-TX ANSI X3.263-1995

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
V_{ODIFF}	Absolute peak differential output voltage	MDI[1:0]	10BASE-T no cable	2.2	2.5	2.8	V
		MDI[1:0]	10BASE-T cable model	585[1]			mV
		MDI[1:0]	100BASE-TX mode	0.950	1	1.050	V
		MDI[3:0]	1000BASE-T[2]	0.67	0.75	0.82	V
	Overshoot[2]	MDI[1:0]	100BASE-TX mode	0		5%	V
	Amplitude Symmetry (positive/ negative)	MDI[1:0]	100BASE-TX mode	0.98x		1.02x	V+/V-
V_{IDIFF}	Peak Differential Input Voltage	MDI[1:0]	10BASE-T mode	585[3]			mV
	Signal Detect Assertion	MDI[1:0]	100BASE-TX mode	1000	460[4]		mV peak-peak
	Signal Detect De-assertion	MDI[1:0]	100BASE-TX mode	200	360[5]		mV peak-peak

1. IEEE 802.3 Clause 14, Figure 14.9 shows the template for the “far end” wave form. This template allows as little as 495 mV peak differential voltage at the far end receiver.
2. IEEE 802.3ab Figure 40 -19 points A&B.
3. The input test is actually a template test ; IEEE 802.3 Clause 14, Figure 14.17 shows the template for the receive wave form.
4. The ANSI TP-PMD specification requires that any received signal with peak-to-peak differential amplitude greater than 1000 mV should turn on signal detect (internal signal in 100BASE-TX mode). The 88E1111 device will accept signals typically with 460 mV peak-to-peak differential amplitude.
5. The ANSI TP-PMD specification requires that any received signal with peak-to-peak differential amplitude less than 200 mV should de-assert signal detect (internal signal in 100BASE-TX mode). The 88E1111 device will reject signals typically with peak-to-peak differential amplitude less than 360 mV.

4.6.1 Serial and SGMII Interface

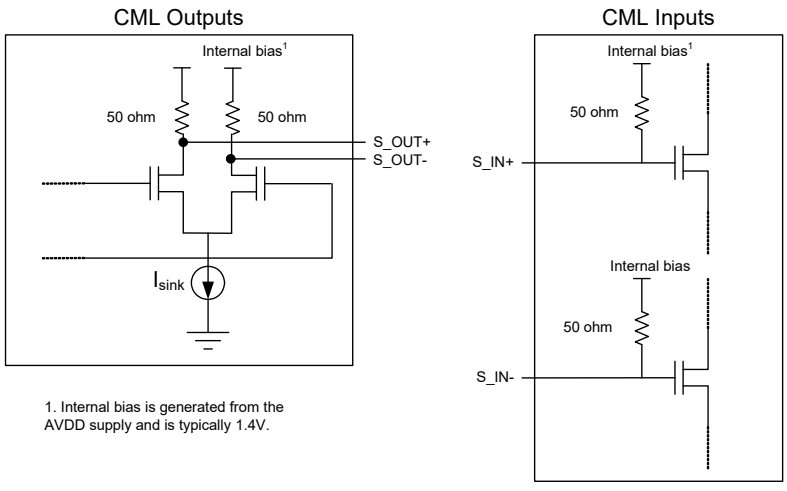
4.6.1.1 Transmitter DC Characteristics

Table 134: Transmitter DC Characteristics

Symbol	Parameter[1]	Min	Typ	Max	Units
V_{OH}	Output Voltage High			1600	mV
V_{OL}	Output Voltage Low	800			mV
V_{RING}	Output Ringing			10	mV
$\|V_{ODI}\|^2$	Output Voltage Swing (differential, peak)	Programmable - see Table 102.			mV peak
V_{OS}	Output Offset Voltage	Variable - see 4.6.1.2 for details.			mV
R_O	Output Impedance (single-ended) (50 ohm termination)	40		60	ohm
	Output Impedance (single-ended) (75 ohm termination)	60		90	
Delta R_O	Mismatch in a pair			10	%
Delta V_{OD}	Change in V_{OD} between 0 and 1			25	mV
Delta V_{OS}	Change in V_{OS} between 0 and 1			25	mV
I_{S+}, I_{S-}	Output current on short to VSS			40	mA
I_{S+-}	Output current when S_OUT+ and S_OUT- are shorted			12	mA
I_{X+}, I_{X-}	Power off leakage current			10	mA

1. See Section 2.1.1.2 "Fiber Interface" on page 50 for details. Parameters are measured with outputs AC connected with 100 ohm differential load.
2. Output amplitude is programmable by writing to Register 26.2:0.

Figure 44: CML I/Os



4.6.1.2 Common Mode Voltage (Voffset) Calculations

There are four different main configurations for the SGMII/Fiber interface connections. These are:

- DC connection to an LVDS receiver
- AC connection to an LVDS receiver
- DC connection to an CML receiver
- AC connection to an CML receiver

If AC coupling or DC coupling to an LVDS receiver is used, the DC output levels are determined by the following:

- The output voltage swing is programmed by Register 26_2.2:0 (see Table 102).
- Voffset (i.e., common mode voltage) = Internal bias - Single-ended peak-peak voltage swing. See Figure 45 for details.

If DC coupling is used with a CML receiver, then the DC levels will be determined by a combination of the MACs output structure, and the 88E1111 input structure shown in the CML Inputs diagram in Figure 46. Assuming the same MAC CML voltage levels and structure, the common mode output levels will be determined by:

- Voffset (i.e., common mode voltage) = Internal bias - Single-ended peak-peak voltage swing/2. See Figure 46 for details.

Figure 45: AC connections (CML or LVDS receiver) or DC connection LVDS receiver

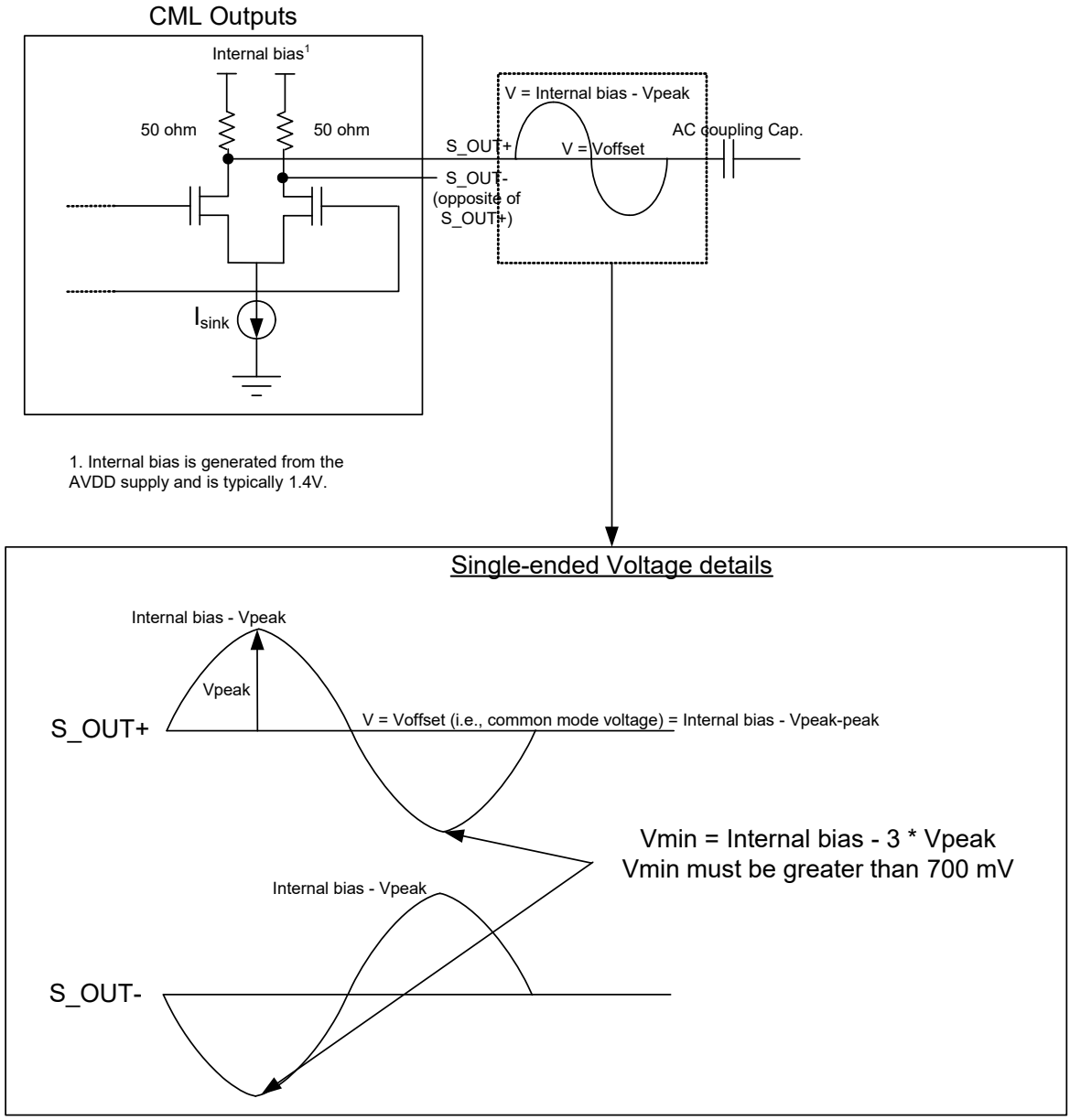
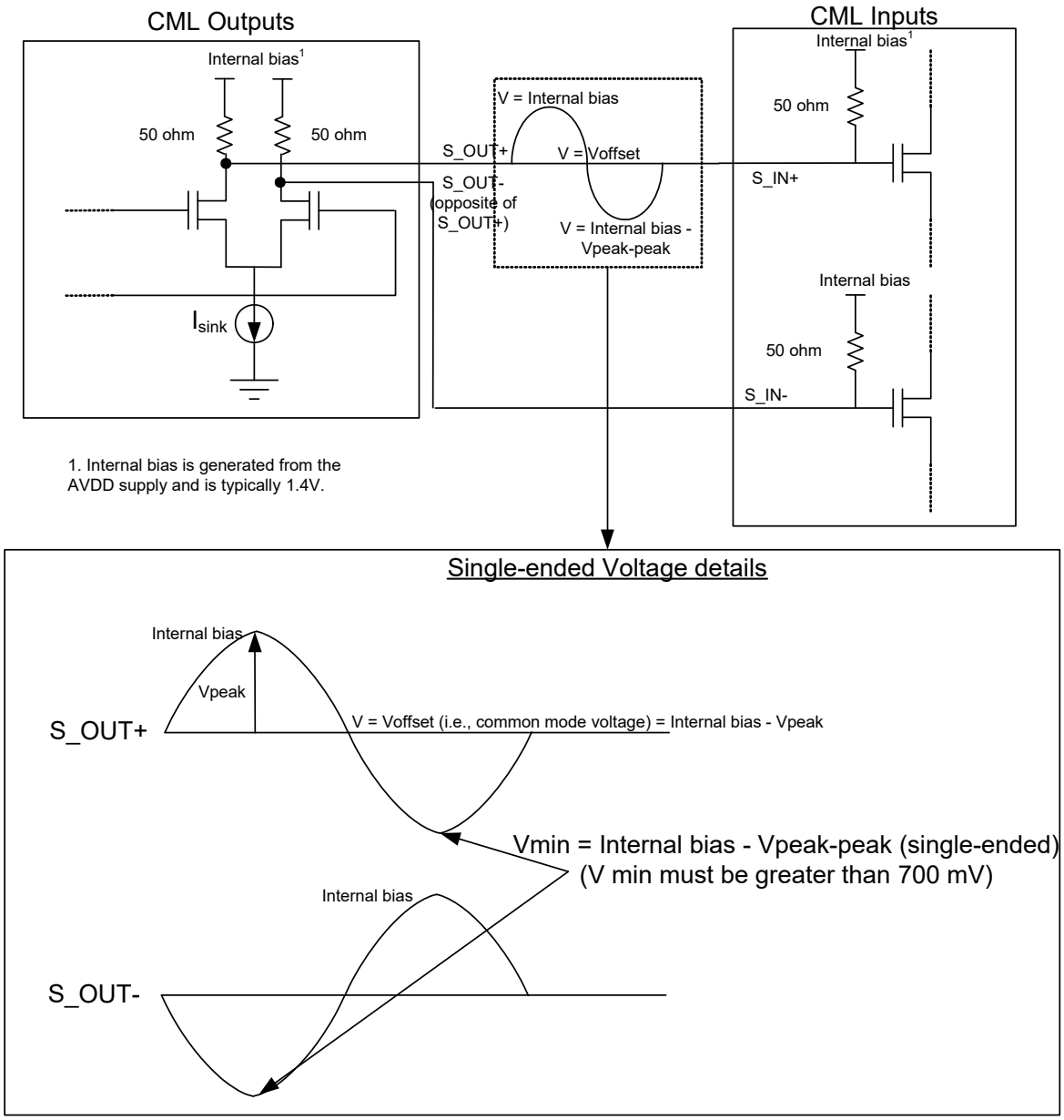


Figure 46: DC connection to a CML receiver



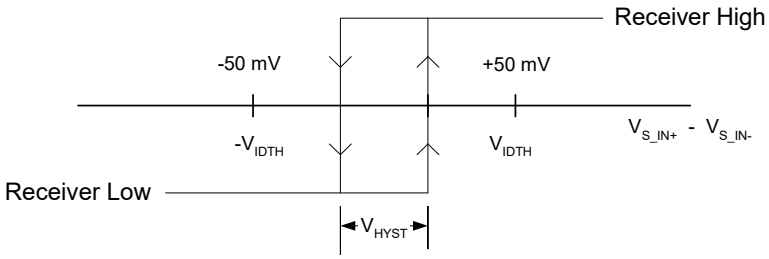
4.6.1.3 Receiver DC Characteristics

Table 135: Receiver DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
V_I	Input DC Voltage range S_IN+ or S_IN-	750		1650	mV
V_{IDTH}[1]	Input Differential Threshold |S_IN+ - S_IN-|, |SD+ - SD-|	50			mV (peak differential)
V_{HYST}[1]	Input Differential Hysteresis	25			mV
R_{IN}	Receiver 100 ohm Differential Input Impedance	80		120	ohm
	Receiver 150 ohm Differential Input Impedance	120		180	ohm

1. Receiver is at high level when V_{S_IN+} - V_{S_IN-} is greater than V_{IDTH}(min) and is at low level when V_{S_IN+} - V_{S_IN-} is less than -V_{IDTH}(min). A minimum hysteresis of V_{HYST} is present between -V_{IDTH} and +V_{IDTH} as shown in the figure. When the fiber link is down, an offset is applied to prevent false signal detect due to noise. When the fiber link is up, the offset circuit is disabled.

Figure 47: Input Differential Hysteresis



4.7 AC Timing Reference Values

Table 136: AC Timing Reference Values

Symbol	Parameter	Pins	Min	Typ	Max	Units
V_{IH_GMII} (Min.)	GMII input high voltage reference	TXD[7:0], TX_EN, TX_ER, GTX_CLK	1.9[1]			V
V_{IL_GMII} (Max.)	GMII input low voltage reference	TXD[7:0], TX_EN, TX_ER, GTX_CLK,			0.7	V
V_{OH_GMII} (Min.)	GMII output high voltage reference	RXD[7:0], RX_DV, RX_ER, RX_CLK, TX_CLK, CRS, COL	1.9			V
V_{OL_GMII} (Max.)	GMII output low voltage reference	RXD[7:0], RX_DV, RX_ER, RX_CLK, TX_CLK, CRS, COL			0.7	V
V_{IH_TBI} (Min.)	TBI input high voltage reference	TXD[9:0]	2.0			V
V_{IL_TBI} (Max.)	TBI input low voltage reference	TXD[9:0]			0.8	V
V_{I_TBI}	TBI input clock threshold	GTX_CLK		1.4		V
V_{OH_TBI} (Min.)	TBI output high voltage reference	RXD[9:0]	2.0			V
V_{OL_TBI} (Max.)	TBI output low voltage reference	RXD[9:0]			0.8	V
V_{O_TBI}	TBI output clock threshold	RCLK0, RCLK1		1.4		V

1. The VIH values in this AC table are not to be confused with the VIH values in the DC table. See IEEE Clause 35 GMII interface description for details.

4.8 AC Electrical Specifications

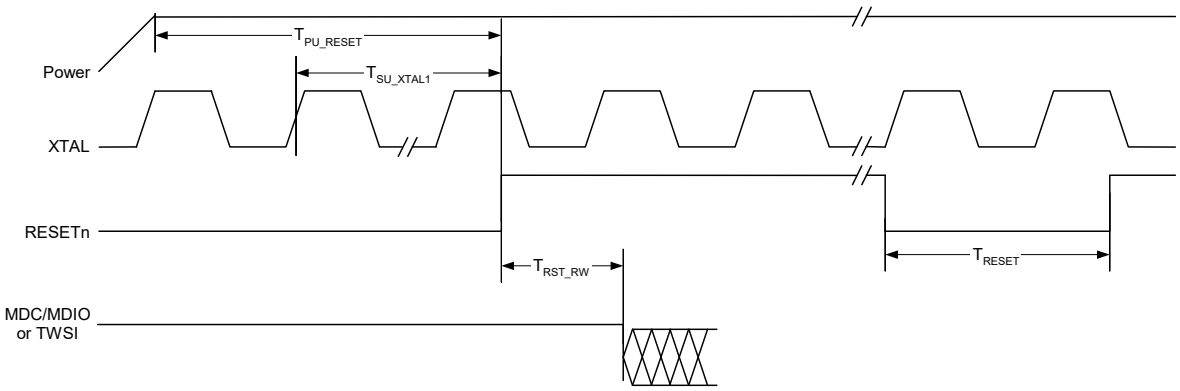
4.8.1 Reset Timing

Table 137: Reset Timing

(Over Full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{PU_RESET}	Valid power to RESETn de-asserted		10			ms
T_{SU_XTAL1}	Number of valid XTAL1 cycles prior to RESETn de-asserted		10			clks
T_{RESET}	Minimum reset pulse width during normal operation		10			ms
T_{RST_RW}	Delay after deasserting reset before register Read/ write available.		5			ms

Figure 48: Reset Timing



4.8.2 XTAL1 Input Clock Timing

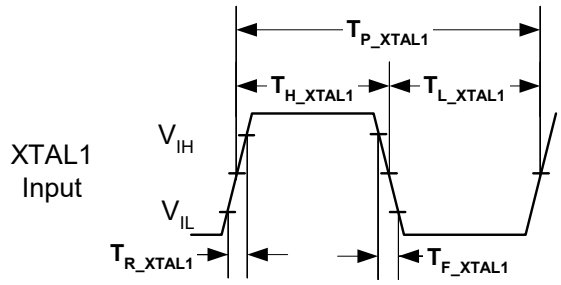
Table 138: XTAL1 Input Clock Timing[1]

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{P_XTAL1}	XTAL1 Period	25 MHz	40 -50 ppm	40	40 +50 ppm	ns
		125 MHz	8 -50 ppm	8	8 +50 ppm	ns
T_{H_XTAL1}	XTAL1 High time	25 MHz	14	20	26	ns
		125 MHz	2.8	4	5.2	ns
T_{L_XTAL1}	XTAL1 Low time	25 MHz	14	20	26	ns
		125 MHz	2.8	4	5.2	ns
T_{R_XTAL1}	XTAL1 Rise	V_{IL}(max) to V_{IH}(min) - 25 MHz	-	3.0	-	ns
		V_{IL}(max) to V_{IH}(min) - 125 MHz		0.6		ns
T_{F_XTAL1}	XTAL1 Fall	V_{IH}(min) to V_{IL}(max) - 25 MHz	-	3.0	-	ns
		V_{IH}(min) to V_{IL}(max) - 125 MHz		0.6		ns
T_{J_XTAL1}	XTAL1 total jitter[2]	25 MHz	-	-	200	ps[3]
		125 MHz			40	ps[3]

1. If the crystal option is used, ensure that the frequency is 25 MHz ± 50 ppm. Capacitors must be chosen carefully - see application note supplied by the crystal vendor.
2. PLL generated clocks are not recommended as input to XTAL1 since they can have excessive jitter. Zero delay buffers are also not recommended for the same reason.
3. 12 kHz to 20 MHz rms = 4 ps (GMII/RGMII to Copper), 3 ps (SGMII to Copper), 2 ps (1000BX to Copper, GMII/RGMII to 1000BX/SGMII).

Figure 49: XTAL1 Input Clock Timing



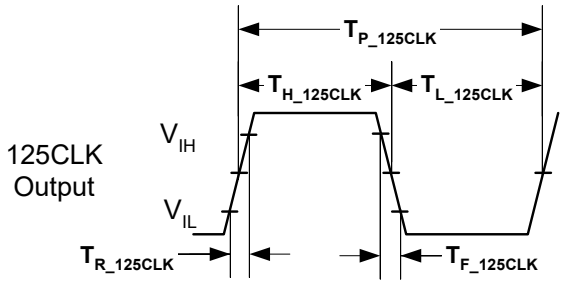
4.8.3 125CLK Output Timing

Table 139: 125CLK Output Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{P_125CLK}	125CLK Period		8 -50 ppm	8	8 +50 ppm	ns
T_{H_125CLK}	125CLK High time		3.5	4	4.4	ns
T_{L_125CLK}	125CLK Low time		3.5	4	4.4	ns
T_{R_125CLK}	125CLK Rise	V_{IL}(max) to V_{IH}(min)	-	1	-	ns
T_{F_125CLK}	125CLK Fall	V_{IH}(min) to V_{IL}(max)	-	1	-	ns
T_{J_125CLK}	125CLK Total Jitter		-	-	80	ps (peak-peak)
T_{P_CD}	125CLK power up to stable clock delay				38	µs

Figure 50: 125CLK Output Timing



4.9 GMII Interface Timing

4.9.1 GMII Transmit Timing

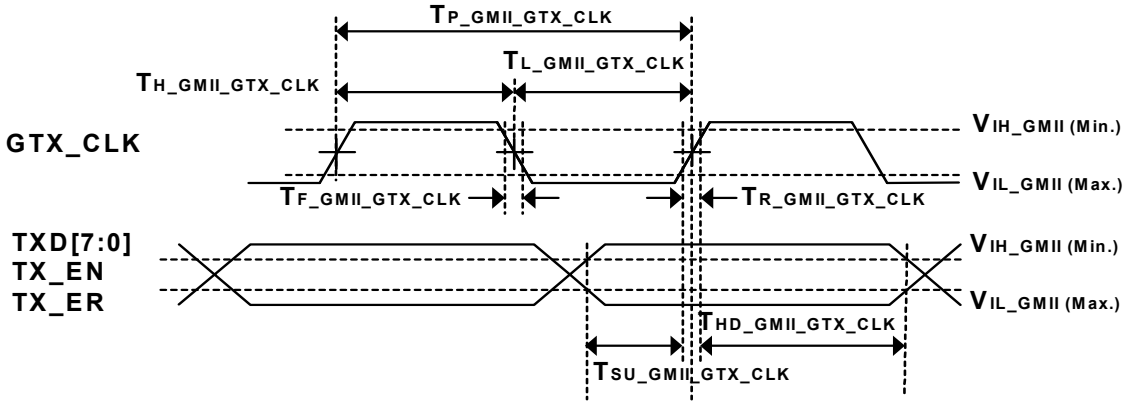
Table 140: GMII Transmit Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{SU\_GMII\_GTX\_CLK}$	GMII Setup Time		2.0			ns
$T_{HD\_GMII\_GTX\_CLK}$	GMII Hold Time		0			ns
$T_{H\_GMII\_GTX\_CLK}$	GTX_CLK High		2.5[1]			ns
$T_{L\_GMII\_GTX\_CLK}$	GTX_CLK Low		2.5[1]			ns
$T_{P\_GMII\_GTX\_CLK}$	GTX_CLK Period		7.5[1]	8.0	8.5	ns
$F_{GMII\_GTX\_CLK}$	GTX_CLK Frequency[2]		125[1] -100 ppm		125 +100 ppm	MHz
$T_{R\_GMII\_GTX\_CLK}$	GTX_CLK Rise Time				1.0	ns
$T_{F\_GMII\_GTX\_CLK}$	GTX_CLK Fall Time				1.0	ns

1. GTX_CLK toggle rate is “don’t care” if link is down, or if not in 1000BASE-T mode in any clock cycle period.
2. Long Term Average Frequency

Figure 51: GMII Transmit Timing



4.9.2 GMII Receive Timing

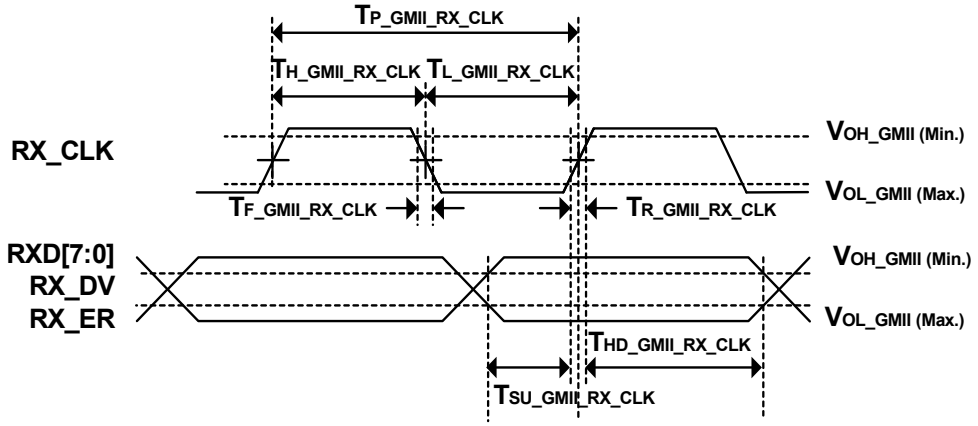
Table 141: GMII Receive Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{SU\_GMII\_RX\_CLK}$	GMII output to clock		2.5			ns
$T_{HD\_GMII\_RX\_CLK}$	GMII clock to output		0.5			ns
$T_{H\_GMII\_RX\_CLK}$	RX_CLK High		2.5[1]		5.5	ns
$T_{L\_GMII\_RX\_CLK}$	RX_CLK Low		2.5[1]		5.5	ns
$T_{P\_GMII\_RX\_CLK}$	RX_CLK Period		7.5[1]	8.0		ns
$T_{R\_GMII\_RX\_CLK}$	RX_CLK Rise Time				1.0	ns
$T_{F\_GMII\_RX\_CLK}$	RX_CLK Fall Time				1.0	ns
$T_{RSLEW\_GMII\_RX\_CLK}$	RX_CLK Rising Slew Rate		0.6[2]			V/ns
$T_{FSLEW\_GMII\_RX\_CLK}$	RX_CLK Falling Slew Rate		0.6[2]			V/ns

1. RX_CLK numbers not guaranteed during transition between 10/100/1000BASE-T operation.
2. Instantaneous change during internal VIH_GMII (Min.) and VIL_GMII (Max.)

Figure 52: GMII Receive Timing



4.10 MII Interface Timing

4.10.1 100 Mbps MII Transmit Timing

Table 142: 100 Mbps MII Transmit Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

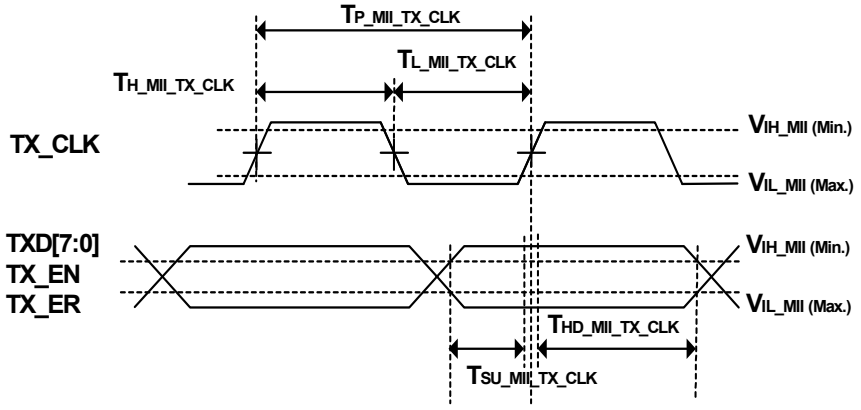
Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{SU\_MII\_TX\_CLK}$	MII Setup Time		10			ns
$T_{HD\_MII\_TX\_CLK}$	MII Hold Time		0			ns
$T_{H\_MII\_TX\_CLK}$	TX_CLK High		14		26	ns
$T_{L\_MII\_TX\_CLK}$	TX_CLK Low		14		26	ns
$T_{P\_MII\_TX\_CLK}$	TX_CLK Period			40		ns

4.10.2 10 Mbps MII Transmit Timing

Table 143: 10 Mbps MII Transmit Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{SU\_MII\_TX\_CLK}$	MII Setup Time		10			ns
$T_{HD\_MII\_TX\_CLK}$	MII Hold Time		0			ns
$T_{H\_MII\_TX\_CLK}$	TX_CLK High		140		260	ns
$T_{L\_MII\_TX\_CLK}$	TX_CLK Low		140		260	ns
$T_{P\_MII\_TX\_CLK}$	TX_CLK Period			400		ns

Figure 53: 10/100 Mbps Transmit Timing



4.10.3 100 Mbps MII Receive Timing

Table 144: 100 Mbps MII Receive Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{SU\_MII\_RX\_CLK}$	MII Output to Clock		12			ns
$T_{HD\_MII\_RX\_CLK}$	MII Clock to Output		12			ns
$T_{H\_MII\_RX\_CLK}$	RX_CLK High		14		26	ns
$T_{L\_MII\_RX\_CLK}$	RX_CLK Low		14		26	ns
$T_{P\_MII\_RX\_CLK}$	RX_CLK Period			40		ns

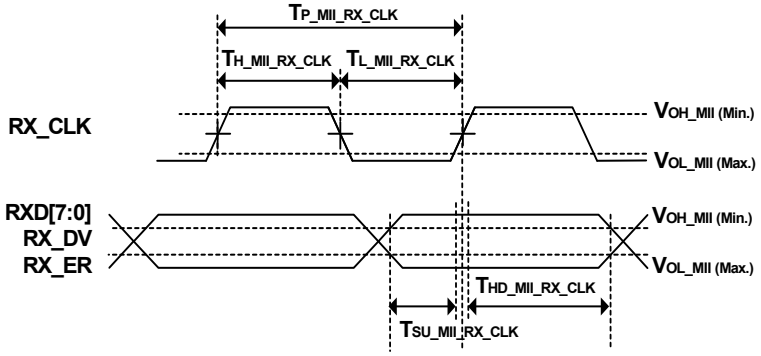
4.10.4 10 Mbps MII Receive Timing

Table 145: 10 Mbps MII Receive Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{SU\_MII\_RX\_CLK}$	MII Output to Clock		12			ns
$T_{HD\_MII\_RX\_CLK}$	MII Clock to Output		12			ns
$T_{H\_MII\_RX\_CLK}$	RX_CLK High		140		260	ns
$T_{L\_MII\_RX\_CLK}$	RX_CLK Low		140		260	ns
$T_{P\_MII\_RX\_CLK}$	RX_CLK Period			400		ns

Figure 54: 10/100 Mbps Receive Timing



4.11 TBI Interface Timing

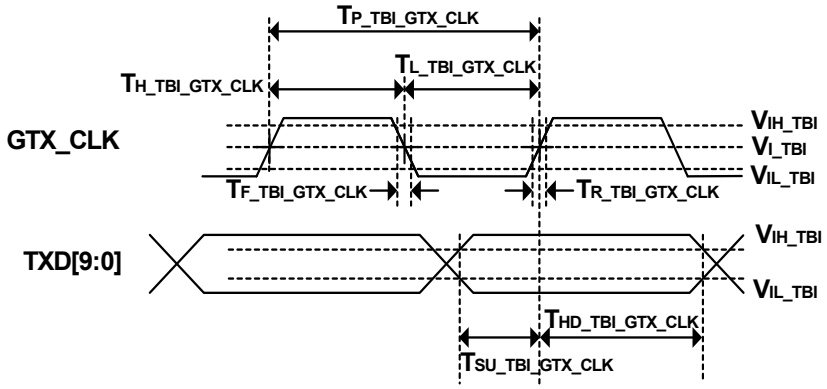
4.11.1 TBI Transmit Timing

Table 146: TBI Transmit Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{SU\_TBI\_GTX\_CLK}$	TBI Setup Time		2.0			ns
$T_{HD\_TBI\_GTX\_CLK}$	TBI Hold Time		1.0			ns
$T_{H\_TBI\_GTX\_CLK}$	GTX_CLK High		3.2		4.8	ns
$T_{L\_TBI\_GTX\_CLK}$	GTX_CLK Low		3.2		4.8	ns
$T_{P\_TBI\_GTX\_CLK}$	GTX_CLK Period		8.0 -100ppm	8.0	8.0 +100ppm	ns
$T_{R\_TBI\_GTX\_CLK}$	GTX_CLK Rise Time				2.4	ns
$T_{F\_TBI\_GTX\_CLK}$	GTX_CLK Fall Time				2.4	ns

Figure 55: TBI Transmit Timing



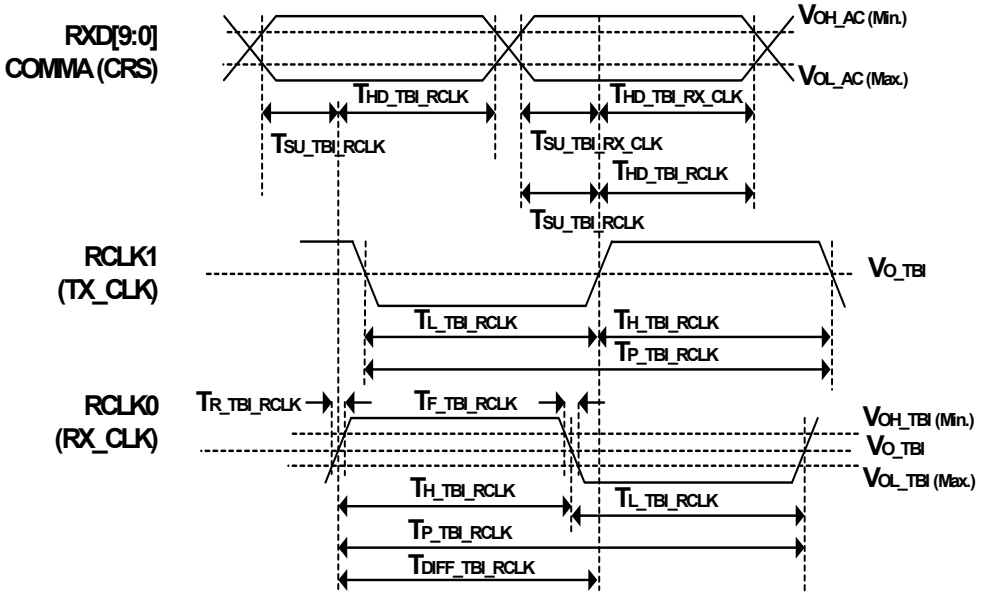
4.11.2 TBI Receive Timing

Table 147: TBI Receive Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{SU\_TBI\_RCLK}$	TBI Output to RCLK		2.5			ns
$T_{HD\_TBI\_RCLK}$	TBI RCLK to Output		1.5			ns
$T_{H\_TBI\_RCLK}$	RCLK High		7.0	8.0	9.0	ns
$T_{L\_TBI\_RCLK}$	RCLK Low		7.0	8.0	9.0	ns
$T_{P\_TBI\_RCLK}$	RCLK Period			16.0		ns
$T_{DIFF\_TBI\_RCLK}$	RCLK0/RCLK1 Offset		7.5	8.0	8.5	ns
$T_{R\_TBI\_RCLK}$	RCLK Rise Time				2.0	ns
$T_{F\_TBI\_RCLK}$	RCLK Fall Time				2.0	ns

Figure 56: TBI Receive Timing



4.12 RGMII/RTBI Interface Timing

4.12.1 RGMII AC Characteristics

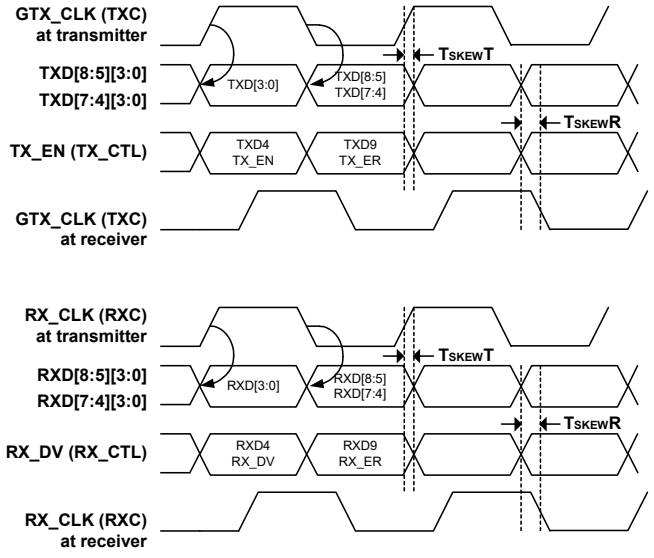
Table 148: RGMII AC Characteristics

(For other timing modes see Section 4.12.2 "RGMII/RTBI Delay Timing for different RGMII/RTBI Modes" on page 213.)

Symbol	Parameter	Min	Typ	Max	Units
TskewT	Data to Clock output Skew (at transmitter)	-500	0	500	ps
TskewR	Data to Clock input Skew (at receiver)	1.0	-	2.8	ns
T_{CYCLE}	Clock Cycle Duration	7.2	8.0	8.8	ns
$T_{CYCLE\_HIGH1000}$	High Time for 1000BASE-T [1]	3.6	4.0	4.4	ns
$T_{CYCLE\_HIGH100}$	High Time for 100BASE-T[1]	16	20	24	ns
T_{CYCLE_HIGH10}	High Time for 10BASE-T[1]	160	200	240	ns
T_{RISE}/T_{FALL}	Rise/Fall Time (20-80%)			0.75	ns

1. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three TCYCLE of the lowest speed transitioned between.

Figure 57: RGMII/RTBI Multiplexing and Timing



4.12.2 RGMII/RTBI Delay Timing for different RGMII/RTBI Modes

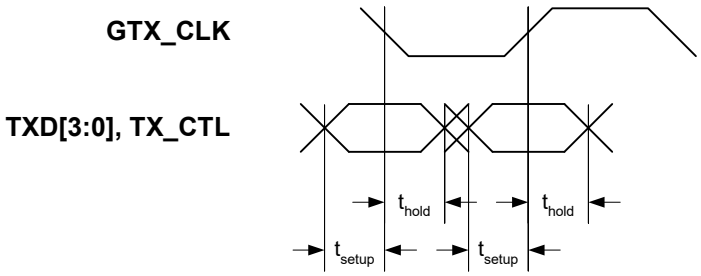
4.12.2.1 PHY Input - GTX_CLK Delay when Register 20.1 = 0

Table 149: PHY Input - GTX_CLK Delay when Register 20.1 = 0

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{setup}	Register 20.1 = 0	1.0			ns
t_{hold}		0.8			ns

Figure 58: GTX_CLK Delay Timing - Register 20.1 = 0



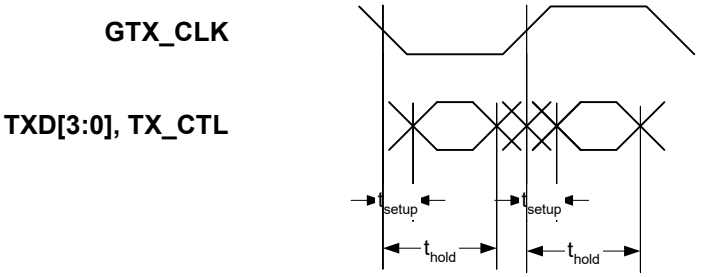
4.12.2.2 PHY Input - GTX_CLK Delay when Register 20.1 = 1

Table 150: PHY Input - GTX_CLK Delay when Register 20.1 = 1

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{setup}	Register 20.1 = 1 (add delay)	-0.9			ns
t_{hold}		2.7			ns

Figure 59: GTX_CLK Delay Timing - Register 20.1 = 1 (add delay)



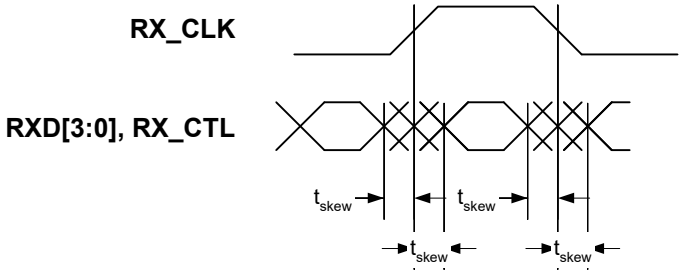
4.12.2.3 PHY Output - RX_CLK Delay

Table 151: PHY Output - RX_CLK Delay

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{skew}	Register 20.7 = 0	- 0.5		0.5	ns

Figure 60: RGMII RX_CLK Delay Timing - Register 20.7 = 0



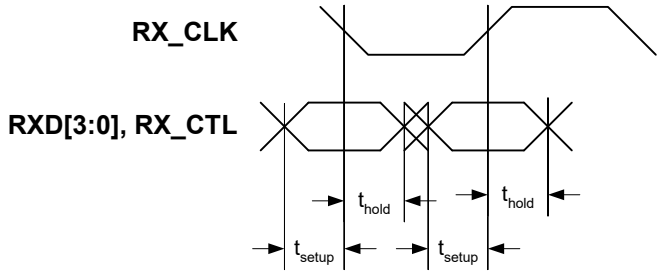
4.12.2.4 PHY Output - RX_CLK Delay

Table 152: PHY Output - RX_CLK Delay

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{setup}	Register 20.7 = 1 (add delay)	1.2			ns
t_{hold}		1.2			ns

Figure 61: RGMII RX_CLK Delay Timing - Register 20.7 = 1 (add delay)



4.13 Serial and SGMII Interface Timing

4.13.1 Serial Interface and SGMII Transmitter AC Characteristics

Table 153: Serial Interface and SGMII Transmitter AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
CLOCK	Clock signal duty cycle @ 625 MHz	48		52	%
T_{FALL}	VOD Fall time (20% - 80%)	100		200	ps
T_{RISE}	VOD Rise time (20% - 80%)	100		200	ps
T_{SKEW1}[1]	Skew between two members of a differential pair			20	ps
$T_{CLOCK2Q}$[2]	Clock to data relationship from either edges of the clock to valid data	250		550	ps

1. Skew measured at 50% of the transition.
2. Skew measured at 0V differential.

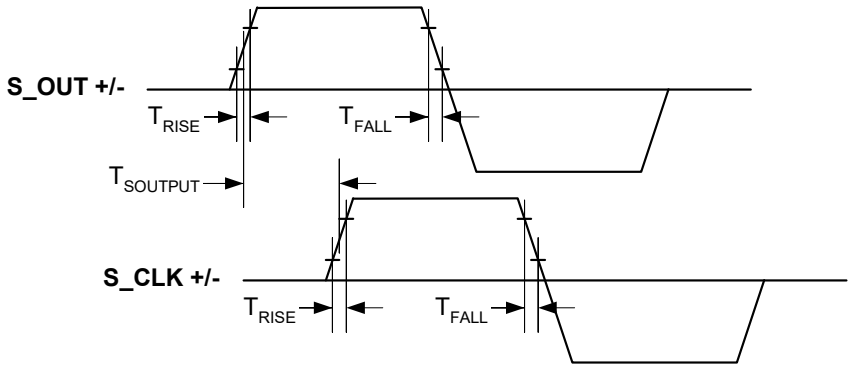
4.13.2 Serial Interface and SGMII Receiver AC Characteristics

Table 154: Serial Interface and SGMII Receiver AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
$T_{SOUTPUT}$[1]	SERDES output to S_CLK	360	400	440	ps

1. Measured at 50% of the transition.

Figure 62: Serial Interface Rise and Fall Times



4.14 Latency Timing

4.14.1 GMII to 1000BASE-T Transmit Latency Timing

Table 155: GMII to 1000BASE-T Transmit Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_TXEN\_CRS\_1000}$	1000BASE-T TX_EN Asserted to CRS Asserted				16	ns
$T_{AS\_TXEN\_COL\_1000}$	1000BASE-T TX_EN Asserted to COL Asserted				16	ns
$T_{AS\_TXEN\_MDI\_1000}$	1000BASE-T TX_EN Asserted to MDI SSD1		76[1]		84	ns
$T_{DA\_TXEN\_CRS\_1000}$	1000BASE-T TX_EN De-asserted to CRS De-asserted				16	ns
$T_{DA\_TXEN\_COL\_1000}$	1000BASE-T TX_EN De-asserted to COL De-asserted				16	ns
$T_{DA\_TXEN\_MDI\_1000}$	1000BASE-T TX_EN De-asserted to MDI CSReset, CSExtend, CSExtend_Err		76[1,2]		84	ns

1. Assumes register 16.15:14 is set to 00, which is the minimum latency. Each increase in setting adds 8 ns of latency.
2. Minimum and maximum values on end of packet assume zero frequency drift between the transmitted signal on MDI and GTX_CLK in GMII or TBI modes, or the received signal on S_IN± in serial interface mode. The worst case variation will be outside these limits, if there is a frequency difference.

4.14.2 MII to 100BASE-TX Transmit Latency Timing

Table 156: MII to 100BASE-TX Transmit Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_TXEN\_CRS\_100}$	100BASE-TX TX_EN Asserted to CRS Asserted				24	ns
$T_{AS\_TXEN\_COL\_100}$	100BASE-TX TX_EN Asserted to COL Asserted				24	ns
$T_{AS\_TXEN\_MDI\_100}$	100BASE-TX TX_EN Asserted to /J/		64		72	ns
$T_{DA\_TXEN\_CRS\_100}$	100BASE-TX TX_EN De-asserted to CRS De-asserted				24	ns
$T_{DA\_TXEN\_COL\_100}$	100BASE-TX TX_EN De-asserted to COL De-asserted				24	ns
$T_{DA\_TXEN\_MDI\_100}$	100BASE-TX TX_EN De-asserted to /T/		64		72	ns

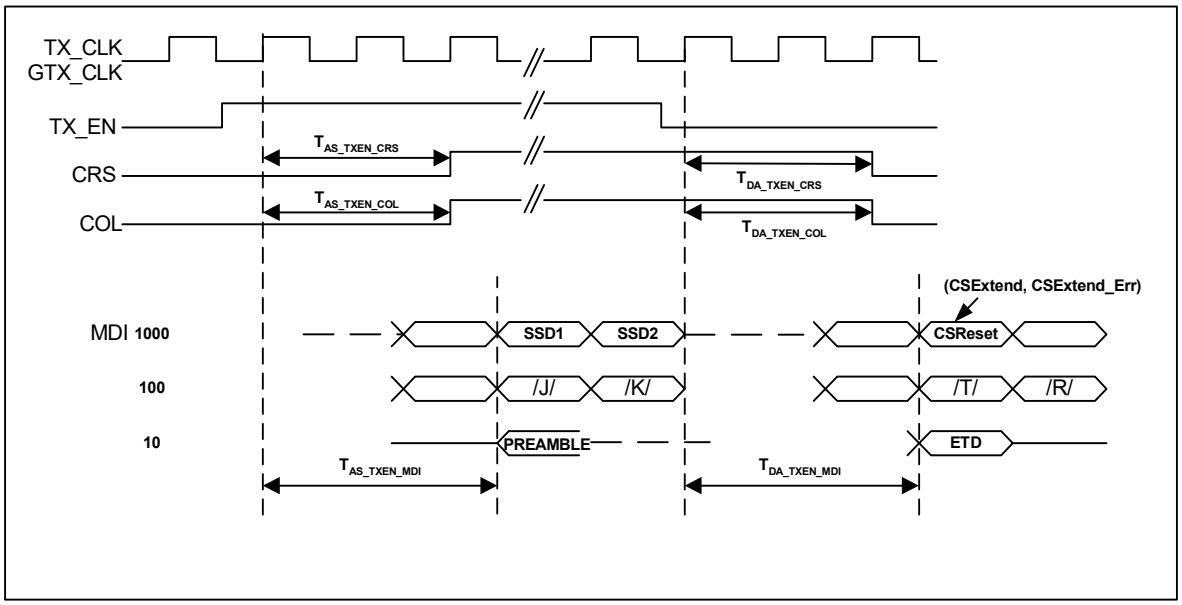
4.14.3 MII to 10BASE-T Transmit Latency Timing

Table 157: MII to 10BASE-T Transmit Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_TXEN\_CRS\_10}$	10BASE-T TX_EN Asserted to CRS Asserted				200	ns
$T_{AS\_TXEN\_COL\_10}$	10BASE-T TX_EN Asserted to COL Asserted				200	ns
$T_{AS\_TXEN\_MDI\_10}$	10BASE-T TX_EN Asserted to Preamble		200		300	ns
$T_{DA\_TXEN\_CRS\_10}$	10BASE-T TX_EN De-asserted to CRS De-asserted				200	ns
$T_{DA\_TXEN\_COL\_10}$	10BASE-T TX_EN De-asserted to COL De-asserted				200	ns
$T_{DA\_TXEN\_MDI\_10}$	10BASE-T TX_EN De-asserted to ETD		200		300	ns

Figure 63: GMII/MII to 10/100/1000BASE-T Transmit Latency Timing



4.14.4 1000BASE-T to GMII Receive Latency Timing

Table 158: 1000BASE-T to GMII Receive Latency Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_MDI\_CRS\_1000}$	1000BASE-T MDI start of Packet to CRS Asserted		156[1]		188	ns
$T_{AS\_MDI\_COL\_1000}$	1000BASE-T MDI start of Packet to COL Asserted		156[1]		188	ns
$T_{AS\_MDI\_RXDV\_1000}$	1000BASE-T MDI start of Packet to RX_DV Asserted		176[1]		208	ns
$T_{DA\_MDI\_CRS\_1000}$	1000BASE-T MDI CSReset to CRS De-asserted		172[1]		204	ns
$T_{DA\_MDI\_COL\_1000}$	1000BASE-T MDI CSReset to COL De-asserted		172[1]		204	ns
$T_{DA\_MDI\_RXDV\_1000}$	1000BASE-T MDI CSReset, CSExtend, CSExtend_Err to RX_DV De-asserted		176[1]		208	ns

1. In 1000BASE-T, the signals on the 4 MDI pairs arrive at different times because of the skew introduced by the cable. All timing on MDI±[3:0] is referenced from the latest arriving signal.

4.14.5 100BASE-TX to MII Receive Latency Timing

Table 159: 100BASE-TX to MII Receive Latency Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_MDI\_CRS\_100}$	100BASE-TX MDI start of Packet to CRS Asserted		152		184	ns
$T_{AS\_MDI\_COL\_100}$	100BASE-TX MDI start of Packet to COL Asserted		152		184	ns
$T_{AS\_MDI\_RXDV\_100}$	100BASE-TX MDI start of Packet to RX_DV Asserted		216		248	ns
$T_{DA\_MDI\_CRS\_100}$	100BASE-TX MDI /T/ to CRS De-asserted		192		224	ns
$T_{DA\_MDI\_COL\_100}$	100BASE-TX MDI /T/ to COL De-asserted		192		224	ns
$T_{DA\_MDI\_RXDV\_100}$	100BASE-TX MDI /T/ to RX_DV De-asserted		216		248	ns

4.14.6 10BASE-T to MII Receive Latency Timing

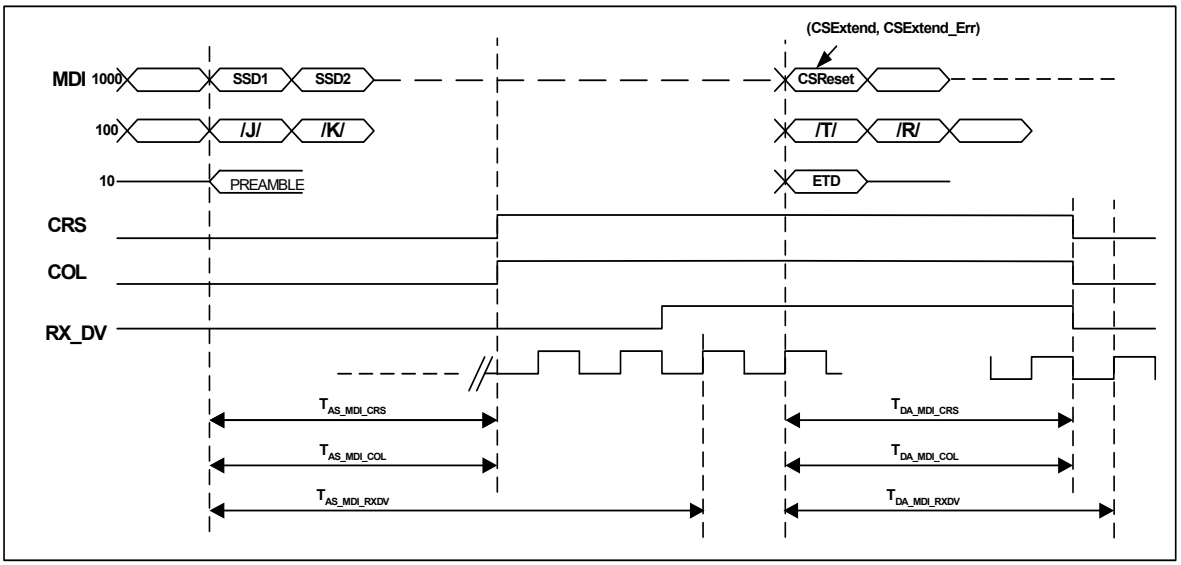
Table 160: 10BASE-T to MII Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_MDI\_CRS\_10}$	10BASE-T MDI start of Packet to CRS Asserted		800		1000	ns
$T_{AS\_MDI\_COL\_10}$	10BASE-T MDI start of Packet to COL Asserted		400		600	ns
$T_{AS\_MDI\_RXDV\_10}$	10BASE-T MDI start of Packet to RX_DV Asserted			1400[1]		ns
$T_{DA\_MDI\_CRS\_10}$	10BASE-T MDI ETD to CRS De-asserted			1300[1]		ns
$T_{DA\_MDI\_COL\_10}$	10BASE-T MDI ETD to COL De-asserted			1300[1]		ns
$T_{DA\_MDI\_RXDV\_10}$	10BASE-T MDI ETD to RX_DV De-asserted			1300[1]		ns

1. Actual values depend on number of bits in preamble and number of dribble bits, since nibbles on MII are aligned to start of frame delimiter and dribble bits are truncated.

Figure 64: 10/100/1000BASE-T to GMII/MII Receive Latency Timing



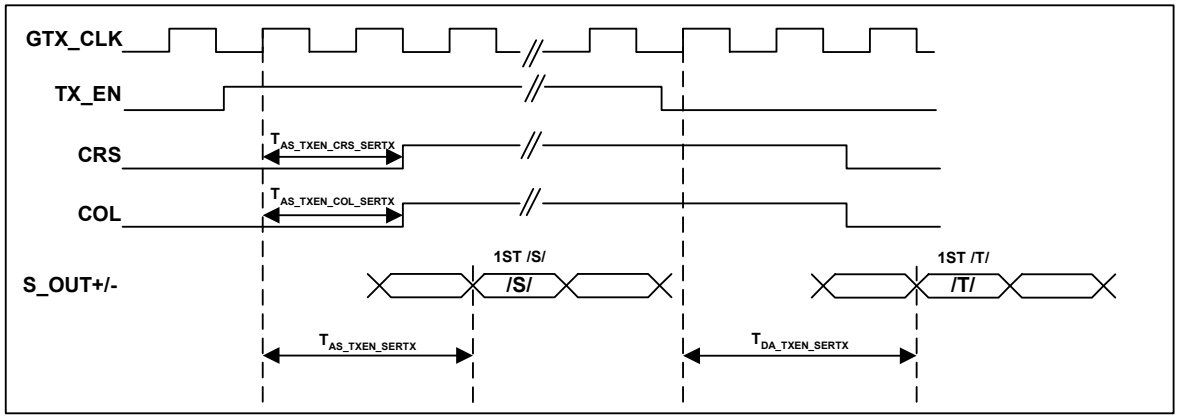
4.14.7 GMII to 1000BASE-X Transmit Latency Timing

Table 161: GMII to 1000BASE-X Transmit Latency Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_TX-EN\_CRS\_SERTX}$	1000BASE-T TX_EN Asserted to CRS Asserted				16	ns
$T_{AS\_TX-EN\_COL\_SERTX}$	1000BASE-T TX_EN Asserted to COL Asserted				16	ns
$T_{AS\_TX-EN\_SERTX}$	1000BASE-X TX_EN Asserted to S_OUT± Start of Packet /S/		90[1]		106	ns
$T_{DA\_TX-EN\_CRS\_SERTX}$	1000BASE-T TX_EN De-asserted to CRS De-asserted				16	ns
$T_{DA\_TX-EN\_COL\_SERTX}$	1000BASE-T TX_EN De-asserted to COL De-asserted				16	ns
$T_{DA\_TX-EN\_SERTX}$	1000BASE-X TX_EN De-asserted to S_OUT± /T/		90[1,2]		106	ns

1. Assumes Register 16.13:12 is set to 00, which is the minimum latency. Each increase in setting adds 8 ns of latency.
2. Minimum and maximum values on end of packet assume zero frequency drift between the transmitted signal on S_OUT± and GTX_CLK, which is based on XTAL1. The worst case variation will be outside these limits, if there is a frequency difference.

Figure 65: GMII to 1000BASE-X Transmit Latency Timing



4.14.8 1000BASE-X to GMII Receive Latency Timing

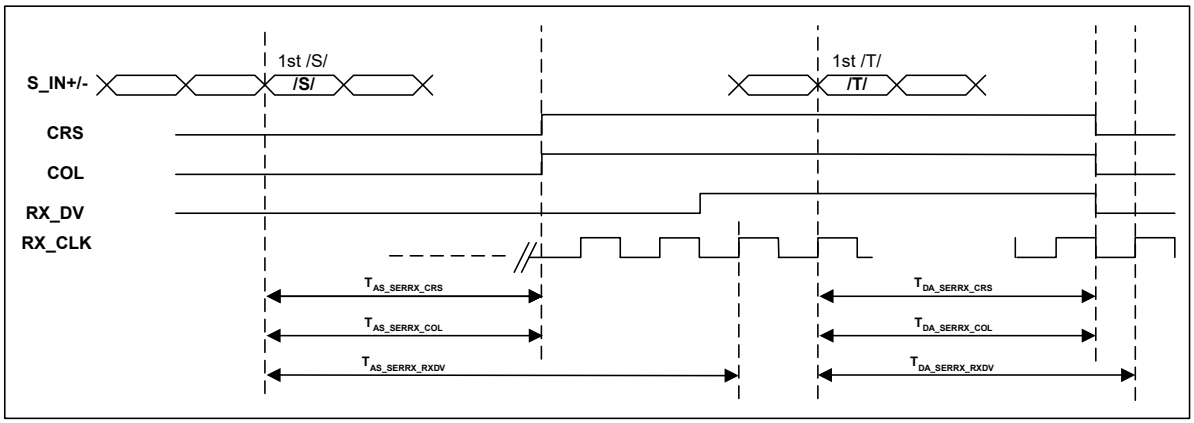
Table 162: 1000BASE-X to GMII Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_SERRX\_CRS}$	S_IN± Start of Packet /S/ to CRS Asserted		76		84	ns
$T_{AS\_SERRX\_COL}$	S_IN± Start of Packet /S/ to COL Asserted		84		92	ns
$T_{AS\_SERRX\_RXDV}$	S_IN ± Start of Packet /S/ to RX_DV Asserted		100[1]		108	ns
$T_{DA\_SERRX\_CRS}$	S_IN± /T/ to CRS De-asserted		100		108	ns
$T_{DA\_SERRX\_COL}$	S_IN± /T/ to COL De-asserted		84		92	ns
$T_{DA\_SERRX\_RXDV}$	S_IN± /T/ to RX_DV De-asserted		100[1,2]		108	ns

1. Assumes Register 16.15:14 is set to 00, which is the minimum latency. Each increase in setting adds 8 ns of latency.
2. Minimum and maximum values on end of packet assume zero frequency drift between the received signal on S_IN± and RX_CLK, which is derived from recovered clock of the fiber media. The worst case variation will be outside these limits, if there is a frequency difference.

Figure 66: 1000BASE-X to GMII Receive Latency Timing



4.14.9 RGMII to 1000BASE-T Transmit Latency Timing

Table 163: RGMII to 1000BASE-T Transmit Latency Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_TXC\_MDI\_1000}$	1000BASE-T TX_CTL Asserted to MDI SSD1		76[1]		84	ns
$T_{DA\_TXC\_MDI\_1000}$	1000BASE-T TX_CTL De-asserted to MDI CSReset, CSExtend, CSExtend_Err		76[1,2]		84	ns

1. Assumes Register 16.15:14 is set to 00, which is the minimum latency. Each increase in setting adds 8 ns of latency.
2. Minimum and maximum values on end of packet assume zero frequency drift between the transmitted signal on MDI and GTX_CLK. The worst case variation will be outside these limits, if there is a frequency difference.

4.14.10 RGMII to 100BASE-TX Transmit Latency Timing

Table 164: RGMII to 100BASE-TX Transmit Latency Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

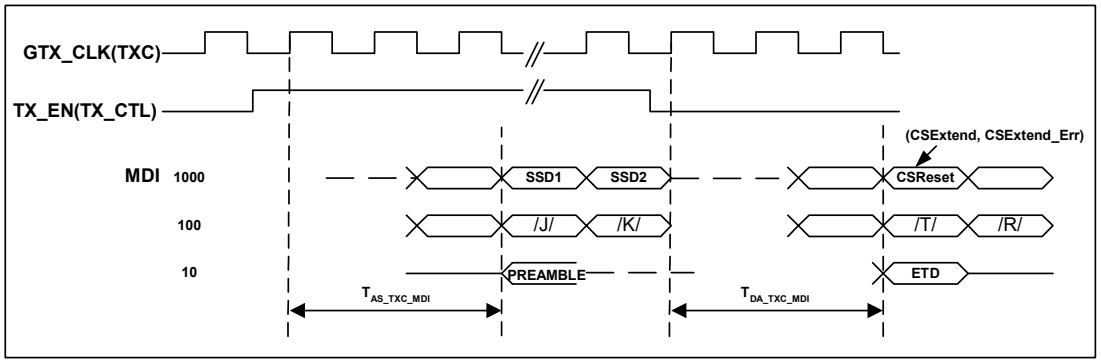
Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_TXC\_MDI\_100}$	100BASE-TX TX_CTL Asserted to /J/		84		92	ns
$T_{DA\_TXC\_MDI\_100}$	100BASE-TX TX_CTL De-asserted to /T/		84		92	ns

4.14.11 RGMII to 10BASE-T Transmit Latency Timing

Table 165: RGMII to 10BASE-T Transmit Latency Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_TXC\_MDI\_10}$	10BASE-T TX_CTL Asserted to Preamble		200		300	ns
$T_{DA\_TXC\_MDI\_10}$	10BASE-T TX_CTL De-asserted to ETD		200		300	ns

Figure 67: RGMII/MII to 10/100/1000BASE-T Transmit Latency Timing



4.14.12 1000BASE-T to RGMII Receive Latency Timing

Table 166: 1000BASE-T to RGMII Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_MDI\_RXC\_1000}$	1000BASE-T MDI start of Packet to RX_CTL Asserted		176[1]		208	ns
$T_{DA\_MDI\_RXC\_1000}$	1000BASE-T MDI CSReset, CSExtend, CSExtend_Err to RX_CTL De-asserted		176[1]		208	ns

4.14.13 100BASE-TX to RGMII Receive Latency Timing

Table 167: 100BASE-TX to RGMII Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_MDI\_RXC\_100}$	100BASE-TX MDI start of Packet to RX_CTL Asserted		200		232	ns
$T_{DA\_MDI\_RXC\_100}$	100BASE-TX MDI /T/ to RX_CTL De-asserted		200		232	ns

4.14.14 10BASE-T to RGMII Receive Latency Timing

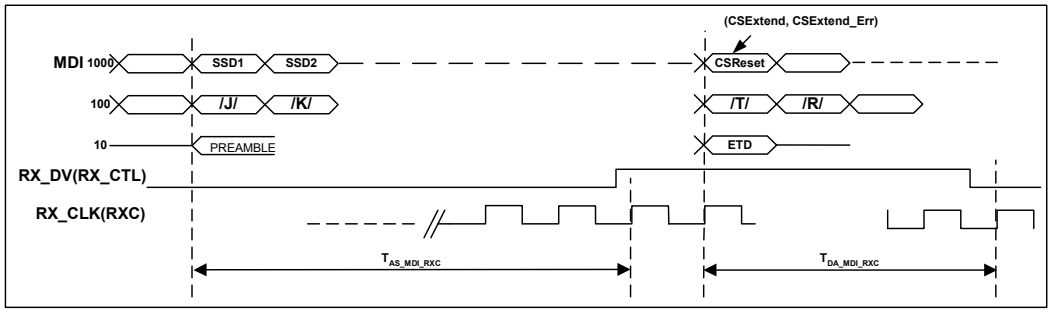
Table 168: 10BASE-T to RGMII Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_MDI\_RXC\_10}$	10BASE-T MDI start of Packet to RX_CTL Asserted			1400[1]		ns
$T_{DA\_MDI\_RXC\_10}$	10BASE-T MDI ETD to RX_CTL De-asserted			1400[1]		ns

1. Actual values depend on number of bits in preamble and number of dribble bits, since nibbles on MII are aligned to start of frame delimiter and dribble bits are truncated.

Figure 68: 10/100/1000BASE-T to RGMII Receive Latency Timing



4.14.15 RGMII to 1000BASE-X Transmit Latency Timing

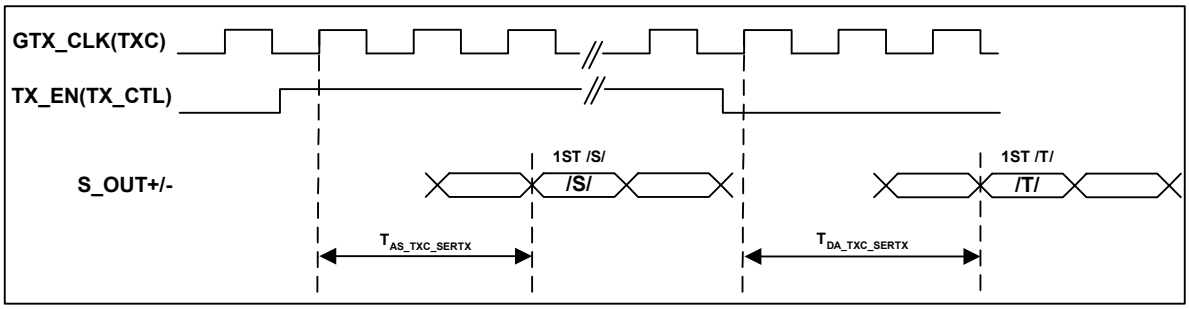
Table 169: RGMII to 1000BASE-X Transmit Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_TXC\_SERTX}$	1000BASE-X TX_CTL Asserted to S_OUT± Start of Packet /S/		90[1]		106	ns
$T_{DA\_TXC\_SERTX}$	1000BASE-X TX_CTL De-asserted to S_OUT± /T/		90[1,2]		106	ns

1. Assumes Register 16.13:12 is set to 00, which is the minimum latency. Each increase in setting adds 8 ns of latency.
2. Minimum and maximum values on end of packet assume zero frequency drift between the transmitted signal on S_OUT± and GTX_CLK, which is based on XTAL1. The worst case variation will be outside these limits, if there is a frequency difference.

Figure 69: RGMII to 1000BASE-X Transmit Latency Timing



4.14.16 1000BASE-X to RGMII Receive Latency Timing

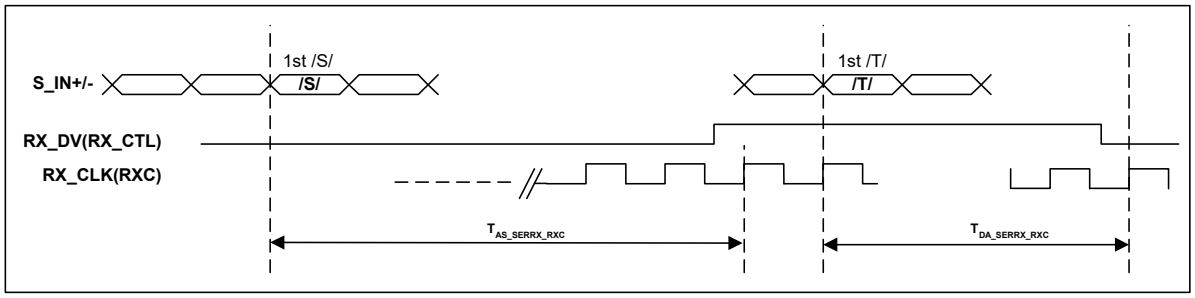
Table 170: 1000BASE-X to RGMII Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_SERRX\_RXC}$	S_IN± Start of Packet /S/ to RX_CTL Asserted		100[1]		108	ns
$T_{DA\_SERRX\_RXC}$	S_IN± /T/ to RX_CTL De-asserted		100[1,2]		108	ns

1. Assumes Register 16.15:14 is set to 00, which is the minimum latency. Each increase in setting adds 8 ns of latency.
2. Minimum and maximum values on end of packet assume zero frequency drift between the received signal on S_IN± and RX_CLK, which is derived from recovered clock of the fiber media. The worst case variation will be outside these limits, if there is a frequency difference.

Figure 70: 1000BASE-X to RGMII Receive Latency Timing



4.14.17 TBI to 1000BASE-T Transmit Latency Timing

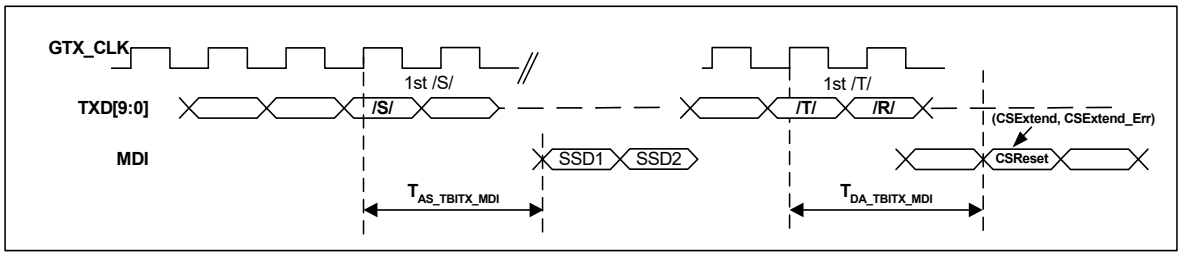
Table 171: TBI to 1000BASE-T Transmit Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_TBITX\_MDI}$	TBI Start of Packet to MDI SSD1		100[1]		108	ns
$T_{DA\_TBITX\_MDI}$	TBI /T/ to MDI CSReset, CSExtend, CSExtend_Err		100[1,2]		108	ns

1. Assumes register 16.15:14 is set to 00, which is the minimum latency. Each increase in setting adds 8 ns of latency.
2. Minimum and maximum values on end of packet assume zero frequency drift between the transmitted signal on MDI and GTX_CLK in GMII or TBI modes, or the received signal on S_IN± in serial interface mode. The worst case variation will be outside these limits, if there is a frequency difference.

Figure 71: TBI to 100BASE-T Transmit Latency Timing



4.14.18 1000BASE-T to TBI Receive Latency Timing

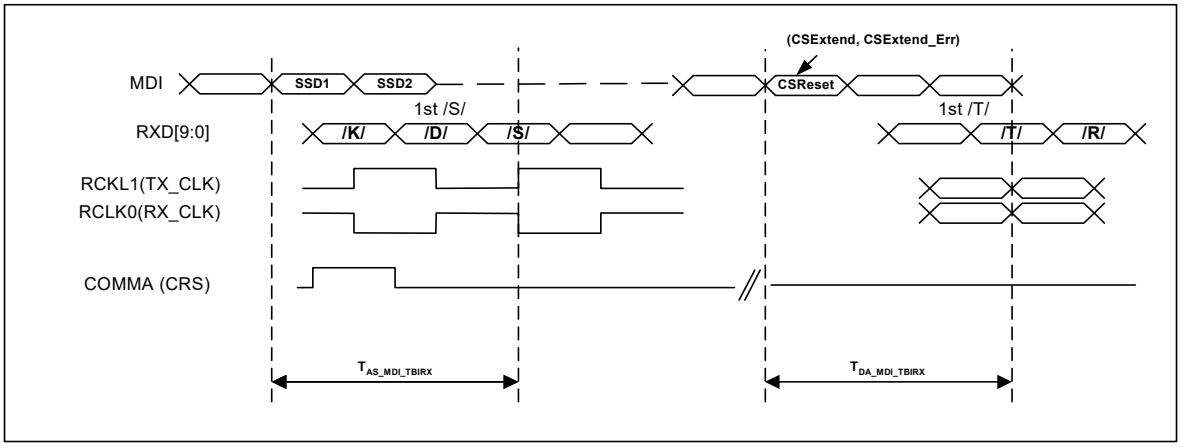
Table 172: 1000BASE-T to TBI Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_MDI\_TBIRX}$	MDI Start of Packet /S/ to TBI Start of Packet		228[1,2]		276	ns
$T_{DA\_MDI\_TBIRX}$	MDI CSReset, CSExtend, CSExtend_Err to TBI /T/		228[1,2,3]		276	ns

1. In 1000BASE-T, the signals on the 4 MDI pairs arrive at different times because of the skew introduced by the cable. All timing on MDI ±[3:0] is referenced from the latest arriving signal.
2. Assumes Register 16.15:14 is set to 00, which is the minimum latency. Each increase in setting adds 8 ns of latency.
3. Minimum and maximum values on end of packet assume zero frequency drift between the transmitted signal on MDI and the internally generated reference clock. The worst case variation will be outside these limits if there is a frequency difference.

Figure 72: 1000BASE-T to TBI Receive Latency Timing



4.14.19 RTBI to 1000BASE-T Transmit Latency Timing

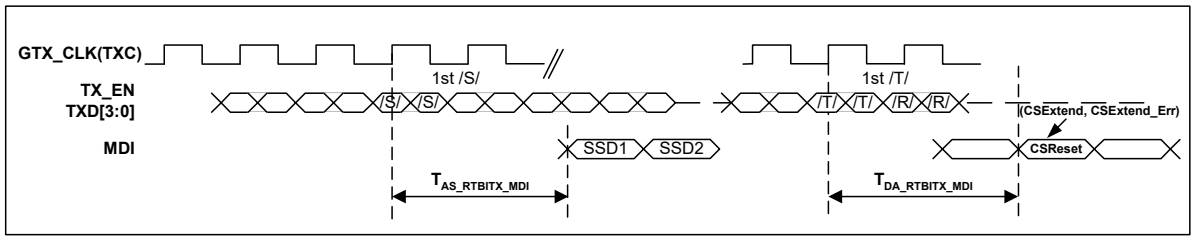
Table 173: RTBI to 1000BASE-T Transmit Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_RTBITX\_MDI}$	RTBI Start of Packet to MDI SSD1		100[1]		108	ns
$T_{DA\_RTBITX\_MDI}$	RTBI /T/ to MDI CSReset, CSExtend, CSExtend_Err		100[1,2]		108	ns

1. Assumes Register 16.15:14 is set to 00, which is the minimum latency. Each increase in setting adds 8 ns of latency.
2. Minimum and maximum values on end of packet assume zero frequency drift between the transmitted signal on MDI and GTX_CLK. The worst case variation will be outside these limits, if there is a frequency difference.

Figure 73: RTBI to 1000BASE-T Transmit Latency Timing



4.14.20 1000BASE-T to RTBI Receive Latency Timing

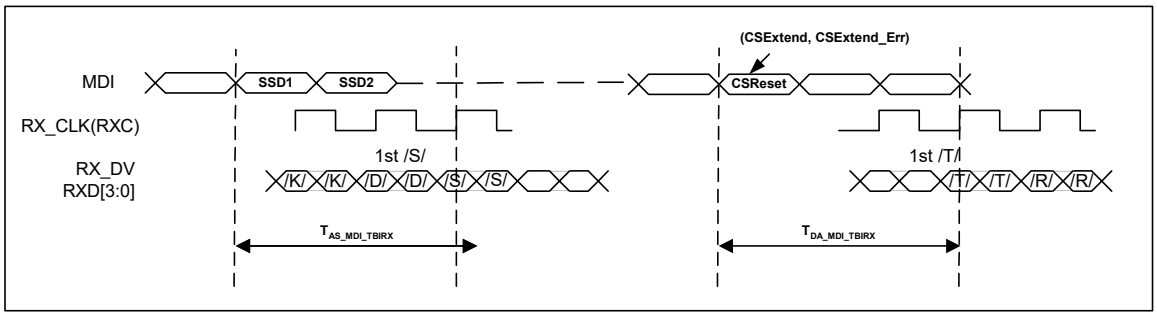
Table 174: 1000BASE-T to RTBI Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_MDI\_RTBIRX}$	MDI Start of Packet /S/ to RTBI Start of Packet		228[1,2]		276	ns
$T_{DA\_MDI\_RTBIRX}$	MDI CSReset, CSExtend, CSExtend_Err to RTBI /T/		228[1,2,3]		276	ns

1. In 1000BASE-T, the signals on the 4 MDI pairs arrive at different times because of the skew introduced by the cable. All timing on MDI ±[3:0] is referenced from the latest arriving signal.
2. Assumes Register 16.13:12 is set to 00, which is the minimum latency. Each increase in setting adds 8 ns of latency.
3. Minimum and maximum values on end of packet assume zero frequency drift between the received signal on MDI and RCLK1/ RCLK0, which are derived from XTAL1. The worst case variation will be outside these limits if there is a frequency difference.

Figure 74: 1000BASE-T to RTBI Receive Latency Timing



4.14.21 SGMII to 10/100/1000BASE-T Transmit Latency Timing

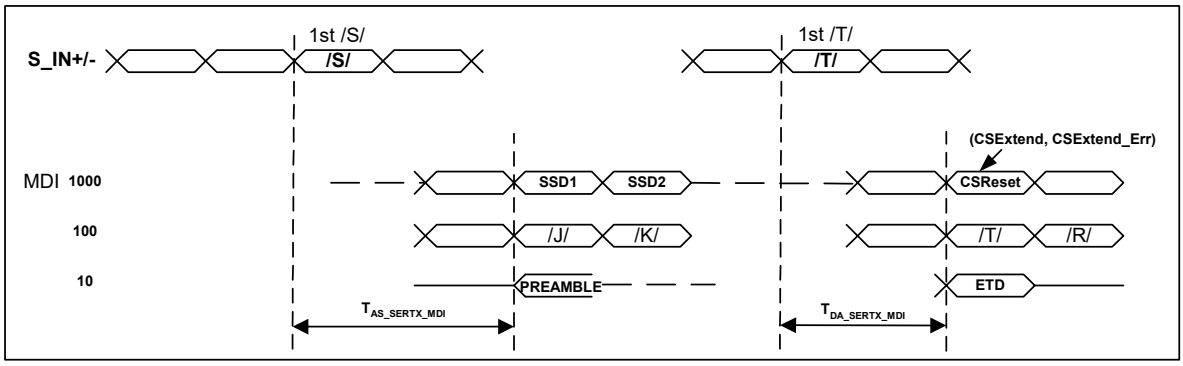
Table 175: SGMII to 10/100/1000BASE-T Transmit Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_SERTX\_MDI\_1000}$	S_IN± Start of Packet /S/ to MDI SSD1		124[1]		148	ns
$T_{DA\_SERTX\_MDI\_1000}$	S_IN± /T/ to MDI CSReset, CSExtend, CSExtend_Err		124[1,2]		148	ns
$T_{AS\_SERTX\_MDI\_100}$	S_IN± Start of Packet /S/ to MDI /J/		250[1]		310	ns
$T_{DA\_SERTX\_MDI\_100}$	S_IN± /T/ to MDI /T/		250[1,2]		310	ns
$T_{AS\_SERTX\_MDI\_10}$	S_IN± Start of Packet /S/ to MDI Preamble		1200[1]		2000	ns
$T_{DA\_SERTX\_MDI\_10}$	S_IN± /T/ to MDI ETD		1200[1,2]		2000	ns

1. Assumes Register 16.15:14 is set to 00, which is the minimum latency. Each increase in setting adds 8 ns of latency in 1000 Mbps, 40 ns in 100 Mbps, and 400 ns in 10 Mbps.
2. Minimum and maximum values on end of packet assume zero frequency drift between the transmitted signal on MDI and the received signal on S_IN±. The worst case variation will be outside these limits, if there is a frequency difference.

Figure 75: SGMII to 10/100/1000BASE-T Transmit Latency Timing



4.14.22 10/100/1000BASE-T to SGMII Receive Latency Timing

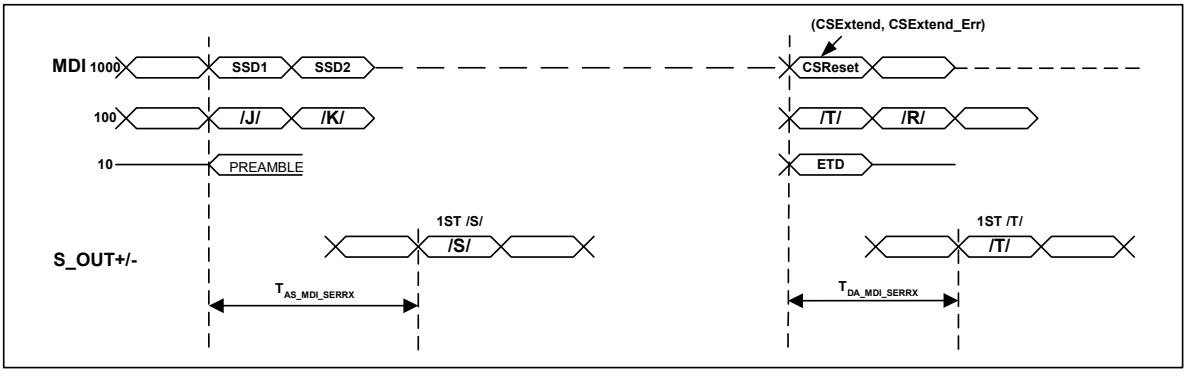
Table 176: 10/100/1000BASE-T to SGMII Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_MDI\_SERRX\_1000}$	MDI SSD1 to S_OUT± Start of Packet		248[1,2]		296	ns
$T_{DA\_MDI\_SERRX\_1000}$	MDI CSReset, CSExtend, CSExtend_Err to S_OUT± /T/		248[1,2,3]		296	ns
$T_{AS\_MDI\_SERRX\_100}$	MDI /J/ to S_OUT± Start of Packet		370[2]		434	ns
$T_{DA\_MDI\_SERRX\_100}$	MDI /T/ to S_OUT±/T/		370[2,3]		434	ns
$T_{AS\_MDI\_SERRX\_10}$	MDI Preamble to S_OUT± Start of Packet			2700[2,4]		ns
$T_{DA\_MDI\_SERRX\_10}$	MDI ETD to S_OUT± /T/			2700[2,3,4]		ns

1. In 1000BASE-T the signals on the 4 MDI pairs arrive at different times because of the skew introduced by the cable. All timing on MDI±[3:0] is referenced from the latest arriving signal.
2. Assumes Register 16.13:12 is set to 00, which is the minimum latency. Each increase in setting adds 8 ns of latency 1000 Mbps, 40 ns in 100 Mbps, and 400 ns in 10 Mbps.
3. Minimum and maximum values on end of packet assume zero frequency drift between the received signal on MDI and S_OUT±, which is based on XTAL1. The worst case variation will be outside these limits if there is a frequency difference.
4. Actual values depend on number of bits in preamble and number of dribble bits, since nibbles on MII are aligned to start of frame delimiter and dribble bits are truncated.

Figure 76: 10/100/1000BASE-T to SGMII Receive Latency Timing



4.14.23 1000BASE-X to 1000BASE-T Transmit Latency Timing

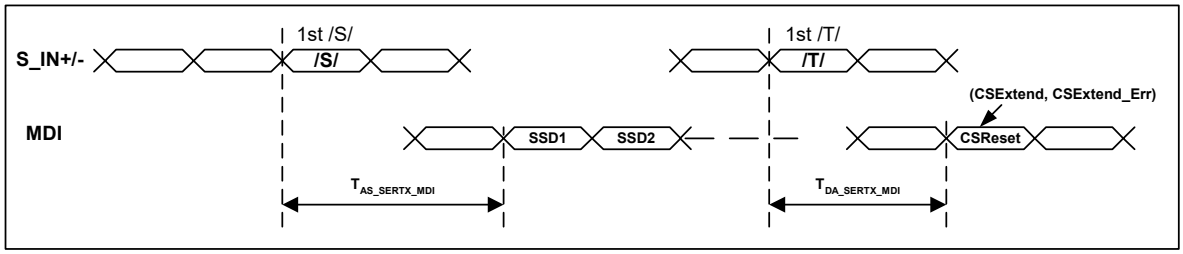
Table 177: 1000BASE-X to 1000BASE-T Transmit Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_SERTX\_MDI\_1000}$	S_IN ± Start of Packet /S/ to MDI SSD1		124[1]		148	ns
$T_{DA\_SERTX\_MDI\_1000}$	S_IN ± /T/ to MDI CSReset, CSExtend, CSExtend_Err		124[1,2]		148	ns

1. Assumes Register 16.15:14 is set to 00, which is the minimum latency. Each increase in setting adds 8 ns of latency.
2. Minimum and maximum values on end of packet assume zero frequency drift between the transmitted signal on MDI and the received signal on S_IN±. The worst case variation will be outside these limits, if there is a frequency difference.

Figure 77: 1000BASE-X to 1000BASE-T Transmit Latency Timing



4.14.24 1000BASE-T to 1000BASE-X Receive Latency Timing

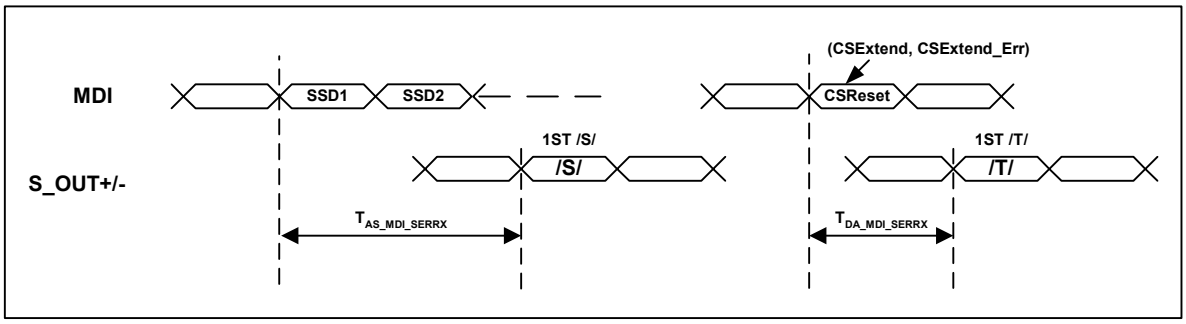
Table 178: 1000BASE-T to 1000BASE-X Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_MDI\_SERRX\_1000}$	MDI SSD1 to S_OUT ± Start of Packet		248[1,2]		296	ns
$T_{DA\_MDI\_SERRX\_1000}$	MDI CSReset, CSExtend, CSExtend_Err to S_OUT ± /T/		248[1,2,3]		296	ns

1. In 1000BASE-T the signals on the 4 MDI pairs arrive at different times because of the skew introduced by the cable. All timing on MDI±[3:0] is referenced from the latest arriving signal.
2. Assumes Register 16.13:12 is set to 00, which is the minimum latency. Each increase in setting adds 8 ns of latency.
3. Minimum and maximum values on end of packet assume zero frequency drift between the received signal on MDI and S_OUT±, which is based on XTAL1. The worst case variation will be outside these limits if there is a frequency difference.

Figure 78: 1000BASE-T to 1000BASE-X Receive Latency Timing



4.15 Serial Management Interface, Two-Wire Serial Interface, and JTAG Timing

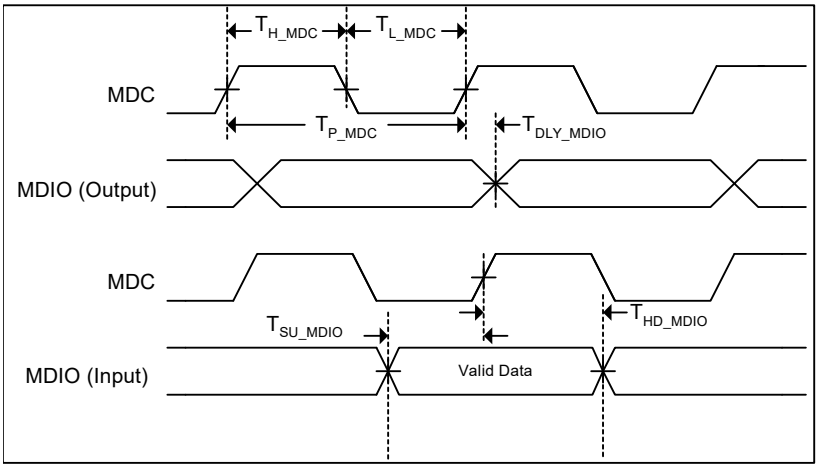
4.15.1 Serial Management Interface Timing

Table 179: Serial Management Interface Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{DLY_MDIO}	MDC to MDIO (Output) Delay Time		0		20	ns
T_{SU_MDIO}	MDIO (Input) to MDC Setup Time		10			ns
T_{HD_MDIO}	MDIO (Input) to MDC Hold Time		10			ns
T_{P_MDC}	MDC Period		120			ns
T_{H_MDC}	MDC High		30			ns
T_{L_MDC}	MDC Low		30			ns

Figure 79: Serial Management Interface Timing



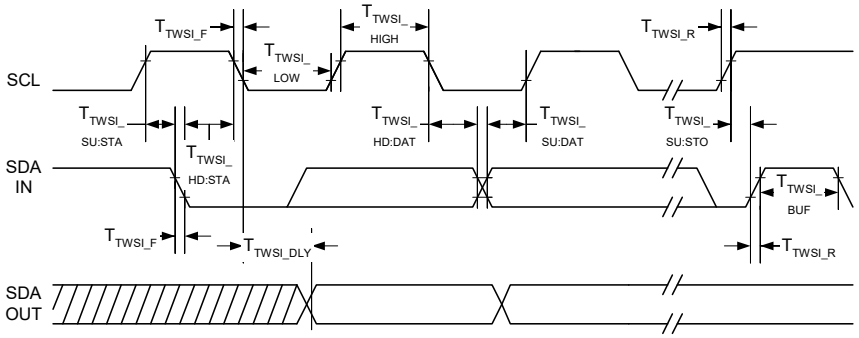
4.15.2 Two-Wire Serial Interface (TWSI) Timing

Table 180: Two-Wire Serial Interface (TWSI) Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
FTWSI_SCL	SCL Clock Frequency	100 kHz			100	kHz
		400 kHz			400	
TTWSI_R	SDA Rise time	100 kHz			1000	ns
		400 kHz			300	
TTWSI_F	SDA Fall Time	100 kHz			300	ns
		400 kHz			300	
TTWSI_HIGH	Clock High Period	100 kHz	4000			ns
		400 kHz	600			
TTWSI_LOW	Clock Low Period	100 kHz	4700			ns
		400 kHz	1300			
TTWSI_SU:STA	Start Condition Setup Time (for a Repeated Start Condition)	100 kHz	4700			ns
		400 kHz	600			
TTWSI_HD:STA	Start Condition Hold Time	100 kHz	4000			ns
		400 kHz	600			
TTWSI_SU:STO	Stop Condition Setup Time	100 kHz	4000			ns
		400 kHz	600			
TTWSI_SU:DAT	Data in Setup Time	100 kHz	250			ns
		400 kHz	100			
TTWSI_HD:DAT	Data in Hold Time	100 kHz	300			ns
		400 kHz	300			
TTWSI_BUF	Bus Free Time	100 kHz	4700			ns
		400 kHz	1300			
TTWSI_DLY	SCL Low to SDA Data Out Valid	100 kHz	40		200	ns
		400 kHz	40		200	

Figure 80: Two-Wire Serial Interface Timing

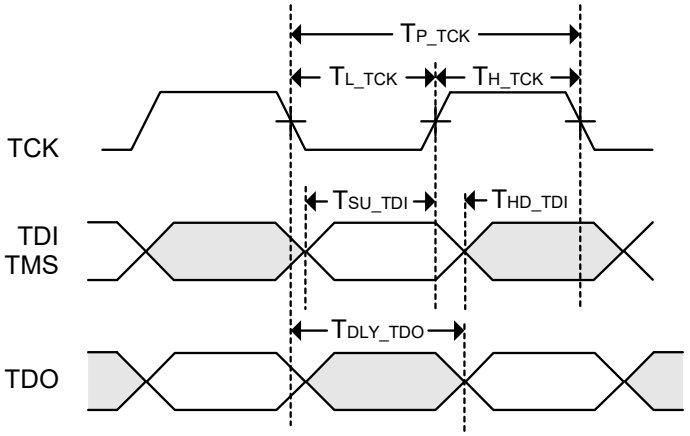


4.15.3 JTAG Timing

Table 181: JTAG Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{P_TCK}	TCK Period		40			ns
T_{H_TCK}	TCK High		12			ns
T_{L_TCK}	TCK Low		12			ns
T_{SU_TDI}	TDI, TMS to TCK Setup Time		10			ns
T_{HD_TDI}	TDI, TMS to TCK Hold Time		10			ns
T_{DLY_TDO}	TCK to TDO Delay		0		15	ns

Figure 81: JTAG Timing



4.16 IEEE AC Transceiver Parameters

Table 182: IEEE AC Transceiver Parameters

IEEE tests are typically based on templates and cannot simply be specified by number. For an exact description of the templates and the test conditions, refer to the IEEE specifications:
-10BASE-T IEEE 802.3 Clause 14-2000
-100BASE-TX ANSI X3.263-1995
-1000BASE-T IEEE 802.3ab Clause 40 Section 40.6.1.2 Figure 40-26 shows the template waveforms for transmitter electrical specifications.

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

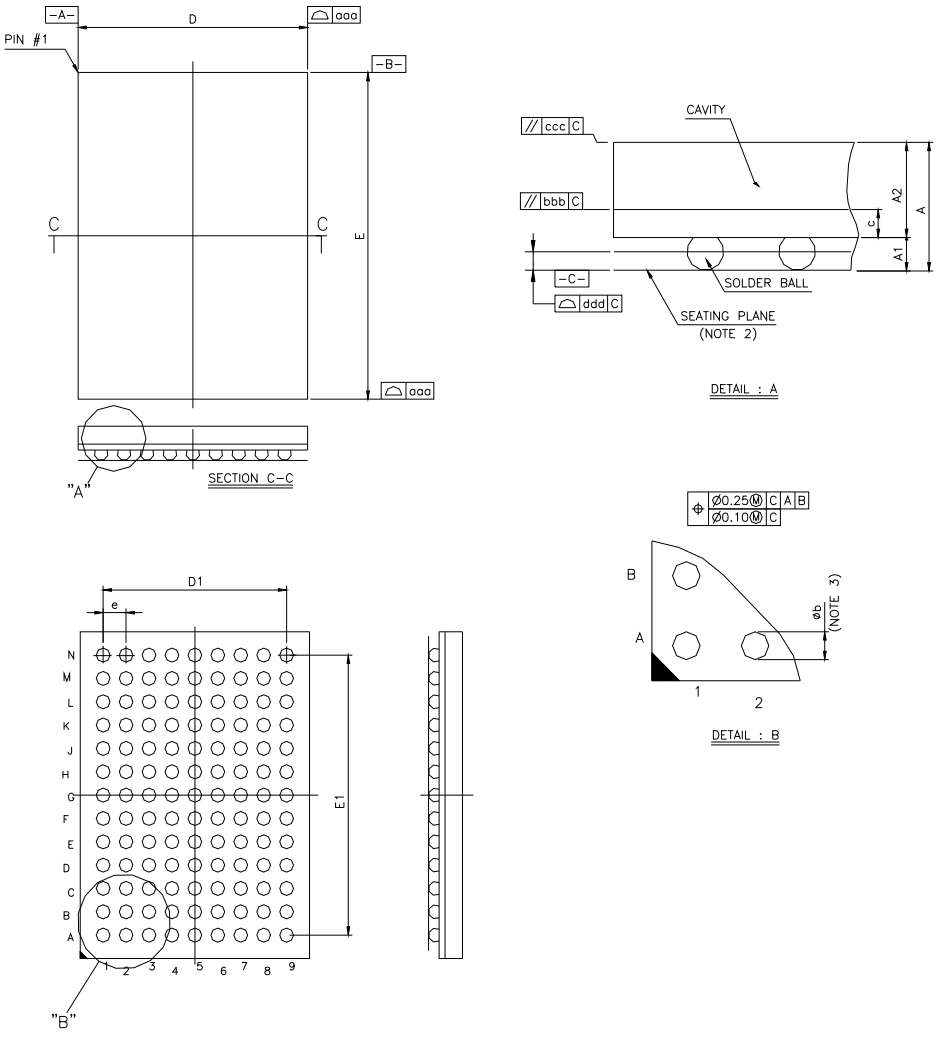
Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
T_{RISE}	Rise time	MDI[1:0]	100BASE-TX	3.0	4.0	5.0	ns
T_{FALL}	Fall Time	MDI[1:0]	100BASE-TX	3.0	4.0	5.0	ns
T_{RISE}/ T_{FALL} Symmetry		MDI[1:0]	100BASE-TX	0		0.5	ns
DCD	Duty Cycle Distortion	MDI[1:0]	100BASE-TX	0		0.5[1]	ns, peak-peak
Transmit Jitter		MDI[1:0]	100BASE-TX	0		1.4	ns, peak-peak

1. ANSI X3.263-1995 Figure 9-3

5 Package Mechanical Dimensions

5.1 117-pin TFBGA Package

Figure 82: 117-pin TFBGA Package Mechanical Drawings



(All dimensions in mm.)

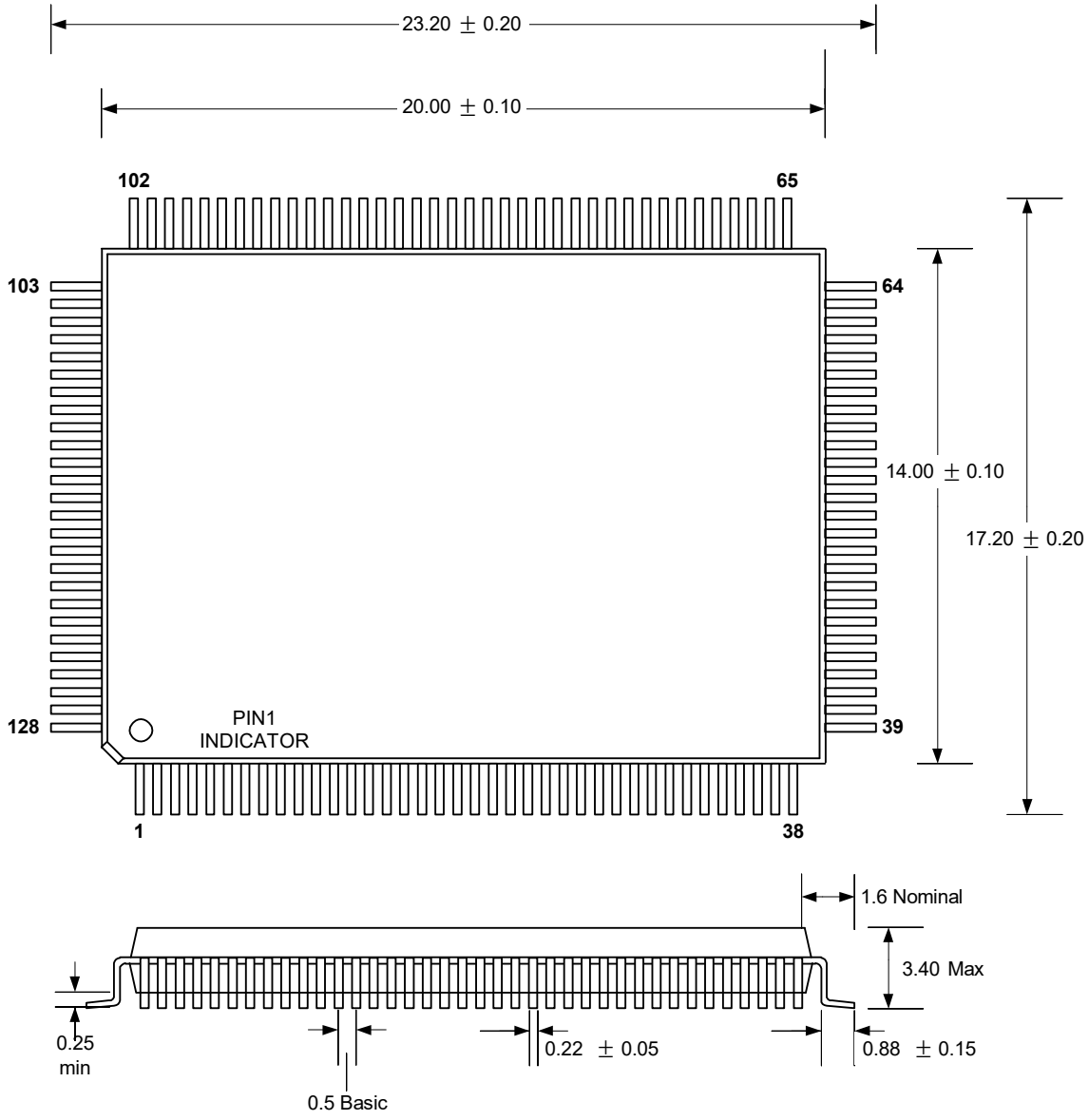
Table 183: 117-Pin TFBGA Package Dimensions

Dimensions in mm			
Symbol	**MIN**	**NOM**	**MAX**
A	--	--	1.54
A1	0.40	0.50	0.60
A2	0.84	0.89	0.94
c	0.32	0.36	0.40
D	9.90	10.00	10.10
E	13.90	14.00	14.10
D1	--	8.00	--
E1	--	12.00	--
e	--	1.00	--
b	0.50	0.60	0.70
aaa	0.20		
bbb	0.25		
ccc	0.35		
ddd	0.15		
MD/ME			

NOTE:
1. CONTROLLING DIMENSION: MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.

5.2 128-Pin PQFP Package

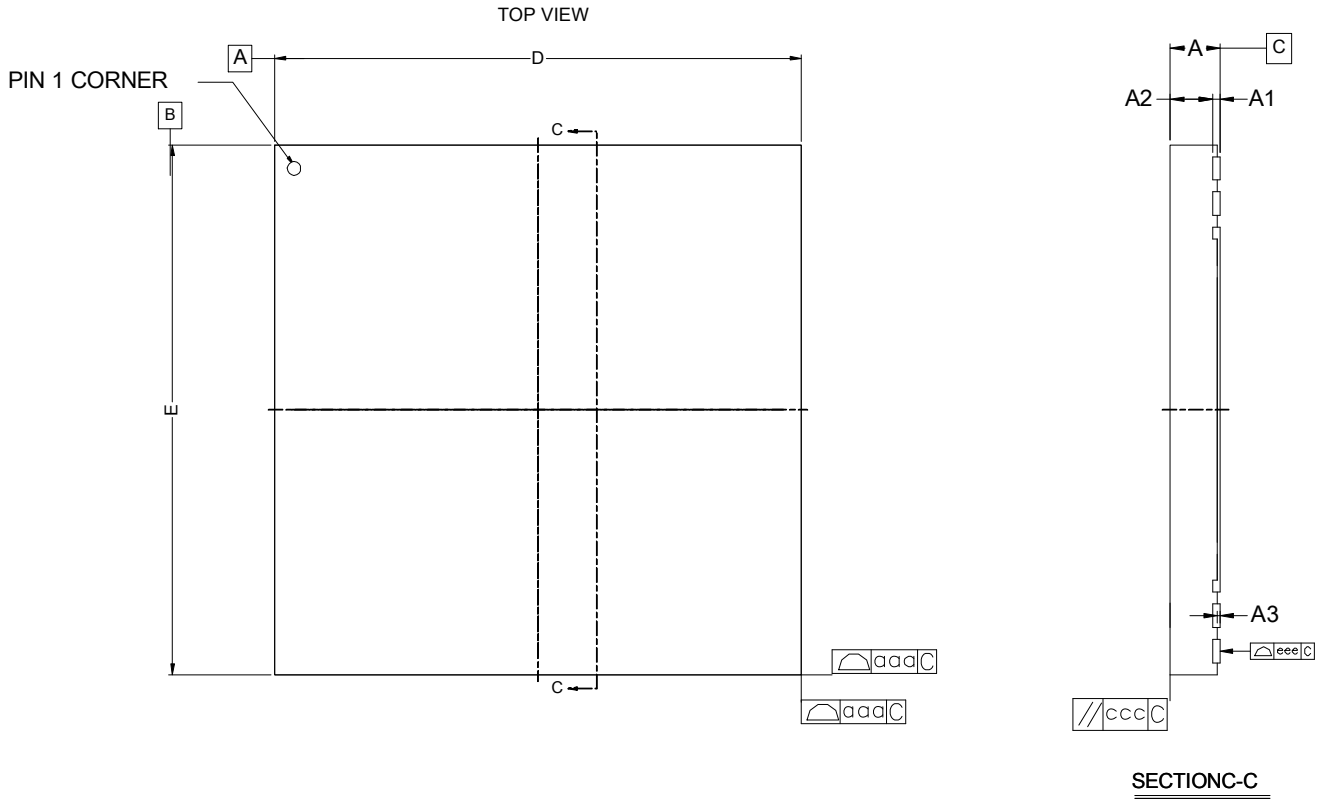
Figure 83: 128-pin PQFP Package Mechanical Drawings



5.3 96-pin aQFN Package

5.3.1 96-pin aQFN Package - Top View

Figure 84: 96-pin aQFN Package Mechanical Drawings - Top View



5.3.2 96-Pin aQFN Package - Bottom View

Figure 85: 96-pin aQFN Package Mechanical Drawings - Bottom View

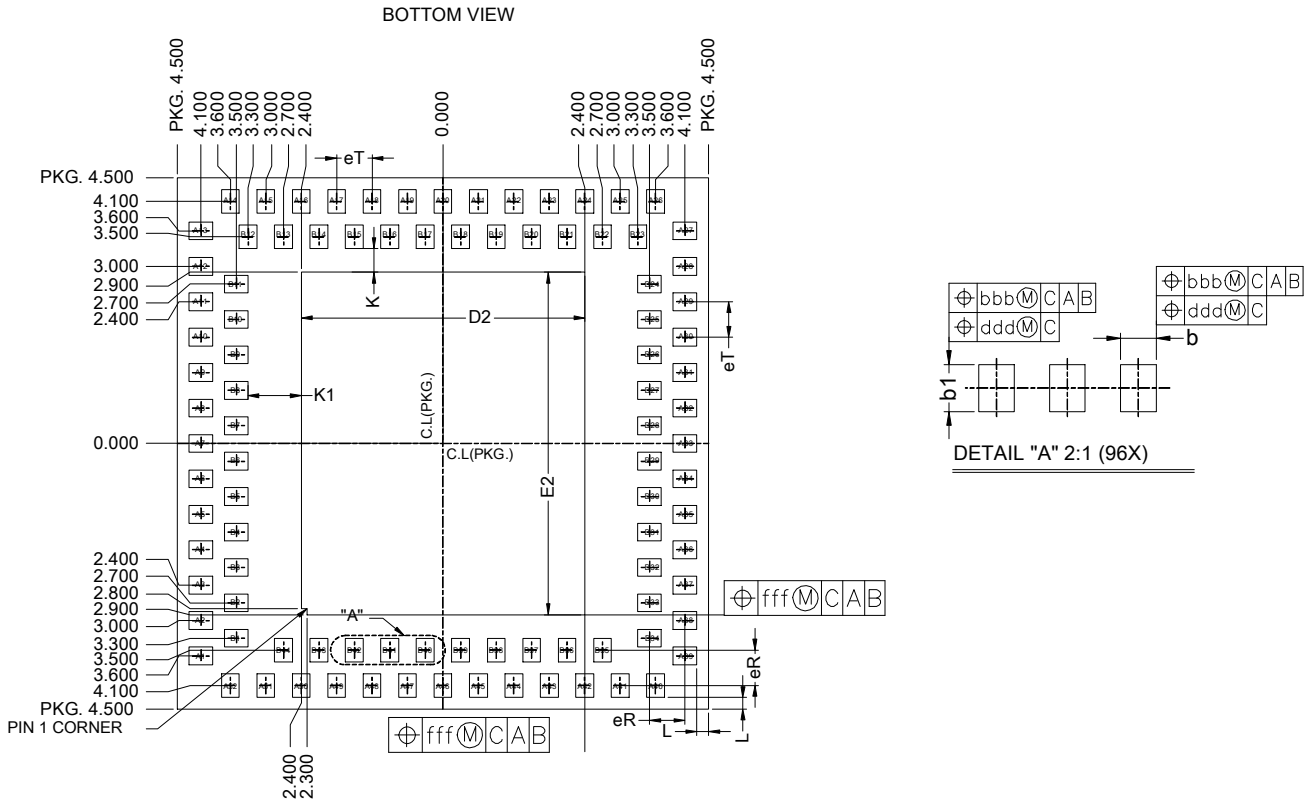


Table 184: 96-Pin aQFN Package Dimensions

Controlling Dimension: MM			
Symbol	**MIN**	**NOM**	**MAX**
A	--	--	0.85
A3	0.020	0.050	0.080
A2	0.640	0.675	0.710
A1	0.120	0.130	0.140
b	0.250	0.300	0.350
b1	0.350	0.400	0.450
D	9.00 BSC		
D2	4.700	4.800	4.900
E	9.00 BSC		
E2	5.700	5.800	5.900
eT	0.600		
eR	0.600		
K	0.350	0.400	0.450
K1	0.850	0.900	0.950
L	0.150	0.200	0.250
Tolerances of Form and Position			
aaa	0.150		
bbb	0.100		
ddd	0.050		
ccc	0.080		
eee	0.080		
fff	0.100		

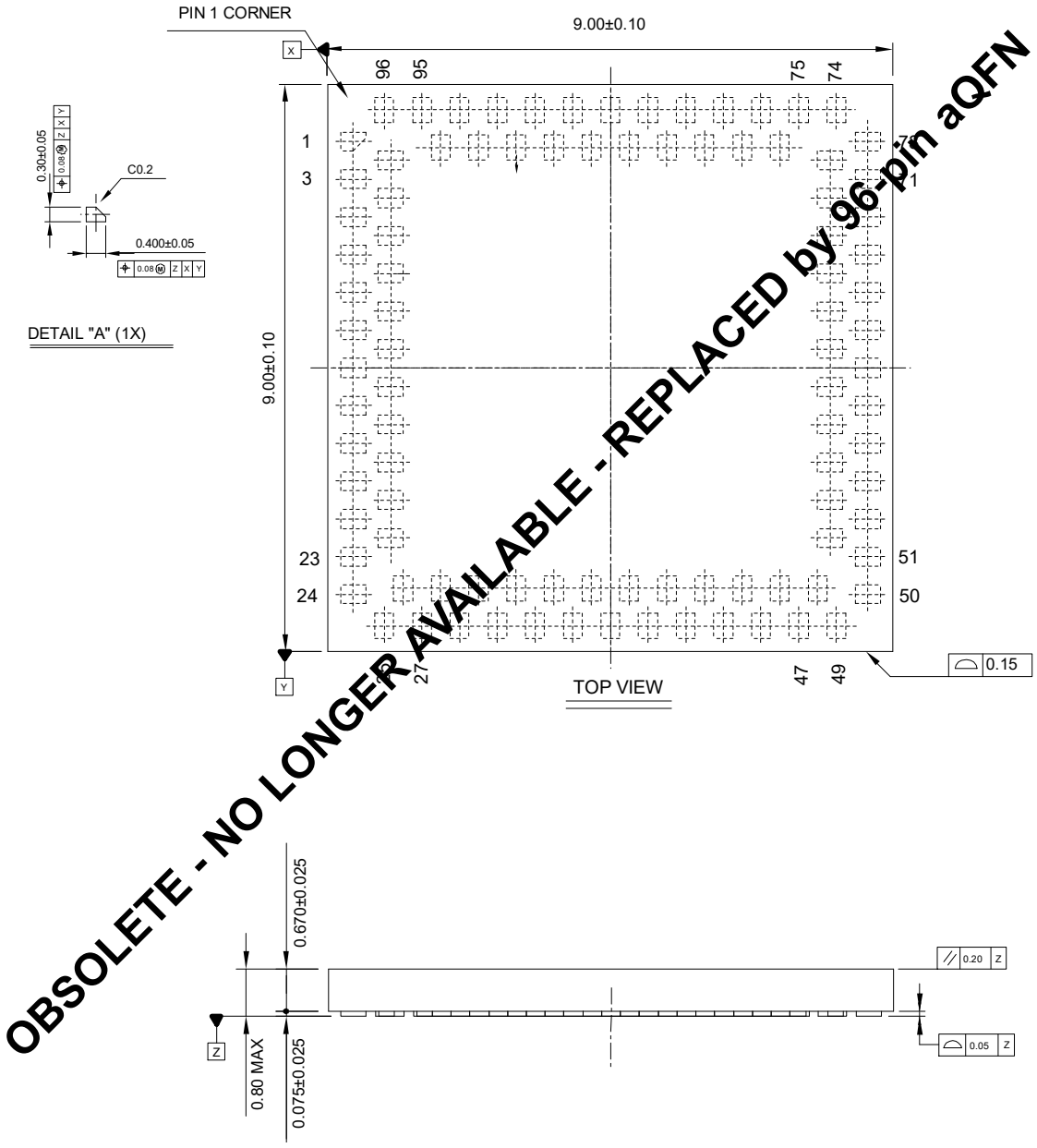
5.4 96-pin BCC Package - No Longer Available - Replaced by the 96-Pin aQFN Package

Note

The 96-Pin aQFN package is a pin compatible replacement for the 96-Pin BCC package. See Product Change Notification 1210066 and Table 186 for details.

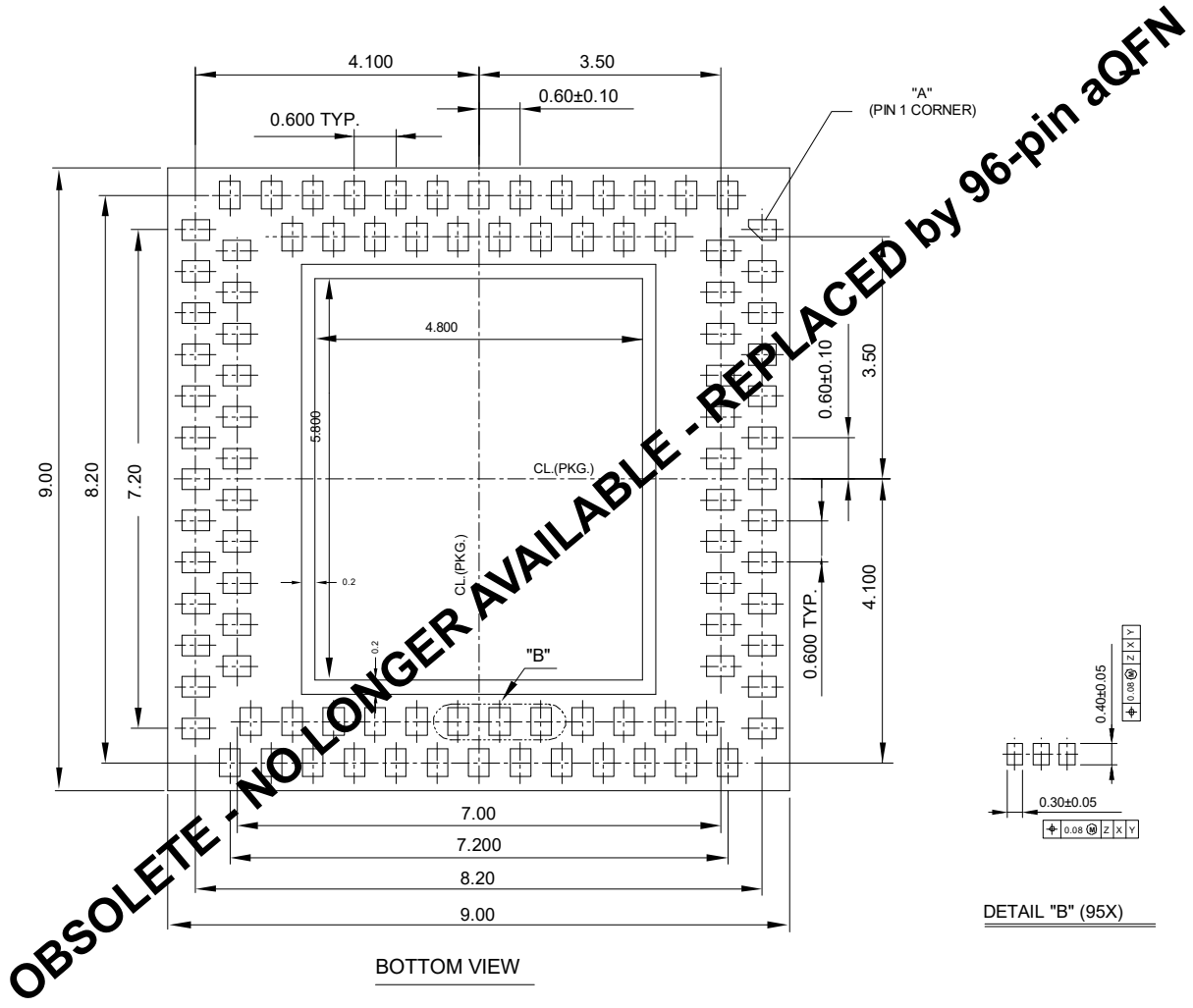
5.4.1 96-pin BCC Package - Top View - OBSOLETE - No Longer Available - Replaced by the 96-Pin aQFN Package

Figure 86: 96-pin BCC Package - Top View - OBSOLETE - No Longer Available - Replaced by the 96-Pin aQFN Package



5.4.2 96-Pin BCC Package - Bottom View - OBSOLETE - No Longer Available - Replaced by the 96-Pin aQFN Package

Figure 87: 96-pin BCC Package - Bottom View - OBSOLETE - No Longer Available - Replaced by the 96-Pin aQFN Package



6 Part Order Numbering/Package Marking

6.1 Part Order Numbering

Figure 88 shows the ordering part numbering scheme for the 88E1111 device. Refer to Marvell Field Application Engineers (FAEs) or representatives for further information when ordering parts.

Figure 88: Sample Part Number

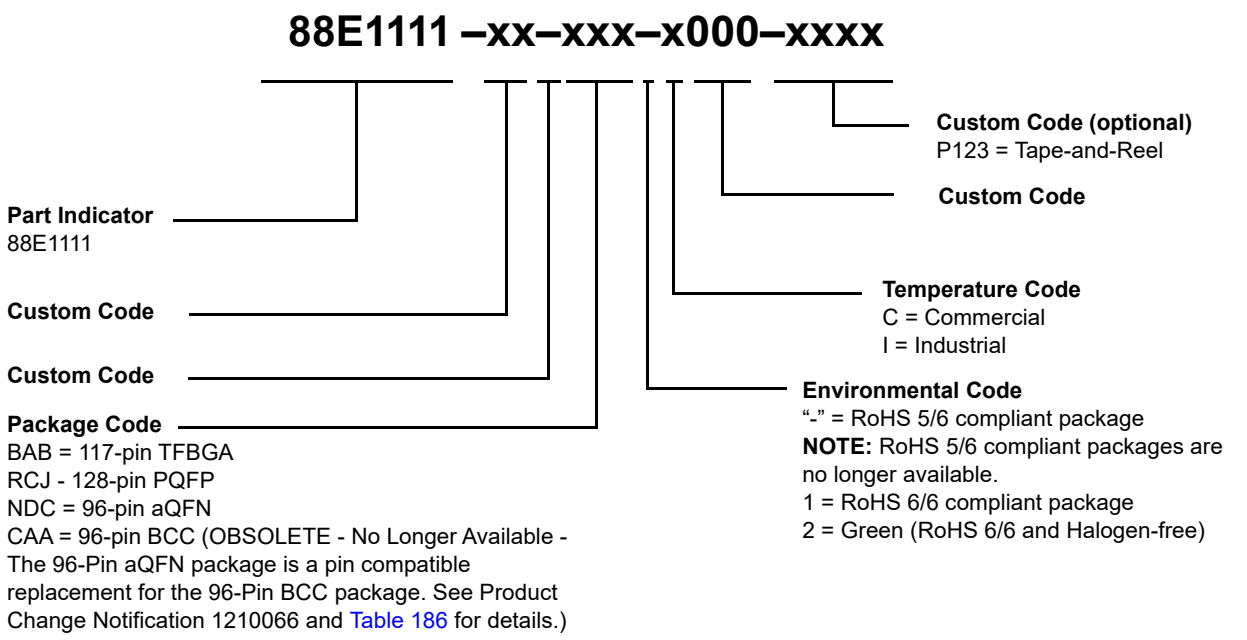


Table 185: 88E1111 Part Order Options

Package Type	Part Order Number
Commercial	
88E1111 117-pin TFBGA	88E1111-XX-BAB1C000 (Commercial, RoHS 6/6 package)
	88E1111-XX-BAB2C000 (Commercial, Green, RoHS 6/6 and Halogen-free package)
88E1111 117-pin TFBGA Tape-and-Reel	88E1111-XX-BAB2C000-P123 (Commercial, Green, RoHS 6/6 and Halogen-free package)
88E1111 128-pin PQFP	88E1111-XX-RCJ1C000 (Commercial, RoHS 6/6 package)
88E1111 96-pin aQFN	88E1111-XX-NDC2C000 (Commercial, Green, RoHS 6/6 and Halogen-free package)
88E1111 96-pin BCC	88E1111-XX-CAA1C000 (Commercial [OBSOLETE - no longer available - replaced by 96-pin aQFN])
Industrial	
88E1111 117-pin TFBGA	88E1111-XX-BAB1I000 (Industrial, RoHS 6/6 package)
88E1111 117-pin TFBGA	88E1111-XX-BAB2I000 (Industrial, Green, RoHS 6/6 and Halogen-free package)
88E1111 96-pin aQFN	88E1111-XX-NDC2I000 (Industrial, Green, RoHS 6/6 and Halogen-free package)
88E1111 96-pin BCC	88E1111-XX-CAA1I000 (Industrial [OBSOLETE - no longer available - replaced by 96-pin aQFN])

Table 186: 96-pin BCC Package Replacement Part Numbers

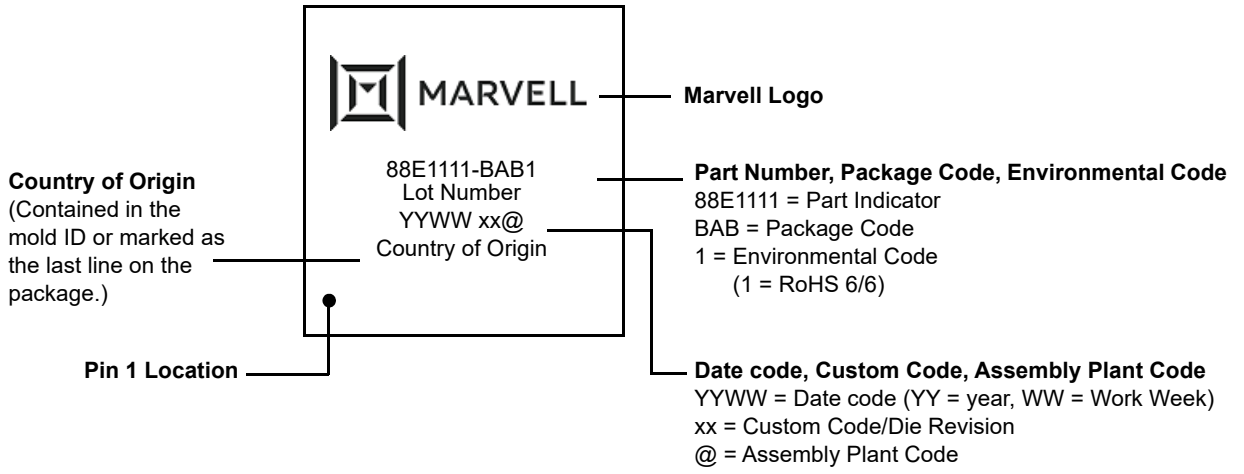
Existing 96-pin BCC Package Part Number	Recommended 96-pin aQFN Package Replacement Part Number
88E1111-B0-CAA-C000	88E1111-B0-NDC2C000
88E1111-B0-CAA1C000	88E1111-B0-NDC2C000
88E1111-B2-CAA-C000	88E1111-B2-NDC2C000
88E1111-B2-CAA-I000	88E1111-B2-NDC2I000
88E1111-B2-CAA1C000	88E1111-B2-NDC2C000
88E1111-B2-CAA1I000	88E1111-B2-NDC2I000

6.2 Package Marking

6.2.1 Commercial

Figure 89 is an example of the package marking and pin 1 location for the 88E1111 117-pin TFBGA Commercial RoHS 6/6 compliant package.

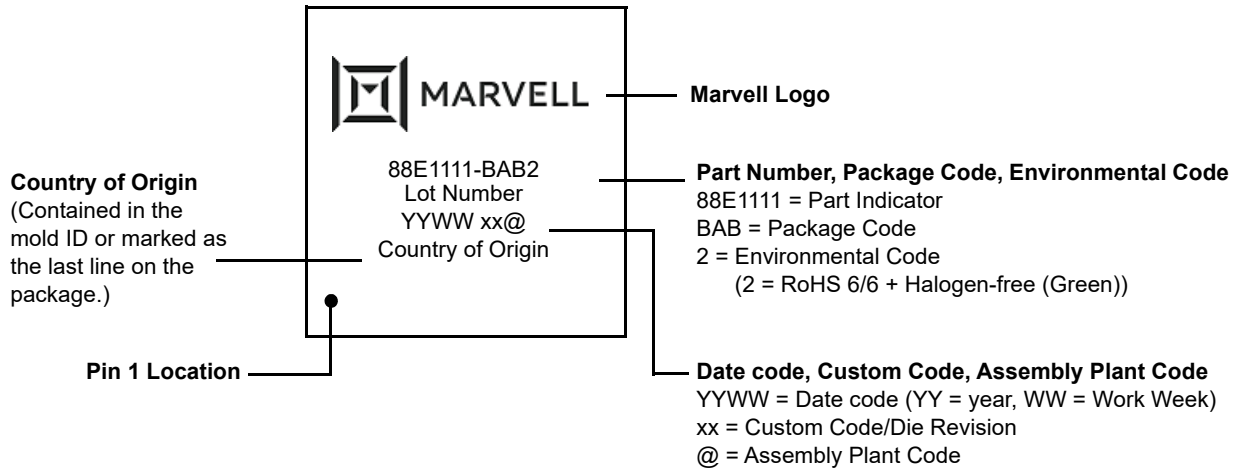
Figure 89: 88E1111 117-pin TFBGA Commercial RoHS 6/6 Compliant Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. Location of markings is approximate.

Figure 90 is an example of the package marking and pin 1 location for the 88E1111 117-pin TFBGA Commercial Green compliant package.

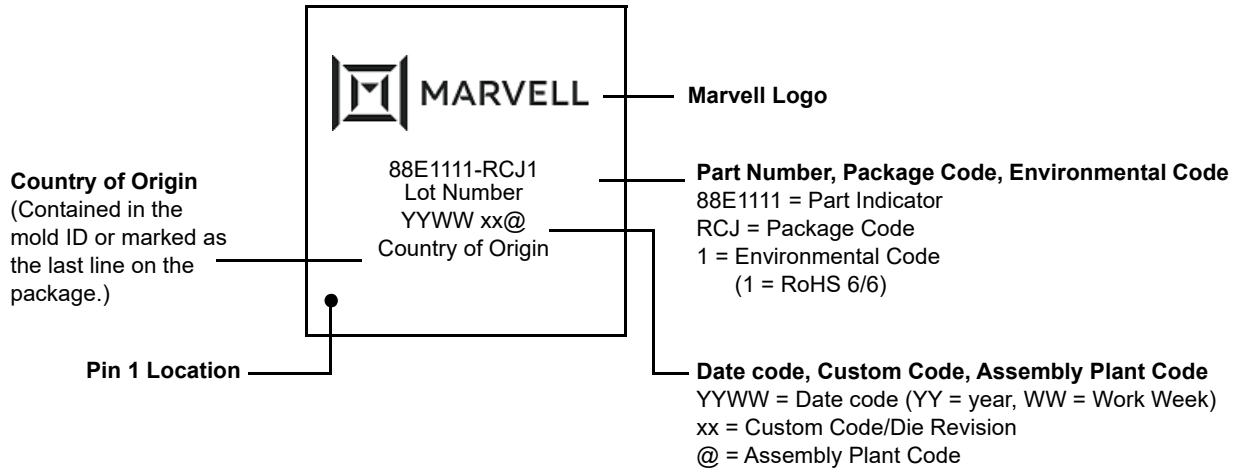
Figure 90: 88E1111 117-pin TFBGA Commercial Green Compliant Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. Location of markings is approximate.

Figure 91 is an example of the package marking and pin 1 location for the 88E1111 128-pin PQFP Commercial RoHS 6/6 compliant package.

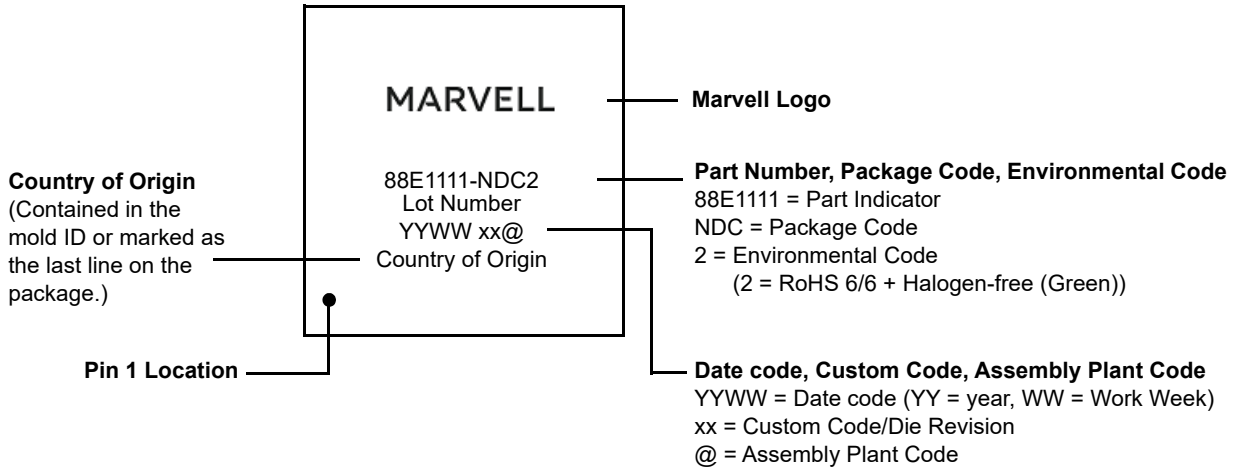
Figure 91: 88E1111 128-pin PQFP Commercial RoHS 6/6 Compliant Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. Location of markings is approximate.

Figure 92 is an example of the package marking and pin 1 location for the 88E1111 96-pin aQFN Commercial Green compliant package.

Figure 92: 88E1111 96-pin aQFN Commercial Green Compliant Package Marking and Pin 1 Location

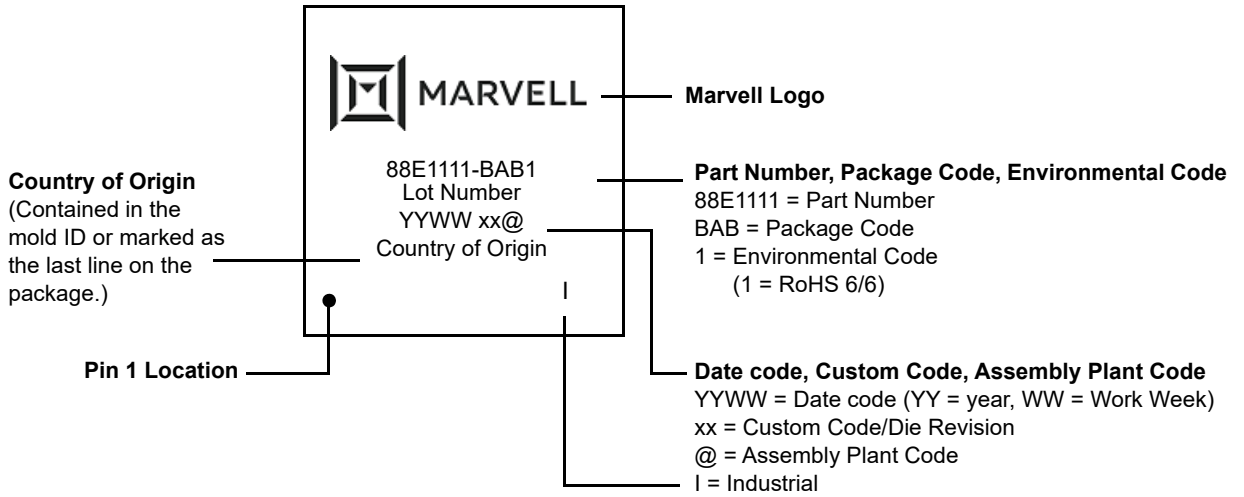


Note: The above drawing is not drawn to scale. Location of markings is approximate.

6.2.2 Industrial

Figure 93 is an example of the package marking and pin 1 location for the 88E1111 117-pin TFBGA Industrial RoHS 6/6 compliant package.

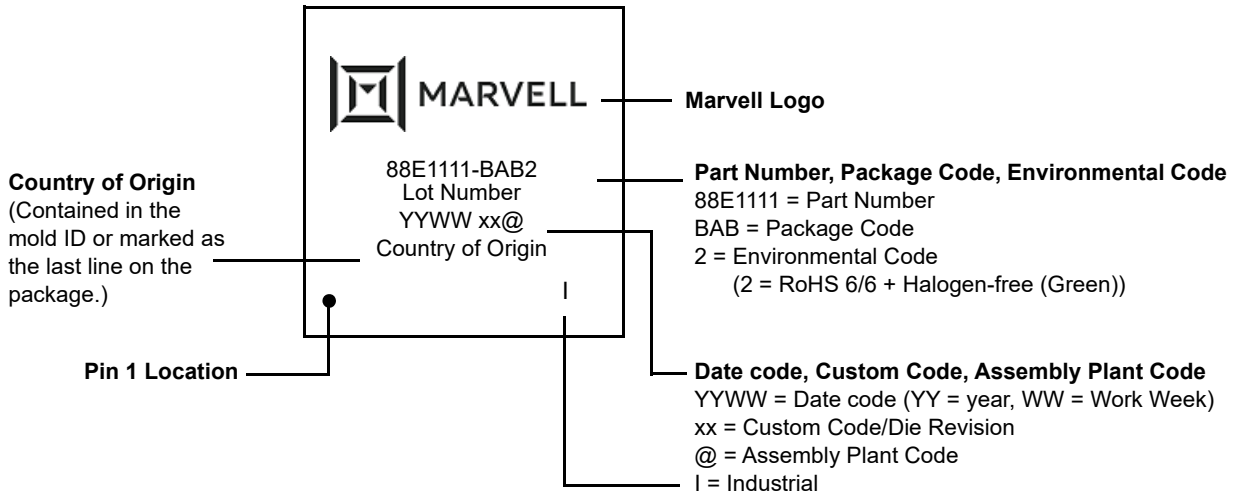
Figure 93: 88E1111 117-pin TFBGA Industrial RoHS 6/6 Compliant Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. Location of markings is approximate.

Figure 94 is an example of the package marking and pin 1 location for the 88E1111 117-pin TFBGA Industrial Green compliant package.

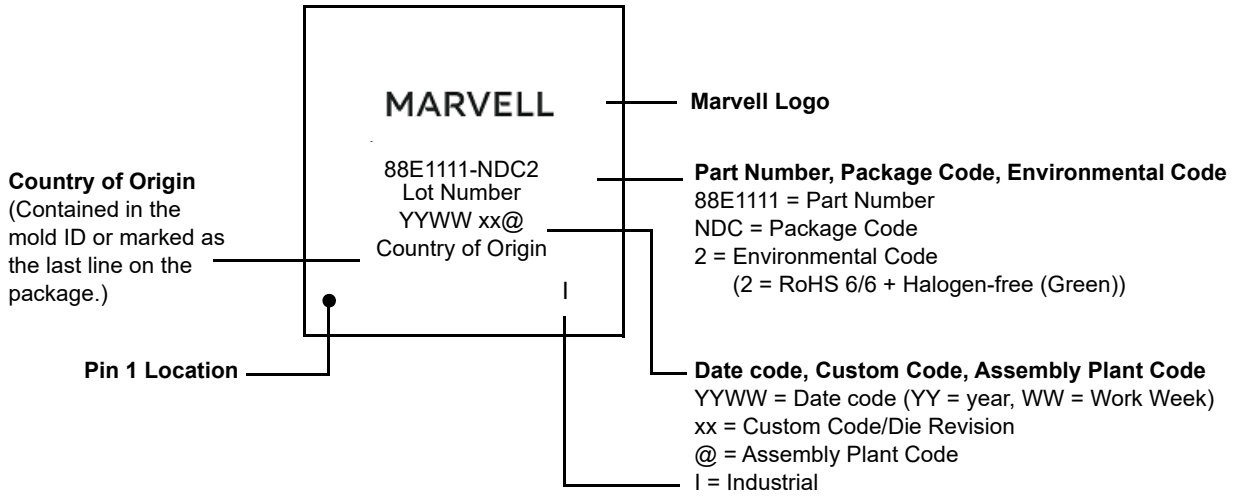
Figure 94: 88E1111 117-pin TFBGA Industrial Green Compliant Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. Location of markings is approximate.

Figure 95 is an example of the package marking and pin 1 location for the 88E1111 96-pin aQFN Industrial Green compliant package.

Figure 95: 88E1111 96-pin aQFN Industrial Green Compliant Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. Location of markings is approximate.

A Revision History

Table 187: Revision History

Revision	Date	Chapter	Detail
Rev. M	08/31/20	All applicable	Corporate rebranding and template update.
			New Marvell logos added to all figures with Marvell logo marking.
			Approved for release as Public accessible datasheet.
		Datasheet Release	
Rev. L	05/16/18	All applicable	Cosmetic enhancements throughout datasheet Added List of Tables and List of Figures
		Part Order Numbering/Package Marking	Added Part Order Numbers: 88E1111-B2-BAB2C000 88E1111-B2-BAB2C000-P123 (Tape-and-Reel) 88E1111-B2-BAB2I000
	06/04/18	Datasheet Release	
Rev. K	07/03/13	Introduction	Features - removed "0.13 Um digital CMOS process"
		All applicable	Replaced "The 96-Pin aQFN package replaces the 96-Pin BCC package." with "The 96-Pin aQFN package is a pin compatible replacement for the 96-Pin BCC package." where applicable.
		Package Mechanical Dimensions	Section 5.5 96-Pin aQFN Package - Bottom View - updated aQFN bottom view mechanical drawing to include the correct pad dimensions.
	10/14/13	Datasheet Release	

Table 187: Revision History (Continued)

Revision	Date	Chapter	Detail
Rev. J	10/16/12	Overview/Features	Replaced 96-pin BCC package details with 96-pin aQFN package details. Also added note regarding 96-Pin BCC package obsolescence, replaced by 96-Pin aQFN package.
		Signal Description	Section 1.2 96-Pin BCC Package replaced by 96-Pin aQFN package. OBSOLETE - NO LONGER AVAILABLE - REPLACED by 96-pin aQFN text added over 96-pin BCC package.
			Section 1.2 Added Note stating 96-Pin aQFN package replaces the 96-pin BCC package, and product change notification details.
			Section 1.2 Added 96-Pin aQFN package pinout.
			Tables 1 - 15 - table headings 96-Pin BCC replaced by 96-Pin aQFN and pin #s updated accordingly.
			Section 1.7 - Section heading 96-Pin BCC replaced by 96-Pin aQFN. 96-Pin aQFN package details added to table.
		Functional Description	Section 2.7.5 - last sentence - replaced "Current Consumption DVDD (1.0V) on page 199 will increase by 20%" with "Current Consumption DVDD (1.2V) on page 200"
			Table 36: 88E111 device to Two-Wire Serial Interface Signal Mapping - changed MDI to MDIO.
			Section 2.22.1.1 Enabling Counters - Register 30: 0x0001 changed to 30.0 = 1
			Section 2.22.1.2 Disabling and Clearing Counters - Register 30: 0x0000 to 30.0 = 0
		Electrical Specifications	Section 4.3.2 Thermal Conditions for 96-Pin aQFN Package - added aQFN package details.
			Section 4.4.4 Current Consumption DVDD - added (1.0V) to title and updated values for 1.0V power to digital core.
			Added Section 4.4.5 Current Consumption DVDD (1.2V)
			Section 4.5.1.2 VDDOX - removed VDDOX 1.5V details as there is no VDDOX 1.5V operation.
		Package Mechanical Dimensions	Sections 5.2 and 5.3 96-pin BCC Package - Top View - added "OBSOLETE..." text to section heading. OBSOLETE - NO LONGER AVAILABLE - REPLACED by 96-pin aQFN text added over 96-pin BCC package drawing.
			Sections 5.2 and 5.3 - Added Note stating 96-Pin aQFN package replaces the 96-pin BCC package, and product change notification details.
			Added Sections 5.4 and 5.5 96-pin aQFN package mechanical drawings.
			Added Table 115 96-pin aQFN Packge Dimensions

Table 187: Revision History (Continued)

Revision	Date	Chapter	Detail
Rev. J	10/16/12	Order Information	Figure 79 Sample Part Number Added Note regarding RoHS 5/6 compliant packages no longer available.
			Figure 79 Sample Part Number Added Green compliant package details.
			Figure 79 Sample Part Number - added OBSOLETE Note to 96-pin BCC Package and Product Change Notification 1210066 reference
			Removed Table 116 88E1111 Part Order Options - RoHS 5.6 Compliant Package
			Table 117 - Added "OBSOLETE..." text to 96-pin BCC Package details.
			Added Table 118 88E1111 Part Order Options - Green Compliant Package
			Added Table 119 96-pin BCC Package Replace Part Numbers
			Section 6.1.1 Removed 88E1111 96-pin BCC Commercial RoHS 5/6 Compliant Package Marking and Pin 1 Location figure
			Section 6.1.1 Removed 88E1111 96-pin BCC Industrial RoHS 5/6 Compliant Package Marking and Pin 1 Location
			Section 6.1.2 Removed 88E1111 96-pin BCC Commercial RoHS 6/6 Compliant Package Marking and Pin 1 Location
			Section 6.1.2 Removed 88E1111 96-pin BCC Industrial RoHS 6/6 Compliant Package Marking and Pin 1 Location
			Added Section 6.1.3 Green Compliant Marking Examples
	11/20/12	Datasheet Release	

Table 187: Revision History (Continued)

Revision	Date	Chapter	Detail
Rev. I	09/11/07	Functional Description	Section 2.3.1.6 - Removed second sentence in next to last paragraph - "Until mode is determined, RXD[3:2] should be...:
			Section 2.3.4 Mode Switching - Added second bullet "When Switching from RGMII to SGMII mode to RGMII to fiber mode..."
			Figures 21 and 22 - Typical MDC/MDIO Read/Write Operation diagrams - updated diagrams to reflect correct format.
			Added TRR Byte Stuffing Blocking Feature
			Table 39: Registers for DTE Power - Register 20.2 Enable power over Ethernet detection HW reset description changed from DIS_POWER bit of configuration to 0.
			Section 2.20.1 - First paragraph, second sentence - changed 30 ohm to 45 ohm.
			Section 2.20.2 - MAC Interface Calibration Register Definitions - Added Table 41 - Miscellaneous Control
			Section 2.20.4 - Fifth paragraph "Figure 33 and Figure 34..." removed references to 1.8V and 3.3V trend lines.
			Figure 33: PMOS Output Impedance - removed 1.8V from title and removed 1.8V trend line.
			Figure 34: NMOS Output Impedance - removed 1.8V from title and removed 1.8V trend line.
			Table 49: LED outputs fro LED_RX Pins - Added Receive Activity to 0, and Receive Activity/Link to 1 and swapped definitions for 0 and 1 to reflect correct Register definition.
		Register Description	able 83: Extended Status Register - Bit 12 - changed 1 and 0 setting definitions to match field name (1000BASE-X full-duplex to 1000BASE-T half-duplex).
			Table 83: Extended Status Register - Bit 13 1000BASE-T Full-Duplex - Definition - changed references of 1000BASE-X to 1000BASE-T.
			Table 83: Extended Status Register - Bit 14 changed 1 and 0 setting definitions to match field name (full-duplex to half-duplex).
			Table 91: Extended PHY Specific Control Register - Bit 15 - Block Carrier Extension Bit - updated definition to include TRR details.
			Table 91: Extended PHY Specific Control Register - Bit 2 DTE detect enable - HW Rst to 0 Definition - removed "Upon hardware reset this bit defaults as follows:" and DIS_DTE and Bit 20.2 settings.
			Table 91: Extended PHY Specific Control Register - Bit 0 - changed bit to Reserved.

Table 187: Revision History (Continued)

Revision	Date	Chapter	Detail
Rev. I (cont.)		Electrical Specifications	Section 4.2 Recommended Operating Conditions - Removed first sentence of footnote 3 "The important parameter..."
			Section 4.4.1 Current Consumption AVDD - removed references to AVDDH and AVDDL - added SERDES and SGMII current consumption details.
			Section 4.4.2 - 4.4.4 - added SERDES and SGMII current consumption details.
			Section 4.8.2 XTAL1 Input Clock Timing - Updated footnote 3.
			Section 4.10.3 100 Mbps MII Receive Timing and 4.10.4 10 Mbps MII Receive Timing - changed MII Output to Clock (min) and MII Clock to Output (min) from 10 ns to 12 ns.
			Section 4.14.8 1000BASE-X to GMII Receive Latency Timing - changed first sentence in footnote 2 to include "which is derived..."
			Section 4.14.16 1000BASE-X to RGMII Receive Latency Timing- changed first sentence in footnote 2 to include "which is derived..."
			Section 4.15.2 Two-Wire Serial Interface (TWSI) TIming - Removed TTWSI_NS symbol row.
	03/15/10	Datasheet release.	
Rev. H	09/21/06	Electrical Specifications	Section 4.4.1 Current Consumption AVDDH, AVDDL - Added “GMII/RGMII over SGMII or ” in the boxes for “GMII/RGMII over 1000Base-X”
			Section 4.4.2 Current Consumption VDDO, VDDOX, VDDOH - Added “GMII/RGMII over SGMII” in the boxes for “GMII/RGMII over 1000Base-X”
			Section 4.4.4 Current Consumption DVDD - Added “GMII/RGMII over SGMII” in the boxes for “GMII/RGMII over 1000Base-X”
		Order Information	Changed Non lead-free to RoHS 5/6 where applicable.
	10/11/06	Datasheet release.	

Table 187: Revision History (Continued)

Revision	Date	Chapter	Detail
Rev. G	12/13/04	All applicable	Updated datasheet to "Preliminary" status.
		Cover	Updated disclaimer.
		Introduction	Added 96-BCC Industrial grade option to features bullets.
		Signal Description	Table 11 - JTAG Interface - Updated TRSTn pin definition to include 1149.1 specification details.
			Section 1.5 I/O State at Various Test or Reset Modes - Power Down and Isolate column - 125CLK row- changed order of 1 = Low, 0 = Toggle to 0 = Toggle, 1 = Low
		Functional Description	Section 2.1.1.2 added the word "Interface" to title.
			Section 2.8.3.1 COMA Mode - Second paragraph - third sentence - added "a hardware reset must be completed for..." and changed "will" to "to" in same sentence.
			Section 2.11.6 Serial Interface Auto-Negotiation Bypass Mode - added Note symbol for note text at end of paragraph.
			Section 2.14.1 MAC Interface Loopback - Figure in section had Table title - changed to Figure title.
			Section 2.14.3 External 1000 Mbps Loopback - added "See the following sections...".
			Section 2.14.3.3 Disabling 1000 Mbps Stub Loopback - Changed last sentence in paragraph to Note.
		Register Description	Table 54 Control Register - Copper - bit 11 Power Down - Removed "On hardware reset bit defaults as follows:" and "PWRUP and Bit 0_0.11" descriptions.
			Table 55 Control Register - Fiber - bit 11 Power Down - Removed "On hardware reset bit defaults as follows:" and "PWRUP and Bit 0_0.11" descriptions.
			Table 83 PHY Specific Control Register - bits 9:8 Energy Detect - SW Rst - changed from Retain to Update.
			Table 84 PHY Specific Status Register - Copper - bit 4 Copper Energy Detect Status - HW Rst and SW Rst changed from 0x1 to 0x0 and added Description text.
			Table 88 Interrupt Status Register - bit 4 Energy Detect Changed - added bit 17.4 details to description.
			Table 98 Extended PHY Specific Status Register - bits 3:0 HWCFG_MODE - added 0001 and 0101 (Reserved) definitions.
			Table 107 Force Gigabit Mode - bit 3 Force Gigabit Mode - added description.
		Electrical Specifications	Section 4.2 Recommended Operating Conditions - added footnote 2 and 1.0V Typ.
			Section 4.5.1.3 VDDO Removed VOL_LED row.
			Section 4.5.1.4 Added + and - details and footnote.
		Order Information	Changed Die Revision to "Custom Code" where applicable.

Table 187: Revision History (Continued)

Revision	Date	Chapter	Detail
Rev. G		Order Information (cont.)	Changed Speed Code to Custom Code where applicable.
			Changed "lead-free" to "RoHS 6/6 compliant" where applicable.
			Added 96-pin BCC package Industrial grade option details and updated marking examples.
		Address Page	Updated Address Page
	02/14/06	Datasheet Release	
Rev. F	11/29/04	Functional Description	Page 52 - Section 2.2.3 Reduced Pin Count GMII (RGMII) - added note that RGMII specification version 2.0 does not support HSTL, but does support the timing specified in RGMII version 2.0.
			Page 73 - Section 2.7.1 VDDO – corrected footnote to remove all references to multi-port pins.
			Page 73 - Section 2.7.2 VDDOH – corrected footnotes to remove all references to multi-port pins, and add "LED_" where applicable.
		Electrical Specifications	Page 196 - Section 4.5.1.1 VDDOH - Added and/or removed "LED_" to the applicable pins to reflect correct pin names used in datasheet.
			Page 198 - Section 4.5.1.3 VDDO - corrected footnote to remove all references to multi-port pins.
			Page 201 - Section 4.6.1.1 - Transmitter DC Characteristics - changed VOD and VOS min and max to "Programmable" and "Variable" respectively.
			Page 202 - Section 4.6.1.2 Common Mode Voltage (Voffset) Calculations - added AC and DC coupling details for CML and LVDS receivers.
			Pages 203 and 204 - Figures 40 and 41 updated/added details to include AC and DC connections to LVDS and CML receivers.
	12/03/04	Datasheet Release	

Table 187: Revision History (Continued)

Revision	Date	Chapter	Detail
Rev. E	04/20/04	All applicable	Updated all Marvell Logos
			Updated complete document to reflect "Preliminary Information" document status.
			Added Industrial Grade offering for 117-Pin TFBGA package.
		Cover	Updated disclaimer.
		Introduction	Overview, second paragraph, third sentence removed "open" and "short" from sentence to read "...will also detect cable opens, or shorts..."
		Signal Description	Rotated 96-Pin BCC package drawing to orientate Pin 1 in lower left corner and removed Pin 1 Location diagram.
			Expanded all pin names (example MDI[0]+/- to MDI[0]+ and MDI[0]- to list pin locations directly across from pin names.
			Added "Z" to all applicable "Output" Pin Types.
			Added "The GMII interface pins..." and "The MAC interface pins..." sentences to GMII/MII introduction text.
			Added "The TBI interface uses..." and "The MAC interface pins..." sentences to TBI introduction text.
			Added "The RGMII interface pins..." and "The MAC interface pins..." sentences to RGMII introduction text.
			Added "The RTBI interface uses..." and "The MAC interface pins..." sentences to RGMII introduction text.
			Added "3.3V Tolerant" to MDC and MDIO Pin Type definitions.
			Added "mA" to all LED Pin Type definitions.
			Added "PU" to TDI Pin Type definition.
			Added "TDI contains an internal 150 kohm pull-up resistor." to TDI pin definition.
			Added "...for XTAL1 input" to SEL_FREQ Pin definition. For NC and Tied Low added "Select", and added "Internally divided to 25 MHz."
			Changed XTAL 1 pin definition by replacing first sentence with "25 MHz +/- 50 ppm or..."
			Added "There is no option for 125 MHz..." to XTAL2 pin definition.
			Added "Power Down and Isolate" column to Section 1.5.
			In Section 1.5 TDO changed all Active to Tri-State
		Functional Description	Section 2.1.1.2 "Signal Detect Input for Fiber Mode" added "...Auto-Negotiation is disabled and..." to last sentence.
			Changed 2.3.3 title from GMII/RGMII to SGMII modes to "GMII/MII to SGMII and RGMII to SGMII mode", as well as related body text.

Table 187: Revision History (Continued)

Revision	Date	Chapter	Detail
Rev. E	04/20/04	Functional Description (cont.)	Section 2.7.5 DVDD description - updated description.
			Section 2.10 Two-Wire Serial Interface - Added "The 88E1111 device will be available for read/write operations 5 ms after hardware reset." to body text.
			Removed 3.3V trend lines from Figure 32 and Figure 33.
			Added Table 49 - LED outputs for LED_RX pins.
		Register Description	Changed all Reserved bit definitions to "These bits must be read and left unchanged when performing a write".
			Table 61 - Auto-Negotiation Advertisement Register - Copper - Added "If 1000BASE-T is advertised then the required next pages..." to description.
			Table 84 - PHY Specific Control Register - bit 3 added "In Modes 011 or 0011 RX_CLK will not toggle..."
			Table 85 - PHY Specific Status Register - Copper - bit 11 Speed and Duplex Resolved added "(If bit 27.11 is 1,..."
		Electrical Specifications	Section 4.4.3 Current Consumption Center_Tap - added "External Magnetics Center Tap Pin" to Pins column.
			Section 4.5.1.1 VDDOH footnote - added "Although VDDOH requires..."
			Section 4.5.1.1 VDDOH VIH_VDDOH Max changed from VDDOH + 0.8V to 3.47V.
			Section 4.5.1.2 VDDOX footnote - added "Although VDDOX requires..."
			Section 4.5.1.2 VDDOX VIH_VDDOX Max changed from VDDOX + 0.8V to 3.47V.
			Section 4.5.1.3 VDDO VIH_VDDO Min changed from 2.0 to 1.7 and Max changed from VDDO + 0.8V to 3.47V.
			Section4.8.1 Reset Timing - Added "Delay after deasserting reset before register Read/write available" details and timing.
			Section 4.8.2 XTAL1 Input Clock Timing - Added 125 MHz timing details.
			Section 4.8.2 XTAL1 Input Clock Timing - Added footnote 1.
			Added Section 4.8.3 125CLK Output Timing.
			Section 4.10.1 100 Mbps MII Transmit Timing MII Setup Time from 15 ns to 10 ns.
			Section 4.10.2 10 Mbps MII Transmit Timing MII Setup Time from 15 ns to 10 ns.
			Section 4.15.2 Two-Wire Serial Interface (TWSI) Timing - TTWSI_HD:DAT Min changed from 0 to 300 for both 100 and 400 kHz
		Part Ordering	Added Lead-Free details
	11/19/04	Datasheet Release	
Rev. D	03/17/04	Cover Page	Updated Disclaimer.
		Signal Description	96-pin package diagram pin 1 name changed from VDDO to DVDD.
	03/18/04	Datasheet Release	

Table 187: Revision History (Continued)

Revision	Date	Chapter	Detail
Rev. C	08/07/03	All applicable	Complete datasheet update to reflect Rev. B template details.
			Added new cover, disclaimer, and address pages.
			Added 128-pin PQFP package details.
			Added Downshift mode details
			Changed Bi-Directional Data Transfer Interface to Two-Wire Serial Interface (TWSI).
			Added Auto-Calibration details.
			Added Packet Generation details.
			Added CRC checker and packet counter details.
			Added Virtual Cable Tester™ (VCT™) details.
			Added Smal Form Factor Pluggable (SFP) details.
		Functional Description	Complete re-organization of section.
		Register Description	Complete re-organization of section.
		Electrical Specifications	Complete re-organization of section.
		Order Information	Complete update of section.
	10/23/03	Datasheet Release	
Rev. B	08/02	Signal Description	Updated DVDD pin description.
		Functional Description	Updated 3.5.7 Power Supply DVDD definition.
		Electrical Specifications	Updated 5.1 Absolute Maximum Ratings details.
			Updated 5.2 Recommended Operating Conditions details.
			Updated 5.4.3 Current Consumption DVDD "parameter" column details.
	09/06/02	Datasheet Release	
Rev. A	06/02	Signal Description	B7 - 117 pin package - updated to AVDD
			N5 - 117 pin package - updated to AVDD
			SEL_FREQ pin definition updated
			No Connect (NC) pin definition updated
		Functional Description	Updated GBIC functional description
			Updated Management Interface pin definition
			Added Cable Diagnostic Feature functional description
	06/20/02	Datasheet Release	
Rev --	02/20/02	All	Initial release to Doc Ctrl.

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