Alaska® M 88E2010/88E2040L

Single and Quad 10/100/1000/2.5G/5GBASE-T Ethernet Transceiver

Datasheet - Public

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PRODUCT OVERVIEW

The Marvell® Alaska® M 88E2010/88E2040L is a family of fully IEEE 802.3bz-compliant 1-port (88E2010) or 4-port (88E2040L) physical layer (PHY) devices. The devices support a wide variety of host-side interfaces including 5GBASE-R, 2500BASE-X, and SGMII to support full backward-compatibility with lower speed legacy Ethernet rates including: 1 Gbps, 100 Mbps, and 10 Mbps.

The flexibility of this device family enables extremely low power across all structured wiring cable lengths, enabling dense 5 Gbps applications. The device supports Category 6-type (screened or unscreened), Category 6A-type (Augmented), Category 7-type cables, and Category 5e-type cables for distances up to 100 meters.

Features

- 1- or 4-port, five-speed PHY. Operates at 10M, 100M, 1G, 2.5G, or 5G data rates on UTP copper lines.
- Compliant with IEEE 802.3bz specifications for 2.5G and 5G modes
- 5GBASE-R, 2500BASE-X, and SGMII system-side interfaces on all devices
- Allows dense multi-port 2.5G/5G applications
- BER better than 1E-15
- 100m reach on CAT 5e for 2.5G and 5G modes
- Clause 45 MDC/MDIO management interface
- Small 10 mm × 12 mm HFCBGA package for 88E2010 single-port applications;
  23 mm × 23 mm HFCBGA package for 88E2040L quad-port applications
- Available in commercial and industrial grades

Figure 1: 88E2010 Top-level Block Diagram

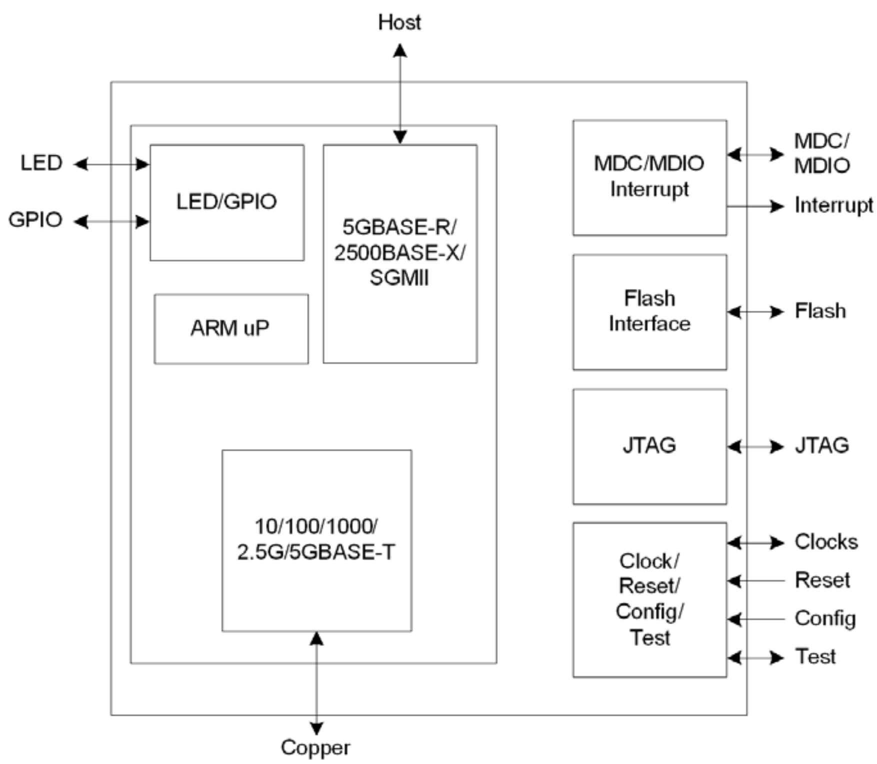
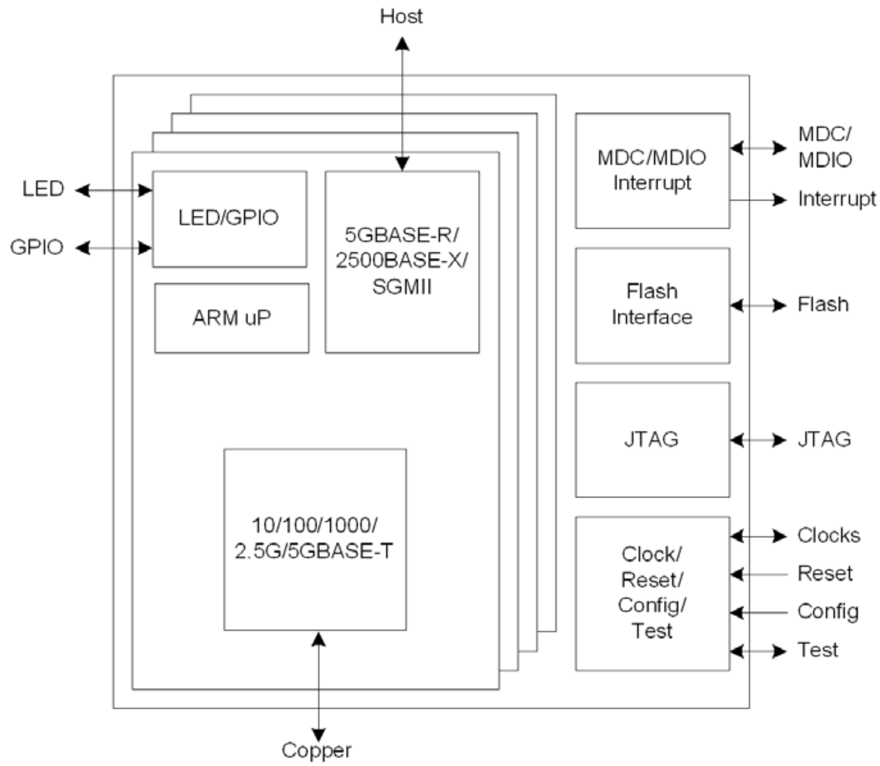


Figure 2: 88E2040L Top-level Block Diagram



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1 General Chip Description

The 88E2010 and 88E2040L devices are a family of one- and four-port integrated multi-speed copper Ethernet Transceivers.

The host interface to the MAC is via 5GBASE-R, 2500BASE-X, or SGMII interface.

Figure 3: 88E2010 Device Functional Block Diagram

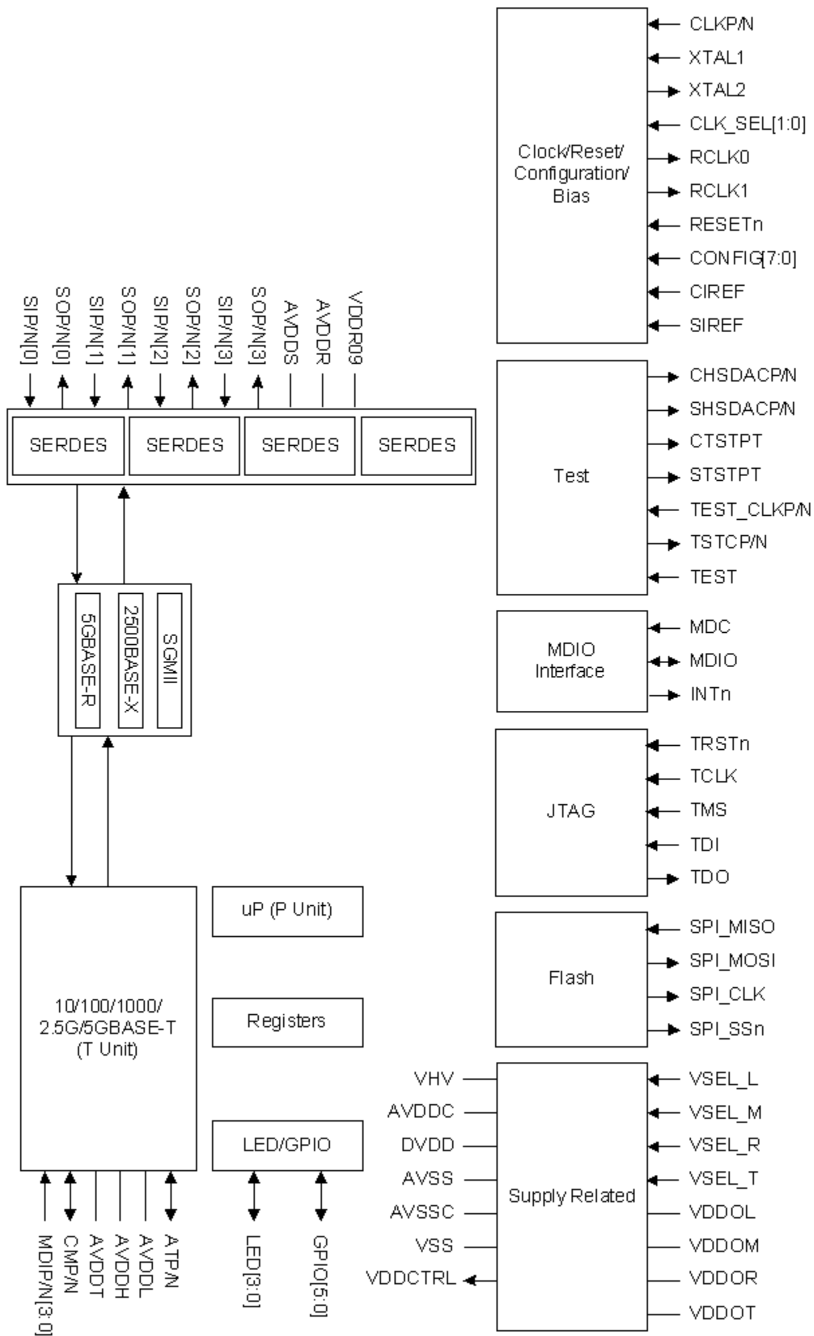
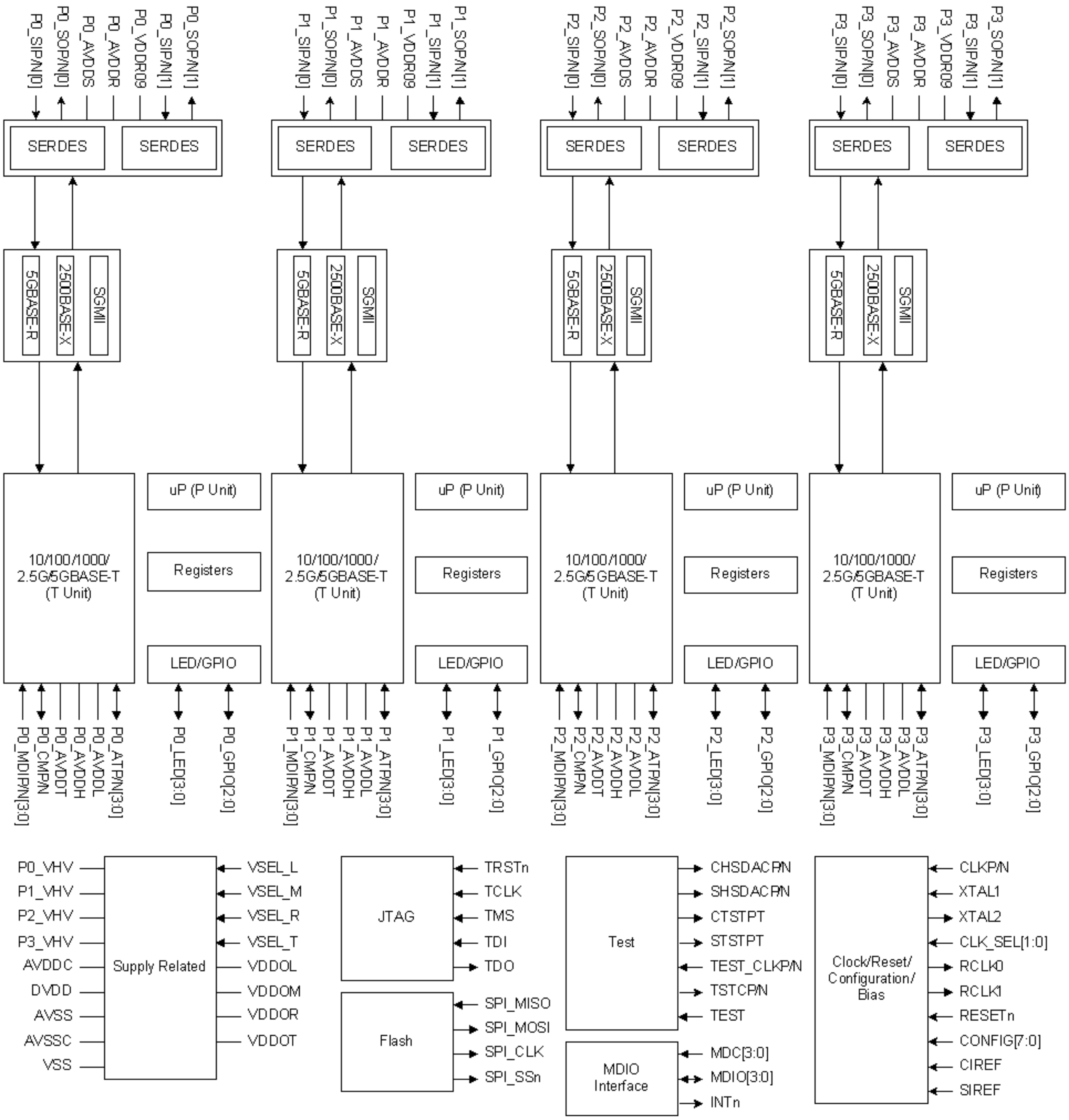


Figure 4: 88E2040L Device Functional Block Diagram



The datasheet is divided as follows:

Section 1 describes the general function of the device.

Section 2 describes the pinout and pin definitions.

Section 3 describes the detailed device functions.

Section 4 describes the copper interface functions (T Unit).

Section 5 describes the MAC interface functions (H Unit).

Section 6 describes the electrical specifications.

Section 7 describes the package mechanical dimensions.

Section 8 describes the order information.

The conventions used in the datasheet are as follows.

All registers are specified per IEEE 802.3 section 45. The format is X.Y, X.Y.Z, or X.Y.Z1:Z2, where X is the device address in decimal from 0 to 31, Y is the register address in hexadecimal from 0000 to FFFF, and Z is the bit in decimal from 0 to 15.

T Unit – 10/100/1000/2.5G/5GBASE-T interface.

H Unit – SGMII/2500BASE-X/5GBASE-R host interface.

Note

Unless otherwise noted, all descriptions apply to the one-, two-, and four-port devices.

2 Signal Description

Table 1: Pin Type Definitions

Pin Type	Definition
H	Input with hysteresis
I/O	Input and output
I	Input only
O	Output only
PU	Internal pull-up
PD	Internal pull-down
D	Open drain output
Z	Tri-state output
mA	DC sink capability

2.1 Pin Maps

2.1.1 88E2010 Device Pin Map

	1	2	3	4	5	6	7	8	9	10	11	12	
A	VSS	AVSS	SOP[3]	AVSS	SOP[2]	AVSS	SOP[1]	AVSS	SOP[0]	AVSS	SHSDACP	AVSS	A
B	MDC	TEST	SON[3]	AVSS	SON[2]	AVSS	SON[1]	AVSS	SON[0]	AVSS	SHSDACN	SIREF	B
C	MDIO	INTn	AVSS	SIP[3]	AVSS	SIP[2]	AVSS	SIP[1]	AVSS	SIP[0]	AVSS	STSTPT	C
D	CONFIG[1]	CONFIG[2]	CONFIG[6]	SIN[3]	AVSS	SIN[2]	AVSS	SIN[1]	AVDDS	SIN[0]	SPI_SSn	RESETn	D
E	LED[0]	CONFIG[3]	AVDDS	AVDDR	AVSS	VDDR09	AVSS	AVDDR	AVDDC	VSEL_R	SPI_MOSI	SPI_MISO	E
F	LED[1]	LED[3]	VSEL_M	VSS	DVDD	VSS	DVDD	VSS	VHV	GPIO[0]	VSS	SPI_CLK	F
G	LED[2]	CONFIG[4]	VDDOM	VSS	DVDD	VSS	DVDD	VSS	VDDOR	GPIO[1]	RCLK1	GPIO[5]	G
H	CONFIG[0]	CONFIG[5]	CONFIG[7]	VSS	DVDD	VSS	DVDD	VSS	VSEL_T	GPIO[2]	GPIO[4]	RCLK0	H
J	CLKN	VDDCTRL	VDDOL	VSS	DVDD	VSS	DVDD	VSS	VDDOT	VSS	TMS	TDO	J
K	CLKP	CLK_SEL[0]	VSEL_L	AVDDL	AVSS	AVDDL	AVSS	AVDDL	AVSS	GPIO[3]	TDI	TCK	K
L	XTAL2	CLK_SEL[1]	ATN	AVSS	AVDDH	AVSS	AVDDH	AVSS	AVDDH	AVSS	TEST_CLKP	TRSTn	L
M	XTAL1	AVDDC	ATP	AVDDT	AVSS	AVDDT	AVSS	AVDDT	AVSS	AVDDC	TEST_CLKN	CTSTPT	M
N	AVSSC	TSTCN	AVSS	MDIP[3]	MDIN[2]	AVDDT	CMN	MDIP[1]	MDIN[0]	AVSS	CHSDACN	CIREF	N
P	AVSS	TSTCP	AVSS	MDIN[3]	MDIP[2]	AVSS	CMP	MDIN[1]	MDIP[0]	AVSS	CHSDACP	AVSS	P
	1	2	3	4	5	6	7	8	9	10	11	12	

(Top View)

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2.1.2 88E2040L Device Pin Map

Due to the large number of pins, the package is depicted graphically over two pages.

	1	2	3	4	5	6	7	8	9	10	11	
A	AVSS	P0_SOP[0]	AVSS	P0_SOP[1]	AVSS	P1_SOP[1]	AVSS	P1_SOP[0]	AVSS	MDIO[1]	MDC[1]	A
B	AVSS	P0_SON[0]	AVSS	P0_SON[1]	AVSS	P1_SON[1]	AVSS	P1_SON[0]	AVSS	VSS	MDC[0]	B
C	P0_SIP[0]	AVSS	P0_SIP[1]	AVSS	AVSS	AVSS	P1_SIP[1]	AVSS	P1_SIP[0]	AVSS	MDIO[0]	C
D	P0_SIN[0]	P0_ AVDDS	P0_SIN[1]	P0_ AVDDS	AVSS	P1_ AVDDS	P1_SIN[1]	P1_ AVDDS	P1_SIN[0]	AVSS	INTn	D
E	AVSS	P0_ VDDR09	AVSS	P0_AVDDR	AVSS	P1_AVDDR	AVSS	P1_ VDDR09	AVSS	AVSS	VDDOM	E
F	P3_LED[0]	P3_LED[1]	P3_LED[2]	P3_LED[3]	P0_VHV	VSS	DVDD	VSS	DVDD	VSS	P1_VHV	F
G	P2_LED[0]	P2_LED[1]	VSS	P2_LED[3]	CONFIG[7]	VSS	DVDD	VSS	DVDD	VSS	DVDD	G
H	CONFIG[4]	P2_LED[2]	P1_LED[2]	CONFIG[5]	VDDOL	VSS	DVDD	VSS	DVDD	VSS	DVDD	H
J	P1_LED[0]	VSS	P1_LED[1]	P1_LED[3]	CONFIG[6]	VSS	DVDD	VSS	DVDD	VSS	DVDD	J
K	P0_LED[0]	P0_LED[1]	P0_LED[2]	P0_LED[3]	VDDOL	VSS	DVDD	VSS	DVDD	VSS	DVDD	K
L	CONFIG[0]	CONFIG[1]	VSS	CONFIG[3]	VSEL_L	VSS	DVDD	VSS	DVDD	VSS	DVDD	L
M	AVSS	CONFIG[2]	CLK_SEL[0]	CLK_SEL[1]	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	M
N	CLKN	P0_ AVDDH	P0_ AVDDH	P0_ AVDDH	P0_ AVDDH	AVSS	P1_ AVDDH	P1_ AVDDH	P1_ AVDDH	P1_ AVDDH	AVSS	N
P	CLKP	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	P
R	XTAL2	P0_ AVDDL	P0_ AVDDL	P0_ AVDDL	P0_ AVDDL	AVSS	P1_ AVDDL	P1_ AVDDL	P1_ AVDDL	P1_ AVDDL	AVSS	R
T	XTAL1	P0_ AVDDT	P0_ AVDDT	P0_ AVDDT	P0_ AVDDT	AVSS	P1_ AVDDT	P1_ AVDDT	P1_ AVDDT	P1_ AVDDT	AVSS	T
U	AVSSC	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	U
V	TSTCN	P0_ATN[0]	P0_ATN[1]	P0_ATN[2]	P0_ATN[3]	AVSS	P1_ATN[3]	P1_ATN[2]	P1_ATN[1]	P1_ATN[0]	AVSS	V
W	TSTCP	P0_ATP[0]	P0_ATP[1]	P0_ATP[2]	P0_ATP[3]	AVSS	P1_ATP[3]	P1_ATP[2]	P1_ATP[1]	P1_ATP[0]	AVSS	W
Y	AVDDC	AVSS	P0_CMN	P0_CMP	AVSS	AVSS	AVSS	P1_CMP	P1_CMN	AVSS	AVSS	Y
AA	AVSS	P0_MDIN[0]	P0_MDIN[1]	P0_MDIN[2]	P0_MDIN[3]	AVSS	P1_MDIN[3]	P1_MDIN[2]	P1_MDIN[1]	P1_MDIN[0]	AVSS	AA
AB	AVSS	P0_MDIP[0]	P0_MDIP[1]	P0_MDIP[2]	P0_MDIP[3]	AVSS	P1_MDIP[3]	P1_MDIP[2]	P1_MDIP[1]	P1_MDIP[0]	AVSS	AB
	1	2	3	4	5	6	7	8	9	10	11	

(Top View)

	12	13	14	15	16	17	18	19	20	21	22	
A	MDC[2]	MDIO[2]	AVSS	P2_SOP[0]	AVSS	P2_SOP[1]	AVSS	P3_SOP[1]	AVSS	P3_SOP[0]	AVSS	A
B	MDC[3]	VSS	AVSS	P2_SON[0]	AVSS	P2_SON[1]	AVSS	P3_SON[1]	AVSS	P3_SON[0]	AVSS	B
C	MDIO[3]	AVSS	P2_SIP[0]	AVSS	P2_SIP[1]	AVSS	AVSS	AVSS	P3_SIP[1]	AVSS	P3_SIP[0]	C
D	TEST	AVSS	P2_SIN[0]	P2_AVDDS	P2_SIN[1]	P2_AVDDS	AVSS	P3_AVDDS	P3_SIN[1]	P3_AVDDS	P3_SIN[0]	D
E	VSEL_M	P2_VDDR09	AVSS	P2_AVDDR	AVSS	P3_AVDDR	AVSS	P3_VDDR09	AVSS	SIREF	AVSS	E
F	P2_VHV	DVDD	VSS	DVDD	VSS	DVDD	P3_VHV	SHSDACP	SHSDACN	AVDDC	STSTPT	F
G	VSS	DVDD	VSS	DVDD	VSS	DVDD	VSS	VDDOR	SPI_MOSI	SPI_SSn	RESETn	G
H	VSS	DVDD	VSS	DVDD	VSS	DVDD	VSS	VSEL_R	P1_GPIO[2]	VSS	P0_GPIO[2]	H
J	VSS	DVDD	VSS	DVDD	VSS	DVDD	VSS	VDDOR	SPI_MISO	P2_GPIO[2]	RCLK1	J
K	VSS	DVDD	VSS	DVDD	VSS	DVDD	VSS	VDDOT	SPI_CLK	P3_GPIO[2]	RCLK0	K
L	VSS	DVDD	VSS	DVDD	VSS	DVDD	VSS	VSEL_T	P0_GPIO[1]	VSS	P0_GPIO[0]	L
M	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	P1_GPIO[1]	P2_GPIO[1]	P1_GPIO[0]	M
N	P2_AVDDH	P2_AVDDH	P2_AVDDH	P2_AVDDH	AVSS	P3_AVDDH	P3_AVDDH	P3_AVDDH	P3_AVDDH	P3_GPIO[1]	P2_GPIO[0]	N
P	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	VSS	P3_GPIO[0]	P
R	P2_AVDDL	P2_AVDDL	P2_AVDDL	P2_AVDDL	AVSS	P3_AVDDL	P3_AVDDL	P3_AVDDL	P3_AVDDL	TCK	TRSTn	R
T	P2_AVDDT	P2_AVDDT	P2_AVDDT	P2_AVDDT	AVSS	P3_AVDDT	P3_AVDDT	P3_AVDDT	P3_AVDDT	TDI	TEST_CLKN	T
U	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	TDO	TEST_CLKP	U
V	P2_ATN[0]	P2_ATN[1]	P2_ATN[2]	P2_ATN[3]	AVSS	P3_ATN[3]	P3_ATN[2]	P3_ATN[1]	P3_ATN[0]	TMS	AVSS	V
W	P2_ATP[0]	P2_ATP[1]	P2_ATP[2]	P2_ATP[3]	AVSS	P3_ATP[3]	P3_ATP[2]	P3_ATP[1]	P3_ATP[0]	AVDDC	CTSTPT	W
Y	AVSS	P2_CMN	P2_CMP	AVSS	AVSS	AVSS	P3_CMP	P3_CMN	AVSS	AVDDC	CIREF	Y
AA	P2_MDIN[0]	P2_MDIN[1]	P2_MDIN[2]	P2_MDIN[3]	AVSS	P3_MDIN[3]	P3_MDIN[2]	P3_MDIN[1]	P3_MDIN[0]	CHSDACN	AVSS	AA
AB	P2_MDIP[0]	P2_MDIP[1]	P2_MDIP[2]	P2_MDIP[3]	AVSS	P3_MDIP[3]	P3_MDIP[2]	P3_MDIP[1]	P3_MDIP[0]	CHSDACP	AVSS	AB
	12	13	14	15	16	17	18	19	20	21	22	

(Top View)

2.2 Pin Description

Note 88E2010 device pin names are not prefixed with P0_.

Table 2: Media Dependent Interface

88E2010Pin #	88E2040L Pin #	Pin Name	Pin Type	Description
P9 N9	AB2 AA2	P0_MDIP[0] P0_MDIN[0]	I/O	Media Dependent Interface[0], Port 0. In 2.5G/5GBASE-T and 1000BASE-T modes in MDI configuration, MDIP/N[0] correspond to BI_DA±. In MDIX configuration, MDIP/N[0] correspond to BI_DB±. In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIP/N[0] are used for the transmit pair. In MDIX configuration, MDIP/N[0] are used for the receive pair. MDIP/N[0] should be tied to ground if not used. The device contains an internal 100Ω resistor between the MDIP/N[0] pins.
N8 P8	AB3 AA3	P0_MDIP[1] P0_MDIN[1]	I/O	Media Dependent Interface[1], Port 0. In 2.5G/5GGBASE-T and 1000BASE-T modes in MDIX configuration, MDIP/N[1] correspond to BI_DA±. In MDI configuration, MDIP/N[1] correspond to BI_DB±. In 100BASE-TX and 10BASE-T modes in MDIX configuration, MDIP/N[1] are used for the transmit pair. In MDI configuration, MDIP/N[1] are used for the receive pair. MDIP/N[1] should be tied to ground if not used. The device contains an internal 100Ω resistor between the MDIP/N[1] pins.
P5 N5	AB4 AA4	P0_MDIP[2] P0_MDIN[2]	I/O	Media Dependent Interface[2], Port 0. In 2.5G/5GGBASE-T and 1000BASE-T modes in MDI configuration, MDIP/N[2] correspond to BI_DC±. In MDIX configuration, MDIP/N[2] correspond to BI_DD±. In 100BASE-TX and 10BASE-T modes, these pins are floating. MDIP/N[2] should be tied to ground if not used. The device contains an internal 100Ω resistor between the MDIP/N[2] pins.

Table 2: Media Dependent Interface (Continued)

88E2010Pin #	88E2040L Pin #	Pin Name	Pin Type	Description
N4 P4	AB5 AA5	P0_MDIP[3] P0_MDIN[3]	I/O	Media Dependent Interface[3], Port 0. In 2.5G/5GBASE-T and 1000BASE-T modes in MDIX configuration, MDIP/N[3] correspond to BI_DC±. In MDI configuration, MDIP/N[3] correspond to BI_ DD±. In 100BASE-TX and 10BASE-T modes these pins are floating. MDIP/N[3] should be tied to ground if not used. The device contains an internal 100Ω resistor between the MDIP/N[3] pins.
-- --	AB10 AA10	P1_MDIP[0] P1_MDIN[0]	I/O	Media Dependent Interface[0], Port 1.
-- --	AB9 AA9	P1_MDIP[1] P1_MDIN[1]	I/O	Media Dependent Interface[1], Port 1.
-- --	AB8 AA8	P1_MDIP[2] P1_MDIN[2]	I/O	Media Dependent Interface[2], Port 1.
-- --	AB7 AA7	P1_MDIP[3] P1_MDIN[3]	I/O	Media Dependent Interface[3], Port 1.
-- --	AB12 AA12	P2_MDIP[0] P2_MDIN[0]	I/O	Media Dependent Interface[0], Port 2.
-- --	AB13 AA13	P2_MDIP[1] P2_MDIN[1]	I/O	Media Dependent Interface[1], Port 2.
-- --	AB14 AA14	P2_MDIP[2] P2_MDIN[2]	I/O	Media Dependent Interface[2], Port 2.
-- --	AB15 AA15	P2_MDIP[3] P2_MDIN[3]	I/O	Media Dependent Interface[3], Port 2.
-- --	AB20 AA20	P3_MDIP[0] P3_MDIN[0]	I/O	Media Dependent Interface[0], Port 3.
-- --	AB19 AA19	P3_MDIP[1] P3_MDIN[1]	I/O	Media Dependent Interface[1], Port 3.
-- --	AB18 AA18	P3_MDIP[2] P3_MDIN[2]	I/O	Media Dependent Interface[2], Port 3.
-- --	AB17 AA17	P3_MDIP[3] P3_MDIN[3]	I/O	Media Dependent Interface[3], Port 3.
P7 N7	Y4 Y3	P0_CMP P0_CMN	I	Media Dependent Interface, optional common mode sense, Port 0
-- --	Y8 Y9	P1_CMP P1_CMN	I	Media Dependent Interface, optional common mode sense, Port 1
-- --	Y14 Y13	P2_CMP P2_CMN	I	Media Dependent Interface, optional common mode sense, Port 2
-- --	Y18 Y19	P3_CMP P3_CMN	I	Media Dependent Interface, optional common mode sense, Port 3

Table 3: SERDES Interface

88E2010 Pin #	88E2040L Pin #	Pin Name	Pin Type	Description
C10 D10	C1 D1	P0_SIP[0] P0_SIN[0]	I	Host Interface Input Lane 0, Port 0 5GBASE-R, 2500BASE-X, SGMII
C8 D8	C3 D3	P0_SIP[1] P0_SIN[1]	I	Host Interface Input Lane 1 Port 0
C6 D6 C4 D4	-- -- -- --	SIP[2] SIN[2] SIP[3] SIN[3]	I	Host Interface Input Lane 2 and 3.
-- --	C9 D9	P1_SIP[0] P1_SIN[0]	I	Host Interface Input Lane 0, Port 1 5GBASE-R, 2500BASE-X, SGMII
-- --	C7 D7	P1_SIP[1] P1_SIN[1]	I	Host Interface Input Lane 1, Port 1
-- --	C14 D14	P2_SIP[0] P2_SIN[0]	I	Host Interface Input Lane 0, Port 2 5GBASE-R, 2500BASE-X, SGMII,
-- --	C16 D16	P2_SIP[1] P2_SIN[1]	I	Host Interface Input Lane 1, Port 2
-- --	C22 D22	P3_SIP[0] P3_SIN[0]	I	Host Interface Input Lane 0, Port 3 5GBASE-R, 2500BASE-X, SGMII
-- --	C20 D20	P3_SIP[1] P3_SIN[1]	I	Host Interface Input Lane 1, Port 3
A9 B9	A2 B2	P0_SOP[0] P0_SON[0]	O	Host Interface Output Lane 0, Port 0 5GBASE-R, 2500BASE-X, SGMII
A7 B7	A4 B4	P0_SOP[1] P0_SON[1]	O	Host Interface Output Lane 1 Port 0
A5 B5 A3 B3	-- -- -- --	SOP[2] SON[2] SOP[3] SON[3]	O	Host Interface Output Lane 2 and 3.
-- --	A8 B8	P1_SOP[0] P1_SON[0]	O	Host Interface Output Lane 0, Port 1 5GBASE-R, 2500BASE-X, SGMII
-- --	A6 B6	P1_SOP[1] P1_SON[1]	O	Host Interface Output Lane 1, Port 1
-- --	A15 B15	P2_SOP[0] P2_SON[0]	O	Host Interface Output Lane 0, Port 2 5GBASE-R, 2500BASE-X, SGMII, lane 0
-- --	A17 B17	P2_SOP[1] P2_SON[1]	O	Host Interface Output Lane 1, Port 2 These signals can be configured as lane 1 host interface.
-- --	A21 B21	P3_SOP[0] P3_SON[0]	O	Host Interface Output Lane 0, Port 3 5GBASE-R, 2500BASE-X, SGMII, lane 0

Table 3: SERDES Interface (Continued)

88E2010 Pin #	88E2040L Pin #	Pin Name	Pin Type	Description
-- --	A19 B19	P3_SOP[1] P3_SON[1]	O	Host Interface Output Lane 1, Port 3 These signals can be configured as lane 1 host interface.

Table 4: Clock/Reset/Reference

88E2010 Pin #	88E2040L Pin #	Pin Name	Pin Type	Description
N12	Y22	CIREF	I	Analog Reference, Copper. This pin should be connected via a 4.99 kΩ 1% resistor to VSS.
B12	E21	SIREF	I	Analog Reference, SERDES. This pin should be connected via a 4.99 kΩ 1% resistor to VSS
K1 J1	P1 N1	CLKP CLKN	I	156.25 MHz or 50 MHz Differential Reference Clock Input. ±50 ppm tolerance.
M1	T1	XTAL1	I	50 MHz crystal input **NOTE:** 50 MHz crystal operation is only supported for commercial-grade devices.
L1	R1	XTAL2	O	50 MHz crystal output **NOTE:** 50 MHz crystal operation is only supported for commercial-grade devices.
H12	K22	RCLK0	O	Recovered Clock Output 0 to 25 MHz
G11	J22	RCLK1	O	Recovered Clock Output 1 to 25 MHz
D12	G22	RESETn	I	Reset 0 = Reset 1 = Normal

Table 5: Management Interface

88E2010 Pin #	88E2040L Pin #	Pin Name	Pin Type	Description
B1 -- -- --	B11 A11 A12 B12	MDC[0] MDC[1] MDC[2] MDC[3]	I	Management Clock pin. MDC is the management data clock reference for the serial management interface. A continuous clock stream is not expected. The maximum continuous frequency supported is 12.5 MHz. A 30 MHz non-continuous mode is also supported. 88E2040L: If the device is configured to shared MDC/MDIO mode, then MDC[2]/MDIO[2] is used to access all four ports. If the device is configured to dual MDC/MDIO mode, then MDC[1]/MDIO[1] is used to access Ports 0 and 1 while MDC[2]/MDIO[2] is used to access Ports 2 and 3. If MDC[x] is unused, then it should be tied low.
C1 -- -- --	C11 A10 A13 C12	MDIO[0] MDIO[1] MDIO[2] MDIO[3]	I/O	Management Data pin. MDIO is the management data. MDIO transfers management data in and out of the device synchronously to MDC. This pin requires a pull-up resistor in a range from 1.5 kΩ to 10 kΩ. If MDIO[x] is unused, then it should be left floating.
C2	D11	INTn	OD	Interrupt pin. (Polarity programmable)

Table 6: SPI Interface

88E2010 Pin #	88E2040L Pin #	Pin Name	Pin Type	Description
D11	G21	SPI_SSn	O	SPI device enable
F12	K20	SPI_CLK	O	SPI clock
E11	G20	SPI_MOSI	O	SPI serial out
E12	J20	SPI_MISO	I	SPI serial in

Table 7: LED

88E2010 Pin #	88E2040L Pin #	Pin Name	Pin Type	Description
E1 F1 G1 F2	K1 K2 K3 K4	P0_LED[0] P0_LED[1] P0_LED[2] P0_LED[3]	I/O	LED Outputs, Port 0
-- -- -- --	J1 J3 H3 J4	P1_LED[0] P1_LED[1] P1_LED[2] P1_LED[3]	I/O	LED Outputs, Port 1
-- -- -- --	G1 G2 H2 G4	P2_LED[0] P2_LED[1] P2_LED[2] P2_LED[3]	I/O	LED Outputs, Port 2
-- -- -- --	F1 F2 F3 F4	P3_LED[0] P3_LED[1] P3_LED[2] P3_LED[3]	I/O	LED Outputs, Port 3
F10 G10 H10	L22 L20 H22	Reserved Reserved Reserved	–	Reserved
K10 H11 G12	-- -- --	Reserved Reserved Reserved	–	Reserved
-- -- --	M22 M20 H20	Reserved Reserved Reserved	–	Reserved
-- -- --	N22 M21 J21	Reserved Reserved Reserved	–	Reserved
-- -- --	P22 N21 K21	Reserved Reserved Reserved	–	Reserved

Table 8: Configuration

88E2010 Pin #	88E2040L Pin #	Pin Name	Pin Type	Description
K2 L2	M3 M4	CLK_SEL[0] CLK_SEL[1]	I, PD	Reference clock selection 00 = 50 MHz XTAL1/2 01 = 50 MHz CLKP/N 10 = 156.25 MHz CLKP/N 11 = Reserved **NOTE:** 50 MHz crystal operation is only supported for commercial-grade devices.
H1 D1 D2 E2 G2 H2 D3 H3	L1 L2 M2 L4 H1 H4 J5 G5	CONFIG[0] CONFIG[1] CONFIG[2] CONFIG[3] CONFIG[4] CONFIG[5] CONFIG[6] CONFIG[7]	I	Hardware Configuration
K3	L5	VSEL_L	I	VDDOL Voltage Level Select VSS = 2.5V/3.3V, VDDOL = 1.5V/1.8V
F3	E12	VSEL_M	I	VDDOM Voltage Level Select VSS = 2.5V/3.3V, VDDOM = 1.2V/1.5V/1.8V
E10	H19	VSEL_R	I	VDDOR Voltage Level Select VSS = 2.5V/3.3V, VDDOR = 1.5V/1.8V
H9	L19	VSEL_T	I	VDDOT Voltage Level Select VSS = 2.5V/3.3V, VDDOT = 1.5V/1.8V

Table 9: JTAG Interface

88E2010 Pin #	88E2040L Pin #	Pin Name	Pin Type	Description
K11	T21	TDI	I, PU	JTAG Data Input
J12	U21	TDO	O	JTAG Data Output
J11	V21	TMS	I, PU	JTAG Mode Select
K12	R21	TCK	I, PU	JTAG Clock
L12	R22	TRSTn	I, PU	JTAG Reset. TRSTn pin requires a 4.7 kΩ pull-down externally for normal operation.

Table 10: Test Pins

88E2010 Pin #	88E2040L Pin #	Pin Name	Pin Type	Description
M3 L3 -- -- -- -- -- --	W2 V2 W3 V3 W4 V4 W5 V5	P0_ATP[0] P0_ATN[0] P0_ATP[1] P0_ATN[1] P0_ATP[2] P0_ATN[2] P0_ATP[3] P0_ATN[3]	O	Analog Test Port 0
-- -- -- -- -- -- -- --	W10 V10 W9 V9 W8 V8 W7 V7	P1_ATP[0] P1_ATN[0] P1_ATP[1] P1_ATN[1] P1_ATP[2] P1_ATN[2] P1_ATP[3] P1_ATN[3]	O	Analog Test Port 1
-- -- -- -- -- -- -- --	W12 V12 W13 V13 W14 V14 W15 V15	P2_ATP[0] P2_ATN[0] P2_ATP[1] P2_ATN[1] P2_ATP[2] P2_ATN[2] P2_ATP[3] P2_ATN[3]	O	Analog Test Port 2
-- -- -- -- -- -- -- --	W20 V20 W19 V19 W18 V18 W17 V17	P3_ATP[0] P3_ATN[0] P3_ATP[1] P3_ATN[1] P3_ATP[2] P3_ATN[2] P3_ATP[3] P3_ATN[3]	O	Analog Test Port 3
P11 N11	AB21 AA21	CHSDACP CHSDACN	O	Copper AC Test
A11 B11	F19 F20	SHSDACP SHSDACN	O	SERDES AC Test
M12	W22	CTSTPT	O	Copper DC Test
C12	F22	STSTPT	O	SERDES DC Test
L11 M11	U22 T22	TEST_CLKP TEST_CLKN	I	Test clock input

Table 10: Test Pins (Continued)

88E2010 Pin #	88E2040L Pin #	Pin Name	Pin Type	Description
P2 N2	W1 V1	TSTCP TSTCN	O	Test clock output When using the 50 MHz XTAL option, the (CLK_SEL[1:0] = 00), TSTCP/N output pins must be AC coupled with a 0.1 µF capacitor and connected to CLK_P/N input pins on the board (88E2040L devices only).
B2	D12	TEST	I, PD	Test Enable. This pin should be left floating if not used.

Table 11: Power and Ground

88E2010 Pin #	88E2040L Pin #	Pin Name	Pin Type	Description
F9 -- -- --	F5 F11 F12 F18	P0_VHV P1_VHV P2_VHV P3_VHV	Power	High Voltage Fuse Programming These pins must be left floating.
L5 L7 L9 --	N2 N3 N4 N5	P0_AVDDH	Power	1.8V or 2.0V analog power
-- -- -- -- --	N7 N8 N9 N10	P1_AVDDH	Power	
-- -- -- --	N12 N13 N14 N15	P2_AVDDH	Power	
-- -- -- --	N17 N18 N19 N20	P3_AVDDH	Power	
M4 M6 M8 N6	T2 T3 T4 T5	P0_AVDDT	Power	2.5V or 2.3V analog power and center-tap power.
-- -- -- --	T7 T8 T9 T10	P1_AVDDT	Power	
-- -- -- --	T12 T13 T14 T15	P2_AVDDT	Power	
-- -- -- --	T17 T18 T19 T20	P3_AVDDT	Power	

Table 12: Power and Ground (Continued)

88E2010 Pin #	88E2040L Pin #	Pin Name	Pin Type	Description
E9 M2 M10 --	F21 W21 Y1 Y21	AVDDC	Power	1.5V analog power
K4 K6 K8 -- --	R2 R3 R4 R5	P0_AVDDL	Power	1.5V analog power
-- -- -- -- --	R7 R8 R9 R10	P1_AVDDL	Power	
-- -- -- --	R12 R13 R14 R15	P2_AVDDL	Power	
-- -- -- --	R17 R18 R19 R20	P3_AVDDL	Power	
D9 E3	D2 D4	P0_AVDDS	Power	1.5V analog power
-- --	D6 D8	P1_AVDDS	Power	
-- --	D15 D17	P2_AVDDS	Power	
-- --	D19 D21	P3_AVDDS	Power	
E4 E8 -- --	E4 E6 E15 E17	P0_AVDDR P1_AVDDR P2_AVDDR P3_AVDDR	Power	1.5V analog power
E6 -- -- --	E2 E8 E13 E19	P0_VDDR09 P1_VDDR09 P2_VDDR09 P3_VDDR09	Power	0.9V internally regulated power. This pin must be tied to a capacitor. Do not connect this pin to external power.

Table 12: Power and Ground (Continued)

88E2010 Pin #	88E2040L Pin #	Pin Name	Pin Type	Description
F5 F7 G5 G7 H5 H7 J5 J7	F7 F9 F13 F15 F17 G7 G9 G11 G13 G15 G17 H7 H9 H11 H13 H15 H17 J7 J9 J11 J13 J15 J17 K7 K9 K11 K13 K15 K17 L7 L9 L11 L13 L15 L17	DVDD	Power	Digital power 0.8V for C-grade 0.88V for I-grade
J3	H5 K5	VDDOL	Power	I/O power - LED, CONFIG, CLK_SEL
G3	E11	VDDOM	Power	I/O power - MDC, MDIO, INTn, TEST
G9	G19 J19	VDDOR	Power	I/O power - RESETn, SPI, RCLK0, RCLK1
J9	K19	VDDOT	Power	I/O power - JTAG

Table 12: Power and Ground (Continued)

88E2010 Pin #	88E2040L Pin #	Pin Name	Pin Type	Description
A2 A4 A6 A8 A10 A12 B4 B6 B8 B10 C3 C5 C7 C9 C11 D5 D7 E5 E7 K5 K7 K9 L4 L6 L8 L10 M5 M7 M9 N3 N10 P1 P3 P6 P10 P12	A1 A3 A5 A7 A9 A14 A16 A18 A20 A22 B1 B3 B5 B7 B9 B14 B16 B18 B20 B22 C2 C4 C5 C6 C8 C10 C13 C15 C17 C18 C19 C21 D5 D10 D13 D18 E1 E3 E5 E7 E9 E10 E14 E16 E18 E20 E22 M1 M5 M6 M7 M8	AVSS	Power	Analog Ground

Table 12: Power and Ground (Continued)

88E2010 Pin #	88E2040L Pin #	Pin Name	Pin Type	Description
--	M9 M10 M11 M12 M13 M14 M15 M16 M17 M18 M19 N6 N11 N16 P2 P3 P4 P5 P6 P7 P8 P9 P10 P11 P12 P13 P14 P15 P16 P17 P18 P19 P20 R6 R11 R16 T6 T11 T16 U2 U3 U4 U5 U6 U7 U8 U9 U10 U11 U12 U13 U14	AVSS (cont.)	Power	Analog Ground

Table 12: Power and Ground (Continued)

88E2010 Pin #	88E2040L Pin #	Pin Name	Pin Type	Description
--	U15 U16 U17 U18 U19 U20 V6 V11 V16 V22 W6 W11 W16 Y2 Y5 Y6 Y7 Y10 Y11 Y12 Y15 Y16 Y17 Y20 AA1 AA6 AA11 AA16 AA22 AB1 AB6 AB11 AB16 AB22	AVSS (cont.)	Power	Analog Ground

Table 12: Power and Ground (Continued)

88E2010 Pin #	88E2040L Pin #	Pin Name	Pin Type	Description
N1	U1	AVSSC	Power	Analog Ground This must be isolated from AVSS.
A1 F4 F6 F8 F11 G4 G6 G8 H4 H6 H8 J4 J6 J8 J10	B10 B13 F6 F8 F10 F14 F16 G3 G6 G8 G10 G12 G14 G16 G18 H6 H8 H10 H12 H14 H16 H18 H21 J2 J6 J8 J10 J12 J14 J16 J18 K6 K8 K10 K12 K14 K16 K18 L3 L6 L8 L10 L12 L14 L16 L18 L21 P21	VSS	Power	Ground

2.3 Pin Assignment Lists

2.3.1 88E2010 Device Pin Assignment List

Table 13: 88E2010 Pin List — Alphabetical by Signal Name

Pin Number	Pin Name
L3	ATN
M3	ATP
K4	AVDDL
K6	AVDDL
K8	AVDDL
L5	AVDDH
L7	AVDDH
L9	AVDDH
M4	AVDDT
M6	AVDDT
M8	AVDDT
N6	AVDDT
E9	AVDDC
M2	AVDDC
M10	AVDDC
E4	AVDDR
E8	AVDDR
D9	AVDDS
E3	AVDDS
A2	AVSS
A4	AVSS
A6	AVSS
A8	AVSS
A10	AVSS
A12	AVSS
B4	AVSS
B6	AVSS

Pin Number	Pin Name
B8	AVSS
B10	AVSS
C3	AVSS
C5	AVSS
C7	AVSS
C9	AVSS
C11	AVSS
D5	AVSS
D7	AVSS
E5	AVSS
E7	AVSS
K5	AVSS
K7	AVSS
K9	AVSS
L4	AVSS
L6	AVSS
L8	AVSS
L10	AVSS
M5	AVSS
M7	AVSS
M9	AVSS
N3	AVSS
N10	AVSS
P1	AVSS
P3	AVSS
P6	AVSS
P10	AVSS
P12	AVSS
N1	AVSSC
N11	CHSDACN

Pin Number	Pin Name
P11	CHSDACP
N12	CIREF
K2	CLK_SEL[0]
L2	CLK_SEL[1]
J1	CLKN
K1	CLKP
N7	CMN
P7	CMP
H1	CONFIG[0]
D1	CONFIG[1]
D2	CONFIG[2]
E2	CONFIG[3]
G2	CONFIG[4]
H2	CONFIG[5]
D3	CONFIG[6]
H3	CONFIG[7]
M12	CTSTPT
F5	DVDD
F7	DVDD
G5	DVDD
G7	DVDD
H5	DVDD
H7	DVDD
J5	DVDD
J7	DVDD
F10	–
G10	–
H10	–
K10	–
H11	–

Pin Number	Pin Name
G12	–
C2	INTn
E1	LED[0]
F1	LED[1]
G1	LED[2]
F2	LED[3]
B1	MDC
N9	MDIN[0]
P8	MDIN[1]
N5	MDIN[2]
P4	MDIN[3]
C1	MDIO
P9	MDIP[0]
N8	MDIP[1]
P5	MDIP[2]
N4	MDIP[3]
H12	RCLK0
G11	RCLK1
D12	RESETn
B11	SHSDACN
A11	SHSDACP
D10	SIN[0]
D8	SIN[1]
D6	SIN[2]
D4	SIN[3]
C10	SIP[0]
C8	SIP[1]
C6	SIP[2]
C4	SIP[3]
B12	SIREF

Pin Number	Pin Name
B9	SON[0]
B7	SON[1]
B5	SON[2]
B3	SON[3]
A9	SOP[0]
A7	SOP[1]
A5	SOP[2]
A3	SOP[3]
F12	SPI_CLK
E12	SPI_MISO
E11	SPI_MOSI
D11	SPI_SSn
C12	STSTPT
K12	TCK
K11	TDI
J12	TDO
B2	TEST
M11	TEST_CLKN
L11	TEST_CLKP
J11	TMS
L12	TRSTn
N2	TSTCN
P2	TSTCP
J2	VDDCTRL
J3	VDDOL
G3	VDDOM
G9	VDDOR
J9	VDDOT
E6	VDDR09
F9	VHV

Pin Number	Pin Name
K3	VSEL_L
F3	VSEL_M
E10	VSEL_R
H9	VSEL_T
A1	VSS
F4	VSS
F6	VSS
F8	VSS
F11	VSS
G4	VSS
G6	VSS
G8	VSS
H4	VSS
H6	VSS
H8	VSS
J4	VSS
J6	VSS
J8	VSS
J10	VSS
M1	XTAL1
L1	XTAL2

2.3.2 88E2040L Device Pin Assignment List

Table 14: 88E2040L Pin List — Alphabetical by Signal Name

Pin Number	Pin Name
F21	AVDDC
W21	AVDDC
Y1	AVDDC
Y21	AVDDC
A1	AVSS
A3	AVSS
A5	AVSS
A7	AVSS
A9	AVSS
A14	AVSS
A16	AVSS
A18	AVSS
A20	AVSS
A22	AVSS
B1	AVSS
B3	AVSS
B5	AVSS
B7	AVSS
B9	AVSS
B14	AVSS
B16	AVSS
B18	AVSS
B20	AVSS
B22	AVSS
C2	AVSS
C4	AVSS
C5	AVSS
C6	AVSS

Pin Number	Pin Name
C8	AVSS
C10	AVSS
C13	AVSS
C15	AVSS
C17	AVSS
C18	AVSS
C19	AVSS
C21	AVSS
D5	AVSS
D10	AVSS
D13	AVSS
D18	AVSS
E1	AVSS
E3	AVSS
E5	AVSS
E7	AVSS
E9	AVSS
E10	AVSS
E14	AVSS
E16	AVSS
E18	AVSS
E20	AVSS
E22	AVSS
M1	AVSS
M5	AVSS
M6	AVSS
M7	AVSS
M8	AVSS
M9	AVSS
M10	AVSS

Pin Number	Pin Name
M11	AVSS
M12	AVSS
M13	AVSS
M14	AVSS
M15	AVSS
M16	AVSS
M17	AVSS
M18	AVSS
M19	AVSS
N6	AVSS
N11	AVSS
N16	AVSS
P2	AVSS
P3	AVSS
P4	AVSS
P5	AVSS
P6	AVSS
P7	AVSS
P8	AVSS
P9	AVSS
P10	AVSS
P11	AVSS
P12	AVSS
P13	AVSS
P14	AVSS
P15	AVSS
P16	AVSS
P17	AVSS
P18	AVSS
P19	AVSS

Pin Number	Pin Name
P20	AVSS
R6	AVSS
R11	AVSS
R16	AVSS
T6	AVSS
T11	AVSS
T16	AVSS
U2	AVSS
U3	AVSS
U4	AVSS
U5	AVSS
U6	AVSS
U7	AVSS
U8	AVSS
U9	AVSS
U10	AVSS
U11	AVSS
U12	AVSS
U13	AVSS
U14	AVSS
U15	AVSS
U16	AVSS
U17	AVSS
U18	AVSS
U19	AVSS
U20	AVSS
V6	AVSS
V11	AVSS
V16	AVSS
V22	AVSS

Pin Number	Pin Name
W6	AVSS
W11	AVSS
W16	AVSS
Y2	AVSS
Y5	AVSS
Y6	AVSS
Y7	AVSS
Y10	AVSS
Y11	AVSS
Y12	AVSS
Y15	AVSS
Y16	AVSS
Y17	AVSS
Y20	AVSS
AA1	AVSS
AA6	AVSS
AA11	AVSS
AA16	AVSS
AA22	AVSS
AB1	AVSS
AB6	AVSS
AB11	AVSS
AB16	AVSS
AB22	AVSS
U1	AVSSC
AA21	CHSDACN
AB21	CHSDACP
Y22	CIREF
M3	CLK_SEL[0]
M4	CLK_SEL[1]

Pin Number	Pin Name
N1	CLKN
P1	CLKP
L1	CONFIG[0]
L2	CONFIG[1]
M2	CONFIG[2]
L4	CONFIG[3]
H1	CONFIG[4]
H4	CONFIG[5]
J5	CONFIG[6]
G5	CONFIG[7]
W22	CTSTPT
F7	DVDD
F9	DVDD
F13	DVDD
F15	DVDD
F17	DVDD
G7	DVDD
G9	DVDD
G11	DVDD
G13	DVDD
G15	DVDD
G17	DVDD
H7	DVDD
H9	DVDD
H11	DVDD
H13	DVDD
H15	DVDD
H17	DVDD
J7	DVDD
J9	DVDD

Pin Number	Pin Name
J11	DVDD
J13	DVDD
J15	DVDD
J17	DVDD
K7	DVDD
K9	DVDD
K11	DVDD
K13	DVDD
K15	DVDD
K17	DVDD
L7	DVDD
L9	DVDD
L11	DVDD
L13	DVDD
L15	DVDD
L17	DVDD
D11	INTn
B11	MDC[0]
A11	MDC[1]
A12	MDC[2]
B12	MDC[3]
C11	MDIO[0]
A10	MDIO[1]
A13	MDIO[2]
C12	MDIO[3]
V2	P0_ATN[0]
V3	P0_ATN[1]
V4	P0_ATN[2]
V5	P0_ATN[3]
W2	P0_ATP[0]

Pin Number	Pin Name
W3	P0_ATP[1]
W4	P0_ATP[2]
W5	P0_ATP[3]
R2	P0_AVDDL
R3	P0_AVDDL
R4	P0_AVDDL
R5	P0_AVDDL
N2	P0_AVDDH
N3	P0_AVDDH
N4	P0_AVDDH
N5	P0_AVDDH
T2	P0_AVDDT
T3	P0_AVDDT
T4	P0_AVDDT
T5	P0_AVDDT
E4	P0_AVDDR
D2	P0_AVDDS
D4	P0_AVDDS
Y3	P0_CMN
Y4	P0_CMP
L22	P0_GPIO[0]
L20	P0_GPIO[1]
H22	P0_GPIO[2]
K1	P0_LED[0]
K2	P0_LED[1]
K3	P0_LED[2]
K4	P0_LED[3]
AA2	P0_MDIN[0]
AA3	P0_MDIN[1]
AA4	P0_MDIN[2]

Pin Number	Pin Name
AA5	P0_MDIN[3]
AB2	P0_MDIP[0]
AB3	P0_MDIP[1]
AB4	P0_MDIP[2]
AB5	P0_MDIP[3]
D1	P0_SIN[0]
D3	P0_SIN[1]
C1	P0_SIP[0]
C3	P0_SIP[1]
B2	P0_SON[0]
B4	P0_SON[1]
A2	P0_SOP[0]
A4	P0_SOP[1]
E2	P0_VDDR09
F5	P0_VHV
V10	P1_ATN[0]
V9	P1_ATN[1]
V8	P1_ATN[2]
V7	P1_ATN[3]
W10	P1_ATP[0]
W9	P1_ATP[1]
W8	P1_ATP[2]
W7	P1_ATP[3]
R7	P1_AVDDL
R8	P1_AVDDL
R9	P1_AVDDL
R10	P1_AVDDL
N7	P1_AVDDH
N8	P1_AVDDH
N9	P1_AVDDH

Pin Number	Pin Name
N10	P1_AVDDH
T7	P1_AVDDT
T8	P1_AVDDT
T9	P1_AVDDT
T10	P1_AVDDT
E6	P1_AVDDR
D6	P1_AVDDS
D8	P1_AVDDS
Y9	P1_CMN
Y8	P1_CMP
M22	P1_GPIO[0]
M20	P1_GPIO[1]
H20	P1_GPIO[2]
J1	P1_LED[0]
J3	P1_LED[1]
H3	P1_LED[2]
J4	P1_LED[3]
AA10	P1_MDIN[0]
AA9	P1_MDIN[1]
AA8	P1_MDIN[2]
AA7	P1_MDIN[3]
AB10	P1_MDIP[0]
AB9	P1_MDIP[1]
AB8	P1_MDIP[2]
AB7	P1_MDIP[3]
D9	P1_SIN[0]
D7	P1_SIN[1]
C9	P1_SIP[0]
C7	P1_SIP[1]
B8	P1_SON[0]

Pin Number	Pin Name
B6	P1_SON[1]
A8	P1_SOP[0]
A6	P1_SOP[1]
E8	P1_VDDR09
F11	P1_VHV
V12	P2_ATN[0]
V13	P2_ATN[1]
V14	P2_ATN[2]
V15	P2_ATN[3]
W12	P2_ATP[0]
W13	P2_ATP[1]
W14	P2_ATP[2]
W15	P2_ATP[3]
R12	P2_AVDDL
R13	P2_AVDDL
R14	P2_AVDDL
R15	P2_AVDDL
N12	P2_AVDDH
N13	P2_AVDDH
N14	P2_AVDDH
N15	P2_AVDDH
T12	P2_AVDDT
T13	P2_AVDDT
T14	P2_AVDDT
T15	P2_AVDDT
E15	P2_AVDDR
D15	P2_AVDDS
D17	P2_AVDDS
Y13	P2_CMN
Y14	P2_CMP

Pin Number	Pin Name
N22	P2_GPIO[0]
M21	P2_GPIO[1]
J21	P2_GPIO[2]
G1	P2_LED[0]
G2	P2_LED[1]
H2	P2_LED[2]
G4	P2_LED[3]
AA12	P2_MDIN[0]
AA13	P2_MDIN[1]
AA14	P2_MDIN[2]
AA15	P2_MDIN[3]
AB12	P2_MDIP[0]
AB13	P2_MDIP[1]
AB14	P2_MDIP[2]
AB15	P2_MDIP[3]
D14	P2_SIN[0]
D16	P2_SIN[1]
C14	P2_SIP[0]
C16	P2_SIP[1]
B15	P2_SON[0]
B17	P2_SON[1]
A15	P2_SOP[0]
A17	P2_SOP[1]
E13	P2_VDDR09
F12	P2_VHV
V20	P3_ATN[0]
V19	P3_ATN[1]
V18	P3_ATN[2]
V17	P3_ATN[3]
W20	P3_ATP[0]

Pin Number	Pin Name
W19	P3_ATP[1]
W18	P3_ATP[2]
W17	P3_ATP[3]
R17	P3_AVDDL
R18	P3_AVDDL
R19	P3_AVDDL
R20	P3_AVDDL
N17	P3_AVDDH
N18	P3_AVDDH
N19	P3_AVDDH
N20	P3_AVDDH
T17	P3_AVDDT
T18	P3_AVDDT
T19	P3_AVDDT
T20	P3_AVDDT
E17	P3_AVDDR
D19	P3_AVDDS
D21	P3_AVDDS
Y19	P3_CMN
Y18	P3_CMP
P22	P3_GPIO[0]
N21	P3_GPIO[1]
K21	P3_GPIO[2]
F1	P3_LED[0]
F2	P3_LED[1]
F3	P3_LED[2]
F4	P3_LED[3]
AA20	P3_MDIN[0]
AA19	P3_MDIN[1]
AA18	P3_MDIN[2]

Pin Number	Pin Name
AA17	P3_MDIN[3]
AB20	P3_MDIP[0]
AB19	P3_MDIP[1]
AB18	P3_MDIP[2]
AB17	P3_MDIP[3]
D22	P3_SIN[0]
D20	P3_SIN[1]
C22	P3_SIP[0]
C20	P3_SIP[1]
B21	P3_SON[0]
B19	P3_SON[1]
A21	P3_SOP[0]
A19	P3_SOP[1]
E19	P3_VDDR09
F18	P3_VHV
K22	RCLK0
J22	RCLK1
G22	RESETn
F20	SHSDACN
F19	SHSDACP
E21	SIREF
K20	SPI_CLK
J20	SPI_MISO
G20	SPI_MOSI
G21	SPI_SSn
F22	STSTPT
R21	TCK
T21	TDI
U21	TDO
D12	TEST

Pin Number	Pin Name
T22	TEST_CLKN
U22	TEST_CLKP
V21	TMS
R22	TRSTn
V1	TSTCN
W1	TSTCP
H5	VDDOL
K5	VDDOL
E11	VDDOM
G19	VDDOR
J19	VDDOR
K19	VDDOT
L5	VSEL_L
E12	VSEL_M
H19	VSEL_R
L19	VSEL_T
B10	VSS
B13	VSS
F6	VSS
F8	VSS
F10	VSS
F14	VSS
F16	VSS
G3	VSS
G6	VSS
G8	VSS
G10	VSS
G12	VSS
G14	VSS
G16	VSS

Pin Number	Pin Name
G18	VSS
H6	VSS
H8	VSS
H10	VSS
H12	VSS
H14	VSS
H16	VSS
H18	VSS
H21	VSS
J2	VSS
J6	VSS
J8	VSS
J10	VSS
J12	VSS
J14	VSS
J16	VSS
J18	VSS
K6	VSS
K8	VSS
K10	VSS
K12	VSS
K14	VSS
K16	VSS
K18	VSS
L3	VSS
L6	VSS
L8	VSS
L10	VSS
L12	VSS
L14	VSS

Pin Number	Pin Name
L16	VSS
L18	VSS
L21	VSS
P21	VSS
T1	XTAL1
R1	XTAL2

3 Functional Description

This section describes the chip-level functionality.

3.1 Buffering

Packets may flow through some buffering. Buffering will occur for a variety of all the reasons described in this section.

3.1.1 EEE Buffering

EEE PHY functionality to operate correctly, an EEE-compliant MAC is required to control the PHY as when to enter and exit the low power idle (LPI) state and buffer packets to allow the PHY adequate time to exit the low power idle state. The PHY should beset to transparent (slave) EEE mode when operating with an EEE-compliant MAC (register 1.C033.0 = 0).

The device is able to support non-EEE compliant MACs by enabling the internal EEE buffering by setting register 1.C033.0 to 1. EEE buffering is automatically disabled when the device or its link partner is not capable of EEE operation.

When the EEE buffer is empty for the amount of time specified by registers 1.C033.15:8, 31.F004.7:0, 31.F004.15:8 for 10 Gbps, 1000 Mbps, and 100 Mbps speeds, respectively (in units of 1 microsecond), the buffer will indicate to the PHY that it wishes to enter the LPI state.

When the EEE buffer is not empty it will indicate to the PHY that it must exit the LPI state. The EEE buffer ensures that no packets are lost by the PHY during the transition from LPI state to normal mode of operation. When the media interface exits the LPI state, the data in the buffer is then released and transmitted to the line. The amount of time the packet is held in the buffer prior to release can be programmed via registers 31.F005.15:8, 31.F006.7:0, and 31.F006.15:8 for 10 Gbps, 1000 Mbps, and 100 Mbps speeds, respectively. The unit is in microseconds. The minimum IPG between packets as set in 31.F005.7:0 will be used to separate packets until the EEE buffer is fully drained.

3.2 Link Interrupt

When the MACs are not bypassed, all local and remote faults received on the line or host will be terminated by the MAC. For example, if a local fault is received on the line, then the MAC terminates the local fault and never passes it upstream to the host. The MAC will transmit a remote fault back to the line.

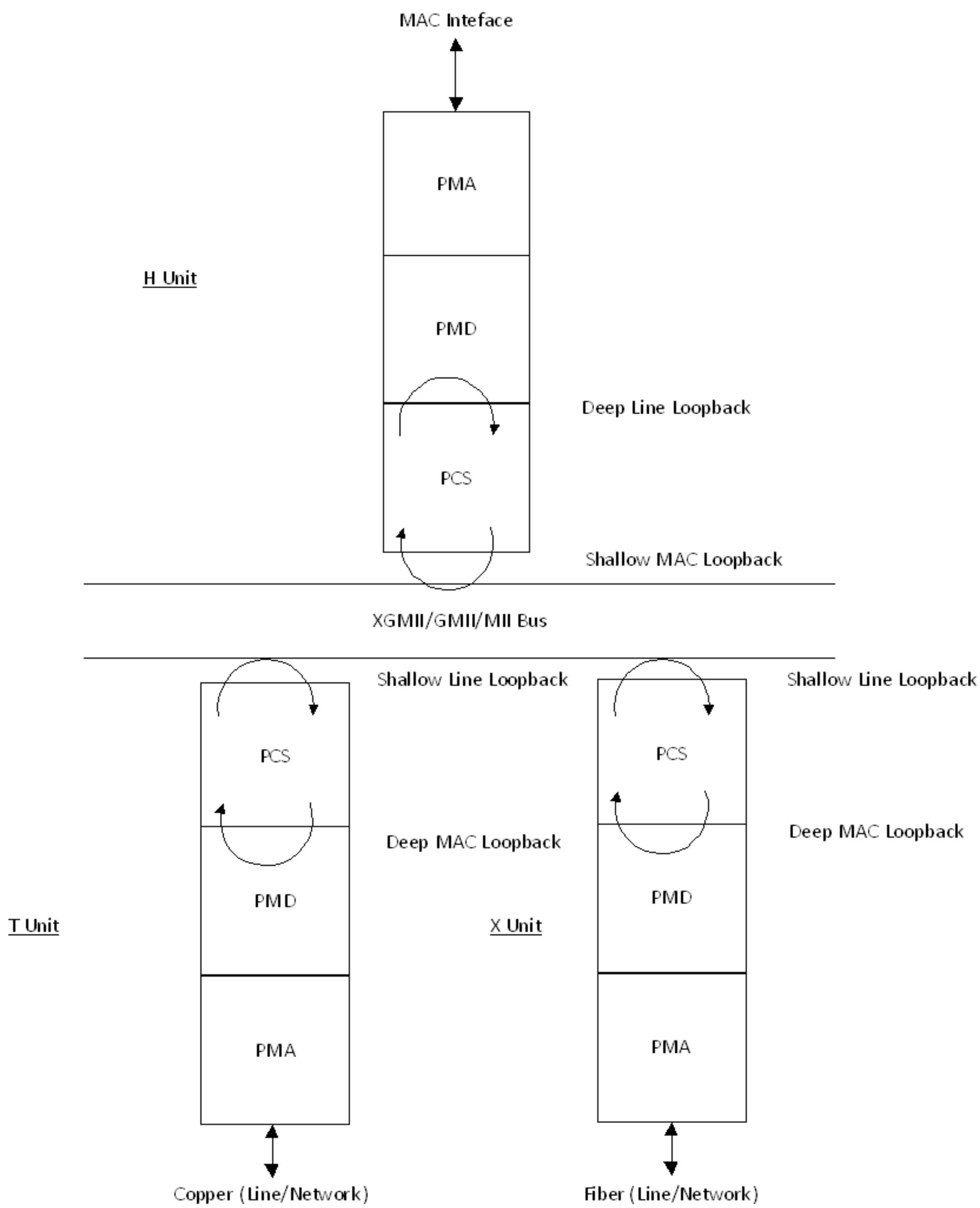
3.3 Loopback

The T, X, and H Units has the ability to perform MAC loopback and line loopback as shown in Figure 5. Each unit can only be in MAC loopback or line loopback at any given time. If MAC loopback is engaged, then loopback speed depends upon the media link speed. If the media link is down, then the MAC interface speed is dependent upon the setting in 31.F000.7:6, Default MAC Interface Speed. A deep line loopback must not be enabled at the same time as a MAC loopback or a closed internal bus loop will be created.

Table 15: Loopback Control

Loopback Point	Register	Function	Setting
A	3.0000.14	T Unit Deep MAC Loopback	1 = Loopback 0 = Normal operation
B	3.1000.14 3.2000.14	X Unit Deep MAC Loopback	1 = Loopback 0 = Normal operation
C	4.0000.14 4.1000.14 4.2000.14	H Unit Deep Line Loopback	1 = Loopback 0 = Normal operation
D	3.8002.5	T Unit Shallow Line Loopback for 1000/100/10 mode	1 = Enable Line Loopback 0 = Normal operation
E	1.C000.11	T Unit Shallow Line Loopback for 5G/2.5G mode	1 = Enable Line Loopback 0 = Normal operation
F	3.F003.12	X Unit Shallow Line Loopback	1 = Enable Line Loopback 0 = Normal operation
G	4.F003.12	H Unit Shallow MAC Loopback	1 = Enable Line Loopback 0 = Normal operation
–	31.F000.7:6	Default MAC Interface Speed	This is the MAC Interface Speed during Link down. 00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps 11 = 10 Gbps
–	31.F0A8.1:0	Device Max Speed Limit Control	This controls the link down max speed. 00 = 10 Gbps 10 = 5 Gbps 11 = 2.5 Gbps Port soft reset should be followed.

Figure 5: Loopback Paths



3.3.1 MAC Loopback

MAC loopback is defined as taking data from the MAC interface and transmitting that data back towards the MAC interface. For the loopback to occur, the unit must have control of the XGMII bus that it is outputting on, that is, that unit must have control of the data path.

If the link is down, then the loopback speed will be determined by register 31.F000.7:6 and 31.F0A8.1:0. Only host shallow MAC loopback is supported when the media link is down.

3.3.2 Line Loopback

Line loopback is defined to be looping the data that is received on the network interface and transmitting that data back onto the network interface.

The speed of the loopback is determined by the active link speed.

3.4 Configuration and Resets

The device can be configured in the following ways:

- Hardware configuration strap options
- MDC/MDIO register access

All hardware configuration options can be overwritten via the other methods except PHYADR and MDIO.

This section will discuss the hardware configuration.

3.4.1 Hardware and Software Resets

RESETn is the hardware reset pin for the entire chip. To ensure that the stopping of the hardware configuration is correct, it is required that upon system power-up, a reset signal be applied to RESETn or the RESETn pin be held low until all the power rails are settled down.

In addition to the hardware reset pin (RESETn), there are several software reset bits that reset various parts of the chip.

- A hardware reset will reset the entire chip and initialize all the registers to their hardware reset default.
- A software reset has a similar effect on the affected units as a hardware reset except all Retain-type of will hold their value, and the Update-type registers will have the previously written values take effect.

Register 31.F001.14 is a software bit that emulates the hardware reset. Setting the bit to 1 will reset the entire chip (all ports) as if the RESETn pin is asserted. All ports have register 31.F001.14; however, special care should be taken when selecting the specific port number to achieve entire chip reset. The applicable register in Port 3 (88E2040L) and Port 0 (88E2010) should be programmed. When triggered, registers are not accessible through the MDIO until the chip reset completes.

Setting register 31.F001.15 to 1 software resets the entire port except for the T Unit. The T Unit will briefly power down and Auto-Negotiation will restart.

Setting registers 31.F001.13, 1.0000.15, 3.0000.15, or 7.0000.15 to 1 software resets the T Unit only.

Setting registers 4.0000.15, 4.1000.15, or 4.2000.15 to 1 software resets the H Unit only.

3.4.2 Hardware Configuration

After the deassertion of RESETn the device will be hardware configured through the CONFIG[7:0] pins. Each pin is used to configure 3 bits. The 3-bit value is set depending on which LED pin or static level is connected to the CONFIG pins at the deassertion of hardware reset.

The three configuration bits per pin mapping for the 88E2010 device is shown in Table 16.

The three bit mapping for the 88E2010 device during hardware configuration is shown in Table 17.

Table 16: 88E2010 Device Configuration Mapping

Pin Test	Bit 2	Bit 1	Bit 2
CONFIG[0]	PHYAD[4]	PHYAD[3]	PHYAD[2]
CONFIG[1]	ANEG_MS	PHYAD[1]	PDSTATE
CONFIG[2]	ANEG_SPD[2]	ANEG_SPD[1]	ANEG_SPD[0]
CONFIG[3]	MACTYPE[2]	MACTYPE[1]	MACTYPE[0]
CONFIG[4]	MEDIATYPE[2]	MEDIATYPE[1]	MEDIATYPE[0]
CONFIG[5]	SPI_CONFIG	RESERVED	RESERVED
CONFIG[7]	FACTORY_TEST	RESERVED	RESERVED

Table 17: 88E2010 Three Bit Mapping

Pin	Bit 2
VSS	000
LED[0]	001
LED[1]	010
LED[2]	011
LED[3]	100
Reserved	101
Reserved	110
VDDO	111

The three configuration bits per pin mapping for the 88E2040L device is shown in Table 18.

The three bit mapping for the 88E2040L device during hardware configuration is shown in Table 19.

Table 18: 88E2040L Device Configuration Mapping

Pin	Bit 2	Bit 1	Bit 0
CONFIG[0]	PHYAD[4]	PHYAD[3]	PHYAD[2]
CONFIG[1]	ANEG_MS	RESERVED	PDSTATE
CONFIG[2]	ANEG_SPD[2]	ANEG_SPD[1]	ANEG_SPD[0]
CONFIG[3]	MACTYPE[2]	MACTYPE[1]	MACTYPE[0]
CONFIG[4]	MEDIATYPE[2]	MEDIATYPE[1]	MEDIATYPE[0]
CONFIG[5]	SPI_CONFIG	RESERVED	RESERVED
CONFIG[7]	FACTORY_TEST	MDIO[1]	MDIO[0]

Table 19: 88E2040L Device Three Bit Mapping

Pin	Bit 2:0
VSS	000
P3_LED[0]	001
P3_LED[1]	010
P2_LED[0]	011
P2_LED[1]	100
P1_LED[0]	101
P1_LED[1]	110
VDDO	111

The configuration bit definition is shown in Table 20.

Table 20: Configuration Bit Definition

Bits	Definition	Description
PHYAD[4:0]	PHY Address	88E2040L PHYAD[1:0] is hardcoded as a function of REV_ PHYAD.
REV_PHYAD	88E2040L - Reverse PHYAD[1:0] order 88E2010 - N/A	88E2040L PHYAD[1:0] corresponds to the following: 0 = 00 - Port 0 01 - Port 1 10 - Port 2 11 - Port 3 1 = 00 - Port 3 01 - Port 2 10 - Port 1 11 - Port 0
MDIO[1:0] (88E2040L)	This determines whether the four ports are accessed from a 1 MDIO, 2 ports per MDIO, or 1 MDIO per port. 00 = MDC[2]/MDIO[2] Access on all four ports 01 = MDC[1]/MDIO[1] Accesses Port 0 and Port 1 MDC[2]/MDIO[2] Accesses Port 2 and Port 3 10 = MDC[0]/MDIO[0] Accesses Port 0 MDC[1]/MDIO[1] Accesses Port 1 MDC[2]/MDIO[2] Accesses Port 2 MDC[3]/MDIO[3] Accesses Port 3 11 = Reserved	None

Table 20: Configuration Bit Definition (Continued)

Bits	Definition	Description
MACTYPE[2:0] (88E2040L)	000 = Reserved 001 = Reserved 010 = Reserved 011 = Reserved 100 = 5GBASE-R/2500BASE-X/SGMII Auto-Negotiation On 101 = 5GBASE-R/2500BASE-X/SGMII Auto-Negotiation Off 110 = Reserved 111 = Reserved	C Unit Host interface mode for 88E2040L
MACTYPE[2:0] (88E2010)	000 = Reserved 001 = Reserved 010 = Reserved 011 = 5GBASE-R/2500BASE-X/SGMII Auto-Negotiation On 100 = 5GBASE-R/2500BASE-X/SGMII Auto-Negotiation On 101 = 5GBASE-R/2500BASE-X/SGMII SGMII Auto-Negotiation Off 110 = Reserved 111 = Reserved	C Unit Host interface mode for 88E2010
MEDIATYPE[2:0]	000 = Copper Only 001-111 = RESERVED	C Unit Line-side interface
PDSTATE	0 = Start In Power Up State 1 = Start In Power Down State	T Unit Copper power down state
ANEG_MS	0 = Prefer Slave 1 = Prefer Master	T Unit Master and slave configuration
FACTORY_TEST	Factory Test Mode 0 = Normal mode (default) 1 = Test Mode (reserved for Marvell)	None
ANEG_SPD[2:0]	This sets the default for speed advertisement during Auto-Negotiation. 000 = Reserved 001 = 5G, 2.5G, 1000 Mbps Full 010 = 5G, 2.5G, 1000 Mbps Full, 100 Mbps Full 011 = 5G, 2.5G, 1000 Mbps Full, 100 Mbps Full, 10 Mbps Full 100 = 5G, 2.5G, 1000 Mbps Full, 100 Mbps Full/Half 101 = 5G, 2.5G, 1000 Mbps Full, 100 Mbps Full/Half, 10 Mbps Full/Half 110 = 5G, 2.5G, 1000 Mbps Full/Half, 100 Mbps Full/Half 111 = 5G, 2.5G, 1000 Mbps Full/Half, 100 Mbps Full/Half, 10 Mbps Full/Half	–

Table 20: Configuration Bit Definition (Continued)

Bits	Definition	Description
SPI_CONFIG	–	C Unit 31.F008.5 <= SPI_CONFIG This determines whether the embedded processor loads the firmware image from flash or waits for the image to be downloaded via MDIO. 0 = Download code via SPI. 1 = Wait for download via MDIO. To override this configuration, change 31.F008.5 and then perform a T Unit hardware reset using 31.F001.12.

3.4.3 Reference Clock Selection

CLK_SEL[1:0] selects which the type and speed of the reference clock input as shown in Table 21. CLK_SEL must be stable and the selected clock toggling prior to de-assertion of RESETn. CLK_SEL must not change value for the duration of device operation.

Table 21: CLK_SEL[1:0] Selection

CLK_SEL[1:0]	XTAL1/XTAL2	CLKP/CLKN
00	50 MHz	Floating
01	GND	50 MHz
10	GND	156.25 MHz
11	Reserved	Reserved

Note

50 MHz crystal operation is only supported for commercial-grade devices.

3.5 MDC/MDIO Register Access

The management interface provides access to the internal registers via the MDC and MDIO pins and is compliant with IEEE 802.3 Clause 45. MDC is the management data clock input and it can run from DC to a maximum continuous rate of 12.5 MHz. At high MDIO fanouts, the maximum rate may be decreased depending on the output loading. MDIO is the management data input/output and is a bi-directional signal that runs synchronously to MDC.

The MDIO does not require a pull-up resistor. If another open-drain device driving MDIO requires a pull-up resistor, then it should drive or be pulled up to the same voltage value as the VDDOM rail.

The PHY address is configured during the hardware reset sequence. Refer to Section 3.4, Configuration and Resets, on page 65 for information on how to configure PHY addresses.

Typical read and write operations on the management interface are shown in Figure 6 and Figure 7. The MDIO interface supports preamble suppression operation by default. Between subsequence MDIO access sequences, there must be at least 1 IDLE MDC cycle (MDIO driven high). So the minimum MDC clock cycle for a MDIO operation will 33 cycles. The start of a MDIO operation is marked by the insertion of two MDC cycle with MDIO driven to zero as this will mark the start of frame (ST) pattern as defined in IEEE 802.3 standard. All the required serial management registers are implemented as well as several optional registers. A description of the registers can be found in the register description.

Figure 6: Typical MDC/MDIO Read Operation

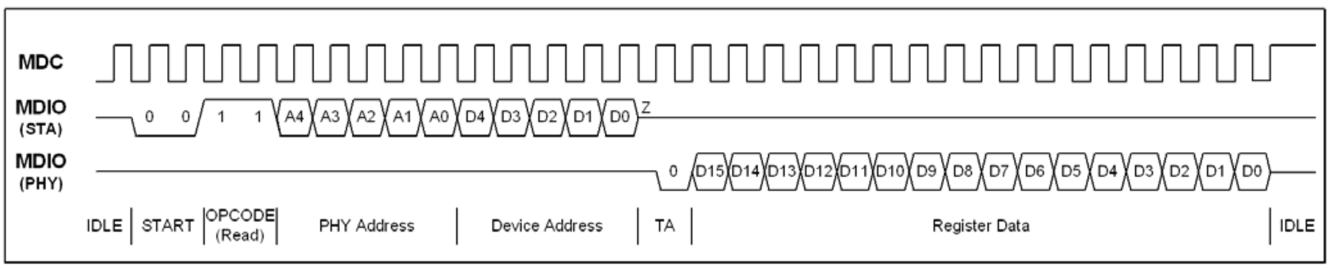
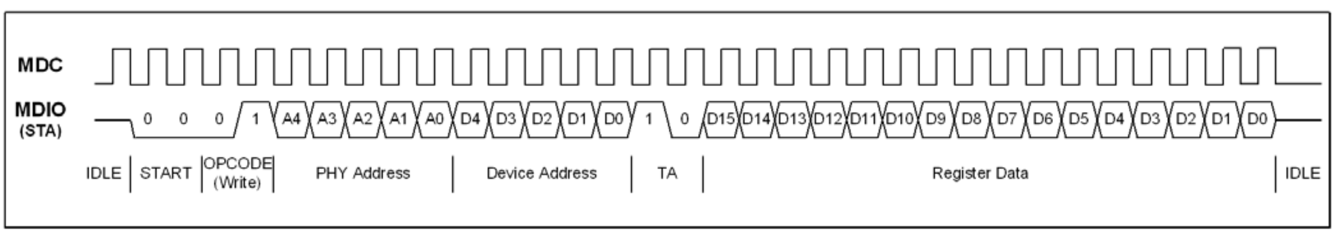


Figure 7: Typical MDC/MDIO Write Operation



3.5.1 Clause 45 MDIO Framing

The extensions for Clause 45 MDIO indirect register accesses are specified in Table 22.

Table 22: Extensions for Management Frame Format for Indirect Access

Frame	PRE	ST	OP	PHYAD	DEVADR	TA	ADDRESS/DATA	Idle
Address	1...1	00	00	PPPPP	DDDDD	10	AAAAAAAAAAAAAAAA	Z
Write	1...1	00	01	PPPPP	DDDDD	10	DDDDDDDDDDDDDDDD	Z
Read	1...1	00	11	PPPPP	DDDDD	Z0	DDDDDDDDDDDDDDDD	Z
Read Increment	1...1	00	10	PPPPP	DDDDD	Z0	DDDDDDDDDDDDDDDD	Z

The MDIO implements a 16-bit address register that stores the address of the register to be accessed. For an address cycle, it contains the address of the register to be accessed on the next cycle. For read, write, post-read-increment-address cycles, the field contains the data for the register. At power up and reset, the contents of the register are undefined.

Write, read, and post-read-increment-address frames access the address register, though write and read frames do not modify the contents of the address register.

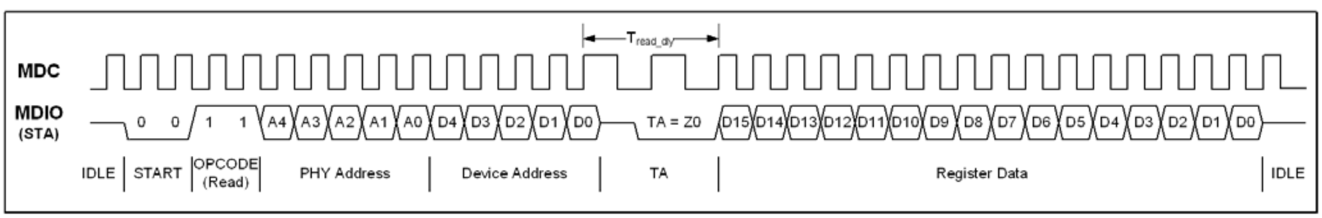
3.5.2 30 MHz High-Speed MDC/MDIO Management Interface Protocol

In addition to supporting the typical MDC/MDIO protocol, the device has the capability to run MDC down to a clock period of 35 ns. The write operation can operate normally at this speed; however, for the read operation, the MDC clock cycle must be slowed down for the TA period as shown in the Figure 8.

During read operations, the MDC clock must slow down so that the PHY has sufficient time to retrieve the data.

See Section 6.4.4, MDC/MDIO Management Interface Timing, on page 123 for timing details.

Figure 8: 30 MHz MDC/MDIO Read Operation



3.5.3 Independent MDC/MDIO Support

The 88E2040L device can be configured to operate with 1, 2, or 4 MDC/MDIO interfaces by setting the MDIO[1:0] configuration bits during hardware reset. The behavior is shown in Table 23.

Table 23: 88E2040L Device MDC/MDIO Interface Mapping

MDIO[1:0] Configuration Bit	00	01	10
MDC[0]/MDIO[0]	Pull-low/Do not connect	Pull-low/Do not connect	Port 0 MDC/MDIO
MDC[1]/MDIO[1]	Pull-low/Do not connect	Port 0, 1 MDC/MDIO	Port 1 MDC/MDIO
MDC[2]/MDIO[2]	Port 0, 1, 2, 3 MDC/MDIO	Port 2, 3 MDC/MDIO	Port 2 MDC/MDIO
MDC[3]/MDIO[3]	Pull-low/Do not connect	Pull-low/Do not connect	Port 3 MDC/MDIO

Note

Ensure that unused MDC is pulled low and MDIO be left unconnected.

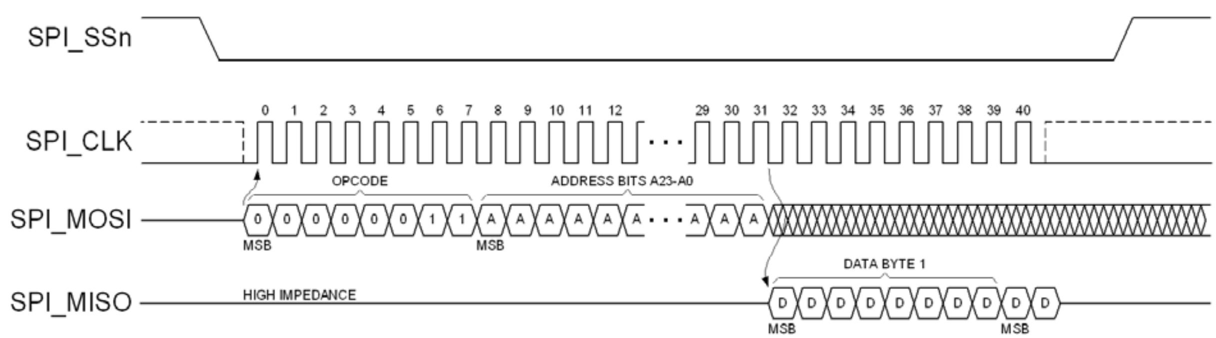
3.6 Firmware Loading

3.6.1 Flash Memory Interface

The device can download code from an external flash memory via the Serial Peripheral Interface bus (SPI) into the processor memory. The SPI bus is a 4-wire serial communications interface used by many microprocessor peripheral chips. When the hardware configuration SPI_CONFIG strap bit is set to 0, the device will download code after the de-assertion of RESETn.

The SPI controller will issue a read array command starting from address 0x000000 as shown in Figure 9. The number of bytes read will be determined by the values contained in the flash image header.

Figure 9: SPI Read Array



The device is always the master and the flash is the slave. Chip select (output SPI_SSn) is driven low by the device during every flash access.

3.6.2 Firmware Download to RAM

As an alternative to using a flash device for storing the firmware image, the image may be downloaded directly to the microcontroller RAM by the host using the Serial Management Interface (MDC/MDIO). In this case, the SPI_CONFIG strap bit must be set to 1 and the device will wait for the firmware to be downloaded to RAM. Refer to the 88E2010/88E2040L Software API package for instructions on downloading firmware to RAM via Serial Management Interface.

3.7 Power Management

This section discusses the general power down for the device. See the unit level sections for details on advanced power management of each unit.

3.7.1 Manual Power Down

The device will automatically power down unused circuits without the need for the user to intervene. The following registers can be set to force the units to power down.

Setting register 31.F001.11 to 1 powers down the entire port. Care should be used when setting this bit. When this bit is set to 1, there is no way to clear this bit via processor instructions. Clear this bit through a hardware reset or via an MDC/MDIO write.

Setting registers 1.0000.11 or 3.0000.11 to 1 powers down the T Unit only.

Setting registers 4.0000.11, 4.1000.11, or 4.2000.11 to 1 powers down the H Unit only.

3.7.2 MAC Interface Power Down

Register 31.F000.3 controls whether the H Unit is powered down while the link is down.

0 = Power down when the link is down.

1 = Always keep the H Unit powered up.

3.7.3 Controlling and Sensing

Register 31.F013 controls whether LED[3:0] pins are inputs or outputs. Each pin can be individually controlled.

Register 31.F012 allows the pins to be controlled and sensed. When configured as input, a read to register 31.F012 will return the real-time sampled state of the pin at the time of the read. A write will write the output register, but it have no immediate effect on the pin since the pin is configured to be an input. The input is sampled once every 38.4 ns.

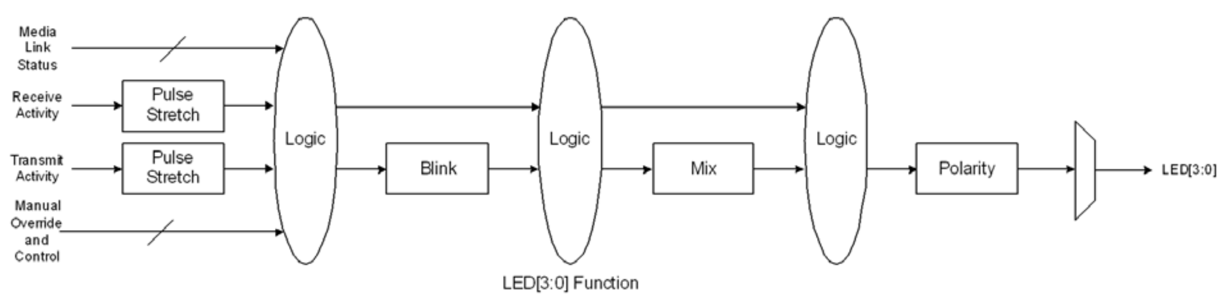
When configured as output, a read to register 31.F012 will return the value in the output register. A write will write the output register which will in turn drive the state of the pin.

3.8 LED

The LED[3:0] pins can be used to drive LED pins. Registers 31.F020 through 31.F027 control the operation of the LED pins. LED[3:0] are used to configure the PHY per Section 3.4.2.

Figure 10 shows the general chaining of function for the LEDs. The various functions are described in the following sections.

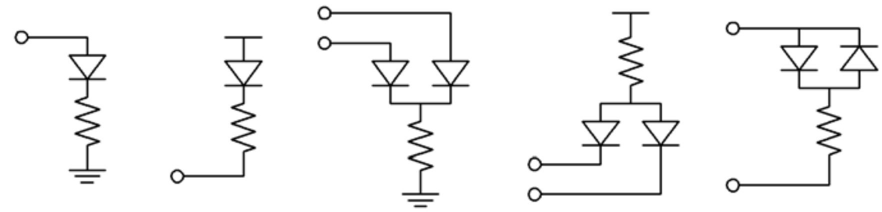
Figure 10: LED Chain



3.8.1 LED Polarity

There are a variety of ways to hook up the LEDs. Some examples are shown in Figure 11. Registers 31.F023.1:0, 31.F022.1:0, 31.F021.1:0, and 31.F020.1:0 specify the output polarity for the LED[3:0] function to accommodate a variety of installation options. The lower bit of each pair specified the on (active) state of the LED, either high or low. The upper bit of each pair specifies whether the off state of the LED should be driven to the opposite level of the on state or Hi-Z. The Hi-Z state is useful in cases such the LOS and INIT function where the inactive state is Hi-Z.

Figure 11: Various LED Hookup Configurations



3.8.2 Pulse Stretching and Blinking

Register 31.F027.14:12 specifies the pulse stretching duration of a particular activity. Only the transmit activity, receive activity, collision activity, and (transmit or receive) activity are stretched. All other statuses are not stretched since they are static in nature and no stretching is required.

Some status will require blinking state instead of a solid on state. Registers 31.F027.10:8 and 31.F027.6:4 specify the two blink rates. The pulse stretching is applied first and the blinking will reflect the duration of the stretched pulse.

Registers 31.F020.2, 31.F021.2, 31.F022.2, and 31.F023.2 select which of the two blink rates to use for LED[0] to LED[3], respectively.

- 0 = Select Blink Rate 1.
- 1 = Select Blink Rate 2.

The stretched or blinked output will be mixed if needed (see Section 3.8.3) and then inverted/Hi-Z according to the polarity described in Section 3.8.1.

3.8.3 Bi-Color LED Mixing

In the dual LED modes, the mixing function allows the 2 colors of the LED to be mixed to form a third color. This is useful since the PHY supports 10/100 Mbps, 1G, and 5G/2.5G operation speeds. Register 31.F026.7:4 controls the amount to mix in the LED[3], and LED[1] pins. Register 31.F026.3:0 controls the amount to mix in the LED[2] and LED[0] pins. Mixing is determined by the percentage of time the LED is on during the active state. The percentage is selectable in 12.5% increments.

There are two classes of bi-color LEDs: three-terminal type and two-terminal type. For example, the third and fourth LED block from the left in Figure 11 illustrates three-terminal types and the block on the far right is the two-terminal type. In the three-terminal type, both of the LEDs can be turned on at the same time. So the sum of the percentage specified by 31.F026.7:4 and 31.F026.3:0 can exceed 100%. However, in the two-terminal type, the sum should never exceed 100% since only one LED can be turned on at any given time.

Mixing only applies when register 31.F020.12:8 or 31.F022.12:8 are set to 11xxx. There is no mixing in single LED modes.

The behavior for the various dual LED modes are described in Table 24.

Table 24: Dual LED Mode Behavior

Dual Mode Description	Blink Mix		Solid Mix		Speed Type 1		Speed Type1		Speed Type 2		Speed Type 2	
31.F020, 31.F022, bits 12:8	11010		11011		11100		11101		11110		11111	
Current State	LED3 LED1	LED2 LED0	LED3 LED1	LED2 LED0	LED3 LED1	LED2 LED0	LED3 LED1	LED2 LED0	LED3 LED1	LED2 LED0	LED3 LED1	LED2 LED0
5/2.5 Gbps	Blink Mix	Blink Mix	Solid Mix	Solid Mix	Solid	Off	Solid	Off	Solid	Off	Solid	Off
1 Gbps	Blink Mix	Blink Mix	Solid Mix	Solid Mix	Solid Mix	Solid Mix	Solid Mix	Solid Mix	Off	Solid	Off	Solid
100 Mbps Link	Blink Mix	Blink Mix	Solid Mix	Solid Mix	Off	Solid	Off	Solid	Solid Mix	Solid Mix	Solid Mix	Solid Mix
10 Mbps Link	Blink Mix	Blink Mix	Solid Mix	Solid Mix	Off	Off	Off	Off	Off	Off	Off	Off
Link Down	Blink Mix	Blink Mix	Solid Mix	Solid Mix	Off	Off	Off	Off	Off	Off	Off	Off

3.8.4 Modes of Operation

The LED pins relay various statuses of the PHY so that they can be displayed by the LEDs.

The basic statuses are shown in Table 25. The compound statuses are formed with the basic status plus the speed information as shown in Table 26. The status information is generated by the copper (T Unit) interfaces.

Table 25: Basic LED Status

Status	Copper
Transmit	Copper Transmit
Receive	Copper Receive
Link	Copper Link
Full Duplex	Copper Duplex
Master	Master/Slave

Table 26: Compound LED Status

Compound Status	Copper
Transmit or Receive	Copper Transmit or Copper Receive
Collision (Transmit and Receive)	Copper Transmit and Copper Receive and Copper Half Duplex
10 Mbps Link	Copper Speed = 10 Mbps and Copper Link
100 Mbps Link	Copper Speed = 100 Mbps and Copper Link

Table 26: Compound LED Status (Continued)

Compound Status	Copper
1 Gbps Link	Copper Speed = 1 Gbps and Copper Link
5/2.5 Gbps Link	Copper Speed = 5/2.5 Gbps and Copper Link
Link	Copper Link
Half Duplex	Not Copper Full Duplex
Slave	Not Master
10 Mbps Link or 100 Mbps Link	Copper 10 Mbps Link or Copper 100 Mbps Link
10 Mbps Link or 100 Mbps Link or 1 Gbps Link	Copper 10 Mbps Link or Copper 100 Mbps Link or Copper 1 Gbps Link
100 Mbps Link or 5/2.5 Gbps Link	Copper 100 Mbps or Copper 5/2.5 Gbps Link
1 Gbps or 5/2.5 Gbps Link	Copper 1 Gbps or Copper 5/2.5 Gbps Link

The status that the LED displays is defined by registers 31.F020 to 31.F023 as shown in Table 25 and Table 26. For each LED if the condition selected by bits 12:8 is true the LED will blink. If the condition selected by bits 7:3 is true, then the LED will be solid on. If both selected conditions are true, then the blink will take precedence.

3.8.5 Speed Blink

When 31.F020.7:3 is set to 11111, the LED[0] pin assumes the following behavior:

- LED[0] outputs the sequence shown in Table 27 depending on the status of the link. The sequence consists of 10 segments.
- For a 10 Gbps link, 4 pulses are output.
- For a 1000 Mbps link, 3 pulses are output.
- For a 100 Mbps link, 2 pulses are output.
- For a 10 Mbps link, 1 pulse is output.
- No link outputs 0 pulses.
- The sequence repeats indefinitely.
- The odd-numbered segment pulse duration is specified in 31.F027.1:0. The even-numbered segment pulse duration is specified in 31.F027.3:2.

Table 27: Speed Blinking Sequence

Segment	10 Mbps	100 Mbps	1 Gbps	10 Gbps	No Link	Duration
1	On	On	On	On	Off	31.F027.3:2
2	Off	Off	Off	Off	Off	31.F027.1:0
3	Off	On	On	On	Off	31.F027.3:2
4	Off	Off	Off	Off	Off	31.F027.1:0
5	Off	Off	On	On	Off	31.F027.3:2
6	Off	Off	Off	Off	Off	31.F027.1:0
7	Off	Off	Off	On	Off	31.F027.3:2
8	Off	Off	Off	Off	Off	31.F027.1:0
9	Off	Off	Off	Off	Off	31.F027.3:2

Table 27: Speed Blinking Sequence (Continued)

Segment	10 Mbps	100 Mbps	1 Gbps	10 Gbps	No Link	Duration
10	Off	Off	Off	Off	Off	31.F027.1:0

3.8.6 Combo LED Modes

Combo LED mode is activated when register 31.F024.15 is set to 1.

3.8.6.1 Combo LED Mode Select

There are five Combo LED modes which are set by 31.F024.14:12 as described in Table 28.

Table 28: Combo LED Modes

Combo LED Mode	Function					
Combo LED Mode 1 (31.F02414:12 = 000)	**Link Down**	**Link up and no activity**		**Link up and activity**		**Faulty link (including crc error, alignment, runt and jabber errors)**
LED0	Off	Solid green		Flashing green (rate determined by number of packets)		When TIMER_A is high, LED0 is on and green LED1 is off; when TIMER_A is low, LED0 is off, LED1 is on and amber.
LED1	Off	Off		Off		Default = TIMER_A on for 0.5s off for 0.5s
Combo LED Mode 2 (31.F02414:12 = 001)	**CRC Error**	**Alignment**		**Runt**		**Jabber**
LED0	LED0 is green when TIMER_B is high, default = LED0 high for 168 ms, LED1 low for 168 ms.					
LED1	LED1 amber is on when TIMER_B is low.					
Combo LED Mode 3 (31.F02414:12 = 010)	**STP[a] blocked/disabled**					
LED0	Off					
LED1	On (solid amber)					
Combo LED Mode 4 (31.F02414:12 = 011)	STP is blocked, but is it still receiving/sending data.					
LED0	Off					
LED1	On/Off as per TIMER_D (flashing amber), default = 41 ms on and 41 ms off					
Combo LED Mode 5 (31.F02414:12 = 100)	**10 Mbps**	**100 Mbps**	**1000 Mbps**	**2.5G**	**5G**	

Table 28: Combo LED Modes (Continued)

Combo LED Mode	Function					
LED0	Off	On	On 5% (105 ms) Off 95% (1895 ms) Rate = TIMER_1G	On 10% (210 ms) Off 90% (1790 ms) Rate = TIMER_ 2.5G	On 20% (420 ms) Off 80% (1580 ms) Rate = TIMER_5G	
LED1	Off	Off	Off	Off	Off	

a. Spanning Tree Protocol

Table 29: Combo Mode Timer Control

Mode	Rate	Setting
1	When the link is up, the flashing rate is based on the number of frames received within 2 ms.	Refer to Table 30 for flashing rate setup.
1	Faulty Link	TIMER_A = 31.F024.7:0
2	CRC, alignment, Runt, and Jabber Errors	TIMER_B = 31.F029.15:8
4	STP is blocked, but it still receiving/sending data.	TIMER_D = 31.F039.7:0
5	1G	TIMER_1G = 31.F028.7:0
	2.5G	TIMER_2.5G = 31.F028.15:8
	5G	TIMER_5G = 31.F029.7:0

3.8.6.2 LED Activity Control

When the Combo LED Mode Selection bits (31.F024.14:12) are set to 000 and the link is up, the flash/blink activity of LED0 indicates the number of frames received within the last 2.1 seconds. Activity flashing of the LED is based on the transmitted and received frames on a link. Register 31.F026.11:10 is used to monitor transmit (31.F026.11:10 = 00) or receive (31.F026.11:10 = 01) or both (31.F026.11:10 = 11) at the same time.

LED0 can flash in two different ways:

- When Combo LED flash bit is set to 0, the more packets received within the previous 2100 ms, the longer LED0 stays on.
- When Combo LED flash bit is set to 1, the more packets received within the previous 2100 ms, the faster LED0 blinks.

The Combo LED flash rate details are listed in Table 30.

Table 30: Combo LED Flash Mode

Combo LED Flash (31.F024.11)	Flash Rate
0	<10: on for 31.F030[7:0], the remaining of 2.1s off; $<10^2$: on for 31.F030[15:8], the remaining of 2.1s off; $<5*10^2$: on for 31.F031[7:0], the remaining of 2.1s off; $<10^3$: on for 31.F031[15:8], the remaining of 2.1s off; $<5*10^3$: on for 31.F032[7:0], the remaining of 2.1s off; $<10^4$: on for 31.F032[15:8], the remaining of 2.1s off; $<5*10^4$: on for 31.F033[7:0], the remaining of 2.1s off; $<10^5$: on for 31.F033[15:8], the remaining of 2.1s off; $<5*10^5$: on for 31.F034[7:0], the remaining of 2.1s off; $<10^6$: on for 31.F034[15:8], the remaining of 2.1s off; $<5*10^6$: on for 31.F035[7:0], the remaining of 2.1s off; $<10^7$: on for 31.F035[15:8], the remaining of 2.1s off **NOTE:** For registers 31.F030, 31.F031, 31.F032, 31.F033, 31.F034, and 31.F035, the unit of bit[7:0] and [15:8] is 21 ms. Any value greater than 8'd100 will be ignored.
1	<10: LED on/off every 1/2 of 2.1s; $<10^2$: LED on/off every 1/4 of 2.1s; $<5*10^2$: LED on/off every 1/8 of 2.1s; $<10^3$: LED on/off every 1/16 of 2.1s; $<5*10^3$: LED on/off 1/32 of 2.1s; $<10^4$: LED on/off 1/64 of 2.1s; $<5*10^4$: LED on/off 1/128 of 2.1s; $<10^5$: LED on/off 1/256 of 2.1s; $<5*10^5$: LED on/off 1/512 of 2.1s; $<10^6$: LED on/off 1/1024 of 2.1s; $<5*10^6$: LED on/off 1/2048 of 2.1s; $<10^7$: LED on/off 1/4096 of 2.1s

For example:

When the number of frames received within 2.1 seconds is 4000, in the following 2.1 seconds, the LED will behave as follows:

- If 31.F024.11 = 0, then LED0 will be on for 31.F031[7:0] * 21 ms, and off for (100 - 31.F031[7:0]) * 21 ms.
- If 31.F024.11 = 1, then LED0 will on for 1/32 * 2100 ms and off for 1/32 * 2100 ms repeatedly for 2.1 seconds.

3.9 Interrupt

The T, H, and P Units and the GPIO function can generate interrupts.

The Unit Interrupt Status Register (see 31.F040) shows a summary of which unit is requesting the interrupt.

Each bit of the Unit Interrupt Status Register will be masked with the Unit Interrupt Mask Register (see 31.F043) respectively, and each masked output is ORed to form the aggregated unit interrupt.

The Port Interrupt Status (see 31.F042.0) is the result of logical OR of the aggregated unit interrupt request along with register 31.F041.0 (see Force Interrupt bit) to form the port interrupt. When the bit is 1, the INTn will be driven as an active interrupt exists. The INTn's polarity is controlled by 31.F041.2:0.

In case of multiple port devices such as 88E2040L, INTn is active when one or more ports have the active Port Interrupt. There is no aggregated interrupt register for all ports. So, the Port Interrupt bit (see 31.F042.0) for all ports should be examined to determine which port or how many ports have pending interrupt requests.

The Interrupt Polarity bits (see 31.F041.2:1) for the INTn pin are valid only from Port 0. Other port's Polarity control bit are not valid; however, setting register 31.F041.0 in any port will force the INTn pin as active.

3.10 IEEE 1149.1 and 1149.6 Controller

The IEEE 1149.1 standard defines a test access port and boundary-scan architecture for digital integrated circuits and for the digital portions of mixed analog/digital integrated circuits. The IEEE 1149.6 standard defines a test access port and boundary-scan architecture for AC-coupled signals.

This standard provides a solution for testing assembled printed circuit boards and other products based on highly complex digital integrated circuits and high-density surface-mounting assembly techniques.

The device implements the instructions shown in Table 31. Upon reset, ID_CODE instruction is selected. The PROG_HYST is a proprietary command used to adjust the test receiver hysteresis threshold. The instruction opcodes are shown in Table 31.

Table 32 and Table 34 list the 88E2010 and 88E2040L device boundary scan orders, respectively, where:

TDI ➔ P0_SON/P[0] (AC/DC) ➔ … ➔ SPI_SSn(Output) ➔ TDO

Table 31: TAP Controller Opcodes

Instruction	OpCode
EXTEST	00000000
SAMPLE/PRELOAD	00000001
CLAMP	00000010
HIGH-Z	00000011
ID_CODE	00000100
EXTEST_PULSE	00000101
EXTEST_TRAIN	00000110
PROG_HYST	00001000
BYPASS	11111111

The device reserves five pins called the Test Access Port (TAP) to provide test access:

- Test Mode Select Input (TMS)
- Test Clock Input (TCK)
- Test Data Input (TDI)
- Test Data Output (TDO)
- Test Reset Input (TRSTn)

To ensure race-free operation, all input and output data is synchronous with the test clock (TCK). TAP input signals (TMS and TDI) are clocked into the test logic on the rising edge of TCK, while output signal (TDO) is clocked on the falling edge. For additional details, refer to the IEEE 1149.1 Boundary Scan Architecture document.

3.10.1 BYPASS Instruction

The BYPASS instruction uses the bypass register. This register contains a single shift-register stage and is used to provide a minimum length serial path between the TDI and TDO pins of the device when test operation is not required. This arrangement allows rapid movement of test data to and from other testable devices in the system.

3.10.2 SAMPLE/PRELOAD Instruction

The SAMPLE/PRELOAD instruction enables scanning of the boundary-scan register without causing interference to the normal operation of the device. Two functions are performed when this instruction is selected: SAMPLE and PRELOAD.

SAMPLE allows a snapshot to be taken of the data flowing from the system pins to the on-chip test logic or vice versa, without interfering with normal operation. The snapshot is taken on the rising edge of TCK in the Capture-DR controller state, and the data can be viewed by shifting through the component's TDO output.

While sampling and shifting data out through TDO for observation, PRELOAD enables an initial data pattern to be shifted in through TDI and to be placed at the latched parallel output of the boundary-scan register cells that are connected to system output pins. This step ensures that known data is driven through the system output pins upon entering the extest instruction. Without PRELOAD, indeterminate data would be driven until the first scan sequence is complete. The shifting of data for the sample and preload phases can occur simultaneously. While data capture is being shifted out, the preload data can be shifted in.

Table 32: 88E2010 Boundary Scan Chain Order

Order	Pin	I/O
1	SPI_SSn	Output
2	SPI_SSn	Output Enable
3	SPI_CLK	Output
4	SPI_CLK	Output Enable
5	SPI_MOSI	Output
6	SPI_MOSI	Output Enable
7	SPI_MISO	Input
8	RESETn	Input
9	RCLK1	Output
10	RCLK1	Output Enable
11	RCLK0	Output
12	RCLK0	Output Enable
13	CONFIG[7]	Input
14	CONFIG[6]	Input
15	CONFIG[5]	Input
16	CONFIG[4]	Input
17	CONFIG[3]	Input
18	CONFIG[2]	Input
19	CONFIG[1]	Input
20	CONFIG[0]	Input
21	MDIO[0]	Input
22	MDIO[0]	Output
23	MDIO[0]	Output Enable
24	MDC[0]	Input
25	P0_LED[3]	Input
26	P0_LED[3]	Output
27	P0_LED[3]	Output Enable
28	P0_LED[2]	Input
29	P0_LED[2]	Output

Table 32: 88E2010 Boundary Scan Chain Order (Continued)

Order	Pin	I/O
30	P0_LED[2]	Output Enable
31	P0_LED[1]	Input
32	P0_LED[1]	Output
33	P0_LED[1]	Output Enable
34	P0_LED[0]	Input
35	P0_LED[0]	Output
36	P0_LED[0]	Output Enable
37	Reserved	Input
38	Reserved	Output
39	Reserved	Output Enable
40	Reserved	Input
41	Reserved	Output
42	Reserved	Output Enable
43	Reserved	Input
44	Reserved	Output
45	Reserved	Output Enable
46	Reserved	Input
47	Reserved	Output
48	Reserved	Output Enable
49	Reserved	Input
50	Reserved	Output
51	Reserved	Output Enable
52	Reserved	Input
53	Reserved	Output
54	Reserved	Output Enable
55	INTn	Output
56	INTn	Output Enable
57	CLK_SEL[1]	Input

Table 32: 88E2010 Boundary Scan Chain Order (Continued)

Order	Pin	I/O
58	CLK_SEL[0]	Input
59	P0_SIN[3]	Input
60	P0_SIP[3]	Input
61	P0_SON[3]/ P0_SOP[3]	Output
62	P0_SON[3]/ P0_SOP[3]	AC/DC Select
63	P0_SIN[2]	Input
64	P0_SIP[2]	Input
65	P0_SON[2]/ P0_SOP[2]	Output
66	P0_SON[2]/ P0_SOP[2]	AC/DC Select
67	P0_SIN[1]	Input
68	P0_SIP[1]	Input
69	P0_SON[1]/ P0_SOP[1]	Output
70	P0_SON[1]/ P0_SOP[1]	AC/DC Select
71	P0_SIN[0]	Input
72	P0_SIP[0]	Input
73	P0_SON[0]/ P0_SOP[0]	Output
74	P0_SON[0]/ P0_SOP[0]	AC/DC Select

Table 33: 88E2010 Boundary Scan Exclusion List

Pin	I/O
MDIN[0]	Analog
MDIN[1]	Analog
MDIN[2]	Analog
MDIN[3]	Analog
MDIP[0]	Analog
MDIP[1]	Analog
MDIP[2]	Analog
MDIP[3]	Analog
TSTCP	Analog
TSTCN	Analog
TEST_CLKP	Analog
TEST_CLKN	Analog
CMN	Analog
CMP	Analog
ATN	Analog
ATP	Analog
CIREF	Analog
SIREF	Analog
CLKP	Analog
CLKN	Analog
XTAL1	Analog
XTAL2	Analog
CHSDACP	Analog
CHSDACN	Analog
SHSDACP	Analog
SHSDACN	Analog
CTSTPT	Analog
STSTPT	Analog
TEST	Analog

Table 33: 88E2010 Boundary Scan Exclusion List (Continued)

Pin	I/O
VDDCTRL	Analog
TDI	JTAG
TDO	JTAG
TMS	JTAG
TCK	JTAG
TRSTn	JTAG
VSEL_L	Power
VSEL_M	Power
VSEL_R	Power
VSEL_T	Power
VHV	Power
AVDDL	Power
AVDDH	Power
AVDDT	Power
AVSSC	Power
AVSS	Power
VDDR09	Power
AVDDS	Power
AVDDR	Power
AVDDC	Power
DVDD	Power
VDDOL	Power
VDDOM	Power
VDDOR	Power
VDDOT	Power
VSS	Power

Table 34: 88E2040L Boundary Scan Chain Order

Order	Pin	I/O
1	SPI_SSn	Output
2	SPI_SSn	Output Enable
3	SPI_CLK	Output
4	SPI_CLK	Output Enable
5	SPI_MOSI	Output
6	SPI_MOSI	Output Enable
7	SPI_MISO	Input
8	RESETn	Input
9	RCLK1	Output
10	RCLK1	Output Enable
11	RCLK0	Output
12	RCLK0	Output Enable
13	CONFIG[7]	Input
14	CONFIG[6]	Input
15	CONFIG[5]	Input
16	CONFIG[4]	Input
17	CONFIG[3]	Input
18	CONFIG[2]	Input
19	CONFIG[1]	Input
20	CONFIG[0]	Input
21	MDIO[3]	Input
22	MDIO[3]	Output
23	MDIO[3]	Output Enable
24	MDC[3]	Input
25	P3_LED[3]	Input
26	P3_LED[3]	Output
27	P3_LED[3]	Output Enable
28	P3_LED[2]	Input
29	P3_LED[2]	Output

Table 34: 88E2040L Boundary Scan Chain Order (Continued)

Order	Pin	I/O
30	P3_LED[2]	Output Enable
31	P3_LED[1]	Input
32	P3_LED[1]	Output
33	P3_LED[1]	Output Enable
34	P3_LED[0]	Input
35	P3_LED[0]	Output
36	P3_LED[0]	Output Enable
37	Reserved	Input
38	Reserved	Output
39	Reserved	Output Enable
40	Reserved	Input
41	Reserved	Output
42	Reserved	Output Enable
43	Reserved	Input
44	Reserved	Output
45	Reserved	Output Enable
46	P3_SIN[1]	Input
47	P3_SIP[1]	Input
48	P3_SON[1]/ P3_ SOP[1]	Output
49	P3_SON[1]/ P3_ SOP[1]	AC/DC Select
50	P3_SIN[0]	Input
51	P3_SIP[0]	Input
52	P3_SON[0]/ P3_ SOP[0]	Output
53	P3_SON[0]/ P3_ SOP[0]	AC/DC Select
54	MDIO[2]	Input
55	MDIO[2]	Output
56	MDIO[2]	Output Enable

Table 34: 88E2040L Boundary Scan Chain Order (Continued)

Order	Pin	I/O
57	MDC[2]	Input
58	P2_LED[3]	Input
59	P2_LED[3]	Output
60	P2_LED[3]	Output Enable
61	P2_LED[2]	Input
62	P2_LED[2]	Output
63	P2_LED[2]	Output Enable
64	P2_LED[1]	Input
65	P2_LED[1]	Output
66	P2_LED[1]	Output Enable
67	P2_LED[0]	Input
68	P2_LED[0]	Output
69	P2_LED[0]	Output Enable
70	Reserved	Input
71	Reserved	Output
72	Reserved	Output Enable
73	Reserved	Input
74	Reserved	Output
75	Reserved	Output Enable
76	Reserved	Input
77	Reserved	Output
78	Reserved	Output Enable
79	P2_SIN[1]	Input
80	P2_SIP[1]	Input
81	P2_SON[1]/ P2_ SOP[1]	Output
82	P2_SON[1]/ P2_ SOP[1]	AC/DC Select

Table 34: 88E2040L Boundary Scan Chain Order (Continued)

Order	Pin	I/O
83	P2_SIN[0]	Input
84	P2_SIP[0]	Input
85	P2_SON[0]/ P2_ SOP[0]	Output
86	P2_SON[0]/ P2_ SOP[0]	AC/DC Select
87	MDIO[1]	Input
88	MDIO[1]	Output
89	MDIO[1]	Output Enable
90	MDC[1]	Input
91	P1_LED[3]	Input
92	P1_LED[3]	Output
93	P1_LED[3]	Output Enable
94	P1_LED[2]	Input
95	P1_LED[2]	Output
96	P1_LED[2]	Output Enable
97	P1_LED[1]	Input
98	P1_LED[1]	Output
99	P1_LED[1]	Output Enable
100	P1_LED[0]	Input
101	P1_LED[0]	Output
102	P1_LED[0]	Output Enable
103	Reserved	Input
104	Reserved	Output
105	Reserved	Output Enable
106	Reserved	Input
107	Reserved	Output
108	Reserved	Output Enable
109	Reserved	Input

Table 34: 88E2040L Boundary Scan Chain Order (Continued)

Order	Pin	I/O
110	Reserved	Output
111	Reserved	Output Enable
112	P1_SIN[1]	Input
113	P1_SIP[1]	Input
114	P1_SON[1]/ P1_ SOP[1]	Output
115	P1_SON[1]/ P1_ SOP[1]	AC/DC Select
116	P1_SIN[0]	Input
117	P1_SIP[0]	Input
118	P1_SON[0]/ P1_ SOP[0]	Output
119	P1_SON[0]/ P1_ SOP[0]	AC/DC Select
120	MDIO[0]	Input
121	MDIO[0]	Output
122	MDIO[0]	Output Enable
123	MDC[0]	Input
124	P0_LED[3]	Input
125	P0_LED[3]	Output
126	P0_LED[3]	Output Enable
127	P0_LED[2]	Input
128	P0_LED[2]	Output
129	P0_LED[2]	Output Enable
130	P0_LED[1]	Input
131	P0_LED[1]	Output
132	P0_LED[1]	Output Enable
133	P0_LED[0]	Input
134	P0_LED[0]	Output
135	P0_LED[0]	Output Enable
136	Reserved	Input

Table 34: 88E2040L Boundary Scan Chain Order (Continued)

Order	Pin	I/O
137	Reserved	Output
138	Reserved	Output Enable
139	Reserved	Input
140	Reserved	Output
141	Reserved	Output Enable
142	Reserved	Input
143	Reserved	Output
144	Reserved	Output Enable
145	INTn	Output
146	INTn	Output Enable
147	CLK_SEL[1]	Input
148	CLK_SEL[0]	Input
149	P0_SIN[1]	Input
150	P0_SIP[1]	Input
151	P0_SON[1]/ P0_ SOP[1]	Output
152	P0_SON[1]/ P0_ SOP[1]	AC/DC Select
153	P0_SIN[0]	Input
154	P0_SIP[0]	Input
155	P0_SON[0]/ P0_ SOP[0]	Output
156	P0_SON[0]/ P0_ SOP[0]	AC/DC Select

Table 35: 88E2040L Boundary Scan Exclusion List

Pin	I/O
P0_MDIN[0]	Analog
P0_MDIN[1]	Analog
P0_MDIN[2]	Analog
P0_MDIN[3]	Analog
P0_MDIP[0]	Analog
P0_MDIP[1]	Analog
P0_MDIP[2]	Analog
P0_MDIP[3]	Analog
P1_MDIN[0]	Analog
P1_MDIN[1]	Analog
P1_MDIN[2]	Analog
P1_MDIN[3]	Analog
P1_MDIP[0]	Analog
P1_MDIP[1]	Analog
P1_MDIP[2]	Analog
P1_MDIP[3]	Analog
P2_MDIN[0]	Analog
P2_MDIN[1]	Analog
P2_MDIN[2]	Analog
P2_MDIN[3]	Analog
P2_MDIP[0]	Analog
P2_MDIP[1]	Analog
P2_MDIP[2]	Analog
P2_MDIP[3]	Analog
P3_MDIN[0]	Analog
P3_MDIN[1]	Analog
P3_MDIN[2]	Analog
P3_MDIN[3]	Analog
P3_MDIP[0]	Analog

Table 35: 88E2040L Boundary Scan Exclusion List (Continued)

Pin	I/O
P3_MDIP[1]	Analog
P3_MDIP[2]	Analog
P3_MDIP[3]	Analog
TSTCP	Analog
TSTCN	Analog
TEST_CLKN	Analog
TEST_CLKP	Analog
P0_CMN	Analog
P0_CMP	Analog
P1_CMN	Analog
P1_CMP	Analog
P2_CMN	Analog
P2_CMP	Analog
P3_CMN	Analog
P3_CMP	Analog
P0_ATN[1]	Analog
P0_ATN[1]	Analog
P0_ATN[2]	Analog
P0_ATN[3]	Analog
P0_ATP[0]	Analog
P0_ATP[1]	Analog
P0_ATP[2]	Analog
P0_ATP[3]	Analog
P1_ATN[0]	Analog
P1_ATN[1]	Analog
P1_ATN[2]	Analog

Table 35: 88E2040L Boundary Scan Exclusion List (Continued)

Pin	I/O
P1_ATN[3]	Analog
P1_ATP[0]	Analog
P1_ATP[1]	Analog
P1_ATP[2]	Analog
P1_ATP[3]	Analog
P2_ATN[0]	Analog
P2_ATN[1]	Analog
P2_ATN[2]	Analog
P2_ATN[3]	Analog
P2_ATP[0]	Analog
P2_ATP[1]	Analog
P2_ATP[2]	Analog
P2_ATP[3]	Analog
P3_ATN[0]	Analog
P3_ATN[1]	Analog
P3_ATN[2]	Analog
P3_ATN[3]	Analog
P3_ATP[0]	Analog
P3_ATP[1]	Analog
P3_ATP[2]	Analog
P3_ATP[3]	Analog
CIREF	Analog
SIREF	Analog
CLKP	Analog
CLKN	Analog
XTAL1	Analog
XTAL2	Analog

Table 35: 88E2040L Boundary Scan Exclusion List (Continued)

Pin	I/O
CHSDACP	Analog
CHSDACN	Analog
SHSDACP	Analog
SHSDACN	Analog
CTSTPT	Analog
STSTPT	Analog
TEST	Analog
TDI	JTAG
TDO	JTAG
TMS	JTAG
TCK	JTAG
TRSTn	JTAG
VSEL_L	Power
VSEL_M	Power
VSEL_R	Power
VSEL_T	Power
P0_VHV	Power
P1_VHV	Power
P2_VHV	Power
P3_VHV	Power
P0_AVDDL	Power
P1_AVDDL	Power
P2_AVDDL	Power
P3_AVDDL	Power
P0_AVDDH	Power
P1_AVDDH	Power
P2_AVDDH	Power
P3_AVDDH	Power

Table 35: 88E2040L Boundary Scan Exclusion List (Continued)

Pin	I/O
P0_AVDDT	Power
P1_AVDDT	Power
P2_AVDDT	Power
P3_AVDDT	Power
AVSSC	Power
AVSS	Power
P0_VDDR09	Power
P1_VDDR09	Power
P2_VDDR09	Power
P3_VDDR09	Power
P0_AVDDS	Power
P1_AVDDS	Power
P2_AVDDS	Power
P3_AVDDS	Power
P0_AVDDR	Power
P1_AVDDR	Power
P2_AVDDR	Power
P3_AVDDR	Power
AVDDC	Power
DVDD	Power
VDDOL	Power
VDDOM	Power
VDDOR	Power
VDDOT	Power
VSS	Power

3.10.3 EXTEST Instruction

The EXTEST instruction enables circuitry external to the device (typically the board interconnections) to be tested. Prior to executing the EXTEST instruction, the first test stimulus to be applied is shifted into the boundary-scan registers using the SAMPLE/PRELOAD instruction. So, when the change to the extest instruction occurs, known data is driven immediately from the device to its external connections. The SOP/N[1:0] pins will be driven to static levels. The positive and negative legs of the SOP/N[1:0] pins are controlled via a single boundary scan cell.The positive leg outputs the level specified by the boundary scan cell while the negative leg outputs the opposite level.

3.10.4 CLAMP Instruction

The CLAMP instruction enables the state of the signals driven from component pins to be determined from the boundary-scan register while the bypass register is selected as the serial path between TDI and TDO. The signals driven from the component pins do not change while the clamp instruction is selected.

3.10.5 HIGH-Z Instruction

The HIGH-Z instruction places all of the digital component system logic outputs in an inactive high-impedance drive state. In this state, an in-circuit test system may drive signals onto the connections normally driven by a component output without incurring the risk of damage to the component.

3.10.6 ID CODE Instruction

The ID CODE instruction contains the manufacturer identity, part and version.

Table 36: ID CODE Instruction

Device	Version	Part Number	Manufacturer Identity	
	Bit 31 to 28	Bit 27 to 12	Bit 11 to 1	Bit 0
88E2010	0000	0000000000011001	00111101110	1
88E2040L	0000	0000000000011011	00111101110	1

3.10.7 EXTEST_PULSE Instruction

The AC- or DC-JTAG test modes can be selected for each port individually by scanning in the desired bit value into AC/DC select scan registers shown in the scan chain (Table 32, 88E2010 Boundary Scan Chain Order, on page 84 or Table 34, 88E2040L Boundary Scan Chain Order, on page 87). When the AC/DC select is set to DC the EXTEST_PULSE instruction has the same behavior as the EXTEST instruction.

When the AC/DC select is set to AC, the EXTEST_PULSE instruction has the same behavior as the EXTEST instruction except for the behavior of the SOP/N[1:0] pins.

As in the EXTEST instruction, the test stimulus must first be shifted into the boundary-scan registers. Upon the execution of the EXTEST_PULSE instruction the SOP[1:0] pins output the level specified by the test stimulus and SON[1:0] pins output the opposite level.

However, if the TAP controller enters into the Run-Test/Idle state, then the SON[1:0] pins output the level specified by the test stimulus and SOP[1:0] pins output the opposite level.

When the TAP controller exits the Run-Test/Idle state, the SOP[1:0] pins again output the level specified by the test stimulus and SON[1:0] pins output the opposite level.

3.10.7.1 EXTEST_TRAIN Instruction

When the AC/DC select is set to DC, the EXTEST_TRAIN instruction has the same behavior as the EXTEST instruction.

When the AC/DC select is set to AC, the EXTEST_TRAIN instruction has the same behavior as the EXTEST instruction except for the behavior of the SOP/N[1:0] pins.

As in the EXTEST instruction, the test stimulus must first be shifted into the boundary-scan registers. Upon the execution of the EXTEST_PULSE instruction the SOP[1:0] pins output the level specified by the test stimulus and SON[1:0] pins output the opposite level.

However, if the TAP controller enters into the Run-Test/Idle state the SOP/N[1:0] will toggle between inverted and non-inverted levels on the falling edge of TCK. This toggling will continue for as long as the TAP controller remains in the Run-Test/Idle state.

When the TAP controller exits the Run-Test/Idle state, the SOP[1:0] pins again output the level specified by the test stimulus and SON[1:0] pins output the opposite level.

3.10.8 PROG_HYST Instruction

The test receivers connected to the XIP/N[3:0] and MIP/N[3:0] pins require the hysteresis level to be set according to the application that the SERDES is used in. The amount of hysteresis required is a function of the expected voltage swing on the input. The proprietary command PROG_HYST will program three registers in the TAP controller which will set the value of the hysteresis.

When the PROG_HYST opcode is in the instruction register, the following actions occur in the TAP controller states:

- Capture-DR state: Load the value in HYST[2:0] into SR_HYST[2:0].
- Shift-DR state: Shift TDI into SR_HYST[0], SR_HYST[1:0] into SR_HYST[2:1], and SR_HYST[2] to TDO. Three bits should be loaded to set the new test receiver hysteresis value.
- Update-DR state: Load the value in SR_HYST[2:0] into HYST[2:0].
- HYST[2:0] is the register that sets the hysteresis in the test receiver.
- SR_HYST[2:0] is the 3-bit shift register used to shift the values in and out.

The hysteresis mapping is shown in Table 37. 70 mV is the default setting. When the TAP controller is in the Test-Logic-Reset state or when TRSTn is forced low, the HYST[2:0] is reset to the default state

Table 37: Test Receiver Hysteresis Setting

HYST[2:0]	Hysteresis
000	12 mV
001	25 mV
010	50 mV
011	70 mV
100	90 mV
101	105 mV
110	135 mV
111	150 mV

3.10.9 AC-JTAG Fault Detection

The fault detection across AC-coupled connections can be detected with a combination of (DC) EXTEST and any one of the AC-JTAG commands. The AC-coupled connection is shown in Figure 12. The fault signature is shown in Table 38. Column 1 lists the fault type.

Columns 2 to 5 lists the behavior when both the transmitter and receiver are running the EXTEST_TRAIN and EXTEST_PULSE commands. Column 2 shows the expected value captured by the boundary scan cell that is connected to the test receiver, which is connected to the positive input when a negative differential pulse is transmitted. Column 3 is the same as column 2 except for the negative input. Columns 4 and 5 are similar to columns 2 and 3 except a positive differential pulse is transmitted.

Columns 6 to 9 is similar to columns 2 to 5 except both the transmitter and receiver are running the (DC) EXTEST command.

While it is not possible to identify precisely which fault is occurring based on the fault signature, the signature to the no fault condition is unique when the (DC) EXTEST command is run with at least one of the EXTEST_TRAIN or EXTEST_PULSE commands. Running only AC-JTAG commands is not sufficient since the no fault condition signature is not distinguishable from the Tx to Rx short (see shaded cells in Table 38).

Figure 12: AC-Coupled Connection

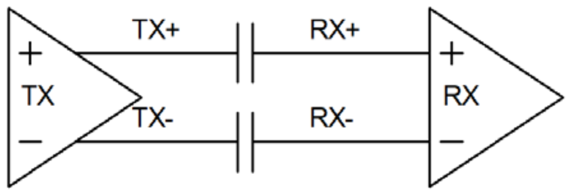


Table 38: AC-Coupled Connection Fault Signature

DC-Coupled Fault	AC Testing Sample 0		AC Testing Sample 1		(DC) EXTEST Sample 0		(DC) EXTEST Sample 1	
	Positive Leg	Negative Leg	Positive Leg	Negative Leg	Positive Leg	Negative Leg	Positive Leg	Negative Leg
TX+ Open	0	X	0	X	1	X	1	X
TX- Open	X	0	X	0	X	1	X	1
RX+ Open	0	X	0	X	1	X	1	X
RX- Open	X	0	X	0	X	1	X	1
TX+ short to power	0/Note 2	X	0/Note 2	X	1	X	1	X
TX- short to power	X	0/Note 2	X	0/Note 2	X	1	X	1
RX+ short to power	0/Note 2	X	0/Note 2	X	1	X	1	X
RX- short to power	X	0/Note 2	X	0/Note 2	X	1	X	1
TX+ short to ground	0	X	0	X	1	X	1	X
TX- short to ground	X	0	X	0	X	1	X	1
RX+ short to ground	0	X	0	X	0	X	0	X
RX- short to ground	X	0	X	0	X	0	X	0
TX+ short to TX-	Note 1	Note 1	Note 1	Note 1	1	1	1	1
RX+ short to RX-	Note 1	Note 1	Note 1	Note 1	1	1	1	1
TX+ short to RX-	X	0	X	1	X	0	X	1

Table 38: AC-Coupled Connection Fault Signature (Continued)

DC-Coupled Fault	AC Testing Sample 0		AC Testing Sample 1		(DC) EXTEST Sample 0		(DC) EXTEST Sample 1	
	Positive Leg	Negative Leg	Positive Leg	Negative Leg	Positive Leg	Negative Leg	Positive Leg	Negative Leg
TX- short to RX+	1	X	0	X	1	X	0	X
TX+ short to RX+	0	X	1	X	0	X	1	X
TX- short to RX-	X	1	X	0	X	1	X	0
No Fault	0	1	1	0	1	1	1	1
Note 1	Short on positive and negative leg can have several behavior on the test receiver. If both drivers cancel each other out, then output on both legs is 0. If one driver dominates the other driver, then both legs are either both 1 or both 0. In any case, the result is that both legs will have the same value.							
Note 2	A solid short to power is assumed. If the short has high inductance, then a pulse may still be sent at the receiver and will be mistaken as a good connection.							

The fault detection across DC-coupled connections can be detected with any one of the AC-JTAG or (DC) EXTEST commands.The DC-coupled connection is shown in Figure 13. The fault signature is shown in Table 39.

Figure 13: DC-Coupled Connection

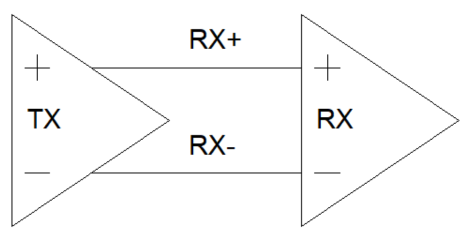


Table 39: DC-Coupled Connection Fault Signature

DC-Coupled Fault	AC Testing Sample 0		AC Testing Sample 1		(DC) EXTEST Sample 0		(DC) EXTEST Sample 1	
	Positive Leg	Negative Leg	Positive Leg	Negative Leg	Positive Leg	Negative Leg	Positive Leg	Negative Leg
RX+ Open	0	X	0	X	1	X	1	X
RX- Open	X	0	X	0	X	1	X	1
RX+ short to power	0/Note 2	X	0/Note 2	X	1	X	1	X
RX- short to power	X	0/Note 2	X	0/Note 2	X	1	X	1
RX+ short to ground	0	X	0	X	0	X	0	X
RX- short to ground	X	0	X	0	X	0	X	0

Table 39: DC-Coupled Connection Fault Signature

DC-Coupled Fault	AC Testing Sample 0		AC Testing Sample 1		(DC) EXTEST Sample 0		(DC) EXTEST Sample 1	
	Positive Leg	Negative Leg	Positive Leg	Negative Leg	Positive Leg	Negative Leg	Positive Leg	Negative Leg
RX+ short to RX-	Note 1	Note 1	Note 1	Note 1	Note 1	Note 1	Note 1	Note 1
No Fault	0	1	1	0	0	1	1	0
Note 1	Short on positive and negative leg can have several behaviors on the test receiver. If both drivers cancel each other out, then output on both legs is 0. If one driver dominates the other driver, then both legs are either both 1 or both 0. In any case, the result is that both legs will have the same value.							
Note 2	A solid short to power is assumed. If the short has high inductance, then a pulse may still be sent at the receiver and will be mistaken as a good connection.							

3.11 Reference Clock

The 88E2010/88E2040L device can use a 50 MHz or 156.25 MHz differential clock into CLKP/N or a 50 MHz crystal as the reference clock.

The device can use one of three clocking options as shown in Table 40. CLK_SEL must be stable and the selected clock toggling prior to de-assertion of RESETn. CLK_SEL must not change value for the duration of device operation.

Table 40: Reference Clock Options

CLK_SEL[1:0]	XTAL1/XTAL2	CLKP/CLKN
00	50 MHz	Floating
01	GND	50 MHz
10	GND	156.25 MHz
11	Reserved	Reserved

Note

50 MHz crystal operation is only supported for commercial-grade devices.

3.12 Power Supplies

The 88E2010/88E2040L device requires the following power supplies: AVDDT, AVDDL, AVDDH, DVDD. and VDDO.

3.12.1 AVDDL

AVDDL is the copper transmitter and receiver 1.5V analog supply.

3.12.2 AVDDH

AVDDH is the copper transmitter and receiver 1.8V or 2.0V analog supply.

3.12.3 AVDDT

AVDDT is the copper transmitter 2.3V or 2.5V analog supply.

3.12.4 AVDDC

AVDDC is the common analog supply of 1.5V.

3.12.5 AVDDS

AVDDS is the SERDES analog supply of 1.5V.

3.12.6 AVDDR

AVDDR is the regulator supply and should be tied to 1.5V.

3.12.7 DVDD

DVDD is the core logic 0.8V or 0.88V digital supply. (0.88V for I-grade only)

3.12.8 VDDO

There are four separate VDDO segments (VDDOT, VDDOR, VDDOL, and VDDOM). Each segment can be independently set to one for the following voltages: 1.5V, 1.8V, 2.5V, or 3.3V, except VDDOM that can also support 1.2V. Each VDDO segment has a corresponding voltage select configuration pin (VSEL_T, VSEL_R, VSEL_L, and VSEL_M). Table 41 lists the signals under each of the VDDO segments.

If the VDDO* segment is set to 1.2V, 1.5V, or 1.8V, then its corresponding VSEL_* should tied to VDDO*.

If the VDDO* segment is set to 2.5V, or 3.3V, then its corresponding VSEL_* should tied to VSS.

The input pins are not high voltage tolerant. For example, if VDDOR is tied to 2.5V, then RESETn should not be driven to 3.3V.

Table 41: Signal Power Segment

Power Segment	VDDOT	VDDOR	VDDOL	VDDOM
Voltage Select	VSEL_T	VSEL_R	VSEL_L	VSEL_M
Signals	TCK	GPIO[x:0]	CLK_SEL[1:0]	INTn
	TDI	RCLK0	CONFIG[7:0]	MDC[x:0]
	TDO	RCLK1	LED0[3:0]	MDIO[x:0]
	TMS	RESETn		TEST
	TRST	SPI_CLK		
		SPI_MOS0		
		SPI_MOS1		
		SPI_SSn		

3.12.9 VHV

The VHV pin is a test pin and should be left floating during normal operation.

3.12.10 VDD09

VDD09 is the 0.9V internally generated regulated output and these pins should be tied to an external 0.22 µF capacitor to VSS.

4 Copper Unit (T Unit)

This section describes the copper unit (T Unit) interface functions.

4.1 Media Interface

The copper interface consists of the MDIP/N[3:0] pins that connect to the physical media for 5GBASE-T, 2.5GBASE-T, 1000BASE-T, 100BASE-TX, and 10BASE-T modes of operation.

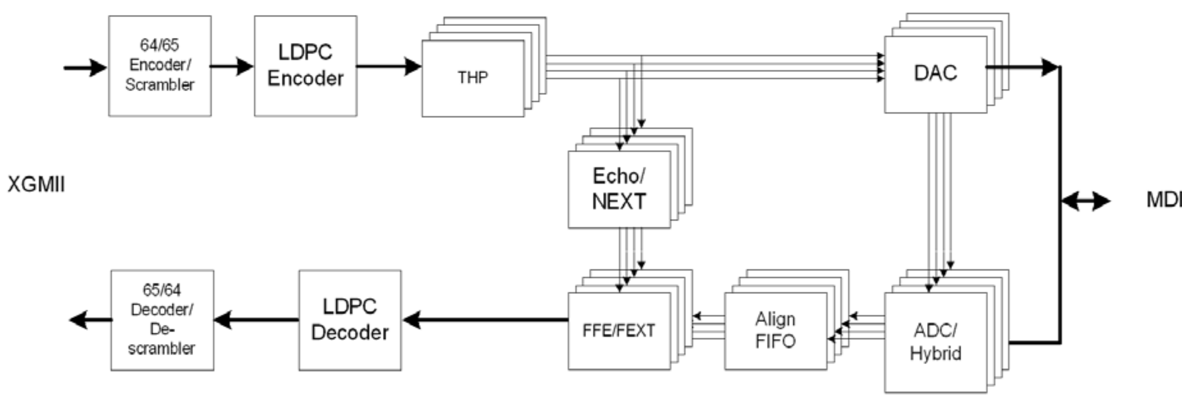
The device integrates MDI interface termination resistors. The IEEE 802.3 specification requires that both sides of a link have termination resistors to prevent reflections. Traditionally, these resistors and additional capacitors are placed on the board between a PHY device and the magnetics. The resistors must be very accurate to meet the strict IEEE return loss requirements. Typically, ±1% accuracy resistors are used on the board. These additional components between the PHY and the magnetics complicate board layout. Integrating the resistors has many advantages including component cost savings, better ICT yield, board reliability improvements, board area savings, improved layout, and signal integrity improvements. See the *Benefits of Integrating Termination Resistors for Ethernet Application Note* for details.

The transmitter can be shut down in all operational speeds by setting register 3.8109.0 to 1 in 10M/100M/1G operation and register 1.0009.0 to 1 for 2.5G/5G operation.

Each channel's transmitter's polarity can be reversed by setting the corresponding bit in register 3.8001.3:0 to 1 in 10M/100M/1G operation. Channel transmitter polarity reversal is not supported for 2.5G/5G operation. The devices support Auto-MDI/MDIX to automatically switch to the proper configuration when a cable is connected.

4.1.1 2.5GBASE-T and 5GBASE-T

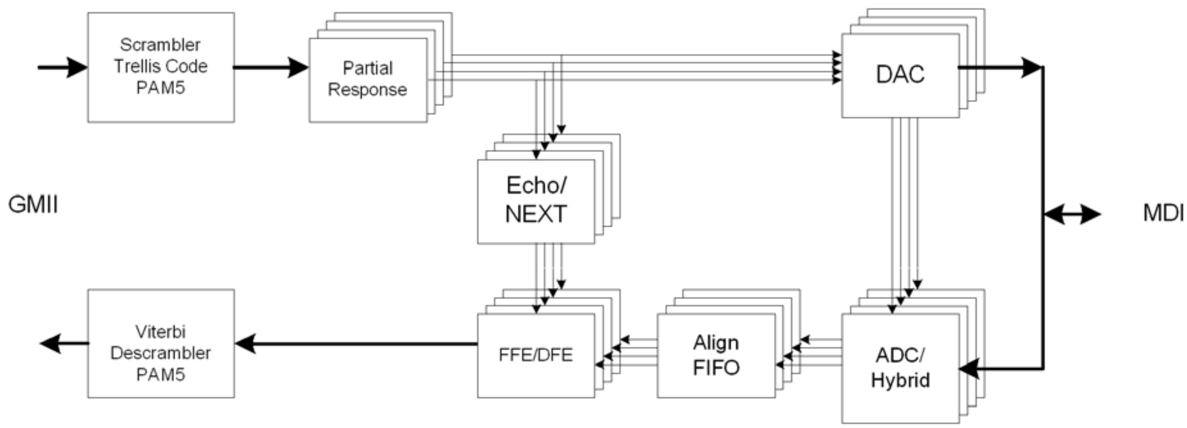
Figure 14: 2.5GBASE-T and 5GBASE-T Data Path



The device performs all the physical layer functions of 2.5GBASE-T and 5GBASE-T over a CAT 5e, 6A, and 7 cable system. The device performs scrambling, LDPC coding, PAM16 mapping, and THP pre-coding on the transmit side with adaptive equalization, full echo cancellation, decoding and de-scrambling on the receive side. It is fully compliant to the IEEE 802.3 standard, including the PMA and PCS sublayers for full physical layer functionality.

4.1.2 1000BASE-T

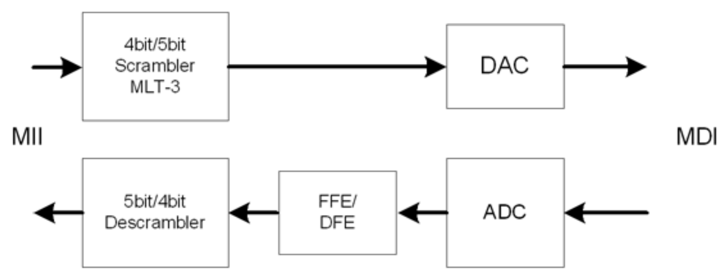
Figure 15: 1000BASE-T Data Path



The device performs all the physical layer functions of 1000BASE-T full or half duplex on twisted pair CAT 5, 6, and 7 cable. It is fully compliant to the IEEE 802.3 standard, including the PMD, PMA, and PCS sublayers. The device, for 1000BASE-T, performs scrambling, Trellis coding, PAM5 mapping functions on the transmit side with adaptive equalization, echo cancellation, viterbi decoding and de-scrambling on the receive side.

4.1.3 100BASE-TX

Figure 16: 100BASE-TX Data Path

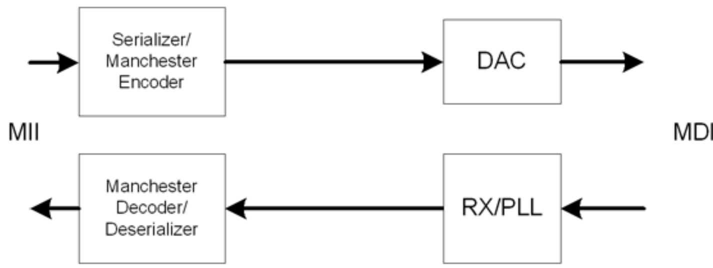


The device performs all the physical layer functions of 100BASE-TX full or half duplex on twisted pair CAT 5, 6, and 7 cable. It is fully compliant to the IEEE 802.3 standard, including the PMD, PMA, and PCS sublayers. The device supports Auto-MDI/MDIX to automatically switch to the proper configuration once a cable is connected. As mentioned, the device also integrates the PHY termination resistors enabling BOM material and cost savings, ease of board layout, and bettered signal integrity.

Document Classification: Public

4.1.4 10BASE-T

Figure 17: 10BASE-T Data Path



The device additionally performs all the physical layer functions of 10BASE-T full or half duplex on twisted pair cable. It is compliant to the IEEE 802.3 standard, including the PMD, PMA, and PCS sublayers.

4.1.5 Taking Down the Link

4.1.5.1 Taking Down the Link in 5GBASE-T/2.5GBASE-T Modes

When the link is established, the link monitor algorithm will detect conditions where a retrain is required, such as the link partner has dropped the link or the link quality has dropped below acceptable levels.

The PHY supports fast retrain defined for 2.5G/5GBASE-T in IEEE 802.3bz-2016. The PHY also supports a Negotiated Fast Retrain defined for pre-standard devices. If the local device and the link partner have negotiated fast retrain support and the link quality has dropped below operating conditions, then the PHY will enter fast retrain in coordination with the link partner and return to normal operation within the defined fast retrain duration. If the PHY fails to achieve acceptable link quality or the fast retrain process fails, then the PHY will drop the link and return to normal training.

When fast retrain is not negotiated and the link quality has dropped below operating conditions, the PHY will perform a retrain as defined in IEEE Std. 802.3an-2006. Upon a failure to retrain, the PHY will return to Auto-Negotiation.

4.1.5.2 Taking Down the Link in 1000BASE-T Mode

The link is established when both sides so indicate. Each side continues sending idle symbols whenever it has no data to transmit. The link is maintained as long as valid idle, data, or carrier extension symbols are received.

4.1.5.3 Taking Down the Link in 100BASE-TX Mode

For 100BASE-TX links, the PHY devices and its link partner begin transmitting idle symbols after completion of the Auto-Negotiation process. Each side continues sending idle symbols whenever it has no data to transmit. The link is maintained as long as valid idle symbols or data are received.

The PHY devices take down an established link when the required conditions are no longer met. When a link is down, data transmission stops.

For 100BASE-TX and 1000BASE-T links, taking down a link occurs after valid idle codes are no longer received. After the link is down, if Auto-Negotiation is enabled, then the PHY devices reenter the Auto-Negotiation phase and begin transmitting FLPs.

4.2 Loopback

The T Unit implements multiple loopback paths.

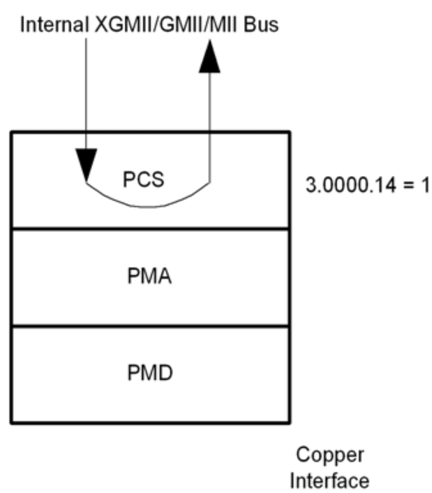
4.2.1 MAC Loopback

The T Unit can loop back data from the internal XGMII/GMII/MII bus by setting register 3.0000.14 to 1 for all modes. In 10/100/1000 loopback mode, the data received from the internal GMII/MII bus is not transmitted on the media interface and the link will be dropped. In 2.5G/5G loopback mode, the link will remain active and data from the internal XGMII bus will be transmitted on to the media interface.

If Auto-Negotiation and loopback are enabled, then FLP Auto-Negotiation codes will be transmitted. If the T Unit is in forced 10BASE-T mode and loopback is enabled, then 10BASE-T idle link pulses will be transmitted on the media interface. If the T Unit is in forced 100BASE-T mode and loopback is enabled, then 100BASE-T idles will be transmitted on the media interface.

When MAC loopback is enabled, the loopback speed will be the active link speed of the T Unit. If the link is down, then the loopback speed will be determined by register 31.F000.7:6.

Figure 18: MAC Interface Loopback Diagram — Copper Media Interface



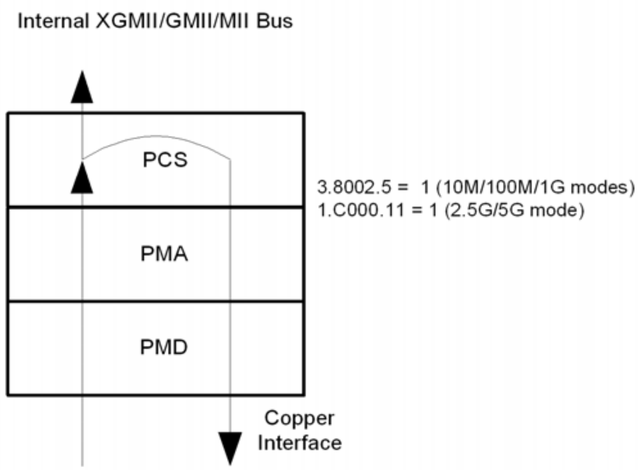
4.2.2 Line Loopback

Line loopback allows a link partner to send frames into the media interface to test the transmit and receive data paths. Frames from a link partner into the PHY bus are looped back and sent out on the line before reaching the internal XGMII/GMII/MII. They are also sent to the internal XGMII/GMII/MII bus. The packets received from the internal XGMII/GMII/MII bus are ignored during line loopback. This allows the link partner to receive its own frames.

Before enabling the line loopback feature, the PHY must first establish link to another PHY link partner. If Auto-Negotiation is enabled, then both link partners should advertise the same speed and full duplex. If Auto-Negotiation is disabled, then both link partners must be forced to the same speed and full duplex. When link is established, the line loopback mode can be enabled setting register 3.8002.5 to 1 for 10M/100M/1G modes and 1.C000.11 to 1 for 2.5G/5G mode.

If MAC loopback 3.0000.14 is set to 1, then the line loopback registers 3.8002.5 and 1.C000.11 are ignored.

Figure 19: Line Loopback Diagram — Copper Media Interface



4.3 Power Management

The T Unit supports several advanced power management modes that conserve power.

4.3.1 Manual Power Down

The T Unit can be manually powered down by setting register 1.0000.11 or 3.0000.11 to 1. In general, this bit should not be set unless there is a need to only power down the T Unit.

When the device is operating in modes that does not require the T Unit to be operational, the T Unit will be powered down automatically regardless of the setting in register 1.0000.11 or 3.0000.11.

4.3.2 Energy Detect

The T Unit can be placed in energy detect power down modes by selecting either of the two Energy Detect modes. Both modes enable the PHY to wake up on its own by detecting activity on the media interface. The status of the Energy Detect is reported in register 3.8008.4 and the Energy Detect changes are reported in register 3.8011.4.

4.3.2.1 Energy Detect (Mode 1)

Energy Detect (Mode 1) is entered by setting register 3.8000.9:8 to 10.

In Mode 1, only the signal detection circuitry and register are active. If the PHY detects energy on the line, then it starts to Auto-Negotiate sending FLPs for 5 seconds. If at the end of 5 seconds the Auto-Negotiation is not completed, then the PHY stops sending FLPs and goes back to monitoring receive energy. If Auto-Negotiation is completed, then the PHY goes into normal operation. If during normal operation the link is lost, the PHY will restart Auto-Negotiation. If no energy is detected after 5 seconds, then the PHY resumes monitoring receive energy.

4.3.2.2 Energy Detect +™ (Mode 2)

Energy Detect (Mode 2) is entered by setting register 3.8000.9:8 to 11.

In Mode 2, the PHY sends out a single 10 Mbps Normal Link Pulse (NLP) every one second. Except for this difference, Mode 2 is identical to Mode 1 operation. If the T Unit is in Mode 1, then it cannot wake up a connected device; so, the connected device must be transmitting NLPs or either device must be woken up through register access. If the T Unit is in Mode 2, then it can wake a connected device.

4.4 Auto-Negotiation

The PHY supports IEEE 802.3 Clauses 28, 40, and 55 Auto-Negotiation. The PHY also supports proprietary extensions to the Auto-Negotiation protocol.

4.4.1 802.3 Clause 28, 40, and 55 Auto-Negotiation

The 10/100/1000/2.5G/5GBASE-T Auto-Negotiation (AN) is based on Clauses 28, 40, 55, and 126 of the IEEE 802.3 specification. It is also based on the NBASE-T Physical Layer Specification. It is used to negotiate speed, duplex, and flow control. When Auto-Negotiation is initiated, the PHY determines whether the remote device has Auto-Negotiation capability: if so, the PHY and the remote device negotiate the speed and duplex with which to operate.

If the remote device does not have Auto-Negotiation capability, then the PHY uses the parallel detect function to determine the speed of the remote device for 100BASE-TX and 10BASE-T modes. If link is established based on the parallel detect function, then it is required to establish link at half-duplex mode only. Refer to IEEE 802.3 Clauses 28, 40, 55, and 126 for a full description of Auto-Negotiation.

The 10/100/1000/2.5G/5GBASE-T Auto-Negotiation can be enabled and disabled via register 7.0000.12. Auto-Negotiation must be enabled if the PHY is intended to operate in 1000BASE-T, 2.5GBASE-T, or 5GBASE-T. Furthermore, the extended next page control bit (7.0000.13) must also be set to 1 if the PHY is intended to operate in 2.5GBASE-T and 5GBASE-T.

Auto MDI/MDIX and Auto-Negotiation may be disabled and enabled independently.

When Auto-Negotiation is disabled, the speed and duplex can be set via registers 1.0000.13, 1.0000.6, and 7.8000.4, respectively. Changes to any of these bits will take effect immediately when Auto-Negotiation is disabled.

When Auto-Negotiation is enabled the abilities that are advertised can be changed via registers 7.0010, 7.0020, and 7.8000.9:8. Changes to these registers do not take effect upon a copper link drop, changes take effect only after one of the following occurs:

- Software reset (1.0000.15, 3.0000.15, or 7.0000.15).
- Restart Auto-Negotiation (7.0000.9).
- Transition from power down to power up (1.0000.11 or 3.0000.11).
- Auto-Negotiation Enable bit toggles (7.0000.12).
- Extended Next Page Enable bit toggles (7.0000.13).
- Speed and Duplex toggles while Auto-Negotiation is disabled (1.0000.13, 1.0000.6, and 7.8000.4).

Registers 7.0010, 7.0020, and 7.8000.9:8 are internally latched once every time the Auto-Negotiation enters the Ability Detect state in the arbitration state machine only following one of the previously listed events. So a write into registers 7.0010, 7.0020, and 7.8000.9:8 has no effect when the PHY begins to transmit Fast Link Pulses (FLPs). This guarantees that sequences of FLPs transmitted are consistent with one another.

If 1000BASE-T, 2.5GBASE-T, or 5GBASE-T modes are advertised, then the PHY automatically sends the appropriate next pages or extended next page to advertise the capability and negotiate master/slave mode of operation. If the user does not select to transmit additional next pages or extended next pages, then the next page bit (7.0010.15) can be set to zero (default) and no further action is required from the user.

If either next pages or extended next pages are required in addition to those selected, or 1000BASE-T, 2.5GBASE-T, or 5GBASE-T, then the user can set register 7.0010.15 to one. Additional next pages can be transmitted and received via registers 7.0016 and 7.0019, respectively. Additional extended next pages can be transmitted and received via registers 7.0016, 7.0017, 7.0018 and 7.0019, 7.001A, and 7.001B, respectively.

1000BASE-T next page exchanges 2.5GBASE-T and 5GBASE-T extended next page exchanges are automatically handled by the PHY without user intervention, regardless of whether additional next pages are sent.

When the PHY completes Auto-Negotiation, it updates the various status in registers 7.0001, 7.0013, 7.8000, and 7.8001. Various Auto-Negotiation statuses such as speed, duplex, page received, and so on are also available in registers 3.8008 and 3.8011.

Clause 45 defines a 16-bit address space and protocol for 10G PHY management registers. The device supports the Clause 45 protocol and address space. Some of the 10M/100M/1G management register bits have an equivalent defined by IEEE 802.3 within the Clause 45 address space. However, there are also 10M/100M/1G management registers that are not defined by IEEE 802.3 within the Clause 45 address space. In the device these management register bits are mapped into 7.8000, 7.8001, and 7.8002.

The changes in Auto-Negotiation settings via MDIO registers will not take into effect (including a link down event) until Auto-Negotiation restart is initiated.

4.4.2 Exchange Complete — No Link Indicator

Sometimes when link does not come up, it is difficult to determine whether the failure is due to the Auto-Negotiation FLP not completing or from the 10/100/1000/2.5G/5GBASE-T link not being able to come up.

Register 3.8011.3 is a latched high bit that gets set to 1 whenever the FLP exchange is completed but the link cannot be established for some reason. When the bit is set, it can be cleared only by reading the register.

This bit will not be set if the FLP exchange is not completed or if link is established.

4.5 Auto Downshift

The auto downshift feature will downshift to the next highest available speed when a link fails to be established after several attempts to link. Failure to link can be caused by cabling issues such as using long CAT 5 cabling for 5GBASE-T or using cable with two twisted pairs instead of four twisted pairs. In either of the case, the Auto-Negotiation will repeatedly negotiate to the higher speed but fail to link.

With the NBASE-T downshift feature enabled, the T Unit is able to Auto-Negotiate with another link partner using cable pairs 1, 2 and 3, 6 to downshift, and link to the next highest advertised speed common between the two PHYs.

By default, the downshift feature is enabled. Setting register 1.C034.4 to 0 will disable the auto downshift feature.

Registers 1.C034 and 1.C035 specify the amount of attempts to link to 5GBASE-T, 2.5GBASE-T, and 1000BASE-T, respectively before down shifting to the next highest available speed. The number of attempts before downshift is (1.C034.[3:0]+1). So the default setting of 2 means NBASE-T downshift occurs after 3 link failures at current resolved speed. During the process of NBASE-T downshift, the number of attempts already performed is shown in the status register 1.C035.[12:9] which gets reset at next link up. Downshift for 100BASE-T and 10BASE-T are not supported.

When the lowest available speed fails to link after the programmed number of attempts, the PHY will restart the algorithm and attempt to link at the highest available speed.

4.6 Auto MDI/MDIX Crossover

The T Unit automatically determines whether it must cross over between pairs as shown in Table 42 so that an external crossover cable is not required. If the T Unit interoperates with a device that cannot automatically correct for crossover, the T Unit makes the necessary adjustment prior to commencing Auto-Negotiation. If the T Unit interoperates with a device that implements MDI/MDIX crossover, then a random algorithm as described in IEEE 802.3 Clause 40.4.4 determines which device performs the crossover.

When the T Unit interoperates with legacy 10BASE-T devices that do not implement Auto-Negotiation, the T Unit follows the same algorithm as previously described since link pulses are present. However, when interoperating with legacy 100BASE-TX devices that do not implement Auto-Negotiation (such as when link pulses are not present), the T Unit uses signal detect to determine whether to crossover.

The auto MDI/MDIX crossover function can be disabled via register 3.8000.6:5.

The pin mapping in MDI and MDIX modes is shown in Table 42.

Table 42: Media Dependent Interface Pin Mapping

Pin	MDI			MDIX		
	1000/2.5G/ 5GBASE-T	100BASE-TX	10BASE-T	1000/2.5G/ 5GBASE-T	100BASE-TX	10BASE-T
MDIP/N[0]	BI_DA±	TX±	TX±	BI_DB±	RX±	RX±
MDIP/N[1]	BI_DB±	RX±	RX±	BI_DA±	TX±	TX±
MDIP/N[2]	BI_DC±	unused	unused	BI_DD±	unused	unused
MDIP/N[3]	BI_DD±	unused	unused	BI_DC±	unused	unused

Note

Table 42 assumes no crossover on PCB.

The MDI/MDIX status is indicated by register 3.8008.6. This bit indicates whether the signal pairs (3, 6) and (1, 2) are crossed over. In 5GBASE-T, 2.5GBASE-T, and 1000BASE-T operation, the device can also correct for crossover between pairs (4, 5) and (7, 8). However, this is not indicated by register 3.8008.6.

4.7 Auto Polarity Correction

The T Unit automatically corrects polarity errors on the receive pairs in 5GBASE-T, 2.5GBASE-T, 1000BASE-T and 10BASE-T modes. In 100BASE-TX mode, the polarity does not matter.

In 5GBASE-T, 2.5GBASE-T, and 1000BASE-T modes, auto polarity correction is always enabled, receive polarity errors are automatically corrected based on the startup training sequence. When the training is complete the polarity is locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

If a 1000BASE-T, 2.5GBASE-T, or 5GBASE-T link is established, register 1.0082.11:8 (2.5G/5G) and 3.8182.11:8 (1G) report the polarity on all 4 pairs.

In 10BASE-T mode, auto polarity correction is enabled when register 3.8000.1 is set to 0. If register 3.8000.1 is set to 1, then the polarity will be forced to normal. When enabled, polarity errors are corrected based on the detection of validly spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10BASE-T link is up. The polarity becomes unlocked when link is down.

The 10BASE-T polarity correction status is indicated by register 3.8008.1. This bit indicates whether the receive pair (3, 6) is polarity reversed in MDI mode of operation. In the MDIX mode of operation, the receive pair is (1, 2) and register 3.8008.1 indicates whether this pair is polarity reversed. Although all pairs are corrected for receive polarity reversal, register 3.8008.1 only indicates polarity reversal on the pairs described above.

The 10BASE-T receive polarity can be forced to negative by setting register 3.8001.9 to 1. This is useful for debugging and should not be used during normal operation.

5 Host Interface Unit (H Unit)

The host side interface comprises two differential input lanes SIP[1:0]/SIN[1:0] and two differential output lanes SOP[1:0]/SON[1:0]. They are designed to operate over short backplanes to the host device.

These lanes can be arranged to form SGMII, 1000BASE-X, 2500BASE-X, and 5GBASE-R.

5.1 Host Electrical Interface

The input and output buffers of the SERDES interface are internally terminated by 50Ω impedance (100Ω differential). No external terminations are required.

The SERDES transmitter has a three-tap (1 pre-tap and 1 post-tap) FIR filter for channel equalization. The FIR tap can be manually adjusted to optimize the transmit eye over a particular channel.

The receiver performs clock and data recovery and de-serializes the data.

The polarity of the H Unit inputs and outputs can be inverted.

4.F004.15 inverts Lane3 input polarity: 0 = Normal, 1 = Invert

4.F004.14 inverts Lane2 input polarity: 0 = Normal, 1 = Invert

4.F004.13 inverts Lane 1 input polarity: 0 = Normal, 1 = Invert

4.F004.12 inverts Lane 0 input polarity: 0 = Normal, 1 = Invert

4.F004.11 inverts Lane3 output polarity: 0 = Normal, 1= Invert

4.F004.10 inverts Lane2 output polarity: 0 = Normal, 1= Invert

4.F004.9 inverts Lane 1 output polarity: 0 = Normal, 1 = Invert

4.F004.8 inverts Lane 0 output polarity: 0 = Normal, 1 = Invert

Note

Lane 1 is only applicable when MACTYPE[2:0] = 000, 001, 010, or 011. See Section 3.4, Configuration and Resets, on page 65 for MACTYPE[2:0] configuration details.

5.2 PCS

The Host Interface supports several different PCS. Register 31.F001.2:0 determines the behavior of the host interface as shown in Table 43 and Table 44.

Table 43: 88E2010 Host Interface Configuration

	Line Rate				
31.F001.2:0	**5 Gbps**	**2.5 Gbps**	**1 Gbps**	**100 Mbps**	**10 Mbps**
000	5GBASE-R	2500BASE-X	SGMII Auto-Negotiation On		
–	Reserved				
–	Reserved				
011	5GBASE-R	2500BASE-X	SGMII Auto-Negotiation On		
100	5GBASE-R	2500BASE-X	SGMII Auto-Negotiation On		
101	5GBASE-R	2500BASE-X	SGMII Auto-Negotiation Off		
110	5GBASE-R/2500BASE-X				
111	Reserved				

Table 44: 88E2040L Host Interface Configuration

	Line Rate				
31.F001.2:0	**5 Gbps**	**2.5 Gbps**	**1 Gbps**	**100 Mbps**	**10 Mbps**
000	5GBASE-R	2500BASE-X	SGMII Auto-Negotiation On		
001	5GBASE-R	2500BASE-X	SGMII Auto-Negotiation Off		
010	Reserved				
011	Reserved				
100	5GBASE-R	2500BASE-X	SGMII Auto-Negotiation On		
101	5GBASE-R	2500BASE-X	SGMII Auto-Negotiation Off		
110	5GBASE-R/2500BASE-X				
111	Reserved				

5.2.1 5GBASE-R/2500BASE-X

The 5GBASE-R/2500BASE-X PCS is enabled by setting register 31.F001.2:0 = 001 (88E2010 only), 010, 110, or 111.

The 5GBASE-R/2500BASE-X PCS operates according to Clause 49 of the IEEE 802.3ae specification. The PCS uses a 64B/66B coding and scrambling to improve the transmission characteristics of the serial data and ease clock recovery at the receiver. The synchronization headers for 64B/66B code enable the receiver to achieve block alignment on the receive data. For further details, refer to the IEEE 802.3 specification.

5.2.2 5GBASE-R

For the 88E2040L devices, the 5GBASE-R PCS is enabled by setting register 31.F001.2:0 = 000, 001, 100, 101, and the line rate is 5 Gbps.

For the 88E2010 device, the 5GBASE-R PCS is enabled by setting register 31.F001.2:0 = 000, 011, 100, 101, and the line rate is 5 Gbps.

5GBASE-R is identical to 5GBASE-R/2500BASE-X as described in Section 5.2.1, 5GBASE-R/2500BASE-X except at 50% speed.

5.2.3 2500BASE-X

For the 88E2040L device the 2500BASE-X PCS is enabled by setting register 31.F001.2:0 = 000, 001, 100, 101, and the line rate is 2.5 Gbps.

For the 88E2010 device, the 2500BASE-X PCS is enabled by setting register 31.F001.2:0 = 000, 011, 100, 101, and the line rate is 2.5 Gbps.

2500BASE-X is identical to 1000GBASE-X operation as described in Section 5.2.4.1, PCS except at 2.5 times the speed. Auto-Negotiation is not supported in 2500BASE-X.

5.2.4 SGMII (Media)

For the 88E2040L device, the SGMII is enabled by setting register 31.F001.2:0 = 000, 001, 100, 101, and the line rate is 10/100/1000 Mbps. SGMII Auto-Negotiation is enabled with the 000 and 100 settings.

For the 88E2010 device, the SGMII is enabled by setting register 31.F001.2:0 = 000, 011, 100, 101, and the line rate is 10/100/1000 Mbps. SGMII Auto-Negotiation is enabled with the 000, 011 and 100 settings.

5.2.4.1 PCS

The 1000BASE-X PCS operates according to Clause 36 of the IEEE 802.3 specification. The PCS uses a 8/10 bit coding for DC line balancing. For further details, refer to the IEEE 802.3 specification.

The SGMII protocol is also supported over 1000BASE-X. The SGMII allows 10 Mbps, 100 Mbps, and 1000 Mbps throughput over 1000BASE-X line coding.

When SGMII Auto-Negotiation is turned off (4.2000.12 = 0), the speed setting is programmed via register 4.2000 bits 13 and 6. Link is established when the underlying 1000BASE-X establishes link.

When SGMII Auto-Negotiation is turned on (4.2000.12 = 1), the SGMII is set to the speed of the line interface. This speed capability is advertised and Auto-Negotiation has to complete prior to link being established.

5.2.4.2 SGMII Auto-Negotiation

SGMII is a de-facto standard designed by Cisco. SGMII uses 1000BASE-X coding to send data as well as Auto-Negotiation information between the PHY and the MAC. However, the contents of the SGMII Auto-Negotiation are different than the 1000BASE-X Auto-Negotiation. See the *Cisco SGMII Specification* and the *MAC Interfaces and Auto-Negotiation Application Note* for further details.

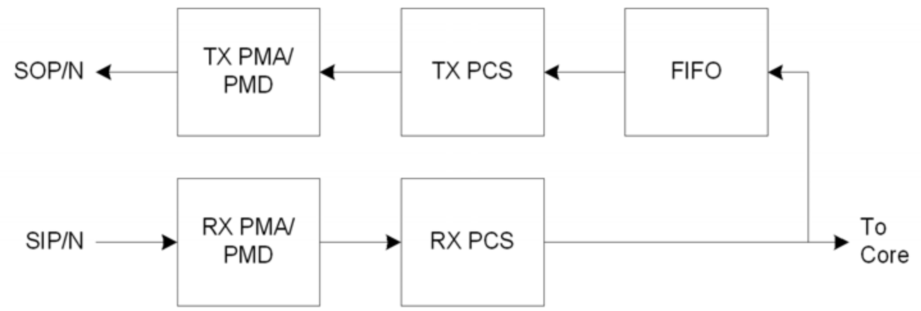
The device supports SGMII interface with and without Auto-Negotiation. Auto-Negotiation can be enabled or disabled by writing to register 4.2000.12. If SGMII Auto-Negotiation is disabled, then the MAC interface link, speed, and duplex status (determined by the media side) cannot be conveyed to the MAC from the PHY. The user must program the MAC with this information in some other way (for example, by reading PHY registers for link, speed, and duplex status).

5.3 Loopback

The host-side SERDES support two loopback paths.

If register 4.F003.12 = 1, then data from the host will loopback to the host as shown in Figure 20.

Figure 20: Shallow Host Loopback



Registers 4.0000.14, 4.1000.14, and 4.2000.14 are physically the same bit. If any of these bits are set to 1, then data from the core will loopback to the core as shown in Figure 21 and Figure 22. If register 4.F003.6, then the ingress path will not be blocked as shown in Figure 21. If register 4.F003.6 = 1, then the ingress path will be blocked as shown in Figure 22.

Figure 21: Deep Line Loopback, No Ingress Blocking

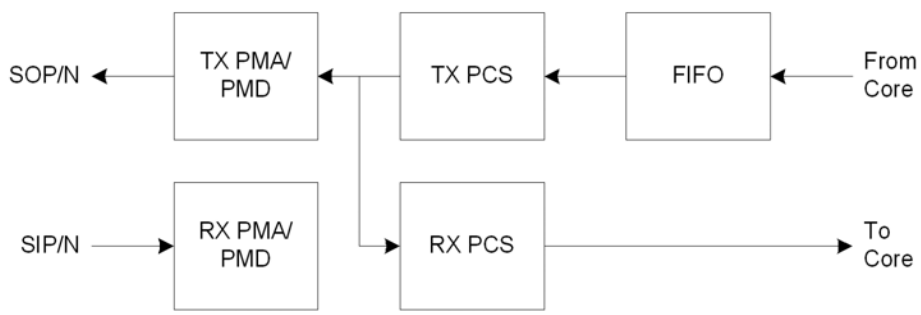
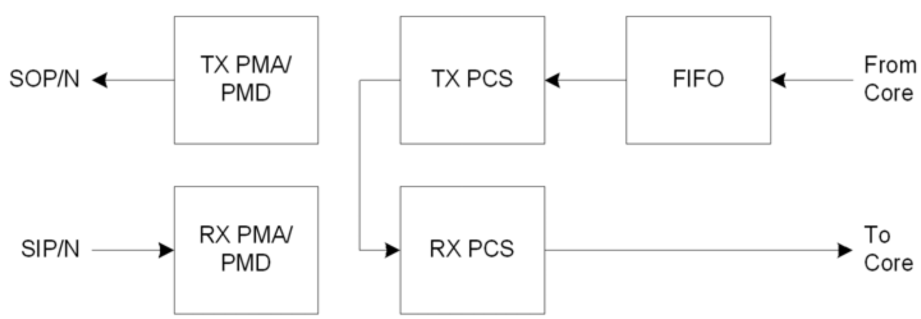


Figure 22: Deep Line Loopback, Ingress Blocking



5.4 Power Management

The device will automatically power down unused circuits. The host side can be forced into a power down state by setting 4.0000.11, 4.1000.11, or 4.2000.11. These power down registers are physically the same bit even though they reside in different locations.

To soft reset the host side only, set registers 4.0000.15, 4.1000.15, or 4.2000.15. These software reset registers are physically the same bit even though they reside in different locations.

6 Electrical Specifications

6.1 Absolute Maximum Ratings

Table 45: Absolute Maximum Rating

Stresses above those listed in Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Symbol	Parameter	Min	Typ	Max	Units
V_{DDAC}	Power Supply Voltage on AVDDC with respect to VSS	-0.5	–	2.5	V
V_{DDAL}	Power Supply Voltage on AVDDL with respect to VSS	-0.5	–	2.5	V
V_{DDAH}	Power Supply Voltage on AVDDH with respect to VSS	-0.5	–	2.5	V
V_{DDAT}	Power Supply Voltage on AVDDT with respect to VSS	-0.5	–	3.0	V
V_{DDAR}	Power Supply Voltage on AVDDR with respect to VSS	-0.5	–	2.5	V
V_{DDAS}	Power Supply Voltage on AVDDS with respect to VSS	-0.5	–	2.5	V
V_{DD}	Power Supply Voltage on DVDD with respect to VSS	-0.5	–	1.2	V
V_{DDO}	Power Supply Voltage on VDDOL, VDDOM, VDDOR, VDDOT with respect to VSS	-0.5	–	3.6	V
V_{HV}	Power Supply Voltage on VHV with respect to VSS	-0.5	–	1.2	V
V_{PIN}	Voltage Applied to Any Digital Input Pin	-0.5	–	3.6	V
$T_{STORAGE}$[a]	Storage Temperature	-55	–	+125[b]	°C

a. The conditions for storing unpowered and unmounted devices are as follows:
- Packed inside a vacuum-sealed moisture barrier bag with desiccant and humidity indicator card (HIC)
- Stored at <40°C and <90% relative humidity (RH)

b. 125°C is only used as bake temperature for not more than 24 hours. Long-term storage (for example, weeks or longer) should be kept at 85°C or lower.

6.2 Recommended Operating Conditions

Table 46: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DDAC}[a, b]	AVDDC Supply	For AVDDC	1.455	1.5	1.545	V
V_{DDAL}[1, 2]	AVDDL Supply	For AVDDL	1.455	1.5	1.545	V
V_{DDAH}[1, 2]	AVDDH Supply	For AVDDH	1.940	2.0	2.060	V
			1.746	1.8	1.854	V
V_{DDAT}[1, 2]	AVDDT Supply	For AVDDT	2.425	2.5	2.575	V
			2.231	2.3	2.396	V
V_{DDAR}[1, 2]	AVDDR Supply	For AVDDR	1.455	1.5	1.545	V
V_{DDAS}[1, 2]	AVDDS Supply	For AVDDS	1.455	1.5	1.545	V
V_{DD}[1, 2]	DVDD Supply	For DVDD (C-temp)	0.776	0.8	0.824	V
		For DVDD (I-temp)	0.854	0.88	0.906	V
V_{DDO}[1, 2]	VDDOL, VDDOM, VDDOR, VDDOT Supply	For VDDOM at 1.2V	1.14	1.2	1.26	V
		For VDDO* at 1.5V	1.425	1.5	1.575	V
		For VDDO* at 1.8V	1.71	1.8	1.89	V
		For VDDO* at 2.5V	2.375	2.5	2.625	V
		For VDDO* at 3.3V	3.135	3.3	3.465	V
V_{HV}[1, 2]	VHV Supply	Leave floating	–	–	–	V
IREF	Internal Bias Reference CIREF, SIREF	Resistor connected to V_{SS}	–	4.99K ±1% Tolerance	–	Ω
T_A	Commercial Ambient Operating Temperature	Commercial Parts[c]	0	–	70	°C
		Industrial Parts[d]	-40	–	85	°C
T_J	Maximum Junction Temperature		–	–	105[e]	°C

a. Maximum noise allowed on supplies is 25 mV peak-peak.
b. The recommended operating conditions assume that the ripple is included. DC operating conditions with the ripple should never exceed the recommended operating levels. For example, on a system: DVDD supply - 12.5 mV (ripple peak) should be less than 0.776V.
c. Commercial operating temperatures are typically below 70°C, for example, 45°C~55°C. The 70°C maximum is the Marvell specification limit.
d. Industrial part numbers have an *I* following the commercial part numbers. For details, see Section 8.1, Part Order Numbering, on page 143.
e. Refer to the white paper on T_J Thermal Calculations for detailed information.

6.3 Package Thermal Information

6.3.1 Thermal Conditions for 88E2010, 168-pin, HFCBGA Package

Table 47: Thermal Conditions for 88E2010, 168-pin, HFCBGA Package

Symbol	Parameter	Condition	Min	Typ	Max	Units
θ_{JA}	Thermal Resistance[a] - Junction to Ambient for the 168-pin, HFCBGA Package $\theta_{JA} = (T_J - T_A)/P$ P = Total Power Dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow	–	19.56	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow	–	16.90	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow	–	15.42	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow	–	14.35	–	°C/W
ψ_{JT}	Thermal Characteristic Parameter[a] - Junction to the Top Center of the 168-pin, HFCBGA Package $\psi_{JT} = (T_J - T_{top})/P$. P = Total Power Dissipation, $T_{top:}$ Temperature on the Top Center of the Package	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow	–	0.21	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow	–	0.24	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow	–	0.26	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow	–	0.28	–	°C/W
θ_{JC}	Thermal Resistance[a] -Junction to the Case for the 168-pin, HFCBGA Package $\theta_{JC} = (T_J - T_C)/P_{top}$ P_{top} = Power Dissipation from the Top of the Package	JEDEC with no air flow	–	0.66	–	°C/W
θ_{JB}	Thermal Resistance[a] - Junction to the Board for the 168-pin, HFCBGA Package $\theta_{JB} = (T_J - T_B)/P_{bottom}$ P_{bottom} = Power Dissipation from the Bottom of the Package to the PCB Surface	JEDEC with no air flow	–	8.18	–	°C/W

a. Refer to the white paper on T_J Thermal Calculations for detailed information.

6.3.2 Thermal Conditions for 88E2040L, 484-pin, HFCBGA Package

Table 48: Thermal Conditions for 88E2040L, 484-pin, HFCBGA Package

Symbol	Parameter	Condition	Min	Typ	Max	Units
θ_{JA}	Thermal Resistance[a] - Junction to Ambient for the 484-pin, HFCBGA Package $\theta_{JA} = (T_J - T_A)/P$ P = Total Power Dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow	–	9.09	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow	–	7.85	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow	–	7.27	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow	–	6.88	–	°C/W
ψ_{JT}	Thermal Characteristic Parameter[a] - Junction to the Top Center of the 484-pin, HFCBGA Package $\psi_{JT} = (T_J - T_{top})/P$ P = Total Power Dissipation, $T_{top:}$ Temperature on the Top Center of the Package	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow	–	0.16	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow	–	0.25	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow	–	0.28	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow	–	0.30	–	°C/W
θ_{JC}	Thermal Resistance[a] - Junction to the Case for the 484-pin, HFCBGA Package $\theta_{JC} = (T_J - T_C)/P_{top}$ P_{top} = Power Dissipation from the Top of the Package	JEDEC with no air flow	–	0.30	–	°C/W
θ_{JB}	Thermal Resistance[a] - Junction to the Board for the 484-pin, HFCBGA Package $\theta_{JB} = (T_J - T_B)/P_{bottom}$ P_{bottom} = Power Dissipation from the Bottom of the Package to the PCB Surface	JEDEC with no air flow	–	2.60	–	°C/W

a. Refer to the white paper on T_J Thermal Calculations for information.

6.4 Digital I/O Electrical Specifications

6.4.1 DC Operating Conditions

Table 49: DC Operating Conditions

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
VIH	Input High Voltage	All digital inputs	VDDO = 3.3V	2.0	–	VDDO + 0.3V	V
			VDDO = 2.5V	1.75	–	VDDO + 0.3V	V
			VDDO = 1.8V	1.26	–	VDDO + 0.3V	V
			VDDO = 1.5V	1.05	–	VDDO + 0.3V	V
			VDDO = 1.2V	0.84	–	VDDO + 0.3V	V
VIL	Input Low Voltage	All digital inputs	VDDO = 3.3V	-0.3	–	0.8	V
			VDDO = 2.5V	-0.3	–	0.75	V
			VDDO = 1.8V	-0.3	–	0.54	V
			VDDO = 1.5V	-0.3	–	0.45	V
			VDDO = 1.2V	-0.3	–	0.36	V
VOH	High-level Output Voltage	All digital outputs	IOH = -4 mA	VDDO - 0.4V	–	–	V
VOL	Low-level Output Voltage	All digital outputs	IOL = 4 mA	–	–	0.4	V
I_{ILK}	Input Leakage Current	With internal pull-up/pull-down resistor	–	10	–	70	µA
		All others without resistor	–	–	–	10	µA
I_{LED}	Max Current per LED Pin	All LED pins	–	–	–	8	mA
CIN	Input Capacitance	All pins	–	–	–	5	pF

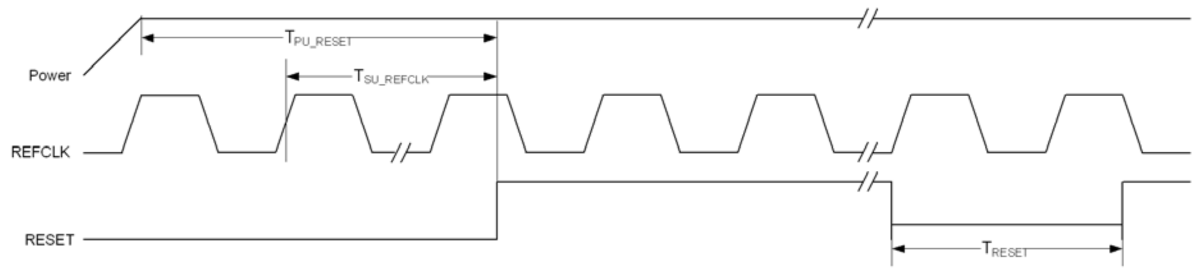
6.4.2 Reset Timing

Table 50: Reset Timing

(Over Full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{PU_RESET}	Valid Power to RESET De-asserted	–	10	–	–	ms
T_{SU_REFCLK}	Number of Valid REFCLK Cycles Prior to RESET De-asserted	–	10	–	–	clks
T_{RESET}	Minimum Reset Pulse Width During Normal Operation	–	10	–	–	ms

Figure 23: Reset Timing

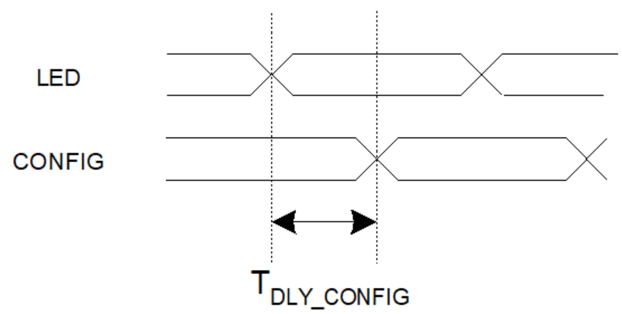


6.4.3 LED to CONFIG Timing

Table 51: LED to CONFIG Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{DLY_CONFIG}	LED to CONFIG Delay	–	0	–	25	ns

Figure 24: LED to CONFIG Timing



6.4.4 MDC/MDIO Management Interface Timing

Table 52: MDC/MDIO Management Interface Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
T_{DLY_MDIO}	MDC-to-MDIO (Output) Delay Time	2	–	16	ns
$T_{SU\_ MDIO}$	MDIO- (Input) to-MDC Setup Time	3	–	–	ns
$T_{HD\_ MDIO}$	MDIO- (Input) to-MDC Hold Time	3	–	–	ns
$T_{P\_ MDC}$	MDC Period	35	–	–	ns
$T_{H\_ MDC}$	MDC High	17	–	–	ns
$T_{L\_ MDC}$	MDC Low	17	–	–	ns
V_{HYST}	VDDO Input Hysteresis	–	360	–	mV
$T_{P\_ MDC}$	MDC Period	35	–	–	ns
T_{read_dly}	Read Delay	160	–	–	ns

Figure 25: MDC/MDIO Management Interface Timing

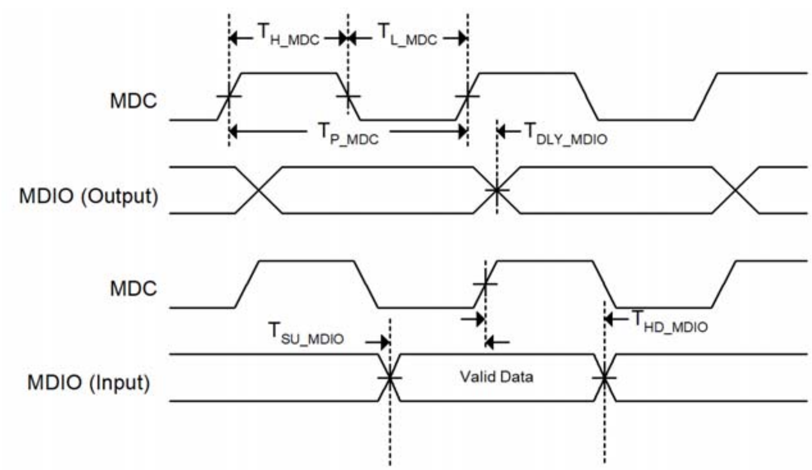


Figure 26: MDC/MDIO Input Hysteresis

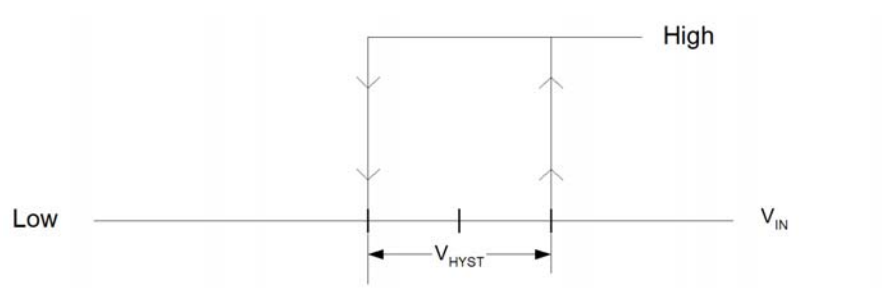
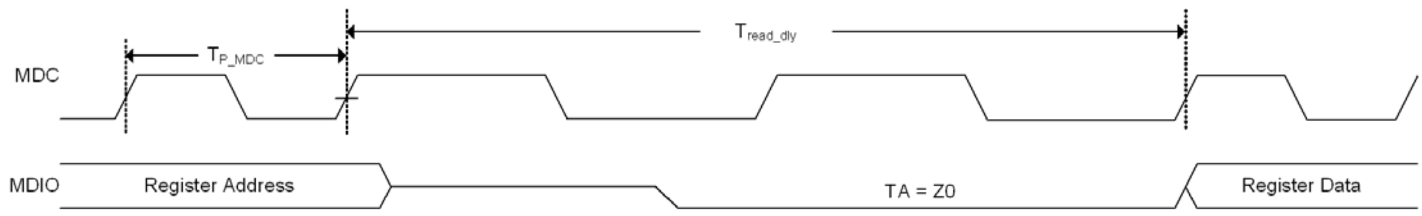


Figure 27: MDC Read Turnaround Delay

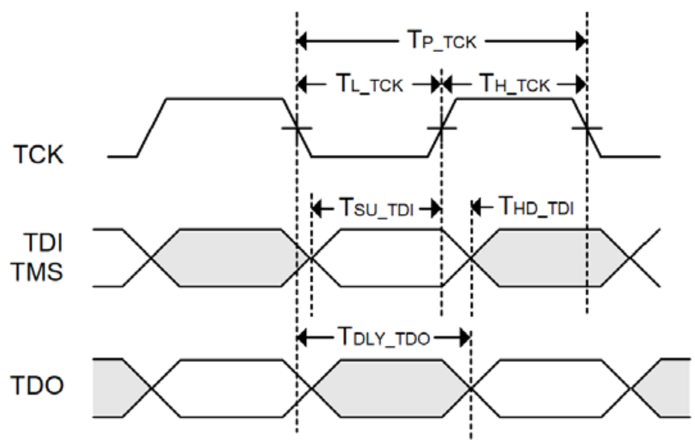


6.4.5 JTAG Timing

Table 53: JTAG Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{P_TCK}	TCK Period	–	60	–	–	ns
T_{H_TCK}	TCK High	–	12	–	–	ns
T_{L_TCK}	TCK Low	–	12	–	–	ns
T_{SU_TDI}	TDI, TMS-to-TCK Setup Time	–	10	–	–	ns
T_{HD_TDI}	TDI, TMS-to-TCK Hold Time	–	10	–	–	ns
T_{DLY_TDO}	TCK-to-TDO Delay	–	0	–	15	ns

Figure 28: JTAG Timing



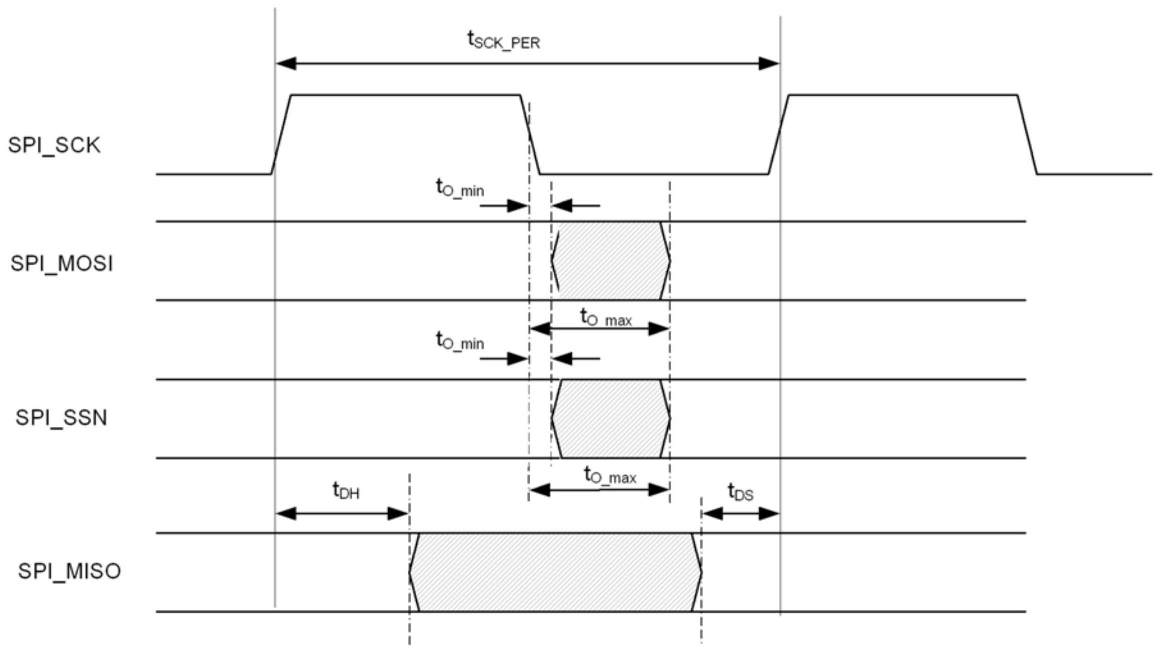
6.4.6 SPI Interface Timing

Table 54: SPI Interface Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{SCK_PER}	SCK Period	–	–	204.8	–	ns
	SCK Duty Cycle	–	48	50	52	%
T_{O_min} to T_{O_max}	MOSI Valid from SCK Low	–	0	–	20	ns
T_{DH}	MISO Hold Time from SCK High	–	0	–	–	ns
T_{DS}	MISO Setup Time to SCK High	–	50	–	–	ns

Figure 29: SPI Interface Timing



6.5 Analog Electrical Specifications

6.5.1 SGMII Electrical Summary

Table 55: SGMII Electrical Summary

Test Parameters	Specification			Units
	Transmitter Tests			
	Min	Mean	Max	
Output Voltage High	–	–	1525	mV
Output Voltage Low	875	–	–	mV
Output Ringing	–	–	10	%
Output Differential Voltage	150	–	400	mV
Output Offset Voltage	1.075	–	–	V
Single-ended Output Impedance	40	–	–	Ω
Output Current On Short to Gnd	–	–	40	mA
Output Current When P and N are Shorted	–	–	12	mA
Power Off Leakage Current	–	–	10	mA
Skew Between P and N	–	–	20	ps
Total Output Jitter	–	–	300	ps
Receiver Tests				
Sensitivity	–	–	100	mVpp
Single-ended Termination	–	50	–	Ω
Jitter Tolerance	500	–	–	ps

6.5.2 2500BASE-X Electrical Summary

Table 56: 2500BASE-X Electrical Summary

Test Parameters	Specification			Units
	Transmitter Tests			
	Min	Mean	Max	
Signaling Rate	-100 ppm	3.125	+100 ppm	GBaud
Nominal Unit Interval	–	320	–	ps
Differential Output	800	1000	1200	mVpp
Deterministic Jitter	–	–	0.17	UI
Random Jitter	–	–	0.27	UI
Total Output Jitter	–	–	0.35	UI
Receiver Tests				
Signaling Rate	-100 ppm	3.125	+100 ppm	GBaud
Nominal Unit Interval	–	320	–	ps
Differential Input Peak-to-Peak Amplitude	–	–	1600	mVpp
Applied Sinusoidal Jitter (Min. Peak-to-Peak)	0.17	–	–	UI
Applied Random Jitter (Min. Peak-to-Peak)	0.18	–	–	UI

6.5.3 5GBASE-R Electrical Summary

Table 57: 5GBASE-R Electrical Summary

Test Parameters	Specification			Units
	Transmitter Tests			
	Min	Mean	Max	
Signaling Rate	-100 ppm	3.125	+100 ppm	GBaud
Nominal Unit Interval	–	193.9	–	ps
Differential Output	–	–	1200	mVpp
Deterministic Jitter	–	–	0.12	UI
Random Jitter	–	–	0.15	UI
Total Output Jitter	–	–	0.27	UI
Receiver Tests				
Signaling Rate	-100 ppm	3.125	+100 ppm	GBaud
Nominal Unit Interval	–	193.9	–	ps
Applied Random Jitter (Min. Peak-to-Peak)	0.15	–	–	UI
	5 UI @ 0.02 MHz	–	–	N/A
	0.15 UI @ 4 MHz	–	–	
Applied Sinusoidal Jitter (Min. Peak-to-Peak)	0.15 UI @ 20 MHz	–	–	

6.5.4 10BASE-Te, 100BASE-TX, and 1000BASE-T Electrical Parameters

IEEE tests are typically based on template and cannot simply be specified by a number. For an exact description of the template and the test conditions, refer to the IEEE specifications.

- 10BASE-Te IEEE 802.3 Clause 14
- 100BASE-TX ANSI X3.263-1995
- 1000BASE-T IEEE Clause 40

Table 58: IEEE DC Transceiver Parameters

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
V_{ODIFF}	Absolute Peak Differential Output Voltage	MDIP/N[1:0]	10BASE-Te no cable	1.54	–	1.96	V
		MDIP/N[1:0]	10BASE-Te cable model	585[a]	–	–	mV
		MDIP/N[1:0]	100BASE-TX mode	0.950	–	1.050	V
		MDIP/N[3:0]	1000BASE-T[b]	0.67	–	0.82	V
	Overshoot[2]	MDIP/N[1:0]	100BASE-TX mode	0	–	5	%
	Amplitude Symmetry (Positive/ Negative)	MDIP/N[1:0]	100BASE-TX mode	98	–	102	V+/V-
V_{IDIFF}	Peak Differential Input Voltage	MDIP/N[1:0]	10BASE-Te mode	585[c]	–	–	mV
	Signal Detect Assertion	MDIP/N[1:0]	100BASE-TX mode	1000	460[d]	–	mV peak-peak
	Signal Detect De-assertion	MDIP/N[1:0]	100BASE-TX mode	200	360[e]	–	mV peak-peak

a. IEEE 802.3 Clause 14, Figure 14.9 shows the template for the far-end wave form. This template allows as little as 495 mV peak differential voltage at the far end receiver.
b. IEEE 802.3ab Figure 40 -19 points A&B.
c. The input test is actually a template test; IEEE 802.3 Clause 14, Figure 14.17 shows the template for the receive waveform.
d. The ANSI TP-PMD specification requires that any received signal with peak-to-peak differential amplitude greater than 1000 mV should turn on signal detect (internal signal in 100BASE-TX mode). The device accepts signals typically with 460 mV peak-to-peak differential amplitude.
e. The ANSI-PMD specification requires that any received signal with peak-to-peak differential amplitide less than 200 mV should de-assert signal detect (internal signal in 100BASE-TX mode). The device will reject signals typically with peak-to-peak differential amplitude less than 360 mV.

6.5.5 IEEE DC Transceiver Parameters

IEEE tests are typically based on template and cannot simply be specified by a number. For an exact description of the template and the test conditions, refer to the IEEE specifications.
-10BASE-T IEEE 802.3 Clause 14
-100BASE-TX ANSI X3.263-1995

Table 59: IEEE DC Transceiver Parameters
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
V_{ODIFF}	Absolute Peak Differential Output Voltage	MDIP/N[1:0]	10BASE-T no cable	0.950	1.0	1.050	V
		MDIP/N[1:0]	10BASE-T cable model	585[a]	–	–	mV
		MDIP/N[1:0]	100BASE-TX mode	0.950	1.0	1.050	V
		MDIP/N[3:0]	1000BASE-T[b]	0.67	0.75	0.82	V
	Overshoot[2]	MDIP/N[1:0]	100BASE-TX mode	0	–	5%	V
	Amplitude Symmetry (Positive/ Negative)	MDIP/N[1:0]	100BASE-TX mode	0.98x	–	1.02x	V+/V-
V_{IDIFF}	Peak Differential Input Voltage	MDIP/N[1:0]	10BASE-T mode	585[c]	–	–	mV
	Signal Detect Assertion	MDIP/N[1:0]	100BASE-TX mode	100	460[d]	–	mV peak-peak
	Signal Detect De-assertion	MDIP/N[1:0]	100BASE-TX mode	200	360[e]	–	mV peak-peak

a. IEEE 802.3 Clause 14, Figure 14.9 shows the template for the far-end waveform. This template allows as little as 495 mV peak differential voltage at the far end receiver.
b. IEEE 802.3ab Figure 40 -19 points A&B.
c. The input test is actually a template test; IEEE 802.3 Clause 14, Figure 14.17 shows the template for the receive wave form.
d. The ANSI TP-PMD specification requires that any received signal with peak-to-peak differential amplitude greater than 1000 mV should turn on signal detect (internal signal in 100BASE-TX mode).
e. The ANSI-PMD specification requires that any received signal with peak-to-peak differential amplitide less than 200 mV should de-assert signal detect (internal signal in 100BASE-TX mode). The device will reject signals typically with peak-to-peak differential amplitude less than 360 mV.

6.6 Reference Clock

6.6.1 CLKP/N Timing — 156.25 MHz

Table 60: CLKP/N Timing — 156.25 MHz

Symbol	Parameter	Condition	Min	Typ	Max	Units
Fclk	Frequency	–	-50 ppm	156.25	+50 ppm	MHz
tr, tf	Rise, Fall Time	20 to 80% of swing	0.3	0.5	0.8	ns
A	Amplitude	Differential pk	0.4	0.75	0.9	V
Tduty	Duty Cycle	–	0.45	0.5	0.55	–
Tj	Jitter	Integrated from 1 to 30 MHz	–	–	0.5	ps, (RMS)
Zin	Input Impedance	Differential	90	100	110	Ω
Vicm	Input CM	CLK can be DC coupled.	0.1	–	AVDDC - 0.1V	V
SDD11	Input Return Loss	Differential, 100Ω	–	–	-12	db

Note

When the transmitter or the receiver is in LPI transmit mode or switching to and from the LPI mode, a short-term rate of frequency variation will be less than 0.1 ppm/second.

6.6.2 CLKP/N Timing — 50 MHz

Table 61: CLKP/N Timing — 50 MHz

Symbol	Parameter	Condition	Min	Typ	Max	Units
Fclk	Frequency	–	-50 ppm	50	+50 ppm	MHz
tr, tf	Rise, Fall Time	20 to 80% of swing	0.3	0.5	0.8	ns
A	Amplitude	Differential pk-pk	0.4	0.75	0.9	V
Tduty	Duty Cycle	–	0.45	0.5	0.55	–
Tj	Jitter	Integrated from 1 to 30 MHz	–	–	0.5	ps, (RMS)
Zin	Input Impedance	Differential	90	100	110	Ω
Vicm	Input CM	CLK can be DC coupled.	0.1	–	AVDDC - 0.1V	V
SDD11	Input Return Loss	Differential, 100Ω	–	–	-12	db

6.6.3 XTAL Timing[a] Data

Table 62: XTAL Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

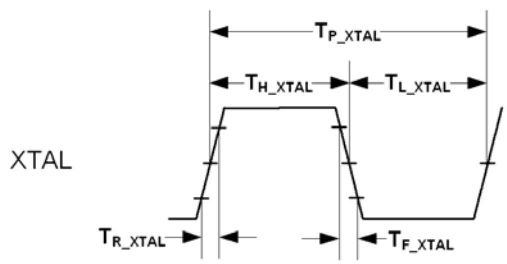
Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{P_XTAL}	XTAL Period	–	20 -50 ppm	20	20 +50 ppm	ns
T_{H_XTAL}	XTAL High Time	–	6.5	10	13.5	ns
T_{L_XTAL}	XTAL Low Time	–	6.5	10	13.5	ns
T_{R_XTAL}	XTAL Rise	10 to 90%	–	2.0	–	ns
T_{F_XTAL}	XTAL Fall	90 to 10%	–	2.0	–	ns
T_{J_XTAL}	XTAL Total Jitter[b]	–	–	–	200	ps

a. If the crystal option is used, then ensure that the frequency is 50 MHz ±50 ppm. Capacitors must be chosen carefully - see the application note supplied by the crystal vendor.
b. PLL-generated clocks are not recommended as input to XTAL since they can have excessive jitter. Zero delay buffers are also not recommended for the same reason.

Note

50 MHz crystal operation is only supported for commercial-grade devices.

Figure 30: XTAL Timing



6.7 Latency

The total latency in the egress direction is T_{EGRESS} + T_{EGRESS_HL} + T_{CORE}. The total latency in the ingress direction is $T_{INGRESS}$ + T_{CORE}. If the high latency mode is not used, then the TCORE and T_{EGRESS_HL} are 0, respectively.

Table 63: Egress Path Latency[a b c d] Data

Symbol	Condition (per Port, Line to Host)	Min	Typ	Max	Unit
T_{EGRESS}	Reserved to 5GBASE-T	1,698	1,713	1,740	ns
	Reserved to 2.5GBASE-T	2,727	2,753	2,802	ns
	Reserved to 1000BASE-T	358	385	423	ns
	Reserved to 1000BASE-X/SGMII-1000	318	367	428	ns
	Reserved to 100BASE-T	2,381	2,552	2,814	ns
	Reserved to 10BASE-T	19,542	21,157	23,593	ns
	5GBASE-R to 5GBASE-T	1,716	1,731	1,752	ns
	2500BASE-X to 2.5GBASE-T	2,746	2,765	2,804	ns
	1000BASE-X/SGMII-1000 to 1000BASE-T	271	302	332	ns
	1000BASE-X/SGMII-1000 to 1000BASE-X	231	284	337	ns
	SGMII to 100BASE-TX	1,143	1,174	1,298	ns
	SGMII to 10BASE-T	6,192	6,290	6,428	ns

a. Latency numbers are based on default ppm FIFO depth = 01 in both egress and ingress direction.
b. The packet size used for ingress side RM FIFO simulation is 1512+4 (CRC) bytes per packet.
c. Low latency enabled
d. T_{EGRESS_HL} @5G = 625 ns, T_{EGRESS_HL} @2.5G = 1,875 ns, and others = 0 ns

Table 64: Ingress Path Latency[a b c d] Data

Symbol	Condition (per Port, Line to Host)	Min	Typ	Max	Unit
$T_{INGRESS}$	5GBASE-T to Reserved	1,394	1,415	1,449	ns
	2.5GBASE-T to Reserved	2,625	2,664	2,726	ns
	1000BASE-T to Reserved	521	556	602	ns
	1000BASE-X/SGMII-1000 to Reserved	412	461	522	ns
	100BASE-TX to Reserved	2,990	3,241	3,583	ns
	5GBASE-R/2500BASE-X to Reserved	125	135	150	ns
	5GBASE-T to 5GBASE-R	1,367	1,384	1,405	ns
	2500BASE-T to 2.5GBASE-X	2,541	2,587	2,626	ns
	1000BASE-T to 1000BASE-X/SGMII-1000	340	379	417	ns
	1000BASE-X to 1000BASE-X/SGMII-1000	231	284	337	ns
	100BASE-TX to SGMII	1,242	1,352	1,391	ns
	10BASE-T to SGMII	11,358	12,193	12,245	ns

a. Latency numbers are based on default ppm FIFO depth = 01 in both egress and ingress direction.
b. The packet size used for ingress side RM FIFO simulation is 1512+4 (CRC) bytes per packet.
c. Low latency enabled.
d. T_{EGRESS_HL} @5G = 625 ns, T_{EGRESS_HL} @2.5G = 1,875 ns, and others = 0 ns

7 Mechanical Drawing

7.1 168-pin 10 mm x 12 mm HFCBGA Package Mechanical Drawings

Figure 31: 168-pin 10 mm x 12 mm HFCBGA Top and Side View

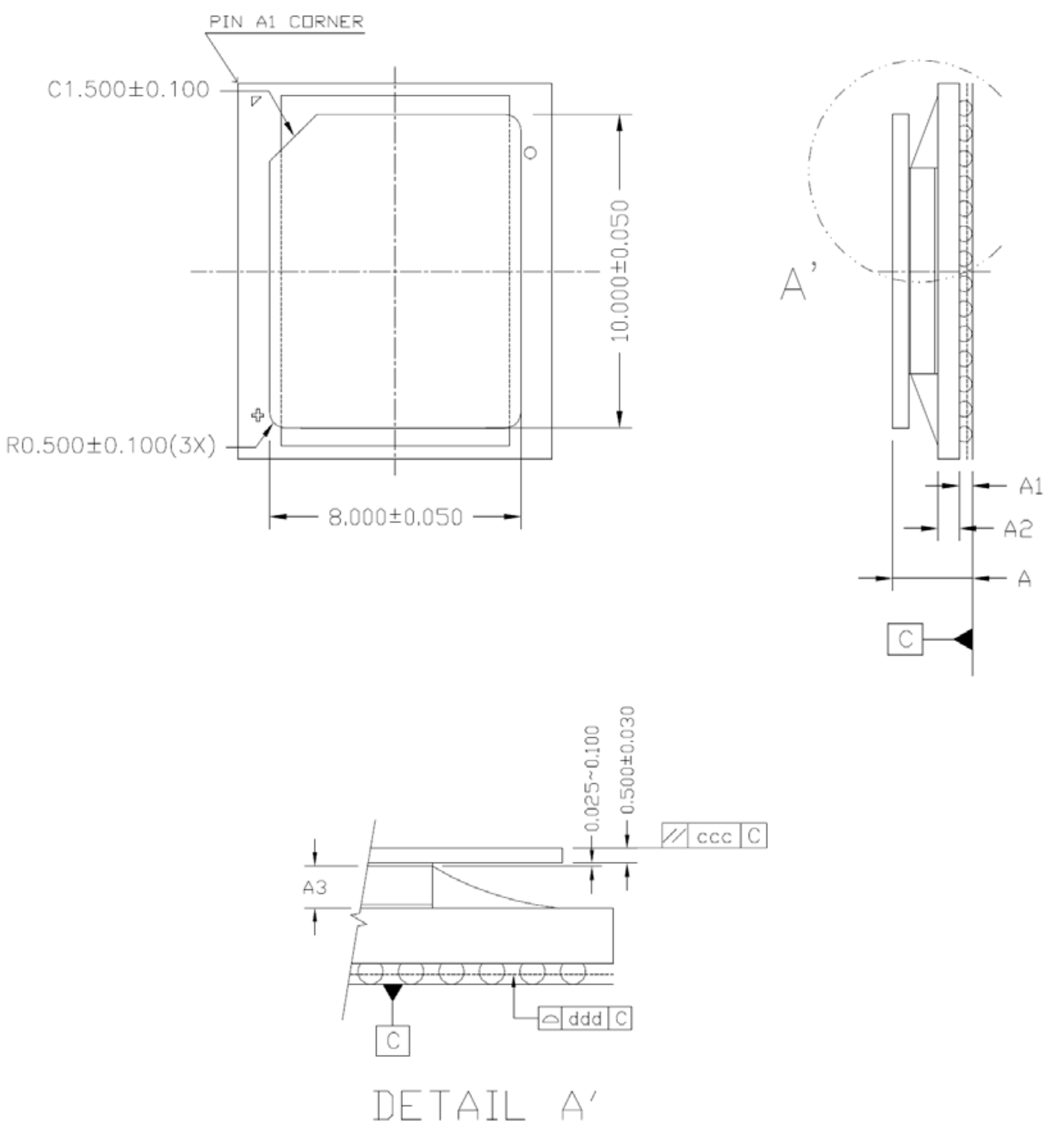


Figure 32: 168-pin 10 mm x 12 mm HFCBGA Bottom View

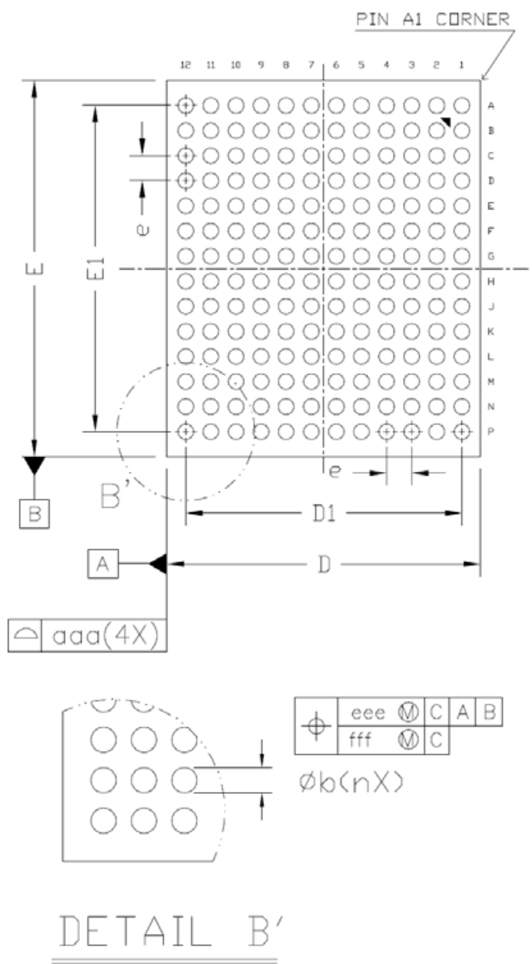
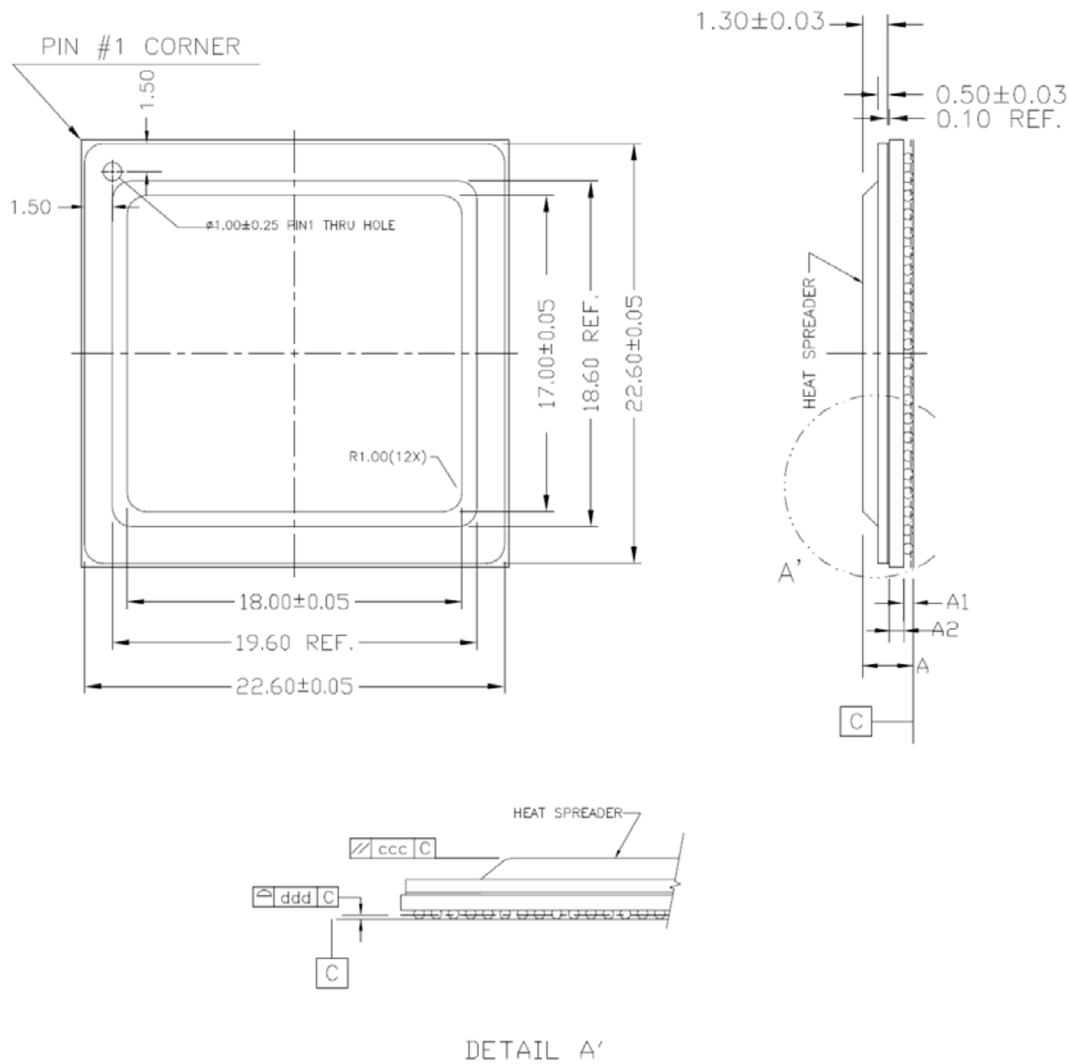


Table 65: 168-pin 10 mm x 12 mm HFCBGA Package Dimensions

	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOM.	MAX.
TOTAL THICKNESS	A	2.407	2.527	2.647
STAND OFF	A1	0.360	--	0.460
SUBSTRATE THICKNESS	A2	0.670 REF		
THICKNESS FROM SUBSTRATE SURFACE TO DIE BACKSIDE	A3	0.887 REF		
BODY SIZE	D	10.000 BSC		
	E	12.000 BSC		
BALL DIAMETER		0.500		
BALL WIDTH	b	0.440	--	0.640
BALL PITCH	e	0.800 BSC		
BALL COUNT	n	168		
EDGE BALL CENTER TO CENTER	D1	8.800 BSC		
	E1	10.400 BSC		
EXPOSE DIE SIZE	D2	--		
	E2	--		
PACKAGE EDGE TOLERANCE	aaa	0.100		
SUBSTRATE PARALLELISM	bbb	--		
TOP PARALLELISM	ccc	0.200		
COPLANARITY	ddd	0.150		
BALL OFFSET (PACKAGE)	eee	0.150		
BALL OFFSET (BALL)	fff	0.80		

7.2 484-pin 23 mm x 23 mm HFCBGA Package Mechanical Drawings

Figure 33: 484-pin 23 mm x 23 mm HFCBGA Top and Side View



Document Classification: Public

September 17, 2019

Figure 34: 484-pin 23 mm x 23 mm HFCBGA Bottom View

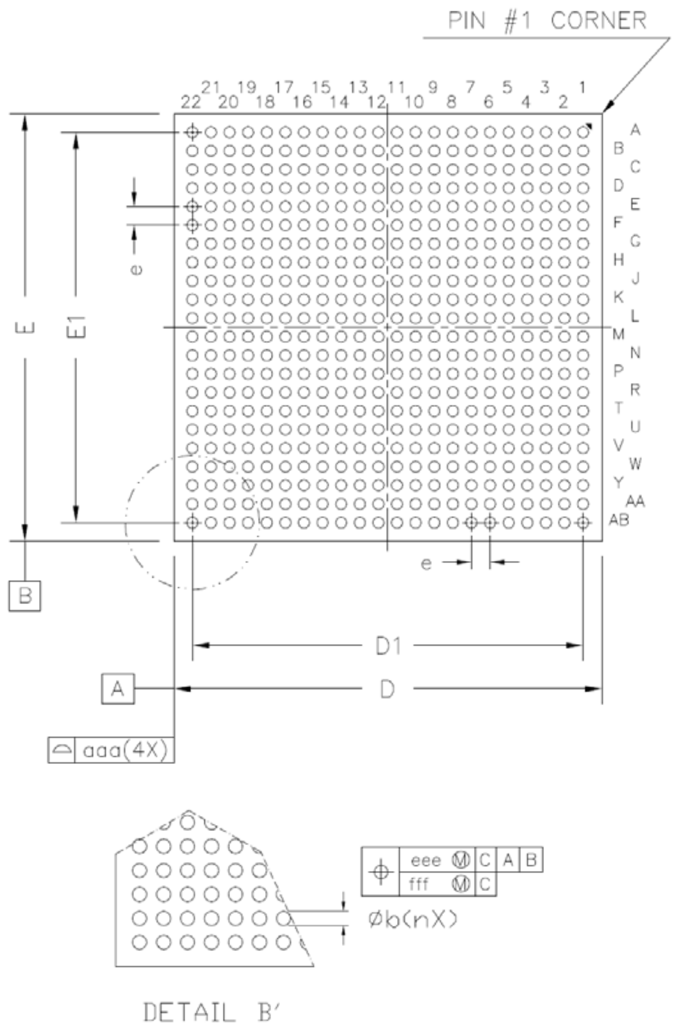


Table 66: 484-pin 23 mm x 23 mm HFCBGA Package Dimensions

	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOM.	MAX.
TOTAL THICKNESS	A	2.580	2.700	2.820
STAND OFF	A1	0.400	--	0.600
SUBSTRATE THICKNESS	A2	0.800 REF		
THICKNESS FROM SUBSTRATE SURFACE TO DIE BACKSIDE	A3	-- REF		
BODY SIZE	D	23.000 BSC		
	E	23.000 BSC		
BALL DIAMETER		0.600		
BALL WIDTH	b	0.500	--	0.700
BALL PITCH	e	1.000 BSC		
BALL COUNT	n	484		
EDGE BALL CENTER TO CENTER	D1	21.000 BSC		
	E1	21.000 BSC		
EXPOSE DIE SIZE	D2	--		
	E2	--		
PACKAGE EDGE TOLERANCE	aaa	0.100		
SUBSTRATE PARALLELISM	bbb	--		
TOP PARALLELISM	ccc	0.200		
COPLANARITY	ddd	0.150		
BALL OFFSET (PACKAGE)	eee	0.150		
BALL OFFSET (BALL)	fff	0.100		

8 Part Order Numbering/Package Marking

This section includes information on the following topics:

- Section 8.1, Part Order Numbering
- Section 8.2, Package Marking

8.1 Part Order Numbering

Figure 35 shows the ordering part numbering scheme for the 88E2010/88E2040L devices. Contact Marvell FAEs or sales representatives for complete ordering information.

Figure 35: Sample Part Number

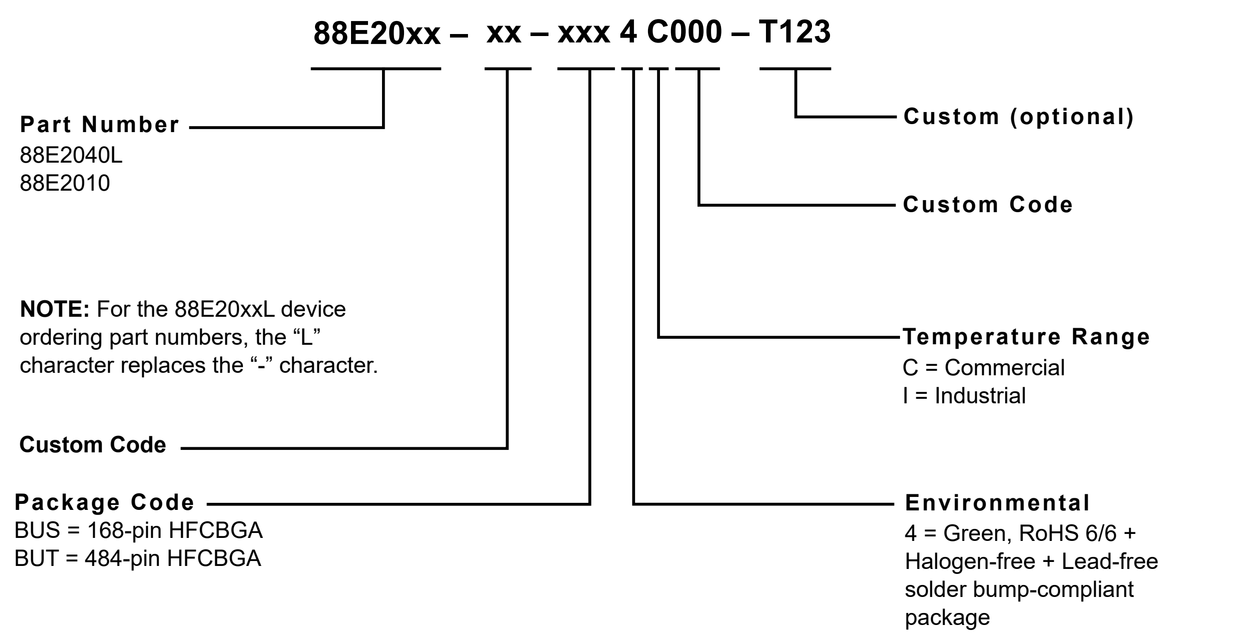


Table 67: 88E2010/88E2040L Commercial Part Order Options

Part Number	Package Type	Part Order Number
88E2010	168-pin 10 mm x 12 mm HFCBGA- Commercial, Green, RoHS 6/6 + Halogen-free + Lead-free solder bump-compliant	88E2010-XX-BUS4C000
88E2040L	484-pin 23 mm x 23 mm HFCBGA - Commercial, Green, RoHS 6/6 + Halogen-free + Lead-free solder bump-compliant	88E2040LXX-BUT4C000

Table 68: 88E2010/88E2040L Industrial Part Order Options

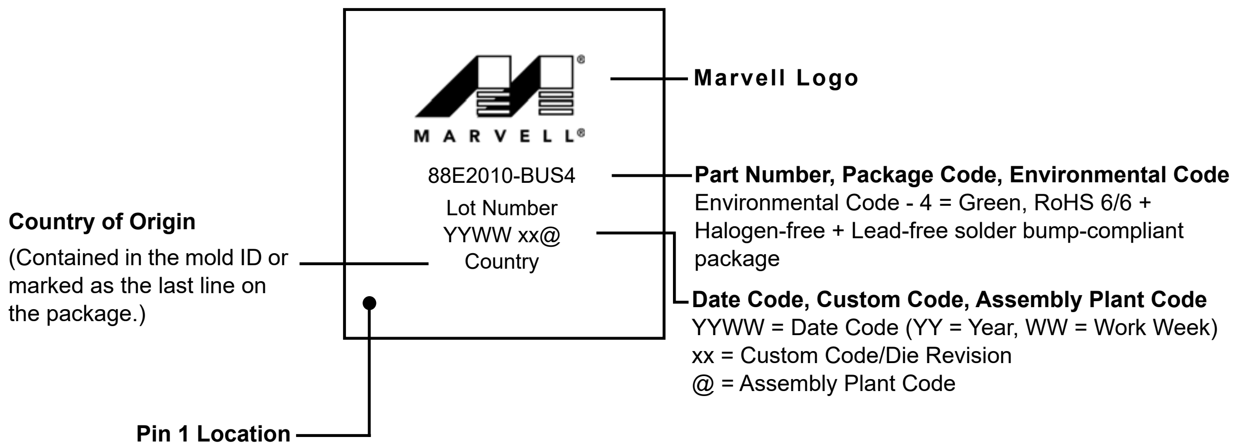
Part Number	Package Type	Part Order Number
88E2010	168-pin 10 mm x 12 mm HFCBGA- Commercial, Green, RoHS 6/6 + Halogen-free + Lead-free solder bump-compliant	88E2010-XX-BUS4I000
88E2040L	484-pin 23 mm x 23 mm HFCBGA - Commercial, Green, RoHS 6/6 + Halogen-free + Lead-free solder bump-compliant	88E2040LXX-BUT4I000

8.2 Package Marking

8.2.1 Commercial Marking Examples

Figure 36 is an example of the package marking and pin 1 location for the 88E2010 package.

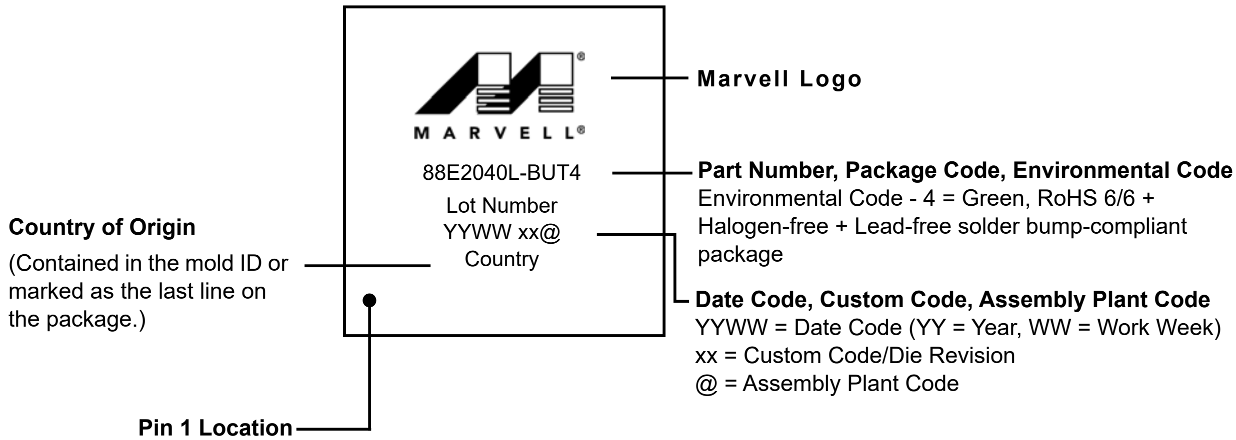
Figure 36: 88E2010 Commercial Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

Figure 37 is an example of the package marking and pin 1 location for the 88E2040L package.

Figure 37: 88E2040L Commercial Package Marking and Pin 1 Location

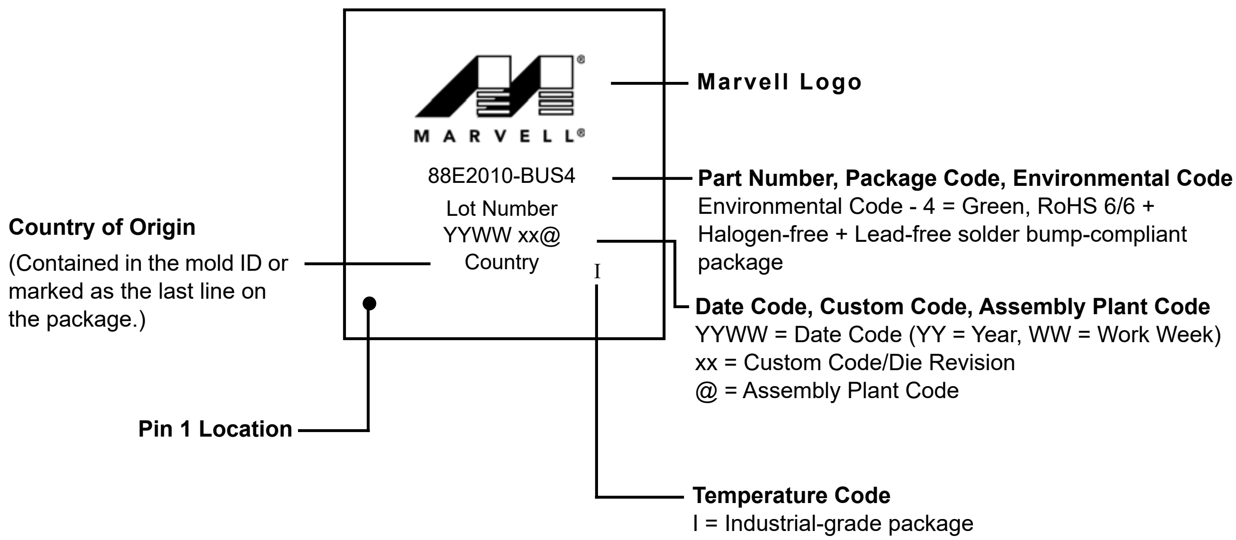


Note: The above example is not drawn to scale. Location of markings is approximate.

8.2.2 Industrial Marking Examples

Figure 38 is an example of the package marking and pin 1 location for the 88E2010 package.

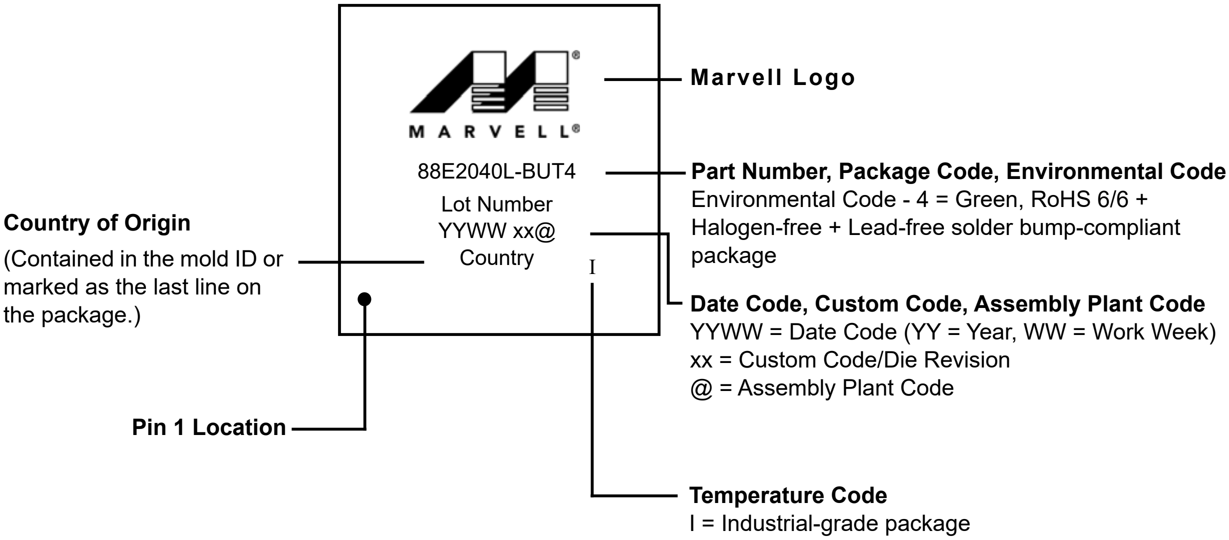
Figure 38: 88E2010 Industrial Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

Figure 39 is an example of the package marking and pin 1 location for the 88E2040L package.

Figure 39: 88E2040L Industrial Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

A Revision History

Table 69: Document Change History

Revision	Date	Section	Detail
Rev. C	September 17, 2019	Revision C released.	
Rev. C 3.01		Section 7, Mechanical Drawing	• Figure 31, 168-pin 10 mm x 12 mm HFCBGA Top and Side View, on page 137 updated. • Figure 32, 168-pin 10 mm x 12 mm HFCBGA Bottom View, on page 138 updated. • Table 65, 168-pin 10 mm x 12 mm HFCBGA Package Dimensions, on page 139 updated. • Figure 33, 484-pin 23 mm x 23 mm HFCBGA Top and Side View, on page 140 updated. • Figure 34, 484-pin 23 mm x 23 mm HFCBGA Bottom View, on page 141 updated. • Table 66, 484-pin 23 mm x 23 mm HFCBGA Package Dimensions, on page 142 updated.
Rev. C 3.00	October 10, 2018	Entire document	• Styles and format updated.
Rev. B 2.08	September 10, 2018	Section 6, Electrical Specifications	• 6.5.1 "SGMII Electrical Summary" on page 127 updated. • 6.5.2 "2500BASE-X Electrical Summary" on page 128 updated. • 6.5.3 "5GBASE-R Electrical Summary" on page 129 updated. • 6.5.4 "10BASE-Te, 100BASE-TX, and 1000BASE-T Electrical Parameters" on page 130 updated. • 6.5.5 "IEEE DC Transceiver Parameters" on page 131 updated.
Rev. B 2.07	August 10, 2018	Entire document	• Styles and format updated.
Rev. B 2.06	August 2, 2018	Cover/Legal	• Legal disclaimer updated.
Rev. B 2.05	July 31, 2018	Section 2, Signal Description	• Table 13, 88E2010 Pin List — Alphabetical by Signal Name, on page 39 added.
		Section 3, Functional Description	• Table 20, Configuration Bit Definition, on page 67 updated.

Table 69: Document Change History (Continued)

Revision	Date	Section	Detail
Rev. B 2.04	May 25, 2018	Product Overview	• Features, on page 3 updated. • References to EEE, 802.3az, Long Reach, Clause 22, AVS, WOL, and GPIO removed.
		Section 2, Signal Description	• Table 2, Media Dependent Interface, on page 21 through Table 12, Power and Ground (Continued), on page 33 updated.
			• Table 10, Adaptive Voltage Scaling Interface (88E2010/P Device Only), on page 49 removed.
		Section 3, Functional Description	• 3.5.1 "Clause 45 MDIO Framing" on page 72 updated. • Table 25, Basic LED Status, on page 76 updated. • 3.8 “Wake On LAN (WOL)” on page 86 removed. • 3.9 “Long Reach Mode of Operation” on page 86 removed. • 3.13 “GPIO” on page 94, 3.13.1 “Enabling the GPIO Function” on page 94 and 3.13.3 “GPIO Interrupts” on page 94 removed. • 3.21 “Adaptive Voltage Scaling (AVS)” on page 134 removed.
		Section 4, Copper Unit (T Unit)	• 4.5 “Energy Efficient Ethernet” on page 140 removed. • 4.4.1 “802.3 Clause 28, 40, and 55 Auto-Negotiation” on page 102 removed.
		Section 6, Electrical Specifications	• Table 46, Recommended Operating Conditions, on page 118 updated.

Table 69: Document Change History (Continued)

Revision	Date	Section	Detail
Rev. B 2.03	April 24, 2018	Cover	• Updated title.
		Product Overview	• Features, on page 3, Figure 1, 88E2010 Top-level Block Diagram, on page 4 and Figure 2, 88E2040L Top-level Block Diagram, on page 5 updated.
		Section 1, General Chip Description	• General Chip Description, on page 13, Figure 3, 88E2010 Device Functional Block Diagram, on page 14 and Figure 3, 88E2010 Device Functional Block Diagram, on page 14 updated.
		Section 2, Signal Description	• 2.1.1 "88E2010 Device Pin Map" on page 18 and 2.1.2 "88E2040L Device Pin Map" on page 19 updated.
			• Table 2, Media Dependent Interface, on page 21, Table 3, SERDES Interface, on page 23, Table 4, Clock/Reset/Reference, on page 25, Table 5, Management Interface, on page 26, Table 6, SPI Interface, on page 27, and Table 7, LED, on page 28 updated.
			• Table 8, Configuration, on page 29, Table 9, JTAG Interface, on page 29, Table 10, Adaptive Voltage Scaling Interface (88E2010/P Device Only), on page 49, Table 10, Test Pins, on page 30, Table 11, Power and Ground, on page 32, and Table 12, Power and Ground (Continued), on page 33, and Table 13, 88E2010 Pin List — Alphabetical by Signal Name, on page 39 updated.
		Section 3, Functional Description	• Figure 5, Device Data Path (88E2040L), on page 54 and Figure 6, Device Data Path (88E2010), on page 55 updated.
			• 3.4 "Configuration and Resets" on page 65, 3.4.2 "Hardware Configuration" on page 65, 3.5.3 "Independent MDC/MDIO Support" on page 72, 3.6.2 "Firmware Download to RAM" on page 73, 3.7.1 "Manual Power Down" on page 73, and 3.7.3 "Controlling and Sensing" on page 74 updated.
			• Table 32, 88E2010 Boundary Scan Chain Order, on page 84 and Table 33, 88E2010 Boundary Scan Exclusion List, on page 86 updated.

Table 69: Document Change History (Continued)

Revision	Date	Section	Detail
Rev. B 2.02	April 23, 2018	Section 3, Functional Description	• Table 32, 88E2010 Boundary Scan Chain Order, on page 84 and Table 33, 88E2010 Boundary Scan Exclusion List, on page 86 updated.
			• 3.10.6 "ID CODE Instruction" on page 93 updated.
		Section 5, Host Interface Unit (H Unit)	• Host Interface Unit (H Unit), on page 111 updated. • 5.2 "PCS" on page 112 updated. • 5.2.1 "5GBASE-R/2500BASE-X" on page 112 updated. • 5.2.2 "5GBASE-R" on page 112 updated. • 5.2.3 "2500BASE-X" on page 113 updated. • 5.2.4 "SGMII (Media)" on page 113 updated.
		Section 6, Electrical Specifications	• 6.3.1 "Thermal Conditions for 88E2010, 168-pin, HFCBGA Package" on page 119 updated. • 6.3.2 "Thermal Conditions for 88E2040L, 484-pin, HFCBGA Package" on page 120 updated. • 6.7 "Latency" on page 135 updated.
		Section 8, Part Order Numbering/Package Marking	• Table 67, 88E2010/88E2040L Commercial Part Order Options, on page 143 and Table 68, 88E2010/88E2040L Industrial Part Order Options, on page 144 updated.
Rev. B 2.01	April 20, 2018	Initial datasheet draft.	

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