Marvell® Alaska® 88E2180/88E2110

Octal 10/100/1000/2.5G/5GBASE-T Ethernet Transceiver

Datasheet - Public

For CUSTOMER Use Only

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Preface

About this Document

This document provides a feature list and overview, pin description, functional description, mechanical drawings, electrical specifications, and order information for the 88E2180 and 88E2110.

Related Document

88E2181/88E2180/88E2111/88E2110 Register Description

This document (MV-S111371-00) provides a description of the registers for the 88E2181, 88E2180, 88E2111, and 88E2110 devices.

PRODUCT OVERVIEW

The Marvell® Alaska® M 88E2180 and 88E2110 are fully IEEE 802.3bz-compliant 1-port (88E2110) or 8-port (88E2180) physical layer (PHY) devices. The devices support a wide variety of host-side interfaces including 5GBASE-R, 2500BASE-X, and SGMII to support full backward compatibility with lower speed legacy Ethernet rates including 1 Gbps, 100 Mbps, and 10 Mbps.

The flexibility of the devices enable extremely low power across all structured wiring cable lengths, enabling dense 5 Gbps applications. The devices support Category 5e-, Category 6- (screened or unscreened), Category 6A- (Augmented), and Category 7-type cables for distances up to 100 meters.

FEATURES

- 1-port (88E2110 only), 5-speed PHY operating at 10M, 100M, 1G, 2.5G, or 5G data rates on UTP copper lines
- 8-port (88E2180 only), 5-speed PHY operating at 10M, 100M, 1G, 2.5G, or 5G data rates on UTP copper lines
- Compliant with both NBASE-T and IEEE 802.3bz specifications for 2.5G and 5G modes
- 5GBASE-R, 2500BASE-X (88E2180 and 88E2110 only), and SGMII system-side interfaces
- EEE for all supported data rates
- Allows dense multi-port 2.5G/5G applications
- BER less than 1E-15 (88E2180), better than 1E-15 (88E2110)
- 100m reach on Category 5e for
- Clause 22 and 45 MDC/MDIO management interface
- TWSI support (88E2110 only)
- Serial LED (88E2180 only)
- 19 mm x 19 mm HFCBGA package (88E2180)
- Small 7 mm x 11 mm FC-TFBGA package (88E2110)
- Available in commercial and industrial grades

Figure 1: 88E2180 Top-level Block Diagram

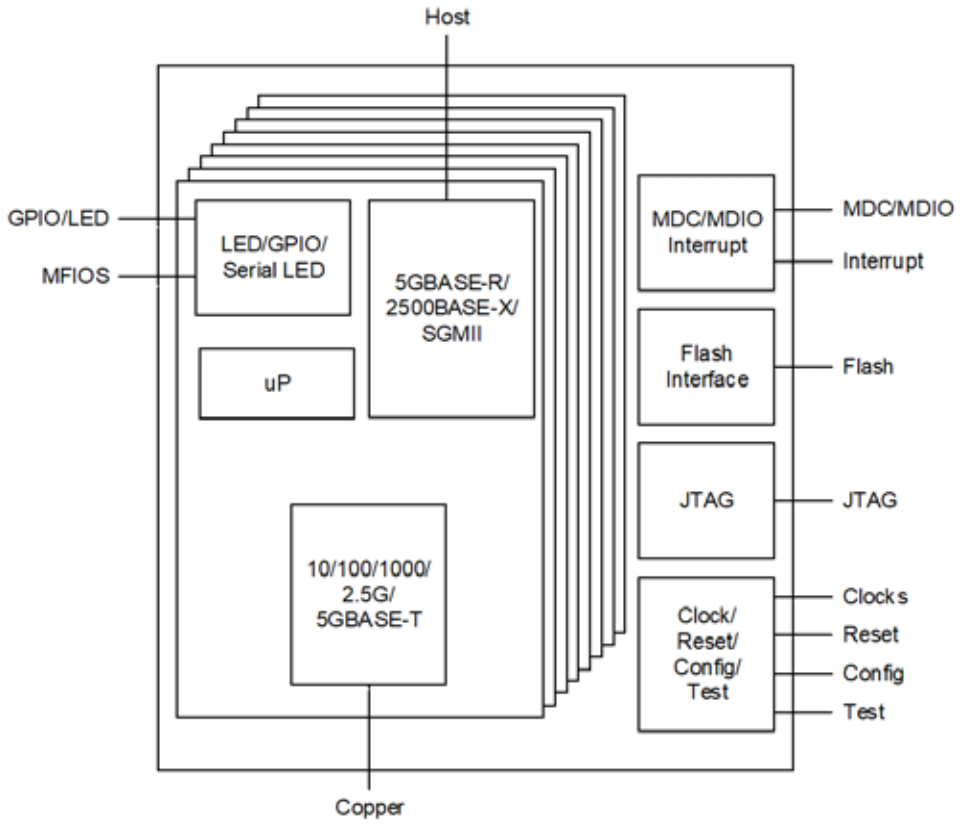
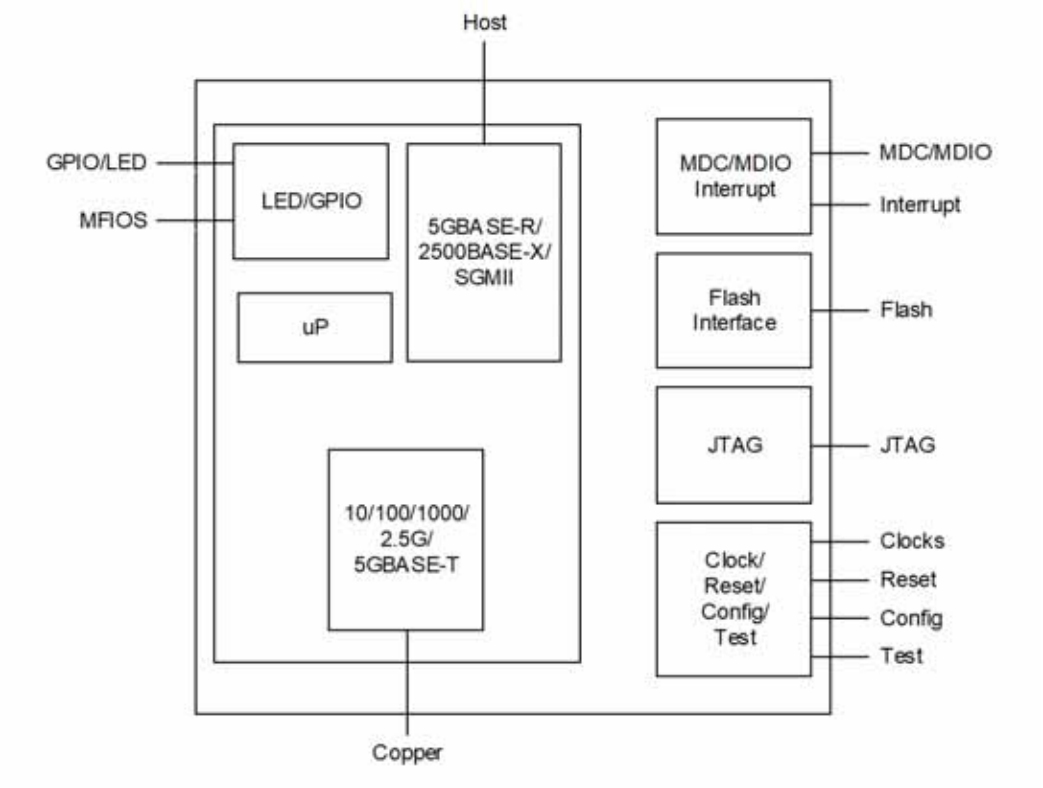
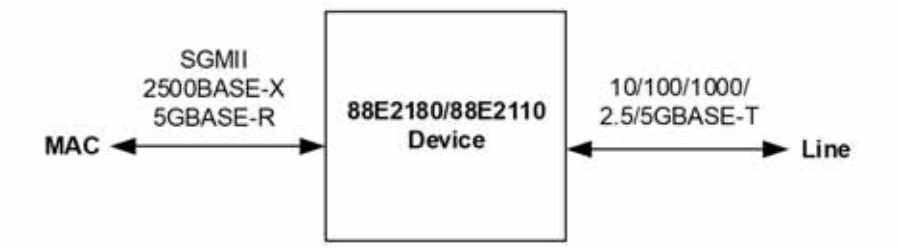


Figure 2: 88E2110 Top-level Block Diagram



CONFIGURATION OPTIONS

Figure 3: Device Application — Host Interface Speed Matched to Line Speed



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1 General Chip Description

The device is an eight-port (88E2180) or single-port (88E2110) integrated multi-speed copper Ethernet transceiver.

For the 88E2180/88E2110 device, the host interface to the MAC is via 5GBASE-R, 2500BASE-X, or SGMII.

Registers can be accessed through standard Clause 45 (or 22) MDC/MDIO or Two-wire Serial Interface (TWSI) for the 88E2110 device.

Figure 4: 88E2180 Device Functional Block Diagram

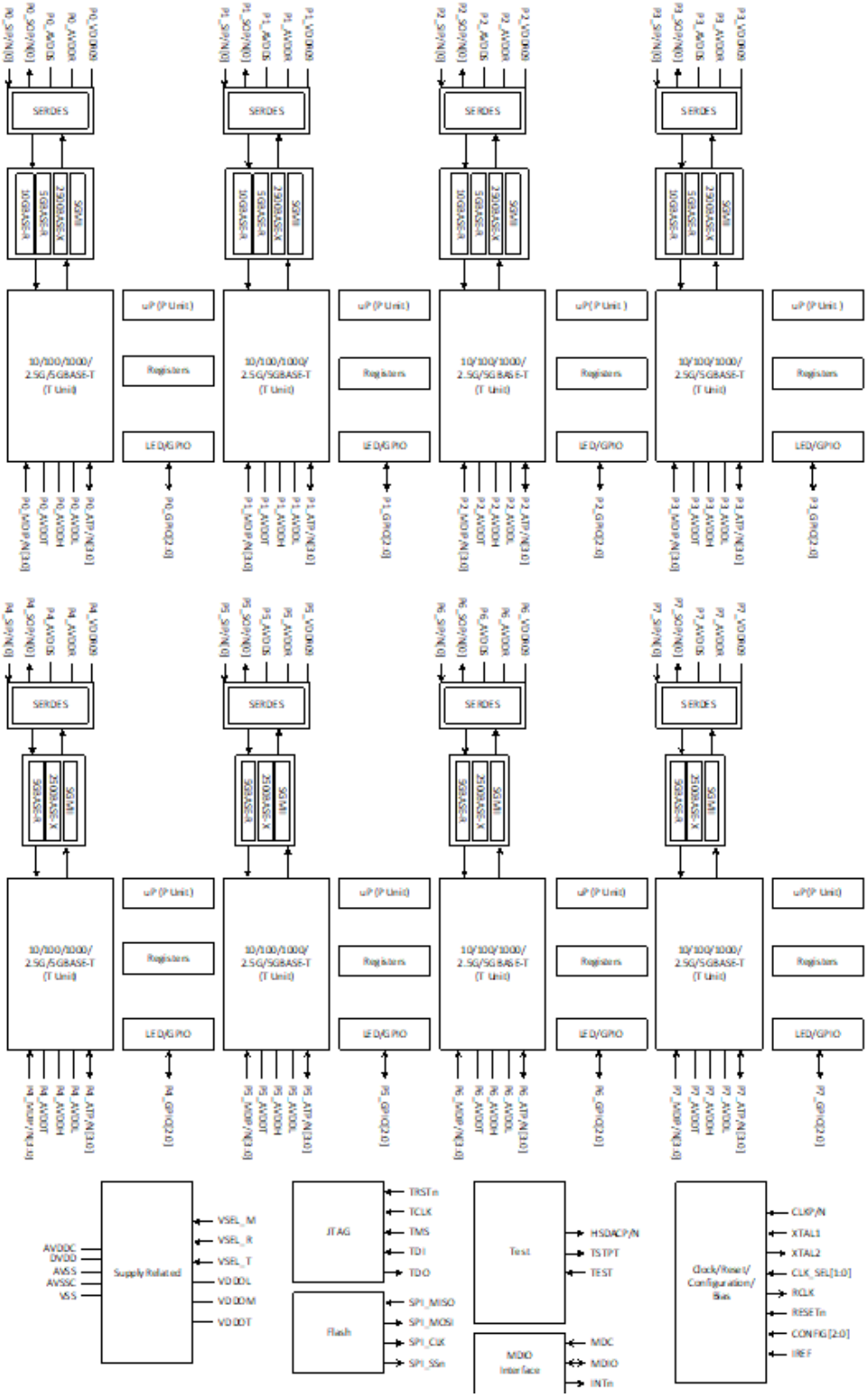
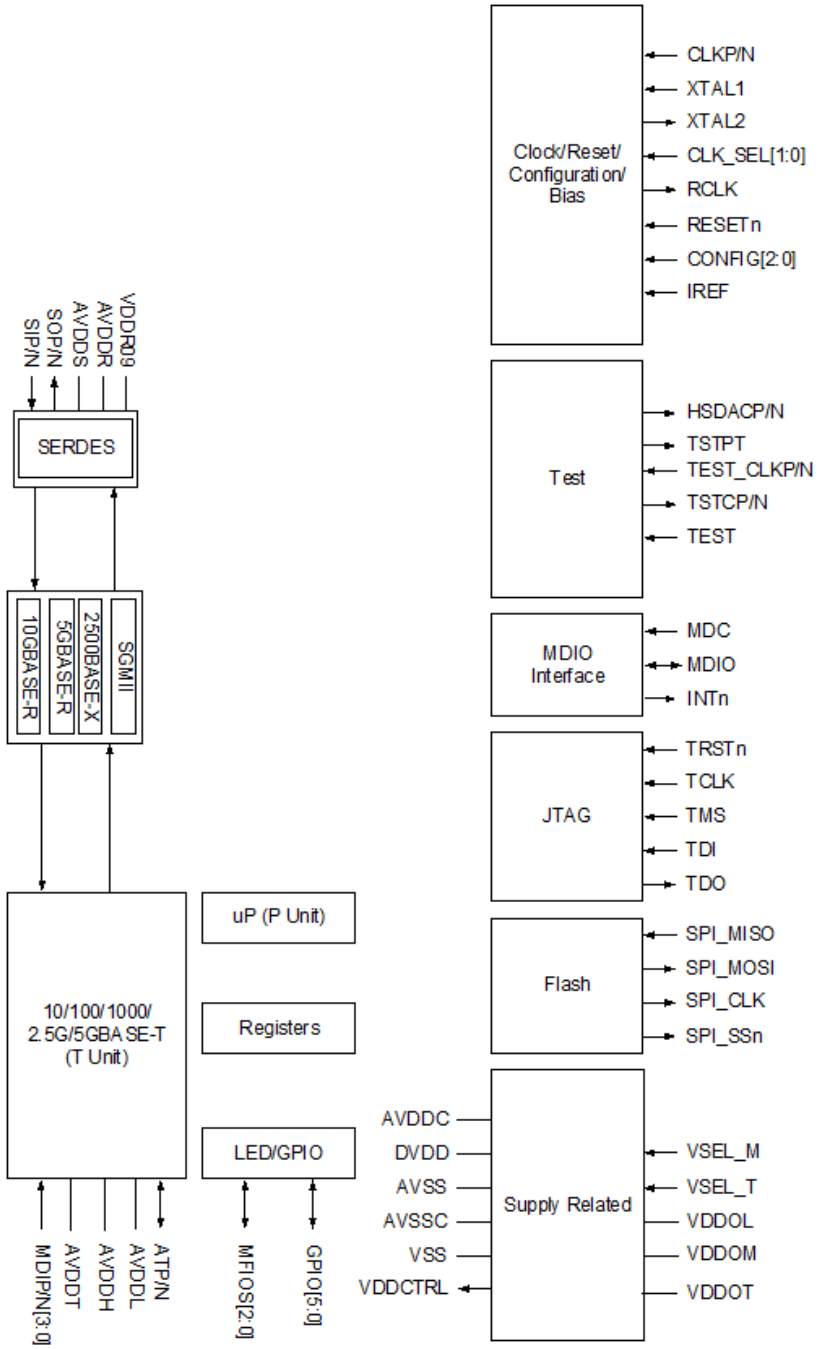


Figure 5: 88E2110 Device Functional Block Diagram



The datasheet comprises the following sections:

- Section 1 describes the general function of the device.
- Section 2 describes signal pinout and pin definitions of the device.
- Section 3 provides a functional description of the device.
- Section 4 describes the copper interface functions (T Unit).
- Section 5 describes the host interface functions (H Unit).
- Section 6 describes the electrical specification of the device.
- Section 7 describes the package mechanical dimensions.
- Section 8 provides the order information.

The conventions used in the datasheet are as follows.

All registers are specified per IEEE 802.3 section 45. The format is X.Y, X.Y.Z or X.Y.Z1:Z2, where X is the device address in decimal from 0 to 31, Y is the register address in hexadecimal from 0000 to FFFF, and Z is the bit in decimal from 0 to 15.

T Unit – 10/100/1000/2.5G/5GBASE-T interface.

H Unit – SGMII/2500BASE-X/5GBASE-R host interface.

2 Signal Description

Table 1: Pin Type Definitions

Pin Type	Definition
H	Input with hysteresis
I/O	Input and output
I	Input only
O	Output only
PU	Internal pull-up
PD	Internal pull-down
D	Open drain output
Z	Tri-state output
mA	DC sink capability

2.1 Pin Maps

2.1.1 88E2110 Device Pin Map

	1	2	3	4	5	6	7	8	
A	VSS	AVSS	SIP	AVSS	SOP	AVSS	RESETn	VSS	A
B	TRSTn	TEST	SIN	AVSS	SON	CONFIG[0]	SPI_SSn	SPI_CLK	B
C	TCK	TMS	VSEL_T	DNC	AVSS	CONFIG[2]	SPI_MOSI	SPI_MISO	C
D	TDI	VDDCTRL	VSS	VSS	VSS	AVDDR	CONFIG[1]	GPIO[0]	D
E	TDO	INTn	DVDD	VSS	DVDD	AVSS	AVDDS	GPIO[1]	E
F	MDIO	VDDOT	DVDD	VSS	DVDD	VDDR09	GPIO[3]	GPIO[2]	F
G	MDC	VDDOM	DVDD	DVDD	DVDD	VSS	RCLK	MFIOS[2]	G
H	VSEL_M	AVDDC	VSS	VSS	VSS	VSS	VDDOL	MFIOS[1]	H
J	CLKN	CLK_SEL[0]	AVSS	AVSS	AVSS	AVSS	HSDACN	MFIOS[0]	J
K	CLKP	CLK_SEL[1]	AVDDH	AVDDL	AVDDL	AVDDT	HSDACP	GPIO[4]	K
L	XTAL2	AVSSC	AVDDH	AVSS	AVSS	AVDDT	TSTPT	GPIO[5]	L
M	XTAL1	AVSS	AVSS	MDIN[1]	MDIN[2]	AVSS	AVSS	IREF	M
N	AVSS	MDIP[0]	MDIN[0]	MDIP[1]	MDIP[2]	MDIN[3]	MDIP[3]	AVSS	N
	1	2	3	4	5	6	7	8	

(Top View)

2.1.2 88E2180 Device Pin Map

Due to the large number of pins, the package is depicted graphically over two pages.

	1	2	3	4	5	6	7	8	9	10	11	12	
A	AVSS	AVSS	P7_MDIP[0]	P7_MDIP[1]	P7_MDIP[2]	P7_MDIP[3]	AVSS	P6_MDIP[3]	P6_MDIP[2]	P6_MDIP[1]	P6_MDIP[0]	AVSS	A
B	RESETn	TRSTn	P7_MDIN[0]	P7_MDIN[1]	P7_MDIN[2]	P7_MDIN[3]	AVSS	P6_MDIN[3]	P6_MDIN[2]	P6_MDIN[1]	P6_MDIN[0]	AVSS	B
C	SPI_MOSI	TDI	TEST	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	C
D	SPI_CLK	TCK	TMS	P7_AVDDT	P7_AVDDT	P7_AVDDL	P7_AVDDL	P6_AVDDL	P6_AVDDL	P6_AVDDT	P6_AVDDT	AVSS	D
E	SPI_MISO	TDO	RCLK	VSEL_T	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	E
F	SPI_SSn	VSS	VSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	P6_SDN	AVSS	F
G	VDDOL	VDDOT	VSS	AVSS	P7_AVDDH	P7_AVDDH	P6_AVDDH	P6_AVDDH	AVSS	AVSS	P6_SOP	AVSS	G
H	AVSS	AVSS	P7_AVDDR	AVSS	VSS	VSS	AVSS	VSS	AVSS	P6_AVDDR	AVSS	AVSS	H
J	P7_SIP	P7_SIN	P7_AVDDS	VSS	VSS	VSS	VSS	VSS	VSS	P6_AVDDS	P6_SIP	AVSS	J
K	AVSS	AVSS	P7_VDDR09	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	VSS	P6_SIN	AVSS	K
L	P7_SOP	P7_SON	AVSS	DVDD	VSS	VSS	VSS	DVDD	VSS	P6_VDDR09	AVSS	AVSS	L
M	AVSS	AVSS	VSS	DVDD	DVDD	DNC	DVDD	DVDD	VSS	AVSS	AVSS	AVSS	M
N	P0_SOP	P0_SON	AVSS	DVDD	VSS	VSS	VSS	DVDD	VSS	P1_VDDR09	AVSS	AVSS	N
P	AVSS	AVSS	P0_VDDR09	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	VSS	P1_SIN	AVSS	P
R	P0_SIP	P0_SIN	P0_AVDDS	VSS	VSS	VSS	VSS	VSS	VSS	P1_AVDDS	P1_SIP	AVSS	R
T	AVSS	AVSS	P0_AVDDR	AVSS	VSS	VSS	AVSS	VSS	AVSS	P1_AVDDR	AVSS	AVSS	T
U	MDC	MDIO	VSS	AVDDC	P0_AVDDH	P0_AVDDH	P1_AVDDH	P1_AVDDH	AVDDC	AVSS	P1_SOP	AVSS	U
V	VSS	VDDOM	VSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	P1_SON	AVSS	V
W	CLKN	TSTCN	VSEL_M	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	W
Y	CLKP	TSTCP	INTn	P0_AVDDT	P0_AVDDT	P0_AVDDL	P0_AVDDL	P1_AVDDL	P1_AVDDL	P1_AVDDT	P1_AVDDT	ATN	Y
AA	XTAL2	AVSSC	CLK_SEL[0]	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	ATP	AA
AB	XTAL1	CLK_SEL[1]	P0_MDIN[0]	P0_MDIN[1]	P0_MDIN[2]	P0_MDIN[3]	AVSS	P1_MDIN[3]	P1_MDIN[2]	P1_MDIN[1]	P1_MDIN[0]	AVSS	AB
AC	AVSS	AVSS	P0_MDIP[0]	P0_MDIP[1]	P0_MDIP[2]	P0_MDIP[3]	AVSS	P1_MDIP[3]	P1_MDIP[2]	P1_MDIP[1]	P1_MDIP[0]	AVSS	AC
	1	2	3	4	5	6	7	8	9	10	11	12	

(Top View)

	13	14	15	16	17	18	19	20	21	22	23	
A	P5_MDIP[0]	P5_MDIP[1]	P5_MDIP[2]	P5_MDIP[3]	AVSS	P4_MDIP[3]	P4_MDIP[2]	P4_MDIP[1]	P4_MDIP[0]	AVSS	AVSS	A
B	P5_MDIN[0]	P5_MDIN[1]	P5_MDIN[2]	P5_MDIN[3]	AVSS	P4_MDIN[3]	P4_MDIN[2]	P4_MDIN[1]	P4_MDIN[0]	CONFIG[2]	CONFIG[1]	B
C	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	MFIOS[0]	P7_GPIO[1]	P7_GPIO[0]	C
D	P5_AVDDT	P5_AVDDT	P5_AVDDL	P5_AVDDL	P4_AVDDL	P4_AVDDL	P4_AVDDT	P4_AVDDT	MFIOS[1]	P6_GPIO[0]	P6_GPIO[1]	D
E	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	MFIOS[2]	P5_GPIO[1]	P5_GPIO[0]	E
F	P5_SDN	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	VSS	VDDOL	P4_GPIO[0]	F
G	P5_SDP	AVSS	AVSS	P5_AVDDH	P5_AVDDH	P4_AVDDH	P4_AVDDH	AVSS	VSS	P4_GPIO[1]	CONFIG[0]	G
H	AVSS	P5_AVDDR	AVSS	VSS	AVSS	VSS	VSS	AVSS	P4_AVDDR	AVSS	AVSS	H
J	P5_SIP	P5_AVDDS	VSS	VSS	VSS	VSS	VSS	VSS	P4_AVDDS	P4_SIN	P4_SIP	J
K	P5_SIN	VSS	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	P4_VDDR09	AVSS	AVSS	K
L	AVSS	P5_VDDR09	VSS	DVDD	VSS	VSS	VSS	DVDD	AVSS	P4_SDN	P4_SDP	L
M	AVSS	AVSS	VSS	DVDD	DVDD	DNC	DVDD	DVDD	VSS	AVSS	AVSS	M
N	AVSS	P2_VDDR09	VSS	DVDD	VSS	VSS	VSS	DVDD	AVSS	P3_SDN	P3_SDP	N
P	P2_SIN	VSS	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	P3_VDDR09	AVSS	AVSS	P
R	P2_SIP	P2_AVDDS	VSS	VSS	VSS	VSS	VSS	VSS	P3_AVDDS	P3_SIN	P3_SIP	R
T	AVSS	P2_AVDDR	AVSS	VSS	AVSS	VSS	VSS	AVSS	P3_AVDDR	AVSS	AVSS	T
U	P2_SDP	AVSS	AVDDC	P2_AVDDH	P2_AVDDH	P3_AVDDH	P3_AVDDH	AVDDC	VSS	P3_GPIO[1]	IREF	U
V	P2_SDN	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	VSS	VDDOL	P3_GPIO[0]	V
W	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	HSDACN	TEST_CLKN	P2_GPIO[1]	W
Y	P2_AVDDT	P2_AVDDT	P2_AVDDL	P2_AVDDL	P3_AVDDL	P3_AVDDL	P3_AVDDT	P3_AVDDT	HSDACP	TEST_CLKP	P2_GPIO[0]	Y
AA	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	TSTPT	P1_GPIO[1]	P1_GPIO[0]	AA
AB	P2_MDIN[0]	P2_MDIN[1]	P2_MDIN[2]	P2_MDIN[3]	AVSS	P3_MDIN[3]	P3_MDIN[2]	P3_MDIN[1]	P3_MDIN[0]	P0_GPIO[1]	P0_GPIO[0]	AB
AC	P2_MDIP[0]	P2_MDIP[1]	P2_MDIP[2]	P2_MDIP[3]	AVSS	P3_MDIP[3]	P3_MDIP[2]	P3_MDIP[1]	P3_MDIP[0]	AVSS	AVSS	AC
	13	14	15	16	17	18	19	20	21	22	23	

(Top View)

2.2 Pin Description for the 88E2110 Device

Table 2: Media Dependent Interface

88E2110 Pin #	Pin Name	Pin Type	Description
N2 N3	MDIP[0] MDIN[0]	I/O	Media Dependent Interface[0] In 2.5G/5GBASE-T and 1000BASE-T modes in MDI configuration, MDIP/N[0] correspond to BI_DA±. In MDIX configuration, MDIP/N[0] correspond to BI_DB±. In 100BASE-TX and 10BASE-Te modes in MDI configuration, MDIP/N[0] are used for the transmit pair. In MDIX configuration, MDIP/N[0] are used for the receive pair. MDIP/N[0] should be tied to ground if not used. The device contains an internal 100Ω resistor between the MDIP/N[0] pins.
N4 M4	MDIP[1] MDIN[1]	I/O	Media Dependent Interface[1] In 2.5G/5GGBASE-T and 1000BASE-T modes in the MDIX configuration, MDIP/N[1] correspond to BI_DA±. In MDI configuration, MDIP/N[1] correspond to BI_DB±. In 100BASE-TX and 10BASE-Te modes in MDIX configuration, MDIP/N[1] are used for the transmit pair. In MDI configuration, MDIP/N[1] are used for the receive pair. MDIP/N[1] should be tied to ground if not used. The device contains an internal 100Ω resistor between the MDIP/N[1] pins.
N5 M5	MDIP[2] MDIN[2]	I/O	Media Dependent Interface[2] In 2.5G/5GGBASE-T and 1000BASE-T modes in the MDI configuration, MDIP/N[2] correspond to BI_DC±. In MDIX configuration, MDIP/N[2] correspond to BI_DD±. In 100BASE-TX and 10BASE-Te modes these pins are floating. MDIP/N[2] should be tied to ground if not used. The device contains an internal 100Ω resistor between the MDIP/N[2] pins.
N7 N6	MDIP[3] MDIN[3]	I/O	Media Dependent Interface[3] In 2.5G/5GBASE-T and 1000BASE-T modes in the MDIX configuration, MDIP/N[3] correspond to BI_DC±. In MDI configuration, MDIP/N[3] correspond to BI_DD±. In 100BASE-TX and 10BASE-Te modes these pins are floating. MDIP/N[3] should be tied to ground if not used. The device contains an internal 100Ω resistor between the MDIP/N[3] pins.

Table 3: SERDES Interface

88E2110 Pin #	Pin Name	Pin Type	Description
A3 B3	SIP SIN	I	Host SERDES Receive, Positive/Negative
A5 B5	SOP SON	O	Host SERDES Transmit, Positive/Negative

Table 4: Clock/Reset/Reference

88E2110 Pin #	Pin Name	Pin Type	Description
M8	IREF	I	Analog Reference. This pin should be connected via a 4.99 kΩ 1% resistor to VSS.
K1 J1	CLKP CLKN	I	156.25 MHz or 50 MHz differential Reference Clock Input. ±50 ppm tolerance.
M1	XTAL1	I	50 MHz crystal input
L1	XTAL2	O	50 MHz crystal output
G7	RCLK	O	Recovered clock output
A7	RESETn	I	Reset 0 = Reset 1 = Normal

Table 5: Management Interface

88E2110 Pin #	Pin Name	Pin Type	Description
G1	MDC	I	Management Clock pin. MDC is the management data clock reference for the serial management interface. A continuous clock stream is not expected. The maximum continuous frequency supported is 12.5 MHz. A 30 MHz non-continuous mode is also supported.
F1	MDIO	I/O	Management Data pin. MDIO is the management data. MDIO transfers management data in and out of the device synchronously to MDC. This pin requires a pull-up resistor in a range from 1.5 kΩ to 10 kΩ.
E2	INTn	OD	Interrupt pin. (Polarity programmable)

Table 6: SPI Interface

88E2110 Pin #	Pin Name	Pin Type	Description
B7	SPI_SSn	O	SPI device enable
B8	SPI_CLK	O	SPI clock
C7	SPI_MOSI	O	SPI serial out
C8	SPI_MISO	I	SPI serial in

Table 7: GPIO

88E2110 Pin #	Pin Name	Pin Type	Description
D8 E8	GPIO[0] GPIO[1]	I/O	General-Purpose I/Os
F8 F7 K8 L8	GPIO[2] GPIO[3] GPIO[4] GPIO[5]	I/O	General-Purpose I/Os

Table 8: Multi-functional Input/Output

88E2180 /88E2110 Pin #	Pin Name	Pin Type	Description
G8 H8 J8	MFIOS[2] MFIOS[1] MFIOS[0]	I/O	MFIOS[2]: output of LED[2] MFIOS[1]: output of LED[1] MFIOS[0]: output of LED[0]

Table 9: Configuration

88E2110 Pin #	Pin Name	Pin Type	Description
J2 K2	CLK_SEL[0] CLK_SEL[1]	I, PD	Reference clock selection 00 = 50 MHz XTAL1/2 01 = 50 MHz CLKP/N 10 = 156.25 MHz CLKP/N 11 = Reserved
B6 D7 C6	CONFIG[0] CONFIG[1] CONFIG[2]	I	Hardware Configuration. Refer to Section 3.5.2 for details.
H1	VSEL_M	I	VDDOM Voltage Level Select VSS = 2.5V/3.3V, VDDOM = 1.2V/1.5V/1.8V
C3	VSEL_T	I	VDDOT Voltage Level Select VSS = 2.5V/3.3V, VDDOT = 1.5V/1.8V

Table 10: JTAG Interface

88E2110 Pin #	Pin Name	Pin Type	Description
D1	TDI	I, PU	JTAG Data Input
E1	TDO	O	JTAG Data Output
C2	TMS	I, PU	JTAG Mode Select
C1	TCK	I, PU	JTAG Clock
B1	TRSTn	I, PU	JTAG Reset. TRSTn pin requires a 4.7 kΩ pull-down externally for normal operation.

Table 11: Test Pins

88E2110 Pin #	Pin Name	Pin Type	Description
K7 J7	HSDACP HSDACN	O	AC Test **NOTE:** Test purposes only, do not connect.
L7	TSTPT	O	DC Test
B2	TEST	I, PD	Test Enable This pin should be left floating.

Table 12: Power and Ground

88E2110 Pin #	Pin Name	Pin Type	Description
E7	AVDDS	Power	1.5V or 1.8V analog power
D6	AVDDR	Power	1.5V or 1.8V analog power. Can tie to AVDDS.
H2	AVDDC	Power	1.5V or 1.8V analog power
K4 K5	AVDDL	Power	1.5V or 1.8V analog power
K3 L3	AVDDH	Power	1.8V analog power
K6 L6	AVDDT	Power	3.3V analog
F6	VDDR09	Power	0.9V internally regulated power. This pin must be tied to a capacitor. Do not connect this pin to external power.
E3 E5 F3 F5 G3 G4 G5	DVDD	Power	Digital power 0.8V core digital power
H7	VDDOL	Power	I/O power - LED, CONFIG, CLK_SEL, TEST, GPIO, MFIOS, SPI, RCLK, RESET
G2	VDDOM	Power	I/O power - MDC, MDIO, INTn
F2	VDDOT	Power	I/O power - JTAG

Table 12: Power and Ground (Continued)

88E2110 Pin #	Pin Name	Pin Type	Description
A2 A4 A6 B4 C5 E6 J3 J4 J5 J6 L4 L5 M2 M3 M6 M7 N1 N8	AVSS	Power	Analog Ground
L2	AVSSC	Power	Analog Ground This must be isolated from AVSS.
A1 A8 D3 D4 D5 E4 F4 G6 H3 H4 H5 H6	VSS	Power	Ground

Table 13: Do Not Connect

88E2110 Pin #	Pin Name	Pin Type	Description
C4	DNC	No Connect	Do not connect.

2.3 Pin Description for the 88E2180 Device

Table 14: Media Dependent Interface

88E2180 Pin #	Pin Name	Pin Type	Description
AC3 AB3	P0_MDIP[0] P0_MDIN[0]	I/O	Media Dependent Interface[0], Port 0. In 2.5G/5GBASE-T and 1000BASE-T modes in MDI configuration, MDIP/N[0] correspond to BI_DA±. In MDIX configuration, MDIP/N[0] correspond to BI_DB±. In 100BASE-TX and 10BASE-Te modes in MDI configuration, MDIP/N[0] are used for the transmit pair. In MDIX configuration, MDIP/N[0] are used for the receive pair. MDIP/N[0] should be tied to ground if not used. The device contains an internal 100Ω resistor between the MDIP/N[0] pins.
AC4 AB4	P0_MDIP[1] P0_MDIN[1]	I/O	Media Dependent Interface[1], Port 0. In 2.5G/5GGBASE-T and 1000BASE-T modes in the MDIX configuration, MDIP/N[1] correspond to BI_DA±. In MDI configuration, MDIP/N[1] correspond to BI_DB±. In 100BASE-TX and 10BASE-Te modes in MDIX configuration, MDIP/N[1] are used for the transmit pair. In MDI configuration, MDIP/N[1] are used for the receive pair. MDIP/N[1] should be tied to ground if not used. The device contains an internal 100Ω resistor between the MDIP/N[1] pins.
AC5 AB5	P0_MDIP[2] P0_MDIN[2]	I/O	Media Dependent Interface[2], Port 0. In 2.5G/5GGBASE-T and 1000BASE-T modes in the MDI configuration, MDIP/N[2] correspond to BI_DC±. In MDIX configuration, MDIP/N[2] correspond to BI_DD±. In 100BASE-TX and 10BASE-Te modes these pins are floating. MDIP/N[2] should be tied to ground if not used. The device contains an internal 100Ω resistor between the MDIP/N[2] pins.
AC6 AB6	P0_MDIP[3] P0_MDIN[3]	I/O	Media Dependent Interface[3], Port 0. In 2.5G/5GBASE-T and 1000BASE-T modes in the MDIX configuration, MDIP/N[3] correspond to BI_DC±. In MDI configuration, MDIP/N[3] correspond to BI_DD±. In 100BASE-TX and 10BASE-Te modes these pins are floating. MDIP/N[3] should be tied to ground if not used. The device contains an internal 100Ω resistor between the MDIP/N[3] pins.
AC11 AB11	P1_MDIP[0] P1_MDIN[0]	I/O	Media Dependent Interface [0], Port 1.
AC10 AB10	P1_MDIP[1] P1_MDIN[1]	I/O	Media Dependent Interface [1], Port 1.
AC9 AB9	P1_MDIP[2] P1_MDIN[2]	I/O	Media Dependent Interface [2], Port 1.
AC8 AB8	P1_MDIP[3] P1_MDIN[3]	I/O	Media Dependent Interface [3], Port 1.
AC13 AB13	P2_MDIP[0] P2_MDIN[0]	I/O	Media Dependent Interface [0], Port 2.
AC14 AB14	P2_MDIP[1] P2_MDIN[1]	I/O	Media Dependent Interface [1], Port 2.

Table 14: Media Dependent Interface (Continued)

88E2180 Pin #	Pin Name	Pin Type	Description
AC15 AB15	P2_MDIP[2] P2_MDIN[2]	I/O	Media Dependent Interface [2], Port 2.
AC16 AB16	P2_MDIP[3] P2_MDIN[3]	I/O	Media Dependent Interface [3], Port 2.
AC21 AB21	P3_MDIP[0] P3_MDIN[0]	I/O	Media Dependent Interface [0], Port 3.
AC20 AB20	P3_MDIP[1] P3_MDIN[1]	I/O	Media Dependent Interface [1], Port 3.
AC19 AB19	P3_MDIP[2] P3_MDIN[2]	I/O	Media Dependent Interface [2], Port 3.
AC18 AB18	P3_MDIP[3] P3_MDIN[3]	I/O	Media Dependent Interface [3], Port 3.
A21 B21	P4_MDIP[0] P4_MDIN[0]	I/O	Media Dependent Interface [0], Port 4.
A20 B20	P4_MDIP[1] P4_MDIN[1]	I/O	Media Dependent Interface [1], Port 4.
A19 B19	P4_MDIP[2] P4_MDIN[2]	I/O	Media Dependent Interface [2], Port 4.
A18 B18	P4_MDIP[3] P4_MDIN[3]	I/O	Media Dependent Interface [3], Port 4.
A13 B13	P5_MDIP[0] P5_MDIN[0]	I/O	Media Dependent Interface [0], Port 5.
A14 B14	P5_MDIP[1] P5_MDIN[1]	I/O	Media Dependent Interface [1], Port 5.
A15 B15	P5_MDIP[2] P5_MDIN[2]	I/O	Media Dependent Interface [2], Port 5.
A16 B16	P5_MDIP[3] P5_MDIN[3]	I/O	Media Dependent Interface [3], Port 5.
A11 B11	P6_MDIP[0] P6_MDIN[0]	I/O	Media Dependent Interface [0], Port 6.
A10 B10	P6_MDIP[1] P6_MDIN[1]	I/O	Media Dependent Interface [1], Port 6.
A9 B9	P6_MDIP[2] P6_MDIN[2]	I/O	Media Dependent Interface [2], Port 6.
A8 B8	P6_MDIP[3] P6_MDIN[3]	I/O	Media Dependent Interface [3], Port 6.
A3 B3	P7_MDIP[0] P7_MDIN[0]	I/O	Media Dependent Interface [0], Port 7.
A4 B4	P7_MDIP[1] P7_MDIN[1]	I/O	Media Dependent Interface [1], Port 7.
A5 B5	P7_MDIP[2] P7_MDIN[2]	I/O	Media Dependent Interface [2], Port 7.

Table 14: Media Dependent Interface (Continued)

88E2180 Pin #	Pin Name	Pin Type	Description
A6 B6	P7_MDIP[3] P7_MDIN[3]	I/O	Media Dependent Interface [3], Port 7.

Table 15: SERDES Interface

88E2180 Pin #	Pin Name	Pin Type	Description
R1 R2	P0_SIP P0_SIN	I	Host SERDES Receive, Positive/Negative, Port 0
R11 P11	P1_SIP P1_SIN	I	Host SERDES Receive, Positive/Negative, Port 1
R13 P13	P2_SIP P2_SIN	I	Host SERDES Receive, Positive/Negative, Port 2
R23 R22	P3_SIP P3_SIN	I	Host SERDES Receive, Positive/Negative, Port 3
J23 J22	P4_SIP P4_SIN	I	Host SERDES Receive, Positive/Negative, Port 4
J13 K13	P5_SIP P5_SIN	I	Host SERDES Receive, Positive/Negative, Port 5
J11 K11	P6_SIP P6_SIN	I	Host SERDES Receive, Positive/Negative, Port 6
J1 J2	P7_SIP P7_SIN	I	Host SERDES Receive, Positive/Negative, Port 7
N1 N2	P0_SOP P0_SON	O	Host SERDES Transmit, Positive/Negative, Port 0
U11 V11	P1_SOP P1_SON	O	Host SERDES Transmit, Positive/Negative, Port 1
U13 V13	P2_SOP P2_SON	O	Host SERDES Transmit, Positive/Negative, Port 2
N23 N22	P3_SOP P3_SON	O	Host SERDES Transmit, Positive/Negative, Port 3
L23 L22	P4_SOP P4_SON	O	Host SERDES Transmit, Positive/Negative, Port 4
G13 F13	P5_SOP P5_SON	O	Host SERDES Transmit, Positive/Negative, Port 5
G11 F11	P6_SOP P6_SON	O	Host SERDES Transmit, Positive/Negative, Port 6
L1 L2	P7_SOP P7_SON	O	Host SERDES Transmit, Positive/Negative, Port 7

Table 16: Clock/Reset/Reference

88E2180 Pin #	Pin Name	Pin Type	Description
U23	IREF	I	Analog Reference. This pin should be connected via a 4.99 kΩ 1% resistor to VSS.
Y1 W1	CLKP CLKN	I	156.25 MHz or 50 MHz differential Reference Clock Input. ±50 ppm tolerance.
AB1	XTAL1	I	50 MHz crystal input
AA1	XTAL2	O	50 MHz crystal output
E3	RCLK	O	25 MHz Recovered clock output
B1	RESETn	I	Reset 0 = Reset 1 = Normal

Table 17: Management Interface

88E2180 Pin #	Pin Name	Pin Type	Description
U1	MDC	I	Management Clock pin. MDC is the management data clock reference for the serial management interface. A continuous clock stream is not expected. The maximum continuous frequency supported is 12.5 MHz. A 30 MHz non-continuous mode is also supported.
U2	MDIO	I/O	Management Data pin. MDIO is the management data. MDIO transfers management data in and out of the device synchronously to MDC. This pin requires a pull-up resistor in a range from 1.5 kΩ to 10 kΩ.
Y3	INTn	OD	Interrupt pin. (Polarity programmable)

Table 18: SPI Interface

88E2180 Pin #	Pin Name	Pin Type	Description
F1	SPI_SSn	O	SPI device enable
D1	SPI_CLK	O	SPI clock
C1	SPI_MOSI	O	SPI serial out
E1	SPI_MISO	I	SPI serial in

Table 19: GPIO

88E2180 Pin #	Pin Name	Pin Type	Description
AB23 AB22	P0_GPIO[0] P0_GPIO[1]	I/O	General-Purpose I/Os, Port 0.
AA23 AA22	P1_GPIO[0] P1_GPIO[1]	I/O	General-Purpose I/Os, Port 1.
Y23 W23	P2_GPIO[0] P2_GPIO[1]	I/O	General-Purpose I/Os, Port 2.
V23 U22	P3_GPIO[0] P3_GPIO[1]	I/O	General-Purpose I/Os, Port 3.
F23 G22	P4_GPIO[0] P4_GPIO[1]	I/O	General-Purpose I/Os, Port 4.
E23 E22	P5_GPIO[0] P5_GPIO[1]	I/O	General-Purpose I/Os, Port 5.
D22 D23	P6_GPIO[0] P6_GPIO[1]	I/O	General-Purpose I/Os, Port 6.
C23 C22	P7_GPIO[0] P7_GPIO[1]	I/O	General-Purpose I/Os, Port 7.

Table 20: Multi-functional Input/Output

88E2180 /88E2110 Pin #	Pin Name	Pin Type	Description
C21 D21 E21	MFIOS[0] MFIOS[1] MFIOS[2]	I/O	Multi-function I/O Serial (GPIO/Serial LED/LED). Refer to Section 3.10 for details on how to configure these pins for Serial LED functionality.

Table 21: Configuration

88E2180 Pin #	Pin Name	Pin Type	Description
AA3 AB2	CLK_SEL[0] CLK_SEL[1]	I, PD	Reference clock selection 00 = 50 MHz XTAL1/2 (50 MHz crystal is for Test Mode Purpose Only) 01 = 50 MHz CLKP/N (50 MHz clock is for Test Mode Purpose Only) 10 = 156.25 MHz CLKP/N 11 = Reserved **NOTE:** 50 MHz crystal or clock is for Test Mode Purpose Only. Normal operation must use 156.25 MHz differential clock.
G23 B23 B22	CONFIG[0] CONFIG[1] CONFIG[2]	I	Hardware Configuration. Refer to Section 3.5.2 for details.

Table 21: Configuration (Continued)

88E2180 Pin #	Pin Name	Pin Type	Description
W3	VSEL_M	I	VDDOM Voltage Level Select VSS = 2.5V/3.3V, VDDOM = 1.2V/1.5V/1.8V
E4	VSEL_T	I	VDDOT Voltage Level Select VSS = 2.5V/3.3V, VDDOT = 1.5V/1.8V

Table 22: JTAG Interface

88E2180 Pin #	Pin Name	Pin Type	Description
C2	TDI	I, PU	JTAG Data Input
E2	TDO	O	JTAG Data Output
D3	TMS	I, PU	JTAG Mode Select
D2	TCK	I, PU	JTAG Clock
B2	TRSTn	I, PU	JTAG Reset. TRSTn pin requires a 4.7 kΩ pull-down externally for normal operation.

Table 23: Test Pins

88E2180 Pin #	Pin Name	Pin Type	Description
Y12 AA12	ATN ATP	O	Copper Test Negative and Positive This pin should be left floating.
Y21 W21	HSDACP HSDACN	O	AC Test **NOTE:** Test purposes only, do not connect.
AA21	TSTPT	O	DC Test
Y22 W22	TEST_CLKP TEST_CLKN	I	Test Clock Input Tie to ground using a 0Ω resistor.
Y2 W2	TSTCP TSTCN	O	Test Clock Output When using the 50 MHz XTAL option, the (CLK_SEL[1:0] = 00), TSTCP/N output pins must be AC coupled with a 0.1 µF capacitor and connected to CLK_P/N input pins on the board. **NOTE:** 50 MHz clock is for Test Mode Purpose Only.
C3	TEST	I, PD	Test Enable This pin should be left floating.

Table 24: Power and Ground

88E2180 Pin #	Pin Name	Pin Type	Description
R3	P0_AVDDS	Power	1.5V or 1.8V analog power
R10	P1_AVDDS		
R14	P2_AVDDS		
R21	P3_AVDDS		

Table 24: Power and Ground (Continued)

88E2180 Pin #	Pin Name	Pin Type	Description
J21	P4_AVDDS		
J14	P5_AVDDS		
J10	P6_AVDDS		
J3	P7_AVDDS		
T3	P0_AVDDR	Power	1.5V or 1.8V analog power. Can tie to AVDDS.
T10	P1_AVDDR		
T14	P2_AVDDR		
T21	P3_AVDDR		
H21	P4_AVDDR		
H14	P5_AVDDR		
H10	P6_AVDDR		
H3	P7_AVDDR		
U4 U9 U15 U20	AVDDC	Power	1.5V or 1.8V analog power
Y6 Y7	P0_AVDDL	Power	1.5V or 1.8V analog power
Y8 Y9	P1_AVDDL		
Y15 Y16	P2_AVDDL		
Y17 Y18	P3_AVDDL		
D17 D18	P4_AVDDL		
D15 D16	P5_AVDDL		
D8 D9	P6_AVDDL		
D6 D7	P7_AVDDL		
U5 U6	P0_AVDDH	Power	1.8V analog power
U7 U8	P1_AVDDH		
U16 U17	P2_AVDDH		
U18 U19	P3_AVDDH		

Table 24: Power and Ground (Continued)

88E2180 Pin #	Pin Name	Pin Type	Description
G18 G19	P4_AVDDH		
G16 G17	P5_AVDDH		
G7 G8	P6_AVDDH		
G5 G6	P7_AVDDH		
Y4 Y5	P0_AVDDT	Power	3.3V analog
Y10 Y11	P1_AVDDT		
Y13 Y14	P2_AVDDT		
Y19 Y20	P3_AVDDT		
D19 D20	P4_AVDDT		
D13 D14	P5_AVDDT		
D10 D11	P6_AVDDT		
D4 D5	P7_AVDDT		
P3	P0_VDDR09	Power	0.9V internally regulated power. This pin must be tied to a capacitor. Do not connect this pin to external power.
N10	P1_VDDR09		
N14	P2_VDDR09		
P21	P3_VDDR09		
K21	P4_VDDR09		
L14	P5_VDDR09		
L10	P6_VDDR09		
K3	P7_VDDR09		

Table 24: Power and Ground (Continued)

88E2180 Pin #	Pin Name	Pin Type	Description
K4 K5 K6 K7 K8 K9 K15 K16 K17 K18 K19 K20 L4 L8 L16 L20 M4 M5 M7 M8 M16 M17 M19 M20 N4 N8 N16 N20 P4 P5 P6 P7 P8 P9 P15 P16 P17 P18 P19 P20	DVDD	Power	Digital power 0.8V/0.88V core digital power (Refer to Section 6.2 for I-temp details.)
F22 G1 V22	VDDOL	Power	I/O power - LED, CONFIG, CLK_SEL, TEST, GPIO, MFIOS, SPI, RCLK, RESET
V2	VDDOM	Power	I/O power - MDC, MDIO, INTn
G2	VDDOT	Power	I/O power - JTAG

Table 24: Power and Ground (Continued)

88E2180 Pin #	Pin Name	Pin Type	Description
A1 A2 A7 A12 A17 A22 A23 B7 B12 B17 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 D12 E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E15	AVSS	Power	Analog Ground

Table 24: Power and Ground (Continued)

88E2180 Pin #	Pin Name	Pin Type	Description
E16 E17 E18 E19 E20 F4 F5 F6 F7 F8 F9 F10 F12 F14 F15 F16 F17 F18 F19 F20 G4 G9 G10 G12 G14 G15 G20 H1 H2 H4 H7 H9 H11 H12 H13 H15 H17 H20 H22 H23 J12 K1 K2 K12 K22 K23 L3 L11 L12 L13 L21 M1 M2 M10	AVSS (cont.)	Power	Analog Ground

Table 24: Power and Ground (Continued)

88E2180 Pin #	Pin Name	Pin Type	Description
M11 M12 M13 M14 M22 M23 N3 N11 N12 N13 N21 P1 P2 P12 P22 P23 R12 T1 T2 T4 T7 T9 T11 T12 T13 T15 T17 T20 T22 T23 U10 U12 U14 V4 V5 V6 V7 V8 V9 V10 V12 V14 V15 V16 V17 V18 V19 V20 W4 W5 W6 W7 W8 W9	AVSS (cont.)	Power	Analog Ground

Table 24: Power and Ground (Continued)

88E2180 Pin #	Pin Name	Pin Type	Description
W10 W11 W12 W13 W14 W15 W16 W17 W18 W19 W20 AA4 AA5 AA6 AA7 AA8 AA9 AA10 AA11 AA13 AA14 AA15 AA16 AA17 AA18 AA19 AA20 AB7 AB12 AB17 AC1 AC2 AC7 AC12 AC17 AC22 AC23	AVSS (cont.)	Power	Analog Ground
AA2	AVSSC	Power	Analog Ground This must be isolated from AVSS.

Table 24: Power and Ground (Continued)

88E2180 Pin #	Pin Name	Pin Type	Description
F2 F3 F21 G3 G21 H5 H6 H8 H16 H18 H19 J4 J5 J6 J7 J8 J9 J15 J16 J17 J18 J19 J20 K10 K14 L5 L6 L7 L9 L15 L17 L18 L19 M3 M9 M15 M21 N5 N6 N7 N9 N15 N17 N18 N19 P10 P14 R4 R5 R6 R7 R8 R9 R15	VSS	Power	Ground

Table 24: Power and Ground (Continued)

88E2180 Pin #	Pin Name	Pin Type	Description
R16 R17 R18 R19 R20 T5 T6 T8 T16 T18 T19 U3 U21 V1 V3 V21	VSS (cont.)	Power	Ground

Table 25: Do Not Connect

88E2180 Pin #	Pin Name	Pin Type	Description
M6 M18	DNC	No Connect	Do not connect.

2.4 Pin Assignment Lists

2.4.1 88E2110 Device Pin Assignment List

Table 26: 88E2110 Pin List — Alphabetical by Signal Name

Pin Number	Pin Name
K3	AVDDH
L3	AVDDH
K4	AVDDL
K5	AVDDL
K6	AVDDT
L6	AVDDT
H2	AVDDC
D6	AVDDR
E7	AVDDS
A2	AVSS
A4	AVSS
A6	AVSS
B4	AVSS
C5	AVSS
E6	AVSS
J3	AVSS
J4	AVSS
J5	AVSS
J6	AVSS
L4	AVSS
L5	AVSS
M2	AVSS
M3	AVSS
M6	AVSS
M7	AVSS
N1	AVSS
N8	AVSS
L2	AVSSC
J2	CLK_SEL[0]
K2	CLK_SEL[1]
J1	CLKN
K1	CLKP
B6	CONFIG[0]
D7	CONFIG[1]
C6	CONFIG[2]
C4	DNC
E3	DVDD
E5	DVDD
F3	DVDD
F5	DVDD
G3	DVDD
G4	DVDD
G5	DVDD
D8	GPIO[0]
E8	GPIO[1]
F8	GPIO[2]
F7	GPIO[3]
K8	GPIO[4]
L8	GPIO[5]

Pin Number	Pin Name
J7	HSDACN
K7	HSDACP
E2	INTn
M8	IREF
G1	MDC
N3	MDIN[0]
M4	MDIN[1]
M5	MDIN[2]
N6	MDIN[3]
F1	MDIO
N2	MDIP[0]
N4	MDIP[1]
N5	MDIP[2]
N7	MDIP[3]
J8	MFIOS[0]
H8	MFIOS[1]
G8	MFIOS[2]
G7	RCLK
A7	RESETn
B3	SIN
A3	SIP
B5	SON
A5	SOP
B8	SPI_CLK
C8	SPI_MISO
C7	SPI_MOSI
B7	SPI_SSn
C1	TCK

Pin Number	Pin Name
D1	TDI
E1	TDO
B2	TEST
C2	TMS
B1	TRSTn
L7	TSTPT
D2	VDDCTRL
H7	VDDOL
G2	VDDOM
F2	VDDOT
F6	VDDR09
H1	VSEL_M
C3	VSEL_T
A1	VSS
A8	VSS
D3	VSS
D4	VSS
D5	VSS
E4	VSS
F4	VSS
G6	VSS
H3	VSS
H4	VSS
H5	VSS
H6	VSS
M1	XTAL1
L1	XTAL2

2.4.2 88E2180 Device Pin Assignment List

Table 27: 88E2180 Pin List — Alphabetical by Signal Name

Pin Number	Pin Name
Y12	ATN
AA12	ATP
U4	AVDDC
U9	AVDDC
U15	AVDDC
U20	AVDDC
A1	AVSS
A2	AVSS
A7	AVSS
A12	AVSS
A17	AVSS
A22	AVSS
A23	AVSS
B7	AVSS
B12	AVSS
B17	AVSS
C4	AVSS
C5	AVSS
C6	AVSS
C7	AVSS
C8	AVSS
C9	AVSS
C10	AVSS
C11	AVSS
C12	AVSS
C13	AVSS
C14	AVSS
C15	AVSS
C16	AVSS
C17	AVSS
C18	AVSS
C19	AVSS
C20	AVSS
D12	AVSS
E5	AVSS
E6	AVSS
E7	AVSS
E8	AVSS
E9	AVSS
E10	AVSS
E11	AVSS
E12	AVSS
E13	AVSS
E14	AVSS
E15	AVSS
E16	AVSS
E17	AVSS
E18	AVSS
E19	AVSS
E20	AVSS
F4	AVSS
F5	AVSS

Pin Number	Pin Name
F6	AVSS
F7	AVSS
F8	AVSS
F9	AVSS
F10	AVSS
F12	AVSS
F14	AVSS
F15	AVSS
F16	AVSS
F17	AVSS
F18	AVSS
F19	AVSS
F20	AVSS
G4	AVSS
G9	AVSS
G10	AVSS
G12	AVSS
G14	AVSS
G15	AVSS
G20	AVSS
H1	AVSS
H2	AVSS
H4	AVSS
H7	AVSS
H9	AVSS
H11	AVSS
H12	AVSS
H13	AVSS

Pin Number	Pin Name
H15	AVSS
H17	AVSS
H20	AVSS
H22	AVSS
H23	AVSS
J12	AVSS
K1	AVSS
K2	AVSS
K12	AVSS
K22	AVSS
K23	AVSS
L3	AVSS
L11	AVSS
L12	AVSS
L13	AVSS
L21	AVSS
M1	AVSS
M2	AVSS
M10	AVSS
M11	AVSS
M12	AVSS
M13	AVSS
M14	AVSS
M22	AVSS
M23	AVSS
N3	AVSS
N11	AVSS
N12	AVSS

Pin Number	Pin Name
N13	AVSS
N21	AVSS
P1	AVSS
P2	AVSS
P12	AVSS
P22	AVSS
P23	AVSS
R12	AVSS
T1	AVSS
T2	AVSS
T4	AVSS
T7	AVSS
T9	AVSS
T11	AVSS
T12	AVSS
T13	AVSS
T15	AVSS
T17	AVSS
T20	AVSS
T22	AVSS
T23	AVSS
U10	AVSS
U12	AVSS
U14	AVSS
V4	AVSS
V5	AVSS
V6	AVSS
V7	AVSS

Pin Number	Pin Name
V8	AVSS
V9	AVSS
V10	AVSS
V12	AVSS
V14	AVSS
V15	AVSS
V16	AVSS
V17	AVSS
V18	AVSS
V19	AVSS
V20	AVSS
W4	AVSS
W5	AVSS
W6	AVSS
W7	AVSS
W8	AVSS
W9	AVSS
W10	AVSS
W11	AVSS
W12	AVSS
W13	AVSS
W14	AVSS
W15	AVSS
W16	AVSS
W17	AVSS
W18	AVSS
W19	AVSS
W20	AVSS

Pin Number	Pin Name
AA4	AVSS
AA5	AVSS
AA6	AVSS
AA7	AVSS
AA8	AVSS
AA9	AVSS
AA10	AVSS
AA11	AVSS
AA13	AVSS
AA14	AVSS
AA15	AVSS
AA16	AVSS
AA17	AVSS
AA18	AVSS
AA19	AVSS
AA20	AVSS
AB7	AVSS
AB12	AVSS
AB17	AVSS
AC1	AVSS
AC2	AVSS
AC7	AVSS
AC12	AVSS
AC17	AVSS
AC22	AVSS
AC23	AVSS
AA2	AVSSC
AA3	CLK_SEL[0]

Pin Number	Pin Name
AB2	CLK_SEL[1]
W1	CLKN
Y1	CLKP
G23	CONFIG[0]
B23	CONFIG[1]
B22	CONFIG[2]
M6	DNC
M18	DNC
K4	DVDD
K5	DVDD
K6	DVDD
K7	DVDD
K8	DVDD
K9	DVDD
K15	DVDD
K16	DVDD
K17	DVDD
K18	DVDD
K19	DVDD
K20	DVDD
L4	DVDD
L8	DVDD
L16	DVDD
L20	DVDD
M4	DVDD
M5	DVDD
M7	DVDD
M8	DVDD

Pin Number	Pin Name
M16	DVDD
M17	DVDD
M19	DVDD
M20	DVDD
N4	DVDD
N8	DVDD
N16	DVDD
N20	DVDD
P4	DVDD
P5	DVDD
P6	DVDD
P7	DVDD
P8	DVDD
P9	DVDD
P15	DVDD
P16	DVDD
P17	DVDD
P18	DVDD
P19	DVDD
P20	DVDD
W21	HSDACN
Y21	HSDACP
Y3	INTn
U23	IREF
U1	MDC
U2	MDIO
C21	MFIOS[0]
D21	MFIOS[1]

Pin Number	Pin Name
E21	MFIOS[2]
U5	P0_AVDDH
U6	P0_AVDDH
Y6	P0_AVDDL
Y7	P0_AVDDL
Y4	P0_AVDDT
Y5	P0_AVDDT
T3	P0_AVDDR
R3	P0_AVDDS
AB23	P0_GPIO[0]
AB22	P0_GPIO[1]
AB3	P0_MDIN[0]
AB4	P0_MDIN[1]
AB5	P0_MDIN[2]
AB6	P0_MDIN[3]
AC3	P0_MDIP[0]
AC4	P0_MDIP[1]
AC5	P0_MDIP[2]
AC6	P0_MDIP[3]
R2	P0_SIN
R1	P0_SIP
N2	P0_SON
N1	P0_SOP
P3	P0_VDDR09
U7	P1_AVDDH
U8	P1_AVDDH
Y8	P1_AVDDL
Y9	P1_AVDDL

Pin Number	Pin Name
Y10	P1_AVDDT
Y11	P1_AVDDT
T10	P1_AVDDR
R10	P1_AVDDS
AA23	P1_GPIO[0]
AA22	P1_GPIO[1]
AB11	P1_MDIN[0]
AB10	P1_MDIN[1]
AB9	P1_MDIN[2]
AB8	P1_MDIN[3]
AC11	P1_MDIP[0]
AC10	P1_MDIP[1]
AC9	P1_MDIP[2]
AC8	P1_MDIP[3]
P11	P1_SIN
R11	P1_SIP
V11	P1_SON
U11	P1_SOP
N10	P1_VDDR09
U16	P2_AVDDH
U17	P2_AVDDH
Y15	P2_AVDDL
Y16	P2_AVDDL
Y13	P2_AVDDT
Y14	P2_AVDDT
T14	P2_AVDDR
R14	P2_AVDDS
Y23	P2_GPIO[0]

Pin Number	Pin Name
W23	P2_GPIO[1]
AB13	P2_MDIN[0]
AB14	P2_MDIN[1]
AB15	P2_MDIN[2]
AB16	P2_MDIN[3]
AC13	P2_MDIP[0]
AC14	P2_MDIP[1]
AC15	P2_MDIP[2]
AC16	P2_MDIP[3]
P13	P2_SIN
R13	P2_SIP
V13	P2_SON
U13	P2_SOP
N14	P2_VDDR09
U18	P3_AVDDH
U19	P3_AVDDH
Y17	P3_AVDDL
Y18	P3_AVDDL
Y19	P3_AVDDT
Y20	P3_AVDDT
T21	P3_AVDDR
R21	P3_AVDDS
V23	P3_GPIO[0]
U22	P3_GPIO[1]
AB21	P3_MDIN[0]
AB20	P3_MDIN[1]
AB19	P3_MDIN[2]
AB18	P3_MDIN[3]

Pin Number	Pin Name
AC21	P3_MDIP[0]
AC20	P3_MDIP[1]
AC19	P3_MDIP[2]
AC18	P3_MDIP[3]
R22	P3_SIN
R23	P3_SIP
N22	P3_SON
N23	P3_SOP
P21	P3_VDDR09
G18	P4_AVDDH
G19	P4_AVDDH
D17	P4_AVDDL
D18	P4_AVDDL
D19	P4_AVDDT
D20	P4_AVDDT
H21	P4_AVDDR
J21	P4_AVDDS
F23	P4_GPIO[0]
G22	P4_GPIO[1]
B21	P4_MDIN[0]
B20	P4_MDIN[1]
B19	P4_MDIN[2]
B18	P4_MDIN[3]
A21	P4_MDIP[0]
A20	P4_MDIP[1]
A19	P4_MDIP[2]
A18	P4_MDIP[3]
J22	P4_SIN

Pin Number	Pin Name
J23	P4_SIP
L22	P4_SON
L23	P4_SOP
K21	P4_VDDR09
G16	P5_AVDDH
G17	P5_AVDDH
D15	P5_AVDDL
D16	P5_AVDDL
D13	P5_AVDDT
D14	P5_AVDDT
H14	P5_AVDDR
J14	P5_AVDDS
E23	P5_GPIO[0]
E22	P5_GPIO[1]
B13	P5_MDIN[0]
B14	P5_MDIN[1]
B15	P5_MDIN[2]
B16	P5_MDIN[3]
A13	P5_MDIP[0]
A14	P5_MDIP[1]
A15	P5_MDIP[2]
A16	P5_MDIP[3]
K13	P5_SIN
J13	P5_SIP
F13	P5_SON
G13	P5_SOP
L14	P5_VDDR09
G7	P6_AVDDH

Pin Number	Pin Name
G8	P6_AVDDH
D8	P6_AVDDL
D9	P6_AVDDL
D10	P6_AVDDT
D11	P6_AVDDT
H10	P6_AVDDR
J10	P6_AVDDS
D22	P6_GPIO[0]
D23	P6_GPIO[1]
B11	P6_MDIN[0]
B10	P6_MDIN[1]
B9	P6_MDIN[2]
B8	P6_MDIN[3]
A11	P6_MDIP[0]
A10	P6_MDIP[1]
A9	P6_MDIP[2]
A8	P6_MDIP[3]
K11	P6_SIN
J11	P6_SIP
F11	P6_SON
G11	P6_SOP
L10	P6_VDDR09
G5	P7_AVDDH
G6	P7_AVDDH
D6	P7_AVDDL
D7	P7_AVDDL
D4	P7_AVDDT
D5	P7_AVDDT

Pin Number	Pin Name
H3	P7_AVDDR
J3	P7_AVDDS
C23	P7_GPIO[0]
C22	P7_GPIO[1]
B3	P7_MDIN[0]
B4	P7_MDIN[1]
B5	P7_MDIN[2]
B6	P7_MDIN[3]
A3	P7_MDIP[0]
A4	P7_MDIP[1]
A5	P7_MDIP[2]
A6	P7_MDIP[3]
J2	P7_SIN
J1	P7_SIP
L2	P7_SON
L1	P7_SOP
K3	P7_VDDR09
E3	RCLK
B1	RESETn
D1	SPI_CLK
E1	SPI_MISO
C1	SPI_MOSI
F1	SPI_SSn
D2	TCK
C2	TDI
E2	TDO
C3	TEST
W22	TEST_CLKN

Pin Number	Pin Name
Y22	TEST_CLKP
D3	TMS
B2	TRSTn
W2	TSTCN
Y2	TSTCP
AA21	TSTPT
F22	VDDOL
G1	VDDOL
V22	VDDOL
V2	VDDOM
G2	VDDOT
W3	VSEL_M
E4	VSEL_T
F2	VSS
F3	VSS
F21	VSS
G3	VSS
G21	VSS
H5	VSS
H6	VSS
H8	VSS
H16	VSS
H18	VSS
H19	VSS
J4	VSS
J5	VSS
J6	VSS
J7	VSS

Pin Number	Pin Name
J8	VSS
J9	VSS
J15	VSS
J16	VSS
J17	VSS
J18	VSS
J19	VSS
J20	VSS
K10	VSS
K14	VSS
L5	VSS
L6	VSS
L7	VSS
L9	VSS
L15	VSS
L17	VSS
L18	VSS
L19	VSS
M3	VSS
M9	VSS
M15	VSS
M21	VSS
N5	VSS
N6	VSS
N7	VSS
N9	VSS
N15	VSS
N17	VSS

Pin Number	Pin Name
N18	VSS
N19	VSS
P10	VSS
P14	VSS
R4	VSS
R5	VSS
R6	VSS
R7	VSS
R8	VSS
R9	VSS
R15	VSS
R16	VSS
R17	VSS
R18	VSS
R19	VSS
R20	VSS
T5	VSS
T6	VSS
T8	VSS
T16	VSS
T18	VSS
T19	VSS
U3	VSS
U21	VSS
V1	VSS
V3	VSS
V21	VSS
AB1	XTAL1

Pin Number	Pin Name
AA1	XTAL2

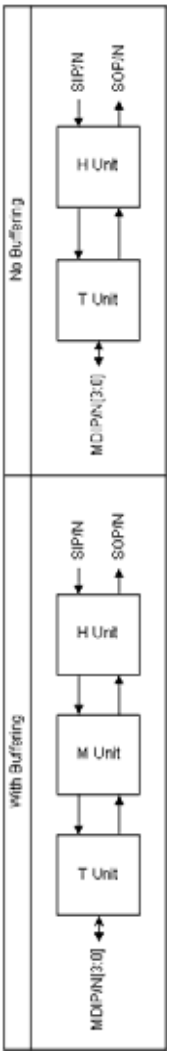
3 Functional Description

This section describes chip-level functionality. Section 4 through Section 6 describe the individual units in detail.

3.1 Data Path

The data path of the 88E2180/88E2110 device flows through the copper interface (T Unit) and the host interface (H Unit). These interfaces are discussed in detail in Section 4 and Section 5, respectively. The internal buffer sits in the (M Unit).

Figure 6: Device Data Path



3.2 Auto-Speed Adjustment

The host interface mode is decided by the media-side speed. For example, when MACTYPE[2:0] is set as 3'b100, the media-side speed is equal or slower than 1G, the host interface becomes SGMII mode. If the line side is 2.5GBASE-T or 5GBASE-T, then the host interface is configured as 2500GBASE-X or 5GBASE-R, respectively.

3.3 Loopback

The T and H Units has the ability to perform MAC loopback and line loopback as shown in Figure 7 for 88E2110 devices and Figure 8 for 88E2180 devices. If MAC loopback is engaged, then loopback speed depends upon the media link speed. If the media link is down, then the MAC interface speed is dependent upon the setting in 31.F000.7:6, Default MAC Interface Speed and in 31.F0A8.1:0, Device Max Speed Limit Control. Only one loopback at a time may be enabled in the PHY.

Table 28: Loopback Control

Register	Function	Setting
3.0000.14	T Unit Deep MAC Loopback	1 = Loopback 0 = Normal
4.0000.14 4.1000.14 4.2000.14	H Unit Deep Line Loopback	1 = Loopback 0 = Normal
4.F003.6	H Unit Deep Line Loopback Ingress Blocking	1 = Block ingress input. 0 = Do not block ingress input.
3.8002.5	T Unit Shallow Line Loopback for 1000/100/10 mode	1 = Loopback 0 = Normal
1.C000.11	T Unit Shallow Line Loopback for 5G/2.5G mode	1 = Loopback 0 = Normal
4.F003.12	H Unit Shallow MAC Loopback	1 = Loopback 0 = Normal
31.F000.7:6	Default MAC Interface Speed	MAC interface speed during link down. 00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps 11 = Speed controlled by 31.F0A8.1:0
31.F0A8.1:0	Device Max Speed Limit Control	Controls the link down maximum speed. 10 = 5 Gbps 11 = 2.5 Gbps

Figure 7: Loopback Paths for 88E2110 Devices

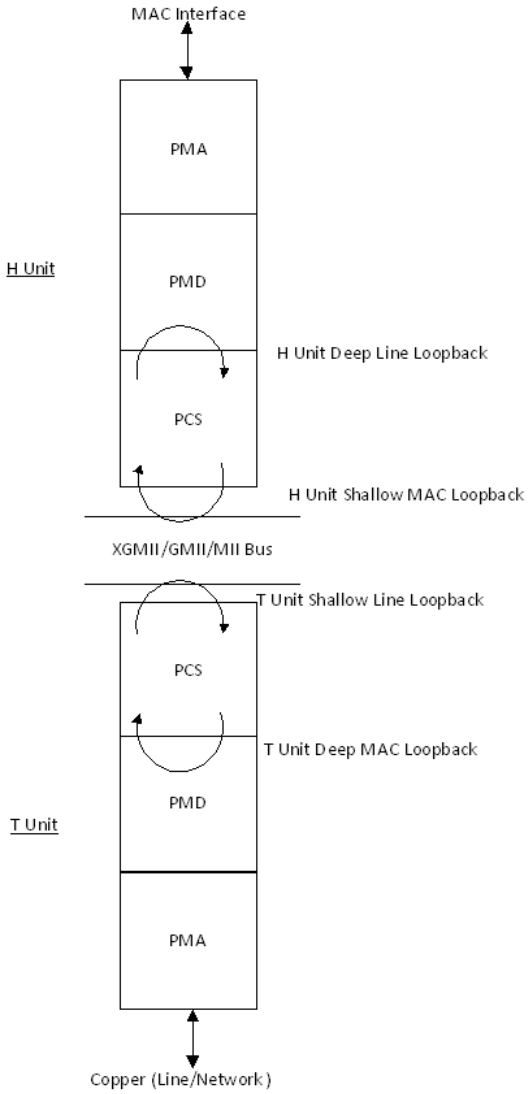
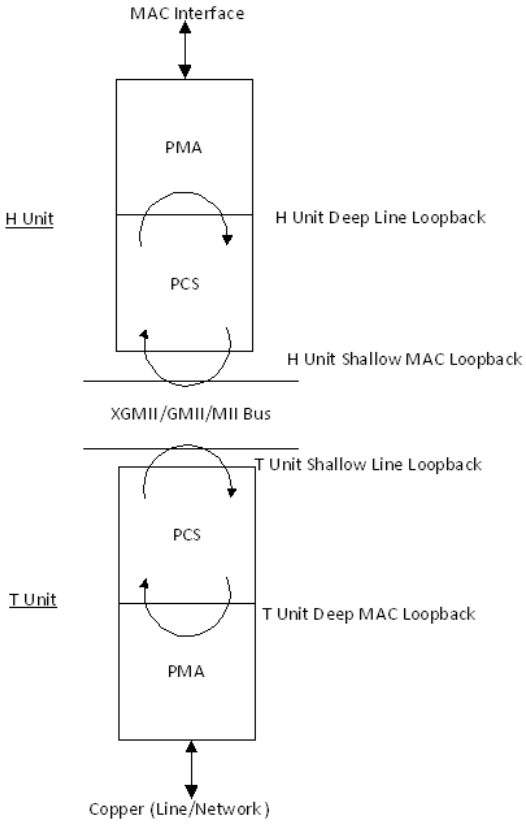


Figure 8: Loopback Paths for 88E2180 Devices



3.3.1 MAC Loopback

The MAC loopback is defined to be looping data from the host interface back to the host interface.

There are two different MAC loopbacks: the H Unit shallow MAC loopback which loops back at the H Unit PCS layer and the T Unit deep MAC loopback which loops back at the T Unit PCS layer.

The H Unit shallow MAC loopback is enabled by setting register 4.F003.12 and the T Unit deep MAC loopback is enabled by setting register 3.0000.14. Register bit 4.F003.6 is used to control whether data passes through or is blocked during the H Unit deep line loopback. The T Unit deep MAC loopback is not supported when the T Unit media-side link is down.

3.3.2 Line Loopback

The line loopback is defined to be looping the data that is received on MDIP/N[3:0] and back out on MDIP/N[3:0]. There are two different line loopbacks: the T Unit shallow line loopback which loops back at the T Unit PCS layer and the H Unit deep line loopback which loops back at the H Unit PCS layer. The shallow line loopback is enabled by setting register 1.C000.11 for speed 2.5G mode and register 3.8002.5 for 1G, 100M, and 10M mode.

The H Unit deep line loopback is enabled by setting register 4.1000.14 or 4.2000.14.

The speed of the loopback is determined by the active link speed.

3.4 FIFO Overview

The PHY has several FIFOs to compensate for frequency differences among the various units. The FIFOs are placed on the transmit path of each unit.

3.5 Configuration and Resets

The device can be configured using the following:

- Hardware configuration strap options
- MDC/MDIO register access

All hardware configuration options can be overwritten via the other methods except PHYADR and MDIO.

This section will discuss the hardware configuration.

3.5.1 Hardware and Software Resets

RESETn is the hardware reset pin for the entire 88E2180/88E2110 device. To ensure that the stopping of the hardware configuration is correct, it is required that upon system power-up a reset signal be applied to RESETn, or the RESETn pin be held low until all the power rails are settled down.

In addition to the hardware reset pin (RESETn), there are several software reset bits that resets various parts of the 88E2180/88E2110 device.

A hardware reset will reset the entire chip and initialize all the registers to their hardware reset default.

A software reset has a similar effect on the affected units as a hardware reset except all Retain-type registers will hold their value, and the Update registers will have the previously written values take effect.

Register 31.F001.14 is a software bit that emulates the hardware reset. Setting the bit to 1 will reset the entire 88E2180/88E2110 device (all ports) as if the RESETn pin is asserted. All ports have a register 31.F001.14. Writing 1 to register 31.F001.14 from any port will result in reseting the entire 88E2180/88E2110 device. When triggered, registers are not accessible through the MDIO until the chip reset completes.

Note

Since the 88E2180/88E2110 device operates by default in MDIO preamble suppression mode, there should be no MDIO activities on the device's interface before the device reset completes, even for the MDIO commands with different PHY address.

Setting register 1.C04A.15 to 1 software resets the entire port except for the T Unit. The T Unit will briefly power down and Auto-Negotiation will restart.

Setting registers 1.C04A.13, 1.0000.15, 3.0000.15, or 7.0000.15 to 1 software resets the T Unit only.

Setting registers 4.0000.15, 4.1000.15, or 4.2000.15 to 1 software resets the H Unit only.

3.5.2 Hardware Configuration

After the de-assertion of RESETn, the device will be hardware configured through the CONFIG[2:0] pins. Each pin is used to configure 3 bits. The 3-bit value is set depending on which GPIO or MFIOS pin or static level is connected to the CONFIG pins at the de-assertion of hardware reset. The three configuration bits per pin mapping is shown in Table 29 for the 88E2110 device and in Table 31 for the device. The three bit mapping during hardware configuration is shown in Table 30 for the device and in Table 32 for the Table 32 device.

For the 88E2180 device, the host unit has the following MACTYPE modes, which can be read via 1.C04A.[2:0]:

- 000 = Reserved
- 001 = Reserved
- 010 = Reserved
- 011 = Reserved
- 100 = 5GBASE-R/2500BASE-X/SGMII Auto-Negotiation On
- 101 = 5GBASE-R/2500BASE-X/SGMII Auto-Negotiation Off
- 110 = Reserved
- 111 = Reserved

For the 88E2110 device, the host unit has the following MAC_SELECT modes, which can be read via 1.C04A.[2:0]:

- 000 = Reserved
- 001 = Reserved
- 010 = Reserved
- 011 = Reserved
- 100 = 5GBASE-R/2500BASE-X/SGMII Auto-Negotiation On
- 101 = 5GBASE-R/2500BASE-X/SGMII Auto-Negotiation Off
- 110 = Reserved
- 111 = Reserved

The default POR value of 1.C04A.2:0 is decided by the strap configuration for all ports.

To set different MACTYPE modes for each port instead of using POR strap option for the 88E2180 device, 1.C0A4.2:0 should be written. Register 1.C04A.2:0 can be read and MACTYPE can be updated only after applying the software reset (1.C0A4.15).

The default of PDSTATE is from the strap option (Power Up State at POR) for the 88E2180 device and is 1'b0 (Power Up State at POR) for the 88E2110 device.

Table 29: 88E2110 Device Configuration Mapping

Pin	Bit2	Bit 1	Bit0
CONFIG[0]	PHYAD[4]	PHYAD[3]	PHYAD[2]
CONFIG[1]	PHYAD[1]	PHYAD[0]	MDIO/I^{2}C
CONFIG[2]	FACTORY_TEST	MAC_SELECT	SPI_CONFIG

Table 30: 88E2110 Device Three Bit Mapping

Pin	Bit[2:0]
VSS	000
GPIO[1]	001
GPIO[2]	010
GPIO[3]	011
GPIO[4]	100
MFIOS[0]	101
MFIOS[1]	110
VDDO	111

Table 31: 88E2180 Device Configuration Mapping

Pin	Bit 2	Bit1	Bit 0
CONFIG[0]	PHYAD[4]	PHYAD[3]	RESERVED
CONFIG[1]	MACTYPE[2]	MACTYPE[1]	MACTYPE[0]
CONFIG[2]	FACTORY_TEST	PDSTATE	SPI_CONFIG

Table 32: 88E2180 Device Three Bit Mapping

Pin	Bit[2:0]
VSS	000
P0_GPIO[1]	001
P1_GPIO[1]	010
P6_GPIO[1]	011
P7_GPIO[1]	100
MFIOS[0]	101
MFIOS[1]	110
VDDO	111

Table 33: 88E2180 Configuration Definition

Bits	Definition	Register Affected
PHYAD[4:0]	PHY Address PHYAD[4:3]	
MACTYPE[2:0]	000 = SXGMII 001 = Reserved 010 = Reserved 011 = Reserved 100 = 5GR/2.5GX/SGMII Auto-Negotiation On 101 = 5GR/2.5GX/SGMII Auto-Negotiation Off 110 = Reserved 111 = Reserved **NOTE:** To program MACTYPE, register 1.C04A.2:0 should be written. Register 1.C04A.2:0 can be read and MACTYPE can be updated only after applying the software reset (1.C04A.15). Refer to Table 35 for details.	Refer to Table 35 for details.
FACTORY_TEST	Factory Test Mode 0 = Normal mode (default) 1 = Test mode (reserved for Marvell)	None
PDSTATE	0 = Start In Power Up State 1 = Start In Power Down State	T Unit 1.0000.11 <= PDSTATE 3.0000.11 <= PDSTATE
SPI_CONFIG	Determines whether the embedded processor loads the firmware image from flash or waits for the image to be downloaded via MDIO. 0 = Download code via SPI. 1 = Wait for download via MDIO.	C Unit 31.F008.5 <= SPI_CONFIG To override this configuration, change 31.F008.5 and then perform a T Unit hardware reset using 31.F001.12.

Table 34: 88E2110 Configuration Definition

Bits	Definition	Register Affected
PHYAD[4:0]	PHY Address PHYAD[4:0]	
MAC_SELECT	The strap option MAC_SELECT decides the default value of MACTYPE[2] at power on reset (POR). When MAC_SELECT = 0, MACTYPE[2:0] is set as 3'b100 at POR. When MAC_SELECT = 1, MACTYPE[2:0] is set as 3'b000 at POR. The value of MACTYPE[2:0] can be changed by programming 1.C04A.2:0 followed by a port soft reset (1.C04A.15). 000 = SXGMII 001 = Reserved 010 = Reserved 011 = Reserved 100 = 5GBASE-R/2500BASE-X/SGMII Auto-Negotiation On 101 = 5GBASE-R/2500BASE-X/SGMII Auto-Negotiation Off 110 = Reserved 111 = Reserved	1.C04A.2:0 4.2000.12
MDIO/I^2C	MDIO or I^2C selection for MDC and MDIO pins 0 = MDC/MDIO 1 = SCL/SDA (I^2C/TWSI)	None
FACTORY_TEST	Factory Test Mode 0 = Normal mode (default) 1 = Test mode (reserved for Marvell)	None
SPI_CONFIG	Determines whether the embedded processor loads the firmware image from flash or waits for the image to be downloaded via MDIO. 0 = Download code via SPI. 1 = Wait for download via MDIO.	C Unit 31.F008.5 <= SPI_CONFIG To override this configuration, change 31.F008.5 and then perform a T Unit hardware reset using 31.F001.12.

Table 35: Possible MACTYPE Change Combinations for the 88E2180 Device

From		To	New MACTYPE (Selected Through 1.C04A.2:0 Programming After a Hardware Reset)							
			000	001	010	011	100	101	110	111
Current MACTYPE (selected through hardware strapping)	000		Allowed	Prohibited	Prohibited	Reserved	Allowed	Allowed	Allowed	Reserved
	001		Allowed (Note 1)	Limited (Note 2)	Prohibited		Allowed (Note 1)	Allowed (Note 1)	Allowed (Note 1)	
	010		Allowed (Note 1)	Reserved	Reserved		Allowed (Note 1)	Allowed (Note 1)	Reserved	
	011		Reserved							
	100		Allowed	Prohibited	Prohibited	Reserved	Allowed	Allowed	Allowed	Reserved
	101		Allowed	Prohibited	Prohibited		Allowed	Allowed	Allowed	
	110		Allowed	Prohibited	Prohibited		Allowed	Allowed	Allowed	
	111		Reserved							
			NOTE 1: For 88E2180/88E2110 devices, if MACTYPE mode is changed by programming register 1.C04A manually, then the PCS scrambler bypass should be disabled by setting register 4.9003.1 to 0.							
			NOTE 2: To apply the port soft reset, register 1.C04A.4 should be set instead of register 1.C04A.15 for 88E2180/88E2110 devices.							

3.6 MDC/MDIO Register Access

The management interface provides access to the internal registers via the MDC and MDIO pins and is compliant with IEEE 802.3 Clause 45. MDC is the management data clock input and it can run from DC to a maximum continuous rate of 12.5 MHz. At high MDIO fanouts, the maximum rate may be decreased depending on the output loading. MDIO is the management data input/output and is a bi-directional signal that runs synchronously to MDC.

The MDIO does not require a pull-up resistor. If another open-drain device driving MDIO requires a pull-up resistor, then it should drive or be pulled up to the same voltage value as the VDDOM rail.

PHY address is configured during the hardware reset sequence. Refer to Section 3.5, Configuration and Resets, on page 62 for detailed information on how to configure PHY addresses.

Typical read and write operations on the management interface are shown in Figure 9 and Figure 10. The MDIO interface supports preamble suppression operation by default. Between subsequence MDIO access sequences, there must be at least 1 IDLE MDC cycle (MDIO driven high). So, the minimum MDC clock cycle for a MDIO operation will 33 cycles. The start of a MDIO operation is marked by the insertion of two MDC cycle with MDIO driven to zero as this will mark the start of frame (ST) pattern as defined in IEEE 802.3 standard. All the required serial management registers are implemented as well as several optional registers. A description of the registers can be found in the *88E2181/88E2180/88E2111/88E2110 Register Description* (MV-S111371-00).

Figure 9: Typical MDC/MDIO Read Operation

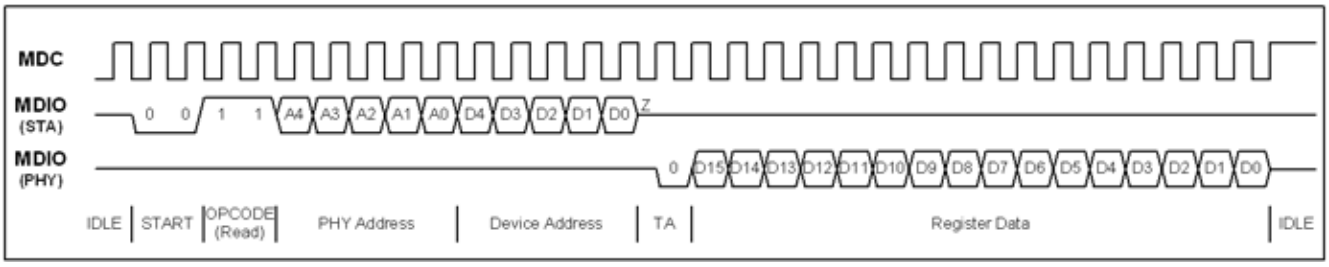
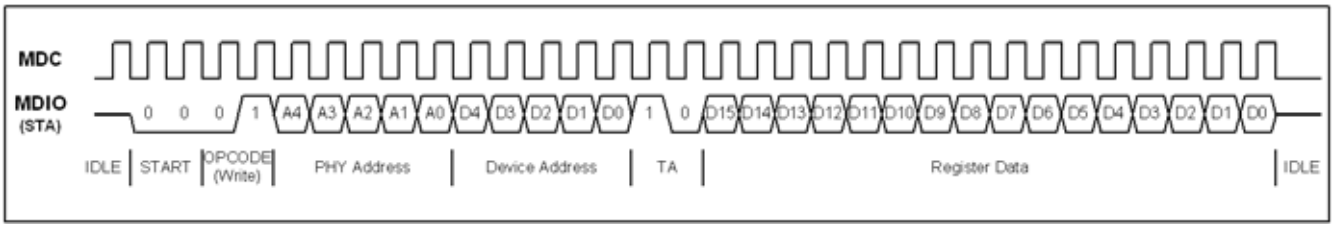


Figure 10: Typical MDC/MDIO Write Operation



3.6.1 Clause 45 MDIO Framing

The MDIO interface frame structure is compatible with that defined in Clause 22 such that the two management interfaces can coexist on the same MDIO bus.

The extensions for Clause 45 MDIO indirect register accesses are specified in Table 36.

Table 36: Extensions for Management Frame Format for Indirect Access

Frame	PRE	ST	OP	PHYAD	DEVADR	TA	ADDRESS/DATA	Idle
Address	1...1	00	00	PPPPP	DDDDD	10	AAAAAAAAAAAAAAAA	Z
Write	1...1	00	01	PPPPP	DDDDD	10	DDDDDDDDDDDDDDDD	Z
Read	1...1	00	11	PPPPP	DDDDD	Z0	DDDDDDDDDDDDDDDD	Z
Read Increment	1...1	00	10	PPPPP	DDDDD	Z0	DDDDDDDDDDDDDDDD	Z

The MDIO implements a 16-bit address register that stores the address of the register to be accessed. For an address cycle, it contains the address of the register to be accessed on the next cycle. For read, write, post-read-increment-address cycles, the field contains the data for the register. At power up and reset, the contents of the register are undefined.

Write, read, and post-read-increment-address frames access the address register, though write and read frames do not modify the contents of the address register.

3.6.1.1 Clause 22 Access to Clause 45 MDIO Manageable Device (MMD)

Clause 22 provides access to registers in a Clause 45 MDIO MMD space using registers 13 and 14. Register 22.7:0 must be set to 0 to 7. If register 22.7:0 is 8 to 255, then the MMD registers are not accessible. See Table 37.

The MMD Access Control Register and Address and Data Register definitions are shown in Table 38 and Table 39.

Table 37: Clause 22 Registers Not Defined in Clause 45

Function	Clause 45 (Device Register Bits)	Clause 22 (Device Register Bits)
IEEE Test Mode	7.8000.15:13	9.15:13
Isolate	7.8000.10	0.10
1000BASE-T Full Duplex	7.8000.9	9.9
1000BASE-T Half Duplex	7.8000.8	9.8
Collision	7.8000.7	0.7
Duplex	7.8000.4	0.8
Jabber Status	7.8000.1	1.1
Parallel Detection Fault	7.8000.0	6.4
1000BASE-T MASTER/SLAVE Configuration Fault[1]	7.8001.15	10.15

Table 37: Clause 22 Registers Not Defined in Clause 45 (Continued)

Function	Clause 45 (Device Register Bits)	Clause 22 (Device Register Bits)
1000BASE-T MASTER/SLAVE Configuration Resolution[1]	7.8001.14	10.14
1000BASE-T Local Receiver Status[1]	7.8001.13	10.13
1000BASE-T Remote Receiver Status[1]	7.8001.12	10.12
Link Partner 1000BASE-T Full Duplex Capability	7.8001.11	10.11
Link Partner 1000BASE-T Half Duplex Capability	7.8001.10	10.10
Link Partner Next Page Able	7.8001.9	6.3
Link Partner Auto-Negotiation Able[1]	7.8001.8	6.0
Idle Error Count	7.8001.7:0	10.7:0
Various Abilities	7.8002.15:5	1.15:6,0
Local Next Page Able	7.8002.4	6.2
Various Abilities	7.8002.3:0	15.15:12

1. This bit's locations apply only when 7.0001.1 Extended Page Status = 0 meaning regular next pages are used. Otherwise these bits are defined for Extended Next Pages in 7.0021 and 7.0001.

Table 38: MMD Access Control Register
Page 0, Register 13

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Function	R/W	0x0	0x0	15:14 00 = Address 01 = Data, no post increment 10 = Data, post increment on reads and writes 11 = Data, post increment on writes only
13:5	Reserved	RO	0x000	0x000	Reserved
4:0	DEVAD	R/W	0x00	0x00	Device address

Table 39: MMD Access Address/Data Register
Page 0, Register 14

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Address Data	R/W	0x0000	0x0000	If 13.15:14 = 00, MMD DEVAD's address register. Otherwise, MMD DEVAD's data register as indicated by the contents of its address register.

Write Operation

To write to the MMD register access:

1. To register 13, write the Function field to 00 (address) and DEVAD field with the device address value.
2. To register 14, write the MMD's register address value.
3. To register 13, write the Function field to 01 (Data, no post increment) and DEVAD field to the same device address value (as step #1).
4. To register 14, write the content to be written to the selected MMD's register.

Step 1 and 2 can be skipped if the MMD's address register was previously configured.

Read Operation

To read from the MMD register access:

1. To register 13, write the Function field to 00 (address) and DEVAD field with the device address value.
2. To register 14, write the MMD's register address value.
3. To register 13, write the Function field to 01 (Data, no post increment) and DEVAD field to the same device address value (as step #1).
4. From register 14, read the content from the selected MMD's register.

Step 1 and 2 can be skipped if the MMD's address register was previously configured.

Write/Read Operation with Post Increment Function

Function 10 can be used to increment the address after each read and write access. Function 11 can be used to increment the address after write operation only. Function 11 enables a read-modify-write capability for successive addressed registers within the MMD.

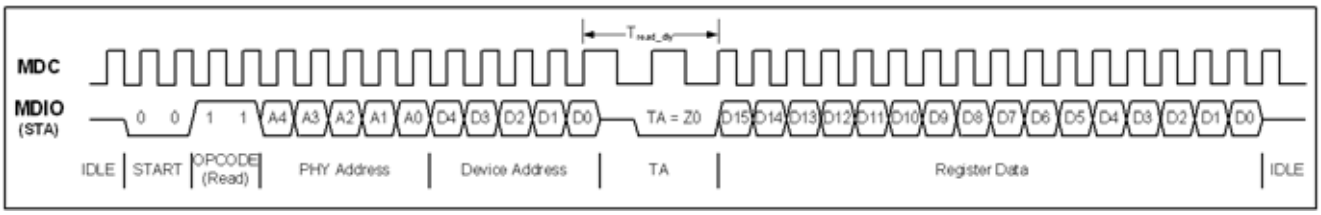
3.6.2 30 MHz High-Speed MDC/MDIO Management Interface Protocol

In addition to supporting the typical MDC/MDIO protocol, the 88E2180/88E2110 device has the capability to run MDC down to a clock period of 35 ns. The write operation can operate normally at this speed; however, for the read operation, the MDC clock cycle must be slowed down for the TA period as shown in the Figure 11.

During read operations, the MDC clock must slow down so that the PHY has enough time to fetch the data.

See Section 6.5.4, MDC/MDIO Management Interface Timing, on page 141 for timing details.

Figure 11: 30 MHz MDC/MDIO Read Operation



3.6.3 XMDIO Register Access via Clause 22 MDIO Protocol

Clause 22 provides access to registers in a Clause 45 MMD using registers 13 and 14. This informative annex provides users with some insight into how these registers can be utilized to access Clause 45 MMD registers. For the purpose of accessing registers in a Clause 45 MMD, access to registers 13 and 14 should be performed atomically to avoid the possibility of another process changing the Function, DEVAD or address fields within the MMD. This is the same requirement with Clause 45 access.

3.6.3.1 Write Operation

To write a Clause 45 register using the Clause 22 access mechanism, perform the following accesses using the appropriate PHY address for the PHY of interest:

a) To register 13, write the Function field to 00 (address) and DEVAD field to the device address value for the desired MMD.
b) To register 14, write the desired address value to the MMD's address register;
c) To register 13, write the Function field to 01 (Data, no post increment) and DEVAD field to the same device address value for the selected MMD.
d) To register 14, write the content of the MMD's selected register. Step a and step b can be skipped if the MMD's address register was previously configured.

3.6.3.2 Read Operation

To read a Clause 45 register using the Clause 22 access mechanism, perform the following accesses using the appropriate PHY address for the PHY of interest:

a) To register 13, write the Function field to 00 (address) and DEVAD field to the device address value for the desired MMD.
b) To register 14, write the desired address value to the MMD's address register;
c) To register 13, write the Function field to 01 (Data, no post increment) and DEVAD field to the same device address value for the desired MMD.
d) From register 14, read the content of the MMD's selected register. Step a and step b can be skipped if the MMD's address register was previously configured.

3.6.3.3 Address

While the Function field contains the value 00 (address):

a) Subsequent writes to register 14 continue to rewrite MMD DEVAD's address register.
b) Subsequent reads from register 14 continue to reread MMD DEVAD's address register.

Data, No Post Increment

While the Function field contains the value 01 (Data, no post increment):

a) Subsequent writes to register 14 continue to rewrite the data register selected by the value in MMD DEVAD's address register.
b) Subsequent reads from register 14 continue to reread the data register selected by the value in MMD DEVAD's address register.

Data, Post increment on Reads and Writes

While the Function field contains the value 10 (Data, post increment on reads and writes):

a) Subsequent writes to register 14 write the next higher addressed data register selected by the value in MMD DEVAD's address register, that is, MMD DEVAD's address register is incremented after each access.
b) Subsequent reads from register 14 read the next higher addressed data register selected by the value in MMD DEVAD's address register, that is, MMD DEVAD's address register is incremented after each access.

Data, Post Increment on Writes Only

While the Function field contains the value 11 (Data, post increment on writes only):

a) Subsequent writes to register 14 write the next higher addressed data register selected by the value in MMD DEVAD's address register, that is, MMD DEVAD's address register is incremented after each access.
b) Subsequent reads from register 14 continue to reread the data register selected by the value in MMD DEVAD's address register. This function enables a read-modify-write capability for successively addressed registers within a MMD.

3.7 Two-Wire Serial Interface (TWSI) Register Access for the 88E2110 Device

Registers can also be accessed over the Two-Wire Serial Interface (TWSI) in the 88E2110 instead of MDC/MDIO.

If the I^2C option is selected in the hardware strap option, then MDC and MDIO pins are configured as SCL and SDA, respectively. This interface is a slave interface only.

The TWSI features are as follows:

- 7-bit device address and 8-bit data transfers
- 100 Kbps mode (Standard mode, SSCL up to 100 kHz)
- 400 Kbps mode (Fast mode, SSCL up to 400 kHz)
- No SCL stretching by the slave

3.7.1 Clause 45 Encapsulation

In Clause 45 encapsulation, the DEVAD[4:0] is introduced. REGAD is extended to 16 bits. The concepts of repeated read or write as well as write post-increment are introduced.

All I^2C transactions will encapsulate PHYAD and DEVAD along with the R/W bit and 3-bit instruction in the first 2 bytes as shown in Figure 12. The INS[2:0] definition is summarized in Table 40.

Figure 12: First Two Bytes of All Transactions

Table 40: INS[2:0] Definition

INS[2:0]	Header	Address
000	Abbreviated Header — Use stored REGAD	Stored REGAD unchanged
001	Abbreviated Header — Use stored REGAD	Post-increment REGAD
010	Full Header — Use specified REGAD	Stored REGAD unchanged
011	Full Header — Use specified REGAD	Post-increment REGAD
100	Dummy Write	–
101	Reserved	Reserved
110	Reserved	Reserved
111	Reserved	Reserved

In Clause 45 MDIO, access the REGAD[15:0] is set independently of the data access. As a result, each DEVAD that is supported must have its own REGAD[15:0] holding register. This also applies in the Clause 45 encapsulation over I^2C. There are two methods to specify the REGAD. The first method is to fully specify the REGAD in the transaction as shown in Figure 13 and Figure 17. The second method is to use abbreviated headers where the stored REGAD register for the corresponding DEVAD is used as shown in Figure 15.

The Clause 45 encapsulation does not differentiate between random versus sequential read/write. All reads and writes can be sustained by the master by not sending a stop bit. So one or more 16-bit words can be passed with the same encapsulated header. REGAD may be post-incremented after each 16-bit word transfer depending on the INS[2:0].

All 16-bit read/write operations operate atomically. If a write transaction terminates with only 8 bits of the 16-bit word written in, then the 8 bits are discarded and REGAD will not post-increment (if selected). If a read transaction terminates with only 8 bits of the 16-bit word read, then the other 8-bits will be lost forever (such as in the case of a clear on read register) and REGAD will not post-increment (if selected).

All read transactions must read least one byte of data. Write transactions can be dummy writes if no data is transferred. If no data is transferred then no post-incrementing will occur.

The slave will acknowledge the first byte only when the following condition is met:

- The PHYAD[4:0] matches and the two most significant bits are 10 (binary).

The slave will acknowledge the second byte only if all the following conditions are met:

- The first byte was acknowledged by the slave.
- The DEVAD[4:0] is among the supported device addresses in the PHY
- INS[2] bit is a 0 (that is, it will not respond to reserved instructions).

The slave will acknowledge the third and subsequent bytes if all the following conditions are met:

- The first and second bytes were acknowledged by the slave.
- The transaction is a write transaction.
- A start bit or stop bit is not detected since the second acknowledge.

The slave will acknowledge the third and fourth bytes if all the following conditions are met:

- The first and second bytes was acknowledged by the slave.
- The instruction indicates a full header is being sent.
- A start bit (not counting the one at the beginning of the current transaction) or stop bit is not detected since the second acknowledge by the slave.

The slave will output 8 bit data if all the following conditions are met:

- The first and second bytes was acknowledged by the slave.
- The third and fourth bytes was acknowledge by the slave if instruction indicates a full header is being sent.
- The transaction is a read transaction.
- A start bit (not counting the one at the beginning of the current transaction), stop bit or no-acknowledge is not detected.

The slave will abort the current 16-bit transfer and will not post-increment the REGAD if a stop bit or no-acknowledge is prematurely detected. All further activities on the bus is ignored by the slave until a start bit is detected.

If the first byte of the REGAD is written and the transaction terminates without the second byte of REGAD being written, then the internal REGAD register will not update.

If a start bit is prematurely detected, then the slave will abort the current 16-bit transfer and will not post-increment the REGAD. This premature start bit will immediately trigger the start of the next I^2C transaction.

If post-increment is active and the REGAD is 0xFFFF, then the REGAD will roll over to 0x0000.

Figure 13: Write, Full Header, Retain REGAD

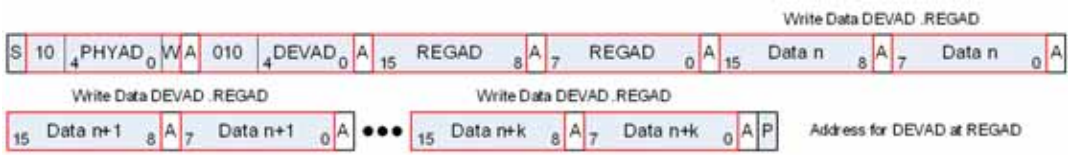


Figure 14: Write, Full Header, Post-Increment

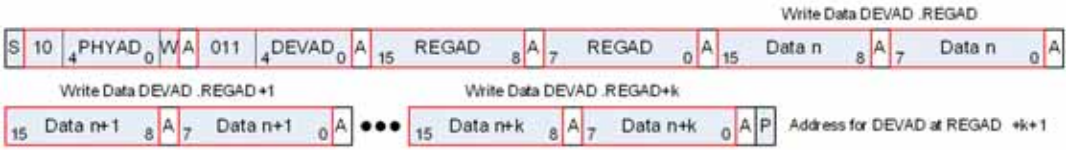


Figure 15: Write, Abbreviated Header, Retain REGAD

Figure 16: Write, Abbreviated Header, Post-Increment

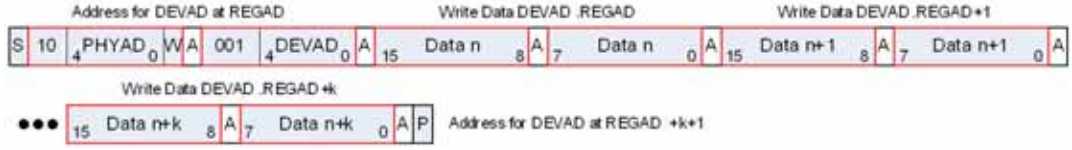


Figure 17: Read, Full Header, Retain REGAD

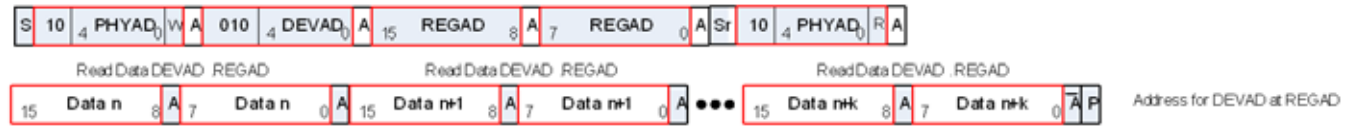


Figure 18: Read, Full Header, Post-Increment

Figure 19: Read, Abbreviated Header, Retain REGAD

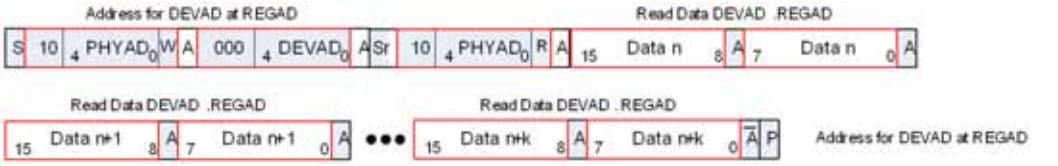
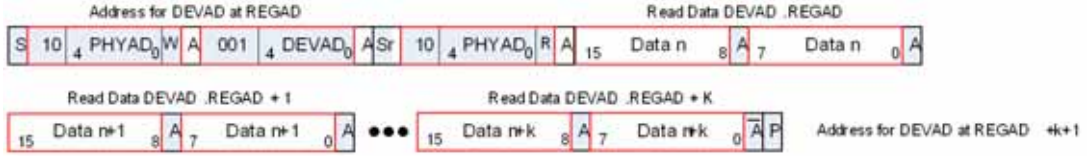


Figure 20: Read, Abbreviated Header, Post-Increment



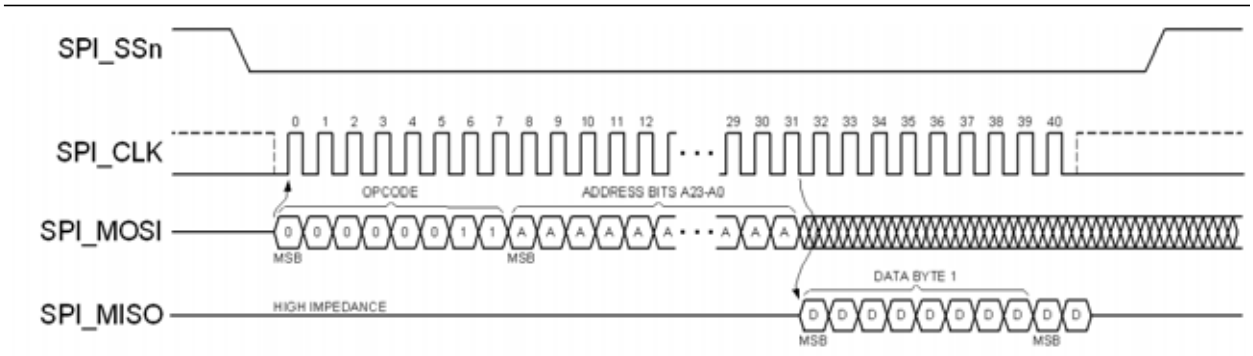
3.8 Firmware Loading

3.8.1 Flash Memory Interface

The device can download code from an external flash memory via the Serial Peripheral Interface bus (SPI) into the processor memory. The Serial Peripheral Interface bus (SPI) is a 4-wire serial communications interface used by many microprocessor peripheral chips.When the hardware configuration SPI_CONFIG strap bit is set to 0, the device will download code after the de-assertion of RESETn.

The SPI controller will issue a read array command starting from address 0x000000 as shown in Figure 21. The number of bytes read will be determined by the values contained in the flash image header.

Figure 21: SPI Read Array



The device is always the master and the flash is the slave. Chip select (output SPI_SSn) is driven low by the device during every flash access.

3.8.2 Firmware Download to RAM

As an alternative to using a flash device for storing the firmware image, the image may be downloaded directly to the microcontroller RAM by the host using the Serial Management Interface (MDC/MDIO). In this case, the SPI_CONFIG strap bit must be set to 1 and the device will wait for the firmware to be downloaded to RAM. Refer to the software API package for instructions on downloading firmware to RAM via the Serial Management Interface.

3.9 Power Management

This section discusses the general power down for the 88E2180/88E2110 device. See the unit level sections for details on advanced power management of each unit.

3.9.1 Manual Power Down

The 88E2180/88E2110 device will automatically power down unused circuits without the need for the user to intervene. The following registers can be set to force the units to power down.

Setting register 31.F001.11 to 1 powers down the entire port. Perform a hardware reset or reset via an MDC/MDIO write to clear this bit.

Setting register 1.0000.11 or 3.0000.11 to 1 powers down the T Unit only.

Setting registers 4.0000.11, 4.1000.11, or 4.2000.11 to 1 powers down the H Unit only.

3.9.2 MAC Interface Power Down

Register 31.F000.3 controls whether the H Unit is powered down while the link is down. To update the H Unit, a global software reset to 1.C04A.15 must be applied.

3.10 GPIO

The GPIO function enables the GPIO[1:0] pins, as well as GPIO[5:2] pins in the case of 88E2110, so that they can be configured to output LED[1:0], respectively. Each pin can operate bi-directionally and can be individually configured.

3.10.1 Enabling the GPIO Function

The GPIO[1:0] pins, as well as GPIO[5:2] pins in the case of 88E2110, can be controlled via the GPIO registers.

3.10.2 Controlling and Sensing

Register 31.F013 controls whether the GPIO[1:0] pins, as well as GPIO[5:2] pins in the case of 88E2110, are inputs or outputs. Each pin can be individually controlled.

Internally for the 88E2180 device, there are 4 LED control modules. The LED out can be multiplexed via Serial LED or GPIO pins. Register 31.F012 allows the pins to be controlled and sensed.

When configured as input, a read to register 31.F012 will return the real-time sampled state of the pin at the time of the read. A write will write the output register but have no immediate effect on the pin since the pin is configured to be an input. The input is sampled once every 38.4 ns.

When configured as output, a read to register 31.F012 will return the value in the output register. A write will write the output register which will in turn drive the state of the pin.

3.10.3 GPIO Interrupts

When the pins are configured as input, several types of interrupt events can be generated. Registers 31.F014 and 31.F016 allow each pin to be configured to generate interrupt on one of five types of events: Low Level, High Level, High-to-Low Transition, Low-to-High Transition, and Transitions on Either Edge. The interrupt generation can also be disabled.

When an interrupt event is generated, it is latched high in register 31.F011. The register bits will remain high until read.

The INT pin can be asserted when interrupt events occur. register 31.F010 sets the interrupt enable. Registers 31.F010 and 31.F011 are bitwise AND together. If the result is non-zero, then the INT pin will assert.

If a previous interrupt event occurred but is not read, then the register will retain its value until read. That is, if an interrupt event occurred while the pin is configured as an input, then the interrupt status bit will be set. If subsequently the pin is set to an output, then the interrupt status bit will remain set until it is read.

When changing a pin from output to input, an edge-triggered event will not be generated on the transition. For example, if the pin is configured as an output and is driven low and there is a pull-up attached to the pin. When the pin is configured as an input (to tri-state the pin) there will be a low to high transition. This low-to-high transition will not trigger an edge event. Subsequent transitions with the pin configured as input will trigger edge events.

3.11 LED

The 88E2180/88E2110 device has 4 LED modules and LED[3:0] signals the 88E2180/88E2110 device inside, but there are no direct LED[3:0] output pins. Instead, for the 88E2110 the LED[3:0] can be output via the MFIOS[2:0] and GPIO[3] pins and the 88E2180 LED[3:0] can be output via Serial LED or GPIO pins. Registers 31.F020 through 31.F027 control the operation of the LED pins.

Figure 22 shows the general chaining of function for the LEDs for the 88E2110 device and Figure 23 shows the general chaining of function for the LEDs for the 88E2180 device. The various functions are described in the following sections.

Figure 22: LED Chain for the 88E2110 Device

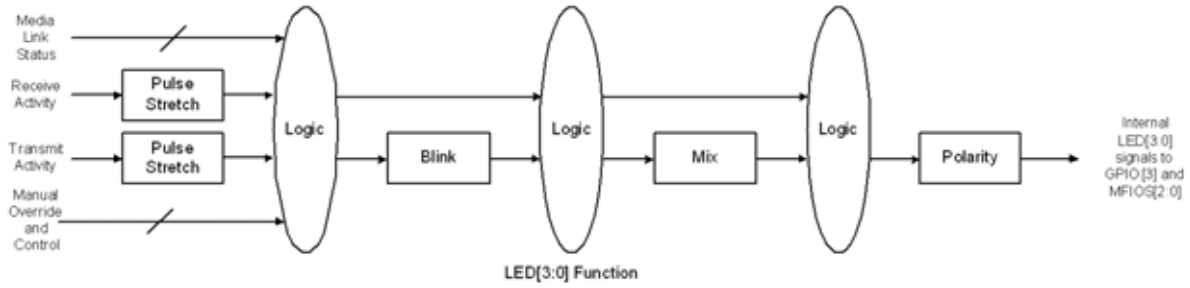
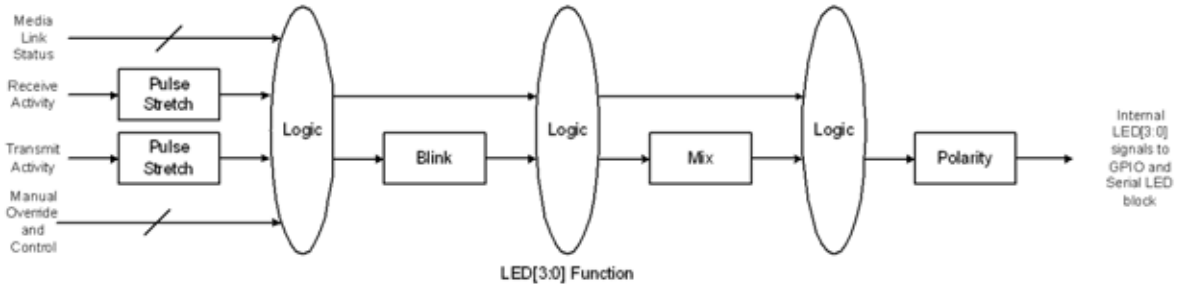


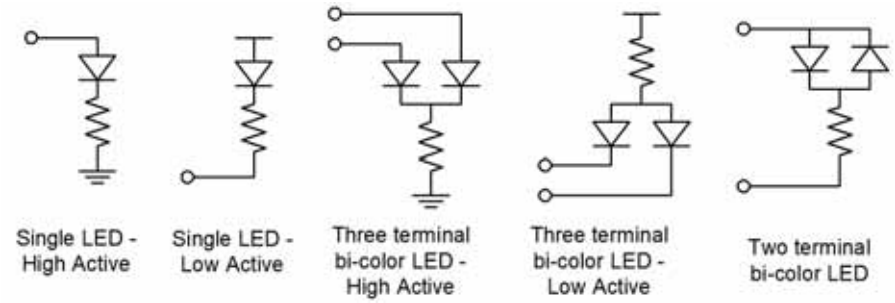
Figure 23: LED Chain for the 88E2180 Device



3.11.1 LED Polarity

There are a variety of methods to hook up the LEDs. Some examples are shown in Figure 24. Registers 31.F023.1:0, 31.F022.1:0, 31.F021.1:0, and 31.F020.1:0 specify the output polarity for the LED[3:0] function to accommodate a variety of installation options. The lower bit of each pair specified the on (active) state of the LED, either high or low. The upper bit of each pair specifies whether the off state of the LED should be driven to the opposite level of the on state or Hi-Z. The Hi-Z state is useful in cases such the LOS and INIT function where the inactive state is Hi-Z.

Figure 24: Various LED Hookup Configurations



3.11.2 Pulse Stretching and Blinking

Register 31.F027.14:12 specifies the pulse stretching duration of a particular activity. Only the transmit activity, receive activity, collision activity, and (transmit or receive) activity are stretched. All other statuses are not stretched since they are static in nature and no stretching is required.

Some status will require a blinking state instead of a solid on state. Registers 31.F027.10:8 and 31.F027.6:4 specify the two blink rates. The pulse stretching is applied first and the blinking will reflect the duration of the stretched pulse.

Registers 31.F020.2, 31.F021.2, 31.F022.2, and 31.F023.2 select which of the two blink rates to use for LED[0] to LED[3], respectively.

- 0 = Select Blink Rate 1
- 1 = Select Blink Rate 2

The stretched/blinked output will then be mixed if needed (Section 3.11.3) and then inverted/Hi-Z according to the polarity described in section (Section 3.11.1).

3.11.3 Bi-Color LED Mixing

In the dual-LED modes, the mixing function allows the two colors of the LED to be mixed to form a third color. This is useful since the PHY supports 10/100 Mbps, 1G and 2.5G operation speeds. Register 31.F026.7:4 controls the amount to mix in the LED[3], and LED[1] signals. Register 31.F026.3:0 controls the amount to mix in the LED[2], and LED[0] signals. The mixing is determined by the percentage of time the LED is on during the active state. The percentage is selectable in 12.5% increments.

There are two types of bi-color LEDs: three-terminal type, and two-terminal type. For example, the third and fourth LED block from the left in Figure 24 illustrates three terminal types, and the type located on the far right is the two-terminal type. In the three-terminal type, both of the LEDs can be turned on at the same time. So the sum of the percentage specified by registers 31.F026.7:4 and 31.F026.3:0 can exceed 100%. However, in the two-terminal type, the sum should never exceed 100% since only one LED can be turned on at any given time.

The mixing only applies when register 31.F020.12:8 or 31.F022.12:8 is set to 11xxx. Mixing single LED modes is not permitted.

The behavior for the various dual LED modes are described in Table 41.

Table 41: Dual LED Mode Behavior

Dual Mode Description	Blink Mix		Solid Mix		Speed/EEE Type 1		Speed Type1		Speed/EEE Type 2		Speed Type 2	
31.F020, 31.F022, bits 12:8	11010		11011		11100		11101		11110		11111	
Current State	LED3 LED1	LED2 LED0	LED3 LED1	LED2 LED0	LED3 LED1	LED2 LED0	LED3 LED1	LED2 LED0	LED3 LED1	LED2 LED0	LED3 LED1	LED2 LED0
5/2.5 Gbps	Blink Mix	Blink Mix	Solid Mix	Solid Mix	Solid	Off	Solid	Off	Solid	Off	Solid	Off
1 Gbps	Blink Mix	Blink Mix	Solid Mix	Solid Mix	Solid Mix	Solid Mix	Solid Mix	Solid Mix	Off	Solid	Off	Solid
100 Mbps Link	Blink Mix	Blink Mix	Solid Mix	Solid Mix	Off	Solid	Off	Solid	Solid Mix	Solid Mix	Solid Mix	Solid Mix
10 Mbps Link	Blink Mix	Blink Mix	Solid Mix	Solid Mix	Off	Off	Off	Off	Off	Off	Off	Off
5/2.5 Gbps Link Operating in EEE Mode	Blink Mix	Blink Mix	Solid Mix	Solid Mix	Blink	Off	Solid	Off	Blink	Off	Solid	Off
1 Gbps Link Operating in EEE Mode	Blink Mix	Blink Mix	Solid Mix	Solid Mix	Blink Mix	Blink Mix	Solid Mix	Solid Mix	Off	Blink	Off	Blink
Link Down	Blink Mix	Blink Mix	Solid Mix	Solid Mix	Off	Off	Off	Off	Off	Off	Off	Off

3.11.4 Modes of Operation

The LED signals relay various statuses of the PHY so that they can be displayed by the LEDs.

The basic statuses are shown in Table 42. The compound statuses are formed with the basic status plus the speed information as shown in Table 43. The status information is generated by the copper (T Unit) interfaces.

Table 42: Basic LED Status

Status	Copper
Transmit	Copper Transmit
Receive	Copper Receive
Link	Copper Link
Full Duplex	Copper Duplex
Master	Master/Slave
Energy Efficient	EEE Active/Inactive

Table 43: Compound LED Status

Compound Status	Copper
Transmit or Receive	Copper Transmit or Copper Receive
Collision (Transmit and Receive)	Copper Transmit and Copper Receive and Copper Half Duplex
10 Mbps Link	Copper Speed = 10 Mbps and Copper Link
100 Mbps Link	Copper Speed = 100 Mbps and Copper Link
1 Gbps Link	Copper Speed = 1 Gbps and Copper Link
5/2.5 Gbps Link	Copper Speed = 5/2.5 Gbps and Copper Link
Link	Copper Link
Half Duplex	Not Copper Full Duplex
Slave	Not Master
10 Mbps Link or 100 Mbps Link	Copper 10 Mbps Link or Copper 100 Mbps Link
10 Mbps Link or 100 Mbps Link or 1 Gbps Link	Copper 10 Mbps Link or Copper 100 Mbps Link or Copper 1 Gbps Link
100 Mbps Link or 5/2.5 Gbps Link	Copper 100 Mbps or Copper 5/2.5 Gbps Link
1 Gbps or 5/2.5 Gbps Link	Copper 1 Gbps or Copper 5/2.5 Gbps Link

The status that the LED displays is defined by registers 31.F020 to 31.F023 as shown in Table 42 and Table 43. For each LED if the condition selected by bits 12:8 is true, then the LED will blink. If the condition selected by bits 7:3 is true, then the LED will be solid on. If both selected conditions are true, then the blink will take precedence.

3.11.5 Speed Blink

When 31.F020.7:3 is set to 11111, the LED[0] pin displays the following behavior.

LED[0] outputs the sequence shown in Table 44 depending on the status of the link. The sequence consists of 10 segments. If a 10 Gbps link is established, then LED[0] outputs 4 pulses, 1000 Mbps outputs 3 pulses, 100 Mbps outputs 2 pulses, 10 Mbps outputs 1 pulse, and no link outputs 0 pulses. The sequence repeats over and over again indefinitely.

The odd-numbered segment pulse duration is specified in 31.F027.1:0. The even-numbered pulse duration is specified in 31.F027.3:2.

Table 44: Speed Blinking Sequence

Segment	10 Mbps	100 Mbps	1 Gbps	10 Gbps	No Link	Duration
1	On	On	On	On	Off	31.F027.3:2
2	Off	Off	Off	Off	Off	31.F027.1:0
3	Off	On	On	On	Off	31.F027.3:2
4	Off	Off	Off	Off	Off	31.F027.1:0
5	Off	Off	On	On	Off	31.F027.3:2
6	Off	Off	Off	Off	Off	31.F027.1:0
7	Off	Off	Off	On	Off	31.F027.3:2
8	Off	Off	Off	Off	Off	31.F027.1:0
9	Off	Off	Off	Off	Off	31.F027.3:2
10	Off	Off	Off	Off	Off	31.F027.1:0

3.11.6 Combo LED Modes

Combo LED mode is activated when register 31.F024.15 is set to 1.

3.11.6.1 Combo LED Mode Select

Table 45: Combo Mode Timer Control

Mode	Rate	Setting
1	When link is up, the flashing rate is based on the number of frames received within 2 ms.	Refer to Table 46 for the flashing rate setup.
1	Faulty Link	TIMER_A = 31.F024.7:0
2	CRC, alignment, Runt, and Jabber Errors	TIMER_B = 31.F029.15:8
4	Spanning Tree Protocol (STP) is blocked, but it is receiving/sending data.	TIMER_D = 31.F039.7:0
5	1G	TIMER_1G = 31.F028.7:0
	2.5G	TIMER_2.5G = 31.F028.15:8

3.11.6.2 LED Activity Control

When the Combo LED Mode Selection bits (31.F024.14:12) are set to 000 and the link is up, the flash/blink activity of LED1 indicates the number of frames received within the last 2.1 seconds. Activity flashing of the LED is based on the transmitted and received frames on a link. Register 31.F026.11:10 is used to monitor transmit (31.F026.11:10 = 00), receive (31.F026.11:10 = 01), or both transmit and receive (31.F026.11:10 = 11) at the same time.

LED1 can flash in two different ways:

- When Combo LED flash bit is set to 0, the more packets received within the previous 2100 ms, the longer LED1 stays on.
- When Combo LED flash bit is set to 1, the more packets received within the previous 2100 ms, the faster LED1 blinks.

The Combo LED flash rate details are listed in Table 46.

Table 46: Combo LED Flash Mode

Combo LED Flash (31.F024.11)	Flash Rate
0	<10: on for 31.F030[7:0], the remaining of 2.1s off; <10^2: on for 31.F030[15:8], the remaining of 2.1s off; <$5*10^2$: on for 31.F031[7:0], the remaining of 2.1s off; <10^3: on for 31.F031[15:8], the remaining of 2.1s off; <$5*10^3$: on for 31.F032[7:0], the remaining of 2.1s off; <10^4: on for 31.F032[15:8], the remaining of 2.1s off; <$5*10^4$: on for 31.F033[7:0], the remaining of 2.1s off; <10^5: on for 31.F033[15:8], the remaining of 2.1s off; <$5*10^5$: on for 31.F034[7:0], the remaining of 2.1s off; <10^6: on for 31.F034[15:8], the remaining of 2.1s off; <$5*10^6$: on for 31.F035[7:0], the remaining of 2.1s off; <10^7: on for 31.F035[15:8], the remaining of 2.1s off **NOTE:** For registers 31.F030, 31.F031, 31.F032, 31.F033, 31.F034, and 31.F035, the unit of bit[7:0] and [15:8] is 21 ms. Any value greater than 8'd100 will be ignored.
1	<10: LED on/off every 1/2 of 2.1s; <10^2: LED on/off every 1/4 of 2.1s; <$5*10^2$: LED on/off every 1/8 of 2.1s; <10^3: LED on/off every 1/16 of 2.1s; <$5*10^3$: LED on/off 1/32 of 2.1s; <10^4: LED on/off 1/64 of 2.1s; <$5*10^4$: LED on/off 1/128 of 2.1s; <10^5: LED on/off 1/256 of 2.1s; <$5*10^5$: LED on/off 1/512 of 2.1s; <10^6: LED on/off 1/1024 of 2.1s; <$5*10^6$: LED on/off 1/2048 of 2.1s; <10^7: LED on/off 1/4096 of 2.1s

For example:

When the number of frames received within 2.1 seconds is 4000, the LED will behave as follows in the next 2.1 seconds:

- If 31.F024.11 = 0, then LED1 will be on for 31.F031[7:0] * 21 ms and off for (100 - 31.F031[7:0]) * 21 ms.
- If 31.F024.11 = 1, then LED1 will be on for 1/32 * 2100 ms and off for 1/32 * 2100 ms repeatedly for 2.1 seconds.

3.11.7 LED Output via MFIO Pins (88E2110), GPIO/LED or Serial LED (88E2180)

For the 88E2110 device, MFIOS[2], MFIOS[1], and MFIOS[0] is assigned as output LED[2], LED[1], and LED[0], respectively.

For the 88E2180 device, each port of the 88E2180 device has only two GPIO pins such as GPIO[1:0]. If an application requires GPIO for other purposes or more LED outputs, then more LED outputs can be supported with Serial LED features. (Details are provided in Section 3.12). The Serial LED feature can support three LED bits per port. An additional LED bit can be brought out via GPIO[0] or GPIO[1] per port.

Table 47: Example of GPIO Assignment for the 88E2180 Device

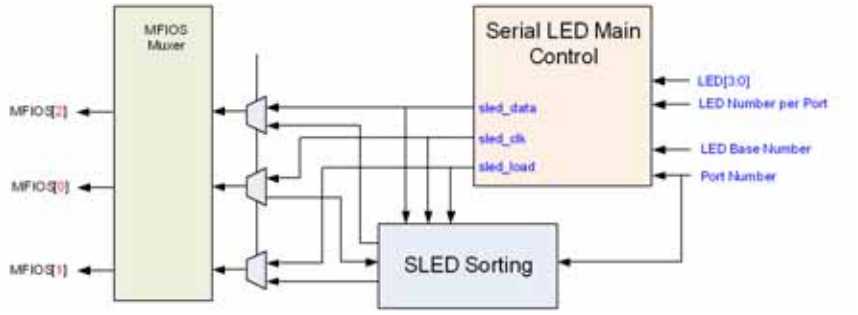
	P0_GPIO[0]	P0_GPIO[1]	P1_GPIO[0]	P1_GPIO[1]	P2_GPIO[0]	P2_GPIO[1]	P3_GPIO[0]	P3_GPIO[1]
Case1	P0_LED[0]	P0_LED[1]	P1_LED[0]	P1_LED[1]	P1_LED[0]	P1_LED[1]	P1_LED[0]	P1_LED[1]
Case2	P0_LED[0]	GPIO	P1_LED[0]	GPIO	P1_LED[0]	GPIO	P1_LED[0]	GPIO

3.12 88E2180 Serial LED

3.12.1 88E2180 Serial LED Interface

MFIOS[0] (Clock), MFIOS[1] (Data Load) and MFIOS[2] (Data) pins are used for the serial interface. In 88E2180 devices, each port has four independent LED control modules internally. One or two of LED[3:0] per port can be output through GPIO[1:0] per port. If an application requires more LED display, then it can be output through serial interface which is called MFIOS[2:0] pins. See Figure 25.

Figure 25: 88E2180 Serial LED Control Block Diagram



The SLED Sorting module aligns the LED output sequence for all 8 ports in sequence as shown in Section 3.12.3.

3.12.2 88E2180 Serial Display Order

LED data from the lower port number is shifted out first and the one from the highest port number comes out last followed by load pulse.

Figure 26: Interface Protocol Example in 88E2180 — One LED per Port

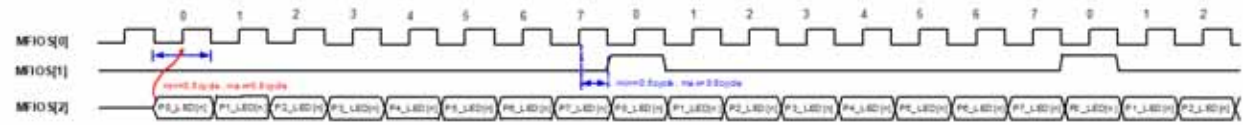
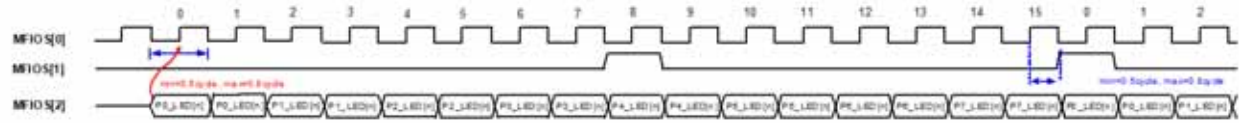


Figure 27: Interface Protocol Example in 88E2180 — Two LEDs per Port



3.12.3 88E2180 Serial Clock Speed Options

Some low-value shifter registers require a lengthy setup time and support a very slow cycle time. To support various shift registers, the clock can be selected with three different options. The speed control register is 31.F03A.5:4. See Table 48.

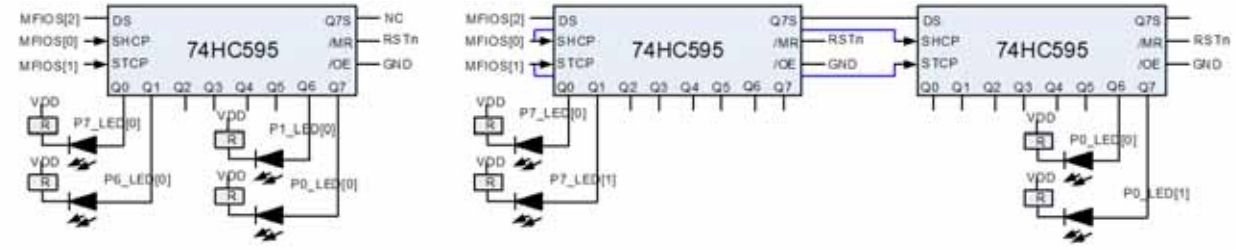
Table 48: Clock Speed Options

mfclk_speed_sel[1:0]	Speed (ns)	# of 156.25 MHz Clock
00	160	25 clocks (13 lows)
01	320	50 clocks
02	384	60 clocks

3.12.4 88E2180 Serial LED Feature Application Examples

When the LED comes out through MFIOS[2:0], the application must add an extra shifter register device outside in the following example. See Figure 28.

Figure 28: 88E2180 Serial LED Application Example: One LED per Port and Two LEDs per Port



Serial LED via MFIOS[2:0] can shift out any LED output such as LED[0], LED[1], LED[2], LED[3] (Single LED per port), or LED[1:0], LED[2:1], LED[3:2] (Dual LEDs per port), or LED[2:0], LED[3:1] (Triple LEDs per port).

Table 49: 88E2180 Serial LED Control Register (Global Register)

Register	Function	Setting	Mode	HW Rst	SW Rst
31.F03A.15:6	Reserved	Set to 0s.	R/W	0x00	Retain
31.F03A.5:4	Serial LED Period Selection	0 = 160 ns 1 = 320 ns 2 = 384 ns 3 = Reserved	R/W	0x01	Retain
31.F03A.3:2	BASE LED Number	0 = LED[0] 1 = LED[1] 2 = LED[2] 3 = LED[3]	R/W	2'b01	Retain

3.13 Interrupt

The T Unit supports various interrupts.

For 2.5G/10G interrupt events:

Registers 3.8011 and 3.8013 are the interrupt status registers and apply to those modes as a group.

For 10M/100M/1G interrupt events:

- Registers 3.8011 and 3.8013 are the interrupt status registers and only apply to those modes individually.
- Registers 3.8010 and 3.8012 are the interrupt enable registers.

The interrupt pin will be activated if any of the enabled events in the interrupt status registers occurs. If a certain interrupt event is not enabled by interrupt enable registers, then it will still be indicated by the corresponding interrupt status registers bits if the interrupt event occurs. However, the unselected events will not cause the interrupt pin to be activated. The interrupts are cleared by reading the interrupt status registers.

The T Unit interrupts are aggregated in the Global Interrupt register 31.F040.

- Registers 3.80111 and 3.8013 apply to 10M/100M/1G individually and 2.5G as a group.
- Registers 3.8010 and 3.8012 apply to 10M/100M/1G only.

Table 50: 88E2180 Global Interrupt Status (Port 0, 1, 6, and 7)

Register	Function	Setting	Mode	HW Rst	SW Rst
31.F042.15:4	Reserved	0	RO	0x000	Retain
31.F042.3	Port 7 Interrupt	0 = No Interrupt 1 = Active Interrupt. This status can be read from any of the ports among 0, 1, 6, and 7 ports.	RO	0x0	Retain
31.F042.2	Port 6 Interrupt	0 = No Interrupt 1 = Active Interrupt. This status can be read from any of the ports among 0, 1, 6, and 7 ports.	RO	0x0	Retain
31.F042.1	Port 1 Interrupt	0 = No Interrupt 1 = Active Interrupt. This status can be read from any of the ports among 0, 1, 6, and 7 ports.	RO	0x0	Retain
31.F042.0	Port 0 Interrupt	0 = No Interrupt 1 = Active Interrupt This status can be read from any of the ports among 0, 1, 6, and 7 ports.	RO	0x0	Retain

Table 51: 88E2180 Global Interrupt Status (Port 2, 3, 4, and 5)

Register	Function	Setting	Mode	HW Rst	SW Rst
31.F042.15:4	Reserved	0	RO	0x000	Retain
31.F042.3	Port 5 Interrupt	0 = No Interrupt 1 = Active Interrupt. This status can be read from any of the ports among 2, 3, 4, and 5 ports.	RO	0x0	Retain
31.F042.2	Port 4 Interrupt	0 = No Interrupt 1 = Active Interrupt This status can be read from any of the ports among 2, 3, 4, and 5 ports.	RO	0x0	Retain
31.F042.1	Port 3 Interrupt	0 = No Interrupt 1 = Active Interrupt. This status can be read from any of the ports among 2, 3, 4, and 5 ports.	RO	0x0	Retain
31.F042.0	Port 2 Interrupt	0 = No Interrupt 1 = Active Interrupt. This status can be read from any of the ports among 2, 3, 4, and 5 ports.	RO	0x0	Retain

3.14 IEEE 1149.1 and 1149.6 Controller

The IEEE 1149.1 standard defines a test access port and boundary-scan architecture for digital integrated circuits and for the digital portions of mixed analog/digital integrated circuits. The IEEE 1149.6 standard defines a test access port and boundary-scan architecture for AC-coupled signals.

This standard provides a solution for testing assembled printed circuit boards and other products based on highly complex digital integrated circuits and high-density surface-mounting assembly techniques.

The device implements the instructions shown in Table 52. Upon reset, ID_CODE instruction is selected. PROG_HYST is a proprietary command used to adjust the test receiver hysteresis threshold. The instruction opcodes are shown in Table 52.

Table 53 lists the 88E2180 device boundary scan orders and Table 54 lists the 88E2110 device boundary scan orders, respectively, where:

TDI ➔ P0_SON/P[0] (AC/DC) ➔ … ➔ SPI_SSn(Output) ➔ TDO

Table 52: TAP Controller Opcodes

Instruction	OpCode
EXTEST	00000000
SAMPLE/PRELOAD	00000001
CLAMP	00000010
HIGH-Z	00000011
ID_CODE	00000100
EXTEST_PULSE	00000101
EXTEST_TRAIN	00000110
PROG_HYST	00001000
BYPASS	11111111

The device reserves five pins called the Test Access Port (TAP) to provide test access:

- Test Mode Select Input (TMS)
- Test Clock Input (TCK)
- Test Data Input (TDI)
- Test Data Output (TDO)
- Test Reset Input (TRSTn)

To ensure race-free operation, all input and output data is synchronous with the test clock (TCK). TAP input signals (TMS and TDI) are clocked into the test logic on the rising edge of TCK, while output signal (TDO) is clocked on the falling edge. For additional details, refer to the IEEE 1149.1 Boundary Scan Architecture document.

3.14.1 BYPASS Instruction

The BYPASS instruction uses the bypass register. This register contains a single shift-register stage and is used to provide a minimum length serial path between the TDI and TDO pins of the device when test operation is not required. This arrangement allows rapid movement of test data to and from other testable devices in the system.

3.14.2 SAMPLE/PRELOAD Instruction

The SAMPLE/PRELOAD instruction enables scanning of the boundary-scan register without causing interference to the normal operation of the device. Two functions are performed when this instruction is selected: SAMPLE and PRELOAD.

SAMPLE allows a snapshot to be taken of the data flowing from the system pins to the on-chip test logic or vice versa, without interfering with normal operation. The snapshot is taken on the rising edge of TCK in the Capture-DR controller state and the data can be viewed by shifting through the component's TDO output.

While sampling and shifting data out through TDO for observation, PRELOAD enables an initial data pattern to be shifted in through TDI and to be placed at the latched parallel output of the boundary-scan register cells that are connected to system output pins. This step ensures that known data is driven through the system output pins upon entering the extest instruction. Without PRELOAD, indeterminate data would be driven until the first scan sequence is complete. The shifting of data for the SAMPLE and PRELOAD phases can occur simultaneously. While data capture is being shifted out, the PRELOAD data can be shifted in.

Table 53: Boundary Scan Chain for the 88E2180 Device

Order	Pin Name	Input/Output
1	RESERVED7	Input
2	RESERVED7	Output
3	RESERVED7	Output Enable
4	P7_GPIO[1]	Input
5	P7_GPIO[1]	Output
6	P7_GPIO[1]	Output Enable
7	P7_GPIO[0]	Input

Table 53: Boundary Scan Chain for the 88E2180 Device (Continued)

Order	Pin Name	Input/Output
8	P7_GPIO[0]	Output
9	P7_GPIO[0]	Output Enable
10	P7_SIN	Input
11	P7_SIP	Input
12	P7_SON/ P7_SOP	Output
13	P7_SON/ P7_SOP	AC/DC Select
14	RESERVED6	Input
15	RESERVED6	Output
16	RESERVED6	Output Enable
17	P6_GPIO[1]	Input
18	P6_GPIO[1]	Output
19	P6_GPIO[1]	Output Enable
20	P6_GPIO[0]	Input
21	P6_GPIO[0]	Output
22	P6_GPIO[0]	Output Enable
23	P6_SIN	Input
24	P6_SIP	Input
25	P6_SON/ P6_SOP	Output
26	P6_SON/ P6_SOP	AC/DC Select
27	RESERVED1	Input
28	RESERVED1	Output
29	RESERVED1	Output Enable
30	P1_GPIO[1]	Input
31	P1_GPIO[1]	Output
32	P1_GPIO[1]	Output Enable
33	P1_GPIO[0]	Input
34	P1_GPIO[0]	Output
35	P1_GPIO[0]	Output Enable

Table 53: Boundary Scan Chain for the 88E2180 Device (Continued)

Order	Pin Name	Input/Output
36	P1_SIN	Input
37	P1_SIP	Input
38	P1_SON/ P1_SOP	Output
39	P1_SON/ P1_SOP	AC/DC Select
40	RESERVED0	Input
41	RESERVED0	Output
42	RESERVED0	Output Enable
43	P0_GPIO[1]	Input
44	P0_GPIO[1]	Output
45	P0_GPIO[1]	Output Enable
46	P0_GPIO[0]	Input
47	P0_GPIO[0]	Output
48	P0_GPIO[0]	Output Enable
49	P0_SIN	Input
50	P0_SIP	Input
51	P0_SON/ P0_SOP	Output
52	P0_SON/ P0_SOP	AC/DC Select
53	SPI_SSn	Output
54	SPI_SSn	Output Enable
55	SPI_CLK	Output
56	SPI_CLK	Output Enable
57	SPI_MOSI	Output
58	SPI_MOSI	Output Enable
59	SPI_MISO	Input
60	RESETn	Input
61	RCLK	Output

Table 53: Boundary Scan Chain for the 88E2180 Device (Continued)

Order	Pin Name	Input/Output
62	RCLK	Output Enable
63	MDIO	Input
64	MDIO	Output
65	MDIO	Output Enable
66	MDC[	Input
67	INTn	Output
68	INTn	Output Enable
69	CLK_SEL[1]	Input
70	CLK_SEL[0]	Input
71	RESERVED5	Input
72	RESERVED5	Output
73	RESERVED5	Output Enable
74	P5_GPIO[1]	Input
75	P5_GPIO[1]	Output
76	P5_GPIO[1]	Output Enable
77	P5_GPIO[0]	Input
78	P5_GPIO[0]	Output
79	P5_GPIO[0]	Output Enable
80	P5_SIN	Input
81	P5_SIP	Input
82	P5_SON/ P5_SOP	Output
83	P5_SON/ P5_SOP	AC/DC Select
84	RESERVED4	Input

Table 53: Boundary Scan Chain for the 88E2180 Device (Continued)

Order	Pin Name	Input/Output
85	RESERVED4	Output
86	RESERVED4	Output Enable
87	P4_GPIO[1]	Input
88	P4_GPIO[1]	Output
89	P4_GPIO[1]	Output Enable
90	P4_GPIO[0]	Input
91	P4_GPIO[0]	Output
92	P4_GPIO[0]	Output Enable
93	P4_SIN	Input
94	P4_SIP	Input
95	P4_SON/ P4_SOP	Output
96	P4_SON/ P4_SOP	AC/DC Select
97	RESERVED3	Input
98	RESERVED3	Output
99	RESERVED3	Output Enable
100	P3_GPIO[1]	Input
101	P3_GPIO[1]	Output
102	P3_GPIO[1]	Output Enable
103	P3_GPIO[0]	Input
104	P3_GPIO[0]	Output
105	P3_GPIO[0]	Output Enable
106	P3_SIN	Input
107	P3_SIP	Input

Table 53: Boundary Scan Chain for the 88E2180 Device (Continued)

Order	Pin Name	Input/Output
108	P3_SON/ P3_SOP	Output
109	P3_SON/ P3_SOP	AC/DC Select
110	CONFIG[2]	Input
111	CONFIG[1]	Input
112	CONFIG[0]	Input
113	MFIOS[2]	Output
114	MFIOS[2]	Output Enable
115	MFIOS[1]	Output
116	MFIOS[1]	Output Enable
117	MFIOS[0]	Output
118	MFIOS[0]	Output Enable
119	RESERVED2	Input
120	RESERVED2	Output
121	RESERVED2	Output Enable
122	P2_GPIO[1]	Input
123	P2_GPIO[1]	Output
124	P2_GPIO[1]	Output Enable
125	P2_GPIO[0]	Input
126	P2_GPIO[0]	Output
127	P2_GPIO[0]	Output Enable
128	P2_SIN	Input
129	P2_SIP	Input
130	P2_SON/ P2_SOP	Output

Table 53: Boundary Scan Chain for the 88E2180 Device (Continued)

Order	Pin Name	Input/Output
131	P2_SON/ P2_SOP	AC/DC Select

Table 54: Boundary Scan Chain for the 88E2110 Device

Order	Pin	I/O Type
1	GPIO[5]	Input
2	GPIO[5]	Output
3	GPIO[5]	Output Enable
4	GPIO[4]	Input
5	GPIO[4]	Output
6	GPIO[4]	Output Enable
7	GPIO[3]	Input
8	GPIO[3]	Output
9	GPIO[3]	Output Enable
10	GPIO[2]	Input
11	GPIO[2]	Output
12	GPIO[2]	Output Enable
13	GPIO[1]	Input
14	GPIO[1]	Output
15	GPIO[1]	Output Enable
16	GPIO[0]	Input
17	GPIO[0]	Output
18	GPIO[0]	Output Enable
19	SIN	Input
20	SIP	Input
21	SON/SOP	Output
22	SON/ SOP	AC/DC Select
23	SPI_SSn	Output
24	SPI_SSn	Output Enable

Table 54: Boundary Scan Chain for the 88E2110 Device (Continued)

Order	Pin	I/O Type
25	SPI_CLK	Output
26	SPI_CLK	Output Enable
27	SPI_MOSI	Output
28	SPI_MOSI	Output Enable
29	SPI_MISO	Input
30	RESETn	Input
31	RCLK	Output
32	RCLK	Output Enable
33	MDIO	Input
34	MDIO	Output
35	MDIO	Output Enable
36	MDC	Input
37	INTn	Output
38	INTn	Output Enable
39	CLK_SEL[1]	Input
40	CLK_SEL[0]	Input
41	CONFIG[2]	Input
42	CONFIG[1]	Input
43	CONFIG[0]	Input
44	MFIOS[2]	Output
45	MFIOS[2]	Output Enable
46	MFIOS[1]	Output
47	MFIOS[1]	Output Enable
48	MFIOS[0]	Output
49	MFIOS[0]	Output Enable

3.14.3 EXTEST Instruction

The EXTEST instruction enables circuitry external to the device (typically the board interconnections) to be tested. Prior to executing the EXTEST instruction, the first test stimulus to be applied is shifted into the boundary-scan registers using the SAMPLE/PRELOAD instruction. So when the change to the extest instruction occurs, known data is driven immediately from the device to its external connections. The SOP/N pins will be driven to static levels. The positive and negative legs of the SOP/N pins are controlled via a single boundary scan cell. The positive leg outputs the level specified by the boundary scan cell while the negative leg outputs the opposite level.

3.14.4 CLAMP Instruction

The CLAMP instruction enables the state of the signals driven from component pins to be determined from the boundary-scan register while the bypass register is selected as the serial path between TDI and TDO. The signals driven from the component pins do not change while the clamp instruction is selected.

3.14.5 HIGH-Z Instruction

The HIGH-Z instruction places all of the digital component system logic outputs in an inactive high-impedance drive state. In this state, an in-circuit test system may drive signals onto the connections normally driven by a component output without incurring the risk of damage to the component.

3.14.6 ID CODE Instruction

The ID CODE contains the manufacturer identity, part, and version.

Table 55: ID CODE Instruction

Version	Part Number	Manufacturer Identity	
Bit 31 to 28	Bit 27 to 12	Bit 11 to 1	Bit 0
(88E2110) 0000	0000000001001000	00111101110	1
(88E2180) 0000	0000000001000111	00111101110	1

3.14.7 EXTEST_PULSE Instruction

The AC-JTAG or DC-JTAG test modes can be selected for each port individually by scanning in the selected bit value into AC/DC select scan registers shown in the scan chain (Table 54 for 88E2110 devices and Table 53 for 88E2180 devices). When the AC/DC select is set to DC the EXTEST_PULSE instruction has the same behavior as the EXTEST instruction.

When the AC/DC select is set to AC, the EXTEST_PULSE instruction has the same behavior as the EXTEST instruction except for the behavior of the SOP/N pins.

As in the EXTEST instruction, the test stimulus must first be shifted into the boundary-scan registers. Upon the execution of the EXTEST_PULSE instruction, the SOP[1:0] pins output the level specified by the test stimulus and SON pins output the opposite level.

However, if the TAP controller enters into the Run-Test/Idle state, then the SON pins output the level specified by the test stimulus and SOP[1:0] pins output the opposite level.

When the TAP controller exits the Run-Test/Idle state, the SOP pins again output the level specified by the test stimulus and SON pins output the opposite level.

3.14.7.1 EXTEST_TRAIN Instruction

When the AC/DC select is set to DC, the EXTEST_TRAIN instruction has the same behavior as the EXTEST instruction.

When the AC/DC select is set to AC, the EXTEST_TRAIN instruction has the same behavior as the EXTEST instruction except for the behavior of the SOP/N pins.

As in the EXTEST instruction, the test stimulus must first be shifted into the boundary-scan registers. Upon the execution of the EXTEST_PULSE instruction, the SOP pins output the level specified by the test stimulus and SON pins output the opposite level.

However, if the TAP controller enters into the Run-Test/Idle state, then the SOP/N will toggle between inverted and non-inverted levels on the falling edge of TCK. This toggling will continue for as long as the TAP controller remains in the Run-Test/Idle state.

When the TAP controller exits the Run-Test/Idle state, the SOP pins again output the level specified by the test stimulus and SON pins output the opposite level.

3.14.8 PROG_HYST Instruction

The test receivers connected to the XIP/N[3:0] and MIP/N[3:0] pins requires the hysteresis level to be set according to the application that the SERDES is used in. The amount of hysteresis required is a function of the expected voltage swing on the input. The proprietary command PROG_HYST will program three registers in the tap controller which will set the value of the hysteresis.

When the PROG_HYST opcode is in the instruction register, the following actions occur in the following TAP controller states.

- Capture-DR state: Load the value in HYST[2:0] into SR_HYST[2:0].
- Shift-DR state: Shift TDI into SR_HYST[0], SR_HYST[1:0] into SR_HYST[2:1], and SR_HYST[2] to TDO. Three bits should be loaded to set the new test receiver hysteresis value.
- Update-DR state: Load the value in SR_HYST[2:0] into HYST[2:0].
- HYST[2:0] is the register that sets the hysteresis in the test receiver.
- SR_HYST[2:0] is the 3-bit shift register used to shift the values in and out.

The hysteresis mapping is shown in Table 56. 70 mV is the default setting. When the TAP controller is in the Test-Logic-Reset state or when TRSTn is forced low, the HYST[2:0] is reset to the default state.

Table 56: Test Receiver Hysteresis Setting

HYST[2:0]	Hysteresis
000	12 mV
001	25 mV
010	50 mV
011	70 mV
100	90 mV
101	105 mV
110	135 mV
111	150 mV

3.14.9 AC-JTAG Fault Detection

The fault detection across AC-coupled connections can be detected with a combination of (DC) EXTEST and any one of the AC-JTAG commands. The AC-coupled connection is shown in Figure 29.

The fault signature is shown in Table 57.

- Column 1 lists the fault type.
- Columns 2 to 5 list the behavior when both the transmitter and receiver are running the EXTEST_TRAIN and EXTEST_PULSE commands.
- Column 2 shows the expected value captured by the boundary scan cell that is connected to the test receiver, which is connected to the positive input when a negative differential pulse is transmitted.
- Column 3 is the same as column 2 except for the negative input.
- Columns 4 and 5 are similar to columns 2 and 3 except a positive differential pulse is transmitted.
- Columns 6 to 9 are similar to columns 2 to 5 except both the transmitter and receiver are running the (DC) EXTEST command.

While it is not possible to identify precisely which fault is occurring based on the fault signature, the signature associated with the no fault condition is unique when the (DC) EXTEST command is run with at least one of the EXTEST_TRAIN or EXTEST_PULSE commands. Running only AC-JTAG commands is not sufficient since the no fault condition signature is not distinguishable from the TX-to-RX short (see shaded cells in Table 57).

Figure 29: AC-Coupled Connection

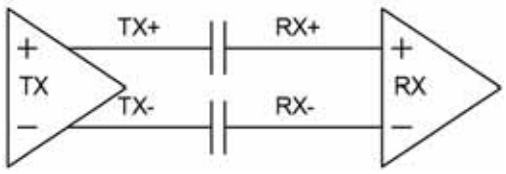


Table 57: AC-Coupled Connection Fault Signature

DC Coupled Fault	AC Testing Sample 0		AC Testing Sample 1		(DC) EXTEST Sample 0		(DC) EXTEST Sample 1	
	Positive Leg	Negative Leg	Positive Leg	Negative Leg	Positive Leg	Negative Leg	Positive Leg	Negative Leg
TX+ Open	0	X	0	X	1	X	1	X
TX- Open	X	0	X	0	X	1	X	1
RX+ Open	0	X	0	X	1	X	1	X
RX- Open	X	0	X	0	X	1	X	1
TX+ short to power	0/Note 2	X	0/Note 2	X	1	X	1	X
TX- short to power	X	0/Note 2	X	0/Note 2	X	1	X	1
RX+ short to power	0/Note 2	X	0/Note 2	X	1	X	1	X
RX- short to power	X	0/Note 2	X	0/Note 2	X	1	X	1
TX+ short to ground	0	X	0	X	1	X	1	X
TX- short to ground	X	0	X	0	X	1	X	1
RX+ short to ground	0	X	0	X	0	X	0	X
RX- short to ground	X	0	X	0	X	0	X	0
TX+ short to TX-	Note 1	Note 1	Note 1	Note 1	1	1	1	1
RX+ short to RX-	Note 1	Note 1	Note 1	Note 1	1	1	1	1
TX+ short to RX-	X	0	X	1	X	0	X	1
TX- short to RX+	1	X	0	X	1	X	0	X
TX+ short to RX+	0	X	1	X	0	X	1	X
TX- short to RX-	X	1	X	0	X	1	X	0
No Fault	0	1	1	0	1	1	1	1
Note 1	A short on the positive and negative leg can have several behaviors on the test receiver. If both drivers cancel each other out, then output on both legs is 0. If one driver dominates the other, then both legs are either both 1 or both 0. In any case, the result is that both legs will have the same value.							
Note 2	A solid short to power is assumed. If the short has high inductance, then a pulse may still be sent at the receiver and will be mistaken as a good connection.							

The fault detection across DC-coupled connections can be detected with any one of the AC-JTAG or (DC) EXTEST commands. The DC-coupled connection is shown in Figure 30. The fault signature is shown in Table 58.

Figure 30: DC-Coupled Connection

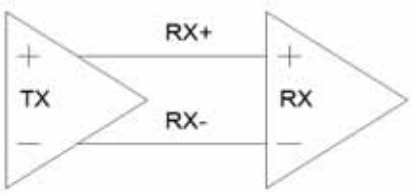


Table 58: DC-Coupled Connection Fault Signature

DC Coupled Fault	AC Testing Sample 0		AC Testing Sample 1		(DC) EXTEST Sample 0		(DC) EXTEST Sample 1	
	Positive Leg	Negative Leg	Positive Leg	Negative Leg	Positive Leg	Negative Leg	Positive Leg	Negative Leg
RX+ Open	0	X	0	X	1	X	1	X
RX- Open	X	0	X	0	X	1	X	1
RX+ short to power	0/Note 2	X	0/Note 2	X	1	X	1	X
RX- short to power	X	0/Note 2	X	0/Note 2	X	1	X	1
RX+ short to ground	0	X	0	X	0	X	0	X
RX- short to ground	X	0	X	0	X	0	X	0
RX+ short to RX-	Note 1	Note 1	Note 1	Note 1	Note 1	Note 1	Note 1	Note 1
No Fault	0	1	1	0	0	1	1	0
Note 1	Short on positive and negative leg can have several behaviors on the test receiver. If both drivers cancel each other out, then output on both legs is 0. If one driver dominates the other, then both legs are either both 1 or both 0. In any case, the result is that both legs will have the same value.							
Note 2	A solid short to power is assumed. If the short has high inductance, then a pulse may still be sent at the receiver and will be mistaken as a good connection.							

3.15 Reference Clock

The 88E2110 device uses a 156.25 MHz differential clock into CLKP/N as the reference clock.

The 88E2180 device can use one of three clocking options as shown in Table 59. CLK_SEL must be stable and the selected clock toggling prior to de-assertion of RESETn. CLK_SEL must not change value for the duration of device operation.

When using XTAL option (CLK_SEL[1:0] = 00), TSTCP/N output pins should be connected to CLK_P/N input pins on the board through AC-coupling capacitors.

Table 59: Reference Clock Options

CLK_SEL[1:0]	XTAL1/XTAL2	CLKP/CLKN
00	50 MHz	Floating
01	GND	50 MHz
10	GND	156.25 MHz
11	Reserved	Reserved

Note

For 88E2180 devices, normal operation must only use the 156.25 MHz differential clock.

3.16 Temperature Sensor

The 88E2180/88E2110 device contains an internal temperature sensor and specifically, this sensor can be accessed via only Port 1 and 3 in the 88E2180/88E2110. The die temperature can be read from 3.8042.7:0 and the temperature sensor is enabled by default. The result returned is an average over 4.5 seconds. The result is invalid for the first six seconds following a hardware reset. The 88E2180/88E2110 device must be powered up if PDSTATE hardware strapping is 1 for the temperature sensor to return correct values. 3.8043.7:0 returns values in 1-degree C increments and is offset by +75°C. That is, the die temperature can be calculated as follows:

Temperature in °C = 3.8042.7:0 -75.

For example, 100°C would have 3.8042 = 0xAF (binary 10101111).

3.17 Power Supplies

The 88E2180/88E2110 device requires three power supplies: 3.3V (analog), 1.8V (analog), and 0.8V (digital). For lower power consumption, AVDDL can operate at 1.5V. In this case, four power supplies are required: 3.3V, 1.8V, 1.5V, and 0.8V.

3.17.1 AVDDL

AVDDL is the copper transmitter and receiver 1.5V or 1.8V analog supply.

3.17.2 AVDDH

AVDDH is the copper transmitter and receiver 1.8V analog supply.

3.17.3 AVDDT

AVDDT is the copper transmitter 3.3V analog.

3.17.4 AVDDC

AVDDC is the common analog supply of 1.5V or 1.8V.

3.17.5 AVDDS

AVDDS is the SERDES analog supply of 1.5V or 1.8V.

3.17.6 AVDDR

AVDDR is the regulator supply and should be tied to 1.5V or 1.8V. It can be tied to AVDDS.

3.17.7 DVDD

DVDD is the core logic digital supply. 0.8V for C-temp and 0.88V for I-temp support.

3.17.8 VDDO

There are three separate VDDO segments: VDDOT VDDOL, and VDDOM. The VDDOM and VDDOT segments can be independently set to one for the following voltages: 1.5V, 1.8V, 2.5V, or 3.3V, except VDDOM that can also support 1.2V. Table 40 lists the signals under each of the VDDO segments.

If the VDDO* segment is set to 1.2V, 1.5V, or 1.8V, then its corresponding VSEL_* should tied to VDDO*.

If the VDDO* segment is set to 2.5V or 3.3V, then its corresponding VSEL_* should tied to VSS.

VDDOL can be set to 2.5V or 3.3V. The VDDOL segment does not support 1.5V or 1.8V.

The input pins are not high voltage tolerant. For example, if VDDO* is tied to 2.5V, then RESETn should not be driven to 3.3V.

Table 60: Signal Power Segment

Power Segment	VDDOT	VDDOL		VDDOM
Signals	TCK	GPIO[x:0]	CLK_SEL[1:0] (88E2180)	INTn
	TDI	RCLK	CONFIG[2:0]	MDC
	TDO	RESETn	MFIOS[2:0]	MDIO
	TMS	SPI_CLK	TEST (88E2180)	CLK_SEL[1:0] (88E2110) – (88E2180)
	TRST	SPI_MOS0	–	–
	TEST(88E2110) – (88E2180)	SPI_MOS1	–	–
	–	SPI_SSn	–	–

3.17.9 VDDR09

VDDR09 is the 0.9V internally generated regulated output and these pins should be tied an external capacitor to VSS.

4 Copper Unit (T Unit)

This section describes the copper unit (T Unit) interface functions.

4.1 Media Interface

The copper interface consists of the MDIP/N[3:0] pins that connect to the physical media for 5GBASE-T, 2.5GBASE-T, 1000BASE-T, 100BASE-TX, and 10BASE-Te modes of operation.

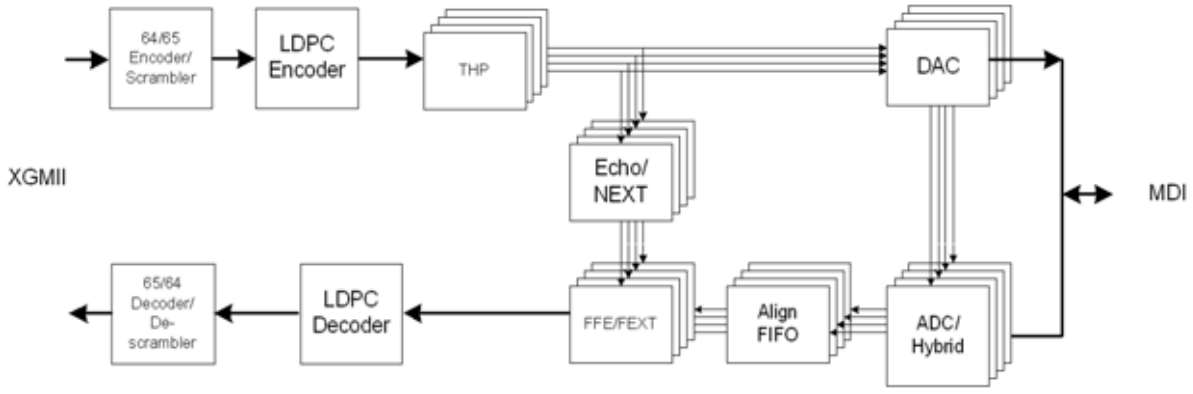
The device integrates MDI interface termination resistors. The IEEE 802.3 specification requires that both sides of a link have termination resistors to prevent reflections. Traditionally, these resistors and additional capacitors are placed on the board between the PHY and the magnetics. The resistors must be very accurate to meet the strict IEEE return loss requirements. Typically, ±1% accuracy resistors are used on the board. These additional components between the PHY and the magnetics complicate board layout. Integrating the resistors has many advantages including component cost savings, better ICT yield, board reliability improvements, board area savings, improved layout, and signal integrity improvements. See the *Benefits of Integrating Termination Resistors for Ethernet Applications* for details.

The transmitter can be shut down in all operational speeds by setting register 3.8109.0 to 1 in 10M/100M/1G operation and 1.0009.0 to 1 for 2.5G/5G operation.

Each channel's transmitter's polarity can be reversed by setting the corresponding bit in register 3.8001.3:0 to 1 in a 10M/100M/1G operation. Channel transmitter polarity reversal is not supported for 2.5G/5G operation. The device supports Auto-MDI/MDIX to automatically switch to the proper configuration when a cable is connected.

4.1.1 2.5GBASE-T and 5GBASE-T

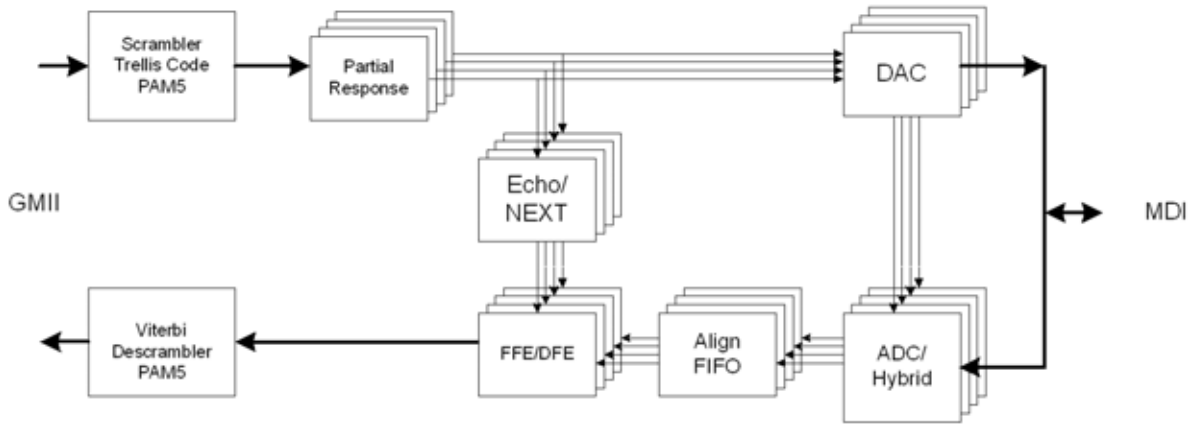
Figure 31: 2.5GBASE-T and 5GBASE-T Data Path



The device performs all the physical layer functions of 2.5GBASE-T and 5GBASE-T over CAT 5e, 6A, and 7 cable systems. The 88E2180/88E2110 device performs scrambling, LDPC coding, PAM16 mapping, and THP pre-coding on the transmit side with adaptive equalization, full echo cancellation, decoding and de-scrambling on the receive side. It is fully compliant to the IEEE 802.3 standard, including the PMA and PCS sublayers for full physical layer functionality.

4.1.2 1000BASE-T

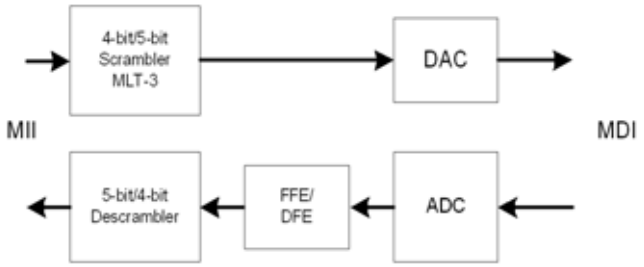
Figure 32: 1000BASE-T Data Path



The device performs all the physical layer functions of 1000BASE-T full or half duplex on twisted pair CAT 5, 6, and 7 cable. It is fully compliant to the IEEE 802.3 standard, including the PMD, PMA, and PCS sublayers. The device for 1000BASE-T performs scrambling, Trellis coding, PAM5 mapping functions on the transmit side with adaptive equalization, echo cancellation, viterbi decoding, and de-scrambling on the receive side.

4.1.3 100BASE-TX

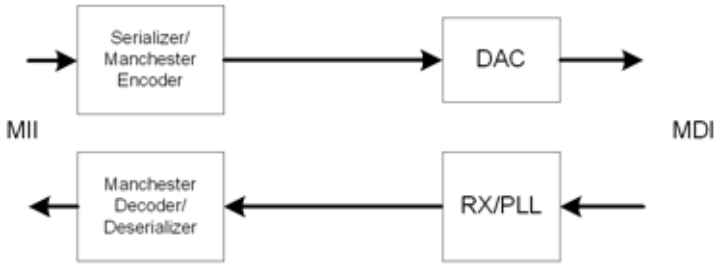
Figure 33: 100BASE-TX Data Path



The device performs all the physical layer functions of 100BASE-TX full or half duplex on twisted pair CAT 5, 6, and 7 cable. It is fully compliant to the IEEE 802.3 standard, including the PMD, PMA, and PCS sublayers. The device supports Auto-MDI/MDIX to automatically switch to the proper configuration when a cable is connected. As mentioned, the device also integrates the PHY termination resistors enabling BOM material and cost savings, ease of board layout, and optimal signal integrity.

4.1.4 10BASE-Te

Figure 34: 10BASE-Te Data Path



The device additionally performs all the physical layer functions of 10BASE-Te full or half duplex on twisted pair cable. It is compliant to the IEEE 802.3 standard, including the PMD, PMA, and PCS sublayers.

4.2 Loopback

The T Unit implements multiple loopback paths.

4.2.1 Line Loopback

See Section 3.3.2.

4.3 Synchronization FIFO

The T Unit has a transmit synchronization FIFO to reconcile frequency differences between the clocks of the internal XGMII/GMII/MII bus and the clock used to transmit data onto the media interface. The depth of the FIFO can be programmed by setting register 3.8002.15:14 in 10M/100M/1G mode and 3.DC8C.15:14 for 2.5G/5G mode.

The FIFO depths can be increased in length to support longer frames. The T Unit has settings for maximum frame sizes of 2 kB, 10 kB, 20 kB, and 40 kB for 10M/100M/1G mode and 10 kB, 15 kB, 20 kB, and 25 kB for 2.5G/5G mode with up to ±100 ppm clock jitter. This directly affects latency: the deeper the FIFO depth is, the higher the latency will be.

The FIFO overflow or underflow status is reported in register 3.8013.1 for 10M/100M/1G mode and 3.DC8B.1:0 for 2.5G/5G mode.

4.4 Power Management

The T Unit supports several advanced power management modes that conserve power.

4.4.1 Manual Power Down

The T Unit can be manually powered down by setting register 1.0000.11 or 3.0000.11 to 1. In general, this bit should not be set unless there is a requirement to only power down the T Unit.

When the device is operating in modes that do not require the T Unit to be operational, the T Unit will be powered down automatically regardless of the setting in register 1.0000.11 or 3.0000.11.

4.4.2 Energy Detect

The T Unit can be placed in Energy Detect power down modes by selecting either of the two Energy Detect modes. Both modes enable the PHY to wake up on its own by detecting activity on the media interface. The status of the Energy Detect is reported in register 3.8008.4 and the energy detect changes are reported in register 3.8011.4.

4.4.2.1 Energy Detect (Mode 1)

Energy Detect (Mode 1) is entered by setting register 3.8000.9:8 to 10.

In Mode 1, only the signal detection circuitry and register are active. If the PHY detects energy on the line, it starts to Auto-Negotiate sending FLPs for 5 seconds. If at the end of 5 seconds the Auto-Negotiation is not completed, then the PHY stops sending FLPs and goes back to monitoring receive energy. If Auto-Negotiation is completed, then the PHY goes into normal operation. If during normal operation the link is lost, the PHY will restart Auto-Negotiation. If no energy is detected after 5 seconds, then the PHY resumes monitoring receive energy.

4.4.2.2 Energy Detect +™ (Mode 2)

Energy Detect (Mode 2) is entered by setting register 3.8000.9:8 to 11.

In Mode 2, the PHY broadcasts a single 10 Mbps Normal Link Pulse (NLP) every one second. Except for this difference, Mode 2 is identical to Mode 1 operation. If the T Unit is in Mode 1, it cannot wake up a connected device; so the connected device must be transmitting NLPs or either device must be woken up through register access. If the T Unit is in Mode 2, then it can wake a connected device.

4.5 Auto-Negotiation

The PHY supports IEEE 802.3 Clauses 28, 40, and 55 Auto-Negotiation. The PHY also supports proprietary extensions to the Auto-Negotiation protocol.

4.5.1 802.3 Clause 28, 40, and 55 Auto-Negotiation

The 10/100/1000/2.5G/5GBASE-T Auto-Negotiation (AN) is based on IEEE 802.3 Clauses 28, 40, and 55. It is used to negotiate speed, duplex, and flow control. When Auto-Negotiation is initiated, the PHY determines whether the remote device has Auto-Negotiation capability. If so, the PHY and the remote device negotiate the speed and duplex with which to operate.

If the remote device does not have Auto-Negotiation capability, then the PHY uses the parallel detect function to determine the speed of the remote device for 100BASE-TX and 10BASE-Te modes. If the link is established based on the parallel detect function, then it is required to establish the link at half-duplex mode only. Refer to IEEE 802.3 Clauses 28, 40, and 55 for a full description of Auto-Negotiation.

The 10/100/1000/2.5G/5GBASE-T Auto-Negotiation can be enabled and disabled via register 7.0000.12. Auto-Negotiation must be enabled if the PHY operates in 1000BASE-T, 2.5GBASE-T, or 5GBASE-T. Furthermore, the extended next page control bit (7.0000.13) must also be set to 1 if the PHY must operate in 2.5GBASE-T and 5GBASE-T.

Auto MDI/MDIX and Auto-Negotiation may be disabled and enabled independently.

When Auto-Negotiation is disabled, the speed and duplex can be set via registers 1.0000.13, 1.0000.6, and 7.8000.4, respectively. Changes to any of these bits will take effect immediately when Auto-Negotiation is disabled.

When Auto-Negotiation is enabled, the abilities that are advertised can be changed via registers 7.0010, 7.0020, and 7.8000.9:8. Changes to these registers do not take effect upon a copper link drop, changes take effect only after one of the following occurs:

- A Software reset (1.0000.15, 3.0000.15, or 7.0000.15).
- A Restart Auto-Negotiation (7.0000.9).
- A transition from power down to power up (1.0000.11 or 3.0000.11).
- An Auto-Negotiation Enable bit toggles (7.0000.12).
- An Extended Next Page Enable bit toggles (7.0000.13).
- Speed and Duplex toggles while Auto-Negotiation is disabled (1.0000.13, 1.0000.6, and 7.8000.4).

Registers 7.0010, 7.0020, and 7.8000.9:8 are internally latched once every time the Auto-Negotiation enters the Ability Detect state in the arbitration state machine only following one of the events listed above. So a write into registers 7.0010, 7.0020, and 7.8000.9:8 has no effect when the PHY begins to transmit Fast Link Pulses (FLPs). This guarantees that consistent sequences of FLPs are transmitted.

If 1000BASE-T, 2.5GBASE-T, or 5GBASE-T modes are advertised, then the PHY automatically sends the appropriate next pages or extended next page to advertise the capability and negotiate master/slave mode of operation. If the user does not select to transmit additional next pages or extended next pages, then the next page bit (7.0010.15) can be set to zero (default), and no further action is required by the user.

If next pages or extended next pages in addition to those necessary for 1000BASE-T, 2.5GBASE-T, or 5GBASE-T are required, then the user can set register 7.0010.15 to 1. Additional next pages can be transmitted and received via registers 7.0016 and 7.0019, respectively. Additional extended next pages can be transmitted and received via registers 7.0016, 7.0017, 7.0018, 7.0019, 7.001A, and 7.001B, respectively.

1000BASE-T next page exchanges and 2.5GBASE-T and 5GBASE-T extended next page exchanges are automatically processed by the PHY without user intervention, regardless of whether additional next pages are sent.

When the PHY completes Auto-Negotiation, it updates the various status in registers 7.0001, 7.0013, 7.8000, and 7.8001. Various Auto-Negotiation statuses such as speed, duplex, page received, and so on are also available in registers 3.8008 and 3.8011.

IEEE 802.3 defines management registers for 10M, 100M, and 1G PHYs using the Clause 22 MDIO protocol and register space with 5-bit address. Clause 45 defines a 16-bit address space and protocol for 10G PHY management registers. The device supports the Clause 45 protocol and address space. Some of the 10M/100M/1G management register bits have an equivalent defined by IEEE 802.3 within the Clause 45 address space. However, there are also 10M/100M/1G management registers that are not defined by IEEE 802.3 within the Clause 45 address space. In the device, these management register bits are mapped into registers 7.8000, 7.8001, and 7.8002.

The changes in Auto-Negotiation settings via MDIO registers will not take into effect (including a link down event) until Auto-Negotiation restart is initiated.

4.5.2 Exchange Complete — No Link Indicator

Occasionally when a link does not come up, it is difficult to determine whether the failure is due to the Auto-Negotiation FLP not completing or from the 10/100/1000/2.5G/5GBASE-T link not being able to come up.

Register 3.8011.3 is a latched high bit that gets set to 1 whenever the FLP exchange is completed but the link cannot be established. When the bit is set, it can be cleared only by reading the register.

This bit will not be set if the FLP exchange is not completed or if link is established.

4.6 Auto Downshift

The auto downshift feature will downshift to the next highest available speed when a link fails to be established after several attempts to link. Failure to link can be caused by cabling issues such as using long Category 5 cabling for 5GBASE-T or using cable with two twisted pairs instead of four twisted pairs. In either of the previously described cases, the Auto-Negotiation will repeatedly negotiate to the higher speed, but fail to link.

With the NBASE-T downshift feature enabled, the T Unit is able to Auto-Negotiate with another link partner using cable pairs (1 and 2) and (3 and 6), respectively to downshift, and link the next highest advertised speed common between the two PHYs.

By default, the downshift feature is enabled. Setting register 1.C034.4 to 0 will disable the auto downshift feature.

Registers 1.C034 and 1.C035 specify the amount of attempts to link to 5GBASE-T, 2.5GBASE-T, and 1000BASE-T, respectively before down shifting to the next highest available speed. The number of attempts before downshift is (1.C034.3:0+1) times because the device counts from 0. So the default setting of 2 means an NBASE-T downshift occurs after 3 link failures at the current resolved speed. During an NBASE-T downshift, the number of attempts already performed is shown in the status register 1.C035.12:9 which gets reset at the next link up. Downshift for 100BASE-T and 10BASE-Te are not supported.

When the lowest available speed fails to link after the programmed number of attempts, the PHY will restart the algorithm and attempt to link at the highest available speed.

4.7 Auto MDI/MDIX Crossover

The T Unit automatically determines whether it must cross over between pairs as shown in Table 61 so that an external crossover cable is not required. If the T Unit interoperates with a device that cannot automatically correct for crossover, then the T Unit makes the necessary adjustment prior to commencing Auto-Negotiation. If the T Unit interoperates with a device that implements MDI/MDIX crossover, then a random algorithm as described in IEEE 802.3 Clause 40.4.4 determines which device performs the crossover.

When the T Unit interoperates with legacy 10BASE-Te devices that do not implement Auto-Negotiation, the T Unit follows the same algorithm as previously described since link pulses are present. However, when interoperating with legacy 100BASE-TX devices that do not implement Auto-Negotiation (for example, link pulses are not present), the T Unit uses signal detect to determine whether to crossover.

The auto MDI/MDIX crossover function can be disabled via register 3.8000.6:5.

The pin mapping in MDI and MDIX modes is shown in Table 61.

Table 61: Media Dependent Interface Pin Mapping

Pin	MDI			MDIX		
	1000/2.5G BASE-T	100BASE-TX	10BASE-Te	1000/2.5G BASE-T	100BASE-TX	10BASE-Te
MDIP/N[0]	BI_DA±	TX±	TX±	BI_DB±	RX±	RX±
MDIP/N[1]	BI_DB±	RX±	RX±	BI_DA±	TX±	TX±
MDIP/N[2]	BI_DC±	unused	unused	BI_DD±	unused	unused
MDIP/N[3]	BI_DD±	unused	unused	BI_DC±	unused	unused

Note Table 61 assumes no crossover on PCB.

The MDI/MDIX status is indicated by register 3.8008.6. This bit indicates whether the signal pairs (3 and 6) and (1 and 2), respectively are crossed over. In 5GBASE-T, 2.5GBASE-T, and 1000BASE-T operation, the device can also correct for crossover between pairs (4 and 5) and (7 and 8), respectively. However, this is not indicated by register 3.8008.6.

4.8 Auto Polarity Correction

The T Unit automatically corrects polarity errors on the receive pairs in 5GBASE-T, 2.5GBASE-T, 1000BASE-T and 10BASE-Te modes. In 100BASE-TX mode, the polarity does not matter.

In 5GBASE-T, 2.5GBASE-T, and 1000BASE-T modes, auto polarity correction is always enabled, receive polarity errors are automatically corrected based on the startup training sequence. When the training is complete, the polarity is locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

If a 1000BASE-T, 2.5GBASE-T, or 5GBASE-T link is established, registers 1.0082.11:8 (2.5G/5G) and 3.8182.11:8 (1G) report the polarity on all 4 pairs.

In 10BASE-Te mode, auto polarity correction is enabled when register 3.8000.1 is set to 0. If register 3.8000.1 is set to 1, then the polarity will be forced to normal. When enabled, polarity errors are corrected based on the detection of validly spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10BASE-Te link is up. The polarity becomes unlocked when the link is down.

The 10BASE-Te polarity correction status is indicated by register 3.8008.1. This bit indicates whether the receive pair (3 and 6) is polarity reversed in MDI mode of operation. In the MDIX mode of operation, the receive pair is (1 and 2) and register 3.8008.1 indicates whether this pair is polarity reversed. Although all pairs are corrected for receive polarity reversal, register 3.8008.1 only indicates polarity reversal on the pairs described above.

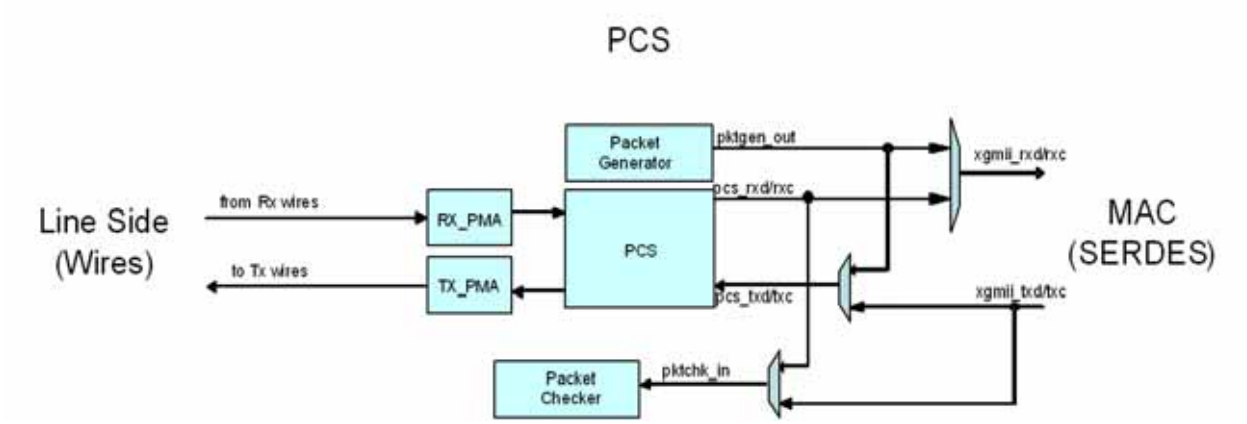
The 10BASE-Te receive polarity can be forced to negative by setting register 3.8001.9 to 1. This is useful for debugging and should not be used during normal operation.

4.9 Packet Generator and Checker

There are dedicated packet generators and checkers in the T Unit for both 2.5G/5G and 10M/100M/1G speed operation. In the T Unit, in 10M/100M/1G mode, the generator can only generate data onto the network, and the checker can only check the data coming in from the network. These packet generators enable the device to generate traffic onto the media without the need to receive data from the host. The counters in the 10M/100M/1G generator and checker are 32 bits long. To read out the 32-bit counters, the 16-bit LSB should be access first to enable the MSB values to be updated. These counters are not clear on read and these counters will be cleared when register 3.8030.0 transitions from 0 to 1.

For 2.5G/5G operation, the generator can generate data onto both the network and the line and the checker can check the data coming in from both the network and the line as shown in Figure 35. The packet checker input is controlled by register 1.C00B.3. Section 4.9.3 describes 2.5G/5G mode packet generator setup and operation. The actual injection of the packets into the data stream is enabled by registers 1.C00B.5 (for injection into xgmii_rx signal) and 1.C00B.4 (for injection into pcs_tx signal).

Figure 35: Packet Generator Data Paths



The counters in the 2.5G/5G generator and checker are 48 bits long. The counters being read out are shadow registers. To read out the content of these counters, the 16-lsb bit should be read first. Reading the 16-lsb will latch the content of the internal counters onto the shadow registers so the count will be consistent. If 3.DC90.4 and 3.DCA0.4 is set to 1, then the counters are clear on read. So reading the 16-lsb will also clear and restart the counting process while the latched value will stay in the shadow registers. If 3.DC90.4 and 3.DCA0.4 is set to 1, then the counters will keep counting until 3.DC90.6 or 3.DC90.5 is set to 1. Refer to registers 3.DC90 to 3.DCA0 for 2.5G/5G counter operation.

4.9.1 10M/100M/1G Mode Packet Generator

In the 10M/100M/1G mode, the operation of the packet generator is as follows:

1. Register 3.8030.1 enables the internal packet generator.
2. Register 3.8033 specifies the number of bytes in the packet that is to be generated. This count includes the frame bytes but does not include neither the 4-byte CRC (unless it is appended - register 3.8030.3 = 0), the terminate symbol, nor the 8 preamble bytes. If the register is set to 0x0000, then the length will be randomly selected between 64 to 1518 bytes. If the register is set to 0x0001, then the length will be randomly selected to be between 64 to 0x0FFF bytes, 0x0002 then 64 to 0x1FFF bytes, 0x0003 then 64 to 0x3FFF bytes, 0x0004 then 64 to 0x7FFF

bytes, 0x0005 then 64 to 0xFFFF bytes. If 0x0008 to 0xFFFF, then the number of bytes transmitted is fixed from 8 to 0xFFFF. Register 3.8034 specifies the number of packets to burst. 0x0000 means stop generation, 0xFFFF means continuously generate packets, 0x0001 to 0xFFFE means send a burst of 1 to 0xFFFE packets.

3. Register 3.8035 specifies the gap between packets. Each increment in the value increases the idle time by 4 bytes. 3.8035.14:0 specifies the upper limit of the gap. If 3.8035.15 is 0, then the lower limit for IPG is also specified by 3.8035.14:0. Otherwise a random gap between 1 x 4 bytes to 3.8035.14:0 x 4 bytes will be used. For the purposes of counting IPG, all lanes must be idle for it to be counted as an IPG. That is, if the terminate symbol is in the XGMII word then it does not count towards the IPG.
4. Registers 3.8031 and 3.8032 specify the initial value of the payload or the fixed value of the payload. The four bytes in this register corresponds to the first four bytes of the frame. Register 3.8030.7:4 specifies the behavior of the payload.
   - When 3.8030.7:4 = 000x, then registers 3.8031 and 3.8032 are used as the payload repeatedly.
   - When 3.8030.7:4 = 0010, then registers 3.8031 and 3.8032 are used as the payload repeatedly but every other GMII word should be inverted. That is, a payload of 034EA675 will result in a sequence of 034EA675, FCB1598A, 034EA675, FCB1598A, and so on.
   - When 3.8030.7:4 = 0011, then registers 3.8031 and 3.8032 are used as the payload repeatedly but inverted every second XGMII word. That is, a payload of 034EA675 will result in a sequence of 034EA675, 034EA675, FCB1598A, FCB1598A, 034EA675, 034EA675, FCB1598A, FCB1598A, and so on.
   - When 3.8030.7:4 = 0100, then registers 3.8031 and 3.8032 are used as the initial value and each byte subsequently bitwise left shifted. That is, a payload of 034EA675 will result in a sequence of 034EA675, 069C4DEA, 0C399AD5, 187235AB, and so on.
   - When 3.8030.7:4 = 0101, then registers 3.8031 and 3.8032 are used as the initial value and each byte subsequently bitwise right shifted.
   - When 3.8030.7:4 = 0110, then registers 3.8031 and 3.8032 are used as the initial value and the 32 bits subsequently bitwise left shifted. That is, a payload of C34EA675 will result in a sequence of C34EA675, 869D4CEB, 0D3A99D7, 1A7533AE, and so on.
   - When 3.8030.7:4 = 0111, then registers 3.8031 and 3.8032 are used as the initial value and the 32 bits subsequently bitwise right shifted.
   - When 3.8030.7:4 = 1000, then registers 3.8031 and 3.8032 are used as the initial value and subsequently bytewise incremented. That is, a payload of FFFE0055 will result in a sequence of FFFE0055, 00FF0156, 01000257, 02010358, and so on.
   - When 3.8030.7:4 = 1001, then registers 3.8031 and 3.8032 are used as the initial value and subsequently bytewise decremented.
   - When 3.8030.7:4 = 1000, then registers 3.8031 and 3.8032 are ignored and a pseudo-random payload is generated. All 4 bytes are the same value for each cycle.
   - When 3.8030.7:4 = 1001 then registers 3.8031 and 3.8032 are ignored and a pseudo-random payload is generated. All 4 bytes are randomly generated for each cycle.

At the start of each packet registers 3.8031 and 3.8032 should be used to reset the initial values to ensure that the pattern in the packet is the same when repeated over and over many times. The only time that the pattern in the packet will be different is when pseudo-random generation is selected.

For each packet generated, the 32-bit counter in 3.8036 and 3.8037 is incremented by 1.

For each byte generated, the 32-bit counter in 3.8038 and 3.8039 is incremented by 1.

Preamble bytes are not counted, but CRC bytes are counted.

Register 3.8030.3 controls whether the CRC is generated.

4.9.2 10M/100M/1G Mode Packet Checker

The 10M/100M/1G mode CRC checker is enabled by setting register 3.8030.1 to 1.

There are three sets of 32-bit counters for the checker. Registers 3.803A and 3.803B are the receive packet counters. Registers 3.803E and 3.803F are the receive packet error counters.

Registers 3.803C and 3.803D are the receive byte counters. The receive packet counter counts the number of packets received regardless of whether there is a CRC error. The receive packet error counter increments once per packet with a CRC error. The byte counter counts the number of bytes in the frame including the CRC. The preamble bytes are not counted.

4.9.3 2.5G/5G Mode Packet Generator and Checker

For 2.5G/5G operation, the generator can generate data onto both the network and the line and the checker can check the data coming in from both the network and the line. Also, the counters in the 2.5G/5G generator and checker are 48-bit long. Refer to Section 4.9 for details.

The function of the 2.5G/5G generator and checker is similar to the 10M/100M/1G counterpart, except some of the control functions can be individually controlled between generator and checker. The register equivalence is summarized in Table 62. Refer to the register description of 3.DC90-3.DC9C and 3.DCA0-3.DCA9 for details.

Table 62: Generator/Checker Register Equivalence Between the 10M/100M/1G Mode

Description	10M/100M/1G Mode	2.5G/5G Mode
Internal packet generation control	3.8030.7:4	3.DC91.7:4
CRC generation	3.8030.3	3.DC91.3
Packet Generator Enable	3.8030.2	3.DC90.1:0
CRC Checker Enable	3.8030.1	3.DCA0.1:0
Generator Counter Clear on read	N/A	3.DC90.4
Checker Counter Clear on read	N/A	3.DCA0.2
Generator Counter Reset	3.8030.0	3.DC90.6:5
Checker Counter Reset	3.8030.0	3.DCA0.3
XOR Mask Byte 1/Byte 1	3.8031.15:8	3.DC92.15:8
XOR Mask Byte 0/Byte 0	3.8031.7:0	3.DC92.7:0
XOR Mask Byte 3/Byte 3	3.8032.15:8	3.DC93.15:8
XOR Mask Byte 2/Byte 2	3.8032.7:0	3.DC93.7:0
Number of bytes in packet	3.8033.15:0	3.DC94.15:0
Number of packets to send	3.8034.15:0	3.DC95.15:0
Random IPG	3.8035.1	3.DC96.15
IPG duration	3.8035.14:0	3.DC96.14:0
Transmit packet count LSB	3.8036.15:0	3.DC97.15:0
Transmit packet count MID-16 bit	N/A	3.DC98.15:0

Table 62: Generator/Checker Register Equivalence Between the 10M/100M/1G Mode (Continued)

Description	10M/100M/1G Mode	2.5G/5G Mode
Transmit packet count MSB	3.8037.15:0	3.DC99.15:0
Transmit byte count LSB	3.8038.15:0	3.DC9A.15:0
Transmit byte count MID-16 bit	N/A	3.DC9B.15:0
Transmit byte count MSB	3.8039.15:0	3.DC9C.15:0
Receive packet count LSB	3.803A.15:0	3.DCA1.15:0
Receive packet count MID-16 bit	N/A	3.DCA2.15:0
Receive packet count MSB	3.803B.15:0	3.DCA3.15:0
Receive byte count LSB	3.803C.15:0	3.DCA4.15:0
Receive byte count MID-16 bit	N/A	3.DCA5.15:0
Receive byte count MSB	3.803D.15:0	3.DCA6.15:0
Packet Error Count LSB	3.803E.15:0	3.DCA7.15:0
Packet Error Count MID-16 bit	N/A	3.DCA8.15:0
Packet Error Count MSB	3.803F.15:0	3.DCA9.15:0

4.9.4 Link Drop Counter

A 16-bit register that counts the number of link drop events is available in register 1.C056. The control of the counter is available in 1.C055 and its functionality and control options are similar to the control options for the packet checker. 1.C055.1 will select if the counter will rollover or saturate at 0xffff.

4.10 Interrupt

The T Unit supports various interrupts.

For 2.5G/5G/10G interrupt events for 88E2180 devices,

- Register 1.C007 is the interrupt status register.

Register 1.C006 is the interrupt status register.

For 10M/100M/1G interrupt events for 88E2180 and 88E2110 devices,

- Registers 3.8011 and 3.8013 are the interrupt status registers.
- Registers 3.8010 and 3.8012 are the interrupt enable registers.

The interrupt pin will be activated if any of the enabled events in the interrupt status registers occurs. If a certain interrupt event is not enabled by interrupt enable registers, it will still be indicated by the corresponding interrupt status registers bits if the interrupt event occurs. However, the unselected events will not cause the interrupt pin to be activated. The interrupts are cleared by reading the interrupt status registers.

The T Unit interrupts are aggregated in the Global Interrupt register 3.F040.

5 Host Interface Unit (H Unit)

The 88E2110 device host-side interface comprises one differential input lane and one differential output lane, designed to operate over short backplanes to the host device. It can operate in SXGMII, 10GBASE-R, 5GBASE-R, 2500BASE-X and SGMII.

The 88E2180 device is an 8-port device and the host-side interface can be arranged to form SXGMII, 10GBASE-R, 5GBASE-R, 2500BASE-X, and SGMII.

5.1 Host Electrical Interface

The input and output buffers of the SERDES interface are internally terminated by 50Ω impedance (100Ω differential). No external terminations are required.

The SERDES transmitter has a three tap (1 pre-tap and 1 post-tap) FIR filter for channel equalization. The FIR tap can be manually adjusted to optimize the transmit eye over a particular channel.

The receiver performs clock and data recovery and de-serializes the data.

The polarity of the H Unit inputs and outputs can be inverted.

- 30.8040.7 inverts input polarity: 1 = Normal (default), 0 = Invert
- 30.8040.5 inverts output polarity: 0 = Normal (default), 1 = Invert

5.2 PCS

The host interface supports several different PCS. Register 1.C04A.2:0 determines the behavior of the host interface as shown in Table 63 for the 88E2110 device and Table 64 for the 88E2180 device.

Table 63: 88E2110 Host Interface Configuration

	Line Rate				
1.C04A[2:0], but read back value is checked with 31.F001[2:0]	**5 Gbps**	**2.5 Gbps**	**1 Gbps**	**100 Mbps**	**10 Mbps**
000	SXGMII				
001	Reserved				
010	Reserved				
011	Reserved				
100	5GBASE-R	2500BASE-X	SGMII Auto-Negotiation On		
101	5GBASE-R	2500BASE-X	SGMII Auto-Negotiation Off		
110	Reserved				
111	Reserved				

Table 64: 88E2180 Host Interface Configuration

	Line Rate				
1.C04A[2:0], but read back value is checked with 31.F001[2:0]	**5 Gbps**	**2.5 Gbps**	**1 Gbps**	**100 Mbps**	**10 Mbps**
000	SXGMII				
001	Reserved				
010	Reserved				
011	Reserved				
100	5GBASE-R	2500BASE-X	SGMII Auto-Negotiation On		
101	5GBASE-R	2500BASE-X	SGMII Auto-Negotiation Off		
110	Reserved				
111	Reserved				

For the 88E2180 device, the 5GBASE-R PCS is enabled by setting register 1.C04A.2:0 = 100 or 101 and the line rate is 5 Gbps.

For the 88E2110 device, the 5GBASE-R PCS is enabled by setting register 1.C04A.2:0 = 100 and 101 and the line rate is 5 Gbps.

5.2.1 2500BASE-X

For the 88E2180 device, the 2500BASE-X PCS is enabled by setting register 1.C04A.2:0 = 100 or 101 and the line rate is 2.5 Gbps. 2500BASE-X is identical to 1000GBASE-X operation except at 2.5 times speed. Auto-Negotiation is not supported in 2500BASE-X.

For the 88E2110 device, the 2500BASE-X PCS is enabled by setting register 1.C04A.2:0 = 100 and 101 and the line rate is 2.5 Gbps. 2500BASE-X is identical to 1000GBASE-X operation except at 2.5 times speed. Auto-Negotiation is not supported in 2500BASE-X.

5.2.2 SGMII

For the 88E2180 device, the SGMII is enabled by setting register 1.C04A.2:0 = 100 and 101 and the line rate is 10/100/1000 Mbps. SGMII Auto-Negotiation is enabled with the 100 setting.

For the 88E2110 device, the SGMII is enabled by setting register 1.C04A.2:0 = 100 and 101 and the line rate is 10/100/1000 Mbps. SGMII Auto-Negotiation is enabled with 100 setting.

5.2.2.1 PCS

The 1000BASE-X PCS operates according to Clause 36 of the IEEE 802.3 specification. The PCS uses a 8/10 coding for DC line balancing. For further details, refer to the IEEE 802.3 specification.

The SGMII protocol is also supported over 1000BASE-X. The SGMII allows 10 Mbps, 100 Mbps, and 1000 Mbps throughput over 1000BASE-X line coding.

When SGMII Auto-Negotiation is turned off (4.2000.12 = 0), the speed setting is programmed via register 4.2000 bits 13 and 6. Link is established when the underlying 1000BASE-X establishes link.

When SGMII Auto-Negotiation is turned on (4.2000.12 = 1), the SGMII is set to the speed of the line interface. This speed capability is advertised and Auto-Negotiation has to complete prior to link being established.

5.2.2.2 SGMII Auto-Negotiation

SGMII is a de-facto standard designed by Cisco. SGMII uses 1000BASE-X coding to send data as well as Auto-Negotiation information between the PHY and the MAC. However, the contents of the SGMII Auto-Negotiation are different than the 1000BASE-X Auto-Negotiation. See the *Cisco SGMII Specification* and the *MAC Interfaces and Auto-Negotiation Application Not*e for further details.

The device supports SGMII interface with and without Auto-Negotiation. Auto-Negotiation can be enabled or disabled by writing to register 4.2000.12. If SGMII Auto-Negotiation is disabled, then the MAC interface link, speed, and duplex status (determined by the media side) cannot be conveyed to the MAC from the PHY. The user must program the MAC with this information in some other method (for example, by reading PHY registers for link, speed, and duplex status).

5.2.2.3 Auto-Negotiation Bypass Mode

If the MAC or the PHY implements the Auto-Negotiation function and the other does not, two-way communication is not possible unless Auto-Negotiation is manually disabled and both sides are configured to work in the same operational modes. To solve this problem, the device implements the SGMII Interface Auto-Negotiation Bypass Mode. When entering the state Ability_Detect, a bypass timer begins to count down from an initial value of approximately 200 ms. If the device receives idles during the 200 ms, the device will interpret that the other side is active, but cannot send configuration codes to perform Auto-Negotiation. After 200 ms, the state machine will move to a new state called Bypass_Link_Up in which the device assumes a link-up status and the operational mode is set to the value listed under the Comments column of Table 65.

Table 65: SGMII Auto-Negotiation Modes

Register 4.2000.12	Register 4.A000.13	Comments
0	X	No Auto-Negotiation. User responsible for determining speed, link, and duplex status by reading PHY registers.
1	0	Normal SGMII Auto-Negotiation. Speed, link, and duplex status automatically communicated to the MAC during Auto-Negotiation.
1	1	MAC Auto-Negotiation enabled. Normal operation.
		MAC Auto-Negotiation disabled. After 200 ms the PHY will disable Auto-Negotiation and link based on idles.

5.2.3 SXGMII

SXGMII is enabled by setting register 1.C04A.2:0 = 000.

SXGMII is a host interface standard specified by the NBASE-T Alliance™. SXGMII uses 10GBASE-R coding to send data for all data rates. Groups of four bytes of packet data are replicated 1, 2, 4, 10, 100, or 1000 times when operating in 10 Gbps, 5 Gbps, 2.5 Gbps, 1 Gbps, 100 Mbps, or 10 Mbps, respectively. Auto-Negotiation information between the PHY and the MAC are exchanged via ordered sets.

The SXGMII Auto-Negotiation Mechanism is based on Clause 37 and follows Clause 37-6 functions with following modifications:

i) Next page is not supported.
ii) an_sync_status=fail changed to block_lock=false (restart Autoneg FSM)
iii) Autoneg FSM will restart whenever the link changes
iv) rudi (invalid) changed to idle received during an_restart, ability_detect, acknowledge_ detect
v) Link_timer changed to be configurable from 1 ms to 2 ms in steps of 0.1 ms.
vi) Ability_match and acknowledge_match as per figure 37-6

Extended ordered sets are used for Auto-Negotiation. SXGMII Auto-Negotiation registers 4.F0A0 and 4.F0A1 must be programmed for configuration. Upon completion of the SXGMII Auto-Negotiation and setting of the link speed register, replication and sampling of the packet data starts in both egress and ingress direction.

On the ingress direction, data from line-side PCS is first converted to 4-byte XGMII data if it is not XGMII data and replicated 1, 2, 4, 10, 100, or 1000 times depending on the line-side PCS speed 10 Gbps, 5 Gbps, 2.5 Gbps, 1 Gbps, 100 Mbps, or 10 Mbps. The data is sent to 10GR TX PCS for transmission.

5.3 Loopback

The H Unit implements multiple loopback paths.

5.3.1 MAC Loopback

See Section 3.3.1.

5.4 Power Management

The device will automatically power down unused circuits. The host side can be forced into a power down state by setting 4.1000.11 or 4.2000.11. These power down registers are physically the same bit even though they reside in different locations.

To soft reset only the host side, set registers 4.1000.15 or 4.2000.15. These software reset registers are physically the same bit even though they reside in different locations.

5.5 Traffic Generation and Checking

This section describes the generator and checker functions. All counters are 48 bits long. If register 4.F010.15 is set to 1, then the counters clear on read. If register 4.F010.15 is set to 0, then the counters continue counting until 4.F010.6 is set to 1 to clear the contents.

Each 48-bit counter is atomically latched into a holding register (and cleared at the same time if 4.F010.15 = 1) when either of the following two events occur:

1. A write command occurs when DEVAD = 4 and REGAD is set to the address of the least significant 16-bit of the counter.
2. A read increment command occurs when DEVAD = 4 and the post read incremented REGAD is set to the address of the least significant 16-bit of the counter.

The implication is that the least significant 16-bit of the counter has to be read first.

5.5.1 Packet Generator

A packet generator enables the device to generate traffic onto the host without the need to receive data from the media.

Register 4.F010.1 enables the internal packet generator. To disable the packet generator, ensure that 4.F017 is set to 0000 first, otherwise, packet fragments will result.

Register 4.F016 specifies the number of bytes in the packet that is to be generated. This count includes the frame bytes but includes neither the 4-byte CRC (unless it is appended - register 4.F011.3 = 0), the terminate symbol, nor the 8 preamble bytes. If the register is set to 0x0000, then the length will be randomly selected between 64 to 1518 bytes. If the register is set to 0x0001, then the length will be randomly selected to be between 64 to 0x0FFF bytes, 0x0002 then 64 to 0x1FFF bytes, 0x0003 then 64 to 0x3FFF bytes, 0x0004 then 64 to 0x7FFF bytes, 0x0005 then 64 to 0xFFFF bytes. If 0x0008 to 0xFFFF, then the number of bytes transmitted is fixed from 8 to 0xFFFF.

Register 4.F017 specifies the number of packets to burst. 0x0000 means stop generation, 0xFFFF means continuously generate packets, 0x0001 to 0xFFFE means send a burst of 1 to 0xFFFE packets.

Register 4.F018 specifies the gap between packets. Each increment in the value increases the idle time by 4 bytes. 4.F018.14:0 specifies the upper limit of the gap. If 4.F018.15 is 0, then the lower limit for IPG is also specified by 4.F018.14:0. Otherwise, a random gap between 1 x 4 bytes to 4.F018.14:0 x 4 bytes will be used. For the purposes of counting IPG, all lanes must be idle for it to be counted as an IPG. That is, if the terminate symbol is in the XGMII word, then it does not count towards the IPG.

Registers 4.F012 and 4.F013 specify the initial value of the payload or the fixed value of the payload. The four bytes in this register corresponds to the first four bytes of the frame. Register 4.F011.7:4 specifies the behavior of the payload.

When 4.F011.7:4 = 000x, then registers 4.F012 and 4.F013 are used as the payload repeatedly.

When 4.F011.7:4 = 0010, then registers 4.F012 and 4.F013 are used as the payload repeatedly but every other XGMII word should be inverted. That is, a payload of 034EA675 will result in a sequence of 034EA675, FCB1598A, 034EA675, FCB1598A, and so on.

When 4.F011.7:4 = 0011, then registers 4.F012 and 4.F013 are used as the payload repeatedly but inverted every second XGMII word. That is, a payload of 034EA675 will result in a sequence of 034EA675, 034EA675, FCB1598A, FCB1598A, 034EA675, 034EA675, FCB1598A, FCB1598A, and so on.

When 4.F011.7:4 = 0100, then registers 4.F012 and 4.F013 are used as the initial value and each byte subsequently bitwise left shifted. That is, a payload of 034EA675 will result in a sequence of 034EA675, 069C4DEA, 0C399AD5, 187235AB, and so on.

When 4.F011.7:4 = 0101, then registers 4.F012 and 4.F013 are used as the initial value and each byte subsequently bitwise right shifted.

When 4.F011.7:4 = 0110, then registers 4.F012 and 4.F013 are used as the initial value and the 32 bits subsequently bitwise left shifted. That is, a payload of C34EA675 will result in a sequence of C34EA675, 869D4CEB, 0D3A99D7, 1A7533AE, and so on.

When 4.F011.7:4 = 0111, then registers 4.F012 and 4.F013 are used as the initial value and the 32 bits subsequently bitwise right shifted.

When 4.F011.7:4 = 1000, then registers 4.F012 and 4.F013 are used as the initial value and subsequently bytewise incremented. That is, a payload of FFFE0055 will result in a sequence of FFFE0055, 00FF0156, 01000257, 02010358, and so on.

When 4.F011.7:4 = 1001, then registers 4.F012 and 4.F013 are used as the initial value and subsequently bytewise decremented.

When 4.F011.7:4 = 1000, then registers 4.F012 and 4.F013 are ignored and a pseudo-random payload is generated. All 4 bytes are the same value for each cycle.

When 4.F011.7:4 = 1001, then registers 4.F012 and 4.F013 are ignored and a pseudo-random payload is generated. All 4 bytes are randomly generated for each cycle.

At the start of each packet registers 4.F012 and 4.F013 should be used to reset the initial values to ensure that the pattern in the packet is the same when repeated over and over many times. The only time that the pattern in the packet will be different is when pseudo-random generation is selected.

For each packet generated, the 48-bit counter in 4.F01B, 4.F01C, and 4.F01D is incremented by 1.

For each byte generated, the 48-bit counter in 4.F01E, 4.F01F, and 4.F020 is incremented by 1. Preamble bytes are not counted but CRC bytes are counted.

Register 4.F011.3 controls whether CRC is generated.

5.5.2 Checker

The CRC checker is enabled by setting register 4.F010.0 to 1.

If register 4.F010.2 = 0, then the checker will wait until the start of frame delimiter (SFD) is detected to detect the frame boundary.

If register 4.F010.2 = 1, then the checker will assume the first eight bytes of the packet is the preamble and the frame starts at the ninth byte of the packet.

There are three sets of 48-bit counters for the checker. Registers 4.F021, 4.F022, and 4.F023 are the receive packet counters. Registers 4.F027, 4.F028, and 4.F029 are the receive packet error counters. Register 4.F024, 4.F025, and 4.F026 are the receive byte counters. The receive packet counter counts the number of packets received regardless of whether there is a CRC error. The receive packet error counter increments once per packet with a CRC error. The byte counter counts the number of bytes in the frame including the CRC. The preamble bytes are not counted.

5.5.3 Link Drop Counter

A 16-bit register that counts the number of link drop events is available in register 4.F02A. The counter will automatically be powered up and count all link drop events as the H Unit is released from reset. The control of the counter is the same as the packet checker controls in 4.F010. To determine the number of link drop events between a certain time period, the counter should be reset at the onset of the link drop monitoring period by using 4.F010.15 and 4.F010.6. To reset only the link drop counter, set up the counter read clear mode by setting register 4.F010.15 and read register 4.F02A. The link drop counter will be reset and start counting again. To reset all counters, set 4.F010.15 to zero and then assert and de-assert 4.F010.6. Register 4.F010.6 is not a self-clear bit and to restart counting, the bit must be set to zero.

5.6 PRBS and Pattern Generators

The device supports various IEEE defined and proprietary PRBS generators and checkers, and transmit waveform pattern generators. Only one generator or checker may be enabled at a time. Unpredictable results may occur if multiple generators are enabled simultaneously.

5.6.1 General PRBS Generators and Checkers

The following description is for PRBS generators or checkers in registers 4.F030 to 4.F039.

Register 4.F030 controls the generator and checker.

Setting register 4.F030.5 to 1 enables the generator and setting register 4.F030.4 to 1 enables the checker. If either of these bits is set to 1, then the general PRBS generator and checker overrides the PCS-specific generators and checkers.

Register 4.F030.3:0 controls the pattern that is generated and checked. There is no checker for the high-frequency, low-frequency, mixed-frequency, and square-wave patterns as there are waveforms to check the transmitter performance.

- 0000 = IEEE 49.2.8 - PRBS 31
- 0001 = PRBS 7
- 0010 = PRBS 9 IEEE 83.7
- 0011 = PRBS 23
- 0100 = PRBS 31 Inverted
- 0101 = PRBS 7 Inverted
- 1000 = PRBS 15
- 1001 = PRBS 15 Inverted
- 0110 = PRBS 9 Inverted
- 0111 = PRBS 23 Inverted
- 1100 = High-frequency pattern
- 1101 = Low-frequency pattern

- 1110 = Mixed-frequency pattern
- 1111 = Square-wave pattern

All counters are 48 bits long. If register 4.F030.13 is set to 1, then the counters will clear on read. If register 4.F030.13 is set to 0, then the counters will keep counting until register 4.F030.6 is set to 1 to clear the contents. If register 4.F030.7 is set to 0, then the PRBS counters will not start to count until the checker first locks onto the incoming PRBS data. If register 4.F030.7 is set to 1, then the PRBS checker will start counting errors without first locking to the incoming PRBS data.

Each 48-bit counter is atomically latched into a holding register (and cleared at the same time if 4.F030.13 = 1) when either of the following two events occur:

1. A write command occurs when DEVAD = 4 and REGAD is set to the address of the least significant 16 bits of the counter.
2. A read increment command occurs when DEVAD = 4 and the post read incremented REGAD is set to the address of the least significant 16 bits of the counter.

The implication is that the least significant 16-bit of the counter has to be read first.

Registers 4.F031, 4.F032, and 4.F033 are the transmit bit counters. Registers 4.F034, 4.F035, and 4.F036 are the receive bit counters. Registers 4.F037, 4.F038, and 4.F039 are the receive bit error counters.

5.6.1.1 PRBS Count Over Time Interval

In the 88E2180/88E2110 device, a PRBS count over time interval is supported via the following:

- 16-bit counter (4.F041) that increments one time every 2 seconds (elapsed time) after PRBS locks. (Elapse_Timer)
- 48-bit counter (4.F044 – 4.F042) that adds error count in to the internal counter every 2 seconds before being cleared (Error_Count)

This group of counters will have separate clear_on_read control register bits (in 4.F040) similar to the other counters in the PRBS block. These counters should always be considered as a group for reading and reset purpose so that exact BER can be formed from the error counts/elapse_time. To read out these registers, a register read to the elapse timer (4.F041) should be performed first so that internal counter values for elapse_time and error_count will be latched onto shadow registers at the same time. Only after a register read from 4.F041 will the contents of 4.F044-4.F042 be valid, otherwise, the register only contains the latched values from the last 4.F041 read. If clear_on_read mode is set, then the contents of elapse_timer and error_count will be reset and the count will restart from zero. If clear_on_read is not set, then the register will continue to count.

5.7 Interrupt

The host PCS supports several interrupts.

The INTn interrupt pin will be active if any of the events enabled in the interrupt enable register occurs. If an interrupt event corresponding to a disabled interrupt enable bit occurs, then the corresponding interrupt status bit will be set even though the event does not activate the INTn pin. The interrupts are cleared after a read to the interrupt status register.

6 Electrical Specifications

6.1 Absolute Maximum Ratings

Table 66: Absolute Maximum Ratings

Stresses above those listed in Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Symbol	Parameter	Min	Typ	Max	Units
V_{DDAC}	Power Supply Voltage on AVDDC with respect to VSS	-0.5	–	2.5	V
V_{DDA15}	Power Supply Voltage on AVDDL with respect to VSS	-0.5	–	2.5	V
V_{DDAH}	Power Supply Voltage on AVDDH with respect to VSS	-0.5	–	2.5	V
V_{DDAT}	Power Supply Voltage on AVDDT with respect to VSS	-0.5	–	3.6	V
V_{DDAR}	Power Supply Voltage on AVDDR with respect to VSS	-0.5	–	2.5	V
V_{DDAS}	Power Supply Voltage on AVDDS with respect to VSS	-0.5	–	2.5	V
V_{DD}	Power Supply Voltage on DVDD with respect to VSS	-0.5	–	1.2	V
V_{DDO}	Power Supply Voltage on VDDOL, VDDOM and VDDOT with respect to VSS	-0.5	–	3.6	V
V_{PIN}	Voltage Applied to Any Digital Input Pin	-0.5	–	3.6	V
$T_{STORAGE}$[1]	Storage Temperature	-55	–	+125[2]	°C

1. The conditions for storing unpowered and unmounted devices are as follows:
   - Packed inside a vacuum-sealed moisture barrier bag with desiccant and humidity indicator card (HIC)
   - Stored at <40°C and <90% relative humidity (RH)
2. 125°C is only used as bake temperature for not more than 24 hours. Long-term storage (for example, weeks or longer) should be kept at 85°C or lower.

6.2 Recommended Operating Conditions

Table 67: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DDAC}[1]	AVDDC Supply	For AVDDC	1.455	1.5	1.545	V
			1.746	1.8	1.854	V
V_{DDAL}[1]	AVDDL Supply	For AVDDL	1.455	1.5	1.545	V
			1.746	1.8	1.854	V
V_{DDAH}[1]	AVDDH Supply	For AVDDH	1.746	1.8	1.854	V
V_{DDAT}[1]	AVDDT Supply	For AVDDT	3.201	3.3	3.399	V
V_{DDAR}[1]	AVDDR Supply	For AVDDR	1.455	1.5	1.545	V
			1.746	1.8	1.854	V
V_{DDAS}[1]	AVDDS Supply	For AVDDS	1.455	1.5	1.545	V
			1.746	1.8	1.854	V
V_{DD}[1]	DVDD Supply	For DVDD (C-temp)	0.776	0.8	0.824	V
		For DVDD (I-temp)	0.854	0.88	0.906	V
V_{DDO}[1]	VDDOL, VDDOM, and VDDOT Supply	For VDDOM at 1.2V	1.14	1.2	1.26	V
		For VDDO* at 1.5V	1.425	1.5	1.575	V
		For VDDO* at 1.8V	1.71	1.8	1.89	V
		For VDDO* at 2.5V	2.375	2.5	2.625	V
		For VDDO* at 3.3V	3.135	3.3	3.465	V
IREF	Internal Bias Reference IREF	Resistor connected to V_{SS}	–	4.99K ±1% Tolerance	–	Ω
T_A	Ambient Operating Temperature	Commercial Parts[2, 3]	0	–	70	°C
		Industrial Parts[4]	-40	–	85	°C
T_J	Maximum Junction Temperature	–	–	–	105[5]	°C

1. Maximum noise allowed on supplies is 25 mV peak-peak.
2. Commercial operating temperatures are typically below 70°C, for example, 45°C~55°C. The 70°C maximum is Marvell specification limit.
3. The recommended operating conditions assume that the ripple is included. DC operating conditions with the ripple should never exceed the recommended operating levels. For example, on a system (DVDD supply - 12.5 mV) should be less than 0.776V.
4. Industrial parts have an *I* following the commercial part numbers. See Section 8.1, Part Order Numbering, on page 155.
5. Refer to the white paper on T_J Thermal Calculations for detailed information.

6.3 Package Thermal Information

6.3.1 Thermal Conditions for 104-pin, FC-TFBGA Package for the 88E2110 Device

Table 68: Thermal Conditions for 104-pin, FC-TFBGA Package for the 88E2110 Device

Symbol	Parameter	Condition	Min	Typ	Max	Units
θ_{JA}	Thermal Resistance[1] - Junction to Ambient for the 104-pin, FC-TFBGA Package $\theta_{JA} = (T_J - T_A)/P$ P = Total Power Dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow	–	22.5	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow	–	19.07	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow	–	18.20	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow	–	17.60	–	°C/W
ψ_{JT}	Thermal Characteristic Parameter[a] - Junction to the Top Center of the 104-pin, FC-TFBGA Package $\psi_{JT} = (T_J - T_{top})/P$ P = Total Power Dissipation, $T_{top:}$ Temperature on the Top Center of the Package	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow	–	0.10	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow	–	0.11	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow	–	0.12	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow	–	0.13	–	°C/W
θ_{JC}	Thermal Resistance[a] - Junction to Case for the 104-pin, FC-TFBGA Package $\theta_{JC} = (T_J - T_C)/ P_{top}$ P_{top} = Power Dissipation from the Top of the Package	JEDEC with no air flow	–	5.3	–	°C/W
θ_{JB}	Thermal Resistance[a] - Junction to Board for the 104-pin, FC-TFBGA Package $\theta_{JB} = (T_J - T_B)/P_{bottom}$ P_{bottom} = Power Dissipation from the Bottom of the Package to the PCB Surface	JEDEC with no air flow	–	8.4	–	°C/W

1. Refer to the white paper on T_J Thermal Calculations for detailed information.

6.3.2 Thermal Conditions for 529-pin, HFCBGA Package for the 88E2180 Device

Table 69: Thermal Conditions for 529-pin, HFCBGA Package for the 88E2180 Device

Symbol	Parameter	Condition	Min	Typ	Max	Units
θ_{JA}	Thermal Resistance[1] - Junction to Ambient for the 529-pin, HFCBGA Package $\theta_{JA} = (T_J - T_A)/P$ P = Total Power Dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow	—	10.08	—	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow	—	8.81	—	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow	—	7.96	—	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow	—	7.38	—	°C/W
ψ_{JT}	Thermal Characteristic Parameter[a] - Junction to the Top Center of the 529-pin, HFCBGA Package $\psi_{JT} = (T_J - T_{top})/P$ P = Total Power Dissipation, T_{top}: Temperature on the Top Center of the Package	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow	—	0.11	—	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow	—	0.14	—	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow	—	0.16	—	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow	—	0.18	—	°C/W
θ_{JC}	Thermal Resistance[a] - Junction to the Case for the 529-pin, HFCBGA Package $\theta_{JC} = (T_J - T_C)/P_{top}$ P_{top} = Power Dissipation from the Top of the Package	JEDEC with no air flow	—	0.36	—	°C/W
θ_{JB}	Thermal Resistance[a] - Junction to the Board for the 529-pin, HFCBGA Package $\theta_{JB} = (T_J - T_B)/P_{bottom}$ P_{bottom} = Power Dissipation from the Bottom of the Package to the PCB Surface	JEDEC with no air flow	—	2.65	—	°C/W

1. Refer to the white paper on T_J Thermal Calculations for detailed information.

6.4 Current Consumption

The current consumption is broken down by each power supply. The total current consumption for each power supply is calculated by summing the various components in the following tables. The total chip power consumption is calculated as follows:

$Isupply\_Total\_T_J = Isupply\_Base\_T_J + Isupply\_T_J + I\_supply\_CMS$

Note Supply is one of AVDDT, AVDDL, AVDDH, AVDD15, and DVDD. $Isupply\_Total\_T_J$ is the current for a specific junction temperature and is different for I-temp and C-temp devices.

6.4.1 Current Consumption for C-Temp

Table 70: Base Current Consumption for C-Temp Devices[1]

Symbol	Parameter	Pins	Condition	Base Current Consumption (mA)		
				T_J = 70°C (nominal)[2]	T_J = 105°C (nominal)[2]	T_J = 105°C
$I_{ADVDD33}$	Copper 3.3V	AVDDT	All ports are powered down.	10	10	10
I_{AVDD20}	AVDD 1.8V	AVDDH	All ports are powered down.	6	6	6
I_{AVD15}	Copper and SERDES 1.5V	AVDDL, AVDDS, AVDDR, AVDDC	All ports are powered down.	37	40	44
I_{DVDD}	Digital Core (0.8V)	DVDD	All ports are powered down.	63	158	323

1. Base current consumption is the worst case leakage with T_J = 105°C and margined supplies.
2. Base current measured with nominal device.

Table 71: Operational Current Consumption for per Port[1] — Excludes Base Current

Symbol	Parameter	Pins	Condition	Base Current Consumption (mA)		
			(Host to Line)	T_J = 70°C (nominal)[2]	T_J = 105°C (nominal)[2]	T_J = 105°C
$I_{ADVDD33}$	Copper 3.3V	AVDDT	2500BASE-X to 2.5GBASE-T	106	108	108
			5GBASE-R to 5GBASE-T	107	109	109
I_{AVDD20}	AVDD 1.8V	AVDDH	2500BASE-X to 2.5GBASE-T	148	152	152
			5GBASE-R to 5GBASE-T	208	213	213
I_{AVD15}	Copper and SERDES 1.5V	AVDDL, AVDDS, AVDDR, AVDDC	2500BASE-X to 2.5GBASE-T	199	203	206
			5GBASE-R to 5GBASE-T	226	230	233
I_{DVDD}	Digital Core (0.8V)	DVDD	2500BASE-X to 2.5GBASE-T	300	306	345
			5GBASE-R to 5GBASE-T	590	598	627

1. Current consumption was measured under these specific conditions: cable length = 100m CAT 5e with 3 dB ILM cable, junction temperature = 105°C, voltages margined.
2. Current measured with nominal device.

6.4.2 Additive Current Consumption for C-Temp per Port

Table 72: CMS Enabled

Symbol	Parameter	Pins	Condition	Current Consumption per BASE-T Operation Speed[1, 2] (mA)	
				5GBASE-T	2.5GBASE-T
I_{AVDD20}	AVDD 1.8V	AVDDH	All ports are powered down.	39	39
I_{AVD15}	Copper and SERDES 1.5V	AVDDL, AVDDS, AVDDR, AVDDC	All ports are powered down.	5	5
I_{DVDD}	Digital Core (0.8V)	DVDD	All ports are powered down.	43	22

1. The current consumption is not applicable at all other speeds of operation except for those listed.
2. Current consumption does not vary with T_J.

6.5 Digital I/O Electrical Specifications

6.5.1 DC Operating Conditions

Table 73: DC Operating Conditions
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
VIH	Input High Voltage	All digital inputs	VDDO = 3.3V	2.0	–	VDDO + 0.3V	V
			VDDO = 2.5V	1.75	–	VDDO + 0.3V	V
			VDDO = 1.8V	1.26	–	VDDO + 0.3V	V
			VDDO = 1.5V	1.05	–	VDDO + 0.3V	V
			VDDO = 1.2V	0.84	–	VDDO + 0.3V	V
VIL	Input Low Voltage	All digital inputs	VDDO = 3.3V	-0.3	–	0.8	V
			VDDO = 2.5V	-0.3	–	0.75	V
			VDDO = 1.8V	-0.3	–	0.54	V
			VDDO = 1.5V	-0.3	–	0.45	V
			VDDO = 1.2V	-0.3	–	0.36	V
VOH	High-level Output Voltage	All digital outputs	IOH = -4 mA	VDDO - 0.4V	–	–	V
VOL	Low-level Output Voltage	All digital outputs	IOL = 4 mA	–	–	0.4	V
I_{ILK}	Input Leakage Current	With internal pull-up/pull-down resistor	–	10	–	70	µA
		All others without resistor	–	–	–	10	µA
CIN	Input Capacitance	All pins	–	–	–	5	pF

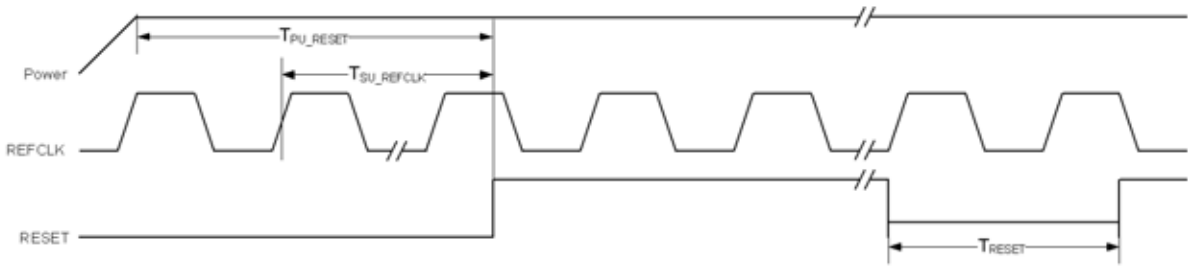
6.5.2 Reset Timing

Table 74: Reset Timing

(Over Full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{PU_RESET}	Valid Power to RESET De-asserted	–	10	–	–	ms
T_{SU_REFCLK}	Number of Valid REFCLK Cycles Prior to RESET De-asserted	–	10	–	–	clks
T_{RESET}	Minimum Reset Pulse Width During Normal Operation	–	10	–	–	ms

Figure 36: Reset Timing

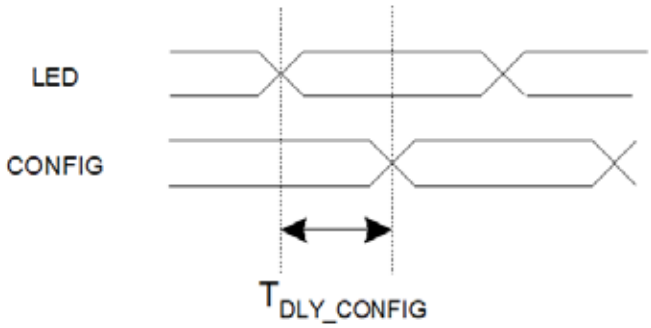


6.5.3 LED to CONFIG Timing

Table 75: LED to CONFIG Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{DLY_CONFIG}	LED to CONFIG Delay	–	0	–	25	ns

Figure 37: LED to CONFIG Timing



6.5.4 MDC/MDIO Management Interface Timing

Table 76: MDC/MDIO Management Interface Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
T_{DLY_MDIO}	MDC to MDIO (Output) Delay Time	2	–	16	ns
T_{SU_MDIO}	MDIO (Input) to MDC Setup Time	3	–	–	ns
T_{HD_MDIO}	MDIO (Input) to MDC Hold Time	3	–	–	ns
T_{P_MDC}	MDC Period	35	–	–	ns
T_{H_MDC}	MDC High	17	–	–	ns
T_{L_MDC}	MDC Low	17	–	–	ns
V_{HYST}	VDDO Input Hysteresis	–	360	–	mV
T_{P_MDC}	MDC Period	35	–	–	ns
T_{read_dly}	Read Delay	160	–	–	ns

Figure 38: MDC/MDIO Management Interface Timing

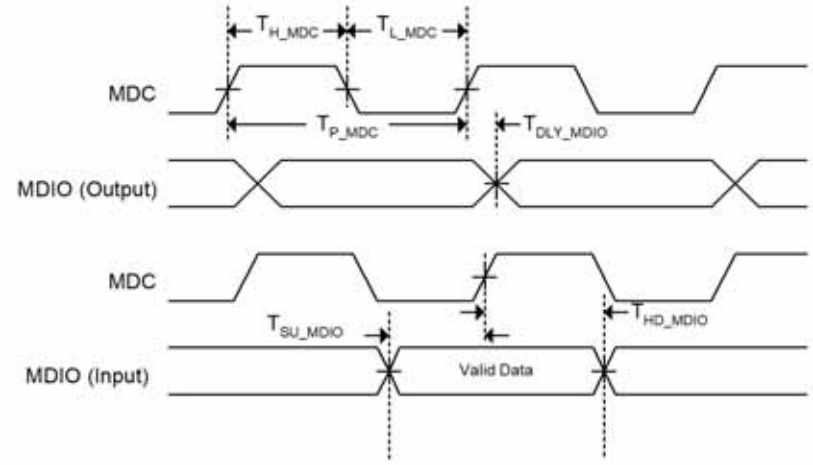


Figure 39: MDC/MDIO Input Hysteresis

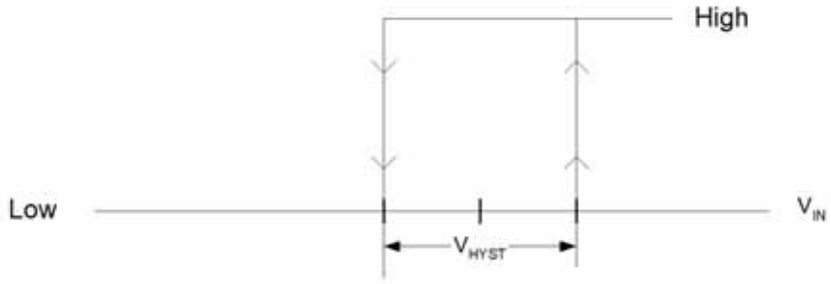
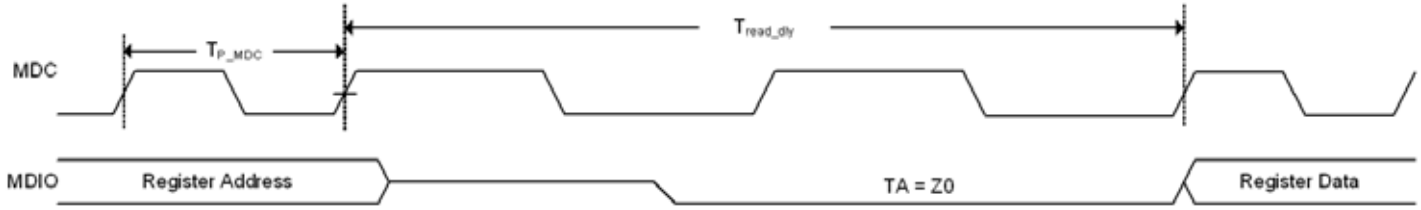


Figure 40: MDC Read Turnaround Delay



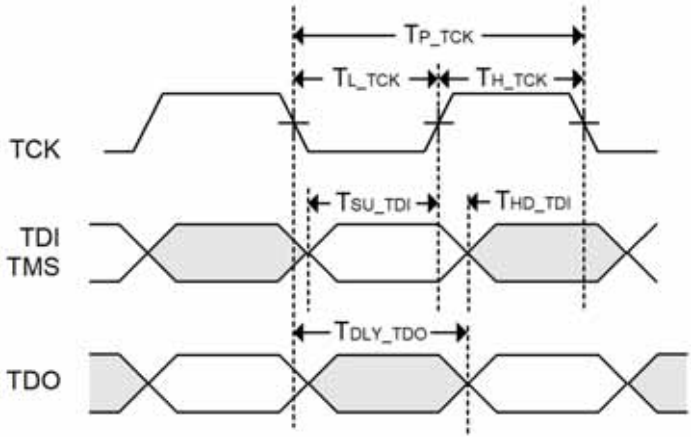
6.5.5 JTAG Timing

Table 77: JTAG Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{P_TCK}	TCK Period	–	60	–	–	ns
T_{H_TCK}	TCK High	–	12	–	–	ns
T_{L_TCK}	TCK Low	–	12	–	–	ns
T_{SU_TDI}	TDI, TMS to TCK Setup Time	–	10	–	–	ns
T_{HD_TDI}	TDI, TMS to TCK Hold Time	–	10	–	–	ns
T_{DLY_TDO}	TCK to TDO Delay	–	0	–	15	ns

Figure 41: JTAG Timing



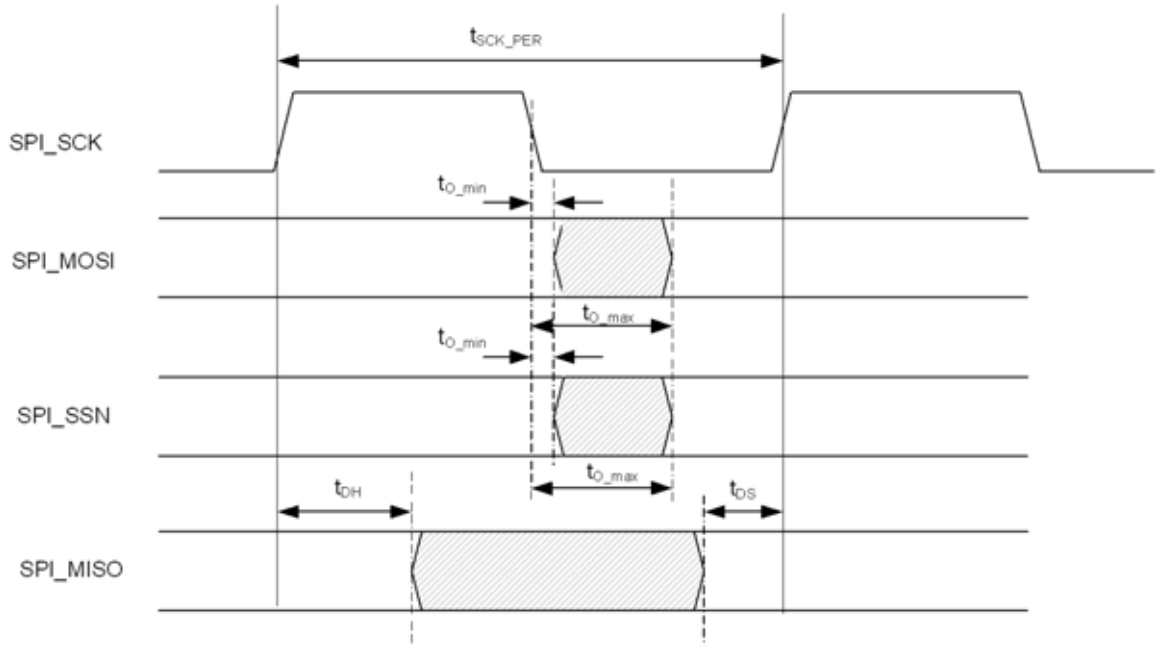
6.5.6 SPI Interface Timing

Table 78: SPI Interface Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{SCK_PER}	SCK Period	–	204.8	–	–	ns
–	SCK Duty Cycle	–	48	50	52	%
T_{O_min} to T_{O_max}	MOSI Valid from SCK Low	–	0	–	20	ns
T_{DH}	MISO Hold Time from SCK High	–	0	–	–	ns
T_{DS}	MISO Setup Time to SCK High	–	50	–	–	ns

Figure 42: SPI Interface Timing

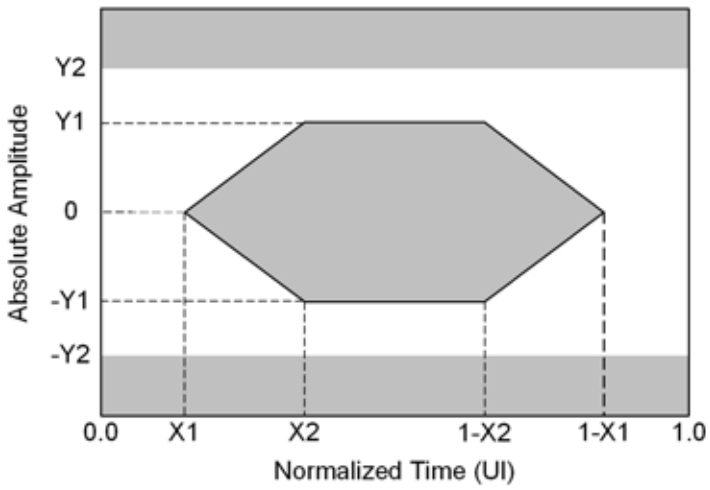


6.5.7 SGMII Electrical Summary

Table 79: SGMII Electrical Summary

Test Parameters	Specification			Units
	Transmitter Tests			
	Min	Mean	Max	
Output Voltage High	–	–	1525	mV
Output Voltage Low	875	–	–	mV
Output Ringing	–	–	10	%
Output Differential Voltage	150	–	400	mV
Output Offset Voltage	1.075	–	–	V
Single-ended Output Impedance	40	–	–	Ω
Output Current On Short to Gnd	–	–	40	mA
Output Current When P and N are Shorted	–	–	12	mA
Power Off Leakage Current	–	–	10	mA
Skew Between P and N	–	–	20	ps
Total Output Jitter	–	–	300	ps
Receiver Tests				
Sensitivity	–	–	100	mVpp
Single-ended Termination	–	50	–	Ω
Jitter Tolerance	500	–	–	ps

Figure 43: Transmitter Eye Mask



6.5.8 2500BASE-X Electrical Summary

Table 80: 2500BASE-X Electrical Summary

Test Parameters	Specification			Units
	Transmitter Tests			
	Min	Mean	Max	
Signaling Rate	-100 ppm	3.125	+100 ppm	GBaud
Nominal Unit Interval	–	320	–	ps
Differential Output	800	1000	1200	mVpp
Deterministic Jitter	–	–	0.17	UI
Random Jitter	–	–	0.27	UI
Total Output Jitter	–	–	0.35	UI
Receiver Tests				
Signaling Rate	-100 ppm	3.125	+100 ppm	GBaud
Nominal Unit Interval	–	320	–	ps
Differential Input Peak-to-Peak Amplitude	–	–	1600	mVpp
Applied Sinusoidal Jitter (Min. Peak-to-Peak)	0.17	–	–	UI
Applied Random Jitter (Min. Peak-to-Peak)	0.18	–	–	UI

6.5.9 5GBASE-R Electrical Summary

Table 81: 5GBASE-R Electrical Summary

Test Parameters	Specification			Units
	Transmitter Tests			
	Min	Mean	Max	
Signaling Rate	-100 ppm	5.15625	+100 ppm	GBaud
Nominal Unit Interval	–	193.9	–	ps
Differential Output	–	–	1200	mVpp
Deterministic Jitter	–	–	0.12	UI
Random Jitter	–	–	0.15	UI
Total Output Jitter	–	–	0.27	UI
Receiver Tests				
Signaling Rate	-100 ppm	5.15625	+100 ppm	GBaud
Nominal Unit Interval	–	193.9	–	ps
Applied Random Jitter (Min. Peak-to-Peak)	0.15	–	–	UI
	5 UI @ 0.02 MHz	–	–	N/A
	0.15 UI @ 4 MHz	–	–	
Applied Sinusoidal Jitter (Min. Peak-to-Peak)	0.15 UI @ 20 MHz	–	–	

6.5.10 10BASE-Te, 100BASE-TX, and 1000BASE-T Electrical Parameters

IEEE tests are typically based on template and cannot simply be specified by a number. For an exact description of the template and the test conditions, refer to the IEEE specifications.

- 10BASE-Te IEEE 802.3 Clause 14
- 100BASE-TX ANSI X3.263-1995
- 1000BASE-T IEEE Clause 40

Table 82: IEEE DC Transceiver Parameters

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
V_{ODIFF}	Absolute Peak Differential Output Voltage	MDIP/N[1:0]	10BASE-Te no cable	1.54	–	1.96	V
		MDIP/N[1:0]	10BASE-Te cable model	585[1]	–	–	mV
		MDIP/N[1:0]	100BASE-TX mode	0.950	–	1.050	V
		MDIP/N[3:0]	1000BASE-T[2]	0.67	–	0.82	V
	Overshoot[2]	MDIP/N[1:0]	100BASE-TX mode	0	–	5	%
	Amplitude Symmetry (Positive/ Negative)	MDIP/N[1:0]	100BASE-TX mode	98	–	102	V+/V-
V_{IDIFF}	Peak Differential Input Voltage	MDIP/N[1:0]	10BASE-Te mode	585[3]	–	–	mV
	Signal Detect Assertion	MDIP/N[1:0]	100BASE-TX mode	1000	460[4]	–	mV peak-peak
	Signal Detect De-assertion	MDIP/N[1:0]	100BASE-TX mode	200	360[5]	–	mV peak-peak

1. IEEE 802.3 Clause 14, Figure 14.9 shows the template for the far-end wave form. This template allows as little as 495 mV peak differential voltage at the far end receiver.
2. IEEE 802.3ab Figure 40 -19 points A&B.
3. The input test is actually a template test; IEEE 802.3 Clause 14, Figure 14.17 shows the template for the receive waveform.
4. The ANSI TP-PMD specification requires that any received signal with peak-to-peak differential amplitude greater than 1000 mV should turn on signal detect (internal signal in 100BASE-TX mode). The device accepts signals typically with 460 mV peak-to-peak differential amplitude.
5. The ANSI-PMD specification requires that any received signal with peak-to-peak differential amplitide less than 200 mV should de-assert signal detect (internal signal in 100BASE-TX mode). The device will reject signals typically with peak-to-peak differential amplitude less than 360 mV.

6.6 Reference Clock

6.6.1 CLKP/N Timing — 156.25 MHz

Table 83: CLKP/N Timing — 156.25 MHz

Symbol	Parameter	Condition	Min	Typ	Max	Units
Fclk	Frequency	–	-50 ppm	156.25	+50 ppm	MHz
tr, tf	Rise, Fall Time	20 to 80% of swing	0.3	0.5	0.8	ns
A	Amplitude	Differential pk	0.4	0.75	0.9	V
Tduty	Duty cycle	–	0.45	0.5	0.55	–
T_J	Jitter	Integrated from 1 to 30 MHz	–	–	0.5	ps, RMS
Zin	Input Impedance	Differential	90	100	110	Ω
SDD11	Input Return Loss	Differential, 100Ω	–	–	-12	db

Note CLKP/N must be AC coupled into the device.

Note When the transmitter or the receiver is in LPI transmit mode, or switching to and from the LPI mode, short-term rate of frequency variation will be less than 0.1 ppm/second.

6.6.2 CLKP/N Timing — 50 MHz

Table 84: CLKP/N Timing — 50 MHz

Symbol	Parameter	Condition	Min	Typ	Max	Units
Fclk	Frequency	–	-50 ppm	50	+50 ppm	MHz
tr, tf	Rise, Fall Time	20 to 80% of swing	0.3	0.5	0.8	ns
A	Amplitude	Differential pk-pk	0.4	0.75	0.9	V
Tduty	Duty cycle	–	0.45	0.5	0.55	–
T_J	Jitter	Integrated from 1 to 30 MHz	–	–	1.0	ps, rms
Zin	Input Impedance	Differential	90	100	110	Ω
SDD11	Input Return Loss	Differential, 100Ω	–	–	-12	dB

Note CLKP/N must be AC coupled into the device.

6.6.3 XTAL Timing[1]

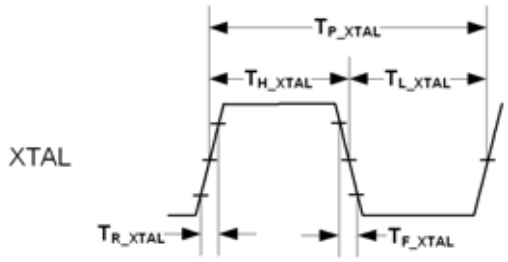
Table 85: XTAL Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{P_XTAL}	XTAL Period	–	20 -50 ppm	20	20 +50 ppm	ns
T_{H_XTAL}	XTAL High Time	–	6.5	10	13.5	ns
T_{L_XTAL}	XTAL Low Time	–	6.5	10	13.5	ns
T_{R_XTAL}	XTAL Rise	10 to 90%	–	2.0	–	ns
T_{F_XTAL}	XTAL Fall	90 to 10%	–	2.0	–	ns
T_{J_XTAL}	XTAL Total Jitter[2]	–	–	–	200	ps

1. If the crystal option is used, then ensure that the frequency is 50 MHz ±50 ppm. Capacitors must be chosen carefully: see the application note supplied by the crystal vendor.
2. PLL-generated clocks are not recommended as input to XTAL since they can have excessive jitter. Zero delay buffers are also not recommended for the same reason.

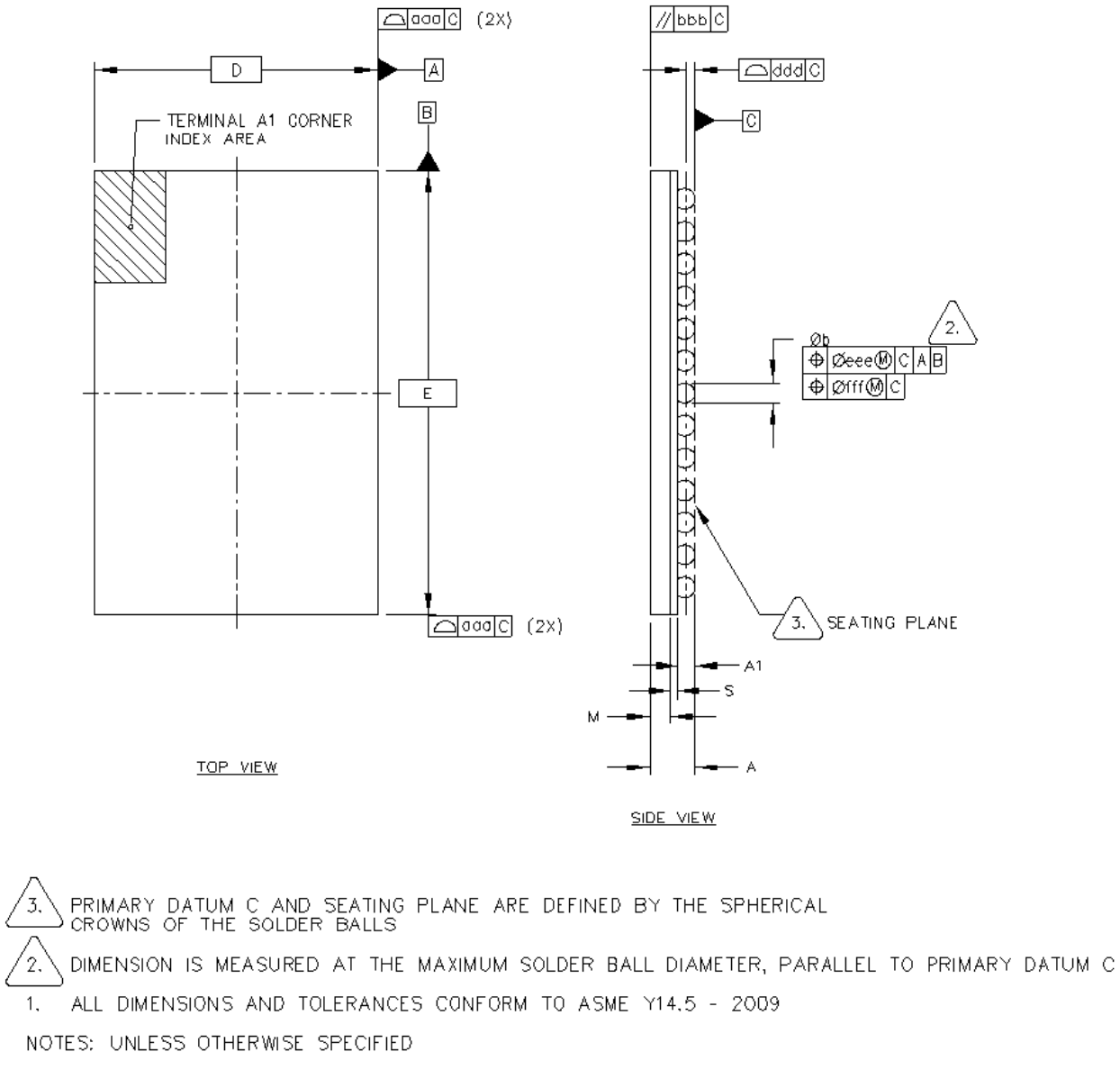
Figure 44: XTAL Timing



7 Mechanical Drawings

7.1 104-pin 7 mm x 11 mm FC-TBGA Package Mechanical Drawings of the 88E2110 Device

Figure 45: 104-pin 7 mm x 11 mm FC-TFBGA Top and Side View of the 88E2110 Device



3. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS

2. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5 - 2009

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 46: 104-pin 7 mm x 11 mm FC-TFBGA Bottom View of the 88E2110 Device

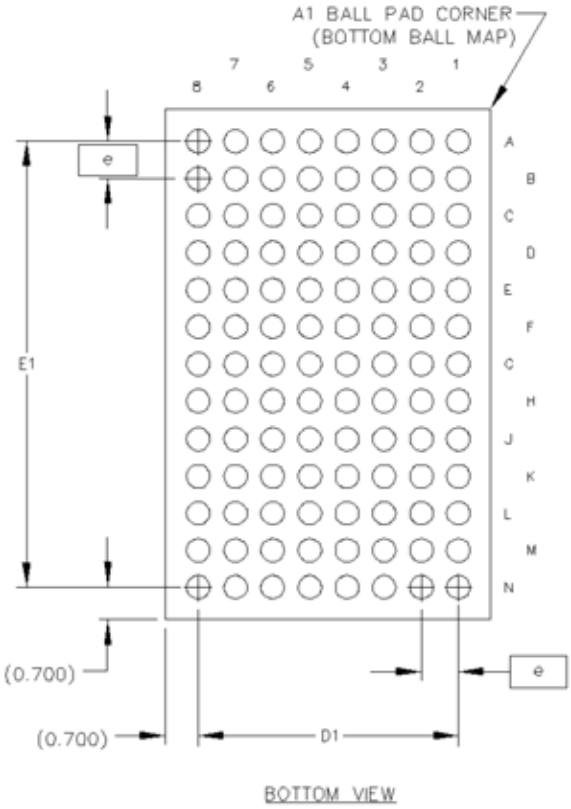


Table 86: 104-pin 7 mm x 11 mm FC-TBGA Package Dimensions of the 88E2110 Device

		SYMBOL	COMMON DIMENSIONS		
			MIN.	NOM.	MAX.
BODY SIZE	X	D	6.90	7.00	7.10
	Y	E	10.90	11.00	11.10
BALL PITCH		e	0.80 BASIC		
TOTAL THICKNESS		A	1.03	1.12	1.21
MOLD THICKNESS		M	0.48	0.53	0.58
SUBSTRATE THICKNESS		S	0.145	0.175	0.205
BALL DIAMETER			0.45	0.50	0.55
STAND OFF		A1	0.36	0.41	0.46
BALL WIDTH		b	0.42	0.52	0.62
PACKAGE EDGE TOLERANCE		aaa	0.10		
MOLD PARALLELISM		bbb	0.10		
COPLANARITY		ddd	0.15		
BALL OFFSET (PACKAGE)		eee	0.15		
BALL OFFSET (BALL)		fff	0.08		
BALL COUNT		n	104		
EDGE BALL CENTER TO CENTER	X	D1	5.60		
	Y	E1	9.60		

7.2 529-pin 19 mm x 19 mm HFCBGA Package Mechanical Drawings of the 88E2180 Device

Figure 47: 529-pin 19 mm x 19 mm HFCBGA Top and Side View of the 88E2180 Device

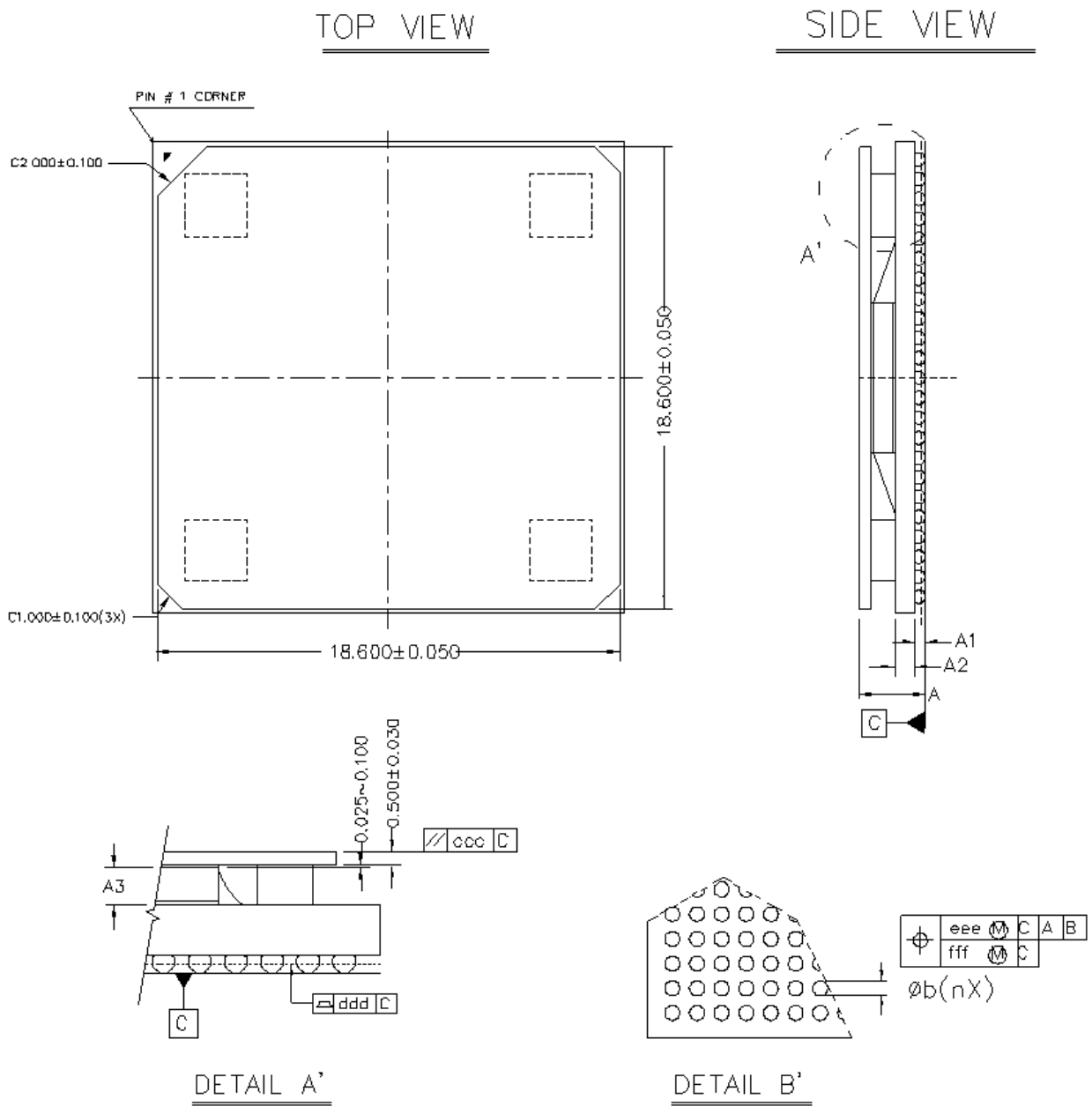


Figure 48: 529-pin 19 mm x 19 mm HFCBGA Bottom View of the 88E2180 Device

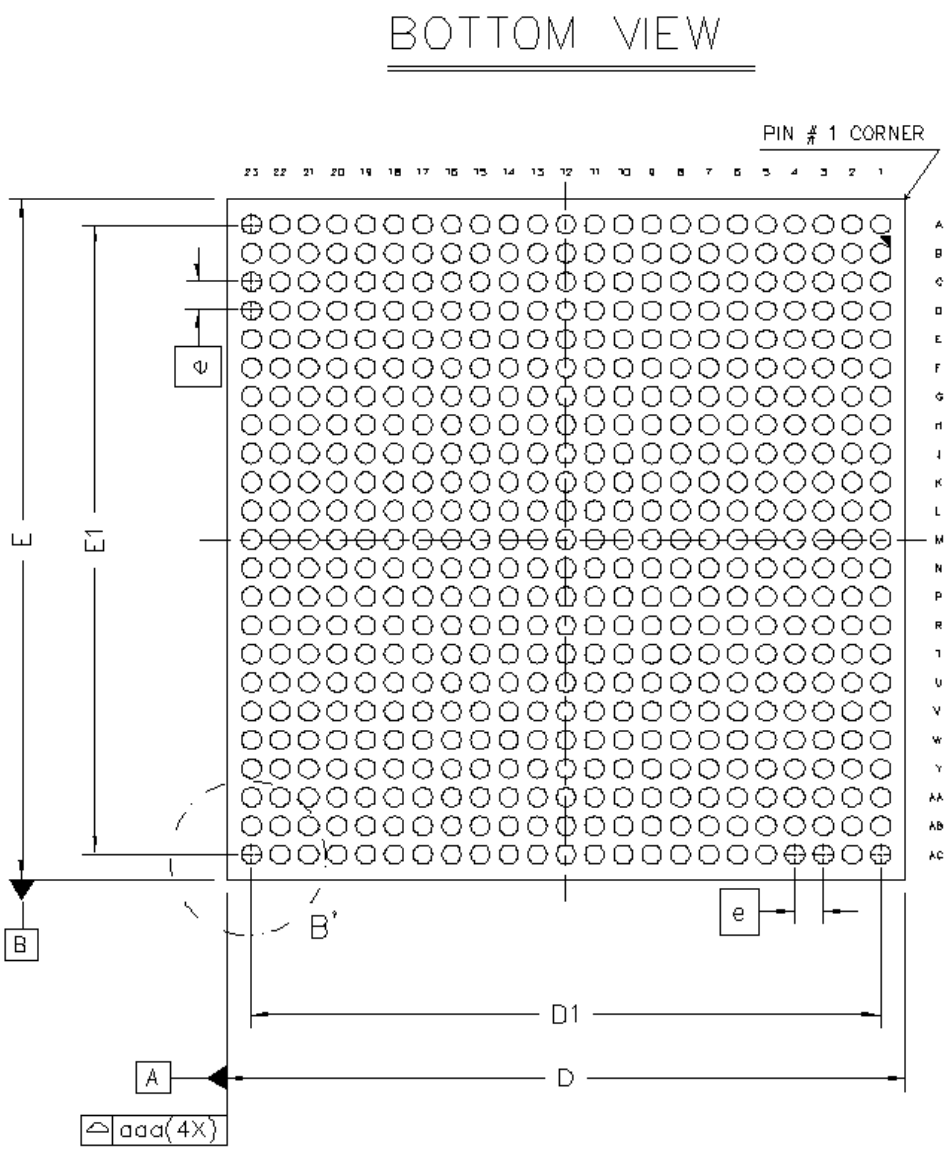


Table 87: 529-pin 19 mm x 19 mm HFCBGA Package Dimensions of the 88E2180 Device

	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOM.	MAX.
TOTAL THICKNESS	A	2.537	2.657	2.777
STAND OFF	A1	0.360	--	0.460
SUBSTRATE THICKNESS	A2	0.800 REF		
THICKNESS FROM SUBSTRATE SURFACE TO DIE BACKSIDE	A3	0.887 REF		
BODY SIZE	D	19.000 BSC		
	E	19.000 BSC		
BALL DIAMETER		0.500		
BALL WIDTH	b	0.440	--	0.640
BALL PITCH	e	0.800 BSC		
BALL COUNT	n	529		
EDGE BALL CENTER TO CENTER	D1	17.600 BSC		
	E1	17.600 BSC		
EXPOSE DIE SIZE	D2	--		
	E2	--		
PACKAGE EDGE TOLERANCE	aaa	0.100		
SUBSTRATE PARALLELISM	bbb	--		
TOP PARALLELISM	ccc	0.200		
COPLANARITY	ddd	0.150		
BALL OFFSET (PACKAGE)	eee	0.150		
BALL OFFSET (BALL)	fff	0.080		

8 Part Order Numbering/Package Marking

8.1 Part Order Numbering

Figure 49 shows the ordering part numbering scheme for the 88E2180 device and Figure 50 shows the ordering part numbering scheme for the 88E2110 device. Contact Marvell FAEs or sales representatives for complete ordering information.

Figure 49: Sample Part Number for 88E2180

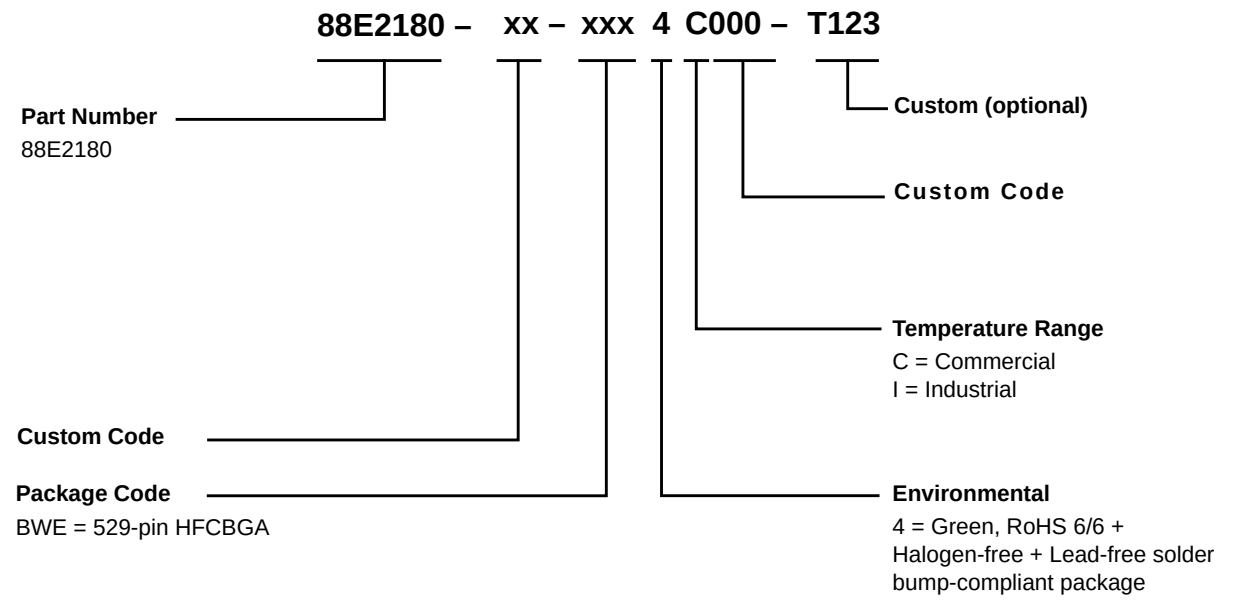


Figure 50: Sample Part Number for 88E2110

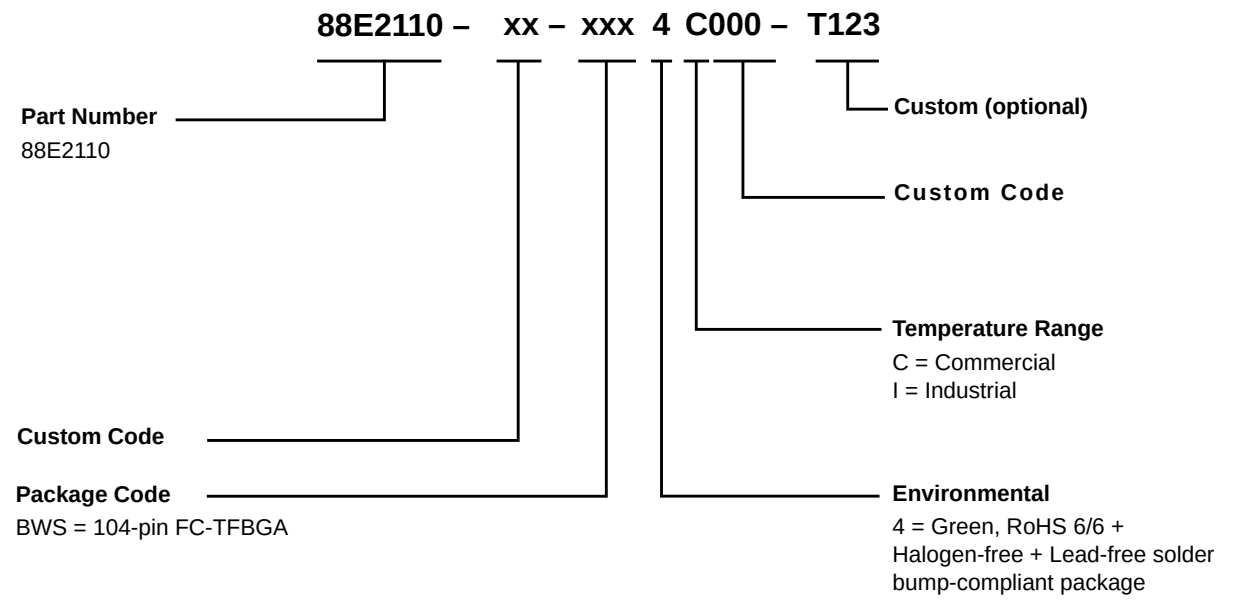


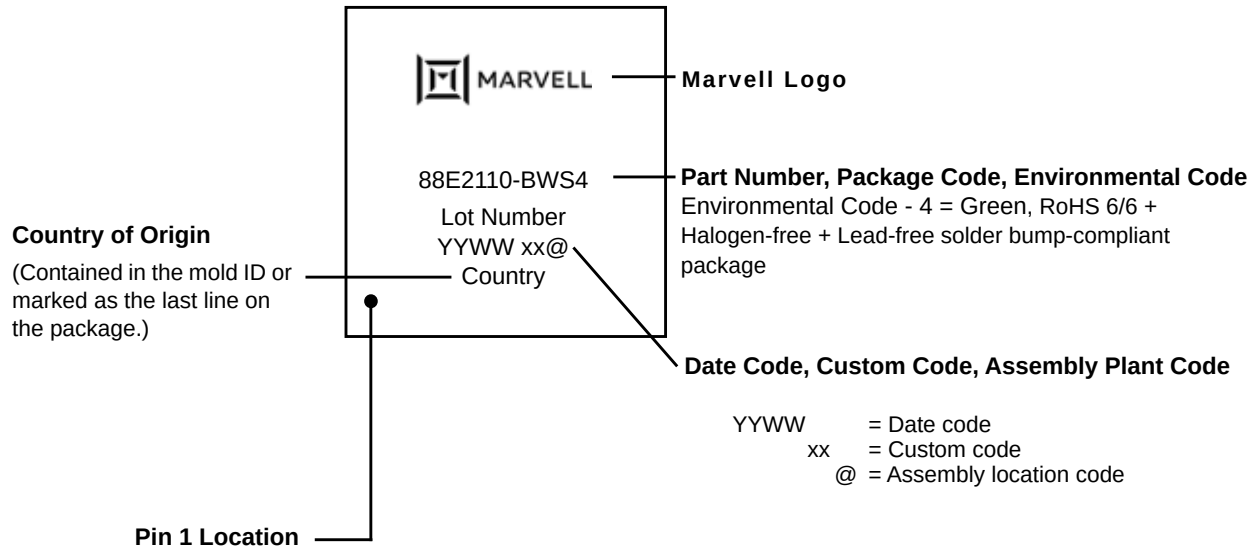
Table 88: 88E2180 and 88E2110 Commercial Part Order Options

Part Number	Package Type	Part Order Number
88E2180	529-pin 19 mm x 19 mm HFCBGA - Commercial, Green, RoHS 6/6 + Halogen-free + Lead-free solder bump-compliant	88E2180-XX-BWE4C000
88E2180	529-pin 19 mm x 19 mm HFCBGA - Industrial, Green, RoHS 6/6 + Halogen-free + Lead-free solder bump-compliant	88E2180-XX-BWE4I000
88E2110	104-pin 7 mm x 11 mm FC-TFBGA - Commercial, Green, RoHS 6/6 + Halogen-free + Lead-free solder bump-compliant	88E2110-XX-BWS4C000
88E2110	104-pin 7 mm x 11 mm FC-TFBGA - Industrial, Green, RoHS 6/6 + Halogen-free + Lead-free solder bump-compliant	88E2110-XX-BWS4I000

8.1.1 Package Marking

Figure 51 is an example of the package marking and pin 1 location for the 88E2110 package.

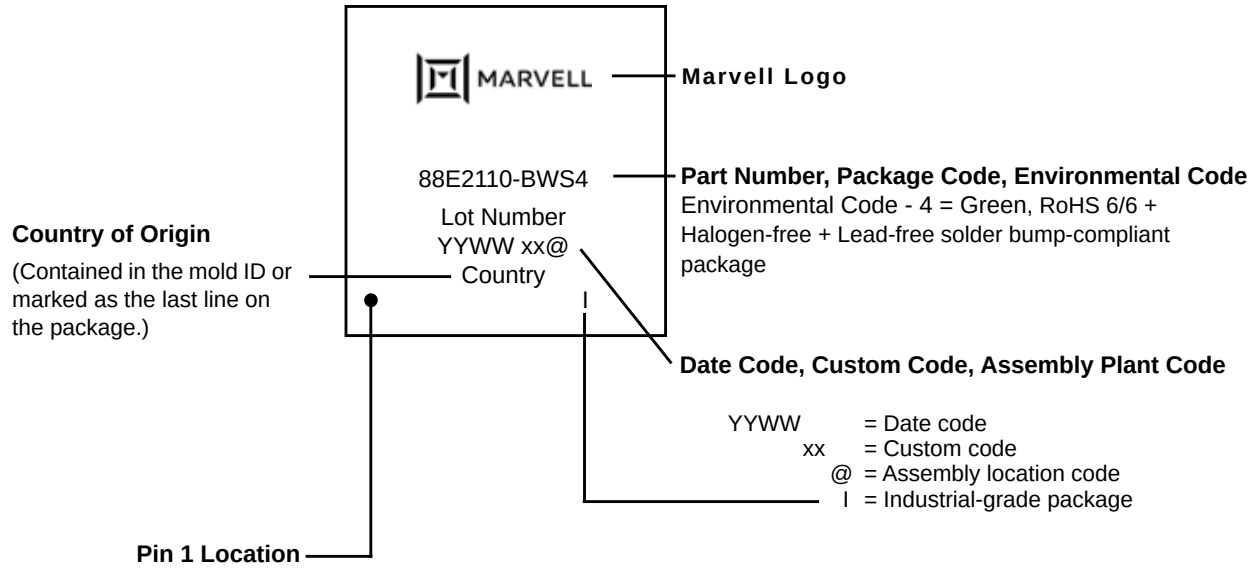
Figure 51: 88E2110 Commercial Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

Figure 52 is an example of the Industrial package marking and pin 1 location for the 88E2110 package.

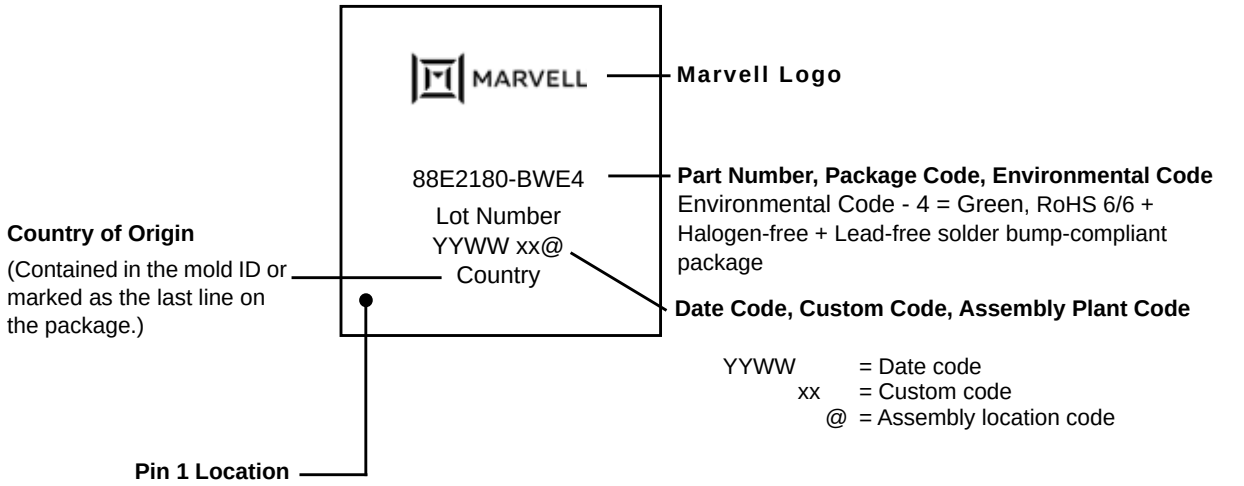
Figure 52: 88E2110 Industrial Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

Figure 53 is an example of the Commercial package marking and pin 1 location for the 88E2180 package.

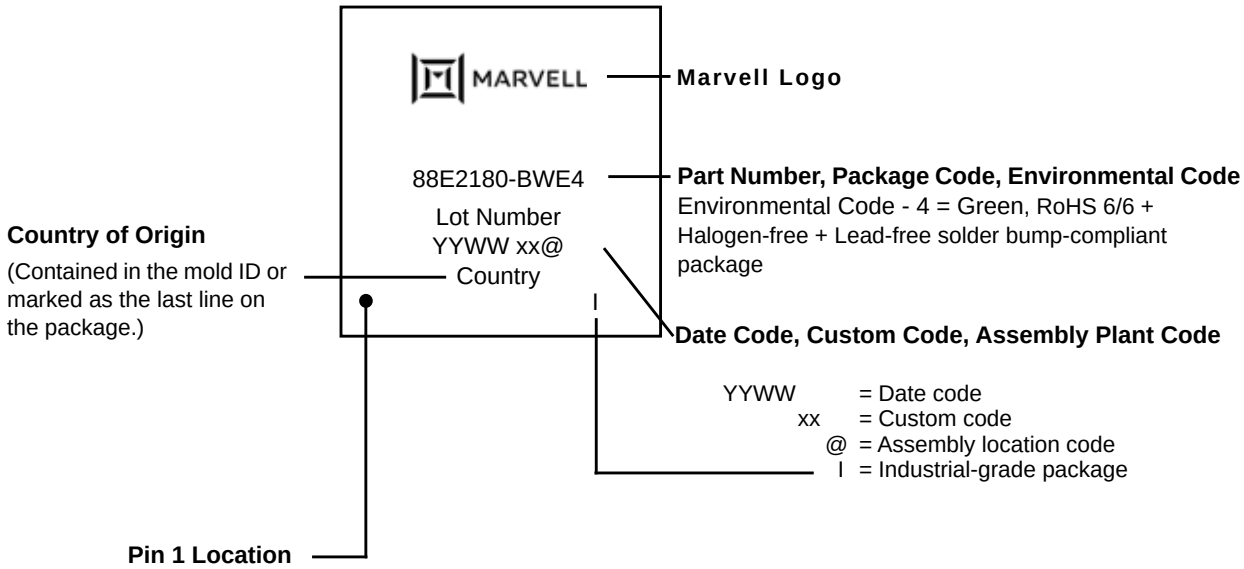
Figure 53: 88E2180 Commercial Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

Figure 54 is an example of the Industrial package marking and pin 1 location for the 88E2180 package.

Figure 54: 88E2180 Industrial Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

A Revision History

Table 89: Document Change History

Revision	Date	Section	Detail
Rev B	July 1, 2021	Section 7 "Mechanical Drawings"	• 7.1 "104-pin 7 mm x 11 mm FC-TBGA Package Mechanical Drawings of the 88E2110 Device" updated. • Figure 45, 104-pin 7 mm x 11 mm FC-TFBGA Top and Side View of the 88E2110 Device, on page 149 updated. • Figure 46, 104-pin 7 mm x 11 mm FC-TFBGA Bottom View of the 88E2110 Device, on page 150 updated. • Table 86, 104-pin 7 mm x 11 mm FC-TBGA Package Dimensions of the 88E2110 Device, on page 151 updated.
Rev A	September 10, 2020	**All applicable** • Disclaimer updated • Corporate rebranding and template update • New Marvell logos added to all figures with Marvell logo marking	
Rev –	November 8, 2018	Initial release.	
Rev – v0.02	November 8, 2018	Section 5 "Host Interface Unit (H Unit)"	• 5 "Host Interface Unit (H Unit)" updated.
Rev – v0.01	October 8, 2018	Initial draft review.	

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Doc. No. MV-S111723-U0 Rev. B Revised: July 1, 2021

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