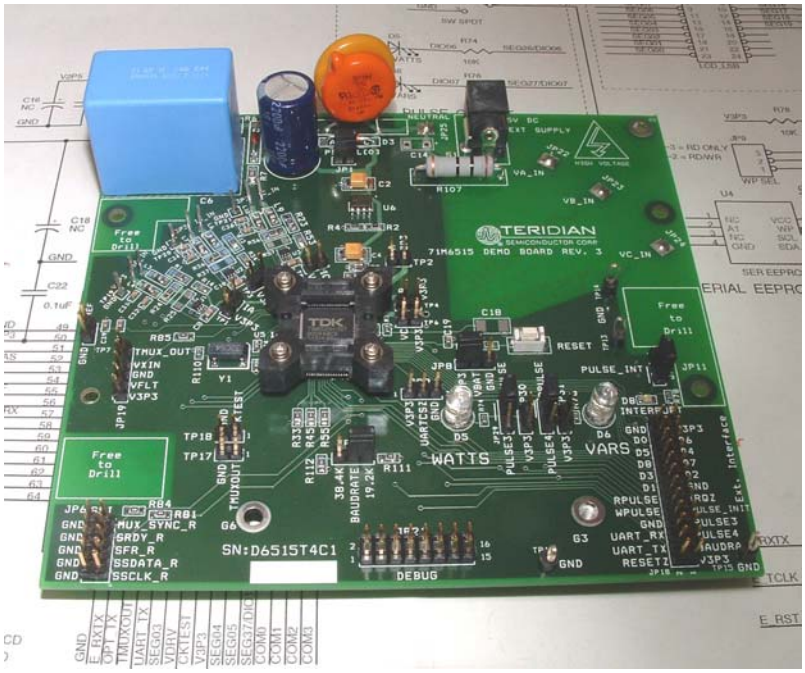
71M6515H Demo Board

USER'S MANUAL



12/5/2005 2:06 PM
Revision 2.0

TERIDIAN Semiconductor Corporation
6440 Oak Canyon Rd.
Irvine, CA 92618-5201
Phone: (714) 508-8800 ▪ Fax: (714) 508-8878
http://www.teridian.com/
meter.support@teridian.com

71M6515H

3-Phase Power Meter AFE IC
DEMO BOARD

USER'S MANUAL

Table of Contents

List of Figures

List of Tables

1

1 GETTING STARTED

1.1 GENERAL

The TERIDIAN Semiconductor Corporation (TSC) 71M6515H Demo Board is a demonstration board for evaluating the 71M6515H IC for 3-phase electronic power metering applications. It incorporates a 71M6515H integrated circuit, peripheral circuitry such an on-board power supply as well as a companion Debug Board that allows a connection to a PC running Windows® 2000/XP through a RS232 port. The demo board allows the evaluation of the 71M6515H power meter controller chip for measurement accuracy and overall system use.

A control program running on a Windows® 2000/XP compatible PC allows control and monitoring of the 71M6515H IC on an abstract level via a graphical user interface (GUI).

1.2 SAFETY AND ESD NOTES

Connecting live voltages to the demo board system will result in potentially hazardous voltages on the demo board.

EXTREME CAUTION SHOULD BE TAKEN WHEN HANDLING THE DEMO BOARD ONCE IT IS CONNECTED TO LIVE VOLTAGES!

THE DEMO SYSTEM IS ESD SENSITIVE! ESD PRECAUTIONS SHOULD BE TAKEN WHEN HANDLING THE DEMO BOARD!

1.3 DEMO KIT CONTENTS

- 71M6515H Demo board containing 71M6515H AFE IC
- Debug Board
- Two 5VDC/1,000mA universal wall transformer with 2.5mm plug (Switchcraft 712A compatible)
- Serial cable, DB9, Male/Female, 2m (Digi-Key AE1020-ND)
- CD-ROM containing documentation (data sheet, board schematics, BOM, layout), PC executable program (GUI), and calibration spreadsheet

Note: The media CD-ROM contains a file named readme.txt that specifies all files found on the media and their purpose.

1.4 COMPATIBILITY STATEMENT

This manual is compatible with REV1.1 (October 14, 2005) of the Control Program (GUI) and with 71M6515H code revision 1.1 (October 14, 2005).

1.5 SUGGESTED EQUIPMENT NOT INCLUDED

PC w/ MS-Windows® versions XT, ME, or 2000, equipped with RS232 port (COM port) via DB9 connector

1.6 DEMO BOARD TEST SETUP

Figure 1-1 shows the basic connections of the Demo Board plus Debug Board with the external equipment.

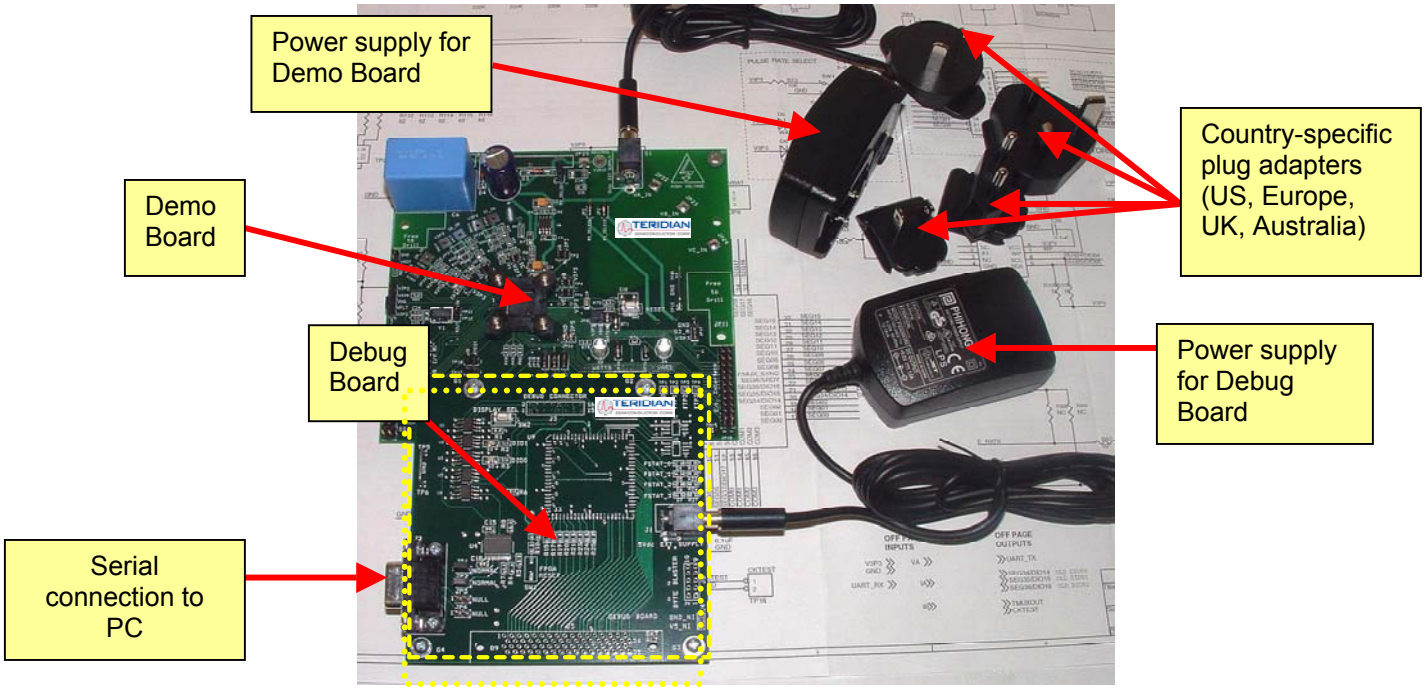


Figure 1-1: TERIDIAN 71M6515H Demo and Debug Boards: Basic Connections

The 71M6515H demo board system is shown in Figure 1-2. It consists of a stand-alone rectangular meter Demo Board and an optional Debug Board (most Debug Boards are partially assembled and have less components than shown in Figure 1-2). The Demo Board contains all circuits necessary for operation as a meter front end, calibration LEDs, and power supply. The Debug Board is optically isolated from the meter and interfaces to a PC through a 9 pin serial port. For serial communication between the PC and the TERIDIAN 71M6515H, the Debug Board needs to be plugged with its connector J3 into connector JP21 of the Demo Board.

Connections to the external signals to be measured, i.e. scaled AC voltages and current signals derived from shunt resistors or current transformers, are provided on the rear side of the demo board.

Note: It is recommended to set up the demo board with no live AC voltage connected, and to connect live AC voltages only after the user is familiar with the demo system.

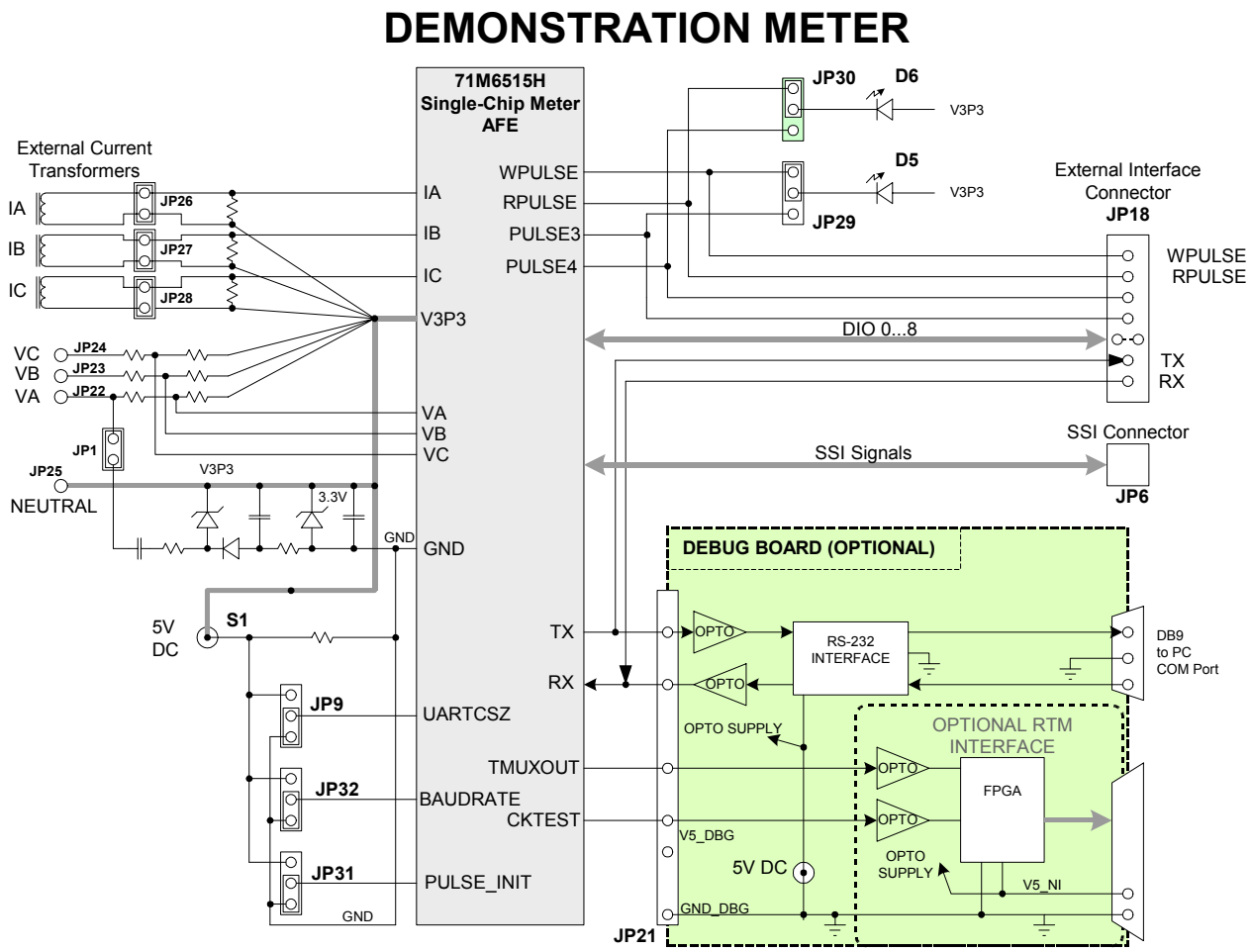


Figure 1-2: Block diagram for the TERIDIAN 71M6515H Demonstration Meter with Debug Board
Note: All input signals are referenced to the V3P3 (3.3V power supply to the chip).

1.6.1 POWER SUPPLY SETUP

There are several choices for meter power supply:

- Internal (using phase A of the AC line voltage). The internal power supply is only suitable when phase A exceeds 220V RMS.
- External 5VDC connector (J1) on the Demo Board and external 5VDC connector (J1) on the Debug Board.

The power supply jumper JP1 must be consistent with the power supply choice. JP1 disconnects phase A from the power supply. This jumper should usually be left in place.

The internal supply is not strong enough to power the Debug Board. Thus, the external power supply should always be used for the Debug Board, regardless whether the meter is powered by its internal supply or through an external supply.

1.6.2 SERIAL CONNECTION SETUP

For connection of the DB9 serial port to a PC, either a straight or a so-called "null-modem" cable may be used. JP1 and JP2 are plugged in for the straight cable, and JP3/JP4 are empty. The jumper configuration is reversed for the null-modem cable, as shown in Table 1-1.

Configuration	JP1	JP2	JP3	JP4
Straight Cable	installed	installed	--	--
Null-Modem Cable	--	--	installed	installed

Table 1-1: Jumper settings on Debug Board

JP1 through JP4 can also be used to alter the connection when the PC is not configured as a DCE device. Table 1-2 shows the connections necessary for the straight DB9 cable and the pin definitions.

PC Pin	Function	Demo Board Pin
2	TX	2
3	RX	3
5	Signal Ground	5

Table 1-2: Straight cable connections

Table 1-3 shows the connections necessary for the null-modem DB9 cable and the pin definitions.

PC Pin	Function	Demo Board Pin
2	TX	3
3	RX	2
5	Signal Ground	5

Table 1-3: Null-modem cable connections

1.7 PREPARING THE PC

The Control Program PMtest.exe must be copied from the CD-ROM to a directory on the host PC. The program can then be started directly by double-clicking on the PMTest.exe icon (see Figure 1-3).

PMTest.exe

Figure 1-3: Control Program Icon

PMTest.exe can work in two baud rates and on any COM port. To configure PMTest.exe for the desired operation mode, the original PMTest.exe file is copied to or renamed to a file with a name of the form:

PMTestxxxCy.exe

If xxx = 192, the program will operate at 19.2kb/s, if xxx = 384, the program will operate at 38.4kb/s (UART speed when communicating with the 71M6515H).

The number substituted for y states the COM port number that the program is using for communicating with the host.

Example: When named PMTest192C2.exe, the program will operate with 19.2kb/s via COM port 2.

Note: For smooth operation of the PMTest program it is important to observe the following rules:

- It is important to exit all programs that access COM port 1 before PMTEST.exe is started.
- Make sure all applicable updates to the Windows ® operating system are installed before running the application.
- **PMTest.exe will not run on Windows® 98 or older operating systems.**

Real-time performance can be affected by processor-intense operations of the PC, such as starting new applications, loading files into applications, or ending applications. Such operations have to be avoided to ensure uninterrupted communication between PC and the 6515H Demo Board.

Do not press the ALT key on the keyboard!

1.8 USING THE DEMO BOARD

The 71M6515H Demo Board is a ready-to-use meter with a preprogrammed scaling factor Kh of 3.2 Wh/pulse. In order to be used with a calibrated load or a meter calibration system, the board should be connected to the AC power source using the spade terminals on the bottom of the board. The current transformers should be connected to the dual-pin headers on the bottom of the board. For the Kh to be adjusted properly, current transformers with 2,000:1 winding ratio must be used.

1.8.1 STARTING UP THE DEMO BOARD AND THE GUI PROGRAM

In order to control and monitor the Demo Board, the connections specified in section 1.6 have to be established.

The sequence of actions when powering up the Demo Board is as follows:

1. Power up the Demo Board
2. Start the GUI Control Program PMTest.exe.
3. Check for communication between the GUI Control Program and the 71M6515H. Communication is established when the green "LED" indicator labeled 1SEC on the GUI screen flashes red every second.
4. Initialize the 71M6515H to match the desired application and measurement parameters. Establish the CE image, calibration factors, pulse parameters, nominal temperature, IMAX/VMAX using the commands and fields described in 1.8.2.
5. Establish the desired configuration using the bits of the *CONFIG* register (field 16 in the GUI window), but do not enable the CE.
6. Enable the CE by clicking the square button next to "CE_ENABLE".

Once, voltage is applied and load current is flowing, the red LED D5 will flash each time an energy sum of 3.2 Wh is collected.

Similarly, the red LED D6 will flash each time a reactive energy sum of 3.2 VARh is collected.

1.8.2 CONTROLLING THE DEMO BOARD

Upon starting the PMTEST.exe application, the graphical user interface (GUI) of the demo application shown in Figure 1-4 will be displayed on the screen. The gray boxes are the meter outputs and the white boxes contain host, i.e. user, inputs.

It is important to enable the computation engine (CE) in order to see activity in the GUI window. You can check the computation engine (CE) status by verifying the status of the button on the left of CE_ENABLE in the "Config" block of the GUI. It should display a "1", as shown in Figure 1-4. If not, the CE can be enabled by clicking the "0" button to the left of the "CE_ENABLE" text using the left mouse button. Upon clicking, the "0" will toggle to a "1", and the green and red indicator lights underneath the "Status/Mask" text will start blinking.

1.8.3 GUI WINDOW - OVERVIEW

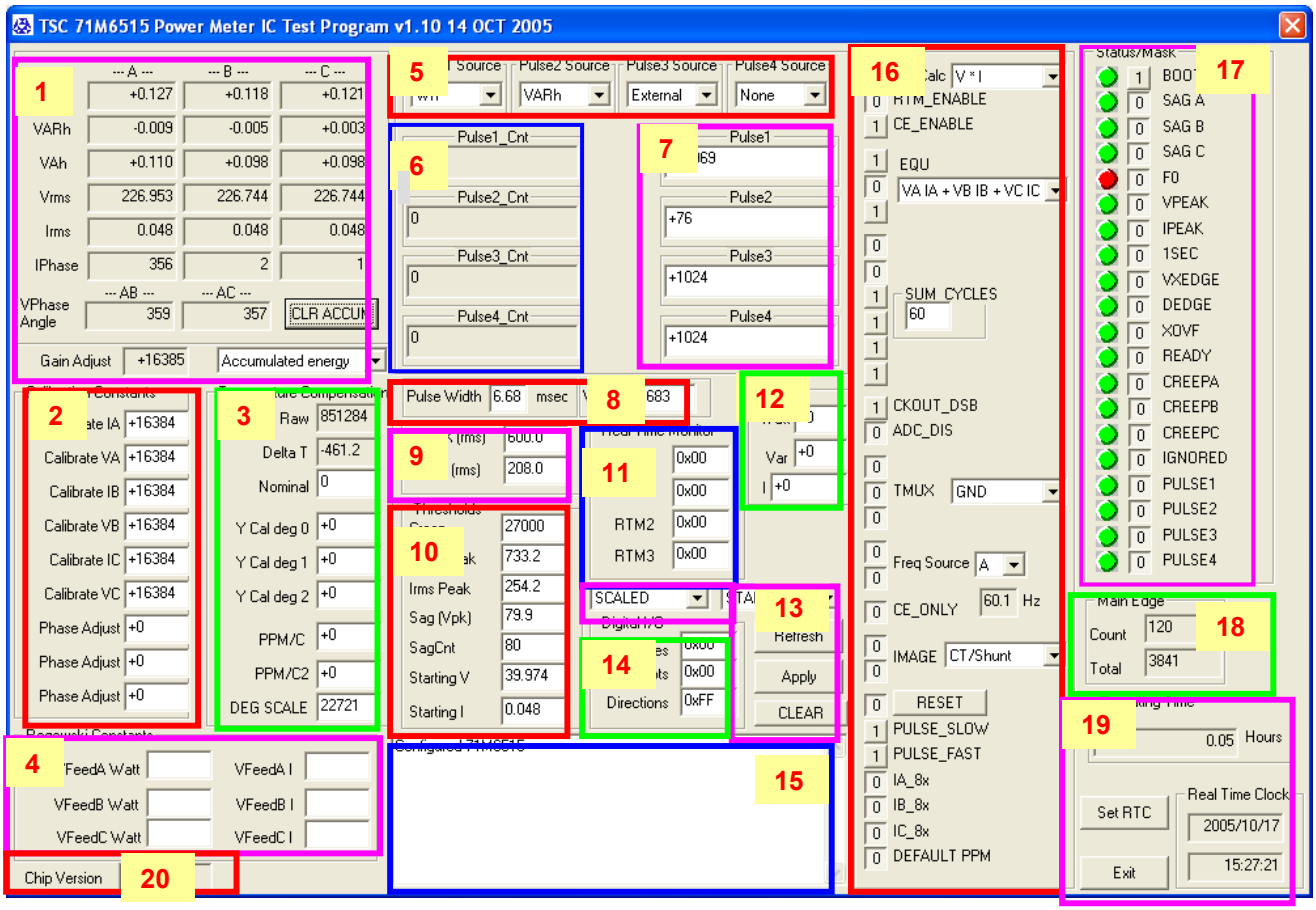


Figure 1-4: Host GUI Window w/ Functional Groups (Areas) Marked and Numbered

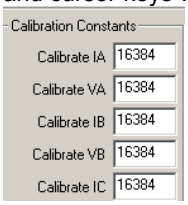
1.8.4 GUI WINDOW – DISPLAY AND CONTROL FIELDS

The PMTEST (GUI) window, as shown in Figure 1-4, contains a number of major blocks or areas (Pulse Source Select, Config, Status/Mask, Calibration Constants, Temperature Compensation, Real-Time Monitor, Digital I/O, Thresholds and Operating Time). These major blocks (labeled 1 through 12 in Figure 1-4) group the functionally related buttons and fields together. The elements of the GUI are as follows:

- **Rectangular buttons:** Buttons that can be clicked by the user to initiate an action.

- **Square buttons**: Buttons that can be clicked by the user to initiate an action. The square buttons have a single digit showing the current state of the signal. A "1" is on and a "0" is off.

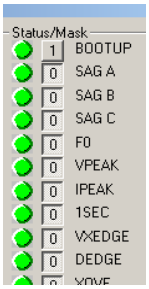
- **Entry fields**: White rectangular fields that can be edited by the user. The delete key plus the number and cursor keys work in this type of field.



- **Display fields**: Gray rectangular fields that indicate settings, measurements etc. of the 6515H chip. These fields cannot be edited by the user.

- **List fields**: Entry fields that allow selection from the pre-determined list of choices once the down-pointing arrow is pressed ("pull-down" menus).

- **Indicator lights**: Red and green activity indicators underneath the "Status/Mask" label.



Green lights mean no activity. Red lights mean that the corresponding bit in the *STATUS* mask is set, i.e. the condition is true.
With an input signal (phase A, B, C voltage) present, the F0 light will be on indicating that the square wave following the input signal is being generated. The light at "1SEC" will blink red every second. Other lights will stay green until the corresponding condition is true, e.g. when the input signal meets a sag or over-voltage threshold.

A summary of all of the GUI window areas follows on the next pages.

1.8.5 GUI WINDOW CONTROL AND DISPLAY FIELDS – DETAILED DESCRIPTION

Energy, Voltage/Current and Phase Area (1):

This area is in the upper left corner of the GUI window and contains a number of display fields arranged in columns. Phase A is the left column, phase B is the center column and phase C is the right column.

Next to the display fields in this area, there are a list field and a rectangular button controlling basic functions of the Energy, Voltage/Current and Phase Area:

GUI Element (Label)	Element Type	Function
Accumulated energy, Instantaneous energy	List field	This control toggles the display of the Wh, VARh and VAh fields from total accumulated energy to instantaneous energy, i.e. energy per accumulation interval
CLR ACCUM	Rectangular button	Resets the accumulators for Wh, VARh and VAh to zero. It also resets the "Main Edge" counters in the Status/Mask area and the pulse counters.

The function of the display fields depends on the selected mode, accumulated or instantaneous energy:

GUI Element (Label)	Function – Accumulated Energy Selected	Function – Instantaneous Energy Selected
Wh	These fields display the accumulated energy (real power x time) for each phase.	These fields display the energy (real power x time) collected during the last accumulation interval for each phase.
VARh	These fields display the accumulated reactive energy (reactive power x time) for each phase.	These fields display the reactive energy (reactive power x time) for each phase.
VAh	These fields display the accumulated apparent energy (apparent power x time) for each phase.	These fields display the accumulated apparent energy (apparent power x time) collected during the last accumulation interval for each phase.
Vrms	These fields display the momentary voltages (RMS) for each phase.	
Irms	These fields display the momentary currents (RMS) for each phase.	
Iphase	These fields display the momentary phase angles of the currents for each phase.	
VPhase angle	These fields display the momentary phase angles between the phases A and B (underneath "--- AB ---") and B and C (underneath "---BC---").	
Gain Adjust	This field displays the current value of the gain adjusted by the temperature compensation mechanism. It is functionally associated with the fields in area 10. When no compensation is active, or the temperature deviation is minimal, the default value of 16384 will be displayed.	

Calibration Constants Area (2):

This area is on the left side of the GUI window and contains three entry fields for each phase. The function depends on the selected CE image (CT/Shunt or Rogowski sensor):

GUI Element (Label)	Function (CT/Shunt)	Function (Rogowski Sensor)
Calibrate IA	Calibration constant for phase A current (default = 16384)	
Calibrate VA	Calibration constant for phase A voltage (default = 16384)	
Calibrate IB	Calibration constant for phase B current (default = 16384)	
Calibrate VB	Calibration constant for phase B voltage (default = 16384)	
Calibrate IC	Calibration constant for phase C current (default = 16384)	
Calibrate VC	Calibration constant for phase C voltage (default = 16384)	
Phase Adjust A	Calibration constant for phase A current angle (default = 0)	Calibration constant for phase A current angle (default = -3973)
Phase Adjust B	Calibration constant for phase B current angle (default = 0)	Calibration constant for phase B current angle (default = -3973)
Phase Adjust C	Calibration constant for phase C current angle (default = 0)	Calibration constant for phase C current angle (default = -3973)

During calibration (see section 2.1), the values of the calibration coefficients obtained with the calibration formulae should be entered in these fields.

Temperature Compensation Area (3):

This area consists of a vertical column of entry and display fields to the right of the Calibration Constants area. The Gain Adjust field from area 1 functionally belongs in the Temperature Compensation area.

GUI Element (Label)	Element Type	Default	Function
Raw	Display field	--	Raw temperature (chip substrate temperature)
Delta T	Display field	--	Difference between raw and nominal (calibration) temperature
Nominal	Entry field	0	The raw temperature should be entered here during calibration
Y Cal deg 0	Entry field	0	The constant correction coefficient for the RTC can be entered here if RTC compensation is required.
Y Cal deg 1	Entry field	0	The linear correction coefficient for the RTC can be entered here if RTC compensation is required.
Y Cal deg 2	Entry field	0	The quadratic correction coefficient for the RTC can be entered here if RTC compensation is required.
PPM/C	Entry field	0	The linear compensation coefficient of gain over temperature is entered here automatically as soon as a temperature value is entered in the "Nominal" field. **Values determined by the host may be entered here if the DEFAULT PPM bit in the Configuration area is set to 0.**
PPM/C2	Entry field	0	The quadratic compensation coefficient of gain over temperature is entered here. See the PPM/C field for details.
DEG SCALE	Entry field	22721	Scaling factor for the calculation of temperature. The default value for DEG SCALE (22721) should not be changed. $TEMP\_X = DEGSCALE * 2^{-22} * (TEMP\_RAW - TEMP\_NOM)$

Rogowski Calibration Area (4):

This area consists of two vertical columns of entry fields in the lower left side of the window. The coefficients are only active when the Rogowski image is selected for the CE.

GUI Element (Label)	Default	Function
VFeedA Watt	0	Calibration coefficient for phase A voltage feed through (default = 0)
VFeedB Watt	0	Calibration coefficient for phase B voltage feed through (default = 0)
VFeedC Watt	0	Calibration coefficient for phase C voltage feed through (default = 0)
VFeed A I	0	Not implemented
VFeed B I	0	Not implemented
VFeed C I	0	Not implemented

Pulse Source Selection Area (5):

This area consists of four list fields to the right of the Energy, Voltage/Current and Phase area. The entries determine the configuration and settings of the two pulse outputs used for four-quadrant metering.

GUI Element (Label)	Default	Function
Pulse1 Source	Wh	This list field allows selection of internal, external, or one of 35 post-processed parameters as the source for the PULSEW output.
Pulse2 Source	VARh	This list field allows selection of internal, external, or one of 35 post-processed parameters as the source for the PULSER output.
Pulse3 Source	Wh	This list field allows selection of either an external (host) input or one of 35 post-processed parameters as the source for the PULSE3 output. The selection "none" is also available. **When "none" is selected, the pulse output is disabled.**
Pulse4 Source	VARh	This list field allows selection of either an external (host) input or one of 35 post-processed parameters as the source for the PULSE4 output. The selection "none" is also available. **When "none" is selected, the pulse output is disabled.**

When external source is selected for any pulse generator, the missing pulse flags (PULSE1, PULSE2, PULSE3, PULSE4) will be active for each accumulation interval for which the host does not provide an input.

Pulse Count Area (6):

This area consists of a vertical column of display fields underneath the Pulse Source area.

GUI Element (Label)	Default	Function
PULSE1_Cnt	0	This field displays the count of pulses generated on the PULSEW output.
PULSE2_Cnt	0	This field displays the count of pulses generated on the PULSER output.
PULSE3_Cnt	0	This field displays the count of pulses generated on the PULSE3 output.
PULSE4_Cnt	0	This field displays the pulse count of pulses generated on the PULSE4.

Pressing the CLR ACCUM button in area 1 will reset the pulse counts to zero.

External Pulse Control Area (7):

This area consists of a vertical column of combined display/entry fields to the right of the Pulse Count area.

A field can be made and entry field by selecting "**External**" for the corresponding pulse source in the Pulse Source Selection area. In all other selections the fields are display fields.

When the corresponding Pulse Source selection in the Pulse Source Selection area is "**External**", values can be entered in the External Pulse Control fields to simulate pulse control by the host.

A new value must be entered in each new accumulation interval. The displayed values return to zero as soon as the next accumulation interval starts and no new values are supplied by the host. If no values are supplied by the host, the associated flags in the STATUS register (see STATUS/MASK area) will be set.

If very large numbers are entered, the pulses may be generated over several accumulation intervals.

When the corresponding Pulse Source selection in the Pulse Source Selection area is "**Internal**" or post-processed values, the display fields of the External Pulse Control area contain input values N that correspond to the pulse rate "f" per the equation:

$$f = WRATE * X * N * 35.82*10^{-12}$$

In other words, the ADC count corresponding to the applied voltages at the Vn and In pins (VA/IA, VB/IB, VC/IC) will be displayed.

GUI Element (Label)	Default	Function
Pulse1	0	Host-provided pulse count for the PULSEW output.
Pulse2	0	Host-provided pulse count for the PULSER output.
Pulse3	0	Host-provided pulse count for the PULSE3 output.
Pulse4	0	Host-provided pulse count for the PULS4W output.

Pulse Width and Pulse Rate Control Area (8):

This area consists of two entry fields to the right of the Temperature Compensation area.

GUI Element (Label)	Default	Function
WRATE	683	This field, together with SUM_CYCLES, $VMAX$, $IMAX$ and $In8$ determines the Kh factor of the chip as follows: $Kh = \frac{VMAX\ IMAX\ In8}{SUM\_CYCLES\ WRATE\ X} 1.5757 \quad Wh/Pulse$ X is determined by the two fields PULSE_SLOW and PULSE_FAST in the Configuration area.
Pulse Width	6.68ms	This field determines the pulse width in ms.

System Constants Area (9):

This area consists of two entry fields to the right of the Temperature Compensation area. Entries in these fields determine the system parameters of the Demo Board.

GUI Element (Label)	Default	Function
IMAX	208A	*IMAX* is the RMS meter current that results in 250mV peak signal at the ADC input. This variable reflects the scaling implemented by the voltage sensing resistors of the Demo Board. Note: When using shunt resistors as current sensors, *IMAX* must be calculated as (V_{ppmax} = 250mV): $IMAX = \frac{V_{pp\max}}{R_{sh} \cdot \sqrt{2}}$
VMAX	600V	*VMAX* is the RMS meter voltage that results in 250mV peak signal at the ADC input. This variable reflects the design of the current sensing circuitry of the Demo Board, assuming a 2000:1 current transformer.

Warning Thresholds Area (10):

This area consists of seven entry fields to the right of the Temperature Compensation area.

GUI Element (Label)	Default	Function
Creep	27000	Determines the creep threshold. For each phase, if *WSUM_X* and *VARSUM_X* of that phase are less than the value in the CREEP field, the contents of I^2h, Wh, and VARh for that phase will be set to zero for the whole accumulation interval. If all phases are below the creep threshold, the *CREEP* bit in the status word is set. The default value is 6000.
Vrms Peak	733.2	Threshold for over-voltage alarms, measured in Vrms.
Irms Peak	254.2	Threshold for over-current alarms, measured in Arms.
Sag (Vpk)	79.9	Determines the voltage sag threshold. The peak voltage must exceed the voltage entered in this field at least once each *SAG_CNT* samples in order to prevent a sag warning. Values can be entered directly in Volts. The GUI will round the entered value to the next possible value that can be represented with the resolution used for this parameter.
SagCnt	80	Determines the sag alarm setting. Sag must persist *SAG_CNT**397µs before the sag alarm is generated. Allowed range is 1 to (2^{15}-1). Default is 80 (31.7ms).
Starting V	39.974	Determines the voltage below which the calculation of frequency, zero crossings and voltage phase is suppressed.
Starting I	0.048	Determines the current below which the calculation of current-related values is suppressed.

Real-Time Monitor Area (11):

This area consists of four entry fields to the right of the System Constants area. The entries determine any four CE data memory locations to be monitored. The RTM_ENABLE square button in the Configuration area has to be in the "1" position for the RTM to be active.

GUI Element (Label)	Default	Function
RTM0	0x00	First CE data memory location to be monitored.
RTM1	0x00	Second CE data memory location to be monitored.
RTM2	0x00	Third CE data memory location to be monitored.
RTM3	0x00	Fourth CE data memory location to be monitored.

Note: Using the RTM interface requires special external hardware. Contact TERIDIAN for details.

QUANT Area (12):

This area consists of three entry fields that can be used to eliminate non-linearity at low currents caused by truncation noise. The parameters entered here are closely related to the calibration parameters.

GUI Element (Label)	Default	Function
Watt	0	Noise compensation factor for the Watt calculation
VAR	0	Noise compensation factor for the VAR calculation
I	0	Noise compensation factor for the current calculation

Multi-Purpose Area (13):

This area consists of two list fields and three rectangular buttons.

GUI Element (Label)	Element Type	Function
SCALED/RAW	List field	This list field toggles the display of display and entry fields between scaled (displayed values scaled using IMAX and VMAX) and raw data (raw counts from 6515H) mode. In scaled mode, values for voltage, current, and energy will be displayed as V, A, Wh, VARh etc. In raw mode, the values will appear in the internal format of the 71M6515H chip.
STANDARD/ HEX	List field	This list field toggles the values shown in display and entry fields between standard (decimal) and hexadecimal mode.
Refresh	Rectangular button	Pressing this button forces the GUI to transmit any changes made in entry or list fields to the 71M6515H chip.
Apply	Rectangular button	Placing the cursor into another entry field will have the same effect as the Refresh button. Pressing this button will apply a change made in an entry field.
CLEAR	Rectangular button	Pressing this button will clear the contents of the Status Window.

Digital I/O Area (14):

This area consists of three entry fields below the Real-Time Monitor area. The entries determine the configuration and settings of the eight DIO pins (D0 to D7).

GUI Element (Label)	Default	Function
Values	0x00	The hexadecimal number entered here defines the pattern that is applied to the I/O pins.
Interrupts	0x00	The hexadecimal pattern entered in this field determines whether a DEDGE interrupt is generated upon a bit changing its status. A 1 means that the corresponding DIO pin generates an interrupt. **DEDGE interrupts are only generated for DIO pins that are configured as inputs.**
Direction	0xFF	The hexadecimal number entered here defines whether I/O pins are inputs (0) or outputs (1).

A signal transition on an input pin will generate a DEDGE interrupt only once. This interrupt will not be synchronized with the accumulation interval or the 1-sec interrupt. Several transitions per accumulation interval are possible.

With every signal transition on a DIO pin, the message "Some Dn pin values have changed!" will be displayed in the Status Window.

Status Window Area (15):

This is the white, rectangular window at the bottom center of the GUI display. Activities of the PMtest.exe GUI Control program, error messages etc. are listed here.

If more events occur than can be displayed in the lines of this window, the display will scroll. Events and messages that occurred in the past will then be displayed by scrolling the window using the scroll arrows to the right of it.

When the rectangular CLEAR button above the Status Window is pressed, the messages displayed in the Status Window are deleted.

Configuration Area (16):

This area labeled "Config" consists of several square buttons, entry fields and list fields located in a column to the left of the Status/Mask area. Combinations of square buttons are mirrored as list fields. This means the same function can be controlled by either pressing the square buttons or by selecting a setting from the corresponding list field.

GUI Element (Label)	Element Type	Default	Function
VA	Square button and List field	0	Selects the method for calculating VAh. If 0 is selected, the VAh is computed from V_{RMS}*I_{RMS}, if 1 is selected, VAh is computed as the square root of Wh^2 + $VARh^2$
RTM_ENABLE	Square button	0	Enables/disables the Real-Time Monitor. CE_ENABLE must be "1".
CE_ENABLE	Square button	0	Enables/disables the CE.
EQU	3 Square buttons and Entry field	101 (5)	The equation to be used by the CE can be selected with the three buttons as a binary word.
SUM_CYCLES	6 Square buttons and Entry field	111100 (60)	The value for SUM_CYCLES can be selected with the six buttons as a binary word. The length of an accumulation cycle is t = SUM_CYCLES * 16.66ms. SUM_CYCLES should be > 15, unless VA = 0 or CE_ONLY = 1.
CKOUT_DSB	Square button	1	Disables the CKOUT pin of the target chip when set to "1".
ADC_DIS	Square button	0	The ADC in the 6515H can be disabled by selecting "1" with this button. This setting can be used for saving power on the target chip.
TMUX	3 Square buttons and List field	0 (GND)	The value for TMUX determines the source selected for the TMUX output pin on the 71M6515H. The value can be selected with the three buttons.
Freq Source	2 Square buttons and Entry field	0/0 (A)	The phase to be used for measuring the signal frequency can be selected with the two buttons as a binary word.
Hz	Display field	--	The measured frequency of the phase determined by the "Freq Source" field is displayed here.
CE_ONLY	Square button	0	The CE only operation mode can be selected by setting this square button to "1". Omits internal calculation of IPHASE, IRMS, VAH, and VRMS. This feature permits smaller accumulation intervals (SUM_CYCLES < 15).
IMAGE	6 Square buttons and Entry field	00 (CT, shunt)	The CE mode to be used (standard or Rogowski) can be selected with the two buttons as a binary word. IMAGE cannot be selected while the CE is running. To change the setting, follow this sequence: 1) Disable the CE. 2) Reset the 6515H. 3) Select the new image. 4) Enable the CE.
RESET	Square button and Rectangular button	0	The 6515H chip can be reset by selecting "1" with this button.

GUI Element (Label)	Element Type	Default	Function
PULSE_SLOW	Square button	1	This button, in conjunction with PULSE_FAST and WRATE (in the Pulse Source area), selects the X factor for the pulse generation rate.
PULSE_FAST	Square button	1	This button, in conjunction with PULSE_SLOW, selects the X factor for the pulse generation rate (see WRATE field).

X	PULSE_SLOW	PULSE_FAST
$1.5*2^2 = 6$	0	0
$1.5*2^9 = 96$	0	1
$1.5*2^{-4} = 0.09375$	1	0
1.5	1	1

IA_8x	Square button	0	Additional ADC gain of 8x can be selected for phase A by selecting "1".
IB_8x	Square button	0	Additional ADC gain of 8x can be selected for phase B by selecting "1".
IC_8x	Square button	0	Additional ADC gain of 8x can be selected for phase C by selecting "1".
DEFAULT PPM	Square button	0	This button enables temperature compensation by the host. If the bit associated with DEFAULT PPM is 0, the 71M6515H internally controls the temperature compensation based on the stored VREF characterization values. When DEFAULT PPM is 0, the host may write values into the PPMC and PPMC2 fields to influence temperature compensation. When DEFAULT PPM is toggled back to 0 after the host had written values to the PPMC and PPMC2 fields, these fields will go back to displaying the original internal values.

Status Word and Status Mask Area (17):

This area consists of 18 square buttons and indicator lights towards the right edge of the GUI window.

The bits of the *STATUS* word are displayed in the indicator lights right next to the square buttons. A green light indicates no activity, a red light indicates that the corresponding bit is set.

Individual bits of the *STATUS* word can be made to generate interrupts. When the square button right next to the status bit is pressed (1), the corresponding bit, when active, will generate an interrupt on the IRQZ output pin. Activity on the IRQZ output pin is indicated with the green LED D8 on the Demo Board.

GUI Element (Label)	Default	Function
BOOTUP	1	BOOTUP bit.
SAG A	0	sag A bit for phase A.
SAG B	0	sag B bit for phase B.
SAG C	0	sag C bit for phase C.
F0	0	F0 (fundamental of the input signal) bit.
MAXV	0	Vpeak bit.
MAXI	0	Ipeak bit.
1SEC	0	1-second bit.
VXEDGE	0	VXEDGE bit (change in the state of the VX comparator).
DEDGE	0	DEDGE bit (change in the state of any selected DIO).
XOFV	0	XOVF bit (host has failed to read at least one energy output value).
READY	0	READY bit (fresh output values are available).
CREEPA	0	Creep bit for phase A.
CREEPB	0	Creep bit for phase B.
CREEPC	0	Creep bit for phase C.
IGNORED	0	Command ignored by the 71M6515H
PULSE1	0	PULSEW_ERR bit (missing host data when in external mode).
PULSE2	0	PULSER_ERR bi (missing host data when in external mode).
PULSE3	0	PULSE3_ERR bit (missing host data when in external mode).
PULSE4	0	PULSE4_ERR bit (missing host data when in external mode).

Main Edge Area (18):

This area consists of two display fields below the Status Word area.

GUI Element (Label)	Default	Function
Main Edge COUNT	0	This field displays the number of zero crossings encountered in the last accumulation interval.
Main Edge TOTAL	0	This field displays the total number of zero crossings counted since the last reset. The value is reset to zero when the CLR ACCUM button in the Energy, Voltage/Current and Phase Area is pressed.

Operating Time/RTC Area (19):

This area consists of three display fields and two rectangular buttons, all located towards the lower right edge of the GUI window.

GUI Element (Label)	Element Type	Function
Operating time	Display field	Displays the total operating time of the 6515H chip, measured in 0.01 hours.
Real Time Clock	Display field	Displays the date of year according to the RTC in the 6515H chip.
Real Time Clock	Display field	Displays the time of day according to the RTC in the 6515H chip.
Set RTC	Rectangular button	Pressing this button synchronizes the RTC of the 6515H chip with the clock of the host PC.
EXIT	Rectangular button	Pressing this button will terminate the GUI control program.

Chip Version Area (20):

This area consists of only one display field.

GUI Element (Label)	Function
Chip Version	This field displays the type and version of the 6515H chip, e.g. 6515HB03.

1.8.6 ADJUSTING THE KH FACTOR FOR THE DEMO BOARD

The Kh factor (i.e. energy per pulse) is determined by the following equation:

$$Kh = \frac{VMAX\ IMAX\ In8}{SUM\_CYCLES\ WRATE\ X} 1.5757 \quad Wh / Pulse$$

Where:

VMAX: The RMS voltage value that corresponds to the 250mV maximum input signal to the IC **(default = 600V).**

IMAX The RMS current value that corresponds to the 250mV maximum input signal to the IC **(default = 208A).**

SUM_CYCLES The value controlling the length of the accumulation cycle, as determined by bits 8-13 in the *CONFIG* register **(default = 60).** The length of an accumulation cycle is t = *SUM_CYCLES* * 16.66ms.

WRATE The value in the pulse rate control register *WRATE*, **(default = 683).**

X The pulse rate acceleration factor, determined by bits 25 (*PULSE_FAST*) and 26 (*PULSE_SLOW*) in the *CONFIG* register **(default = 1.5).**

Almost any desired Kh factor can be selected for the Demo Board by resolving the formula for WRATE.

1.8.7 ADJUSTING THE DEMO BOARDS TO DIFFERENT CURRENT TRANSFORMERS AND VOLTAGE DIVIDERS

The Demo Board is prepared for use with 2000:1 current transformers (CTs). This means that for the unmodified Demo Board, 208A on the primary side at 2000:1 ratio result in 104mA on the secondary side, causing 177mV at the 1.7Ω resistor pairs R24/R25, R36/R37, R56/R57 (2 x 3.4Ω in parallel).

In general, when *IMAX* is applied to the primary side of the CT, the voltage V_{in} at the IA or IB input of the 71M6515H IC is determined by the following formula:

$$V_{in} = R \cdot I = \frac{R \cdot IMAX}{N}$$

where N = transformer winding ratio, R = resistor on the secondary side

If, for example, *IMAX* = 208A are applied to a CT with a 2500:1 ratio, only 83.2mA will be generated on the secondary side, causing only 141mV The steps required to adapt a 71M6515H Demo Board to a transformer with a winding ratio of 2500:1 are outlined below:

1) The formula $R_x = \frac{\frac{177mV}{IMAX}}{N}$ is applied to calculate the new resistor R_x. We calculate Rx to 2.115Ω
2) **Changing the resistors R24/R25, R106/R107 to a combined resistance of 2.115Ω** (for each pair) will cause the desired voltage drop of 177mV appearing at the IA, or IB inputs of the 71M6515H IC.
3) *WRATE* should be adjusted to achieve the desired Kh factor, as described in section 1.8.6.

Simply scaling *IMAX* is not recommended, since peak voltages at the 71M6515H inputs should always be in the range of 0 through ±250mV (equivalent to 177mV rms). If a CT with a much lower winding ratio than 1:2,000 is used, higher secondary currents will result, causing excessive voltages at the 71M6515H inputs. Conversely, CTs with much higher ratio will tend to decrease the useable signal voltage range at the 71M6515H inputs and may thus decrease resolution.

The 71M6515H Demo Board comes equipped with its own network of resistor dividers for voltage measurement mounted on the PCB. The resistor values (for the 4-layer Demo Board) are 2.5477MΩ (R15-R21, R26-R31 combined) and 750Ω (R32), resulting in a ratio of 1:3,393.933. This means that *VMAX* equals 176.78mV*3,393.933 = 600V. A large value for *VMAX* has been selected in order to have headroom for over-voltages. This choice need not be of concern, since the ADC in the 71M6515H has enough resolution, even when operating at 120Vrms or 240Vrms.

If a **different set of voltage dividers** or an external voltage transformer is to be used, scaling techniques similar to those applied for the current transformer should be used.

In the following example we assume that the line voltage is not applied to the resistor divider for VA formed by R15-R21, R26-R31, and R32, but to a voltage transformer with a ratio N of 20:1, followed by a simple resistor divider. We also assume that we want to maintain the value for *VMAX* at 600V to provide headroom for large voltage excursions.

When applying VMAX at the primary side of the transformer, the secondary voltage V_s is:

V_s = VMAX / N

V_s is scaled by the resistor divider ratio R_R. When the input voltage to the voltage channel of the 71M6515H is the desired 177mV, V_s is then given by:

$V_s = R_R$ * 177mV

Resolving for R_R, we get:

R_R = (VMAX / N) / 177mV = (600V / 30) / 177mV = 170.45

This divider ratio can be implemented, for example, with a combination of one 16.95kΩ and one 100Ω resistor.

1.9 CALIBRATING THE DEMO METER

The general calibration procedure is as follows:

1. Obtain the deviation from ideal accuracy using a meter calibration system (see section 2.1).
2. Calculate the calibration values using the error terms obtained in step 1 (see section 2.1).
3. Enter the calibration values generated in step 2 using the GUI.
4. Test the meter with the new calibration constants.

2

2 APPLICATION INFORMATION

2.1 CALIBRATION PROCEDURE

In this section, requirements for calibration systems will be discussed, and calibration procedures will be suggested. Sample calibration procedures for CT/shunt meters are provided requiring three or five measurements. A sample calibration procedure is provided for Rogowski meters.

2.1.1 CALIBRATION SYSTEMS

Performing a proper calibration requires that a calibration system is used, i.e. equipment that applies accurate voltage, load current and load angle to the unit being calibrated, while measuring the response from the unit being calibrated in a repeatable way. By repeatable we mean that the calibration system is synchronized to the meter being calibrated. Best results are achieved when the first pulse from the meter opens the measurement window of the calibration system. This mode of operation is opposed to a calibrator that opens the measurement window at random time and that therefore may or may not catch certain pulses emitted by the meter.

It is also very important that the calibration system, just like the hookup of a real meter, applies voltage constantly while varying the current. **For the calibration of the 71M6515H it is essential that voltage is applied at least a few seconds before the measurement is started**, i.e. before current is applied. This is necessary because:

- In case the internal power supply is used, the 71M6515H needs a few seconds to power up.
- Even if the 71M6515H has DC power (V3P3), filters and other functions inside the CE require time to get synchronized in order to obtain accurate measurements.

For a typical energy calibration, a meter calibration system is used to apply a calibrated load, e.g. 240V at 30A, while interfacing the voltage and current sensors to the 71M6515H. This load should result in an observable pulse rate at the WPULSE output depending on the selected energy per pulse. For example, 7.2kW will result in a pulse rate corresponding to 7200Wh/3600s = 2Wh/s.

Most calibration systems provide ways to evaluate the observed pulse rate by comparing it to the ideal pulse rate.

2.1.2 DEFINITIONS

Each meter phase must be calibrated individually. The PHADJ equations apply only when a current transformer is used for the phase in question. If a Rogowski coil is used, the phase compensation should be correct by default and adjustments are required only to CAL_Ix and CAL_Vx. Note that positive load angles correspond to lagging current (see Figure 2-1).

The calibration procedures described below should be followed after interfacing the voltage and current sensors to the 71M6515H chip. When properly interfaced, the V3P3 power supply is connected to the meter neutral and is the DC reference for each input. Each voltage and current waveform, as seen by the 71M6515H, is scaled to be less than 250mV (peak).

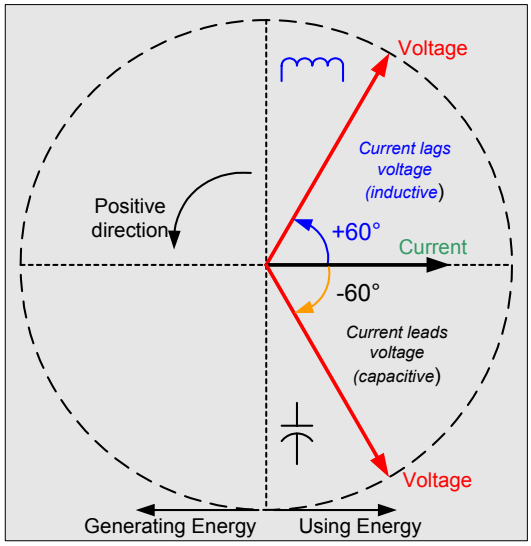


Figure 2-1: Phase Angle Definitions

2.1.3 ERROR SOURCES IN A METER (CT/SHUNT RESISTOR)

A typical meter has phase and gain errors as shown by ϕ_S, A_{XI}, and A_{XV} in Figure 2-2. Following the typical meter convention of current phase being in the lag direction, the small amount of phase lead in a typical current sensor is represented as $-\phi_S$. The errors shown in Figure 2-2 represent the sum of all gain and phase errors. They include errors in voltage attenuators, current sensors, and in ADC gains. In other words, no errors are made in the 'input' or 'meter' boxes.

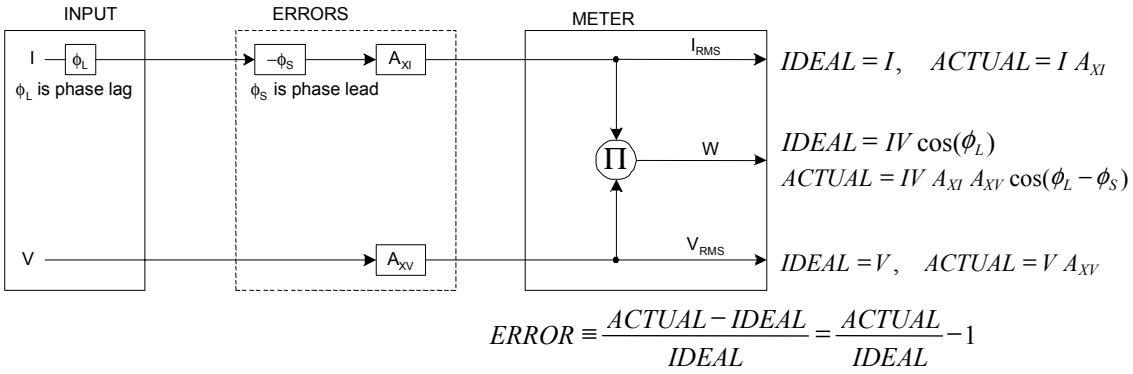


Figure 2-2: Watt Meter with Gain and Phase Errors

During the calibration phase, we measure errors and then introduce correction factors to nullify their effect. With three unknowns to determine, we must make at least three measurements. If we make more measurements, we can average the results.

2.1.4 CALIBRATION WITH THREE MEASUREMENTS

The simplest calibration method is to make three measurements. Typically, a voltage measurement and two Watt-hour (Wh) measurements are made.

We assume the voltage measurement has the error E_V, and the two Wh measurements have errors E_0 and E_{60}, where E_0 is measured with $\phi_L = 0$ and E_{60} is measured with $\phi_L = 60$. These values should be simple ratios—not percentage values. They should be zero when the meter is accurate and negative when the meter runs slow. The fundamental frequency is f_0. T is equal to $1/f_S$, where f_S is the sample frequency (2560.62Hz). Set all calibration factors to nominal: *CAL_IA* = 16384, *CAL_VA* = 16384, *PHADJ_A* = 0.

From the voltage measurement, we determine that

1.➔ $$A_{XV} = E_V + 1$$

We use the other two measurements to determine ϕ_S and A_{XI}.

2. $$E_0 = \frac{IV\, A_{XV}\, A_{XI} \cos(0 - \phi_S)}{IV \cos(0)} - 1 = A_{XV}\, A_{XI} \cos(\phi_S) - 1$$

2a. $$A_{XV} A_{XI} = \frac{E_0 + 1}{\cos(\phi_S)}$$

3. $$E_{60} = \frac{IV\, A_{XV}\, A_{XI} \cos(60 - \phi_S)}{IV \cos(60)} - 1 = A_{XV}\, A_{XI} \frac{\cos(60 - \phi_S)}{\cos(60)} - 1$$

3a. $$E_{60} = \frac{A_{XV} A_{XI} \left[\cos(60)\cos(\phi_S) + \sin(60)\sin(\phi_S)\right]}{\cos(60)} - 1$$

$$= A_{XV} A_{XI} \cos(\phi_S) + A_{XV} A_{XI} \tan(60)\sin(\phi_S) - 1$$

Combining 2a and 3a:

4. $$E_{60} = E_0 + (E_0 + 1)\tan(60)\tan(\phi_S)$$

5. $$\tan(\phi_S) = \frac{E_{60} - E_0}{(E_0 + 1)\tan(60)}$$

6.➔ $$\phi_S = \tan^{-1}\left(\frac{E_{60} - E_0}{(E_0 + 1)\tan(60)}\right)$$

and from 2a:

7.➔ $$A_{XI} = \frac{E_0 + 1}{A_{XV} \cos(\phi_S)}$$

Now that we know the A_{XV}, A_{XI}, and ϕ_S errors, we calculate the new calibration voltage gain coefficient from the previous ones:

$$CAL\_V_{NEW} = \frac{CAL\_V}{A_{XV}}$$

We calculate PHADJ from ϕ_S, the desired phase lag:

$$PHADJ = 2^{20}\left[\frac{\tan(\phi_S)\left[1 + (1 - 2^{-9})^2 - 2(1 - 2^{-9})\cos(2\pi f_0 T)\right]}{(1 - 2^{-9})\sin(2\pi f_0 T) - \tan(\phi_S)\left[1 - (1 - 2^{-9})\cos(2\pi f_0 T)\right]}\right]$$

And we calculate the new calibration current gain coefficient, including compensation for a slight gain increase in the phase calibration circuit.

$$CAL\_I_{NEW} = \frac{CAL\_I}{A_{XI}} \frac{1}{\sqrt{1 + \frac{2^{-20} PHADJ(2 + 2^{-20} PHADJ - 2(1 - 2^{-9})\cos(2\pi f_0 T))}{1 - 2(1 - 2^{-9})\cos(2\pi f_0 T) + (1 - 2^{-9})^2}}}$$

2.1.5 CALIBRATION WITH FIVE MEASUREMENTS

The five measurement method provides more orthogonality between the gain and phase error derivations. This method involves measuring E_V, E_0, E_{180}, E_{60}, and E_{300}. Again, set all calibration factors to nominal, i.e. *CAL_IA* = 16384, *CAL_VA* = 16384, *PHADJ_A* = 0.

First, calculate A_{XV} from E_V:

1.➔ $A_{XV} = E_V + 1$

Calculate A_{XI} from E_0 and E_{180}:

2. $E_0 = \frac{IV\ A_{XV}\ A_{XI} \cos(0 - \phi_S)}{IV \cos(0)} - 1 = A_{XV}\ A_{XI} \cos(\phi_S) - 1$

3. $E_{180} = \frac{IV\ A_{XV}\ A_{XI} \cos(180 - \phi_S)}{IV \cos(180)} - 1 = A_{XV}\ A_{XI} \cos(\phi_S) - 1$

4. $E_0 + E_{180} = 2 A_{XV} A_{XI} \cos(\phi_S) - 2$

5. $A_{XV} A_{XI} = \frac{E_0 + E_{180} + 2}{2\cos(\phi_S)}$

6.➔ $A_{XI} = \frac{(E_0 + E_{180})/2 + 1}{A_{XV} \cos(\phi_S)}$

Use above results along with E_{60} and E_{300} to calculate ϕ_S.

7. $E_{60} = \frac{IV\ A_{XV}\ A_{XI} \cos(60 - \phi_S)}{IV \cos(60)} - 1$

$= A_{XV} A_{XI} \cos(\phi_S) + A_{XV} A_{XI} \tan(60) \sin(\phi_S) - 1$

8. $E_{300} = \frac{IV\ A_{XV}\ A_{XI} \cos(-60 - \phi_S)}{IV \cos(-60)} - 1$

$= A_{XV} A_{XI} \cos(\phi_S) - A_{XV} A_{XI} \tan(60) \sin(\phi_S) - 1$

Subtract 8 from 7

9. $E_{60} - E_{300} = 2 A_{XV} A_{XI} \tan(60) \sin(\phi_S)$

use equation 5:

10. $E_{60} - E_{300} = \frac{E_0 + E_{180} + 2}{\cos(\phi_S)} \tan(60) \sin(\phi_S)$

11. $E_{60} - E_{300} = (E_0 + E_{180} + 2) \tan(60) \tan(\phi_S)$

12.➔ $\phi_S = \tan^{-1}\left(\frac{(E_{60} - E_{300})}{\tan(60)(E_0 + E_{180} + 2)}\right)$

Now that we know the A_{XV}, A_{XI}, and ϕ_S errors, we calculate the new calibration voltage gain coefficient from the previous ones:

$$CAL\_V_{NEW} = \frac{CAL\_V}{A_{XV}}$$

We calculate PHADJ from ϕ_S, the desired phase lag:

$$PHADJ = 2^{20}\left[\frac{\tan(\phi_S)\left[1+(1-2^{-9})^2-2(1-2^{-9})\cos(2\pi f_0 T)\right]}{(1-2^{-9})\sin(2\pi f_0 T)-\tan(\phi_S)\left[1-(1-2^{-9})\cos(2\pi f_0 T)\right]}\right]$$

And we calculate the new calibration current gain coefficient, including compensation for a slight gain increase in the phase calibration circuit.

$$CAL\_I_{NEW} = \frac{CAL\_I}{A_{XI}}\frac{1}{\sqrt{1+\dfrac{2^{-20}PHADJ(2+2^{-20}PHADJ-2(1-2^{-9})\cos(2\pi f_0 T))}{1-2(1-2^{-9})\cos(2\pi f_0 T)+(1-2^{-9})^2}}}$$

2.1.6 CALIBRATION FOR METERS WITH ROGOWSKI COIL SENSORS

Rogowski coils generate a signal that is the derivative of the current. The 6515H Rogowski module implemented in the Rogowski CE image digitally compensates for this effect and has the usual gain and phase calibration adjustments. Additionally, calibration adjustments are provided to eliminate voltage coupling from the sensor input.

Current sensors built from Rogowski coils have a relatively high output impedance that is susceptible to capacitive coupling from the large voltages present in the meter. The most dominant coupling is usually capacitance between the primary of the coil and the coil's output. This coupling adds a component proportional to the derivative of voltage to the sensor output. This effect is compensated by the voltage coupling calibration coefficients.

As with the CT procedure, the calibration procedure for Rogowski sensors uses the meter's display to calibrate the voltage path and the pulse outputs to perform the remaining energy calibrations. The calibration procedure must be done to each phase separately, making sure that the pulse generator is driven by the accumulated real energy for just that phase. In other words, the pulse generator input should be set to WhA, WhB, or WhC, depending on the phase being calibrated.

The IC has to be configured for Rogowski mode (*IMAGE*=01). In preparation of the calibration, all calibration parameters are set to their default values. *VMAX* and *IMAX* are set to reflect the system design parameters. *WRATE* and *PUSE_SLOW*, *PULSE_FAST* are adjusted to obtain the desired Kh.

Step 1: Basic Calibration: After making sure *VFEED_A*, *VFEED_B*, and *VFEED_C* are zero, perform either the three measurement procedure (2.1.4) or the five measurement calibration procedure (2.1.5) described in the CT section. Perform the procedure at a current large enough that energy readings are immune from voltage coupling effects.

The one exception to the CT procedure is the equation for PHADJ—after the phase error, ϕs, has been calculated, use the PHADJ equation shown below. Note that the default value of PHADJ is not zero, but rather –3973.

$$PHADJ = PHADJ_{PREVIOUS} - \phi_S 1786\frac{50}{f_0}$$

If voltage coupling at low currents is introducing unacceptable errors, perform step 2 below to select non-zero values for *VFEED_A*, *VFEED_B*, and *VFEED_C*.

Step 2: Voltage Cancellation: Select a small current, I_{RMS}, where voltage coupling introduces at least 1.5% energy error. At this current, measure the errors E_0 and E_{180} to determine the coefficient $VFEED$.

$$VFEED = \frac{E_0 - E_{180}}{2} 2^{25} \frac{I_{RMS}}{I_{MAX}} \frac{V_{MAX}}{V_{RMS}} - VFEED_{PREVIOUS}$$

2.1.7 CALIBRATION SPREADSHEETS

Calibration spreadsheets are available from TERIDIAN Semiconductor. Figure 2-3 shows the spreadsheet used for three measurements.

Figure 2-3 shows the calibration spreadsheet used for five measurements.

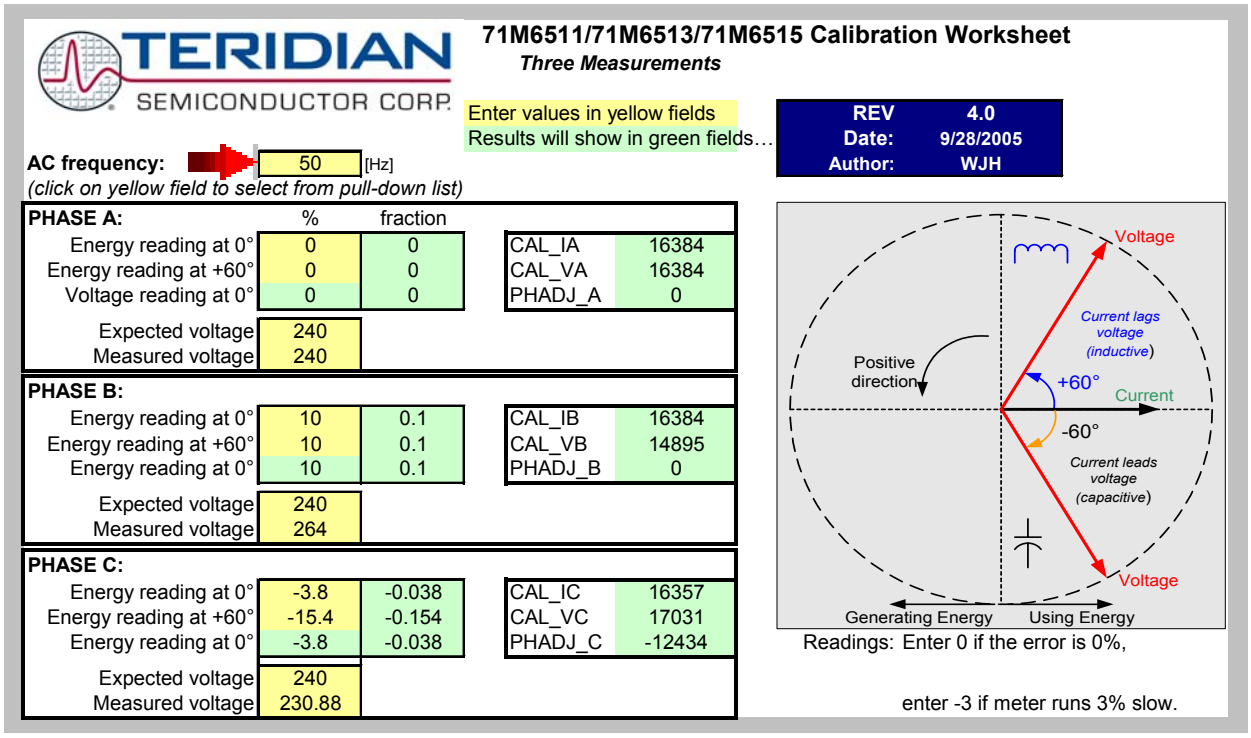
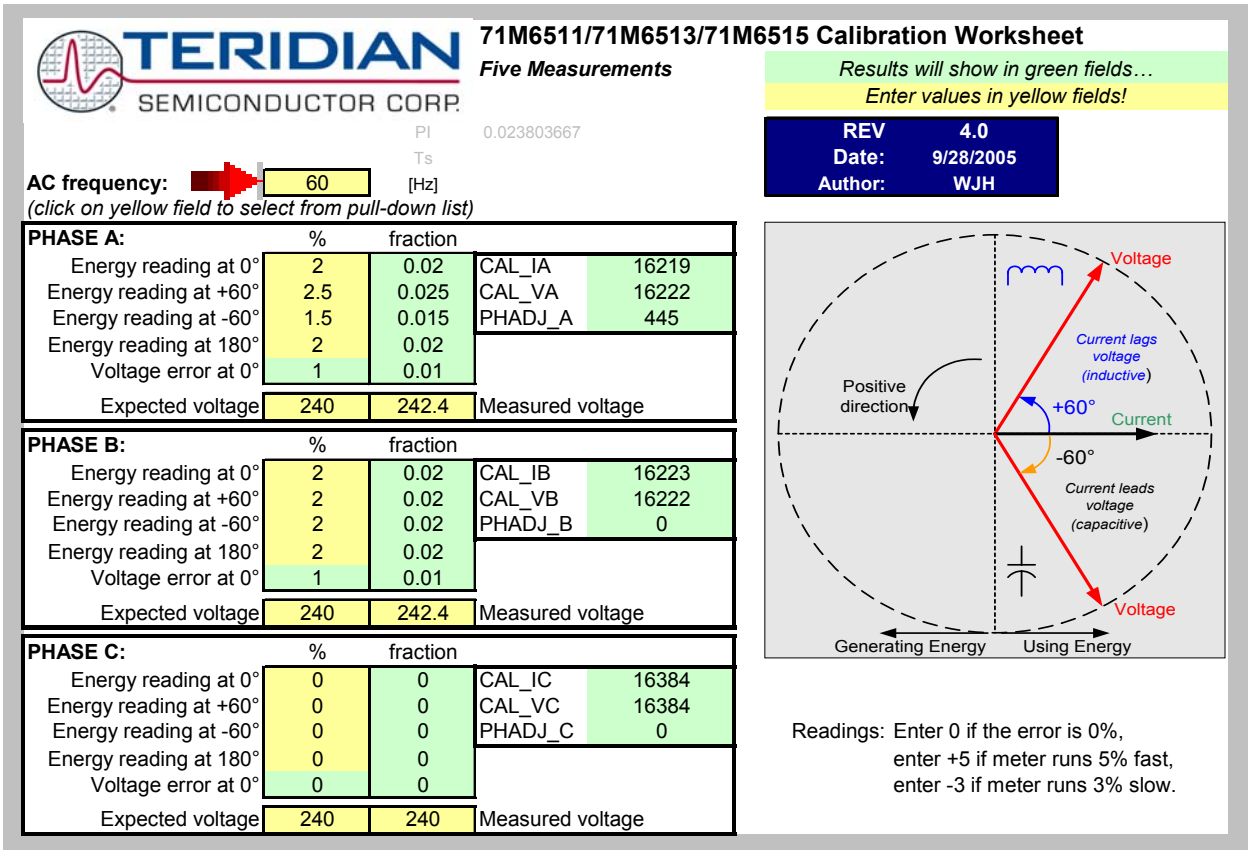


Figure 2-3: Calibration Spreadsheet for Three Measurements



71M6511/71M6513/71M6515 Calibration Worksheet

Five Measurements

Results will show in green fields…
Enter values in yellow fields!

PI 0.023803667
Ts

REV	4.0
Date:	9/28/2005
Author:	WJH

AC frequency: 60 [Hz]
(click on yellow field to select from pull-down list)

PHASE A:	%	fraction		
Energy reading at 0°	2	0.02	CAL_IA	16219
Energy reading at +60°	2.5	0.025	CAL_VA	16222
Energy reading at -60°	1.5	0.015	PHADJ_A	445
Energy reading at 180°	2	0.02		
Voltage error at 0°	1	0.01		
Expected voltage	240	242.4	Measured voltage	

PHASE B:	%	fraction		
Energy reading at 0°	2	0.02	CAL_IB	16223
Energy reading at +60°	2	0.02	CAL_VB	16222
Energy reading at -60°	2	0.02	PHADJ_B	0
Energy reading at 180°	2	0.02		
Voltage error at 0°	1	0.01		
Expected voltage	240	242.4	Measured voltage	

PHASE C:	%	fraction		
Energy reading at 0°	0	0	CAL_IC	16384
Energy reading at +60°	0	0	CAL_VC	16384
Energy reading at -60°	0	0	PHADJ_C	0
Energy reading at 180°	0	0		
Voltage error at 0°	0	0		
Expected voltage	240	240	Measured voltage	

Readings: Enter 0 if the error is 0%,
enter +5 if meter runs 5% fast,
enter -3 if meter runs 3% slow.

Figure 2-4: Calibration Spreadsheet for Five Measurements

2.1.8 COMPENSATING FOR NON-LINEARITIES

Nonlinearity is most noticeable at low currents, as shown in Figure 2-5, and can result from input noise and truncation. Nonlinearities can be eliminated using the *QUANT_W* variable.

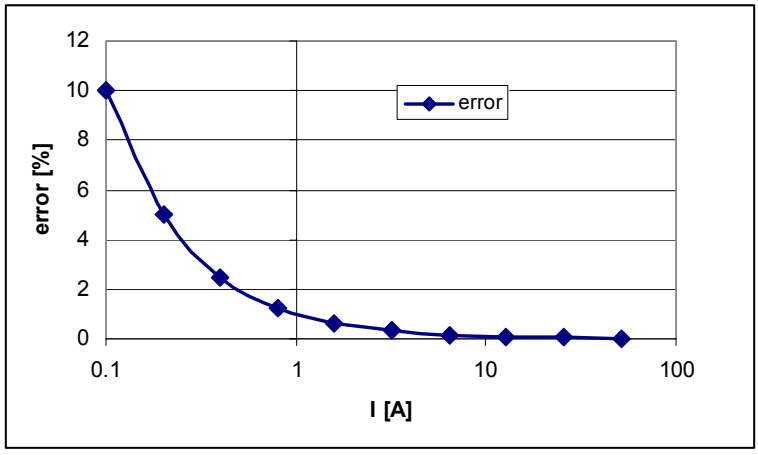


Figure 2-5: Non-Linearity Caused by Quantification Noise

The error can be seen as the presence of a virtual constant noise current. While 10mA hardly contribute any error at currents of 10A and above, the noise becomes dominant at small currents.

The value to be used for QUANT can be determined by the following formula:

$$QUANT\_W = -\frac{\frac{error}{100} V \cdot I}{VMAX \cdot IMAX \cdot LSB}$$

Where error = observed error at a given voltage (V) and current (I),
VMAX = voltage scaling factor, as described in section 1.8
IMAX = current scaling factor, as described in section 1.8
LSB = QUANT LSB value = $7.4162*10^{-10}$W

Example: Assuming an observed error as in Figure 2-5, we determine the error at 1A to be +1%. If VMAX is 600V and IMAX = 208A, and if the measurement was taken at 240V, we determine QUANT as follows:

$$QUANT\_W = -\frac{\frac{1}{100} 240 \cdot 1}{600 \cdot 208 \cdot 7.4162 \cdot 10^{-10}} = -11339$$

QUANT_W is to be written to the CE location 0x2F. It does not matter which current value is chosen as long as the corresponding error value is significant (5% error at 0.2A used in the above equation will produce the same result for *QUANT_W*).

Input noise and truncation can cause similar errors in the VAR calculation that can be eliminated using the *QUANT_VAR* variable. *QUANT_VAR* is determined using the same formula as *QUANT_W*.

2.2 SCHEMATIC INFORMATION

In this section, hints on proper schematic design are provided that will help designing circuits that are functional and sufficiently immune to EMI (electromagnetic interference).

2.2.1 COMPONENTS FOR THE VFLT PIN

The VFLT pin (pin 59) of the 71M6515H must never be left unconnected.

A voltage divider should be used to establish that the voltage at VFLT is in a safe range when the meter is in mission mode (see Figure 2-6). VFLT must be lower than 2.9V in all cases in order to keep the hardware watchdog timer enabled.

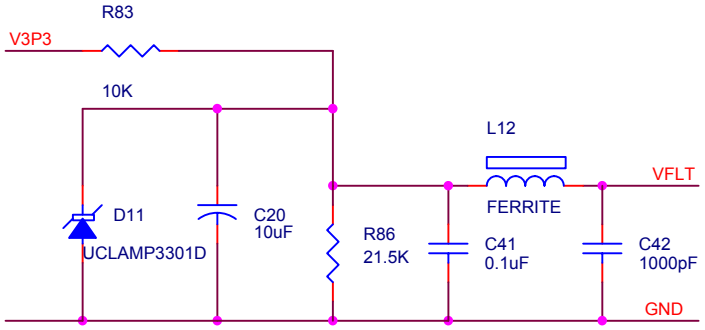


Figure 2-6: Voltage Divider for VFLT

2.2.2 RESET CIRCUIT

Even though a functional meter will not necessarily need a reset switch, the 71M6515H Demo Boards provide a reset pushbutton (SW2) that can be used when prototyping and debugging software. When a circuit is used in an EMI environment, the RESETZ pin should be supported by the external components shown in Figure 2-7. R_{75} should be in the range of 200Ω, R_{77} should be around 10Ω. The capacitor C_{38} should be 1000pF. R_{75} and C_{38} should be mounted as close as possible to the IC. In cases where the trace from the pushbutton switch to the RESETZ pin poses an EMI problem, R_{77} can be removed.

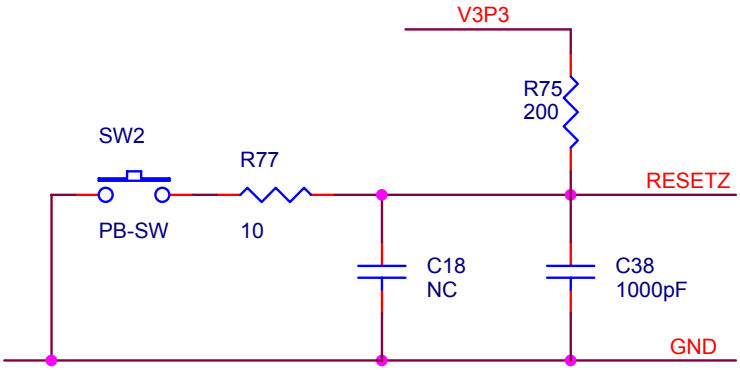


Figure 2-7: External Components for RESETZ

2.2.3 OSCILLATOR

The oscillator of the 71M6515H drives a standard 32.768kHz watch crystal (see Figure 2-8). Crystals of this type are accurate and do not require a high current oscillator circuit. The oscillator in the 71M6515H has been designed specifically to handle watch crystals and is compatible with their high impedance and limited power handling capability. The oscillator power dissipation is very low to maximize the lifetime of any battery backup device attached to the VBAT pin.

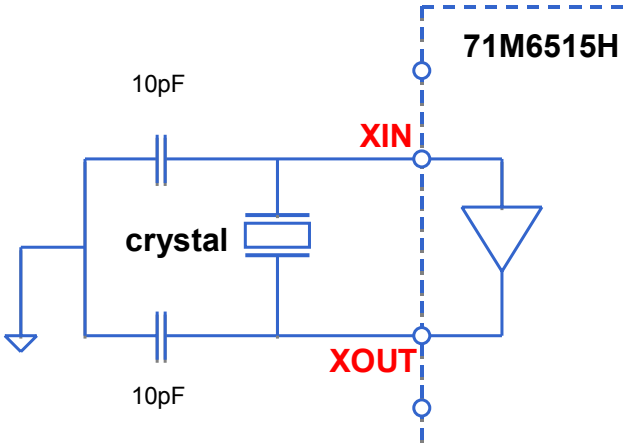


Figure 2-8: Oscillator Circuit

Note: It is not necessary to place an external resistor across the crystal, i.e. R91 on the 4-Layer Demo Board must not be populated.

Note: Capacitor values for the crystal must be <15pF.

2.3 TESTING THE DEMO BOARD

This section will explain how the 71M6515H IC can be tested. Hints given in this section will help evaluating the features of the Demo Board and understanding the IC and its peripherals.

2.3.1 TESTING THE DEMO BOARD USING THE GUI

It is a good idea to get familiar with the features of the 71M6515H chip and the Demo Board using the GUI program. Some features can be explored by just feeding the +5VDC to the Demo Board without any high voltage involved.

When applying voltage and current signals to the Demo Board, the GUI should look similar to the screen print shown in Figure 2-9.

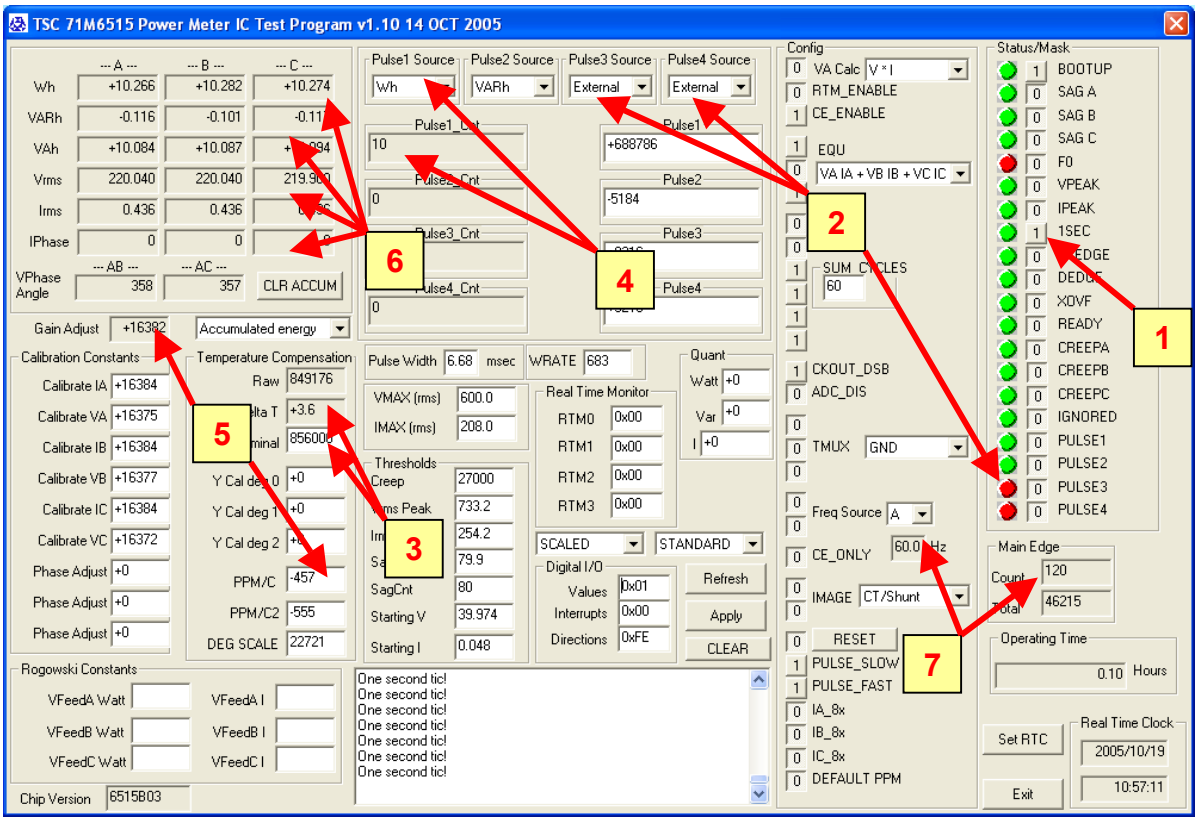


Figure 2-9: Typical GUI Window

A few observations can be derived from the sample GUI window in Figure 2-9:

1. The 1-second interrupt is enabled
2. Pulse source 3 and 4 are selected to be external, but host data is missing, causing the PULSE3 and PULSE4 interrupts to occur.
3. A raw temperature value of 856,000 has been stored in the nominal temperature field. The chip is now 3.6° above the nominal temperature.
4. Wh have been selected for pulse source 1, and 10 Wh pulses have been generated.
5. The temperature compensation factors PPM/C and PPM/C^2 have been calculated by the chip, and, together with the temperature deviation from nominal, the gain is adjusted to 16382.
6. 10.2Wh, -0.1VARh, and 10.08VAh have been collected in each channel, the RMS voltages are close to 220V, the RMS currents are at 0.435A, and the V/I phase angles are at 0 degrees.
7. Phase A is selected for frequency detection. The measured frequency is at 60Hz, and 120 zero crossings were detected in the previous accumulation interval.

2.3.2 FUNCTIONAL METER TEST

This is the test that every Demo Board has to pass before being integrated into a Demo Kit. Before going into the functional meter test, the Demo Board has already passed a series of bench-top tests, but the functional meter test is the first test that applies realistic high voltages (and current signals from current transformers) to the Demo Board.

Figure 2-10 shows a meter connected to a typical calibration system. The calibrator supplies calibrated voltage and current signals to the meter. It should be noted that the current flows through the CT or CTs that are not part of the Demo Board. The Demo Board rather receives the voltage output signals fro the CT. An optical pickup senses the pulses emitted by the meter and reports them to the calibrator. Some calibration systems have electrical pickups. The calibrator measures the time between the pulses and compares it to the expected time, based on the meter Kh and the applied power.

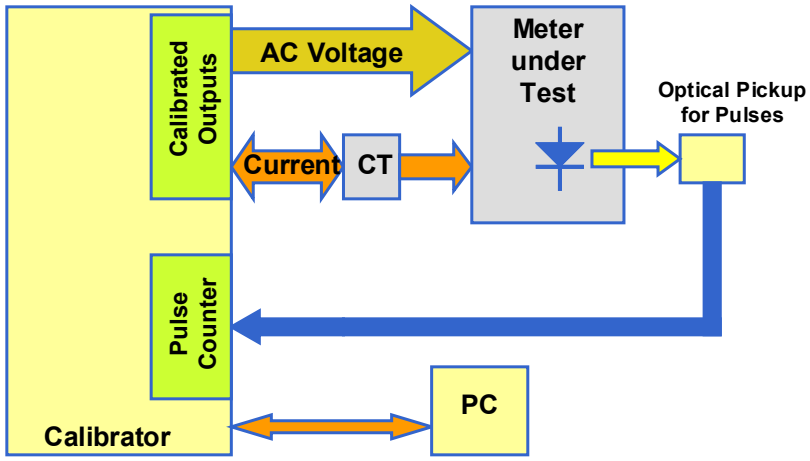


Figure 2-10: Meter with Calibration System

TERIDIAN Demo Boards are not calibrated prior to shipping. However, the Demo Board pulse outputs are tested and compared to the expected pulse output. Figure 2-11 shows the screen on the controlling PC for a typical Demo Board. The numbers in the red fields under "As Found" represents the measured errors. The rows represent measurements under various conditions, such as:

Row 1: Phase A at 30A

Row 2: Phase B at 30A

Row 3: Phase C at 30A

Row 4: All elements combined at 30A each and 60° phase angle.

Row 5: All elements combined at 0.3A each and 0° phase angle.

Row 6: All elements combined at 200A each and 0° phase angle.

Both numbers are given in percent. This means that for the measured Demo Board, the sum of all errors resulting from tolerances of PCB components, CTs, and 71M6515H tolerances was in the range of –0.025% to –0.459%, a range that can easily be compensated by calibration.

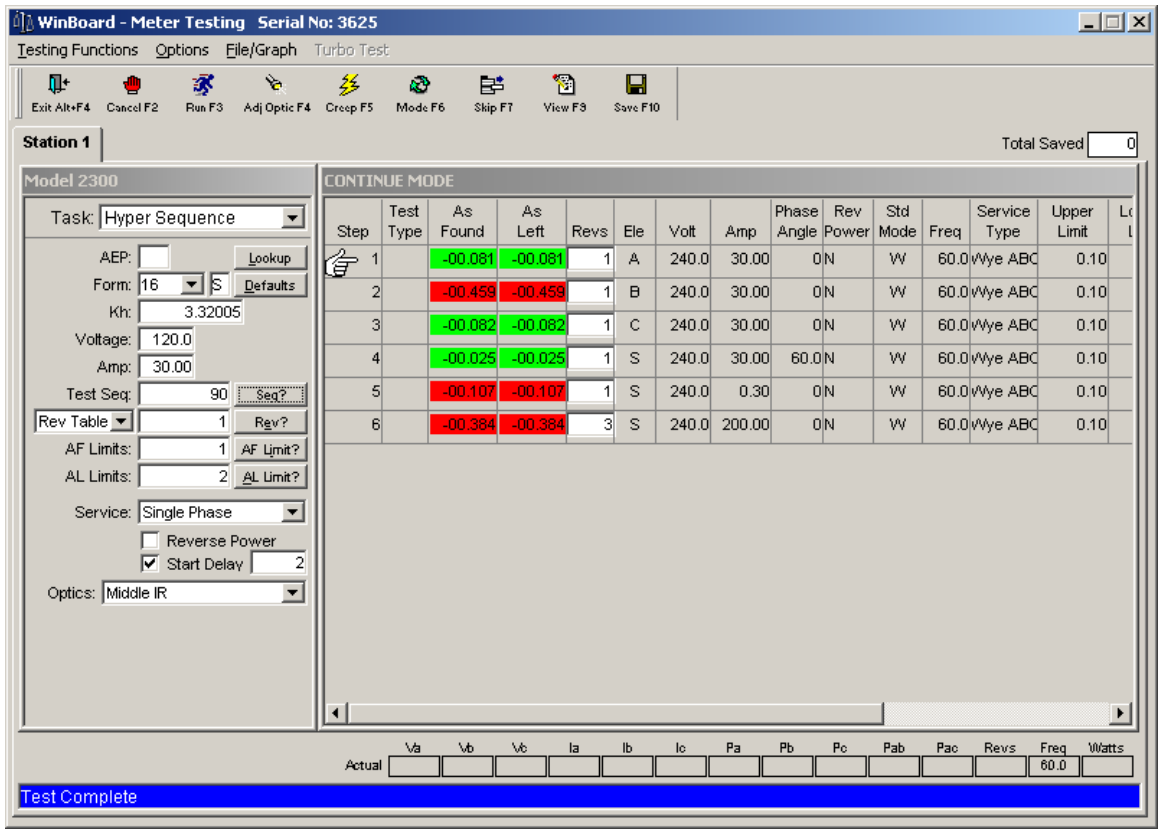


Figure 2-11: Calibration System Screen

3

3 HARDWARE DESCRIPTION

3.1 BOARD DESCRIPTION: JUMPERS, SWITCHES AND TEST POINTS

The items described in the following tables refer to the flags in Figure 3-1

Item # (Figure 2.1)	Schematic & PCB Silk Screen Reference	Name	Use
1	JP6	SSI	Header for high-speed serial interface (SSI). One pin row is connected to GND.
2	TP17	TMUXOUT	Test point for TMUXOUT signal
3	TP18	CKTEST	Test point for CKTEST signal
4	JP19		5-pin header. A jumper should be installed between V3P3 and VFLT to disable the hardware watchdog timer.
5	TP7	VREF	Test point for VREF signal
6	TP1, TP3, TP5	IA, IB, IC	Two-pin headers that provide access to the current input pins of the IC. One terminal is ground, the other is the respective line current sense input to the IC.
7	JP26, JP27, JP28	IA_IN, IB_IN, IC_IN	CT connections. The two-pin headers are mounted on the bottom of the PCB. One terminal is the 3.3V reference.
8	JP1	PS_SEL[0]	Two-pin header. When the jumper is installed, the on-board power supply (AC signal) is used to power the demo board. When not installed, the board must be powered by an external supply connected to S1. Normally installed.
9	TP2, TP4, TP6	VA, VB, and VC	Two-pin header test points. One end is either the VA, VB or VC line voltage input to the IC and the other end is V3P3.
10	JP25	NEUTRAL	A spade terminal mounted on the bottom of the board for the connection of the NEUTRAL wire.
11	JP8	VBAT Selection	Three-pin header that allows selection of power to the VBAT pin. **In the default setting, a jumper is placed between pins 1 and 2, causing VBAT to be tied to the IC supply**. When using an external battery, the battery is connected between pins 2 (+) and 3 (GND).

Table 3-1: 71M6515H Demo Board Description: 1/3

12	S1	5 Volt external supply	Plug for connecting the external 5 VDC power supply ("wall transformer")
13	SW2	RESET	Chip reset switch: The RESETZ pin has an internal pull up that allows normal chip operation. When the switch is pressed, the RESETZ pin is pulled low which resets the IC into a known state.
14	JP22, JP23, JP24	VA_IN, VB_IN, VC_IN 	Spade terminals mounted on the bottom of the board for the connection of the phase A, B, and C wires. Each point has a resistor divider that leads to the VA, VB, or VC pin on the chip. **Caution: High Voltage! Do not touch these pins!**
15	TP13, TP14	GND	GND test points
16	JP13	PULSE_INT	Three-pin header for selecting the pulse output initial power-up voltage. **In the default setting, a jumper is plugged between pins 2 and 3 causing the pulse outputs to be at the low (0V) state**.
17	JP9	UARTCSZ	Three-pin header for enabling the UART of the 71M6515H. **In the default setting, a jumper is plugged between pins 2 and 3, causing the UART to be enabled.**
18	D8	INTERRUPT	When the IC is configured to generate interrupts on the IRQZ pin, this LED will blink. IRQZ active (low) will cause the LED to be on.
19	D6	VARS	This LED is activated by the RPUSE output, if RPULSE is selected with JP30 (pins 2 and 3). Alternatively, the LED can be used to display the PULSE4 output, if the jumper on JP30 is between pins 1 and 2.
20	JP18		Multi-purpose test point consisting of a 12X2 header. The pulse outputs, UART signals, DIO pins, interrupt, control signals for baud rate and pulse polarity can be accessed.
21	TP15, TP16	GND	GND test points
22	TP31		Test point for D6 (VARS). When an optical pickup is not used for the VARS or PULSE4 signal, the pulses may be picked up with an electrical connection to TP31.
23	JP30	PULSE4/RPULSE	This 3-pin header allows selection of the source signal for D6 (VARS) with a jumper. **In the default position (pin 2 to 3) the RPULSE pin drives the LED**. When the jumper is plugged between pins 1 and 2, the PULSE4 pin drives the LED.
24	TP30		Test point for D5 (WATTS). When an optical pickup is not used for the WATTS or PULSE3 signal, the pulses may be picked up with an electrical connection to TP30.
25	JP29	PULSE3/WPULSE	This 3-pin header allows selection of the source signal for D5 (WATTS) with a jumper**. In the default position (pin 2 to 3) the WPULSE pin drives the LED**. When the jumper is plugged between pins 1 and 2, the PULSE3 pin drives the LED.
26	D5	WATTS	This LED is activated by the WPULSE output, if WPULSE is selected with JP29 (pins 2 and 3). Alternatively, the LED can be used to display the PULSE3 output, if the jumper on JP29 is between pins 1 and 2.
27	JP21	DEBUG	Connector for the Debug Board. 2x8 pin male header.

Table 3-2: 71M6515H Demo Board Description: 2/3

28	JP32	BAUDRATE	This 3-pin header allows selection of the baud rate for the UART of the 71M6515H. **In the default position (pin 1 to 2), the chip operates at 19.2kbps**. When the jumper is plugged between pins 2 and 3, the chip operates at 38.4kbps.
29	--	--	Serial number field. The serial number of the Demo Board is entered in this field by TERIDIAN.
30	U5	--	The 64-pin socket containing the 71M6515H chip.

Table 3-3: 71M6515H Demo Board Description: 3/3

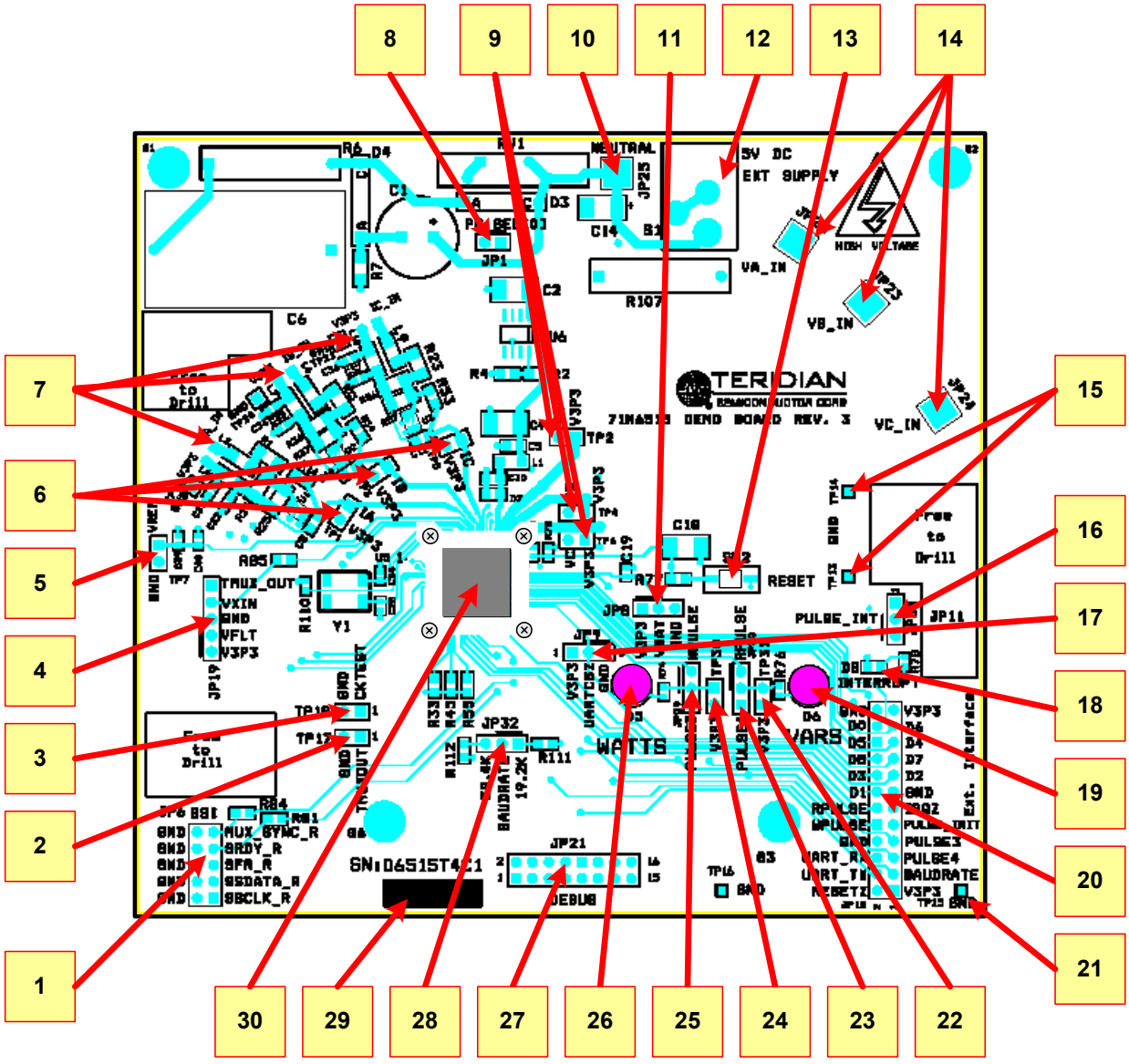


Figure 3-1: 71M6515H Demo Board: Connectors, Headers, LEDs, Switches

3.2 CONNECTOR DESCRIPTIONS

3.2.1 JP6 – SSI INTERFACE

JP6 provides access to the SSI-related pins of the 71M6515H chip via decoupling resistors of 62Ω for each signal. The pin layout for JP6 is shown in Table 3-4.

JP6 Pin	Signal	JP6 Pin	Signal
1	SSCLK	2	ground
3	SSDATA	4	ground
5	SFR	6	ground
7	SRDY	8	ground
9	MUX_SYNC	10	ground

Table 3-4: JP6 Pin Description

3.2.2 JP18 – EXTERNAL INTERFACE

JP18 provides access to the digital I/O pins and to other signals of the 71M6515H chip. The pin layout for JP18 is shown in Table 3-5.

JP18 Pin	Signal		JP18 Pin	Signal		JP18 Pin	Signal
1	V3P3		9	PULSE_INT		17	D7 (DIO)
2	RESETZ		10	WPULSE		18	UARTCSZ
3	BAUDRATE		11	IRQZ		19	D4 (DIO)
4	TX (UART)		12	RPULSE		20	D5 (DIO)
5	PULSE4		13	GND		21	D6 (DIO)
6	RX (UART)		14	D1 (DIO)		22	D0 (DIO)
7	PULSE3		15	D2 (DIO)		23	V3P3
8	GND		16	D3 (DIO)		24	GND

Table 3-5: JP18 Pin Description (pins 3, 5, 7, 9, and 17 are non-functional)

3.2.3 JP21 – DEBUG INTERFACE

JP21 provides the connection to the Debug Board. It carries the UART TX and RX signals needed for the communication with the host. A few other signals are useful for diagnosis and test are provided also. The pin layout for JP21 is shown in Table 3-6.

JP21 Pin	Signal	In-line Resistor		JP21 Pin	Signal	In-line Resistor
1	---	---		2	---	---
3	---	---		4	V3P3	None
5	GND	None		6	CKTEST	62Ω
7	GND	None		8	TMUXOUT	62Ω
9	GND	None		10	TX (UART)	62Ω
11	GND	None		12	RX (UART)	None
13	---	---		14	---	---
15	---	---		16	---	---

Table 3-6: JP21 Pin Description

3.3 BOARD HARDWARE SPECIFICATIONS

PCB Dimensions

- Width 5.125" (130.2mm)
- Length 4.7" (119.4mm)
- Thickness 0.062" (1.6mm)
- Height w/ components and 3/8" spacers 1.5" (38.1mm)

Environmental

- Operating Temperature -40°…+85°C
  (function of crystal oscillator affected outside –10°C to +60°C)
- Storage Temperature -40°…+95°C

Power Supply

- When using AC Input Signal 180V…700V RMS
- DC Input Voltage (powered from DC supply) 5VDC ±0.5V
- Supply Current 25mA typical

Input Signal Range

- AC Voltage Signals (VA, VB, VC) 0…240V RMS
- AC Current Signals (IA, IB, IC) from Transducer 0…250mV p/p

Interface Connectors

- DC Supply Jack (S1) to Wall Transformer Concentric connector, 2.5mm
- Input Signals Spade Terminals and headers on PCB bottom
- Debug Board (JP21) 8x2 Header, 0.1" pitch
- Target Chip (U5) LQFP64 Socket
- External Interface Connector (JP18) 12x2 Header, 0.1" pitch

Functional Specification

- Program Memory 128kByte serial FLASH
- Time Base Frequency 32.768kHz, ±20PPM at 25°C
- Time Base Temperature Coefficient -0.04PPM/°C^2 (max)

Controls and Displays

- Reset Button (SW2)
- "Watts"/"PULSE3" red LED (D5)
- "VARS"/"PULSE4" red LED (D6)
- "INTERRUPT" green LED

Measurement Range

- Voltage 120…700 V rms (resistor division ratio 1:3,398)
- Current 1.7Ω termination for 2,000:1 CT input (200A)

4

4 APPENDIX

71M6515H Demo Board Description

- 71M6515H Demo Board Specifications
- 71M6515H Demo Board Electrical Schematic
- 71M6515H Demo Board Bill of Materials
- 71M6515H Demo Board PCB Silk screen layer – Top side
- 71M6515H Demo Board PCB Silk screen layer – Bottom side
- 71M6515H Demo Board PCB Metal Layer – Top side
- 71M6515H Demo Board PCB Metal Layer – Middle 1, ground plane
- 71M6515H Demo Board PCB Metal Layer – Middle 2, supply plane
- 71M6515H Demo Board PCB Metal Layer – Bottom

Debug Board Description

- Debug Board Electrical Schematic
- Debug Board Bill of Materials
- Debug Board PCB Silk screen layer – Top side
- Debug Board PCB Silk screen layer – Bottom side
- Debug Board PCB Metal Layer – Top side signal layer
- Debug Board PCB Metal Layer – Middle 1, ground plane
- Debug Board PCB Metal Layer – Middle 2, supply plane
- Debug Board PCB Metal Layer – Bottom side signal layer

71M6515H Description

- 71M6515H Pin Description and Pin-out Diagram.

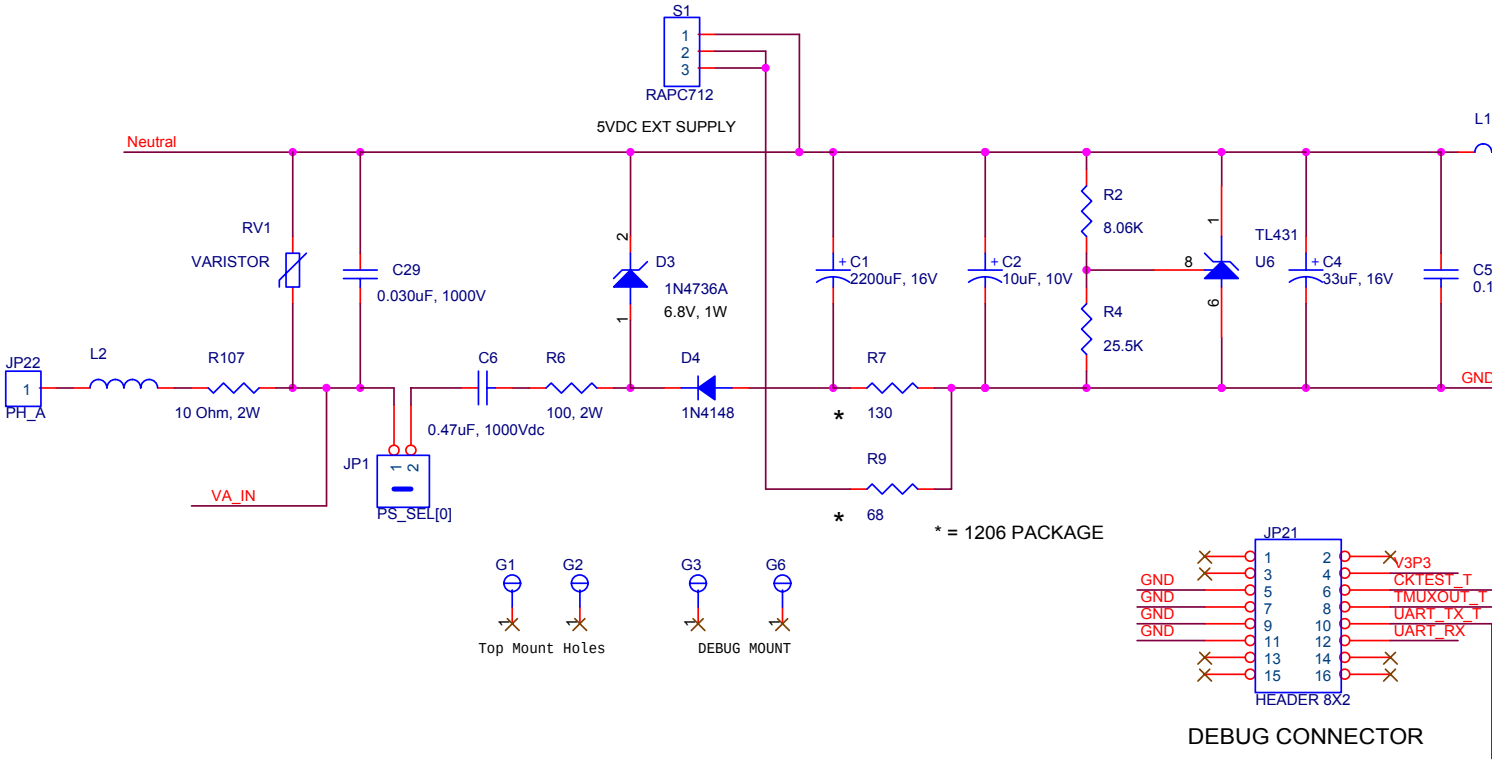


Figure 4-1: TERIDIAN 71M6515H Demo Board: Electrical Schematic 1/3

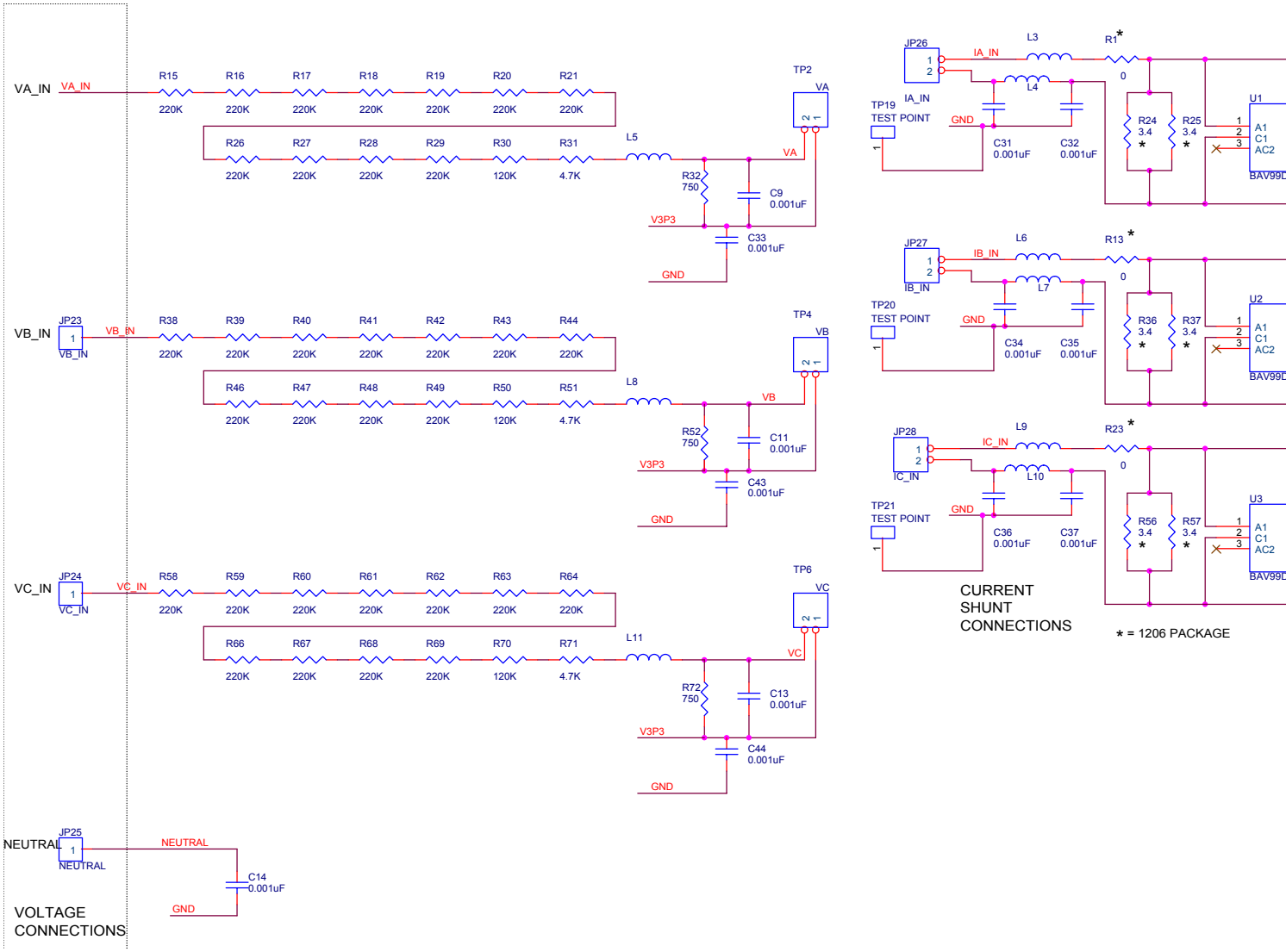


Figure 4-2: TERIDIAN 71M6515H Demo Board: Electrical Schematic 2/3

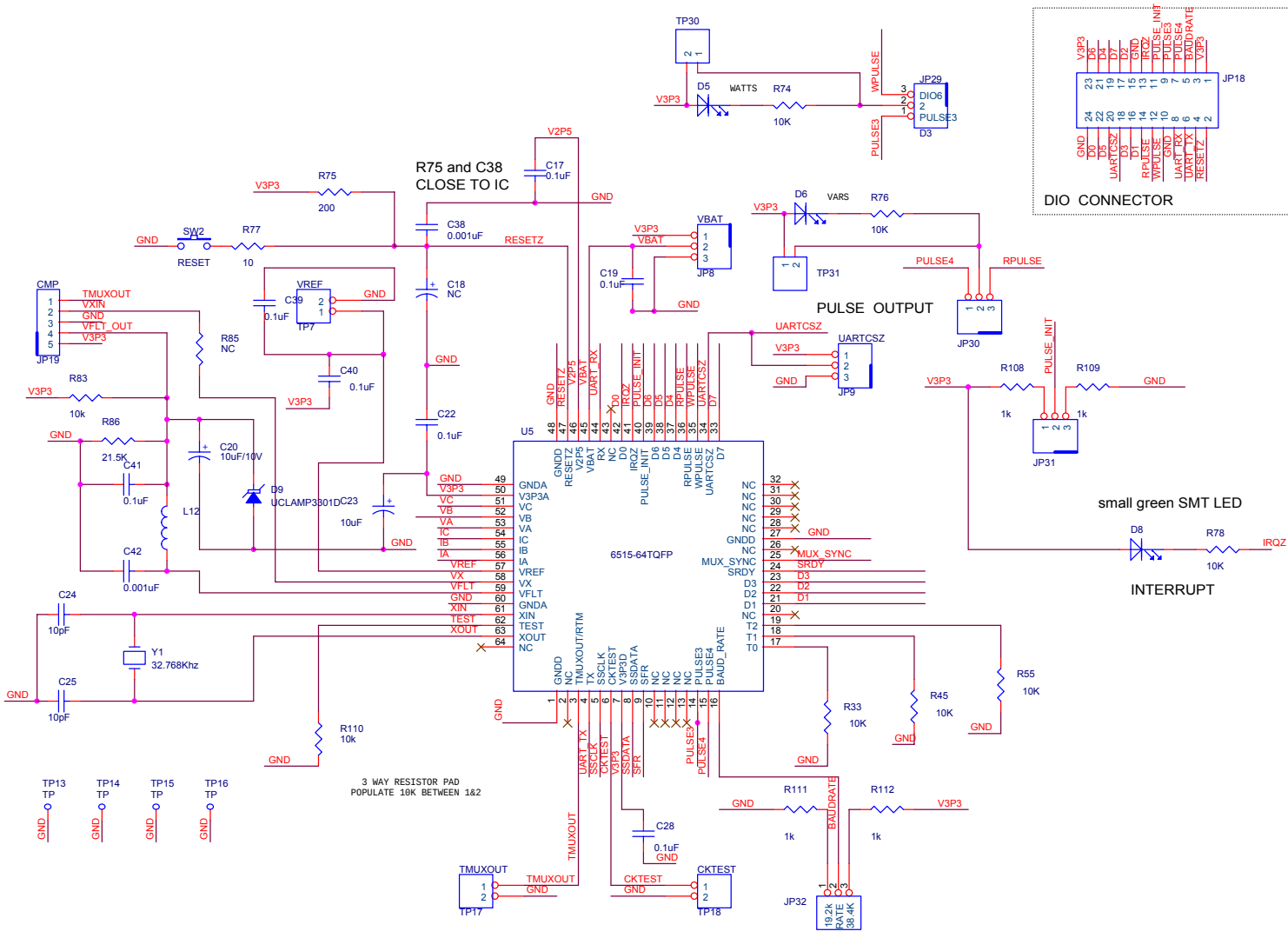


Figure 4-3: TERIDIAN 71M6515H Demo Board: Electrical Schematic 3/3

Item	Q	Reference	Part	PCB Footprint	Digi-Key P/N	Manufacturer P/N	Manufacturer
1	1	C1	2200uF	BULK/Radial	P5143-ND	ECA-1CM222	Panasonic
2	2	C2,C20	10uF	RC1812	478-1672-1-ND	TAJB106K010R	AVX
3	1	C23	10uF	RC0805	PCC1828CT-ND	ECJ-2VB1E104K	Panasonic
4	1	C4	33uF	RC1812	478-1688-1-ND	TAJB336K016R	AVX
5	4	C5,C17,C22,C28	0.1uF	RC0805	445-1349-1-ND	C2012X7R1H104K	TDK
6	1	C6	.47uF	block capacitor	BC1918-ND	222 383 30474	BC Components
7	7	C8-C13,C30	0.001uF,100V	RC0805	445-1337-1-ND	C2012X7R2A102K	TDK
8	2	C14,C18	NC	RC1812	--	--	--
9	4	C19,C39,C40,C41	0.1uF	RC0603	445-1314-1-ND	C1608X7R1H104K	TDK
10	2	C24,C25	10pF	RC0603	445-1269-1-ND	C1608COG1H100D	TDK
11	1	C29	0.03uF, 250V	AXLE	75-125LS30	125LS30	Vishay
12	11	C31-C38,C42-C44	0.001uF	RC0603	445-1298-1-ND	C1608X7R2A102K	TDK
13	1	D3	6.8V ZENER	D041	1N4736ADICT-ND	1N4736A-T	DIODES
14	1	D4	Switching Diode	D035	1N4148DICT-ND	1N4148-T	DIODES
15	1	D5,D6	LED	RADIAL	67-1612-ND	SSL-LX5093SRC/E	LUMEX
16	2	D7,D9	uCLAMP3301d	SOD-323	---	UCLAMP3301D.TCT	SEMTECH
17	1	D8	LED SM (Green)	RC0805	160-1414-1-ND	LTST-C170KGKT	LITEON
18	12	L1-L12	Ferrite, 600 Ohm	RC0805	445-1556-1-ND	MMZ2012S601A	TDK
19	4	JP1,JP26,JP27,JP28	HEADER 2X1	2X1PIN	S1011-36-ND	PZC36SAAN	Sullins
20	1	JP6	HEADER 5X2	5X2PIN	S2011-36-ND	PZC36DAAN	Sullins
21	6	JP8,JP9,JP29-JP32	HEADER 3	3X1PIN	S1011-36-ND	PZC36SAAN	Sullins
22	1	JP18	HEADER 10X2	10X2PIN	S2011-36-ND	PZC36DAAN	Sullins
23	1	JP19	HEADER 5	5X1PIN	S1011-36-ND	PZC36SAAN	Sullins
24	1	JP21	HEADER 8X2	8X2PIN	S2011-36-ND	PZC36DAAN	Sullins
25	4	JP22,JP23,JP24,JP25	spade terminal	spade terminal	A24747CT-ND	62395-1	AMP
26	1	RV1	MOV/Varistor	Radial	581-VZD510XX	VE24M00511K	AVX
27	3	R1,R13,R23	0	RC1206	P0.0ECT-ND	ERJ-8GEY0R00V	Panasonic
28	1	R2	8.06K, 1%	RC0805	311-8.06KCCT-ND	9C08052A8061FKHFT	Yageo
29	1	R4	25.5K, 1%	RC0805	311-25.5KCCT-ND	9C08052A2552FKHFT	Yageo
30	1	R6	100, 2W	AXLE	100W-2-ND	RSF200JB-100R	Yageo
31	1	R7	130, 1%	RC1206	311-130FCT-ND	9C12063A1300FGHFT	Yageo
32	1	R9	68, 1%	RC1206	311-68.0FCT-ND	9C12063A68R0FKHFT	Yageo
33	7	R10,R11,R65,R73,R79,R81,R84	62	RC0805	P62ACT-ND	ERJ-6GEYJ620V	Panasonic
34	1	R12	0	RC0805	P0.0ACT-ND	ERJ-6GEY0R00V	Panasonic
35	6	R14,R32,R34,R52,R53,R72	750, 0.5%	RC0805	RR12P750DCT-ND	RR1220P-751-D	SUSUMU
36	33	R15-R21,R26-R29,R38-R44,	220K, 0.1%	RC0805	RR12P220KBCT-ND	RR0816P-224-B-T5	SUSUMU
		R46-R49,R58-R64,R66-R69					
37	6	R24,R25,R36,R37,R56,R57	3.4, 1%	RC1206	311-3.40FCT-ND	9C12063A3R40FGHFT	Yageo
38	3	R30,R50,R70	120K, 0.1%	RC0805	RR12P120KBCT-ND	RR1220P-124-B-T5	SUSUMU
39	3	R31,R51,R71	4.7K, 0.1%	RC0805	RR12P4.7KBCT-ND	RR1220P-472-B-T5	SUSUMU
40	4	R33,R45,R55,R85	10K	RC0805	P10KACT-ND	ERJ-6GEYJ103V	Panasonic
41	6	R74-R76,R78,R108,R110	10K	RC0603	P10KGCT-ND	ERJ-3GEYJ103V	Panasonic
42	1	R77	10	RC0805	P10ACT-ND	ERJ-6GEYJ100V	Panasonic
43	1	R83	10K, 1%	RC0805	P10.0KCCT-ND	ERJ-6ENF1002V	Panasonic
44	1	R86	21.5K	RC0805	P21.5KCCT-ND	ERJ-6ENF2152V	Panasonic
45	1	R107	10,2W	AXLE	10W-2-ND	RSF200JB-10R	Yageo
46	1	R109	1K	RC0603	P1.0KGCT-ND	ERJ-3GEYJ102V	Panasonic
47	2	R111,R112	1K	RC0805	P1.0KACT-ND	ERJ-6GEYJ102V	Panasonic
48	1	S1	DC connector, 2.5mm	RAPC712	SC1152-ND	RAPC712	Switchcraft
49	1	SW2	PB Switch		P8051SCT-ND	EVQ-PJX05M	Panasonic
50	11	TP1-TP7,TP17,TP18,TP30,TP31	HEADER 2X1	2X1PIN	S1011-36-ND	PZC36SAAN	Sullins
51	4	TP13-TP14,TP15-TP16	TP	test point	5011K-ND	5011	Keystone
52	3	TP19,TP20,TP21	HEADER 1X1	1X1PIN	S1011-36-ND	PZC36SAAN	Sullins
53	3	U1,U2,U3	BAV99DW	SOT363	BAV99DW-FDICT-ND	BAV99DW-7-F	DIODES
54	1	U5	71M6515H	64TQFP	--	71M6515H-IGT	TERIDIAN
55	1	at U5	64TQFP SOCKET	64TQFP	--	IC149-064-169-S5	YAMAICHI
56	1	U6	TL431AIDR	SO8	296-1288-1-ND	TL431AIDR	Texas Instruments
57	1	Y1	32.768KHz	SMT quartz	XC488CT-ND	ECS-.327-12.5-17-TR	ECS

Table 4-1: 71M6515H Demo Board: Bill of Material

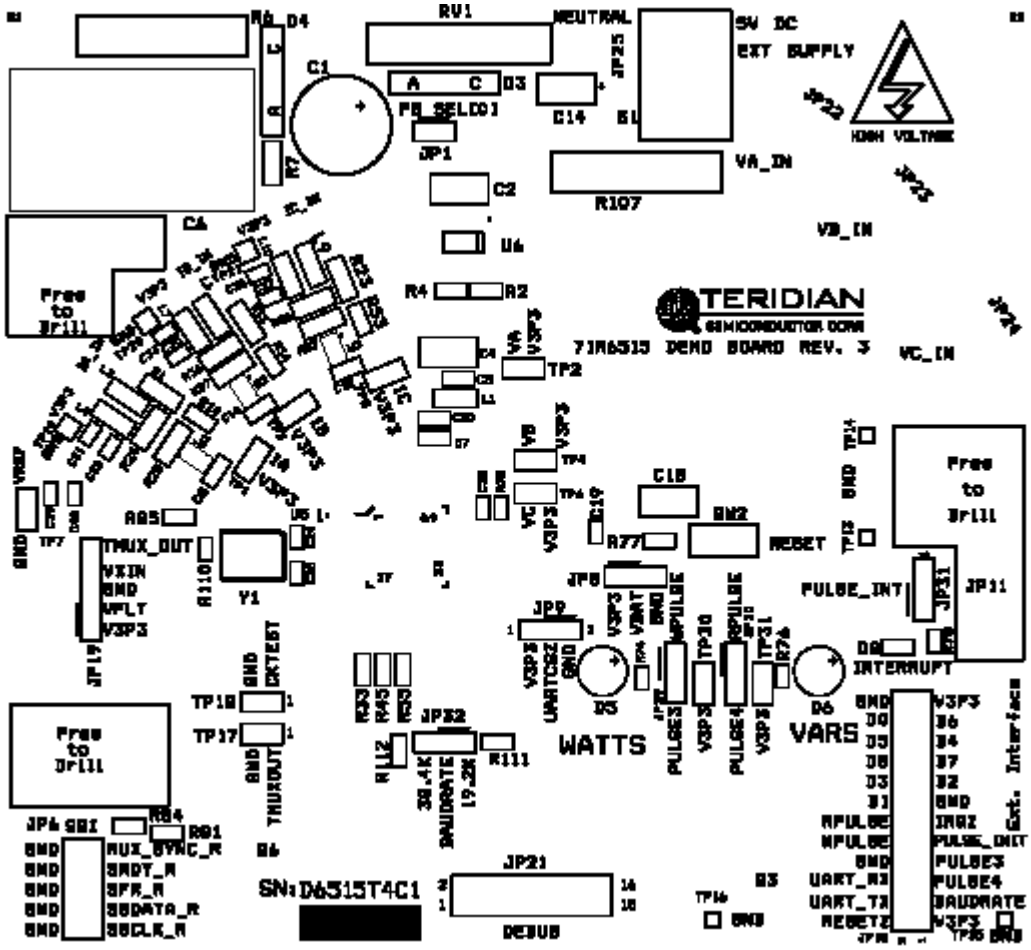


Figure 4-4: TERIDIAN 71M6515H Demo Board: Top View

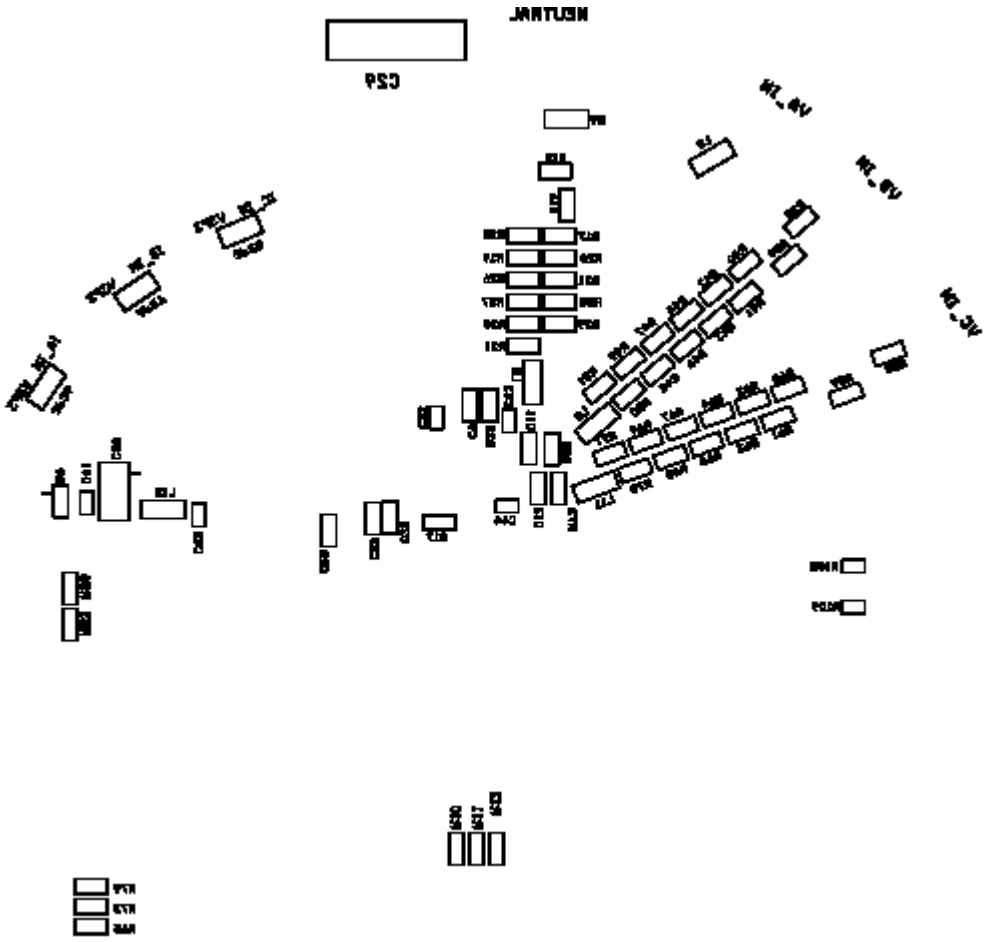


Figure 4-5: TERIDIAN 71M6515H Demo Board: Bottom View

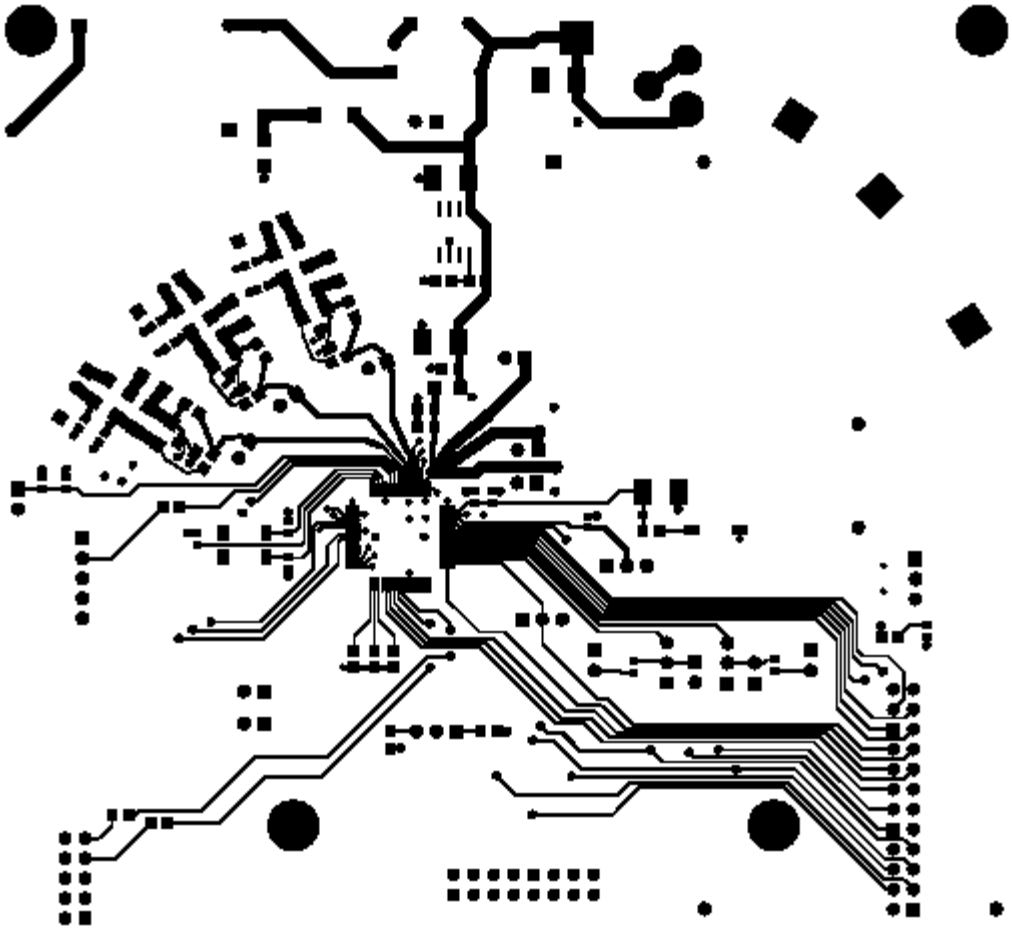


Figure 4-6: TERIDIAN 71M6515H Demo Board: Top Signal Layer

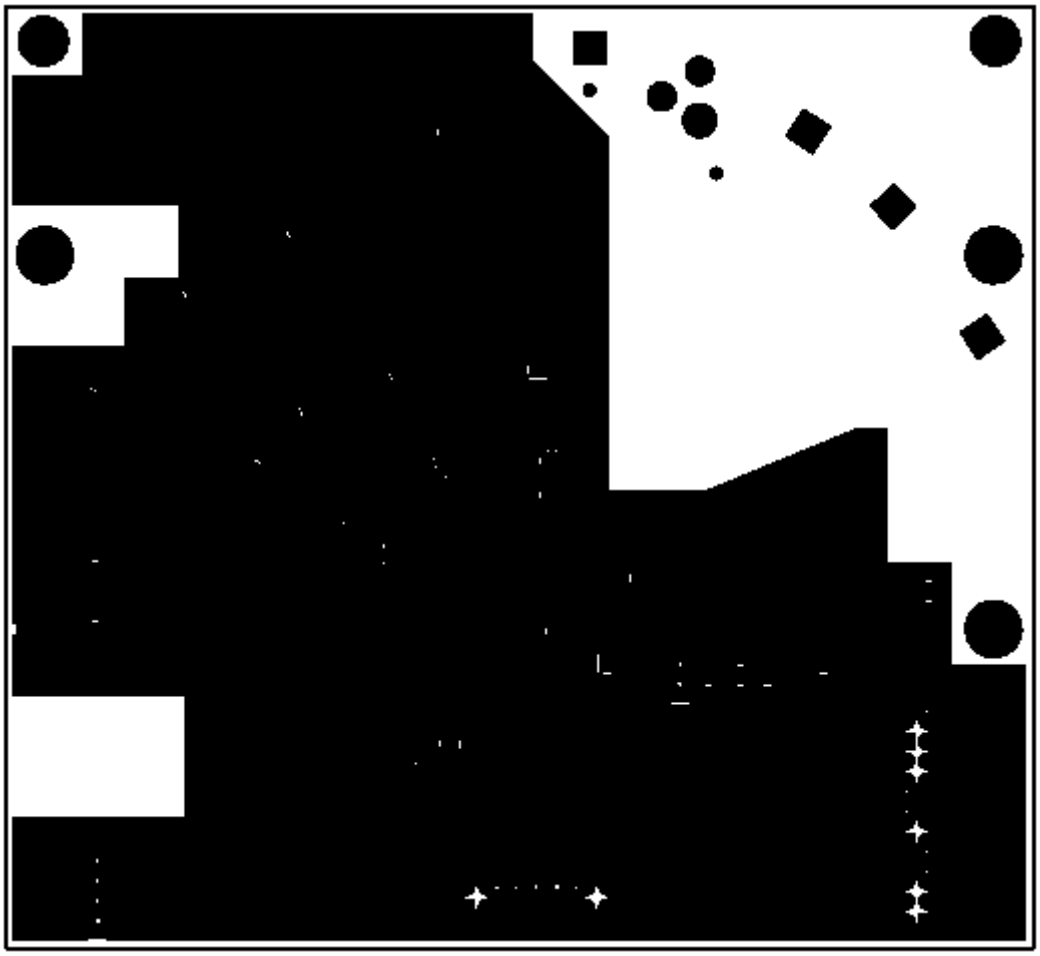


Figure 4-7: TERIDIAN 71M6515H Demo Board: Middle Layer 1, Ground Plane.

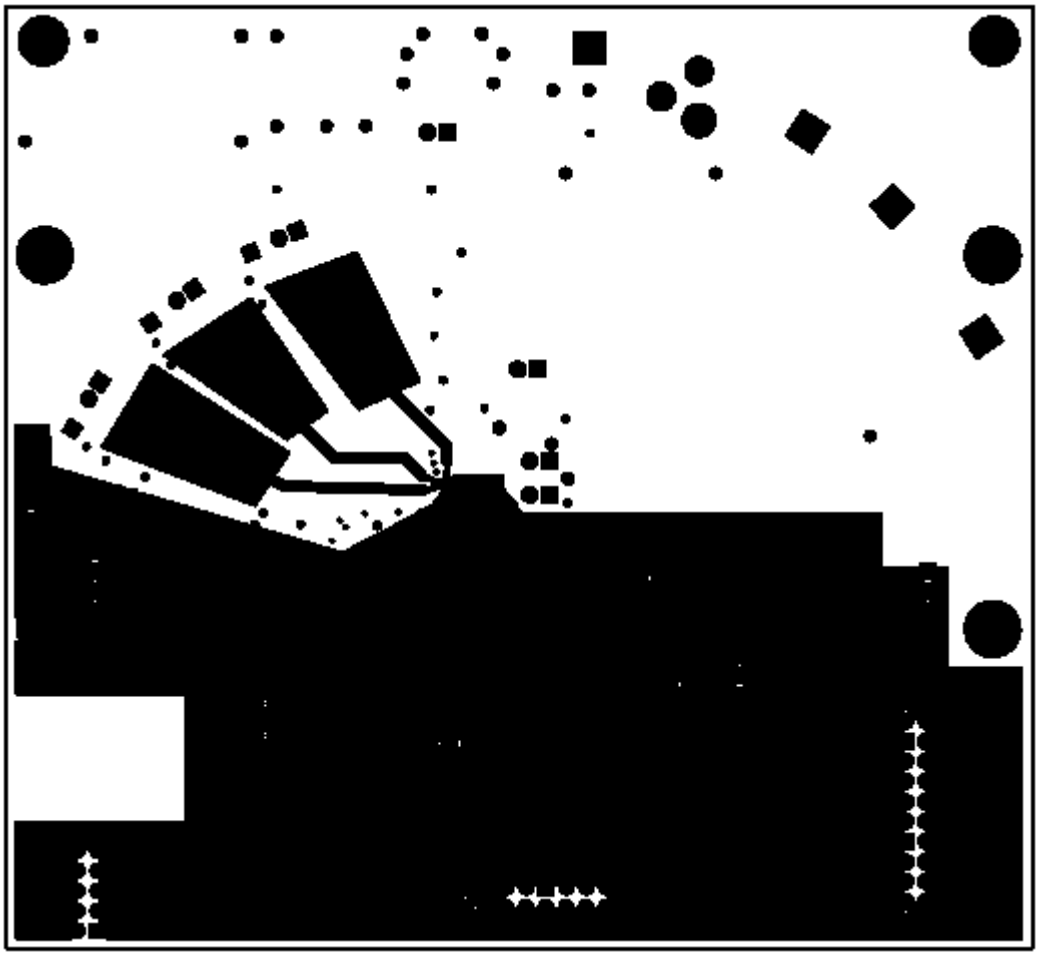


Figure 4-8: TERIDIAN 71M6515H Demo Board: Middle Layer 2, Supply Plane.

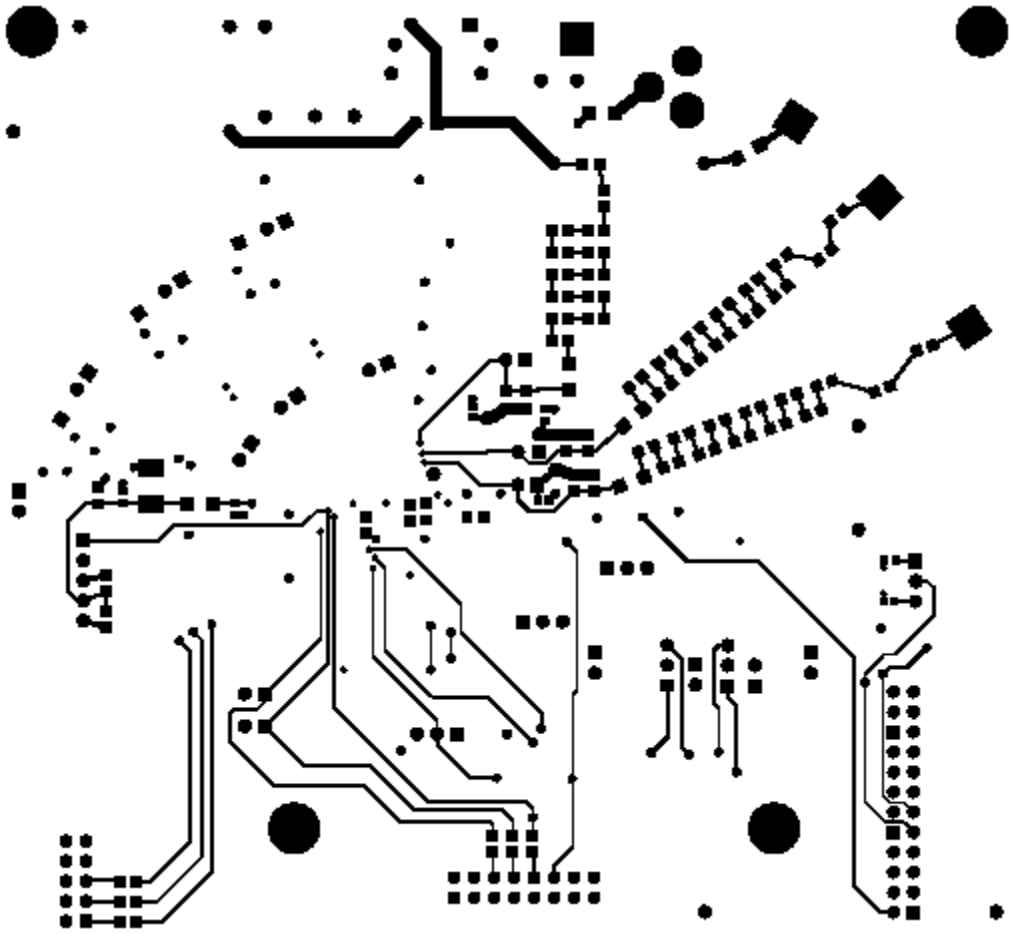


Figure 4-9: TERIDIAN 71M6515H Demo Board: Bottom Signal Layer

Item	Quantity	Reference	Part	PCB Footprint	Digi-Key Part Number	Part Number
1	21	C1-C3,C5-C10,C12-C23	0.1uF	RC0805	445-1349-1-ND	C2012X7R1H104K
2	1	C4	33uF, 10V	RC1812	478-1687-1-ND	TAJB336K010R
3	1	C11	10uF, 16V	RC1812	478-1673-1-ND	TAJB106K016R
4	2	D2,D3	LED	RC0805	160-1414-1-ND	LTST-C170KGKT
5	4	G1,G2,G3,G4	Spacer	MTHOLE	2202K-ND	2202K-ND
6	4		4-40, 1/4" screw		H342-ND	PMS 4400 - 0025 PH
7	2		4-40, 5/16" screw		H343-ND	PMS 4400- 0031 PH
8	2		4-40 nut		H216-ND	HNZ440
9	1	J1	DC Connector	RAPC712	SC1152-ND	RAPC712
10	1	J2	DB9, right angle	DSUB9_SKT	A2100-ND	745781-4
11	1	J3	HEADER (F) 8X2	8X2PIN	929852-01-36-ND	929852-01-36-10
12	4	JP1,JP2,JP3,JP4	HEADER 2	2X1PIN	S1011-36-ND	PZC36SAAN
13	4	R1,R5,R7,R8	10K	RC0805	P10KACT-ND	ERJ-6GEYJ103V
14	2	R2,R3	1K	RC0805	P1.0KACT-ND	ERJ-6GEYJ102V
15	1	R4	NC	RC0805	N/A	N/A
16	1	R6	0	RC0805	P0.0ACT-ND	ERJ-6GEY0R00V
17	1	SW2	PB switch		P8051SCT-ND	EVQ-PJX05M
18	5	U1,U2,U3,U5,U6	ISOLATOR	SOIC8	ADUM1100AR-ND	ADUM1100AR
19	2	TP5,TP6	Test Point	--	5011K-ND	5011
20	1	U4	RS232 DRIVER	28SSOP	MAX3237CAI-ND	MAX3237CAI

Table 4-2: Debug Board: Bill of Material

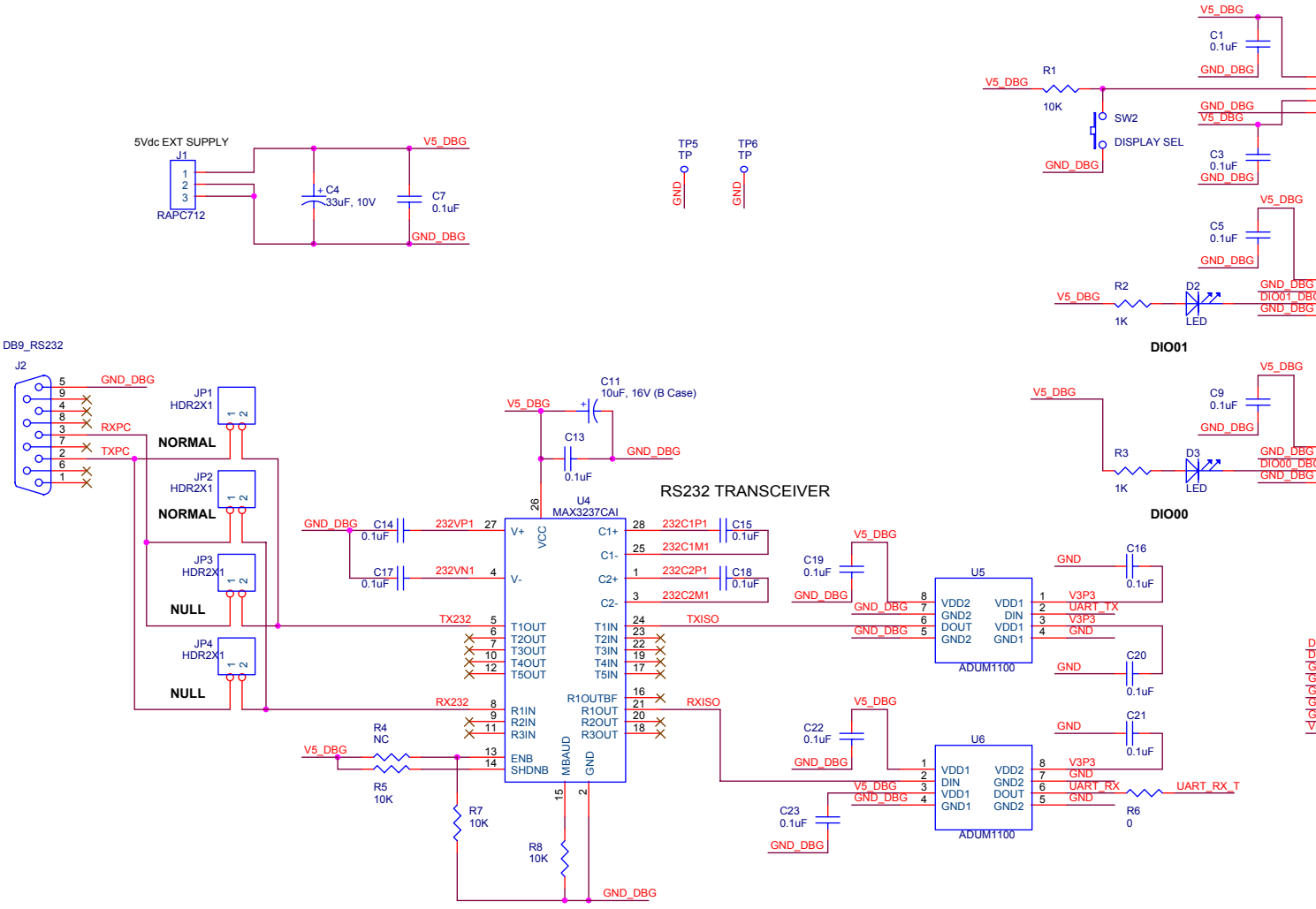


Figure 4-10: Debug Board Schematics

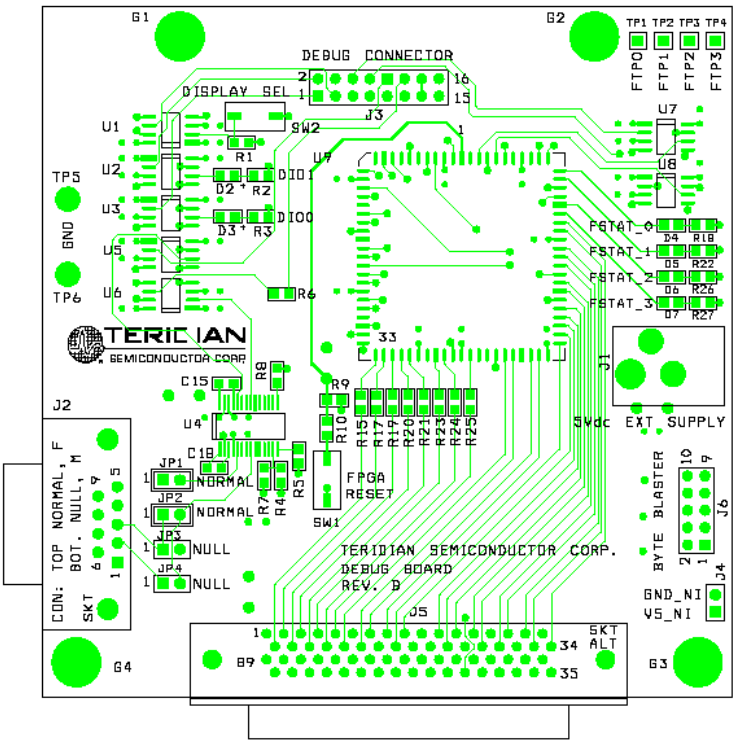


Figure 4-11: Debug Board: Top View

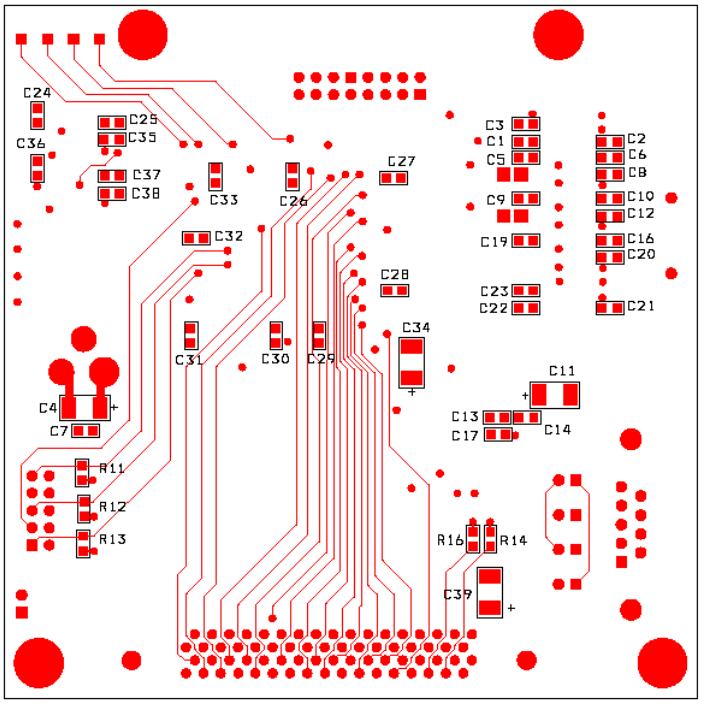


Figure 4-12: Debug Board: Bottom View

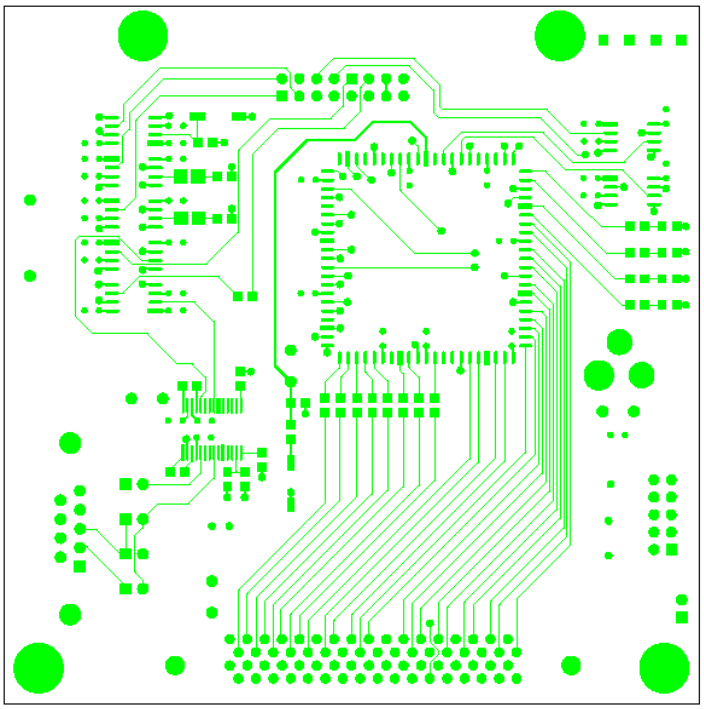


Figure 4-13: Debug Board: Top Signal Layer

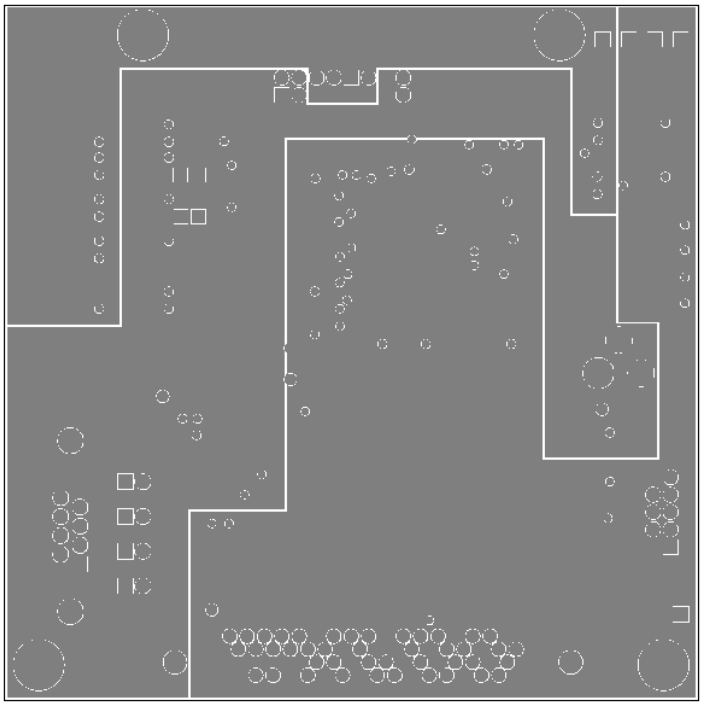


Figure 4-14: Debug Board: Middle Layer 1, Ground Plane

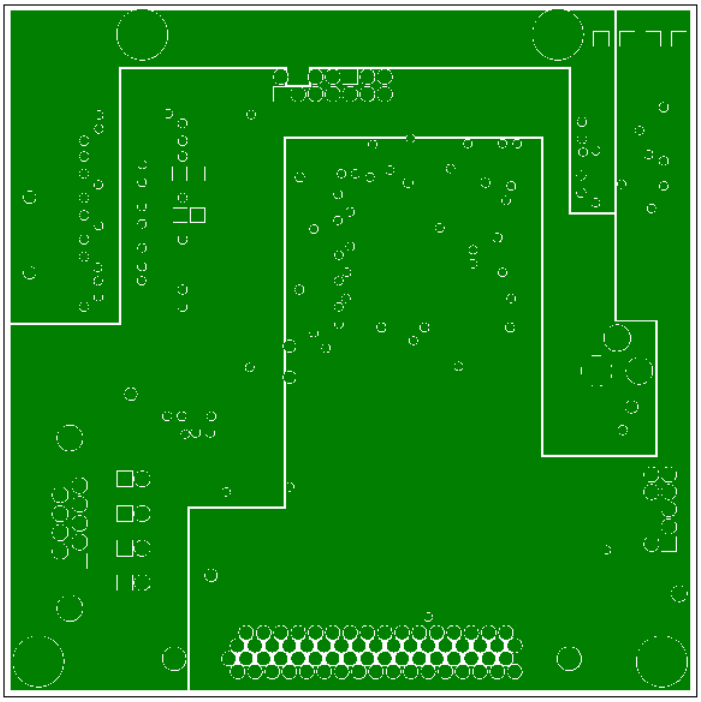


Figure 4-15: Debug Board: Middle Layer 2, Supply Plane

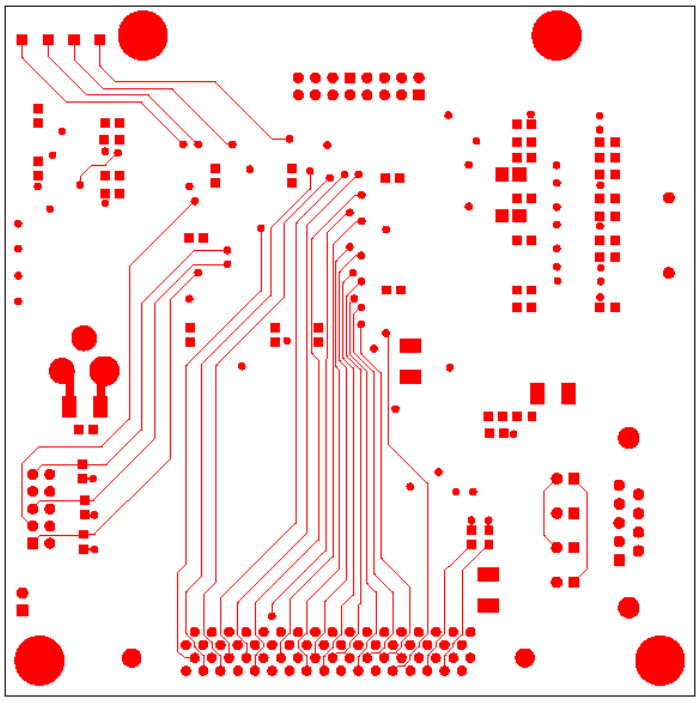


Figure 4-16: Debug Board: Bottom Trace Layer

Power/Ground Pin Description

Name	Pin No.	Type	Description
GNDA	49,60	P	Analog ground: This pin should be connected directly to the ground plane.
GNDD	1,27, 48,62	P	Digital ground: These pins must be connected directly to the ground plane.
V3P3A	50	P	Analog power: A 3.3V analog power supply should be connected to this pin.
V3P3D	7	P	Digital power supply: A 3.3V digital power supply should be connected to this pin.
VBAT	45	P	Battery backup power supply. A battery or super-capacitor is to be connected between VBAT and GNDD. If no battery is used, connect VBAT to V3P3D.
V2P5	46	O	Output of the 2.5V regulator. A 0.1µF capacitor should be connected to this pin.

Analog Pin Description

Name	Pin No.	Type	Description
IA, IB, IC	56,55,54	I	Line Current Sense Inputs: Voltage inputs to the internal A/D converter. Typically, they are connected to the output of a current transformer. The input is referenced to V3P3A
VA, VB, VC	53,52,51	I	Line Voltage Sense Inputs: Voltage inputs to the internal A/D converter. Typically, they are connected to the output of a resistor divider. The input is referenced to V3P3A
VFLT	59	I	Power Fault Input.
VX	58	I	Auxiliary input.
VREF	57	I/O	Voltage Reference for the ADC.
XIN, XOUT	61,63	I	Crystal Inputs: A 32768Hz crystal should be connected across these pins. Typically, a 10pF capacitor is also connected from each pin to GNDA. See the datasheet of the crystal manufacturer for details.

Table 4-3: 71M6515H Pin Description Table 1/2

Digital Pin Description - Pins labeled RESERVED are not to be connected. Unless otherwise indicated, all inputs and outputs are standard CMOS. Inputs do NOT have internal pull-ups or pull-downs.

Name	Pin No.	Type	Description
CKTEST	6	I/O	Clock PLL output. Can be enabled and disabled by *CKOUT_DSB* (see Status Mask).
D0 to D7	42,21…23, 37…39,33	I/O	Input/output pins 0 through 7. These pins should not be floated if configured as input pins.
PULSE4	15	O	The fourth pulse generator output
PULSE3	14	O	The third pulse generator output
PULSE_INIT	40	I	The pulse output initial power-up voltage
BAUD_RATE	16	I	The UART baud rate (1: 38.4kbd, 0: 19.2kbd)
IRQZ	41	O	Interrupt output, low active. A falling edge indicates the end of a measurement frame, as well as alarms. Rises when status word is read.
MUXSYNC	25	O	Falls at beginning of conversion cycle for IA.
RESETZ	47	I	Chip reset: Input pin with internal pull-up resistor, used to reset the chip into a known state. For normal operation, this pin is set to 1. To reset the chip, this pin is driven to 0 for 5 microseconds.
UARTCSZ	34	I	Enables the UART when 0. The UART is disabled when this pin is set to 1. A positive pulse on this pin will reset the UART. No external reset circuitry is necessary for power-up reset.
SRDY SFR SSCLK SSDATA	24 9 5 8	I O O O	High-Speed Synchronous Interface (SSI). If SRDY is not used, it should be tied low. SSI optional handshake input. SSI frame pulse output, one SSCLK wide. SSI clock output (5MHz or 10MHz selectable). SSI data output, changes on the rising edge of SSCLK.
RX TX	44 4	I O	UART serial Interface receiver input. UART serial Interface transmitter output.
RESERVED	2,10,11,12, 13,17,18,19, 20,26,28,29, 30,31,32,43, 64	N/A	These pins must not be connected
TMUXOUT	3	O	Digital output test multiplexer. Controlled by *TMUX[2:0]*.
RPULSE WPULSE	36 35	O O	Selectable pulse output (default: VARh pulse). Selectable pulse output (default: Wh pulse).

Table 4-4: 71M6515H Pin Description Table 2/2

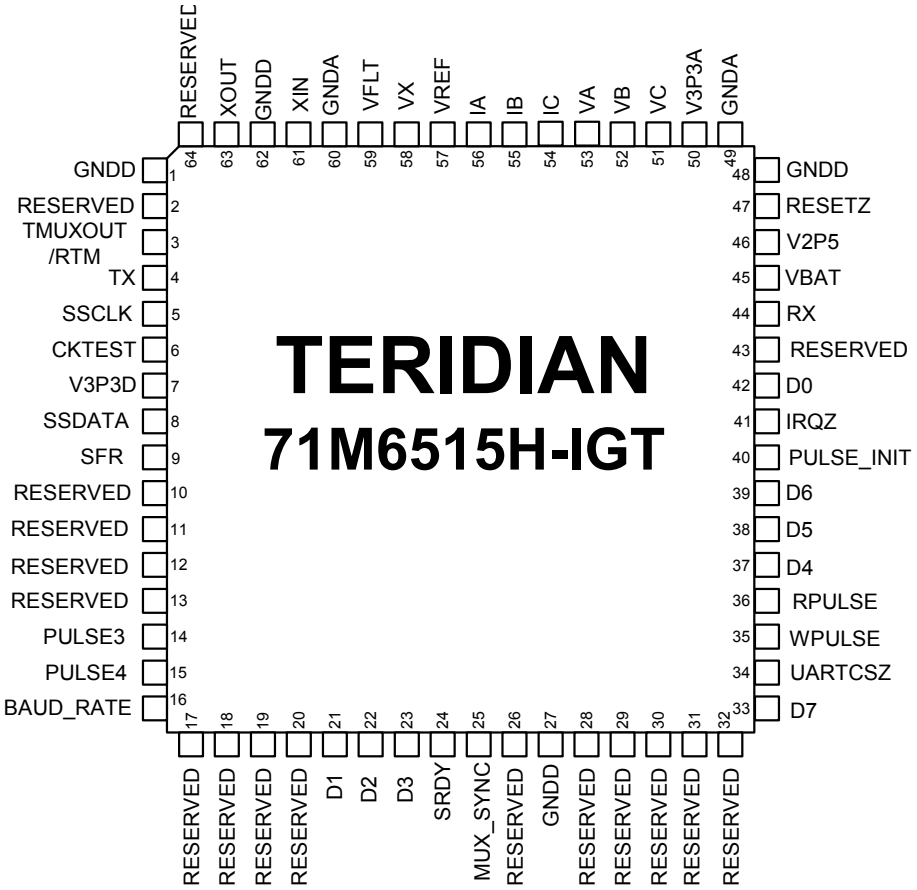


Figure 4-17: TERIDIAN 71M6515H LQFP64: Pinout (top view)

Note: Pins labeled as RESERVED must not be connected.

User's Manual: This User's Manual contains proprietary product definition information of TERIDIAN Semiconductor Corporation (TSC) and is made available for informational purposes only. TERIDIAN assumes no obligation regarding future manufacture, unless agreed to in writing.

If and when manufactured and sold, this product is sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement and limitation of liability. TERIDIAN Semiconductor Corporation (TSC) reserves the right to make changes in specifications at any time without notice. Accordingly, the reader is cautioned to verify that a data sheet is current before placing orders. TSC assumes no liability for applications assistance.

TERIDIAN Semiconductor Corp., 6440 Oak Canyon Rd., Irvine, CA 92618-5201
TEL (714) 508-8800, FAX (714) 508-8877, http://www.teridian.com

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Data Conversion IC Development Tools ***category:***

Click to view products by Maxim ***manufacturer:***

Other Similar products are found below :

EVAL-AD7265EDZ EVAL-AD7719EBZ EVAL-AD7767-1EDZ EVAL-AD7995EBZ AD9211-200EBZ AD9251-20EBZ AD9251-65EBZ AD9613-170EBZ AD9629-20EBZ AD9716-DPG2-EBZ AD9737A-EBZ AD9993-EBZ DAC8555EVM EVAL-AD5061EBZ EVAL-AD5062EBZ EVAL-AD5443-DBRDZ EVAL-AD5570SDZ EVAL-AD7992EBZ EVAL-AD7994EBZ AD9119-MIX-EBZ AD9233-125EBZ AD9629-80EBZ AD9650-80EBZ AD9767-EBZ DAC8531EVM LM96080EB/NOPB EVAL-AD5445SDZ EVAL-AD5660EBZ EVAL-AD7685SDZ EVAL-AD7687SDZ MAX5318PMB# MAX1246EVL11-QSOP MAX117EVKIT-DIP DC2365A-C DC2795A-B DC2795A-A DAC088S085EB/NOPB SIM8909-EVB-KIT 82635ASRCDVKHV 961443 DC1466B-B EVAL-AD5413SDZ ADC12D1600RB/NOPB 1083 RFPDK FOR CMT2X5X TS7003DB TSC2014EVM-PDK MOD-USB3G KDC5514EVALZ 650201392G ISL28005FH-100EVAL1Z