19-5361; Rev 7/11

A Maxim Integrated Products Brand

71M6515H Energy Meter IC

DATA SHEET

JULY 2011

GENERAL DESCRIPTION

The 71M6515H is a high-accuracy analog front-end (AFE) IC that provides measurements for 3-quadrant 3-phase metering. The combination of a 21-bit sigma-delta A/D converter with a six-input analog front-end, a thermally compensated high-precision reference, and a compute engine results in high accuracy and wide dynamic range. Our Single Converter Technology® reduces cross talk and cost. This IC also provides RTC and battery backup for time-of-use (TOU) metering.

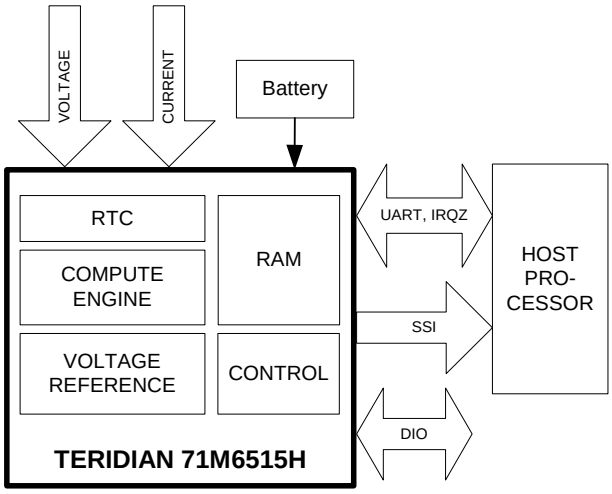


Figure 1: Meter Block Diagram

As shown in the block diagram (Figure 1), the host processor communicates with the 71M6515H through a UART interface using the programmable IRQZ interrupt. The 71M6515H calculates and accumulates meter measurements for each accumulation interval. A high-speed synchronous serial port (SSI) is provided to facilitate high-end metering. Integrated rectifying functions on the battery-backup circuit enable minimal external component usage and minimum back-up current. Also, eight multipurpose pins are provided for control of peripherals.

Single Converter Technology is a registered trademark of Maxim Integrated Products, Inc.

FEATURES

High Accuracy

- < 0.1% Wh accuracy over 2000:1 range
- Exceeds IEC 62053/ANSIC 12.20 specifications
- Up to 10ppm/°C precision ultra-stable voltage reference
- Single Converter Technology reduces cross talk and power consumption
- Six sensor inputs—referenced to V3P3
- Compatible with CTs, resistive shunts and Rogowski Coil sensors
- Digital temperature compensation
- Sag detection
- Measures Wh, VARh, VAh, Vrms, Irms, V-to-V phase and load angle on each phase
- Four-quadrant metering.
- Four low-jitter pulse outputs from selectable measurements
- Four pulse count registers
- Selectable default status for pulse pins
- Same calibration data for 46Hz to 64Hz line frequency
- Broad CT phase compensation (±7deg)

Battery Backup

- Powers real-time clock during power supply outage
- Compatible with Li-ion, NiCd, or super capacitor
- Battery backup current 2µA typical at 25°C

External Data Interface

- UART control interface, two selectable data rates
- 8 general-purpose I/O pins with alarm capability
- 5 or 10MHz selectable high-speed synchronous serial output for DSP interface
- IRQ output signal for alarms and end of measurement intervals
- Alarms on voltage sag, overvoltage, overcurrent

Low System Cost

- Power consumption 30mW at 3.3V typical
- Real-time clock with temperature compensation
- Built-in power-fault detection
- Single 32kHz crystal time base
- Single-supply operation (3.3V)
- 64-lead LQFP package

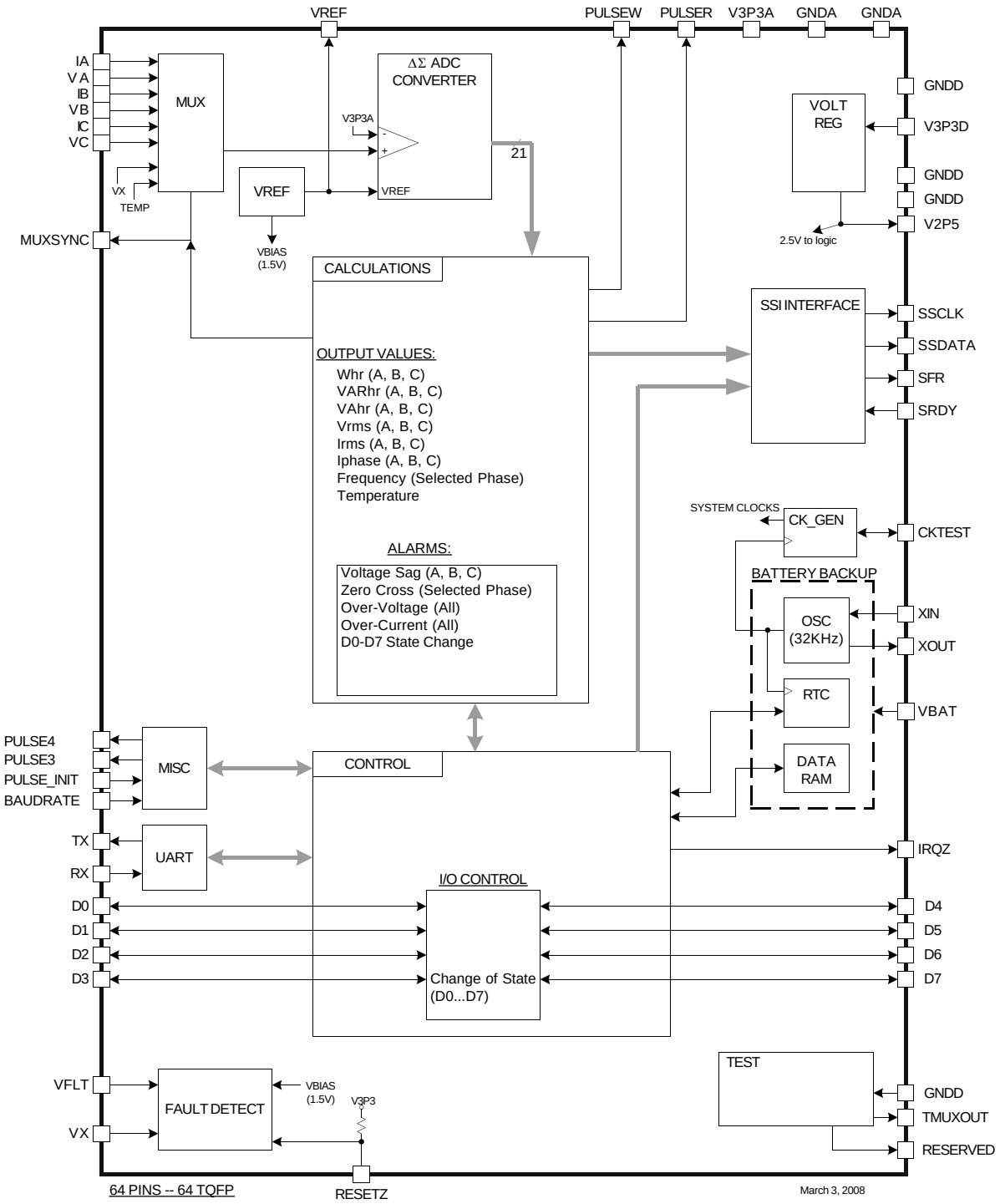


Figure 2: IC Functional Block Diagram

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supplies and Ground Pins:	
V3P3D, V3P3A	–0.5V to 4.6V
|V3P3D – V3P3A|	0V to 0.5V
VBAT	-0.5V to 4.6V
GNDD	-0.5V to +0.5V
Analog Output Pins:	
VREF	-1mA to 1mA, -0.5V to V3P3A+0.5V
V2P5	-1mA to 1mA, -0.5 to 3.0V
Analog Input Pins:	
IA, VA, IB, VB, IC, VC	-0.5V to V3P3A+1.0V
VFLT, VX	-0.5V to V3P3A+0.5V
XIN, XOUT	-0.5V to 3.0V
Digital Input Pins:	
RX	-0.5V to 3.6V
D0…D7	-0.5V to 6V
All other pins	-0.5V to V3P3D+0.5V
Operating junction temperature (peak, 100ms)	140 °C
Operating junction temperature (continuous)	125 °C
Storage temperature	–45 °C to 165 °C
Solder temperature – 10 second duration	250 °C
ESD Stress	
Pins IA, VA, IB, VB, IC, VC, RX, TX	6kV
All other pins	2kV

Stresses beyond Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GNDA.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
3.3V Supply Voltage (**V3P3A, V3P3D**)[+]	Normal Operation	3.0	3.3	3.6	V
	Battery Backup	0		3.8	V
VBAT	No Battery	Externally Connect to V3P3D			
	Battery Backup	2.0		3.8	V
Operating Temperature		-40		85	ºC

[+] V3P3A and V3P3D should be shorted together on the circuit board. GNDD and GNDA should also be shorted on the circuit board.

LOGIC LEVELS

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Digital high-level input voltage, V_{IH}		2		V3P3D	V
Digital low-level input voltage, V_{IL}		–0.3		0.8	V
Digital high-level output voltage V_{OH}	I_{LOAD} = 1mA	V3P3D –0.4		V3P3D	V
	I_{LOAD} = 15mA	V3P3D-0.6[1]			V
Digital low-level output voltage V_{OL}	I_{LOAD} = 1mA	0		0.4	V
	I_{LOAD} = 15mA			0.8[1]	V
Input pull-up current, I_{IL}	VIN=0V				
RESETZ		10		100	µA
E_RXTX, E_ISYNC/BRKRQ		10		100	µA
E_RST		10		100	µA
Other digital inputs		-1		+1	µA
Input pull down current, I_{IH}	VIN=V3P3D				
TEST		10		100	µA
Other digital inputs		-1		+1	µA

[1] Guaranteed by design; not production tested.

SUPPLY CURRENT

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V3P3A + V3P3D	Normal Operation, **V3P3A=V3P3D**=3.3V VBAT=3.6V		8.8	11.5	mA
V3P3A current			3.7	4.7	mA
V3P3D current			5.1	6.8	mA
VBAT current		-300		300	nA
VBAT current, VBAT=3.6V	Battery backup, ≤25°C **V3P3A=V3P3D**=0V f_{OSC} = 32kHz		2	4	µA
	85°C		4	12[1]	µA

[1] Guaranteed by design; not production tested.

VREF

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
VREF output voltage, VNOM(25)	Ta = 25ºC	1.193	1.195	1.197	V
VREF output impedance	I_{LOAD} = 10µA, -10µA			2.5	kΩ
VNOM definition [2]	VNOM(T) = VREF(22) + (T-22)TC1 + (T-22)^{2}TC2				V
VREF(T) deviation from VNOM(T) $\frac{VREF(T)-VNOM(T)}{VNOM}\frac{10^6}{\max(\lvert T-22\rvert,40)}$	Ta = -40ºC to +85ºC, for 71M6515H-IGT/F	-10[1]		+10[1]	PPM/ºC
	Ta = -40ºC to +85ºC, for 71M6515H-IGTW/F	-40[1]		+40[1]	PPM/ºC
VREF aging			±25		PPM/year

[1] Guaranteed by design; not production tested.

[2] This relationship describes the nominal behavior of VREF at different temperatures. The values of TC1 and TC2 are device specific in general and are programmed into the device at manufacturing.

2.5V VOLTAGE REGULATOR

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Voltage Overhead **V3P3D-V2P5**	Reduce V3P3 until V2P5 drops 200mV			440	mV
PSRR **ΔV2P5/ΔV3P3D**	**RESETZ**=1, I_{LOAD}=0	-3		+3	mV/V

RTC

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Range for date		2000	--	2255	year

RESETZ

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Reset pulse width		5			µs
Reset pulse fall time				1[1]	µs

[1] Guaranteed by design; not production tested.

CRYSTAL OSCILLATOR

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Maximum Output Power to Crystal[4]				1	µW
Xin to Xout Capacitance			3		pF
Capacitance to DGND Xin Xout			 5 5		 pF pF
Watchdog RTC_OK threshold				25	kHz

TEMPERATURE SENSOR

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Nominal Sensitivity (S_n)[4]	T_A=25ºC, T_A=85ºC Nominal relationship: $N(T)= S_n*T+N_n$		-900		LSB/ºC
Nominal Offset (N_n)[4]			40000 0		LSB
Temperature Error, relative to 25ºC error $ERR = (T-25) - \frac{(N(T)-N(25))}{S_n}$	T_A = -40ºC to +85ºC	-3[1]		+3[1]	ºC

[1] Guaranteed by design; not production tested.

PULSE GENERATOR TIMING SPECIFICATIONS

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
PULSEW, PULSER maximum rate	APULSE=2^{31}-1, WRATE=2^{15}-1			7.56	kHz
PULSE3, PULSE4 maximum rate	PULSE3=2^{31}-1, WRATE=2^{15}-1			0.15	kHz
Pulse count frequency	all pulse outputs			0.15	kHz

THERMAL CHARACTERISTICS

PARAMETER	CONDITION	VALUE	UNIT
Thermal resistance, junction to ambient ($R\theta_{JA}$)	Air velocity 0 m/s. Part soldered to PCB.	63.7	°C/W

UART HOST INTERFACE

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Baud Rate		19.2	-	38.4	kBaud
Character set			binary		
Data Format			8N1		
Byte-to-byte delay (6515H times out after maximum delay)	Host sending data to 6515H	10		20	ms
Byte-to-byte delay	6515H sending data to host	0		0.1	ms
Response time to read command	6515H has data ready	0.5		2	ms
Response time to read command when 71M6515H is post-processing data	Data not ready *CE_ONLY* = 1 *CE_ONLY* = 0 and *VAH_SELECT* = 0 *CE_ONLY* = 0 and *VAH_SELECT* = 1			40 80 350	ms ms ms

ADC CONVERTER, V3P3 REFERENCED

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Usable Input Range (Vin-**V3P3A**)		-250		250	mV peak
Voltage to Current cross talk: $\frac{10^6 * Vcrosstalk}{Vin}\cos(\angle Vin - \angle Vcrosstalk)$	*Vin* = 200mV peak, 65Hz, on VA, VB, or VC *Vcrosstalk* = largest measurement on IA, IB, or IC	-10^1		$+10^1$	µV/V
THD (First 10 harmonics) 250mV-pk 20mV-pk	Vin=65Hz, 64kpts FFT, Blackman-Harris window		 -75 -90		 dB dB
Input Impedance	Vin=65Hz	40		90	kΩ

Temperature Coefficient of Input Impedance	Vin=65Hz		1.7		Ω/°C
LSB size			355		nV/LSB
Digital Full Scale			±884736		LSB
ADC Gain Error vs. %Power Supply Variation $\frac{10^6 \Delta Nout_{PK}\ 357nV/V_{IN}}{100 \Delta V3P3A/3.3}$	Vin=200mV pk, 65Hz V3P3A=3.0V, 3.6V			50	PPM/ %
Input Offset (Vin-**V3P3A**)		-10		+10	mV

[1] Guaranteed by design; not production tested.

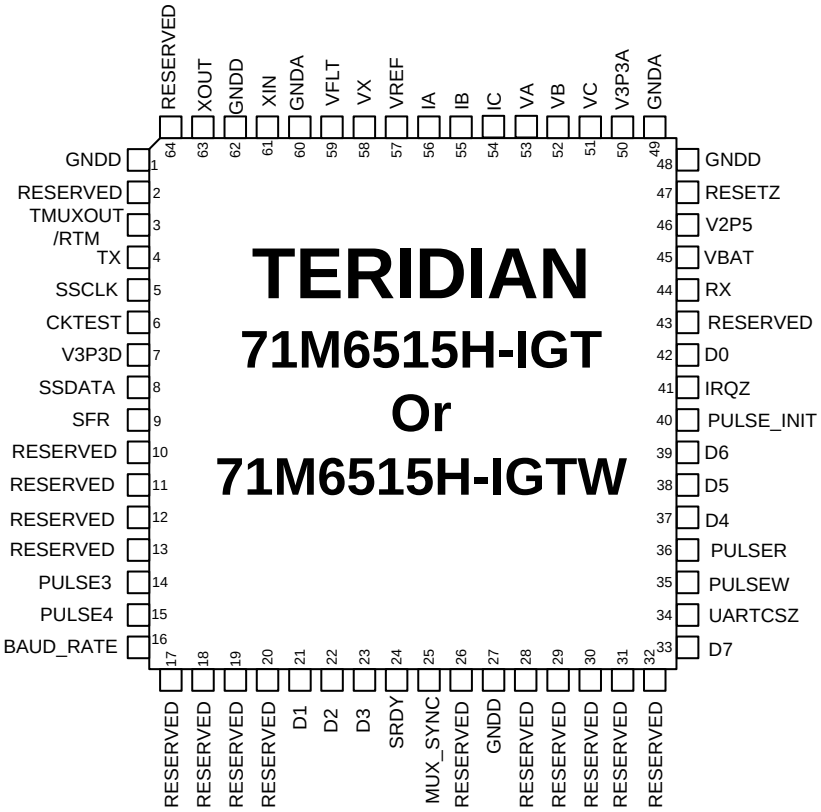
RECOMMENDED EXTERNAL COMPONENTS

NAME	FROM	TO	FUNCTION	VALUE	UNIT
C1	**V3P3A**	**AGND**	Bypass capacitor for 3.3V supply	≥0.1±20%	µF
C2	**V3P3D**	**DGND**	Bypass capacitor for 3.3V supply	≥0.1±20%	µF
XTAL	**XIN**	**XOUT**	32.768kHz crystal – electrically similar to ECS .327-12.5-17X or Vishay XT26T, load capacitance 12.5pF	32.768	kHz
CXS	**XIN**	**AGND**	Load capacitor for crystal (depends on crystal specs and board parasitics).	27±10%	pF
CXL	**XOUT**	**AGND**		27±10%	pF
C2P5	**V2P5**	**DGND**	Bypass capacitor for V2P5	≥0.1±20%	µF

FOOTNOTES:

1 This spec is guaranteed, has been verified in production samples, but is not measured in production.
2 This spec is guaranteed, has been verified in production samples, but is measured in production only at DC.
3 This spec is measured in production at the limits of the specified operating temperature.
4 This spec defines a nominal relationship rather than a measured parameter. Correct circuit operation is verified with other specs that use this nominal relationship as a reference

PIN CONFIGURATION AND PIN FUNCTION



Pins marked RESERVED should be left unconnected during normal use.

Analog Pin Description

Name	Pin No.	Type	Circuit	Description
IA, IB, IC	56 55 54	I	6	Line Current Sense Inputs: Voltage inputs to the internal A/D converter. Typically, they are connected to the output of a current transformer. The input is referenced to V3P3A. **Unused pins must be tied to V3P3A.**
VA, VB, VC	53 52 51	I	6	Line Voltage Sense Inputs: Voltage inputs to the internal A/D converter. Typically, they are connected to the output of a resistor divider. The input is referenced to V3P3A. **Unused pins must be tied to V3P3A.**
VFLT	59	I	7	Power Fault Input. **This pin must be tied to V3P3A.**
VX	58	I	6	Auxiliary input (not used). **This pin should be tied to VREF.**
VREF	57	I/O	9	Voltage Reference for the ADC.
XIN, XOUT	61 63	I	8	Crystal Inputs: A 32768Hz crystal should be connected across these pins. Typically, a 15pF capacitor is also connected from each pin to GNDA. See the datasheet of the crystal manufacturer for details.

Pin types: P = Power, O = Output, I = Input, I/O = Input/Output
The circuit number denotes the equivalent circuit, as specified under "I/O Equivalent Circuits".

Digital Pin Description

Unless otherwise indicated, all inputs and outputs are standard CMOS. Inputs do NOT have internal pull-ups or pull-downs.

Name	Pin No.	Type	Circuit	Description
CKTEST	6	I/O	4	Clock PLL output. Can be enabled and disabled by *CKOUT_DSB* (see Status Mask).
D0 D1 D2 D3 D4 D5 D6 D7	42 21 22 23 37 38 39 33	I/O	3, 4	Input/output pins 0 through 7. **These pins must be terminated to V3P3D or ground if configured as input pins.** **D0 through D7 are high impedance after reset or power-up and are configured as outputs and driven low 140ms after RESETZ goes high.**
PULSE4	15	O	4	The fourth pulse generator output
PULSE3	14	O	4	The third pulse generator output
PULSE_INIT	40	I	3	The pulse output initial power-up voltage (0: 0V, 1: 3.3V), default is 1. **This pin must be terminated to V3P3D or ground.**
BAUD_RATE	16	I	3	The UART baud rate (1: 38.4kbd, 0: 19.2kbd). **This pin must be terminated to V3P3D or ground.**
IRQZ	41	O	4	Interrupt output, low active. A falling edge indicates the end of a measurement frame, as well as alarms. Rises when status word is read.
MUXSYNC	25	O	4	Internal signal. MUXSYNC falls at the beginning of each conversion cycle (multiplexer frame).
RESETZ	47	I	1	Chip reset: Input pin with internal pull-up resistor, used to reset the chip into a known state. For normal operation, this pin is set to 1. To reset the chip, this pin is driven to 0 for 5 microseconds. No external reset circuitry is necessary for power-up reset.

Name	Pin No.	Type	Circuit	Description
UARTCSZ	34	I	3	Enables the UART when 0. The UART is disabled when this pin is set to 1. A positive pulse on this pin will reset the UART. **This pin must be terminated to ground.**
				High-Speed Synchronous Interface (SSI).
SRDY	24	I	3	**The SRDY input should be tied to ground.**
SFR	9	O	4	SSI frame pulse output, one SSCLK wide.
SSCLK	5	O	4	SSI clock output (5MHz or 10MHz selectable).
SSDATA	8	O	4	SSI data output, changes on the rising edge of SSCLK.
RX	44	I	3	UART serial Interface receiver input. **The voltage at this pin must not exceed 3.6V**. **This pin must be terminated to V3P3D or ground.**
TX	4	O	4	UART serial Interface transmitter output.
TMUXOUT	3	O	4	Digital output test multiplexer. Controlled by *TMUX[2:0]*.
PULSER	36	O	4	Selectable pulse output (default: VARh pulse).
PULSEW	35	O	4	Selectable pulse output (default: Wh pulse).

Power/Ground Pin Description

Name	Pin No.	Type	Description
GNDA	49,60	P	Analog ground: This pin should be connected directly to the ground plane.
GNDD	1,27, 48,62	P	Digital ground: These pins must be connected directly to the ground plane.
V3P3A	50	P	Analog power: A 3.3V analog power supply should be connected to this pin.
V3P3D	7	P	Digital power supply: A 3.3V digital power supply should be connected to this pin.
VBAT	45	P	Battery backup power supply. A battery or super-capacitor is to be connected between VBAT and GNDD. If no battery is used, connect VBAT to V3P3D.
V2P5	46	O	Output of the 2.5V regulator. A 0.1µF capacitor should be connected from this pin to GND.

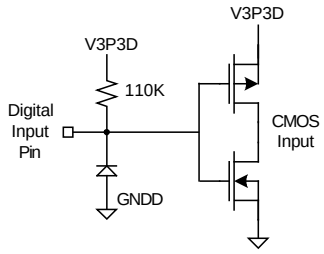
Pin types: P = Power, O = Output, I = Input, I/O = Input/Output
The circuit number denotes the equivalent circuit, as specified under "I/O Equivalent Circuits".

Reserved Pins

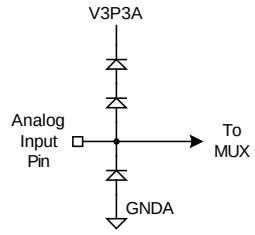
Pins labeled RESERVED are not to be connected.

Name	Pin No.	Description
RESERVED	2,10,11,12, 13,17,18,19, 20,26,28,29, 30,31,32,43, 64	**DO NOT CONNECT THESE PINS!**

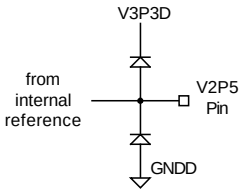
I/O Equivalent Circuits



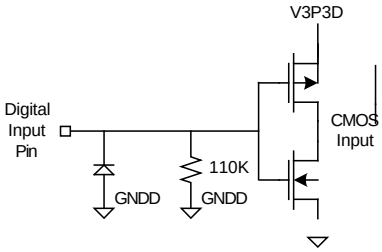
Digital Input Equivalent Circuit Type 1:
Standard Digital Input or pin configured as DIO Input with Internal Pull-Up



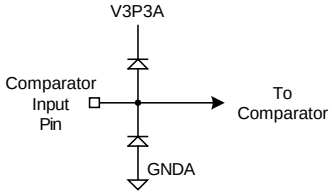
Analog Input Equivalent Circuit Type 6:
ADC Input



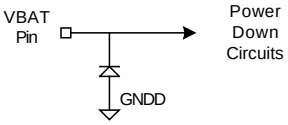
V2P5 Equivalent Circuit Type 10:
V2P5



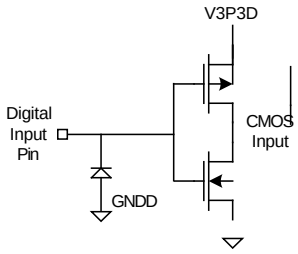
Digital Input Type 2:
Pin configured as DIO Input with Internal Pull-Down



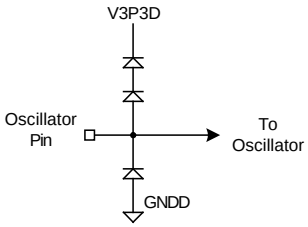
Comparator Input Equivalent Circuit Type 7:
Comparator Input



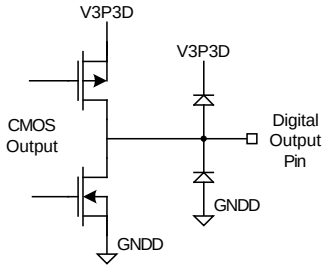
VBAT Equivalent Circuit Type 12:
VBAT Power



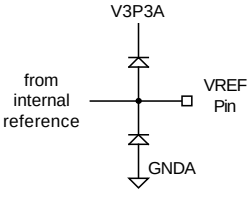
Digital Input Type 3:
Standard Digital Input or pin configured as DIO Input



Oscillator Equivalent Circuit Type 8:
Oscillator I/O



Digital Output Equivalent Circuit Type 4:
Standard Digital Output or pin configured as DIO Output



VREF Equivalent Circuit Type 9:
VREF

TYPICAL PERFORMANCE CHARACTERISTICS

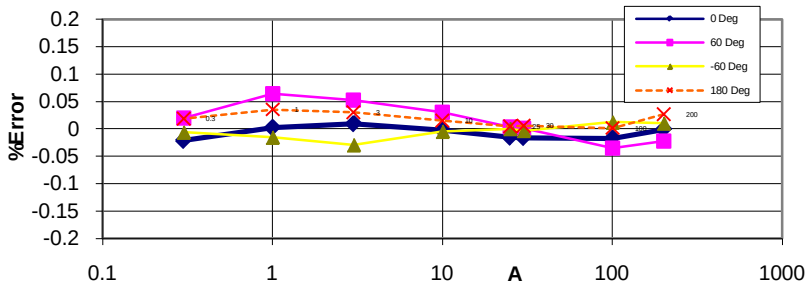


Figure 3: Wh Accuracy, 0.3A - 200A/240V

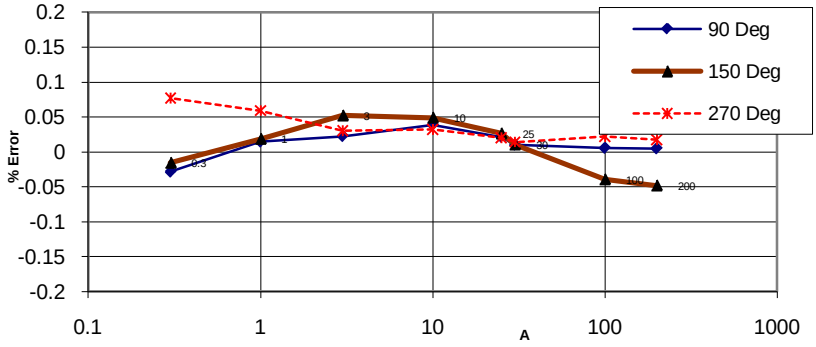
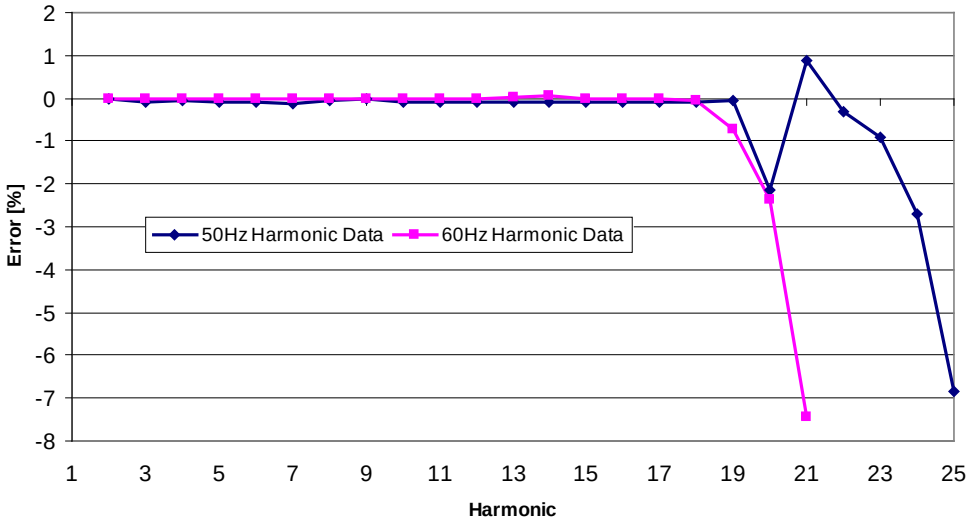


Figure 4: VARh Accuracy for 0.3A to 200A/240V Performance



Measured at current distortion amplitude of 40% and voltage distortion amplitude of 10%.

Figure 5: Meter Accuracy over Harmonics at 240V, 30A

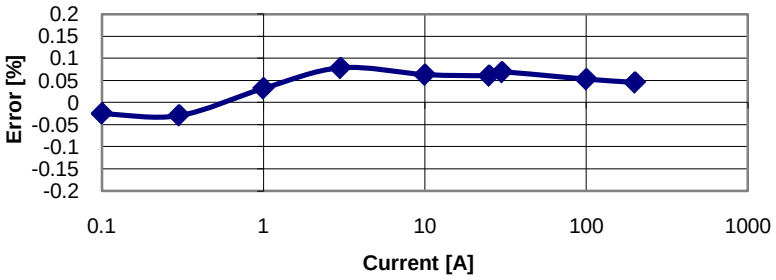


Figure 6: Typical VAh Accuracy for VAh Using Vector Method

FUNCTIONAL DESCRIPTION

THEORY OF OPERATION

The 71M6515H integrates the primary functional blocks required to implement a solid-state electricity meter front end. Included on-chip are an analog front end (AFE), a digital computation engine (CE), a voltage reference, a real time clock, and I/O pins. Various current sensor technologies are supported including Current Transformers (CT), Resistive Shunts, and Rogowski (*di/dt)* Coils.

In a typical application, the 71M6515H sequentially digitizes the voltage inputs on pins IA, VA, IB, VB, IC, VC and performs calculations to measure active energy (Wh), reactive energy (VARh), and apparent energy (VAh). In addition to these measurement functions, the real time clock function allows the device to record time of use (TOU) metering information for multi-rate applications.

The 71M6515H contains a temperature-trimmed ultra-precise voltage reference, and the on-chip digital temperature compensation mechanism includes a temperature sensor and associated controls for correction of unwanted temperature effects on measurement. RTC accuracy can be greatly improved by supplying correction coefficients derived from crystal characterization. The combination of both features enables designers to produce electricity meters with exceptional accuracy over the industrial temperature range.

Meter Equations

The 71M6515H implements the equations in Table 1. Register *EQU* specifies the equation to be used. In one sample time, each of the six inputs is converted and the selected equation updated. In a typical application, IA, IB, IC are connected to current transformers that sense the current on each phase of the line voltage. VA, VB, and VC are typically connected to voltage sensors (resistor dividers) with respect to NEUTRAL. NEUTRAL is to be connected to V3P3A, the analog supply voltage. **NEUTRAL is the zero reference for all analog measurements.**

EQU	Watt & VAR Formula	Application	Channels used from MUX sequence Mux State:					
			0	1	2	3	4	5
0	VA IA	1 element, 2W 1ø	IA	VA	-	-	-	-
1*	VA(IA-IB)/2	1 element, 3W 1ø	IA	VA	IB	-	-	-
2	VA IA + VB IB	2 element, 3W 3 øDelta	IA	VA	IB	VB	-	-
3*	VA (IA - IB)/2 + VC IC	2 element, 4W 3ø Delta	IA	VA	IB	-	IC	VC
4*	VA(IA-IB)/2 + VB(IC-IB)/2)	2 element, 4W 3ø Wye	IA	VA	IB	VB	IC	-
5	VA IA + VB IB + VC IC	3 element, 4W 3ø Wye	IA	VA	IB	VB	IC	VC

Note: Equations 1*, 3*, 4* available only when *IMAGE* = 00 (CT mode).

Table 1: Meter Equations

Table 2 shows how the elements of the meter are mapped for the six possible equations.

EQU	Watt & VAR Formula (WSUM/VARSUM)	Element Output Mapping					
		W0SUM/ VAR0SUM	W1SUM/ VAR1SUM	W2SUM/ VAR2SUM	I0SQ SUM	I1SQ SUM	I2SQ SUM
0	VA IA (1 element, 2W 1ϕ)	VA*IA	-	-	IA	-	-
1	VA*(IA-IB)/2 (1 element, 3W 1ϕ)	VA*(IA-IB)/2	VA*IB	-	IA-IB	IB	-
2	VA*IA + VB*IB (2 element, 3W 3ϕ Delta)	VA*IA	VB*IB	-	IA	IB	-
3	VA*(IA-IB)/2 + VC*IC (2 element, 4W 3ϕ Delta)	VA*(IA-IB)/2	-	VC*IC	IA-IB	IB	IC
4	VA*(IA-IB)/2 + VB*(IC-IB)/2 (2 element, 4W 3ϕ Wye)	VA*(IA-IB)/2	VB*(IC-IB)/2		IA-IB	IC-IB	IC
5	VA*IA + VB*IB + VC*IC (3 element, 4W 3ϕ Wye)	VA*IA	VB*IB	VC*IC	IA	IB	IC

Table 2: Meter Element Output Mapping

ANALOG FRONT END

A/D Converter (ADC)

A single delta-sigma A/D converter (ADC) digitizes the inputs to the device. The resolution of the ADC is 21 bits. The ADC operates at 5MHz oversampling rate and places the digital results in CE memory. Each analog input is sampled at 2520Hz. Once each accumulation interval, it refreshes the temperature value that is placed in the *TEMP_RAW* register. **The analog reference for all inputs is V3P3A, i.e. the ADC processes voltages between the input pins and V3P3A.**

Voltage Reference

The device includes an on-chip precision bandgap voltage reference that incorporates auto-zero techniques as well as production trims to minimize errors caused by component mismatch and drift. The result is a voltage output with a predictable temperature coefficient.

The CE compensates for temperature characteristics of the voltage reference by modifying the gain applied to the V and I channels based on the coefficients *PPMC* and *PPMC2*. See the section "TEMPERATURE COMPENSATION" for details.

DIGITAL COMPUTATION

The six ADC outputs are processed and accumulated digitally. The default product summation is based on 42*60 (if the *SUM_CYCLES* register is set to 60) samples per accumulation interval. At the end of each accumulation interval, a ready interrupt (IRQZ) is signaled (if enabled with the *READY* bit in *STMASK*), indicating that fresh data is available to the host. For instance, if *SUM_CYCLES* =30, the IRQZ rate will be 2Hz (500ms).

A dedicated 32-bit Computation Engine (CE) performs the precision computations necessary to accurately measure energy. Internal CE calculations include frequency-insensitive offset cancellation on all six channels and a frequency insensitive 90° phase shifter for VAR calculations. The CE also includes LPF smoothing filters after each product and squaring circuit to attenuate ripple and eliminate beat frequencies between the power line fundamental and the accumulation time. The CE directly calculates Watts, VARs, V^2, and I^2 and accumulates them for one interval.

At the end of each CE computation cycle, the accumulated data are post-processed to calculate RMS amplitudes, phase angles, and VAh. When post-processing is complete, the IRQZ signal is activated.

The minimum combined cycle time for CE and post-processor is 400ms, which makes the maximum frequency for the IRQZ signal 2.5Hz.

If the 71M6515H is interfacing to an external DSP (typically, but not necessarily through the SSI interface), the host may turn off post-processing by setting the *CE_ONLY* bit in the *CONFIG* word. This will permit setting *SUM_CYCLES* below its recommended lower limit of 24. *SUM_CYCLES* may then be reduced to 1, creating an accumulation interval of only 42 samples. The outputs available in CE only mode are limited to temperature, frequency, voltage phases, input signal zero crossings, plus WSUM and VARSUM for each phase and VSQSUM, ISQSUM, and ISQFRACT for each phase.

Pulse Generators

The chip contains four pulse generators connected to the pins PULSEW, PULSER, PULSE3, and PULSE4 that create low jitter pulses from 32-bit data. The peak time jitter for PULSEW and PULSER is the 397µs MUX frame period, and is independent of the rate of the generator or the length of time the generator is monitored. Thus, if the pulse generator is monitored for 1 second, the peak jitter is 400PPM. After 10 seconds, the peak jitter is 40PPM.

PULSE3 and PULSE4 are updated at a slower rate and have four times higher jitter, i.e. 160PPM after 10 seconds.

The average jitter is always zero. If it is attempted to drive either pulse generator faster than its maximum rate, it will simply output at its maximum rate without exhibiting any roll-over characteristics.

Pulse generator inputs may be from three sources:

- Internal (directly from the CE), PULSEW and PULSER only
- External (controlled by the host writing to registers *APULSEW, APULSER, APULSE3, APULSE4*)
- Post-processed values

The source is selected individually for each pulse output with the *PULSEW_SRC, PULSER_SRC, PULSE3_SRC,* and *PULSE4_SRC* registers. Figure 7 shows internal pulse generation for the PULSEW output selected by writing the value 35 into the *PULSEW_SRC* register.

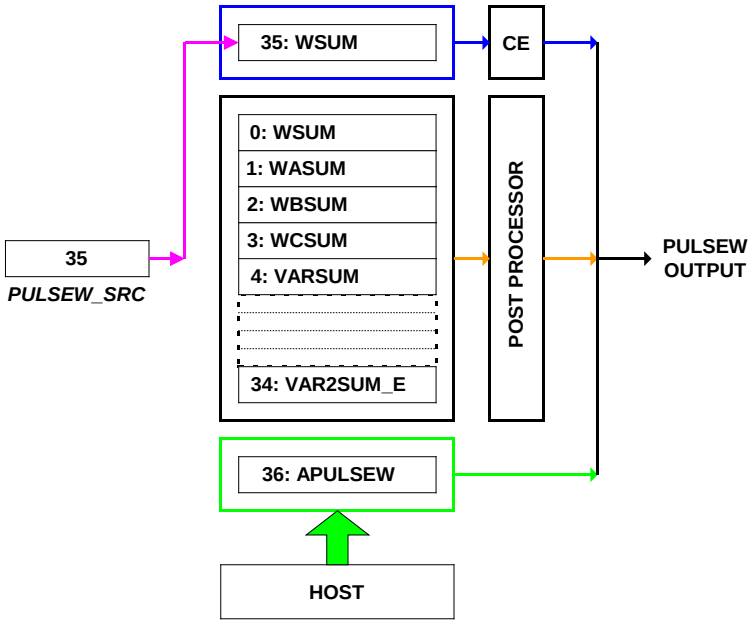


Figure 7: Internal Pulse Generation Selected in the *PULSEW_SRC* Register

Internal data is pulsed out during the accumulation interval immediately following its accumulation interval. Post-processed values are pulsed out one accumulation interval after that.

The pulse generator output rate depends on its input value, *WRATE*, *PULSE_SLOW*, and *PULSE_FAST*. Additionally, its maximum pulse width (negative going pulse) is controlled by *PULSEWIDTH*. High frequency pulses will have 50% duty cycle until their rate slows enough that their pulse width is limited by *PULSEWIDTH*.

In internal and post-processed modes, the pulse rate, expressed as Kh (Wh per pulse) is given by the formula:

$$Kh = \frac{VMAX\ IMAX}{In\_8 \cdot SUM\_CYCLES \cdot WRATE \cdot X} 1.5757 \quad Wh / Pulse$$

where
VMAX is the meter voltage corresponding to an input voltage of 176mV (rms) at the VA, VB, and VC input pins ,
IMAX is the meter current corresponding to an input voltage of 176mV (rms) at the IA, IB, and IC input pins,
In_8 is the additional ADC gain (1 or 8), as controlled by the *IA_X*, *IB_X* and *IC_X* bits in the *CONFIG* register.
X is the pulse speed factor determined from Table 3.

PULSE_SLOW	*PULSE_FAST*	X
0	0	$1.5*2^{2}=6$
0	1	$1.5*2^{6}=96$
1	0	$1.5*2^{-4}=0.09375$
1 (default)	1 (default)	1.5

Table 3: Pulse Speed Factor X

In external pulse mode, the pulse rate is given by the formula:

Rate(Hz) = *WRATE* * X * input * $35.82*10^{-12}$,

where **input** is the value in registers *APULSER, APULSEW. APULSE3* or *APULSE4,*
X is the pulse speed factor determined from Table 3.

External pulse generation can be seen as providing the raw voltage and current readings equivalent to $V_{in}*I_{in}$ / LSB directly to the pulse generator.

The maximum pulse rate is 7.56kHz for PULSEW and PULSER, and 150Hz for PULSE3 and PULSE4.

In external pulse mode, the pulse generators load their data at the beginning of each CE accumulation interval, preserving any partially implemented pulses from the previous interval. The source of data is controlled by the entries in the *PULSE_SRCS* register. *PULSER_SRCS* contains 8-bit entries for each pulse source, PULSEW, PULSER, PULSE3, and PULSE4. See the register description for details.

The procedure for accurate external pulse generation controlled by the host is:

1) Respond to a READY interrupt by reading the accumulated values.
2) Process the accumulated values.
3) Write the processed value(s) to *APULSER, APULSEW, APULSE3,* or *APULSE4*. The host must write to *APULSER, APULSEW, APULSE3,* and *APULSE4* before the next READY interrupt for the pulse generation to be beginning in the following accumulation interval.

Figure 8 illustrates pulse generator timing.

Regardless of the source, the pulse generators should receive new data during each accumulation interval. If this does not occur and if the corresponding bit in the *STMASK* register is set, an *APULSE_ERR* interrupt will be issued.

The PULSEW, PULSER, PULSE3 and PULSE4 pins are suitable for driving LEDs through a current limiting resistor. The LED should be connected so it is on when the pulse pin is low.

The pin PULSE_INIT determines the logic level applied to the pulse pins on power-up, i.e. with PULSE_INIT low, the pulse pins will be initialized to low (default = 1).

The pulse width P_W is controlled with the *PULSEWIDTH* register for the PULSER and PULSEW output pins per the following formula:

$$P_W = \frac{2 \cdot PULSEWIDTH + 1}{2520.6}$$

The PULSE3 and PULSE4 output pins will always generate pulses with 50% duty cycle.

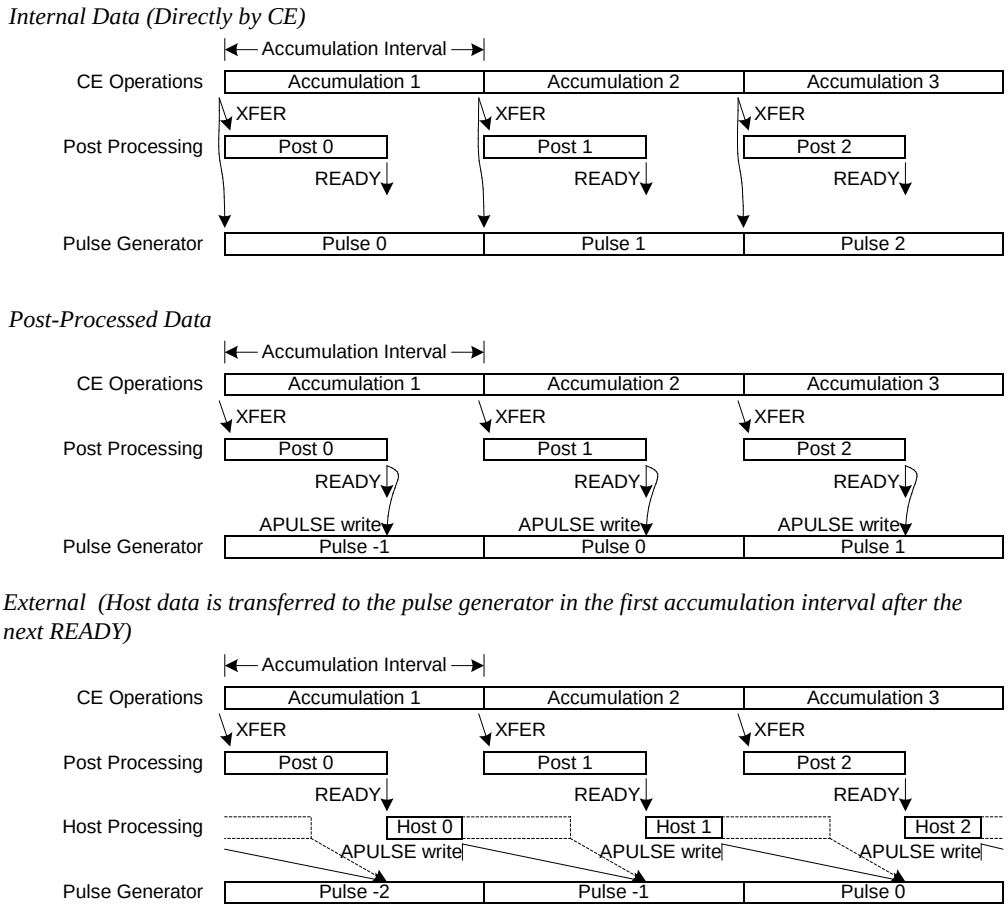


Figure 8: Pulse Generator Timing

Internal Resources

Oscillator

The oscillator drives a standard 32.768kHz watch crystal. Crystals of this type are accurate and do not require a high current oscillator circuit. The 71M6515H oscillator has been designed specifically to handle watch crystals and is compatible with their high impedance and limited power handling capability. The oscillator power dissipation is very low to maximize the lifetime of any battery backup device attached to VBAT. Using PLL techniques, all internal clocks, such as the 4.915MHz clock for the ADC and the post-processor, are derived from the watch crystal frequency.

Real-Time Clock (RTC)

The RTC is driven directly by the crystal oscillator. In the absence of V3P3, it is powered by the battery-backed up supply. The RTC consists of a counter chain and output registers. The counter chain consists of registers for seconds, minutes, hours, day of week, day of month, month, and year. The nominal quadratic temperature coefficient of the crystal is automatically compensated in the RTC. **The RTC is capable of processing leap years.**

I/O Peripherals

The 71M6515H includes several I/O peripheral functions that improve the functionality of the device and reduce the component count for most meter applications. The I/O peripherals include a UART and digital I/O.

Digital I/O

The device includes eight pins of general purpose digital I/O (D0…D7). Each pin can be configured independently as an input or output with the *D_DIR* bits. Inputs are standard CMOS with no pull-ups or pull-downs. Outputs are standard CMOS. The DIO pins are controlled by the *D_CONFIG* register.

Immediately after reset or power-up, D0 through D7 are in tri-state mode. 140 ms after reset, D0 through D7 are configured as outputs and driven low.

UART Host Interface

The UART is a dedicated 2-wire serial interface, which can communicate with the host processor. The operation of each pin is as follows:

RX: Is the pin accepting the serial input data. It inputs data to internal registers. The bytes are input LSB first. The voltage applied to this pin must be restricted to 0 to 3.6V.

TX: Is the pin used for serial output data. It outputs the contents of a block of internal registers. The bytes are output LSB first.

BAUD_RATE: The baud rate can be selected with the BAUD_RATE pin (38.4bps when high, 19.2bps when low).

UARTCSZ: This pin enables the UART when low. The UART can be reset by taking UARTCSZ briefly to the high state and then low again.

The 71M6515H has several on-chip registers, which can be read and written. All transfers start with a stream of 8-bit bytes (LSB first) from the host on the RX input, followed by a (possibly null) stream of 8-bit bytes (LSB first) to the host on the TX output (see Figure 9 and Figure 10). The UART is configured as 8N1 (8 bits, no parity, 1 stop bit).

If the *READY* bit in *STMASK* is enabled, the IRQZ pin can be used to signal data availability to the host. If data read cycles exceeding 1 second are used, care should be taken to prevent data overflow.

UART Write Register Operation

The registers are written by sending a byte, consisting of a starting register address in the seven MSBs and '0' in the LSB indicating this is a write operation. It is followed by a one byte length of bytes to write. If more bytes arrive than fit in the addressed register, subsequent registers will be written. The bytes are processed in "big-endian" order (i.e. most significant byte first). See Figure 9 (read bits and bytes from left to right).

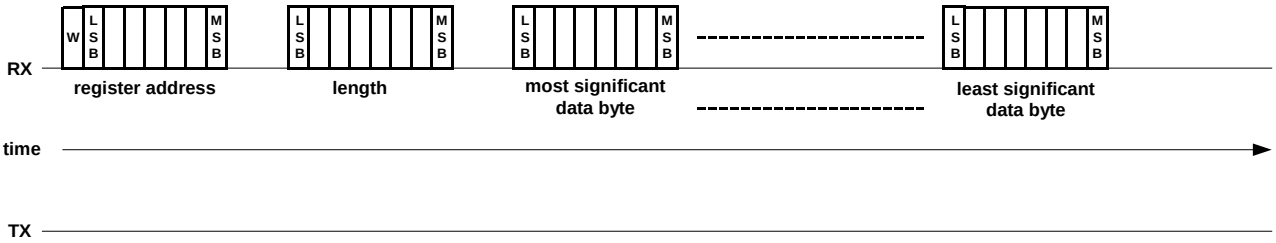


Figure 9: UART Write Operation

UART Read Register Operation

The registers are read by sending a byte, consisting of a start register address in the seven MSBs and '1' in the LSB indicating this is a read operation. It is followed by a one byte length of bytes to read. If more bytes are asked for than the size of the addressed register, subsequent registers will be read. The bytes are in "big-endian" order (i.e. most significant byte first). See Figure 10.

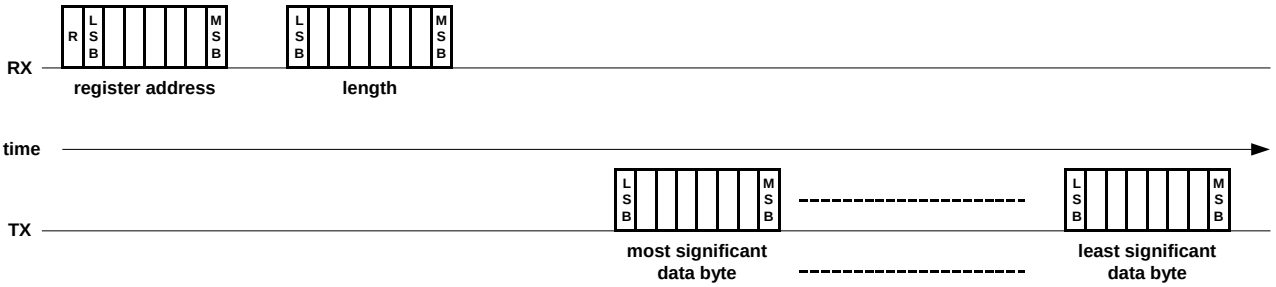


Figure 10: UART Read Operation

Note: In both register read and write operations, the register address can be 0 through 127 (0x7F). The register address byte is obtained by left-shifting the register address by one bit and setting bit 0 to 1 for read or setting bit 0 to 0 for write.

Synchronous Serial Interface (SSI)

A high speed, handshake, serial interface is available to send a contiguous block of CE data to an external data logger or DSP. The block of data, configurable as to location and size, is sent at the beginning of each ADC multiplex cycle. The SSI interface is enabled by the *SSI_EN* bit and consists of the outputs SSCLK, SSDATA, and SFR and of the SRDY input pin. The interface is compatible with 16-bit and 32-bit processors. The operation of each pin is as follows:

SSCLK: This pin provides the serial clock. The clock can be 5MHz or 10MHz, as specified by the *SSI_10M* bit. The *SSI_CKGATE* bit controls whether SSCLK runs continuously or is gated off when no SSI activity is occurring. If SSCLK is gated, it will begin three cycles before SFR rises and will persist three cycles after the last data bit is output.

SSDATA: This pin provides the serial output data. SSDATA changes on the rising edge of SSCLK and outputs the contents of a block of CE words starting with address *SSI_STRT* and ending with *SSI_END*. The words are output MSB first. SSDATA is stable with the falling edge of SSCLK.

SFR: This pin provides the framing pulse. Although CE words are always 32 bits, the SSI interface will frame the entire data block as a single field, as multiple 16 bit fields, or as multiple 32 bit fields. The SFR pulse is one clock cycle wide, changes state on the rising edge of SSCLK and precedes the first bit of each field. The field size is set with *SSI_FSIZE*: 0-entire data block, 1-8 bit fields, 2-16 bit fields, 3-32 bit fields. The polarity of the SFR pulse can be inverted with *SSI_FPOL*. The first SFR pulse in a frame will rise on the third SSCLK clock period after MUX_SYNC (fourth SSCLK period, if SSCLK is 10MHz). MUX_SYNC can be used to synchronize the fields arriving at the data logger or DSP.

SRDY: The SRDY input should always be tied to GND.

The SSI timing is shown in Figure 11.

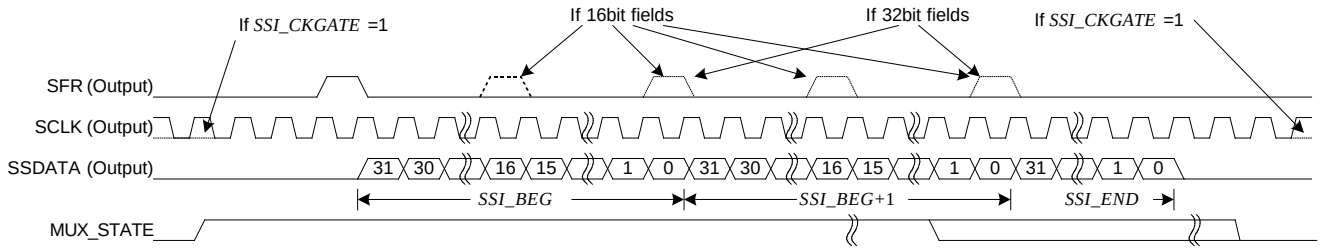


Figure 11: SSI Timing (*SSI_FPOL* = *SSI_RDYPOL* = 0)

Fault and Reset Behavior

Reset Mode

When RESETZ is pulled low or when VFLT < V3P3/2, all activity (i.e. sampling of analog signals, CE, generation of digital outputs) in the chip stops while the analog circuits are active. The exceptions are the oscillator and RTC module, which continue to run. Additionally, all I/O Register bits are cleared. As long as VFLT > V3P3/2, the internal 2.5V regulator will continue to provide power to the digital section.

Once initiated, the reset mode will persist until the reset timer times out. This will occur in 4100 cycles of the real time clock after RESETZ goes high, at which time the 71M6515H will begin executing its preboot and boot sequences.

Power Fault Circuit

The power fault comparator compares the voltage at the VFLT pin to V3P3/2. The comparator output internally enables the battery backup protection for oscillator, RTC and RAM during the power fail mode.

Temperature Compensation

Voltage Reference

The internal voltage reference of the 71M6515H is calibrated at 25°C during device manufacture. The 71M6515H is given additional temperature-related calibrations which further compensate its ADC gain and allow it to achieve 10PPM/°C over ±60°C temperature range.

Temperature Sensor

The device includes an on-chip temperature sensor for determining the temperature of the bandgap reference. The primary use of the temperature data is to determine the magnitude of compensation required to offset thermal drift in the system. The temperature sensor is read once per accumulation interval.

Temperature measurement can be implemented with the following steps:

1) At a known temperature T_N, read the *TEMP_RAW* register and write the value into *TEMP_NOM* register.
2) Read the *DELTA_T* register at the known temperature. The obtained value should be <±0.1°C.
3) The temperature T (in °C) at any environment can be obtained by reading the *DELTA_T* register and applying the following formula:

$$T = T_N + \frac{DELTA\_T}{10}$$

Temperature Compensation for Energy Measurements

TEMP_NOM is one of the calibration parameters that must be loaded by the host in order to enable temperature measurement and thereby temperature compensation.

PPMC and *PPMC2*, the linear and quadratic compensation coefficients, compensate for temperature drift in the 71M6515H reference that affects the meter performance. *PPMC* and *PPMC2* describe how the 71M6515H calculations are to respond to temperature. This means they should be the negative of the meter behavior before compensation. *PPMC* and *PPMC2* are scaled from PPM/°C and PPM/°C^2 values. See the register description for details. Temperature compensation can be selected to operate in one of two modes shown in the table below:

Temperature Compensation Mode	*DEFAULT_PPM* Bit in *CONFIG* Register	*PPMC*, *PPMC2* Calculation
Internal (CE)	1	By post-processor, based on stored VREF characteristics
External (host)	0	By host

When the part is first powered up, *TEMP_NOM*, *PPMC*, and *PPMC2* are zero. When the host writes its calibration value into *TEMP_NOM* (after setting the *DEFAULT_PPM* bit on the *CONFIG* register to 1), *PPMC* and *PPMC2* will automatically be initialized to the values that best compensate for the temperature drift of the internal reference. These parameters will be individually customized for 71M6515H parts. If, for some reason, the host writes to *TEMP_NOM* again, *PPMC* and *PPMC2* will not be changed since they will no longer be zero.

If *TEMP_NOM* is not loaded by the host, *PPMC* and *PPMC2* are ignored, and their values are permanently held at zero. If *TEMP_NOM* is zero, no temperature compensation occurs, even if *PPMC* and *PPMC2* are loaded.

If the host wishes to provide its own compensation, it should read *PPMC* and *PPMC2* and modify them by merging the additional compensation into to them. In that case, the *DEFAULT_PPM* bit in the CONFIG register must be zero.

Temperature Compensation for the Crystal and RTC

The crystal oscillator contributes negligible error to energy calculations. However, sometimes specifications for the real time clock (RTC) require better accuracy than that provided by the untrimmed watch crystal. The 71M6515H therefore allows calibration of the RTC clock. Calibration requires that frequency tolerance and frequency stability either be obtained from the manufacturer or be independently measured (the RTC clock is available on the TMUX pin). Calibration does not change the frequency of the RTC clock, but rather increments or decrements the clock by one second when sufficient error has accumulated. Positive correction makes the clock run faster.

The formula for the RTC correction factor is as follows:

$$\text{CORRECTION [PPM]} = \frac{Y\_CALC0}{10} + \frac{Y\_CALC1}{100}\Delta T + \frac{Y\_CALC2}{1000}\Delta T^2$$

Where ***Y_CALC0*** = 10 * crystal frequency deviation from ideal (measured)

Y_CALC1 = 100 * crystal skew (nominally zero)

Y_CALC2 = 1000 * crystal frequency stability (specified)

ΔT = T - Calibration Temperature in °C

Calibration

Calibration Factors for CT and Resistive Shunt

Once installed in a meter, the TERIDIAN 71M6515H IC has to be calibrated for the tolerances of current sensors, voltage dividers and signal conditioning components. The room temperature reading of its temperature sensor must also be entered. These calibration factors must be stored by the host and, upon power up, loaded into the TERIDIAN 71M6515H. Typical calibration constants are listed in Table 4.

Name	Description
CAL_IA	Gain factors for current and voltage of each phase.
CAL_VA	
CAL_IB	
CAL_VB	
CAL_IC	
CAL_VC	
TEMP_NOM	The value of *TEMP_RAW* at nominal temperature.
PHADJ_A	Phase compensation for each current. If phase compensation is 0 or if current sensors have predictable phase, PHADJ may not need to be measured on every meter.
PHADJ_B	
PHADJ_C	

Table 4: Typical Calibration Parameters (CT)

Gain adjustment (*CAL_Xn* parameters) is used to compensate for tolerances of components used for signal conditioning, especially the resistive components. A 1% increase in *CAL_Xn* will cause a 1% increase in the channel gain.

The phase compensation circuit in the TERIDIAN 71M6515H is optimized for operation with current transformers (CT's). These devices have a low frequency pole and therefore have a slight amount of phase lead at 50 or 60Hz—more at 50Hz than at 60Hz. The phase lead diminishes at higher harmonics. When *PHADJ_n* is calibrated as shown below at either 50Hz or 60Hz, the CT will be correctly compensated from below 25Hz to beyond 1100Hz.

This phase compensator is markedly superior to the more common technique of programming a time delay to compensate for CT phase. The time delay technique results in phase compensation that is correct at only one frequency, and actually amplifies the phase error at harmonics of the frequency.

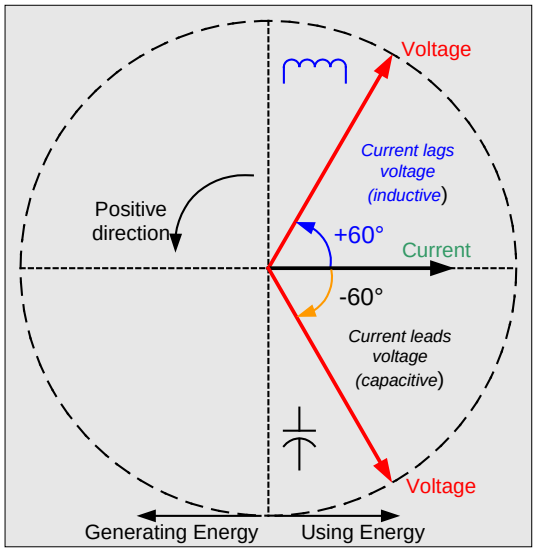
Calibration Factors for Rogowski Coil Sensors

If *IMAGE* is set to 01, i.e. the 71M6515H can be operated with Rogowski Coil sensors. In this case, one more calibration factor per phase is needed. The *PHADJ* parameters have non-zero defaults and do not obey the same formula used for CT calibration. The feedthrough parameter has to be determined by a separate crosstalk measurement. Table 5 shows the parameters involved in the calibration procedure for the Rogowski sensor.

Name	Description
CAL_IA	Gain constants for current and voltage of each phase.
CAL_VA	
CAL_IB	
CAL_VB	
CAL_IC	
CAL_VC	
TEMP_NOM	The value of *TEMP_RAW* at nominal temperature.
PHADJ_A	Phase compensation for each current. If phase compensation is 0 or if current sensors have predictable phase, *PHADJ* may not need to be measured on every meter.
PHADJ_B	
PHADJ_C	
VFEED_A	Feedthrough compensation for each current.
VFEED_B	
VFEED_C	

Table 5: Typical Calibration Parameters (Rogowski)

General Notes on Calibration



The calibration procedures described below should be followed after interfacing the voltage and current sensors to the 71M6515H chip. When properly interfaced, the V3P3 power supply is connected to the meter neutral and is the DC reference for each input. Each voltage and current waveform, as seen by the 6515H, is scaled to be less than 250mV (peak).

Each meter phase must be calibrated individually. The procedures below show how to calibrate a meter phase with either three or five measurements. Note that there is no need to calibrate for VARh if the Wh measurement is calibrated correctly. Note that positive load angles correspond to lagging current (see Figure 12).

For a typical calibration, a meter calibration system is used to apply a calibrated load, e.g. 240V at 30A, while interfacing the voltage and current sensors to the 71M6515H. This load should result in an observable pulse rate at the PULSEW output depending on the selected energy per pulse. For example, 7.2kW will result in an energy rate corresponding to 7200Wh/3600s = 2Wh/s, i.e., when 7.2kW are applied per phase (resulting in a total power of 21.6kW, equivalent to 6Wh/s) and a Kh of 3.2 (Wh/pulse) has been configured, a pulse rate of 6Wh/3.2Whs = 1.875Hz will be established.

Figure 12: Definition of Load Angles

It is entirely possible to calibrate piece-wise, i.e. in segments, to compensate for non-linear sensors. For example, one set of calibration factors can be applied by the host when the current is below 0.5A, while another set is applied when the current is at or above 0.5A.

Calibration Procedure for CT and Resistive Shunt

A typical meter has phase and gain errors as shown by ϕ_S, A_{XI}, and A_{XV} in Figure 13. Following the typical meter convention of current phase being in the lag direction, the small amount of phase lead in a typical current sensor is represented as $-\phi_S$. The errors shown in Figure 13 represent the sum of all gain and phase errors. They include errors in voltage attenuators, current sensors, signal conditioning circuits, and in ADC gains. In other words, no errors are made in the 'input' or 'meter' boxes.

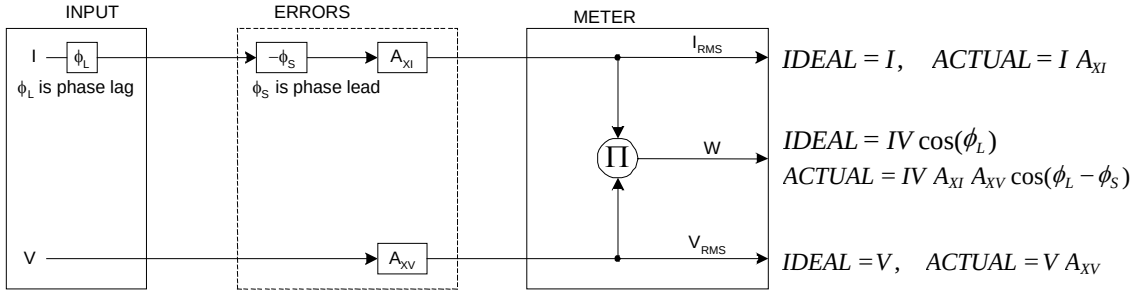


Figure 13: Watt Meter with Gain and Phase Errors.

During the calibration phase, we measure errors and then introduce correction factors to nullify their effect. With three unknowns to determine, we must make at least three measurements. If we make more measurements, we can average the results.

Calibration with Three Measurements

The simplest calibration method is to make three measurements. Typically, a voltage measurement and two Watt-hour (Wh) measurements are made.

If the voltage measurement has the error E_V and the two Wh measurements have errors E_0 and E_{60}, where E_0 is measured with $\phi_L = 0$ and E_{60} is measured with $\phi_L = 60$. These values should be simple ratios—not percentage values. They should be zero when the meter is accurate and negative when the meter runs slow. The fundamental frequency is f_0. T is equal to $1/f_S$, where f_S is the sample frequency (2520.62Hz). Set all calibration factors to nominal: *CAL_IA* = 16384, *CAL_VA* = 16384, *PHADJ_A* = 0.

From the voltage measurement, we determine that

1.➔ $$A_{XV} = E_V + 1$$

We use the other two measurements to determine ϕ_S and A_{XI}.

2. $$E_0 = \frac{IV\, A_{XV}\, A_{XI} \cos(0 - \phi_S)}{IV \cos(0)} - 1 = A_{XV}\, A_{XI} \cos(\phi_S) - 1$$

2a. $$A_{XV} A_{XI} = \frac{E_0 + 1}{\cos(\phi_S)}$$

3. $$E_{60} = \frac{IV\, A_{XV}\, A_{XI} \cos(60 - \phi_S)}{IV \cos(60)} - 1 = A_{XV}\, A_{XI} \frac{\cos(60 - \phi_S)}{\cos(60)} - 1$$

3a. $$E_{60} = \frac{A_{XV} A_{XI} \left[\cos(60)\cos(\phi_S) + \sin(60)\sin(\phi_S)\right]}{\cos(60)} - 1$$

$$= A_{XV} A_{XI} \cos(\phi_S) + A_{XV} A_{XI} \tan(60)\sin(\phi_S) - 1$$

Combining 2a and 3a:

4. $$E_{60} = E_0 + (E_0 + 1)\tan(60)\tan(\phi_S)$$

5. $$\tan(\phi_S) = \frac{E_{60} - E_0}{(E_0 + 1)\tan(60)}$$

6.➔ $$\phi_S = \tan^{-1}\left(\frac{E_{60} - E_0}{(E_0 + 1)\tan(60)}\right)$$

and from 2a:

7.➔ $$A_{XI} = \frac{E_0 + 1}{A_{XV} \cos(\phi_S)}$$

Now that we know the A_{XV}, A_{XI}, and ϕ_S errors, we calculate the new calibration voltage gain coefficient from the previous ones:

$$CAL\_V_{NEW} = \frac{CAL\_V}{A_{XV}}$$

We calculate PHADJ from ϕ_S, the desired phase lag:

$$PHADJ = 2^{20}\left[\frac{\tan(\phi_S)\left[1+(1-2^{-9})^2-2(1-2^{-9})\cos(2\pi f_0 T)\right]}{(1-2^{-9})\sin(2\pi f_0 T)-\tan(\phi_S)\left[1-(1-2^{-9})\cos(2\pi f_0 T)\right]}\right]$$

Finally, we calculate the new calibration current gain coefficient, including compensation for a slight gain increase in the phase calibration circuit.

$$CAL\_I_{NEW} = \frac{CAL\_I}{A_{XI}}\frac{1}{\sqrt{1+\dfrac{2^{-20}\,PHADJ\,(2+2^{-20}\,PHADJ-2(1-2^{-9})\cos(2\pi f_0 T))}{1-2(1-2^{-9})\cos(2\pi f_0 T)+(1-2^{-9})^2}}}$$

Calibration with Five Measurements

The five measurement method provides more orthogonality between the gain and phase error derivations. This method involves measuring E_V, E_0, E_{180}, E_{60}, and E_{300}. Again, set all calibration factors to nominal, i.e. *CAL_IA* = 16384, *CAL_VA* = 16384, *PHADJ_A* = 0..

First, calculate A_{XV} from E_V:

1.➔ $A_{XV} = E_V + 1$

Calculate A_{XI} from E_0 and E_{180}:

2. $E_0 = \dfrac{IV\,A_{XV}\,A_{XI}\cos(0-\phi_S)}{IV\cos(0)} - 1 = A_{XV}\,A_{XI}\cos(\phi_S) - 1$

3. $E_{180} = \dfrac{IV\,A_{XV}\,A_{XI}\cos(180-\phi_S)}{IV\cos(180)} - 1 = A_{XV}\,A_{XI}\cos(\phi_S) - 1$

4. $E_0 + E_{180} = 2A_{XV}A_{XI}\cos(\phi_S) - 2$

5. $A_{XV}A_{XI} = \dfrac{E_0 + E_{180} + 2}{2\cos(\phi_S)}$

6.➔ $A_{XI} = \dfrac{(E_0 + E_{180})/2 + 1}{A_{XV}\cos(\phi_S)}$

Use above results along with E_{60} and E_{300} to calculate ϕ_S.

7. $E_{60} = \dfrac{IV\,A_{XV}\,A_{XI}\cos(60-\phi_S)}{IV\cos(60)} - 1$

$= A_{XV}A_{XI}\cos(\phi_S) + A_{XV}A_{XI}\tan(60)\sin(\phi_S) - 1$

8. $E_{300} = \dfrac{IV\,A_{XV}\,A_{XI}\cos(-60-\phi_S)}{IV\cos(-60)} - 1$

$= A_{XV}A_{XI}\cos(\phi_S) - A_{XV}A_{XI}\tan(60)\sin(\phi_S) - 1$

Subtract 8 from 7:

9. $$E_{60} - E_{300} = 2A_{XV}A_{XI}\tan(60)\sin(\phi_S)$$

use equation 5:

10. $$E_{60} - E_{300} = \frac{E_0 + E_{180} + 2}{\cos(\phi_S)}\tan(60)\sin(\phi_S)$$

11. $$E_{60} - E_{300} = (E_0 + E_{180} + 2)\tan(60)\tan(\phi_S)$$

12.➔ $$\phi_S = \tan^{-1}\left(\frac{(E_{60} - E_{300})}{\tan(60)(E_0 + E_{180} + 2)}\right)$$

Now that we know the A_{XV}, A_{XI}, and ϕ_S errors, we calculate the new calibration voltage gain coefficient from the previous ones:

$$CAL\_V_{NEW} = \frac{CAL\_V}{A_{XV}}$$

We calculate PHADJ from ϕ_S, the desired phase lag:

$$PHADJ = 2^{20}\left[\frac{\tan(\phi_S)\left[1 + (1-2^{-9})^2 - 2(1-2^{-9})\cos(2\pi f_0 T)\right]}{(1-2^{-9})\sin(2\pi f_0 T) - \tan(\phi_S)\left[1 - (1-2^{-9})\cos(2\pi f_0 T)\right]}\right]$$

Finally, we calculate the new calibration current gain coefficient, including compensation for a slight gain increase in the phase calibration circuit.

$$CAL\_I_{NEW} = \frac{CAL\_I}{A_{XI}}\frac{1}{\sqrt{1 + \frac{2^{-20}PHADJ(2 + 2^{-20}PHADJ - 2(1-2^{-9})\cos(2\pi f_0 T))}{1 - 2(1-2^{-9})\cos(2\pi f_0 T) + (1-2^{-9})^2}}}$$

Alternative Calibration Procedures

It is possible to implement a fast calibration based on only one measurement with a zero-degree load angle. Details can be found in the TERIDIAN Application Note AN_651X_022 (Calibration Procedures).

Calibration Procedure for Rogowski Sensor

Rogowski coils generate an output signal that is the derivative of the input current. The 6515H Rogowski module implemented in the Rogowski CE image digitally compensates for this effect and has the usual gain and phase calibration adjustments. Additionally, calibration adjustments are provided to eliminate voltage coupling from the sensor input.

Current sensors built from Rogowski coils have relatively high output impedances that are susceptible to capacitive coupling from the large voltages present in the meter. The most dominant coupling is usually capacitance between the primary of the coil and the coil's output. This coupling adds a component proportional to the derivative of voltage to the sensor output. This effect is compensated by the voltage coupling calibration coefficients.

As with the CT procedure, the calibration procedure for Rogowski sensors uses the meter's display to calibrate the voltage path and the pulse outputs to perform the remaining energy calibrations. The calibration procedure must be performed to each phase separately, making sure that the pulse generator is driven by the accumulated real energy for just that phase. In other words, the pulse generator input should be set to WhA, WhB, or WhC, depending on the phase being calibrated. The IC has to be configured for Rogowski mode (*IMAGE*=01). In preparation of the calibration, all calibration parameters are set to their default values. *VMAX* and *IMAX* are set to reflect the system design parameters. *WRATE* and *PULSE_SLOW*, *PULSE_FAST* are adjusted to obtain the desired Kh.

For details on calibrating a meter for Rogowski coil sensors, see the TERIDIAN Application Note AN_6515_036.

Meter Design - Scaling of Measured Values

An actual meter will always use sensors that scale the voltages and currents managed by the meter to small voltages that can be processed by the 71M6515H. This scaling is reflected in the system parameters *VMAX* and *IMAX*. Scaling is physically implemented with resistor dividers for the voltage signals and current transformers, shunt resistors or Rogowski coils for the current signals.

IMAX is the RMS meter current that results in 250mV peak signal (or 177mV RMS) at the ADC input (IA, IB, IC pins). *VMAX* is the RMS meter voltage that results in 250mV peak signal at the ADC input (VA, VB, VC pins). In_8 is either 1 or 8, depending on *In_8x*, the ADC gain configuration bit for element n (see *IA_8, IB_8, IC_8*) in the *CONFIG* register.

Only the host is aware of the system parameters *VMAX* and *IMAX*, while the CE and the post-processor know signal amplitudes only as values relative to their maximum peak levels (250mV). This makes the host itself responsible for translating the measured values from the 71M6515H registers into real-world values by applying the parameters *VMAX*, *IMAX* and *In_8*. Equally, the host is responsible for non-volatile storage of accumulated energy values, calibration factors, default settings et cetera.

Measured values and values determining the function of the 71M6515H, as controlled by the registers described in the following section, are often stated as fractions or multiples of the system parameters *VMAX*, *IMAX* and *In_8*.

Host Interface - REGISTER DESCRIPTION

Communication between the host and the 71M6515H is established by writing to and reading from the registers described in this section. The registers are accessible via the UART (see UART Write and Read Operation).

The tables below contain the registers that can be accessed by the host to obtain data from the 71M6515H or to control and configure the IC.

Bits with a W (write) direction are written by the host. Bits with R (read) direction can only be read by the host. Write operations attempted to read-only registers will result in the *CMD_IGNORED* bit set in the *STATUS* register. Unless stated otherwise, all registers are four bytes (32 bits), 2's complement, and have a range of $(2^{31}-1)$ to $-(2^{31}-1)$.

Register Groups

Each register belongs to one of the following functional groups:

- Pulse Generation
- Calibration
- Control of Basic Functions
- Temperature
- Temperature Compensation
- Output Signals
- Accumulated Energy and V/I Values
- Alarms and Thresholds
- Time (RTC)
- Test
- Digital I/O Control (pins D0…D7)

Registers in Alphabetical Order

Name	Address (hex)	R/W	Default	Group	Comment
APULSEW *APULSER* *APULSE3* *APULSE4*	0x30 0x31 0x32 0x33	R/W R/W R/W R/W	0 0 0 0	Pulse Generation Control	
CAL_IA *CAL_VA*	0x24 0x25	R/W R/W	2^{14} 2^{14}	Calibration	
CAL_IB *CAL_VB*	0x26 0x27	R/W R/W	2^{14} 2^{14}	Calibration	
CAL_IC *CAL_VC*	0x28 0x29	R/W R/W	2^{14} 2^{14}	Calibration	
CE_DATA	0x63	R/W	N/A	Control of Basic Functions	
CE_DATA_ADDR	0x61	R/W	N/A	Control of Basic Functions	
CE_DATA_INC	0x65	R/W	N/A	Control of Basic Functions	
CE_PROG	0x62	R/W	N/A	Control of Basic Functions	
CE_PROG_ADDR	0x60	R/W	N/A	Control of Basic Functions	
CE_PROG_INC	0x64	R/W	N/A	Control of Basic Functions	
CONFIG	0x16	R/W	0	Control of Basic Functions	
CREEP_THRSLD	0x1D	R/W	6000	Alarms and Thresholds	
DEG_SCALE	0x1C	R/W	22721	Temperature	
D_CONFIG	0x1A	R/W	15	I/O Control	
FREQ_DELTA_T	0x11	R	N/A	Outputs, Temperature	
GAIN_ADJ	0x4E	R	16384	Temperature Compensation	
IASQFRACT *IBSQFRACT* *ICSQFRACT*	0x4A 0x4B 0x4C	R R R	N/A N/A N/A	Outputs	
IASQSUM *IBSQSUM* *ICSQSUM*	0x39 0x3A 0x3B	R R R	N/A N/A N/A	Outputs	
INSQFRACT	0x4D	R	N/A	Outputs	
INSQSUM	0x3C	R	N/A	Outputs	
IPHASE_ABC	0x0F	R	N/A	Outputs	**Uses the post-processor**
IRMS_A *IRMS_B* *IRMS_C*	0x0C 0x0D 0x0E	R R R	N/A N/A N/A	Outputs	**Uses the post-processor**
KVAR	0x2F	R	6444	Calibration	Do not change
MAIN_EDGE_ COUNT	0x35	R	N/A	Outputs	
OP_TIME	0x1E	R/W	0	Time	

Name	Address (hex)	R/W	Default	Group	Comment
PHADJ_A *PHADJ_B* *PHADJ_C*	0x2A 0x2B 0x2C	R/W R/W R/W	CT: 0 CT: 0 CT: 0	Calibration	Defaults are –3973 for Rogowski operation
PPMC1_2	0x1B	R/W	0	Temperature Compensation	
PULSE3_4_ CNTS	0x42	R	N/A	Outputs	
PULSE_SRCS	0x43	R/W		Pulse Generation Control	
PULSEW_R_ CNTS	0x41	R	N/A	Outputs	
PULSE_WIDTH	0x34	R/W	50	Pulse Generation Control	
QUANT_W *QUANT_VAR* *QUANT_I*	0x36 0x37 0x38	R/W R/W R/W	0 0 0	Calibration	
RTC_DATE	0x20	R/W	N/A	Time	
RTC_TIME_DAY	0x1F	R/W	N/A	Time	
RTM	0x21	R/W	0	Test	
SAG	0x2E	R/W	80, 26000	Alarms and Thresholds	
SSI	0x22	R/W	0	Test	
STATUS	0x14	R	N/A	Control of Basic Functions	
STMASK	0x15	R/W	0	Control of Basic Functions	
TEMP_NOM	0x13	R/W	0	Outputs	
TEMP_RAW	0x12	R	N/A	Outputs	
VASQSUM *VBSQSUM* *VCSQSUM*	0x3D 0x3E 0x3F	R R R	N/A N/A N/A	Outputs	
VAH_A *VAH_B* *VAH_C*	0x06 0x07 0x08	R R R	N/A N/A N/A	Outputs	**Uses the post-processor**
VARH_A *VARH_B* *VARH_C*	0x03 0x04 0x05	R R R	N/A N/A N/A	Outputs	
VFEED_A *VFEED_B* *VFEED_C*	0x44 0x45 0x46	R/W R/W R/W	0 0 0	Calibration	
VI_PTHRESH	0x17	W	21000	Alarms and Thresholds	
VI_THRESH	0x40	W	21000	Alarms and Thresholds	

Name	Address (hex)	R/W	Default	Group	Comment
VPHASE_ABC	0x10	R	N/A	Outputs	
VRMS_A *VRMS_B* *VRMS_C*	0x09 0x0A 0x0B	R R R	N/A N/A N/A	Outputs	**Uses the post-processor**
WH_A *WH_B* *WH_C*	0x00 0x01 0x02	R R R	N/A N/A N/A	Outputs	
WRATE	0x2D	R/W	683	Pulse Generation Control	
Y_DEG0	0x18	R/W	0	Temperature Compensation	Holds *Y_CALC0*
Y_DEG1_2	0x19	R/W	0	Temperature Compensation	Holds *Y_CALC1* and *Y_CALC2*

Individual Register Descriptions

Registers for Pulse Generation Control

***APULSEW* (0x30), *APULSER* (0x31), *APULSE3* (0x32), *APULSE4* (0x33),**

Figure 14 shows the registers that control the PULSEW, PULSER, PULSE3 and PULSE4 output pins if the corresponding *PULSE_SRCS* register contains the decimal value 36. This figure uses the *PULSER_SRC* 8-bit portion of the *PULSE_SRCS* register as an example: The internal pulse generation (CE) and the post-processor pulse generation are deselected, and the *APULSER* register acts as the pulse generation source. In this setting (external pulse generation), the host is responsible for updating the data in the *APULSER* register.

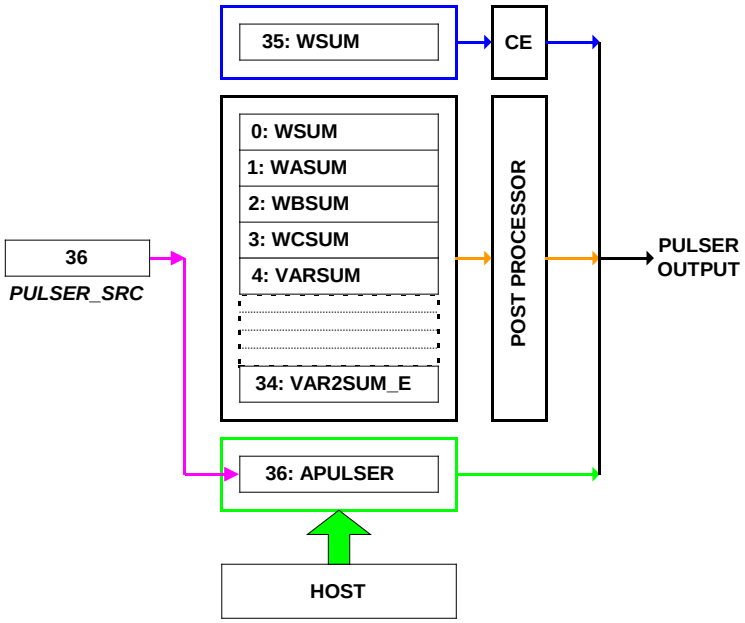


Figure 14: Pulse Generation via *APULSER* Selected in the *PULSER_SRC* Register

***PULSE_SRCS* (0x43)**

This register contains the pulse source selectors for the pulses generated by the PULSEW, PULSER, PULSE3 and PULSE4 output pins. Pulse sources can be selected individually for internal (CE), external (post-processor) or external (supplied by the host). The internal selection is valid for the PULSER and PULSEW generators only. The allocation of the bytes in *PULSE_SRCS* is as follows:

31 24	23 16	15 8	7 0
PULSEW_SRC	*PULSER_SRC*	*PULSE3_SRC*	*PULSE4_SRC*
Source selector register for the PULSEW generator	Source selector register for the PULSER generator	Source selector register for the PULSE3 generator	Source selector register for the PULSE4 generator

Table 6 shows the codes used to select pulse sources.

***PULSE_WIDTH* (0x34)**

This register contains the numerical value controlling the pulse width for the PULSEW and PULSER output pins. The default value is 50, which amounts to 40.07ms. The pulse width P_W follows the formula:

$P_W <= (2 * PULSE\_WIDTH + 1)/2520.6$

At high pulse rates, duty cycle is 50%. At rates less than 1/(2*PWmax), the negative going pulse width is PWmax. The allowed range is 0 to 2^{31}-1.

The pulse width for the PULSE3 and PULSE4 outputs is always at a 50% duty cycle.

The initial voltage level of the pulse pins is defined with the PULSE_INIT pin.

Value in Pulse Source Register (hex)	(dec)	Name	Description
0x00	0	*WSUM*	The signed sum: *W0SUM + W1SUM + W2SUM*
0x01	1	*WASUM*	The sum of Wh samples from individual wattmeter elements. LSB = $9.4045*10^{-13}$ *VMAX IMAX / In_8* Wh
0x02	2	*WBSUM*	
0x03	3	*WCSUM*	
0x04	4	*VARSUM*	The signed sum: *VAR0SUM + VAR1SUM + VAR2SUM*
0x05	5	*VARASUM*	The sum of VARh samples from individual wattmeter elements. LSB = $9.4045*10^{-13}$ *VMAX IMAX / In_8* VARh
0x06	6	*VARBSUM*	
0x07	7	*VARCSUM*	
0x08	8	*VASUM*	The sum of VAh samples from individual samples.
0x09	9	*VAASUM*	The sum of VAh samples from individual wattmeter elements. LSB = $9.4045*10^{-13}$ *VMAX IMAX* / *In_8* VAh
0x0A	10	*VABSUM*	
0x0B	11	*VACSUM*	
0x0C	12	*INSQSUM*	The sum of the square of the calculated neutral current. $\sum (I_0 + I_1 + I_2)^2$. LSB = $9.4045*10^{-13}$ $IMAX^2$ / In_8^2 A^2h
0x0D	13	*IASQSUM*	The sum of squared current samples from each element. LSB = $9.4045*10^{-13}$ $IMAX^2$ / In_8^2 A^2h
0x0E	14	*IBSQSUM*	
0x0F	15	*ICSQSUM*	

Table 6: Pulse Sources Defined by the *PULSE_SRCS* Register (1/2)

Value in Pulse Source Register (hex)	(dec)	Name	Description
0x10	16	*VASQSUM*	The sum of squared voltage samples from each element. LSB = 9.4045*10^{-13} *VMAX*^{2} V^{2}h
0x11	17	*VBSQSUM*	
0x12	18	*VCSQSUM*	
0x13	19	*WSUM_I*	Imported Energy: *W0SUM_I + W1SUM_I + W2SUM_I*
0x14	20	*WASUM_I*	Imported energy from individual wattmeter elements. Never negative. LSB = 9.4045*10^{-13} *VMAX IMAX / In_8* Wh
0x15	21	*WBSUM_I*	
0x16	22	*WCSUM_I*	
0x17	23	*VARSUM_I*	Imported VARh: *VAR0SUM_I + VAR1SUM_I + VAR2SUM_I*
0x18	24	*VARASUM_I*	Exported reactive energy from individual wattmeter elements. Never negative. LSB = 9.4045*10^{-13} *VMAX IMAX / In_8* VARh
0x19	25	*VARBSUM_I*	
0x1A	26	*VARCSUM_I*	
0x1B	27	*WSUM_E*	Exported Energy: *W0SUM_E + W1SUM_E + W2SUM_E*
0x1C	28	*WASUM_E*	Exported energy from individual wattmeter elements. Never negative. LSB = 9.4045*10^{-13} *VMAX IMAX / In_8* Wh
0x1D	29	*WBSUM_E*	
0x1E	30	*WCSUM_E*	
0x1F	31	*VARSUM_E*	Exported VARh: *VAR0SUM_E + VAR1SUM_E + VAR2SUM_E*
0x20	32	*VARASUM_E*	Exported reactive energy from individual wattmeter elements. Never negative. LSB = 9.4045*10^{-13} *VMAX IMAX / In_8 VARh*
0x21	33	*VARBSUM_E*	
0x22	34	*VARCSUM_E*	
0x23	35	Internal (CE)	Connects the pulse generator to the *WSUM* or *VARSUM* values internally calculated by the CE. Not selectable for PULSE3 and PULSE4 pulse generators.
0x24	36	External (host)	Indicates that the host will provide values in the APULSER, APULSEW, APULSE3, and APULSE4 registers and that the pulse generator should be updated on the next READY interrupt..

Table 6: Pulse Sources Defined by the *PULSE_SRCS* Register (2/2)

WRATE (0x2D)

This register controls the rate of the pulse generation for the PULSEW, PULSER, PUSE3 and PULSE4 output pins. The inverse pulse rate, expressed as Wh per pulse is:

$$Kh = \frac{VMAX\ IMAX}{In\_8 \cdot SUM\_CYCLES \cdot WRATE \cdot X} 1.5757 \quad Wh / Pulse$$

(X = value formed by *PULSE_SLOW* and *PULSE_FAST* bits in the *CONFIG* register)

Registers Used for Calibration

***CAL_IA* (0x24), *CAL_VA* (0x25), *CAL_IB* (0x26), *CAL_VB* (0x27), *CAL_IC* (0x28), *CAL_VC* (0x29):**

These registers adjust the gain for the current and voltage measurements of each phase for the purpose of calibration. The calibration factors have to be stored by the host and written to the registers of the 71M6515H after power-up. The allowed range is $(2^{15} – 1)$ to $–(2^{15} – 1)$. The default value of 16384 equals unity gain.

If a voltage measurement of phase C is higher than expected, CAL_VC has to be adjusted to:

CAL_VC = 16384 / (1 + error)

Error must be expressed as a fraction, not a percentage value.

If the percent error is +3.5%, the relative error is 0.035, and the calibration factor becomes:

CAL_VC = 16384 / (1 + 0.035) = 15829.952,

which is rounded up to15830.

***KVAR* (0x2F)**

This register holds the relative gain of the VAR calculation with respect to the Watt calculation. The value should always be 6444.

***PHADJ_A* (0x2A), *PHADJ_B* (0x2B), *PHAD_C* (0x2C)**

These registers hold the phase correction factors for channels A, B, and C. The values are used by the CE to compensate for phase errors induced by current transformers. The allowed range is $(2^{15}-1)$ to $-(2^{15}-1)$. See the Calibration Procedure section for applicable values.

If the CE is operated in Rogowski Coil mode, no phase compensation should be required. The default value is not zero and should need to be changed only slightly, if at all. See the Calibration section for details.

***QUANT_W* (0x36), *QUANT_VAR* (0x37), *QUANT_I* (0x38)**

These registers hold DC values that are added to each calculated product in order to compensate for internal quantization (a very small amount) and external noise. These values are normally set to zero. The LSB values for these variable are listed in Table 7.

Variable	LSB Value	Unit
QUANT_W	$(VMAX\ IMAX/\ In\_8)* 1.04173*10^{-9}$	W
QUANT_VAR	$(VMAX\ IMAX\ /\ In\_8)* 1.04173*10^{-9}$	VAR
QUANT_I	$(IMAX^2\ /\ In\_8^2)* 5.08656*10^{-13}$	A (rms)

Table 7: LSB Values for QUANT Variables

Nonlinearity is most noticeable at low currents, and can result from input noise and truncation. Nonlinearities can be eliminated using the *QUANT_W* register. The error can be seen as the presence of a virtual constant noise current that becomes dominant at small load currents.

The value to be used for *QUANT_W* can be determined by the following formula:

$$QUANT\_W = -\frac{\frac{error}{100} V \cdot I \cdot In\_8}{VMAX \cdot IMAX \cdot LSB}$$

Where error = observed error at a given voltage (V) and current (I),
VMAX = voltage scaling factor, as described in section Scaling of Measured Values
IMAX = current scaling factor, as described in section Scaling of Measured Values
LSB = QUANT LSB value = $1.04173*10^{-9}$W

Example: For a Wh measurement, an error of +1% was observed at 1A. If VMAX is 600V and IMAX = 208A, and if the measurement was taken at 240V, we determine *QUANT_W* as follows:

$$QUANT\_W = -\frac{\frac{1}{100}240 \cdot 1}{600 \cdot 208 \cdot 1.04173 \cdot 10^{-9}} = -18460$$

The negative value obtained by the calculation will compensate for the positive error. It does not matter which current value is chosen as long as the corresponding error value is significant (5% error at 0.2A used in the above equation will produce the same result for *QUANT_W*).

Input noise and truncation can cause similar errors in the VAR calculation that can be eliminated using the *QUANT_VAR* register.

***VFEED_A* (0x44), *VFEED_B* (0x45), *VFEED_C* (0x46)**

These registers hold the compensation factors for feedthrough used for calibrating Rogowski coils. The allowed range is (2^{15}-1) to -(2^{15}-1). See the section on Rogowski Coil Calibration for details.

Registers Controlling Basic Function and Settings of the 71M6515H

***CONFIG* (0x16)**

The four bytes written to this register determine the basic operation of the 71M6515H. The function of the 28 bits used for this register are explained below:

Bit 0: This bit (*VAH_SELECT*) determines the method used by the post-processor for determining the apparent energy measured in VAh. If the bit is 0 (**default**), the calculation is based on V_{RMS}, I_{RMS} and the time (t) per the formula:

$VAh = V_{RMS} * I_{RMS} * t$

The accuracy of the result can be improved for low currents by setting Bit 0 to 1. The calculation is then based on the Wh and VARh values per the formula:

$$VAh = \sqrt{Wh^2 + VARh^2}$$

Using the calculation method above, high accuracy can be achieved for low currents.

Bit 3: This bit (*RTM_EN*) enables the Real-Time Monitor function when set to 1.When used, the RTM signal is available at the TMUX pin.

Bit 4: This bit (*CE_EN*) enables the CE when set to 1. The CE has to be enabled for most metering functions.

Bits 7-5: These three bits (*EQU*) define the equation (see table below) to be implemented by the CE.

EQU	Watt & VAR Formula	Application
0	VA IA	1 element, 2W 1ø
1*	VA(IA-IB)/2	1 element, 3W 1ø
2	VA IA + VB IB	2 element, 3W 3 øDelta
3*	VA (IA - IB)/2 + VC IC	2 element, 4W 3ø Delta
4*	VA(IA-IB)/2 + VB(IC-IB)/2)	2 element, 4W 3ø Wye
5	VA IA + VB IB + VC IC	3 element, 4W 3ø Wye

Bits 13-8: These six bits (*SUM_CYCLES*) define the length of the accumulation interval τ per the formula:

$$\tau = \frac{SUM\_CYCLES \cdot 42}{2520.6}$$

Allowed values are 24 (400ms) through 60 (1000ms), unless the post-processor is disabled. Bit 8 is the LSB.

It is important to note that the length of the accumulation interval, as determined by *SUM_CYCLES,* is not an exact multiple of 1000ms. For example, if *SUM_CYCLES* = 60, the resulting accumulation interval is:

$$\tau = \frac{60 \cdot 42}{\frac{32768Hz}{13}} = \frac{2520}{2520.62Hz} = 999.75ms$$

This means that accurate time measurements should be based on the RTC, not the accumulation interval.

Bit 14: This bit (*CKOUT_DISB*) disables the CKOUT pin when set. The CKOUT pin can be used for diagnostics. For EMC compliance and power saving reasons, *CKOUT_DISB* should always be set.

Bit 15: This bit (*ADC_DIS*) disables the ADC when set, e.g. to save power. Of course, no metering or measuring can be performed with the ADC disabled.

Bits 18-16: These three bits (*TMUX*) select the source for the TMUX diagnostic output pin. For EMC compliance and power saving reasons, *TMUX* should be zero (default) if unused.

Bit 18 *TMUX2*	Bit 17 *TMUX1*	Bit 16 *TMUX0*	*TMUX*	Signal Selected for the TMUX Pin
0	0	0	0	GND
0	0	1	1	MUX_SYNC
0	1	0	2	RTM
0	1	1	3	RTC Output
1	0	0	4	CE_BUSY
1	0	1	5	XFER_BUSY
1	1	0	6	VX_OK (Comparator Output)
1	1	1	7	V3P3/2 =1.5V internal analog voltage

Bits 20-19: These two bits (*F_SELECT*) select the phase that is to be used for frequency measurement. The frequency will be shown in bits 31-16 of the *FREQ_DELTA_T* register (and as bit 4 of the STATUS word – in this form as a digitized zero crossing signal).

Bit 20 *F_SELECT1*	Bit 19 *F_SELECT0*	*F_SELECT*	Phase Selected
0	0	0	Phase A
0	1	1	Phase B
1	0	2	Phase C
1	1	3	Not allowed

Since the signal at the input selected with *F_SELECT* is used to synchronize filters and other processing stages in the CE, accuracy for most measurements will be reduced if no voltage is present at the selected phase input. Accuracy can be established by selecting the phase that carries a stable signal (A, B, or C).

Bit 21: This bit (*CE_ONLY*) disables the post-processor when set to 1. When the post-processor is disabled, the time-intensive computations of IPHASE, IRMS, VAh and VRMS are not performed, and therefore smaller accumulation times (*SUM_CYCLES* < 24*)* are permitted. In this case, the host is responsible for calculating IPHASE, IRMS, VAh and VRMS.

Bits 23-22: These two bits (*IMAGE*) select the code to be used by the CE. The CE can be operated in standard mode when using CTs and/or shunt resistor sensors or in Rogowski mode when using Rogowski coil sensors. In order to switch the operation mode, the CE has to be disabled first by clearing the *CE_EN* bit.

Bit 23 *IMAGE* 1	Bit 22 *IMAGE* 0	*IMAGE*	CE Code Selected
0	0	0	Standard (CT/shunt)
0	1	1	Rogowski coil
1	0	2	Standard (CT/shunt)
1	1	3	Standard (CT/shunt)

Bit 24: This bit (*RESET*), when reset, forces all internal states of the 71M6515H to their power-up default.

Bits 26-25: These two bits (*PULSE_SLOW, PULSE_FAST*) modify the speed of the pulse generator. *PULSE_SLOW* and *PULSE_FAST* determine the factor X in the equation used for Kh as shown in the table below.

PULSE_SLOW	*PULSE_FAST*	X
0	0	$1.5*2^2 = 6$
0	1	$1.5*2^6 = 96$
1	0	$1.5*2^{-4} = 0.09375$
1 (default)	1 (default)	1.5

PULSE_SLOW and *PULSE_FAST* will affect the operation of all four pulse outputs. See the Pulse Generation section for details.

Bits 29-27: These three bits (*IA_8X, IB_8X, IC_8X*) apply an additional gain of 8 to the IA, IB, and IC channels when set to 1. This is a useful tool when very small signals are encountered, as is the case when using current shunt resistors with very low resistance while operating at low currents. Care must be taken to avoid clipping. If the input to the meter exceeds IMAX/8, clipping will occur. These bits should normally be zero, unless additional gain following the ADC stage is needed.

Bit 30: This bit (*DEFAULT_PPM*) defines the source of temperature compensation. When *DEFAULT_PPM* is 1, the 71M6515H will automatically apply compensation coefficients derived from the stored VREF temperature characteristics to the *PPMC* and *PPMC2* registers. When *DEFAULT_PPM* is zero, the host is allowed to write its own values to the *PPMC* and *PPMC2* registers.

***STATUS* (0x14)**

The four bytes in this register reflect the status of the various measurement functions of the 71M6515H. This register is read only. When a bit in the *STMASK* register is set, an interrupt (IRQZ) is generated as soon as the corresponding bit in the *STATUS* register is set.

Bit 0: This bit (*BOOTUP*) signals a request from the 71M6515H to the host to be initialized.

Bit 1: This bit (*SAGA*), when set, indicates that the voltage applied to phase A has sagged below *SAGTHR*. See the for *SAG* register for a detailed description.

Bit 2: This bit (*SAGB),* when set, indicates that the voltage applied to phase B has sagged below *SAGTHR*.

Bit 3: This bit (*SAGC),* when set, indicates that the voltage applied to phase C has sagged below *SAGTHR*.

Bit 4: This bit (*F0)* follows the polarity of the input voltage selected with the *F_SELECT* bits in the *CONFIG* register. It represents a smoothed, filtered and squared copy of the fundamental waveform.

Bit 5: This bit (*MAXV),* when set, indicates that a voltage greater than the voltage limit defined in the *VI_PTHRESHOLD* register had been detected in the previous accumulation interval.

Bit 6: This bit (*MAXI),* when set, indicates that a current greater than the current limit defined in the *VI_PTHRESHOLD* register had been detected in the previous accumulation interval.

Bit 7: This bit (*1SECI,* toggles every second. It is controlled by the RTC.

Bit 8: This bit (*VXEDGE),* when set, indicates a change in state of VX comparator. This bit is updated every accumulation interval.

Bit 9: This bit (*DEDGE),* when set, indicates a change in state of any selected DIO pin. This bit is updated every accumulation interval. Pins have to be configured to generate the *DEDGE* flag using the *DIO_INT_CTRL* bits in the *D_CONFIG* register.

Bit 10: This bit (*XOVF),* when set, indicates that the host failed to read at least one of the Wh values. Between interrupts (indicated by the *READY* bit in the *STATUS* word), the 71M6515H expects the host to read at least one of the *WATTHR_A*, *WATTHR_B*, or *WATTHR_C* values.

Bit 11: This bit (*READY),* when set, indicates that the 71M6515H has fresh output values ready for the host. Setting this bit in *STMASK* will enable the hardware interrupt output pin IRQZ.

Bit 14-12: These bits (bit 12 for phase A, bit 13 for phase B, bit 14 for phase C*),* when set, indicate that the energy received from element A, B, or C is below the creep threshold defined in the *CREEP_THRSHLD* register or that the current in elements A, B, or C is below the threshold defined in bits 15-0 of the *START_THRESHLD* register. The creep condition flagged by bits 14-12 of the *STATUS* register indicates that Wh, VARh, and IRMS measurements of element A, B, or C have been zeroed out. Consequently, accumulation did not occur.

Bit 15: This bit (*CMD_IGNORED),* when set, indicates that the 71M6515H ignored the last command received from the host. The reason can be any type of command incompatibility, e.g. attempts to write to a read-only register.

Bit 16: This bit (*PULSEW_ERR),* when set, indicates that the pulse generator PULSEW is configured for external (host) input, but did not receive an update during the previous accumulation interval.

Bit 17: This bit (*PULSER_ERR),* when set, indicates that the pulse generator PULSER is configured for external (host) input, but did not receive an update during the previous accumulation interval.

Bit 18: This bit (*PULSE3_ERR),* when set, indicates that the pulse generator PULSE3 is configured for external (host) input, but did not receive an update during the previous accumulation interval.

Bit 19: This bit (*PULSE4_ERR),* when set, indicates that the pulse generator PULSE4 is configured for external (host) input, but did not receive an update during the previous accumulation interval.

***STMASK* (0x15)**

The four bytes in this register enable interrupts when the corresponding bit in the *STATUS* register is set. The default value for ***STMASK*** is zero.

When a bit in the *STMASK* register is set, an interrupt (IRQZ) is generated as soon as the corresponding bit in the *STATUS* register is set. Interrupts indicated by IRQZ do not necessarily have to be synchronized with accumulation intervals. For example, the toggling of a signal applied to the DIO pins (D0…D7), when the interrupt is enabled with the *DIO_INT_CTRL* register, can cause an interrupt at any time.

Registers Controlling Temperature Measurement and Compensation

***DEG_SCALE* (0x1C)**

This register holds the scale factor used to calculate the internal temperature value provided by the temperature sensor to temperature in degrees Celsius (°C). The default value is 22721 and should not be changed.

***FREQ_DELTA_T* (0x11)**

This register holds frequency and temperature information in two bytes each.

31 16	15 0
FREQUENCY (see Output Registers)	*DELTA_T*

Bits 15-0: These bits (*DELTA_T*) represent the temperature information relative to the value stored in the *TEMP_NOM* register. One LSB is equivalent to 0.1°C. The formula used for *DELTA_T* is:

$$DELTA\_T = -DEGSCALE * 2^{-22} * (TEMP\_RAW - TEMP\_NOM)$$

***TEMP_NOM* (0x13)**

This register holds the nominal (reference) temperature. During calibration, the host must write the value read from *TEMP_RAW* to *TEMP_NOM* in order to enable temperature compensation. See the Meter Calibration section for details. The temperature available in register *DELTA_T* is based on the difference between the current temperature, as provided in *TEMP_RAW*, and the reference temperature provided by *TEMP_NOM*.

***TEMP_RAW* (0x12)**

This read-only register holds the raw temperature provided by the temperature sensor on the 71M6515H chip. During calibration, the host must write the value read from *TEMP_RAW* to *TEMP_NOM* in order to enable temperature compensation.

Example: At calibration time, the raw temperature value of 853030 was read from the *TEMP_RAW* register and written to the *TEMP_NOM* register. At a later time, the raw temperature register reads 844866. The 71M6515H calculates the temperature difference to:

$$DELTA\_T = -DEGSCALE * 2^{-22} * (TEMP\_RAW - TEMP\_NOM) = 44$$

This value is interpreted as +4.4°C.

***PPMC1_2* (0x1B)**

This register holds the linear and squared compensation factors for the ADC temperature compensation. The allowed range is $(2^{15} - 1)$ to $-(2^{15} - 1)$. Both words are reset to zero if *TEMP_NOM* equals zero.

31 16	15 0
PPMC = ADC linear factor (PPMC = 26.84 * PPM/°C)	*PPMC2* = ADC quadratic factor (PPMC2 = 1374 * PPM/°C^2)

The 71M6515H performs ADC temperature compensation by computing a gain adjustment factor for both the voltage and current samples per the following equation:

$GAIN\_ADJ=16384+floor(1+DELTA\_T*PPMC/2^{14}+DELTA\_T^2*PPMC2/2^{23})$

Changes to ***PPMC1_2*** by the host are only allowed if the *DEFAULT_PPM* bit in the *CONFIG* register is zero. If additional temperature compensation by the host, e.g. for external components, is required, the procedure is as follows:

1) The host sets the *DEFAULT_PPM* bit in the *CONFIG* register to 1 and then reads *PPMC* and *PPMC2*.
2) The host then adds the compensation factors to *PPMC* and *PPMC2*, resets the *DEFAULT_PPM* bit in the *CONFIG* register to 0 and then writes the modified values to *PPMC* and *PPMC2*.

Y_DEG0 **(0x18)**

This register holds the constant compensation factor for the RTC temperature compensation. One LSB is equivalent to 0.1PPM.

Bits 31-16: These bits (*Y_CALC0*) represent the constant compensation factor.

Y_DEG1_2 **(0x19)**

This register holds the linear and quadratic compensation factors for the RTC temperature compensation.

31 16	15 0
Y_CALC1 = linear compensation factor. One LSB is equivalent to 0.01PPM/°	*Y_CALC2* = quadratic compensation factor. One LSB is equivalent to 0.001PPM/°C

Both *Y_DEG0* and *Y_DEG1_2* can be used to compensate the RTC to be accurate over the whole temperature range by characterizing the crystal.

Registers for Output Signals

PULSEW_R_CNTS **(0x41)**

This register contains the pulse count for the PULSEW and PULSER output pins for the past accumulation interval. The counters will be cleared at the beginning of each accumulation interval and then start counting up with each generated pulse.

Bit 15-0: The counter for the PULSER (VARh) generator.

Bit 31-16: The counter for the PULSEW (Wh) generator.

31 16	15 0
Counter for the PULSEW generator (Wh)	Counter for the PULSER generator (VARh)

At pulse rates that do not result in generation of whole counts per accumulation interval, e.g. 3 1/3 pulses, the count equivalent to the next lower natural number will be generated until the residue accumulates to a full count, i.e. the pulse sequence generated will be 3, 3, 3, 4, 3, 3, 3, 4…

PULSE3_4_CNTS **(0x42)**

This register contains the pulse count for the PULSE3 and PULSE4 output pins for the accumulation interval. The counters will be cleared at the beginning of each accumulation interval and then start counting up with each generated pulse.

Bit 15-0: The counter for the PULSE4 generator.

Bit 31-16: The counter for the PULSE3 generator.

31 16	15 0

Counter for the PULSE3 generator	Counter for the PULSE4 generator

***IASQSUM* (0x39), *IBSQSUM* (0x3A), *ICSQSUM* (0x3B)**

These registers hold the sum of the squared current samples collected during the previous accumulation interval. The values for *IASQSUM*, *IBSQSUM*, and *ICSQSUM* are provided directly by the CE and are not post-processed. The magnitude of the accumulated samples is determined by:

$$LSB = \frac{IMAX^2}{In\_8^2} 9.4045 \cdot 10^{-13} \; A^2h$$

***IASQFRACT* (0x4A), *IBSQFRACT* (0x4B), *ICSQFRACT* (0x4C)**

These read-only registers hold the difference between the 10-bit residual squared current sum of the current accumulation interval and the 10-bit residual squared current sum of the previous interval. If ***IASQSUM, IBSQSUM,*** or ***ICSQSUM*** are used to calculate current, the value obtained over several accumulation intervals will be accurate due to averaging, but the individual values will have a higher uncertainty than when using ***IASQFRACT, IBSQFRACT,*** and ***ICSQFRACT.***

The most accurate calculation of the squared current for a phase X (IXSQ) uses the formula:

IXSQ = $IXSQSUM + 2^{-10} \; IXSQFRACT$

***INSQFRACT* (0x4D)**

This register holds the difference between the 10-bit residual squared neutral currents of the current accumulation interval and the 10-bit residual squared neutral currents of the previous interval. The value can be used to improve the accuracy of the squared neutral current reading by applying the formula:

INSQ = $INSQSUM + 2^{-10} \; INSQFRACT$

***INSQSUM* (0x3C)**

This register holds the sum of the square of the calculated neutral current collected during the previous accumulation interval. The calculation is implementing the following equation:

$$INSQSUM = \sum (I0 + I1 + I2)^2$$

The magnitude of the accumulated samples is determined by:

$$LSB = \frac{IMAX^2}{In\_8^2} 9.4045 \cdot 10^{-13} \; A^2h$$

***IPHASE_ABC* (0x0F)**

This register holds voltage-to-current phase information for all three phases. Positive phase means lagging current (inductive load). One LSB is equivalent to 1 degree. The range is from (2^8 – 1) to –(2^8 – 1). Since the phase calculation involves the **post-processor**, these registers will not be functional when the *CE_ONLY* bit in the *CONFIG* register is set.

Bits 8-0: These bits (*IPHASE_C*) represent the voltage-to-current phase angle in phase C.

Bits 17-9: These bits (*IPHASE_B*) represent the voltage-to-current phase angle in phase B.

Bits 26-18: These bits (*IPHASE_A*) represent the voltage-to-current phase angle in phase A.

***IRMS_A* (0x0C), *IRMS_B* (0x0D), *IRMS_C* (0x0E)**

These registers hold the post-processed RMS current for each phase. Only the 16 most significant bits are used. The magnitude of the values is determined by:

$$LSB = \frac{6.8781 \cdot 10^{-9} \, IMAX}{In\_8\sqrt{SUM\_CYCLES}} \quad Arms$$

Since the RMS calculation involves the **post-processor**, these registers will not be functional when the *CE_ONLY* bit in the *CONFIG* register is set. If higher precision is required, the host must calculate the RMS currents from the values in the *IASQSUM*, *IBSQSUM*, and *ICSQSUM* registers. For even higher precision, the ***IASQFRACT, IBSQFRACT, ICSQFRACT*** registers should be used.

***Example**:* The register *IRMS_C* reads the value 2,079,670. Assuming IMAX to be 208A, and using the formula above, we determine the RMS current of phase C to:

$$I_{RMS} = 2079670 \cdot \frac{6.8781 \cdot 10^{-9} 208}{\sqrt{60}} = 0.0385A$$

***VASQSUM* (0x3D), *VBSQSUM* (0x3E), *VCSQSUM* (0x3F)**

These registers hold the sum of the squared voltage samples collected during the previous accumulation interval. The values for *VASQSUM*, *VBSQSUM*, and *VCSQSUM* are provided directly by the CE and are not post-processed. The magnitude of the accumulated samples is determined by:

$$LSB = VMAX^2 9.4045 \cdot 10^{-13} V^2 h$$

***VAH_A* (0x06), *VAH_B* (0x07), *VAH_C* (0x08)**

These registers hold the apparent energy collected during the previous accumulation interval. The magnitude of the accumulated samples is determined by:

$$LSB = 9.4045 \cdot 10^{-13} \frac{VMAX\ IMAX}{In\_8} \quad VAh$$

Since the VAh calculation involves the **post-processor**, these registers will not be functional when the *CE_ONLY* bit in the *CONFIG* register is set.

***VARH_A* (0x03), *VARH_B* (0x04), *VARH_C* (0x05)**

These registers hold the reactive energy collected during the previous accumulation interval. The magnitude of the accumulated samples is determined by:

$$LSB = 9.4045 \cdot 10^{-13} \frac{VMAX\ IMAX}{In\_8} \quad VARh$$

***VPHASE_ABC* (0x10)**

This register holds the phase angle between the voltages of phases A/C and A/B. The LSB is one degree.

Bits 15-0: These bits (*VPHASE_AC*) hold the phase angle between VA and VC.

Bits 31-16: These bits (*VPHASE_AB*) hold the phase angle between VA and VB.

***VRMS_A* (0x09), *VRMS_B* (0x0A), *VRMS_C* (0x0B)**

These registers hold the post-processed RMS voltage for each phase. Only the 16 most significant bits are used. The magnitude of the values is determined by:

$$LSB = \frac{6.8781 \cdot 10^{-9} VMAX}{\sqrt{SUM\_CYCLES}} \quad V\ rms$$

Since the RMS calculation involves the **post-processor**, these registers will not be functional when the *CE_ONLY* bit in the *CONFIG* register is set.

If higher precision is required, the host must calculate the RMS voltages from the values in the *VASQSUM*, *VBSQSUM*, and *VCSQSUM* registers.

***Example**:* The register *VRMS_B* reads the value 425,778,000. Assuming VMAX to be 600V, and using the formula above, we determine the RMS voltage of phase B to:

$$V_{RMS} = 425778000 \cdot \frac{6.8781 \cdot 10^{-9} 600}{\sqrt{60}} = 226.85V$$

***WH_A* (0x00), *WH_B* (0x01), *WH_C* (0x02)**

These registers hold the real energy collected during the previous accumulation interval. The magnitude of the values is determined by:

$$LSB = 9.4045 \cdot 10^{-13} \frac{VMAX\ IMAX}{In\_8} \quad Wh$$

***Example**:* The register *WH_A* reads the value 236,675 for one accumulation interval of one second. Assuming 600V for VMAX, 208A for IMAX, and unity gain, we determine the real energy to be:

E = 236,675*600*208*9.4045*10^{-13} Wh = 0.0277781Wh.

By multiplying with 3,600, we get 100Wh/h, which means the applied power is 100W.

***FREQ_DELTA_T* (0x11)**

This register holds frequency and temperature information in two bytes each.

Bits 31-16: These bits (*FREQUENCY*) represent the frequency of the input signal selected with the *F_SELECT* bit of the *CONFIG* register. One LSB is equivalent to 0.1Hz.

***MAIN_EDGE_CNT* (0x35)**

This register holds the number of zero crossings of the input phase selected by the *F_SELECT* bits in the *CONFIG* register detected in the previous accumulation interval. The value in ***MAIN_EDGE_CNT*** can be used by the host to correct its own RTC or to synchronize events to the line voltage.

Registers Controlling Alarms and Thresholds

***CREEP_THRSLD* (0x1D)**

The four bytes written to this register determine the creep threshold. Setting a creep threshold helps suppressing I2H, Wh and VARh readings when the values of WSUM and VARSUM are determined to be below the creep threshold.

Example: The creep threshold of a meter operating with an accumulation interval of 1000ms is to be configured to be 15mA at 240V. The meter is using a VMAX of 600V, an IMAX of 208A, and is not using the additional gain of 8. The numerical value for the *CREEP_THRSLD* register is to be determined.

With 15mA, the power per phase will be 3.6W, or 0.001Wh per second. With the LSB of WSUM readings given as 9.4045*10^{-13}*VMAX*IMAX [Wh], we determine the value to:

n = 0.001Wh / (9.4045*10^{-13}*VMAX*IMAX /In_8 Wh) = 8520.2

The rounded down value of 8520 is written to the *CREEP_THRSLD* register.

***SAG* (0x2E)**

This register holds the voltage and timing threshold for sag detection.

Bits 15-0: These bits (*SAG_CNT*) hold the sag count. A sag condition must persist for at least *SAG_CNT* samples before a sag alarm is generated. The allowed range is 1 to (2^{15}-1), and the default is 80 (31.7ms). The time period defined by *SAG_CNT* is:

T = *SAG_CNT**397µs

Bits 31-16: These bits (*SAGTHR*) hold the voltage threshold that is to be applied for sag detection. The peak voltage must exceed *SAGTHR* once each *SAG_CNT* samples in order to prevent a SAG warning. One LSB is defined as:

$$LSB = 7.8798 \cdot 2^{16} \cdot 10^{-9}\ VMAX$$

Example: A meter operating at 50Hz and 240V (RMS) is supposed to apply a sag threshold of 180V (RMS) for at least four periods before a sag warning is issued. VMAX is 600V. Which values are to be selected for *SAG*?

Four periods translate to T = 4 * 20ms = 80ms. This means that

SAG_CNT = *T*/397µs = 202.

180V (RMS) translate to 255V (peak), so *SAGTHR* is determined by

$$SAGTHR = \frac{255}{LSB} = \frac{255}{7.8798 \cdot 2^{16} \cdot 10^{-9}\ 600} = 823$$

***START_THRESHLD* (0x40)**

This register holds the voltage and current thresholds that apply to the calculation of frequency, zero crossings, voltage phase and energy values. If the current is below the value stored in *I_START*, calculation of RMS current, and energy (Wh, VARh and VAh) is suppressed.

Bits 15-0: These bits (*I_START*) hold the threshold to be applied for under-current. If ISQSUM< *I_START*, all post-processed values are set to zero for that phase. This includes reported values for Wh, VARh, VAh, IRMS, VPHASE, IPHASE, PULSER, PULSEW, PULSE3 and PULSE4. This applies only if *CREEP_THRSLD* is not set to zero. One LSB is defined as:

$$LSB = \frac{IMAX^2}{In\_8} \cdot 9.4045 \cdot 10^{-13}\ A^2h$$

Elements with ISQSUM< *I_START* will set the creep bits in the *STATUS* register.

Bits 31-16: These bits (*V_START*). hold the threshold to be applied for under-voltage. If VRMS<*V_START*, the values for frequency (register *FREQ_DELTA_T*), zero crossings (register *MAIN_EDGE_CNT*), and voltage phase (register *V_PHASE_ABC*) are set to zero. Additionally, if VRMS< *V_START*, the reported value of VRMS is set to zero. One LSB is defined as:

$$LSB = VMAX^2 \cdot 2^{16} \cdot 9.4045 \cdot 10^{-13} V^2h$$

Elements with VRMS< *V_START* will **not** set the creep bits in the *STATUS* register.

***VI_PTHRESHOLD* (0x17)**

This register holds the threshold for over-voltage and over-current alarms.

Bits 15-0: These bits (*I_PTHRESHOLD*) hold the threshold to applied for over-current alarm. The threshold comparison is applied to the upper 16 bits of the values in *IRMS*: One LSB is defined as:

$$LSB = \frac{450.76 \cdot 10^{-6}\ IMAX}{In\_8\sqrt{SUM\_CYCLES}} \quad Arms$$

Bits 31-16: These bits (*V_PTHRESHOLD*). hold the threshold to applied for over-voltage alarm. The threshold comparison is applied to the upper 16 bits of the values in *VRMS* One LSB is defined as:

$$LSB = \frac{450.76 \cdot 10^{-6} VMAX}{\sqrt{SUM\_CYCLES}} \quad V\ rms$$

Example: A meter designed with VMAX=600V and IMAX=208A is supposed to apply an overvoltage threshold of 520V (RMS) and an over-current threshold of 400A (RMS). Which values are to be selected for ***V_PTHRESHOLD and I_PTHRESHOLD***?

$$V\_PTHRESHOLD = \frac{520}{LSB} = \frac{520}{\frac{450.76 \cdot 10^{-6} 600}{\sqrt{SUM\_CYCLES}}} = 14{,}893$$

$$I\_PTHRESHOLD = \frac{400}{LSB} = \frac{400}{\frac{450.76 \cdot 10^{-6} 208}{\sqrt{SUM\_CYCLES}}} = 33{,}046$$

Registers Controlling Time and RTC Functions

***OP_TIME* (0x1E)**

This register holds the operating time expressed in 1/100 hours. The register will be reset to zero whenever the host writes time or date to the RTC.

***RTC_DATE* (0x20)**

This register holds the date information provided by the RTC. The register can be written to in order to set the date.

Bits 15-8: These bits contain the year information (0 to 255). The value 0 represents the year 2000.

Bits 23-16: These bits contain the month information (01 to 12). The value 01 represents January.

Bits 31-24: These bits contain the day of month information (01 to 31).

***RTC_TIME_DAY* (0x1F)**

This register holds the time and day information provided by the RTC. The register can be written to in order to set the time.

Bits 7-0: These bits contain the day of the week (01 to 07). The value 01 represents Sunday.

Bits 15-8: These bits contain the hour information (00 to 23). The value 00 represents midnight.

Bits 23-16: These bits contain the minutes information (00 to 59).

Bits 31-24: These bits contain the seconds information (00 to 59).

***Example**:* The value 200835 is read from the *OP_TIME* register. This means that the meter has been running since the last reset or power-up for

t = 800850/100h = 8008.50h or 8,008h and 30 minutes (333.6875 days or 333 days and 16.5h).

Registers Used for Test Functions

***RTM* (0x21)**

This register controls the Real-Time Monitor. When the *RTM_EN* bit in the *CONFIG* register is set, the values of CE RAM locations specified with the *RTM* register can be routed to the TMUX pin as a serial data stream. The TMUX bits in the *CONFIG* register must be set to 3 in order to select the RTM output for the TMUX pin.

Bits 7-0: These bits (*RTM3*) select the CE address for RTM3.

Bits 15-8:. These bits (*RTM2*) select the CE address for RTM2.

Bits 23-16: These bits (*RTM1*) select the CE address for RTM1.

Bits 31-24: These bits (*RTM0*) select the CE address for RTM0.

***SSI* (0x22)**

This register controls the function of the Serial Synchronous Interface (SSI). The function of the SSI is described in the Internal Resources section of this data sheet. If the SSI is enabled (bit 23, *SSI_EN*, in the *SSI* register), a block of *CNT* words starting at the address *BEG* will be transmitted each 397µs.

Bits 7-0: These bits (*CNT*) select the number of CE RAM address locations to be transmitted. The value in *CNT* must be >= 0.

Bits 15-8: These bits (*BEG*) define the start address of the transfer region of the CE data RAM address.

Bit 16: This bit must be set to zero.

Bit 17: This bit must be set to zero.

Bit 18: This bit (*SSI_FPOL*) defines the polarity of the SFR pulse signal (0: positive, 1: negative).

Bits 20-19: These bits (*SSI_FSIZE*) define the frame pulse format as follows:

Bit 20	Bit 19	*SSI_FSIZE*	SSI Frame Pulse Format
0	0	0	Once at beginning of SSI sequence
0	1	1	Every 8 bits
1	0	2	Every 16 bits
1	1	3	Every 32 bits

Bit 21: This bit (*SSI_CGATE*) enables the clock to be gated. When low, the SSCLK signal is active continuously, when high, the SSCLK signal is held low when no data is being transferred.

Bit 22: This bit (*SSI_10M*) defines the speed of the SSCLK signal: 0: 5MHz, 1: 10MHz.

Bit 23: This bit (*SSI_EN*), when set to 1, enables the SSI interface.

Registers Used for I/O Control

***D_CONFIG* (0x1A)**

This register holds three bytes that are used to manipulate the DIO pins of the 71M6515H.

Bits 7-0: These bits (*DIO_VALUE*) form the data register for the DIO pins D0 through D7. When a byte is written to *DIO_VALUE*, the pins configured as outputs (using the *D_DIR* register) will change their state accordingly. Pins configured as inputs will ignore the byte written to *DIO_VALUE*.

Reading *DIO_VALUE* will return a byte that reflects the state of all pins regardless whether they are configured as inputs or outputs.

Bits 15-8: These bits are not used

Bits 23-16: These bits (*D_DIR*) define the data direction. Bit 0 controls the D0 pin, bit 7 controls the D7 pin. Setting the bit corresponding to a pin to 1 makes the pin an output, clearing it to 0 makes it an input.

Bits 31-24: These bits (*DIO_INT_CTRL*) form a mask enabling the *DEDGE* interrupt (bit 9 of the *STATUS* word register). Bit 8 controls the D0 pin, bit 15 controls the D7 pin. Setting the bit corresponding to a pin to 1 enables the DEDGE interrupt, clearing the bit disables the interrupt. If the bit in DIO_INT_CTRL is set and a transition from high to low or from low to high occurs, the *DEDGE* interrupt bit in the *STATUS* word register will be set in the following accumulation interval.

Example: DIO pins D0 through D3 are to be configured as outputs, while D4 through D7 are to be inputs. DIO7 must generate a *DEDGE* interrupt when the input value changes, and D0 through D3 must apply the hexadecimal pattern 0x05. This makes the selection for the *D_CONFIG* registers as follows:

DIO_INTCTRL = 0x80, *D_DIR* = 0x0F, *DIO_VALUE* = 0x05

The values are combined into the 32-bit pattern 0x800F0005.

Example: D0 through D5 are to be configured as outputs, while D6 and D7 are to be inputs. D6 and D7 must generate a *DEDGE* interrupt when their input value changes. This makes the selection for the *D_CONFIG* registers as follows:

DIO_INTCTRL = 0xC0, *D_DIR* = 0x3F

The values are combined into the 32-bit pattern 0xC03F0000.

Registers in Numerical Order

Address	Name
0x00	*WH_A*
0x01	*WH_B*
0x02	*WH_C*
0x03	*VARH_A*
0x04	*VARH_B*
0x05	*VARH_C*
0x06	*VAH_A*
0x07	*VAH_B*
0x08	*VAH_C*
0x09	*VRMS_A*
0x0A	*VRMS_B*
0x0B	*VRMS_C*
0x0C	*IRMS_A*
0x0D	*IRMS_B*
0x0E	*IRMS_C*
0x0F	*IPHASE_ABC*
0x10	*VPHASE_ABC*
0x11	*FREQ_DELTA_T*
0x12	*TEMP_RAW*
0x13	*TEMP_NOM*
0x14	*STATUS*
0x15	*STMASK*
0x16	*CONFIG*
0x17	*VI_PTHRESH*
0x18	*Y_DEG0*
0x19	*Y_DEG1_2*
0x1A	*D_CONFIG*
0x1B	*PPMC1_2*
0x1C	*DEG_SCALE*
0x1D	*CREEP_THRSLD*
0x1E	*OP_TIME*
0x1F	*RTC_TIME_DAY*

Address	Name
0x20	*RTC_DATE*
0x21	*RTM*
0x22	*SSI*
0x23	RESERVED
0x24	*CAL_IA*
0x25	*CAL_VA*
0x26	*CAL_IB*
0x27	*CAL_VB*
0x28	*CAL_IC*
0x29	*CAL_VC*
0x2A	*PHADJ_A*
0x2B	*PHADJ_B*
0x2C	*PHADJ_C*
0x2D	*WRATE*
0x2E	*SAG*
0x2F	*KVAR*
0x30	*APULSEW*
0x31	*APULSER*
0x32	*APULSE3*
0x33	*APULSE4*
0x34	*PULSE_WIDTH*
0x35	*MAIN_EDGE_CNT*
0x36	*QUANT_W*
0x37	*QUANT_VAR*
0x38	*QUANT_I*
0x39	*IASQSUM*
0x3A	*IBSQSUM*
0x3B	*ICSQSUM*
0x3C	*INSQSUM*
0x3D	*VASQSUM*
0x3E	*VBSQSUM*
0x3F	*VCSQSUM*

Address	Name
0x40	*START_THRESHLD*
0x41	*PULSEW_R_CNTS*
0x42	*PULSE3_4_CNTS*
0x43	*PULSE_SRCS*
0x44	*VFEED_A*
0x45	*VFEED_B*
0x46	*VFEED_C*
0x47	
0x48	
0x49	
0x4A	*IASQFRACT*
0x4B	*IBSQFTACT*
0x4C	*ICSQFRACT*
0x4D	*INSQFRACT*
0x4E	*GAIN_ADJ*
0x60	*CE_PROG_ADDR*
0x61	*CE_DATA_ADDR*
0x62	*CE_PROG*
0x63	*CE_DATA*
0x64	*CE_PROG_INC*
0x65	*CE_DATA_INC*

APPLICATION INFORMATION

Meter Circuits

Bits 7 through 5 (*EQU*) of the *CONFIG* register allow the selection of the metering equation that is to be implemented by the 71M6515H. The equation to be used depends on the meter configuration.

Figure 15 shows how the 71M6515H is connected for the most common configuration, the three-phase, four-wire WYE. The neutral wire connects to V3P3A. For this configuration, equation 5 must be selected.

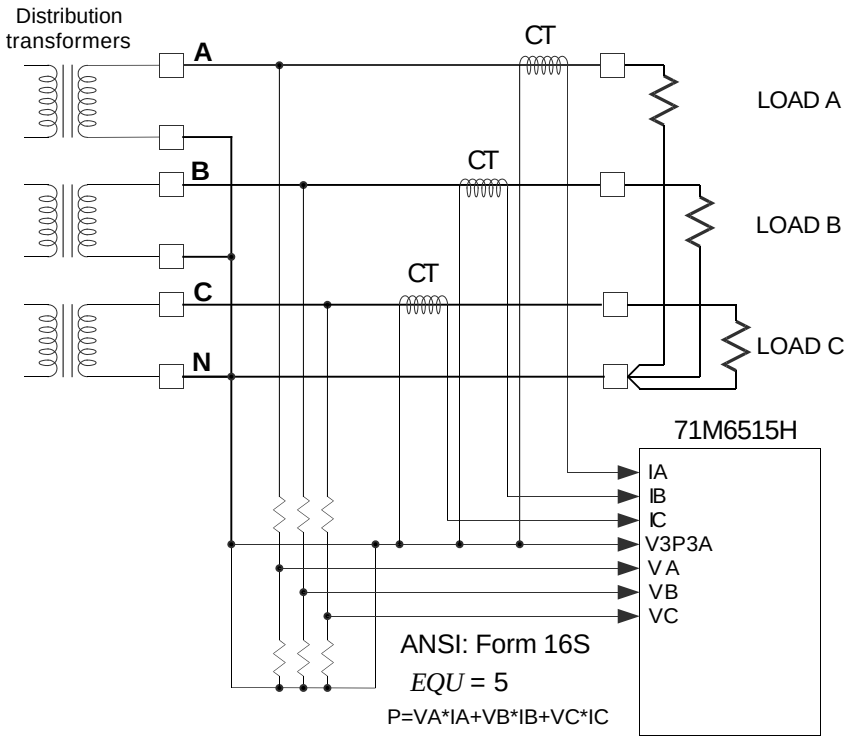


Figure 15: 4-Wire 3-Phase WYE Connection

In many three-phase three-wire configurations, one phase can be grounded, as shown in Figure 16. Again, the grounded wire is connected to V3P3A. For this configuration, equation 2 must be selected.

The four-wire three-phase delta configuration is shown in Figure 19. In this case, the center tap of the transformer that provides the A-C voltage is grounded. the grounded wire is connected to V3P3A. For this configuration, equation 2 must be selected. For this configuration, equation 3 must be selected, i.e. P = VA*(IA-IB)/2 + VC*IC.

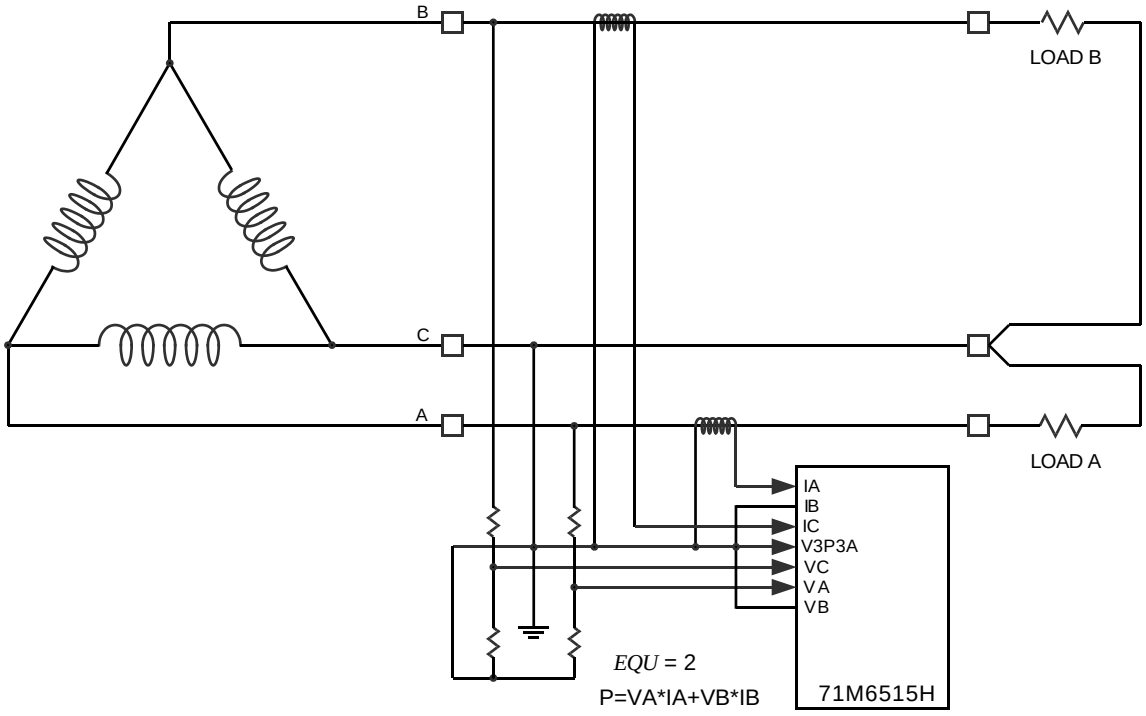


Figure 16: 3-Wire 3-Phase Delta Connection

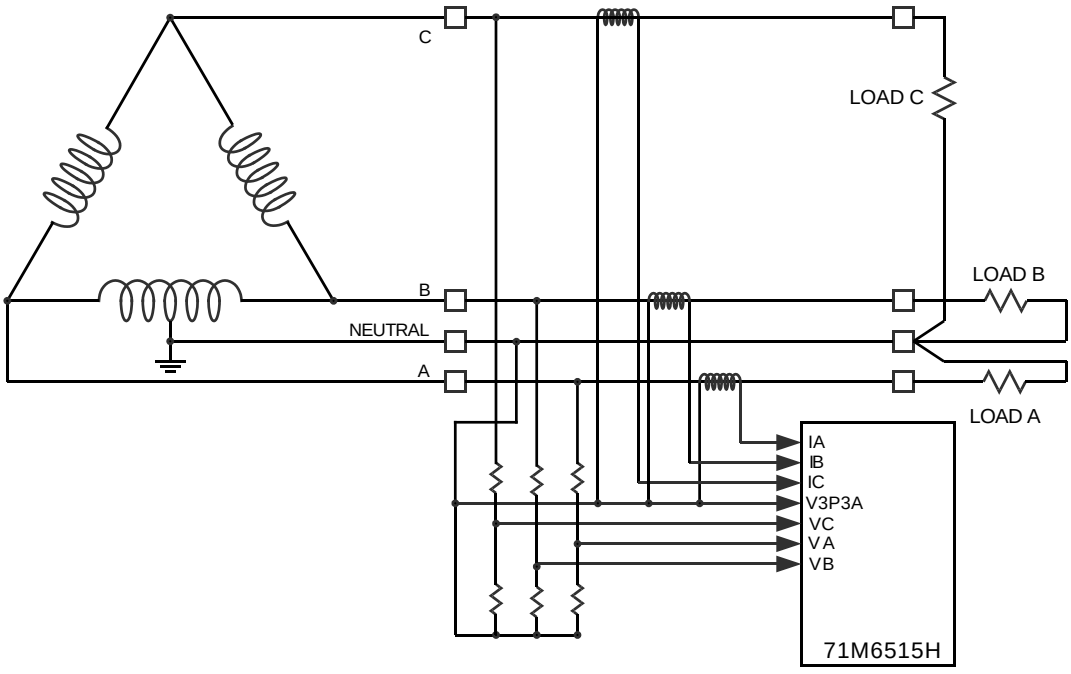


Figure 17: 4-Wire 3-Phase Delta Connection

Communication between the 71M6515H and the Host Processor

General

To ensure proper transfer of energy and other values from the 71M6515H to the host, the output data of the 71M6515H must be read by the host each time they are ready, and no energy-related datum can be missed. This requires close synchronization between the 71M6515H and the host.

Control Signals

Figure 18 shows the control signals between the 71M6515H and the host processor. These signals are:

1) TX: Serial transmit output pin of the 71M6515H
2) RX: Serial receive input pin of the 71M6515H
3) IRQZ: Interrupt output, used as “Data Ready” hardware signal of the 71M6515H (low-active)
4) RESETZ: Reset input pin of the 71M6515H (low-active, should be pulled up to V3P3)
5) UARTCSZ: UART reset input pin of the 71M6515H (low-active)
6) BAUD_RATE: Baud rate select input pin of the 71M6515H (optional)
7) PULSE_INIT: Pulse polarity select input pin of the 71M6515H (optional)

TX and RX are the most essential signals for the communication between the 71M6515H and the host processor. The IRQZ pin provides a useful output signal that can be used by the host to determine whether the 71M6515H has fresh data ready. IRQZ can be connected to either an interrupt input or general I/O input of the host processor.

RESETZ can be used to force a hardware reset of the 71M6515H, and UARTCSZ can be used to reset (purge) the UART of the 71M6515H communication buffers for reconfiguration. The additional pins BAUD_RATE and PULSE_INIT can be hard-wired for configuring the communication baud rate and the pulse status, or controlled on power up by the host processor.

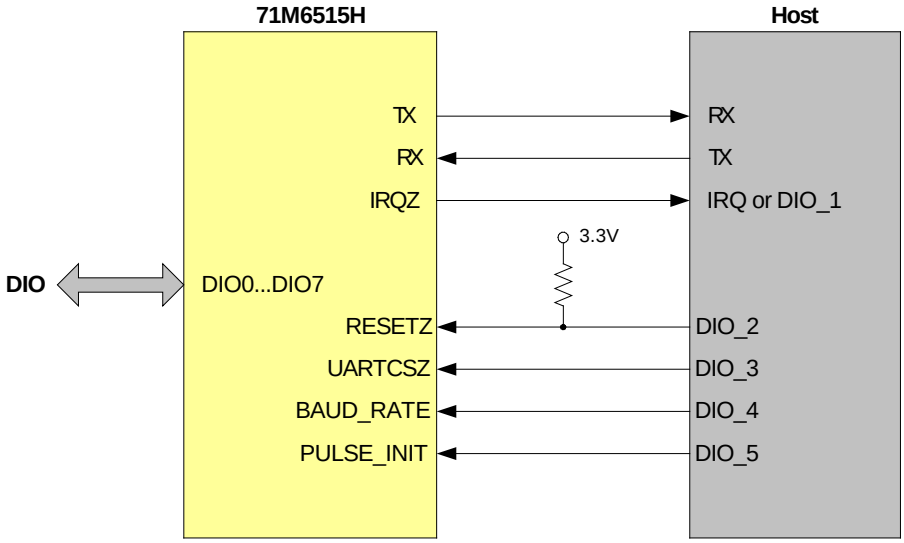


Figure 18: Connections between 71M6515H and Host

Note that the DIO pins of the host processor used to control the 71M6515H are not lost, since the 71M6515H can provide eight DIO pins ((DIO0…DIO7) to act as general-purpose DIO pins.

Since the communication between the 71M6515H and its host is based on a binary protocol, it is imperative for the host to issue a clean character stream without added bytes (UART drivers of high-level operating systems often add extra bytes to the character stream, relying on error-detecting protocols). In case the 71M6515H loses synchronization due to unexpected bytes sent by the host, it times out after 10ms (maximum 20ms). The 71M6515H flags a time-out condition by setting the *BOOTUP*

flag in the *STATUS* register. This happens because the incomplete or garbled data could have included a write command to the *CONFIG* register or other important registers.

Methods of Control

Two different methods of control can be used by the host processor:

1) Synchronization using the IRQZ pin of the 71M6515H (interrupt or DIO pin polling method, see Figure 19):

   a. Interrupt Method: The IRQZ pin of the 71M6515H is connected to a pin of the host processor that can generate an interrupt for the host processor. This is the easiest method for synchronization between the 71M6515H and the host. The *CONFIG* register of the 71M6515H is set up to generate an interrupt on the IRQZ pin whenever fresh data are ready, and the interrupt service routine of the host processor reads the fresh data out of the 71M6515H.

   b. DIO pin polling method: The IRQZ pin of the 71M6515H is connected to a DIO pin of the host processor. The host processor polls the status of the DIO pin as frequently as possible or through a timer-based polling method. The *CONFIG* register of the 71M6515H is set up to have the IRQZ pin to go low on every fresh data ready status, and the timer-serviced polling of the host processor will monitor the status of the DIO pin and initiate the serial communication when IRQZ is detected. For this method to be effective, the firmware of the host processor must maintain the timer interrupt to be the highest priority, followed by the serial communications priority.

2) Polling the *READY* bit in the *STATUS* word of the 71M6515H (status polling method, see Figure 20).
   This method requires that the host processor utilizes a timer with 1ms to 5ms resolution tied into the highest-priority interrupt. The interrupt service routine must initiate reading the *STATUS* register, preferably at least every 10ms, in order to monitor the *READY* bit, but the host processor must wait for the response of each status request. Otherwise, the *STATUS* register read operations will be stacked in the 71M6515H resulting in multiple responses.
   If a delayed response is received upon a *STATUS* register read, the host processor will know that the 71M6515H is within its post-processing period, which makes it necessary hat the host waits for the response. Every time the *READY* bit in the *STATUS* register is not set, indicating that data is not available, the host should poll again

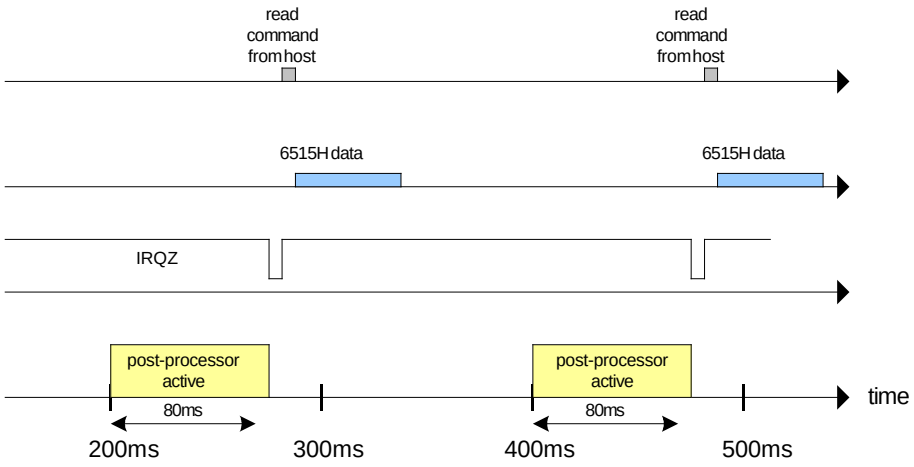


Figure 19: Timing Diagram (Using IRQZ, *SUM_CYCLES* = 12)

The communication between the 71M6515H and the host processor can always be reset without disturbing the metering function by utilizing the UARTCSZ and BAUDRATE pins. Configuring the BAUDRATE pin without resetting the UART buffers is not recommended. The UART of the 71M6515H can be “reset” by pulling the UARTCSZ pin low. This will force the UART back into the default configuration while clearing all buffers (UART buffers, UART-related buffers in the firmware).

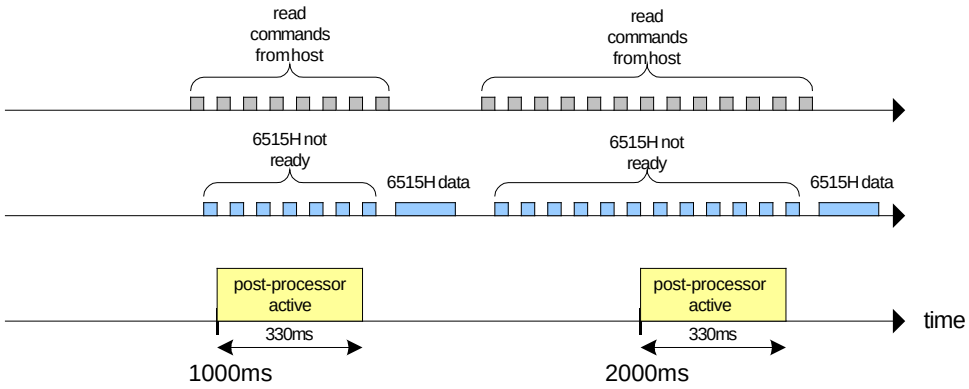


Figure 20: Timing Diagram (Host Polling)

Communication Steps for Interrupt Method:

The following is a list of commands required from the host processor to establish communication with the 71M6515H.

1) Establish host baud rate and data format as required by the 71M6515H.
2) Configure the DIO pins (D0…D7), if required, using the *D_CONFIG* register
3) Configure the 71M6515H by selecting the CE image (bits 23-22), equation (bits 7-5), pulse rate (bits 26-25), followed by enabling the CE (bit 4 in the *CONFIG* register). The bit pattern sent to *CONFIG* should have all bits set to their default state, as given in the Register Table.
4) Write the *TEMP_RAW* value obtained at calibration into the *TEM_NOM* register to enable temperature compensation.
5) Write the calibration coefficients into registers *CAL_IA, CAL_VA, CAL_IB, CAL_VB, CAL_C, CAL_VC, PHADJ_A, PHADJ_B, PHADJ_C*. Write calibration values to the *VFEED_A/B/C* registers if the Rogowski image is used.
6) Configure *WRATE* with the value required to generate the desired pulse rate.
7) Establish creep, sag and over/under voltage/current thresholds, if necessary, by writing values to the *CREEP_THRSLD, SAG, VI_PTHRESH,* and *VI_THRSHLD* registers.
8) Set the *READY* bit in the status mask *STMASK* in order to enable the generation of interrupts on the IRQZ pin.
9) Read at least one accumulated value register (*WATTH_X*, or *VAH_X*, or *VARH_X*).
10) Wait for the IRQZ pin to go low.
11) After receiving the interrupt, read at least one accumulated value register (*WATTH_X*, or *VAH_X*, or *VARH_X*) in order to maintain interrupt generation. Read the bits in the *STATUS* word to detect potential faults (overflow signaled by the *XOVF* flag or uninitialized condition signaled by the *BOOTUP* flag) or warnings and events (sag, creep, excessive voltage or current, DIO signal changes). If necessary, take corrective action.
12) After reading the required data from the 71M6515H, configuration changes should be made, if necessary. These configuration changes should be completed before the pre-processing period begins again.

Timing

The fundamental factor for all timing considerations is *SUM_CYCLES*, which determines the length of the accumulation interval for the 71M6515H per the equation:

$$\tau = \frac{SUM\_CYCLES \cdot 42}{2520.6Hz}$$

The default setting for *SUM_CYCLES* is 60, which yields an accumulation interval close to 1,000ms. A conservative minimum number for *SUM_CYCLES* is 24, which yields an accumulation interval close to 400ms. Both calculations by the post-processor in the 71M6515H and the communication between 71M6515H and the host have to be completed within the accumulation interval. If an accumulation interval has passed, and the energy values have not been read by the host, they are lost forever.

In order to analyze the timing of the communication between the 71M6515H and the host, it is useful to know the basic timing requirements of the post-processor of the 71M6515H. Some timing parameters are listed in Table 8.

CE_ONLY	VAh Calculation	Resulting Calculation Time
Disabled	Vector method: $VAh = \sqrt{Wh^2 + VARh^2}$	350ms
Disabled	Vrms*Irms method	80ms
Enabled	X	40ms

Table 8: Post-processor Timing

As can be seen in Table 8, the calculation time can be greatly reduced if the VAh values are calculated using the method of multiplying Vrms by Irms (by resetting bit 0 in the *CONFIG* register), which is less accurate at low currents.

Further improvement can be achieved by disabling the post-processor using the *CE_ONLY* bit in the *CONFIG* register. This is possible for applications where the registers *IPHASE*, *IRMS*, *VAh* and *VRMS* are not required.

It becomes clear now that the minimum value of 24 for *SUM_CYCLES*, equivalent to a 400ms accumulation interval, accommodates the worst-case scenario, using the vector method, which requires 350ms post-processing time. This setting leaves around 50ms for the communication to take place between the 71M6515 and the host. If the simpler Irms*Vrms method is chosen for VAh, a lower value can be selected for *SUM_CYCLES*.

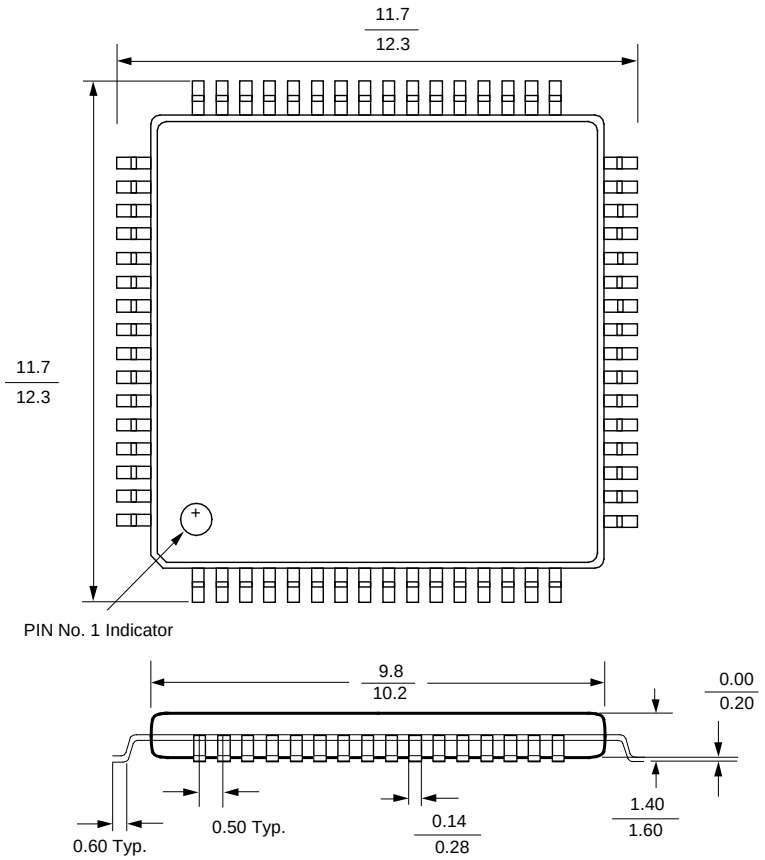
Lower values for *SUM_CYCLES*, for example 12, yielding a 200ms accumulation interval, are possible, leaving still 120ms for host communications, as long as the Vrms*Irms method for VAh is used.

Some other timing parameters are listed in Table 9.

Parameter	Value	Comment
Time from power-up to UART being functional	370ms ±10%	
Time from HW reset to UART being functional	370ms ±10%	
Time from soft reset to UART being functional	245ms ±10%	Soft reset = *RESET* bit in *CONFIG* register is set high.
Time from UARTCSZ pin low to UART being functional	20ms	UARTCSZ is polled just before the 71M6515H checks its data buffer for a command. This means that the command latency specified in the Electrical Specifications section also applies to the UARTCSZ pin.

Table 9: UART Timing Parameters

PACKAGE OUTLINE



NOTE: Controlling dimensions are in mm

Ordering Information

PART DESCRIPTION	ORDER NO.	PACKAGING MARK
71M6515H 64-Pin LQFP Lead-Free, 10PPM/°C VREF	71M6515H-IGT/F	71M6515H-IGT
71M6515H 64-Pin LQFP Lead-Free, 10PPM/°C VREF, T&R	71M6515H-IGTR/F	71M6515H-IGT
71M6515H 64-Pin LQFP Lead-Free, 40PPM/°C VREF	71M6515H-IGTW/F[1]	71M6515H-IGTW
71M6515H 64-Pin LQFP Lead-Free, 40PPM/°C VREF, T&R	71M6515H-IGTWR/F[1]	71M6515H-IGTW

[1] 71M6515H-IGTW requires program loading by the customer. Please contact factory for more information.

REVISION HISTORY

Revision	Date	Description
Rev. 1.0	October 26, 2005	First publication.
Rev. 1.1	December 11, 2006	Changed capacitor values for XIN/XOUT Corrected addresses for CE_DATA and made addresses CE_DATA etc. visible in table "Registers in Numerical Order". Changed frequency range to 46-64Hz and "Real-time clock for TOU" to "Real-time clock with temperature compensation" on title page. Added complete chapter on communication between host and 6515H. Changed pin name V1 to VFLT in Electrical Specification. Consolidated spelling for CREEP_THRSLD register. Added explanation for X in formula for WRATE. Added information on processing time for registers involving post-processing. Changed default value for WRATE to 683. Deleted note on low-pass filter in the CE in *CONFIG* register description. Added note at *CONFIG* register description stating that phase with stable voltage can be selected with F_SELECT to avoid inaccurate measurements and note stating that PULSE_SLOW and PULSE_FAST affect all four pulse sources. Added diagram "Connections between 71M6515H and host".
Rev. 1.2	March 15, 2007	Added I/O Equivalent Circuit diagrams and circuit type numbers in Pin Descriptions. Added note in Pin Descriptions stating that the voltage at RX must not exceed 3.6V. Added VREF aging data. Clarified polarity of SSDAT and SSCLK pins.
Rev. 1.3	August 17, 2007	Changed recommended value for capacitors at XIN/XOUT to 22pF. Changed recommended crystal to ECS ECX-3TA series. Added note on exact length of default accumulation interval. Corrected bit locations for *D_CONFIG* register. Added note in pin description for D0-D7 and Digital I/O" section: D0 through D7 are high impedance after reset or power-up and are configured as outputs and driven low 140ms after RESETZ goes high. Updated default values for *VIPTHRESH* and *VI_THRESH*.
Rev. 1.4	March 5, 2008	Changed pin and register names to PULSEW and PULSER and updated block diagram (Figure 2), updated pin-out diagram with corrected pin names. Removed COMPARATOR table in ELECTRICAL SPECIFICATIONS. Changed note for SRDY in pin description table to "SRDY should be tied to ground", deleted Figure 13 (SRDY function) and removed all text describing the function of SRDY (except that SRDY should be grounded), deleted Figure 13 (SSI Timing w/ SRDY) and removed references to SRDY in Figure 12. Consolidated spelling of Y_CALC etc. constants in section "Temperature Compensation for the Crystal and RTC" and in the register tables. Added reference to fast calibration procedure (AN_651X_022). Added diagrams for metering configurations. Improved Table 6 and explanation of PULSE_SRC register. Changed capacitor values for XIN/XOUT to 27pF and added recommended load capacitance value (12.5pF). Changed register name at location 0x38 from *QUANT_V* to *QUANT_I*. Removed non lead-free packages from Ordering Information. Updated Teridian street address. Added text at explanation of bits 14-12 of the *STATUS* register stating that these bits are also set when the current is below the threshold defined by bits 15-0 of the *START_THRESHLD* register. Added at explanation of *START_THRESHLD* : "Elements with VRMS< *V_START* will not set the creep bits in the *STATUS* register" and "Elements with ISQSUM< *I_START* will set the creep bits in the *STATUS* register".

		Added value for $R\theta_{JA}$ in Electrical Specification.
Rev 1.5	January 18, 2011	Changes for transition to Maxim DC: - Title page: Deleted reference to temperature range in 0.1% Wh accuracy statement. Deleted “Protects accumulated data” under “Battery Backup”. - Deleted reference to “patented” technology - Deleted Figure 6 (Typical Meter Accuracy over Temperature) Added Guaranteed By Design notes to Electrical Specifications. Changed the Crystal Oscillator electrical specification TYP from blank to 3. Changed the Capacitance to DGND Xin and Xout TYP from blank to 5. Deleted the MAX values. Changed the ADC Converter, V3P3 Reference electrical specification THD 250mV-pk TYP from blank to -75. Changed the THD 20mV-pk TYP from blank to -90. Deleted the MAX values.
Rev 1.6	July 8, 2011	Added 71M6515H-IGTW to the data sheet. Added footnotes to VREF and temperature sensor specifications.

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