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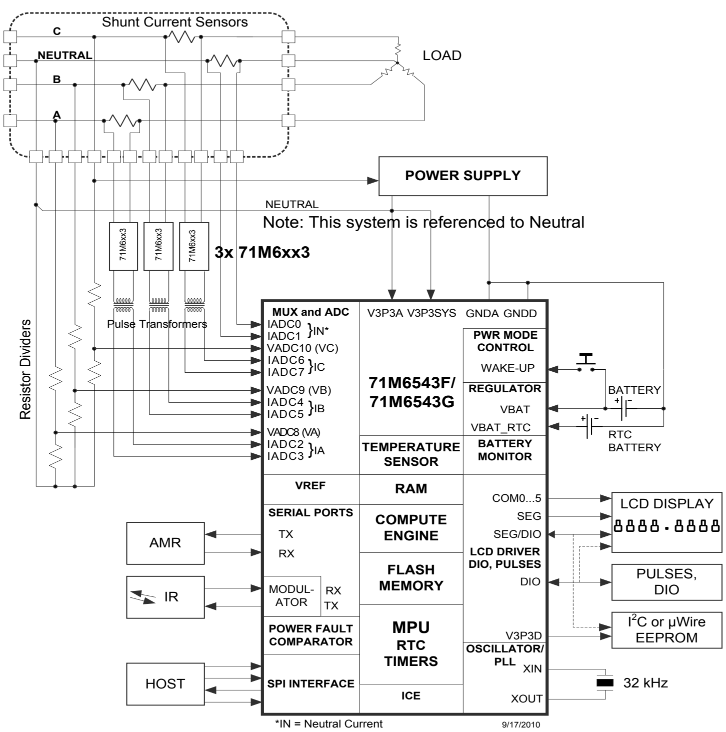
71M6543F/71M6543G Energy Meter ICs

GENERAL DESCRIPTION

The 71M6543F/71M6543G are 4th-generation polyphase metering systems-on-chips (SoCs) with a 5MHz 8051-compatible MPU core, low-power real-time clock (RTC) with digital temperature compensation, flash memory, and LCD driver. Our Single Converter Technology® with a 22-bit delta-sigma ADC, seven analog inputs, digital metrology temperature compensation, precision voltage reference, and a 32-bit computation engine (CE) supports a wide range of metering applications with very few external components.

The 71M6543F/71M6543G support optional interfaces to the 71M6xx3 series of isolated sensors that offer BOM cost reduction, immunity to magnetic tamper, and enhanced reliability. The ICs feature ultra-low-power operation in active and battery modes, 5KB shared RAM, and 64KB (71M6543F) or 128KB (71M6543G) of flash memory, which can be programmed with code and/or data during meter operation.

A complete array of code development tools, demonstration code, and reference designs enable rapid development and certification of meters that meet all ANSI and IEC electricity metering standards worldwide.



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MICROWIRE is a registered trademark of National Semiconductor Corp.

FEATURES

- 0.1% Typical Accuracy Over 2000:1 Current Range
- Exceeds IEC 62053/ANSI C12.20 Standards
- Seven Sensor Inputs with Neutral Current Measurement, Differential Mode Selectable for Current Inputs
- Selectable Gain of 1 or 8 for One Current Input to Support Shunts
- High-Speed Wh/VARh Pulse Outputs with Programmable Width
- 64KB Flash, 5KB RAM (71M6543F)
- 128KB Flash, 5KB RAM (71M6543G)
- Up to Four Pulse Outputs with Pulse Count
- Four-Quadrant Metering, Phase Sequencing
- Digital Temperature Compensation:
  - Metrology Compensation
  - Accurate RTC for TOU Functions with Automatic Temperature Compensation for Crystal in All Power Modes
- Independent 32-Bit Compute Engine
- 46-64Hz Line Frequency Range with the Same Calibration
- Phase Compensation (±7°)
- Three Battery-Backup Modes:
  - Brownout Mode
  - LCD Mode
  - Sleep Mode
- Wake-Up on Pin Events and Wake-on-Timer
- 1μA in Sleep Mode
- Flash Security
- In-System Program Update
- 8-Bit MPU (80515), Up to 5MIPS
- Full-Speed MPU Clock in Brownout Mode
- LCD Driver:
  - 6 Common Segment Drivers
  - Up to 56 Selectable Pins
- Up to 51 Multifunction DIO Pins
- Hardware Watchdog Timer (WDT)
- I²C/MICROWIRE® EEPROM Interface
- SPI Interface with Flash Program Capability
- Two UARTs for IR and AMR
- IR LED Driver with Modulation
- Industrial Temperature Range
- 100-Pin Lead-Free LQFP Package

Table of Contents

Figures

Tables

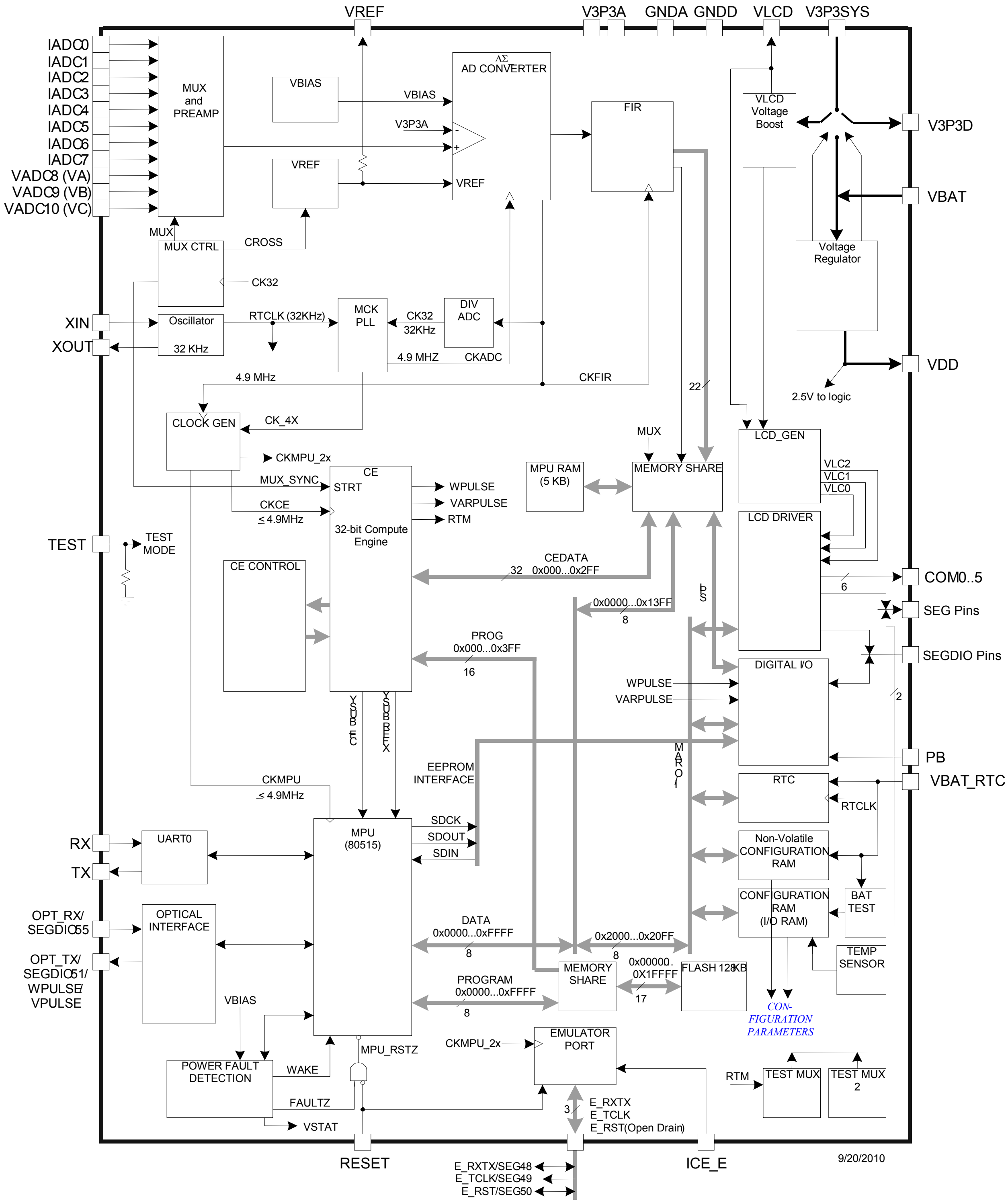


Figure 1: IC Functional Block Diagram

1 Introduction

This data sheet covers the 71M6543F (64KB) and 71M6543G (128KB) 4th-generation polyphase energy measurement system-on-chips (SoCs). The term "71M6543" is used when discussing a device feature or behavior that is applicable to all four part numbers. The specific part numbers are used when discussing those features that apply only to specific part numbers. This data sheet also covers details about the companion 71M6xx3 isolated current sensor device.

This document covers the use of the 71M6543 in conjunction with the 71M6xx3 isolated current sensor. The 71M6543 and 71M6xx3 ICs make it possible to use one non-isolated and three additional isolated shunt current sensors to create polyphase energy meters using inexpensive shunt resistors, while achieving unprecedented performance with this type of sensor technology. The 71M6543 SoCs also support Current Transformers (CT).

To facilitate document navigation, hyperlinks are often used to reference figures, tables and section headings that are located in other parts of the document. All hyperlinks in this document are highlighted in blue. Hyperlinks are used extensively to increase the level of detail and clarity provided within each section by referencing other relevant parts of the document. To further facilitate document navigation, this document is published as a PDF document with bookmarks enabled.

The reader is also encouraged to obtain and review the documents listed in 8 Related Information on page 152 of this document.

2 Hardware Description

2.1 Hardware Overview

The 71M6543 single-chip energy meter integrates all primary functional blocks required to implement a solid-state electricity meter. Included on the chip are:

- An analog front-end (AFE) featuring a 22-bit second-order sigma-delta ADC
- An independent 32-bit digital computation engine (CE) to implement DSP functions
- An 8051-compatible microprocessor (MPU) which executes one instruction per clock cycle (80515)
- A precision voltage reference (VREF)
- A temperature sensor for digital temperature compensation of:
  - Metrology (MPU)
  - Automatic RTC in all power states
  - MPU assisted RTC compensation
- LCD Driver
- RAM and Flash memory
- A real time clock (RTC)
- A variety of I/O pins
- A power failure interrupt
- A zero-crossing interrupt
- Selectable current sensor interfaces for locally-connected sensors as well as isolated sensors (i.e., using the 71M6xx3 companion IC with a shunt resistor sensor)
- Resistive Shunt and Current Transformers are supported

In order to implement a polyphase meter with or without neutral current sensing, one resistive shunt current sensor may be connected directly (non-isolated) to the 71M6543 device, while up to three additional current shunts are isolated using a companion 71M6xx3 isolated sensor IC. An inexpensive, small size pulse transformer is used to electrically isolate the 71M6xx3 remote sensor from the 71M6543. The 71M6543 performs digital communications bi-directionally with the 71M6xx3 and also provides power to the 71M6xx3 through the isolating pulse transformer. Isolated (remote) shunt current sensors are connected to the differential input of the 71M6xx3. The 71M6543 may also be used with Current Transformers; in this case the 71M6xx3 isolated sensors are not required. Included on the 71M6xx3 companion isolator chip are:

- Digital isolation communications interface
- An analog front-end (AFE) featuring a 22-bit second-order sigma-delta ADC
- A precision voltage reference (VREF)
- A temperature sensor (for current-sensing digital temperature compensation)
- A fully differential shunt resistor sensor input
- A pre-amplifier to optimize shunt current sensor performance
- Isolated power circuitry obtains dc power from pulses sent by the 71M6543

In a typical application, the 32-bit compute engine (CE) of the 71M6543 sequentially processes the samples from the voltage inputs on analog input pins and performs calculations to measure active energy (Wh) and reactive energy (VARh), as well as A^2h, and V^2h for four-quadrant metering. These measurements are then accessed by the MPU, processed further and output using the peripheral devices available to the MPU.

In addition to advanced measurement functions, the real time clock (RTC) function allows the 71M6543 to record time of use (TOU) metering information for multi-rate applications and to time-stamp tamper or other events. An automatic RTC temperature compensation circuit operates in all power states including when the MPU is halted, and continues to compensate using back-up battery power during power outages.

Measurements can be displayed on 3.3 V LCDs commonly used in low-temperature environments. The integrated charge pump and temperature sensor can be used by the MPU to enhance 3.3 V LCD performance at cold temperatures. The on-chip charge pump may also drive 5 V LCDs. Flexible mapping of LCD display segments facilitates the integration of existing custom LCDs. Design trade-off between the number of LCD segments and DIO pins can be implemented in software to accommodate various requirements.

In addition to the temperature-trimmed ultra-precision voltage reference, the on-chip digital temperature compensation mechanism includes a temperature sensor and associated controls for correction of unwanted temperature effects on metrology and RTC accuracy (i.e., to meet the requirements of ANSI and IEC standards). Temperature-dependent external components such as the crystal oscillator, current transformers (CTs), Current Shunts and their corresponding signal conditioning circuits can be characterized and their correction factors can be programmed to produce electricity meters with exceptional accuracy over the industrial temperature range.

One of the two internal UARTs is adapted to support an Infrared LED with internal drive and sense configuration and can also function as a standard UART. The optical output can be modulated at 38 kHz. This flexibility makes it possible to implement AMR meters with an IR interface. A block diagram of the IC is shown in Figure 1.

2.2 Analog Front-End (AFE)

The AFE functions as a data acquisition system, controlled by the MPU. The 71M6543 AFE may also be augmented by isolated 71M6xx3 sensors in order to support low-cost current shunt sensors. Figure 2, and Figure 3 show the two most common configurations; other configurations are possible. Sensors that are connected directly to the 71M6543 (i.e., IADC0-IADC1, VADC8, VADC9 and VADC10) are multiplexed into the single second-order sigma-delta ADC input for sampling in the 71M6543. The 71M6543 ADC output is decimated by the FIR filter and stored in CE RAM where it can be accessed and processed by the CE.

Shunt current sensors that are isolated by using a 71M6xx3 device, are sampled by a second-order sigma delta ADC in the 71M6xx3 and the signal samples are transferred over the digital isolation interface through the low-cost isolation pulse transformer.

Figure 2 shows the 71M6543 using shunt current sensors and the 71M6xx3 isolated sensor devices. Figure 2 supports neutral current measurement with a local shunt connected to the IADC0-IADC1 input plus three remote (isolated) shunt sensors. As seen in Figure 2, when a remote isolated shunt sensor is connected via the 71M6xx3, the samples associated with this current channel are not routed to the multiplexer, and are instead transferred digitally to the 71M6543 via the isolation interface and are directly stored in CE RAM. The *MUX_SELn[3:0]* I/O RAM control fields allow the MPU to configure the AFE for the desired multiplexer sampling sequence. Refer to Table 1 and Table 2 for the appropriate CE code and the corresponding AFE settings.

See Figure 31 for the meter wiring configuration corresponding to Figure 2.

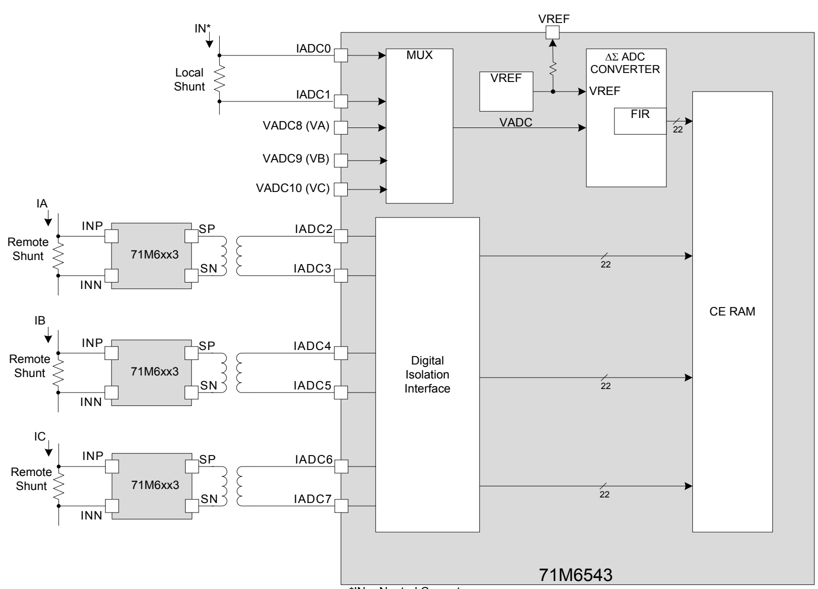


Figure 2: AFE Block Diagram (Shunts: One-Local, Three-Remotes)

The 71M6543 AFE can also be directly interfaced to Current Transformers (CTs), as seen in Figure 3. In this case, all voltage and current channels are multiplexed into a single second-order sigma-delta ADC in the 71M6543 and the 71M6xx3 remote isolated sensors are not used. The fourth CT and the measurement of Neutral current via the IADC0-IADC1 current channel are optional.

See Figure 32 for the meter wiring configuration corresponding to Figure 3.

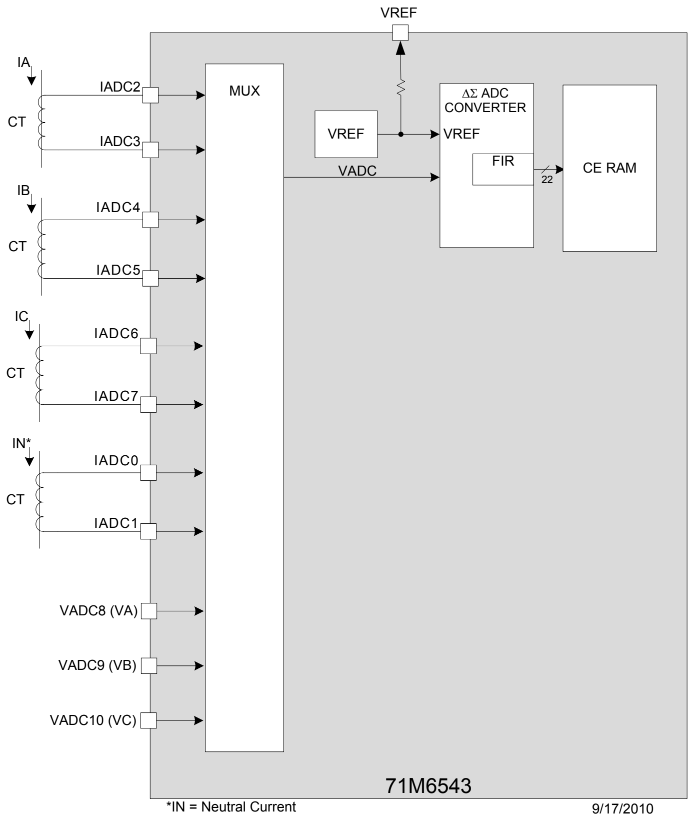


Figure 3. AFE Block Diagram (Four CTs)

2.2.1 Signal Input Pins

The 71M6543 features eleven ADC input pins.

IADC0 through IADC7 are intended for use as current sensor inputs. These eight current sensor inputs can be configured as four single-ended inputs, or can be paired to form four differential inputs. For best performance, it is recommended to configure the current sensor inputs as differential inputs (i.e., IADC0-IADC1, IADC2-IADC3, IADC4-IADC5 and IADC6-IADC7). The first differential input (IADC0-IADC1) features a pre-amplifier with a selectable gain of 1 or 8, and is intended for direct connection to a shunt resistor sensor, and can also be used with a Current Transformer (CT). The three remaining differential pairs (i.e., IADC2-IADC3, IADC4-IADC5 and IADC6-IADC7) may be used with CTs, or may be enabled to interface to a remote 71M6xx3 isolated current sensor providing isolation for a shunt resistor sensor using a low cost pulse transformer.

The remaining three inputs VADC8 (VA), VADC9 (VB) and VADC10 (VC) are single-ended, and are intended for sensing each of the phase voltages in a polyphase meter application. These three single-ended inputs are referenced to the V3P3A pin.

All ADC input pins measure voltage. In the case of shunt current sensors, currents are sensed as a voltage drop in the shunt resistor sensor. In the case of Current Transformers (CT), the current is measured as a voltage across a burden resistor that is connected to the secondary of the CT. Meanwhile, line voltages are sensed through resistive voltage dividers. The VADC8 (VA), VADC9 (VB) and VADC10 (VC) pins are single-ended and their common return is the V3P3A pin. See Figure 27, Figure 28, Figure 29 and Figure 30 for detailed connections for each type of sensor. Also refer to the 71M6543 Demonstration Board schematic and bill of materials for typical component values used in these and other circuits.

Pins IADC0-IADC1 can be programmed individually to be differential or single-ended as determined by the *DIFF0_E* (*I/O RAM 0x210C[4]*) control bit. However, for most applications, IADC0-IADC1 are configured as a differential input to work with a resistive shunt or CT directly interfaced to the IADC0-IADC1 differential input with the appropriate external signal conditioning components.

The performance of the IADC0-IADC1 pins can be enhanced by enabling a pre-amplifier with a fixed gain of 8, using the I/O RAM control bit *PRE_E (I/O RAM 0x2704[5])*. When *PRE_E* = 1, IADC0-IADC1 become the inputs to the 8x pre-amplifier, and the output of this amplifier is supplied to the multiplexer. The 8x amplification is useful when current sensors with low sensitivity, such as shunt resistors, are used. With *PRE_E* set, the IADC0-IADC1 input signal amplitude is restricted to 31.25 mV peak. When *PRE_E* = 0 (Gain = 1), the IADC0-IADC1 input signal is restricted to 250 mV peak.

For the 71M6543 application utilizing shunt resistor sensors (Figure 2), the IADC0-IADC1 pins are configured for differential mode to interface to a local shunt by setting the *DIFF0_E* control bit. Meanwhile, the IADC2-IADC3 , IADC4-IADC5 and IADC6-IADC7 pins are re-configured as digital remote sensor interface designed to communicate with a 71M6xx3 isolated sensor by setting the *RMTx_E* control bits (*I/O RAM 0x2709[5:3]*). The 71M6xx3 communicates with the 71M6543 using a bi-directional digital data stream through an isolating pulse transformer. The 71M6543 also supplies power to the 71M6xx3 through the isolating transformer. This type of interface is further described at the end of this chapter. See 2.2.8 71M6xx3 Isolated Sensor Interface.

For use with Current Transformers (CTs), as shown in Figure 3, the *RMTx_E* control bits are reset, so that IADC2-IADC3, IADC4-IADC5 and IADC6-IADC7 are configured as local analog inputs. The IADC0-IADC1 pins cannot be configured as a remote sensor interface.

2.2.2 Input Multiplexer

When operating with locally connected sensors, the input multiplexer sequentially applies the input signals from the analog input pins to the input of the ADC (see Figure 3), according to the sampling sequence determined by the eleven *MUXn_SEL[3:0]* control fields. One complete sampling sequence is called a multiplexer frame. The multiplexer of the 71M6543 can select up to eleven input signals when the current sensor inputs are configured for single-ended mode. When the current sensor inputs are configured in differential mode (recommended for best performance), the number of input signals is seven (i.e., IADC0-IADC1, IADC2-IADC3, IADC4-IADC5, IADC6-IADC7, VADC8, VADC9 and VADC10) per multiplexer frame. The number of slots in the multiplexer frame is controlled by the I/O RAM control field *MUX_DIV[3:0] (I/O RAM 0x2100[7:4])* (see Figure 4). The multiplexer always starts at state 0 and proceeds until the number of sensor channels determined by the *MUX_DIV[3:0]* field setting have been converted.

The 71M6543 requires a unique CE code that is written for the specific meter configuration. Moreover, each CE code requires specific AFE and MUX settings in order to function properly. Table 1 provides the CE code and settings corresponding to the 1-Local / 3-Remote sensor configuration shown in Figure 2. Table 2 provides the CE code and settings corresponding to the CT configuration shown in Figure 3.

Table 1. Required CE Code and Settings for 1-Local / 3-Remotes

I/O RAM Mnemonic	I/O RAM Location	I/O RAM Setting	Comments
FIR_LEN[1:0]	210C[2:1]	1	288 cycles
ADC_DIV	2200[5]	0	Fast
PLL_FAST	2200[4]	1	19.66 MHz
MUX_DIV[3:0]	2100[7:4]	6	See note 1
MUX0_SEL[3:0]	2105[3:0]	0	Slot 0 is IADC**0**-IADC1 (IN)
MUX1_SEL[3:0]	2105[7:4]	1	Unused (See note 2)
MUX2_SEL[3:0]	2104[3:0]	1	Unused (See note 2)
MUX3_SEL[3:0]	2104[7:4]	8	Slot 3 is VADC**8** (VA)
MUX4_SEL[3:0]	2103[3:0]	9	Slot 4 is VADC**9** (VB)
MUX5_SEL[3:0]	2103[7:4]	A	Slot 5 is VADC**10** (VC)
MUX6_SEL[3:0]	2102[3:0]	0	Slots not enabled
MUX7_SEL[3:0]	2102[7:4]	0	
MUX8_SEL[3:0]	2101[3:0]	0	
MUX9_SEL[3:0]	2101[7:4]	0	
MUX10_SEL[3:0]	2100[3:0]	0	
RMT2_E	2709[3]	1	Enable Remote IADC2-IADC3 (IA)
RMT4_E	2709[4]	1	Enable Remote IADC4-IADC5 (IB)
RMT6_E	2709[5]	1	Enable Remote IADC6-IADC7 (IC)
DIFF0_E	210C[4]	1	Differential IADC0-IADC1 (IN)
DIFF2_E	210C[5]	0	See note 3
DIFF4_E	210C[6]	0	See note 3
DIFF6_E	210C[7]	0	See note 3
PRE_E	2704[5]	1	IADC0-IADC1 Gain = 8
EQU[2:0]	2106[7:5]	5	IA*VA + IB*VB + IC*VC
CE Codes (See note 4)	ce43b016603 (use with 71M6603) ce43b016103 (use with 71M6103) ce43b016113 (use with 71M6113) ce43b016203 (use with 71M6203)		
Equation(s)	5		
Current Sensor Type	1 Local Shunt and 3 Remote Shunts		
Applicable Figures	Figure 2, Figure 4 and Figure 31		

Notes:

1. *MUX_DIV[3:0]* must be set to 0 while writing the other RAM locations in this table.
2. Each unused slot must be assigned to a valid (0 to A), but unused ADC handle.
3. This channel is remote (71M6xx3), hence *DIFFx_E* is irrelevant.
4. Must use the CE code that corresponds to the specific 71M6xx3 device used.

Maxim updates the CE code periodically. Contact your local Maxim representative to obtain the latest CE code and the associated settings.

Table 2. Required CE Code and Settings for CT Sensors

I/O RAM Mnemonic	I/O RAM Location	I/O RAM Setting (Hex)	Comments
FIR_LEN[1:0]	210C[2:1]	1	288 cycles
ADC_DIV	2200[5]	0	Fast
PLL_FAST	2200[4]	1	19.66 MHz
MUX_DIV[3:0]	2100[7:4]	7	See note 1
MUX0_SEL[3:0]	2105[3:0]	2	Slot 0 is IADC**2**-IADC3 (IA)
MUX1_SEL[3:0]	2105[7:4]	8	Slot 1 is VADC**8** (VA)
MUX2_SEL[3:0]	2104[3:0]	4	Slot 2 is IADC**4**-IADC5 (IB)
MUX3_SEL[3:0]	2104[7:4]	9	Slot 3 is VADC**9** (VB)
MUX4_SEL[3:0]	2103[3:0]	6	Slot 4 is IADC**6**-IADC7 (IC)
MUX5_SEL[3:0]	2103[7:4]	A	Slot 5 is VADC**10** (VC)
MUX6_SEL[3:0]	2102[3:0]	0	Slot 6 is IADC0-IADC1 (IN – See note 2)
MUX7_SEL[3:0]	2102[7:4]	0	Slots not enabled
MUX8_SEL[3:0]	2101[3:0]	0	
MUX9_SEL[3:0]	2101[7:4]	0	
MUX10_SEL[3:0]	2100[3:0]	0	
RMT2_E	2709[3]	0	Local Sensor IADC2-IADC3
RMT4_E	2709[4]	0	Local Sensor IADC4-IADC5
RMT6_E	2709[5]	0	Local Sensor IADC6-IADC7
DIFF0_E	210C[4]	1	Differential IADC0-IADC1
DIFF2_E	210C[5]	1	Differential IADC2-IADC3
DIFF4_E	210C[6]	1	Differential IADC4-IADC5
DIFF6_E	210C[7]	1	Differential IADC6-IADC7
PRE_E	2704[5]	0	IADC0-IADC1 Gain = 1
EQU[2:0]	2106[7:5]	5	IA*VA + IB*VB + IC*VC
CE Code	ce43a02		
Equation(s)	5		
Current Sensor Type	4 Current Transformers (CTs)		
Applicable Figures	Figure 3, Figure 4 and Figure 32		

Notes:

1. *MUX_DIV[3:0]* must be set to 0 while writing the other RAM locations in this table.
2. IN is the optional Neutral Current.

Maxim updates the CE code periodically. Contact your local Maxim representative to obtain the latest CE code and the associated settings.

Using settings for the I/O RAM Mnemonics listed in Table 1 and Table 2 that do not match those required by the corresponding CE code being used may result in undesirable side effects and must not be selected by the MPU. Consult your local Maxim representative to obtain the correct CE code and AFE / MUX settings corresponding to the application.

For a polyphase configuration with neutral current sensing using shunt resistor current sensors and the 71M6xx3 isolated sensors, as shown in Figure 2, the IADC0-IADC1 input must be configured as a differential input, to be connected to a local shunt (see Figure 30 for the shunt connection details). The local shunt connected to the IADC0-IADC1 input is used to sense the Neutral current. The voltage sensors (VADC8, VADC9 and VADC10) are also directly connected to the 71M6543 (see Figure 27 for the connection details) and are also routed though the multiplexer, as seen in Figure 2. Meanwhile, the IADC2-IADC3, IADC4-IADC5 and IADC6-IADC7 current inputs are configured as remote sensor digital interfaces and the corresponding samples are not routed through the multiplexer. For this configuration, the multiplexer sequence is as shown in Figure 4.

For a polyphase configuration with optional neutral current sensing using Current Transformer (CTs) sensors, as shown in Figure 3, all four current sensor inputs must be configured as a differential inputs, to be connected to their corresponding CTs (see Figure 29 for the differential CT connection details). The IADC0-IADC1 current sensor input is optionally used to sense the Neutral current for anti-tampering purposes. The voltage sensors (VADC8, VADC9 and VADC10) are directly connected to the 71M6543 (see Figure 27 for the voltage sensor connection details). No 71M6xx3 isolated sensors are used in this configuration and all sensors are routed though the multiplexer, as seen in Figure 3. For this configuration, the multiplexer sequence is as shown in Figure 5.

The multiplexer sequence shown in Figure 4 corresponds to the configuration shown in Figure 2. The frame duration is 13 CK32 cycles (where CK32 = 32,768 Hz), therefore, the resulting sample rate is 32,768 Hz / 13 = 2,520.6 Hz. Note that Figure 4 only shows the currents that pass through the 71M6543 multiplexer, and does not show the currents that are copied directly into CE RAM from the remote sensors (see Figure 2), which are sampled during the second half of the multiplexer frame. The two unused conversion slots shown are necessary to produce the desired 2,520.6 Hz sample rate.

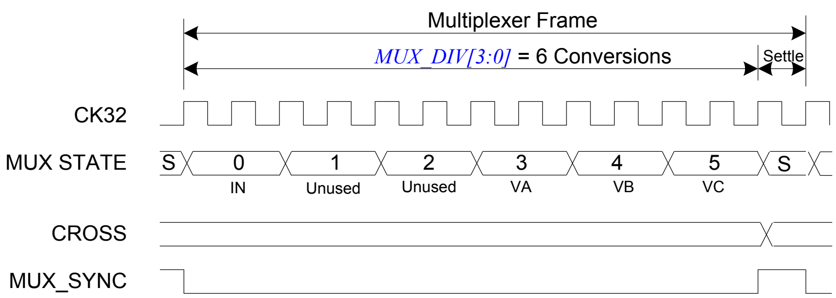


Figure 4: States in a Multiplexer Frame (*MUX_DIV[3:0]* = 6)

The multiplexer sequence shown in Figure 5 corresponds to the CT configuration shown in Figure 3. Since in this case all current sensors are locally connected to the 71M6543, all currents are routed through the multiplexer, as seen in Figure 3. For this multiplexer sequence, the frame duration is 15 CK32 cycles (where CK32 = 32,768 Hz), therefore, the resulting sample rate is 32,768 Hz / 15 = 2,184.5 Hz.

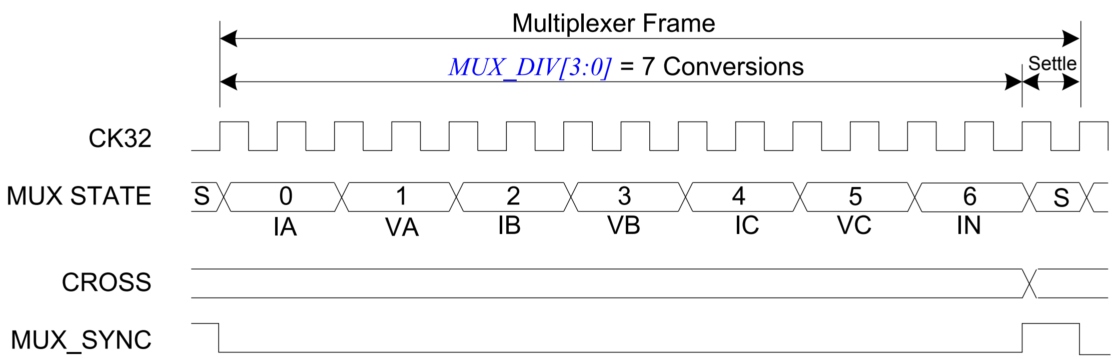


Figure 5: States in a Multiplexer Frame (*MUX_DIV[3:0]* = 7)

Multiplexer advance, FIR initiation and chopping of the ADC reference voltage (using the internal CROSS signal, see 2.2.7 Voltage References) are controlled by the internal MUX_CTRL circuit. Additionally, MUX_CTRL launches each pass of the CE through its code. MUX_CTRL is clocked by CK32, the 32768 Hz clock from the PLL block. The behavior of the MUX_CTRL circuit is governed by:

- *CHOP_E[1:0]* (*I/O RAM 0x2106[3:2]*)
- *MUX_DIV[3:0]* (*I/O RAM 0x2100[7:4]*)
- *FIR_LEN[1:0]* (*I/O RAM 0x210C[2:1]*)
- *ADC_DIV* (*I/O RAM 0x2200[5]*)

The duration of each multiplexer state depends on the number of ADC samples processed by the FIR as determined by the *FIR_LEN[1:0] (I/O RAM 0x210C[2:1]* control field. Each multiplexer state starts on the rising edge of CK32, the 32-kHz clock.

CAUTION: It is required that *MUX_DIV[3:0] (I/O RAM 0x2100[7:4])* be set to zero while changing the ADC configuration to minimize system transients. After all configuration bits are set, *MUX_DIV[3:0]* should be set to the required value.

The duration of each time slot in CK32 cycles depends on *FIR_LEN[1:0], ADC_DIV* and *PLL_FAST*:

Time_Slot_Duration = (3-2**PLL_FAST*)*(*FIR_LEN[1:0]*+1) * (*ADC_DIV*+1)

The duration of a multiplexer frame in CK32 cycles is:

MUX_Frame_Duration = 3-2**PLL_FAST* + Time_Slot_Duration * *MUX_DIV[3:0]*

The duration of a multiplexer frame in CK_FIR cycles is:

MUX frame duration (CK_FIR cycles) =

[3-2**PLL_FAST* + Time_Slot_Duration * *MUX_DIV*] * (48+*PLL_FAST**102)

The ADC conversion sequence is programmable through the *MUXn_SEL* control fields (*I/O RAM 0x2100* to *0x2105*). As stated above, there are up to eleven ADC time slots in the 71M6543, as set by *MUX_DIV[3:0]* (*I/O RAM 0x2100[7:4]*). In the expression *MUXn_SEL[3:0]* = x, 'n' refers to the multiplexer frame time slot number and 'x' refers to the desired ADC input number or ADC handle (i.e., IADC0 to VADC10, or simply 0 to 10 decimal). Thus, there are a total of 11 valid ADC handles in the 71M6543 devices. For example, if *MUX0_SEL[3:0]* = 0, then IADC0, corresponding to the sample from the IADC0-IADC1 input (configured as a differential input), is positioned in the multiplexer frame during time slot 0. See Table 1 and Table 2 for the appropriate *MUXn_SEL[3:0]* settings and other settings applicable to a particular meter configuration and CE code.

Note that when the remote sensor interface is enabled, the samples corresponding to the remote sensor currents do not pass through the 71M6543 multiplexer. The sampling of the remote current sensors occurs in the second half of the multiplexer frame. The VA, VB and VC voltages are assigned the last three slots in the frame. With this slot assignment for VA, VB and VC, the sampling of the corresponding remote sensor currents bears a precise timing relationship to their corresponding phase voltages, and delay compensation is accurately performed (see 2.2.3 Delay Compensation on page 19).

Also when using remote sensors, it is necessary to introduce unused slots to realize the number of slots specified by the *MUX_DIV[3:0]* (*I/O RAM 0x2100[7:4]*) field setting (see Figure 4 and Figure 5). The *MUXn_SEL[3:0]* control fields for these unused ("dummy") slots must be written with a valid ADC handle (i.e., 0 to 10 decimal) that is not otherwise being used. In this manner, the unused ADC handle, is used as a "dummy" place holder in the multiplexer frame, and the correct duration multiplexer frame sequence is generated and also the desired sample rate. The resulting sample data stored in the CE RAM location corresponding to the "dummy" ADC handle is ignored by the CE code. Meanwhile, the digital isolation interface takes care of automatically storing the samples for the remote current sensors in the appropriate CE RAM locations.

✓ Delay compensation and other functions in the CE code require the settings for *MUX_DIV[3:0], MUXn_SEL[3:0], RMT_E, FIR_LEN[1:0], ADC_DIV* and *PLL_FAST* to be fixed for a given CE code. Refer to Table 1 and Table 2 for the settings that are applicable to the 71M6543.

Table 3 summarizes the I/O RAM registers used for configuring the multiplexer, signals pins, and ADC. All listed registers are 0 after reset and wake from battery modes, and are readable and writable.

Table 3: Multiplexer and ADC Configuration Bits

Name	Location	Description
MUX0_SEL[3:0]	2105[3:0]	Selects the ADC input converted during time slot 0.
MUX1_SEL[3:0]	2105[7:4]	Selects the ADC input converted during time slot 1.
MUX2_SEL[3:0]	2104[3:0]	Selects the ADC input converted during time slot 2.
MUX3_SEL[3:0]	2104[7:4]	Selects the ADC input converted during time slot 3.
MUX4_SEL[3:0]	2103[3:0]	Selects the ADC input converted during time slot 4.
MUX5_SEL[3:0]	2103[7:4]	Selects the ADC input converted during time slot 5.
MUX6_SEL[3:0]	2102[3:0]	Selects the ADC input converted during time slot 6.
MUX7_SEL[3:0]	2102[7:0]	Selects the ADC input converted during time slot 7.
MUX8_SEL[3:0]	2101[3:0]	Selects the ADC input converted during time slot 8.
MUX9_SEL[3:0]	2101[7:0]	Selects the ADC input converted during time slot 9.
MUX10_SEL[3:0]	2100[3:0]	Selects the ADC input converted during time slot 10.
ADC_DIV	2200[5]	Controls the rate of the ADC and FIR clocks.
MUX_DIV[3:0]	2100[7:4]	The number of ADC time slots in each multiplexer frame (maximum = 11).
PLL_FAST	2200[4]	Controls the speed of the PLL and MCK.
FIR_LEN[1:0]	210C[2:1]	Determines the number of ADC cycles in the ADC decimation FIR filter.
DIFF0_E	210C[4]	Enables the differential configuration for analog input pins IADC0-IADC1 .
DIFF2_E	210C[5]	Enables the differential configuration for analog input pins IADC2-IADC3 .
DIFF4_E	210C[6]	Enables the differential configuration for analog input pins IADC4-IADC5 .
DIFF6_E	210C[7]	Enables the differential configuration for analog input pins IADC6-IADC7 .
RMT2_E	2709[3]	Enables the remote sensor interface transforming pins IADC2-IADC3 into a digital interface for communications with a 71M6xx3 sensor.
RMT4_E	2709[4]	Enables the remote sensor interface transforming pins IADC4-IADC5 into a digital interface for communications with a 71M6xx3 sensor.
RMT6_E	2709[5]	Enables the remote sensor interface transforming pins IADC6-IADC7 into a digital interface for communications with a 71M6xx3 sensor.
PRE_E	2704[5]	Enables the 8x pre-amplifier.
Refer to Table 70 starting on page 102 for more complete details about these I/O RAM locations.		

2.2.3 Delay Compensation

When measuring the energy of a phase (i.e., Wh and VARh) in a service, the voltage and current for that phase must be sampled at the same instant. Otherwise, the phase difference, Φ, introduces errors.

$$\phi = \frac{t_{delay}}{T} \cdot 360^o = t_{delay} \cdot f \cdot 360^o$$

Where f is the frequency of the input signal, T = 1/f and t_{delay} is the sampling delay between current and voltage.

Traditionally, sampling is accomplished by using two A/D converters per phase (one for voltage and the other one for current) controlled to sample simultaneously. Maxim's Single Converter Technology, however, exploits the 32-bit signal processing capability of its CE to implement "constant delay" all-pass filters. The all-pass filter corrects for the conversion time difference between the voltage and the corresponding current samples that are obtained with a single multiplexed A/D converter.

The "constant delay" all-pass filter provides a broad-band delay 360^o - θ, which is precisely matched to the difference in sample time between the voltage and the current of a given phase. This digital filter does not affect the amplitude of the signal, but provides a precisely controlled phase response.

The recommended ADC multiplexer sequence samples the current first, immediately followed by sampling of the corresponding phase voltage, thus the voltage is delayed by a phase angle Φ relative to the current. The delay compensation implemented in the CE aligns the voltage samples with their corresponding current samples by first delaying the current samples by one full sample interval (i.e., 360^o), then routing the voltage samples through the all-pass filter, thus delaying the voltage samples by 360^o - θ*,* resulting in the residual phase error between the current and its corresponding voltage of θ – Φ. The residual phase error is negligible, and is typically less than ±1.5 milli-degrees at 100Hz, thus it does not contribute to errors in the energy measurements.

When using remote sensors, the CE performs the same delay compensation described above to align each voltage sample with its corresponding current sample. Even though the remote current samples do not pass through the 71M6543 multiplexer, their timing relationship to their corresponding voltages is fixed and precisely known, provided that the *MUXn_SEL[3:0]* slot assignment fields are programmed as shown in Table 1. Note that these slot assignments result in VA, VB and VC occupying multiplexer slots 3, 4 and 5, respectively (see Figure 4).

2.2.4 ADC Pre-Amplifier

The ADC pre-amplifier is a low-noise differential amplifier with a fixed gain of 8 available only on the IADC0-IADC1 sensor input pins. A gain of 8 is enabled by setting *PRE_E* = 1 (*I/O RAM 0x2704[5]*). When disabled, the supply current of the pre-amplifier is <10 nA and the gain is unity. With proper settings of the *PRE_E* and *DIFF0_E* (*I/O RAM 0x210C[4]*) bits, the pre-amplifier can be used whether differential mode is selected or not. For best performance, the differential mode is recommended. In order to save power, the bias current of the pre-amplifier and ADC is adjusted according to the *ADC_DIV* control bit (*I/O RAM 0x2200[5]*).

2.2.5 A/D Converter (ADC)

A single 2^{nd} order sigma-delta A/D converter digitizes the voltage and current inputs to the device. The resolution of the ADC, including the sign bit, is 21 bits (*FIR_LEN[1:0]* = 01, *I/O RAM 0x210C[2:1]*), or 22 bits (*FIR_LEN[1:0]* = 10). The ADC is clocked by CKADC.

Initiation of each ADC conversion is controlled by the internal MUX_CTRL circuit as described earlier. At the end of each ADC conversion, the FIR filter output data is stored into the CE RAM location determined by the multiplexer selection.

2.2.6 FIR Filter

The finite impulse response filter is an integral part of the ADC and it is optimized for use with the multiplexer. The purpose of the FIR filter is to decimate the ADC output to the desired resolution. At the end of each ADC conversion, the output data is stored into the fixed CE RAM location determined by the multiplexer selection stored in the *MUXn_SEL[3:0]* fields. FIR data is stored after being shifted left by 9 bits.

2.2.7 Voltage References

A bandgap circuit provides the reference voltage to the ADC. The amplifier within the reference is chopper stabilized, i.e., the chopper circuit can be enabled or disabled by the MPU using the I/O RAM control field *CHOP_E[1:0] (I/O RAM 0x2106[3:2])*. The two bits in the *CHOP_E[1:0]* field enable the MPU to operate the chopper circuit in regular or inverted operation, or in toggling modes (recommended). When the chopper circuit is toggled in between multiplexer cycles, dc offsets on VREF are automatically be averaged out, therefore the chopper circuit should always be configured for one of the toggling modes.

Since the VREF band-gap amplifier is chopper-stabilized, the dc offset voltage, which is the most significant long-term drift mechanism in the voltage references (VREF), is automatically removed by the chopper circuit. Both the 71M6543 and the 71M6xx3 feature chopper circuits for their respective VREF voltage reference.

The general topology of a chopped amplifier is shown in Figure 6. The CROSS signal is an internal on-chip signal and is not accessible on any pin or register.

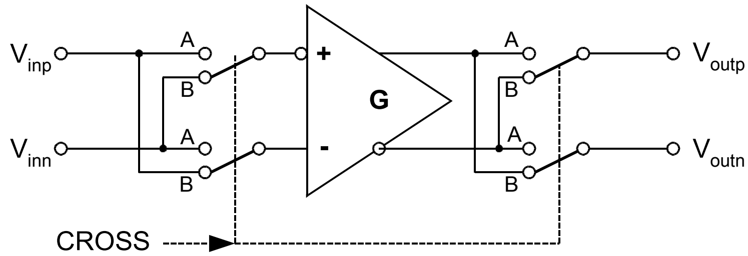


Figure 6: General Topology of a Chopped Amplifier

It is assumed that an offset voltage Voff appears at the positive amplifier input. With all switches, as controlled by CROSS (an internal signal), in the A position, the output voltage is:

Voutp – Voutn = G (Vinp + Voff – Vinn) = G (Vinp – Vinn) + G Voff

With all switches set to the B position by applying the inverted CROSS signal, the output voltage is:

Voutn – Voutp = G (Vinn – Vinp + Voff) = G (Vinn – Vinp) + G Voff, or

Voutp – Voutn = G (Vinp – Vinn) - G Voff

Thus, when CROSS is toggled, e.g., after each multiplexer cycle, the offset alternately appears on the output as positive and negative, which results in the offset effectively being eliminated, regardless of its polarity or magnitude.

When CROSS is high, the connection of the amplifier input devices is reversed. This preserves the overall polarity of that amplifier gain; it inverts its input offset. By alternately reversing the connection, the amplifier's offset is averaged to zero. This removes the most significant long-term drift mechanism in the voltage reference. The *CHOP_E[1:0]* (*I/O RAM 0x2106[3:2]*) control field controls the behavior of CROSS. On the first CK32 rising edge after the last multiplexer state of its sequence, the multiplexer waits one additional CK32 cycle before beginning a new frame. At the beginning of this cycle, the value of CROSS is updated according to the *CHOP_E[1:0]* field. The extra CK32 cycle allows time for the chopped VREF to settle. During this cycle, MUXSYNC is held high. The leading edge of MUXSYNC initiates a pass through the CE program sequence.

CHOP_E[1:0] has four states: positive, reverse, and two toggle states. In the positive state, *CHOP_E[1:0]* = 01, CROSS is held low. In the reverse state, *CHOP_E[1:0]* = 10, CROSS is held high. The two automatic toggling states are selected by setting CHOP_E=11 or CHOP_E=00.

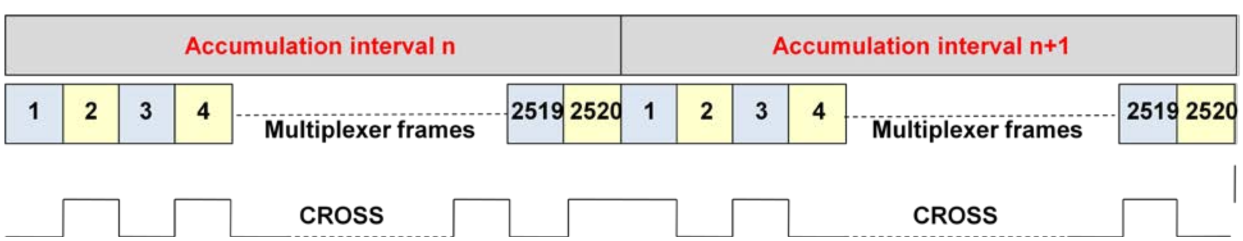


Figure 7: CROSS Signal with *CHOP_E* = 00

Figure 7 shows CROSS over two accumulation intervals when *CHOP_E[1:0]* = 00: At the end of the first interval, CROSS is high, at the end of the second interval, CROSS is low. Operation with *CHOP_E[1:0]* = 00 does not require control of the chopping mechanism by the MPU.

In the second toggle state, *CHOP_E[1:0]* = 11, CROSS does not toggle at the end of the last multiplexer cycle in an accumulation interval.

2.2.8 71M6xx3 Isolated Sensor Interface

2.2.8.1 General Description

Non-isolating sensors, such as shunt resistors, can be connected to the inputs of the 71M6543 via a combination of a pulse transformer and a 71M6xx3 IC (a top-level block diagram of this sensor interface is shown in Figure 31). The 71M6xx3 receives power directly from the 71M6543 via a pulse transformer and does not require a dedicated power supply circuit. The 71M6xx3 establishes 2-way communication with the 71M6543, supplying current samples and auxiliary information such as sensor temperature via a serial data stream.

Up to three 71M6xx3 Isolated Sensors can be supported by the 71M6543. When a remote sensor interface is enabled, the two analog current inputs become re-configured as a digital remote sensor interface. For example, when control bit *RMT2_E* = 1, the IADC2-IADC3 analog pins are re-configured as the digital interface pins to the remote sensor.

Each 71M6xx3 Isolated Sensor consists of the following building blocks:

- Power supply that derives power from pulses received from the 71M6543
- Bi-directional digital communications interface
- Shunt signal pre-amplifier
- 22-bit 2nd Order Sigma-Delta ADC Converter with precision bandgap reference (chopping amplifier)
- Temperature sensor (for digitally compensating VREF)
- Fuse system containing part-specific information

During an ordinary multiplexer cycle, the 71M6543 internally determines which other channels are enabled with *MUX_DIV[3:0] (I/O RAM 0x2100[7:4])*. At the same time, it decimates the modulator output from the 71M6xx3 Isolated Sensors. Each result is written to CE RAM during one of its CE access time slots.

2.2.8.2 Communication between 71M6543 and 71M6xx3 Isolated Sensor

The ADC of the 71M6xx3 derives its timing from the power pulses generated by the 71M6543 and as a result, operates its ADC slaved to the frequency of the power pulses. The generation of power pulses, as well as the communication protocol between the 71M6543 and 71M6xx3 Isolated Sensor, is automatic and transparent to the user. Details are not covered in this data sheet.

2.2.8.3 Control of the 71M6xx3 Isolated Sensor

The 71M6543 can read or write certain types of information from each 71M6xx3 remote sensor.

The data to be read is selected by a combination of the *RCMD[4:0]* and *TMUXRn[2:0]*. To perform a read transaction from one of the 71M6xx3 devices, the MPU first writes the *TMUXRn[2:0]* field (where n = 2, 4, 6, located at *I/O RAM 0x270A[2:0], 0x270A[6:4] and 0x2709[2:0],* respectively). Next, the MPU writes *RCMD[4:0]* (*SFR 0xFC[4:0]*) with the desired command and phase selection. When the *RCMD[4:2]* bits have cleared to zero, the transaction has been completed and the requested data is available in *RMT_RD[15:0]* (*I/O RAM 0x2602[7:0]* is the MSB and *0x2603[7:0]* is the LSB). The read parity error bit, *PERR_RD (SFR 0xFC[6])* is also updated during the transaction. If the MPU writes to *RCMD[4:0]* before a previously initiated read transaction is completed, the command is ignored. Therefore, the MPU must wait for *RCMD[4:2]*=0 before proceeding to issue the next remote sensor read command.

If the CE is running (*CE_E*=1), the MPU must write *RCMD[4:0]* immediately after a CE_BUSY rising edge. *RCMD[4:0]* must be written before the next rising edge of MUX_SYNC. Failure to do this can cause incorrect data to be read.

The *RCMD[4:0]* field is divided into two sub-fields, *COMMAND=RCMD[4:2]* and *PHASE=RCMD[1:0]*, as shown in Table 4.

.

Table 4. *RCMD[4:0]* Bits

Command *RCMD[4:2]*		Phase Selector *RCMD[1:0]*		Associated *TMUXRn* Control Field
000	Invalid	00	Invalid	---
001	Command 1	01	IADC**2**-IADC3	*TMUXR**2**[2:0]*
010	Command 2	10	IADC**4**-IADC5	*TMUXR**4**[2:0]*
011	Reserved	11	IADC**6**-IADC7	*TMUXR**6**[2:0]*
100	Reserved			
101	Invalid			
110	Reserved			
111	Reserved			

Notes:

1. Only two codes of *RCMD[4:2]* (*SFR 0xFC[4:2]*) are relevant for normal operation. These are *RCMD[4:2]* = 001 and 010. Codes 000 and 101 are invalid and will be ignored if used. The remaining codes are reserved and must not be used.
2. For the *RCMD[1:0]* control field, codes 01, 10 and 11 are valid and 00 is invalid and must not be used.
3. The specific phase (A, B or C) associated with each *TMUXRn[2:0]* field, is determined by how the IADCn input pins are connected in the meter design.

Table 5 shows the allowable combinations of values in *RCMD[4:2]* and *TMUXRn[2:0]*, and the corresponding data type and format sent back by the 71M6xx3 remote sensor and how the data is stored in *RMT_RD[15:8]* and *RMT_RD[7:0]*. The MPU selects which of the three phases is read by asserting the proper code in the *RCMD[1:0]* field, as shown in Table 4.

.

Table 5: Remote Interface Read Commands

RCMD[4:2]	*TMUXRn[2:0]*	Read Operation	***RMT_RD*** **[15:8]**	***RMT_RD*** **[7:0]**
001	00X	*TRIMT[7:0]* (trim fuse for all 71M6xx3)	*TRIMT[7]=RMT_RD[8]*	*TRIMT[6:0]=RMT_RD[7:1]*
001	11X	*TRIMBGB[7:0]* and *TRIMBGD[7:0]* (additional trim fuses for 71M6113 and 71M6203 only)	*TRIMBGB[7:0]*	*TRIMBGD[7:0]*
010	00X	*STEMP[10:0]* (sensed 71M6xx3 temperature)	*STEMP[10:8]=RMT_RD[10:8]* (*RMT_RD[15:11]* are sign extended)	*STEMP[7:0]*
010	01X	*VSENSE[7:0]* (sensed 71M6xx3 supply voltage)	*All zeros*	*VSENSE[7:0]*
010	10X	*VERSION[7:0]* (chip version)	*VERSION[7:0]*	*All zeros*

Notes:

1. *TRIMT[7:0]* is the VREF trim value for all 71M6xx3 devices. Note that the *TRIMT[7:0]* 8-bit value is formed by *RMT_RD[8]* and *RMT_RD[7:1]*. See the 71M6xxx Data Sheet for the equations related to *TRIMT[7:0]* and the corresponding temperature coefficient.
2. *TRIMBGB[7:0]* and *TRIMBGD[7:0]* are trim values used for characterizing the 71M6113 (0.5%) and 71M6203 (0.1%) over temperature. See the 71M6xxx Data sheet for the equations related to *TRIMBGB[7:0]* and *TRIMBGD[7:0]* and the corresponding temperature coefficients.
3. See 2.5.6 71M6xx3 Temperature Sensor on page 56.
4. See 2.5.8 71M6xx3 VCC Monitor on page 56.

With hardware and trim-related information on each connected 71M6xx3 Isolated Sensor available to the 71M6543, the MPU can implement temperature compensation of the energy measurement based on the individual temperature characteristics of the 71M6xx3 Isolated Sensors. See 4.5 Metrology Temperature Compensation for details.

Table 6 shows all I/O RAM registers used for control of the external 71M6xx3 Isolated Sensors. See the 71M6xx3 Data Sheet for additional details.

Table 6: I/O RAM Control Bits for Isolated Sensor

Name	Address	RST Default	WAKE Default	R/W	Description
RCMD[4:0]	SFR FC[4:0]	0	0	R/W	When the MPU writes a non-zero value to *RCMD*, the 71M6543 issues a command to the corresponding isolated sensor selected with *RCMD[1:0]*. When the command is complete, the 71M6543 clears *RCMD[4:2]*. The command code itself is in *RCMD[4:2]*.
PERR_RD *PERR_WR*	SFR FC[6] SFR FC[5]	0	0	R/W	The 71M6543 sets these bits to indicate that a parity error on the isolated sensor has been detected. Once set, the bits are remembered until they are cleared by the MPU.
CHOPR[1:0]	2709[7:6]	00	00	R/W	The CHOP settings for the isolated sensors. 00 – Auto chop. Change every multiplexer frame. 01 – Positive 10 – Negative 11 – Same as 00
TMUXR2[2:0]	270A[2:0]	000	000	R/W	The TMUX bits for control of the isolated sensor.
TMUXR4[2:0]	270A[6:4]	000	000	R/W	The TMUX bits for control of the isolated sensor.
TMUXR6[2:0]	2709[2:0]	000	000	R/W	The TMUX bits for control of the isolated sensor.
RMT_RD[15:8] *RMT_RD[7:0]*	2602[7:0] 2603[7:0]	0	0	R	The read buffer for 71M6xx3 read operations.
RFLY_DIS	210C[3]	0	0	R/W	Controls how the 71M6543 drives the 71M6xx3 power pulse. When set, the power pulse is driven high and low. When cleared, it is driven high followed by an open circuit fly-back interval.
RMT2_E	2709[3]	0	0	R/W	Enables the isolated remote sensor interface and re-configures pins IADC2-IADC3 as a balanced pair digital remote interface.
RMT4_E	2709[4]	0	0	R/W	Enables the isolated remote sensor interface and re-configures pins IADC4-IADC5 as a balanced pair digital remote interface.
RMT6_E	2709[5]	0	0	R/W	Enables the isolated remote sensor interface and re-configures pins IADC6-IADC7 as a balanced pair digital remote interface.
Refer to Table 70 starting on page 102 for more complete details about these I/O RAM locations.					

2.3 Digital Computation Engine (CE)

The CE, a dedicated 32-bit signal processor, performs the precision computations necessary to accurately measure energy. The CE calculations and processes include:

- Multiplication of each current sample with its associated voltage sample to obtain the energy per sample (when multiplied by the constant sample time).
- Frequency-insensitive delay cancellation on all channels (to compensate for the delay between samples caused by the multiplexing scheme).
- 90° phase shifter (for VAR calculations).
- Pulse generation.
- Monitoring of the input signal frequency (for frequency and phase information).
- Monitoring of the input signal amplitude (for sag detection).
- Scaling of the processed samples based on calibration coefficients.
- Scaling of samples based on temperature compensation information.

2.3.1 CE Program Memory

The CE program resides in flash memory. Common access to flash memory by the CE and MPU is controlled by a memory share circuit. Each CE instruction word is two bytes long. Allocated flash space for the CE program cannot exceed 4096 16-bit words (8 KB). The CE program counter begins a pass through the CE code each time multiplexer state 0 begins. The code pass ends when a HALT instruction is executed. For proper operation, the code pass must be completed before the multiplexer cycle ends.

The CE program must begin on a 1 KB boundary of the flash address. The I/O RAM control field *CE_LCTN[6/5:0]* (*I/O RAM 0x2109[6/5:0]*) on the 71M6543F and *CE_LCTN[6:0]* (*I/O RAM 0x2109[6:0]*) on the 71M6543G defines which 1 KB boundary contains the CE code. Thus, the first CE instruction is located at 1024**CE_LCTN[5:0]* on the 71M6543F and 1024**CE_LCTN[6:0]* on the 71M6543G.

2.3.2 CE Data Memory

The CE and MPU share data memory (RAM). Common access to XRAM by the CE and MPU is controlled by a memory share circuit. The CE can access up to 3 KB of the 5 KB data RAM (XRAM), i.e. from RAM address 0x0000 to 0x0C00.

The XRAM can be accessed by the FIR filter block, the RTM circuit, the CE, and the MPU. Assigned time slots are reserved for FIR and MPU, respectively, to prevent bus contention for XRAM data access by the CE.

The MPU reads and writes the XRAM shared between the CE and MPU as the primary means of data communication between the two processors.

The CE is aided by support hardware to facilitate implementation of equations, pulse counters, and accumulators. This hardware is controlled through I/O RAM field *EQU[2:0]* (equation assist, *I/O RAM 0x2106[7:5]*), bit *DIO_PV (I/O RAM 0x2457[6]),* bit *DIO_PW* (pulse count assist, *I/O RAM 0x2457[7]*), and *SUM_SAMPS[12:0]* (accumulation assist, *I/O RAM 0x2107[4:0]* and *0x2108[7:0]*).

The integration time for each energy output, when using standard CE code, is *SUM_SAMPS[12:0]* /2184.53 (with *MUX_DIV[3:0]* = 7, *I/O RAM 0x2100[7:4]*). CE hardware issues the XFER_BUSY interrupt when the accumulation is complete.

2.3.3 CE Communication with the MPU

The CE outputs six signals to the MPU: CE_BUSY, XFER_BUSY, XPULSE, YPULSE, WPULSE and VPULSE. These are connected to the MPU interrupt service. CE_BUSY indicates that the CE is actively processing data. This signal occurs once every multiplexer frame. XFER_BUSY indicates that the CE is updating to the output region of the CE RAM, which occurs whenever an accumulation cycle has been completed. Both, CE_BUSY and XFER_BUSY are cleared when the CE executes a HALT instruction.

XPULSE and YPULSE can be configured to interrupt the MPU and indicate zero crossings of the mains voltage, sag failures, or other significant events. Additionally, these signals can be connected directly to DIO pins to provide direct outputs from the CE. Interrupts associated with these signals always occur on the leading edge.

2.3.4 Meter Equations

The 71M6543 provides hardware assistance to the CE in order to support various meter equations. This assistance is controlled through I/O RAM field *EQU[2:0]* (equation assist, *I/O RAM 0x2106[7:5]*). The Compute Engine (CE) firmware configurations can implement the equations listed in Table 7. *EQU[2:0]* specifies the equation to be used based on the meter configuration and on the number of phases used for metering.

Table 7: Inputs Selected in Multiplexer Cycles

*EQU[2:0]**	Description	Wh and VARh formula			Recommended Multiplexer Sequence
		Element 0	Element 1	Element 2	
2	2-element, 3-W, 3ϕ Delta	VA · IA	VB · IB	N/A	IA VA IB VB
3	2-element, 4-W, 3ϕ Delta	VA(IA-IB)/2	VC ·IC	N/A	IA VA IB VB IC VC
4	2-element, 4-W, 3ϕ Wye	VA(IA-IB)/2	VB(IC-IB)/2	N/A	IA VA IB VB IC VC
5	3-element, 4-W, 3ϕ Wye	VA · IA	VB · IB	VC · IC	IA VA IB VB IC VC (ID)

Note:
* Only *EQU[2:0]* = 5 is supported by the currently available CE code versions for the 71M6543. Contact your local Maxim representative for CE codes that support equations 2, 3, and 4.

2.3.5 Real-Time Monitor (RTM)

The CE contains a Real-Time Monitor (RTM), which can be programmed to monitor four selectable XRAM locations at full sample rate. The data from the four monitored locations are serially output to the TMUXOUT pin via the digital output multiplexer at the beginning of each CE code pass. The RTM can be enabled and disabled with *RTM_E (I/O RAM 0x2106[1])*. The RTM output clock is available on the TMUX2OUT pin. Each RTM word is clocked out in 35 cycles and contains a leading flag bit. See Figure 8 for the RTM output format. RTM is low when not in use.

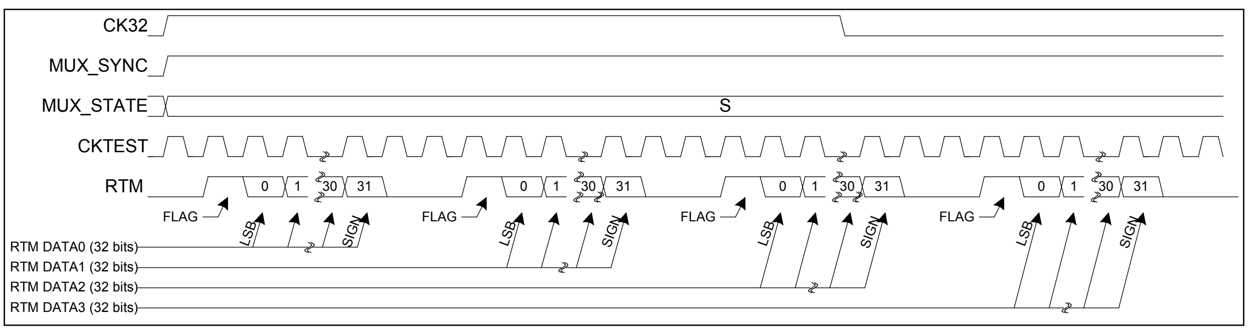


Figure 8: RTM Timing

2.3.6 Pulse Generators

The 71M6543 provides four pulse generators, VPULSE, WPULSE, XPULSE and YPULSE. The XPULSE and YPULSE generators are used by standard CE code to output CE status indicators, for example the status of the sag detection, to DIO pins. All pulses can be configured to generate interrupts to the MPU.

The polarity of the pulses may be inverted with *PLS_INV (I/O RAM 0x210C[0])*. When this bit is set, the pulses are active high, rather than the more usual active low. *PLS_INV* inverts all the pulse outputs.

The function of each pulse generator is determined by the CE code and the MPU code must configure the corresponding pulse outputs in agreement with the CE code. For example, standard CE code produces a mains zero-crossing pulse on XPULSE and a SAG pulse on YPULSE.

A common use of the zero-crossing pulses is to generate interrupts in order to drive real-time clock software in places where the mains frequency is sufficiently accurate to do so and also to adjust for crystal aging. A common use for the SAG pulse is to generate an interrupt that alerts the MPU when mains power is about to fail, so that the MPU code can store accumulated energy and other data to EEPROM before the V3P3SYS supply voltage actually drops.

2.3.6.1 XPULSE and YPULSE

Pulses generated by the CE may be exported to the XPULSE and YPULSE pulse output pins. Pins SEGDIO6 and SEGDIO7 are used for these pulses, respectively. Generally, the XPULSE and YPULSE outputs can be updated once on each pass of the CE code.

See 5.3 CE Interface Description on page 116 for details.

2.3.6.2 VPULSE and WPULSE

Referring to Figure 9, during each CE code pass the hardware stores exported WPULSE and VPULSE sign bits in an 8-bit FIFO and outputs them at a specified interval. This permits the CE code to calculate the VPULSE and WPULSE outputs at the beginning of its code pass and to rely on hardware to spread them over the multiplexer frame. As seen in Figure 9, the FIFO is reset at the beginning of each multiplexer frame. As also seen in Figure 9, the I/O RAM register *PLS_INTERVAL[7:0] (I/O RAM 0x210B[7:0])* controls the delay to the first pulse update and the interval between subsequent updates. The LSB of the *PLS_INTERVAL[7:0]* register is equivalent to 4 CK_FIR cycles (CK_FIR is typically 4.9152MHz if *PLL_FAST*=1 and *ADC_DIV*=0, but other CK_FIR frequencies are possible; see the ADC_DIV definition in Table 70.) If *PLS_INTERVAL[7:0]*=0, the FIFO is deactivated and the pulse outputs are updated immediately.

The MUX frame duration in units of CK_FIR clock cycles is given by:

If *PLL_FAST*=1:

MUX frame duration in CK_FIR cycles = [1 + (*FIR_LEN*+1) * (*ADC_DIV*+1) * (*MUX_DIV*)] * [150 / (*ADC_DIV*+1)]

If *PLL_FAST*=0:

MUX frame duration in CK_FIR cycles = [3 + 3*(*FIR_LEN*+1) * (*ADC_DIV*+1) * (*MUX_DIV*)] * [48 / (*ADC_DIV*+1)]

PLS_INTERVAL[7:0] in units of CK_FIR clock cycles is calculated by:

PLS_INTERVAL[7:0] = floor (Mux frame duration in CK_FIR cycles / CE pulse updates per Mux frame / 4)

Since the FIFO resets at the beginning of each multiplexer frame, the user must specify *PLS_INTERVAL[7:0]* so that all of the possible pulse updates occurring in one CE execution are output before the multiplexer frame completes. For instance, the 71M6543 CE code outputs six updates per multiplexer interval, and if the multiplexer interval is 1950 CK_FIR clock cycles long, the ideal value for the interval is 1950/6/4 = 81.25. However, if *PLS_INTERVAL[7:0]* = 82, the sixth output occurs too late and would be lost. In this case, the proper value for *PLS_INTERVAL[7:0]* is 81 (i.e., round down the result).

Since one LSB of *PLS_INTERVAL[7:0]* is equal to 4 CK_FIR clock cycles, the pulse time interval T_I in units of CK_FIR clock cycles is:

$$T_I = 4 \cdot PLS\_INTERVAL[7:0]$$

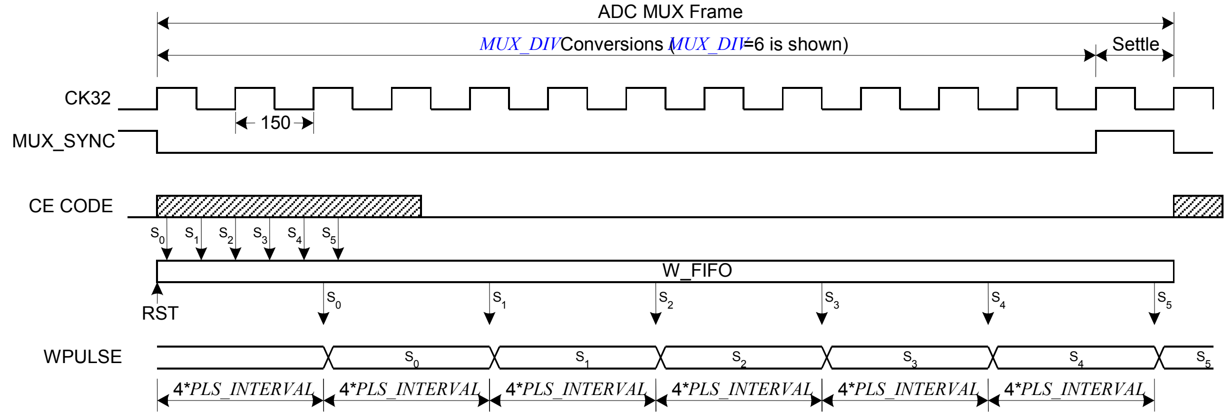
If the FIFO is enabled (i.e., *PLS_INTERVAL[7:0]* ≠ 0), hardware also provides a maximum pulse width feature in control register *PLS_MAXWIDTH[7:0] (I/O RAM 0x210A)* . By default, WPULSE and VPULSE are negative pulses (i.e., low level pulses, designed to sink current through an LED). *PLS_MAXWIDTH[7:0]* determines the maximum negative pulse width T_{MAX} in units of CK_FIR clock cycles based on the pulse interval T_I according to the formula:

$$T_{MAX} = (2 \cdot PLS\_MAXWIDTH[7:0] + 1) \cdot T_I$$

If *PLS_MAXWIDTH* = 255 or *PLS_INTERVAL*=0, no pulse width checking is performed, and the pulses default to 50% duty cycle.

The polarity of the pulses may be inverted with the control bit *PLS_INV* (*I/O RAM 0x210C[0]*). When *PLS_INV* is set, the pulses are active high. The default value for *PLS_INV* is zero, which selects active low pulses.

The WPULSE and VPULSE pulse generator outputs are available on pins SEGDIO0/WPULSE and SEGDIO1/VPULSE, respectively (pins 45 and 44). The pulses can also be output on OPT_TX pin 53 (see *OPT_TXE[1:0]*, *I/O RAM 0x2456[3:2]* for details).



1. This example shows how the FIFO distributes 6 pulse generator updates over one MUX frame.
2. If WPULSE is low longer than *(2*PLS_MAXWIDTH+1)* updates, WPULSE will be raised until the next low-going pulse begins.
3. Only the WPULSE circuit is shown. The VARPULSE circuit behaves identically.
4. All dimensions are in CK_FIR cycles (4.92MHz).
5. If *PLS_INTERVAL* =0, FIFO does not perform delay.

Figure 9. Pulse Generator FIFO Timing

2.3.7 CE Functional Overview

The ADC processes one sample per channel per multiplexer cycle. Figure 10 shows the timing of the samples taken during one multiplexer cycle with *MUX_DIV[3:0]* = 7 *(I/O RAM 0x2100[7:4])*.

The number of samples processed during one accumulation cycle is controlled by the I/O RAM register *SUM_SAMPS[12:0]* (*0x2107[4:0]* and *0x2108[7:0]*). The integration time for each energy output is:

SUM_SAMPS[12:0] / 2184.53, where 2184.53 is the sample rate in Hz

For example, *SUM_SAMPS[12:0]* = 2184 establishes 2184 multiplexer cycles per accumulation cycle or 2184/2184.53 = 0.9998 seconds. After an accumulation cycle is completed, the XFER_BUSY interrupt signals to the MPU that accumulated data are available. The slight difference between the nominal length of the accumulation interval (1000 ms) and the actual length of 999.8 ms (0.025%) is accounted for in the CE code and is of no practical consequence.

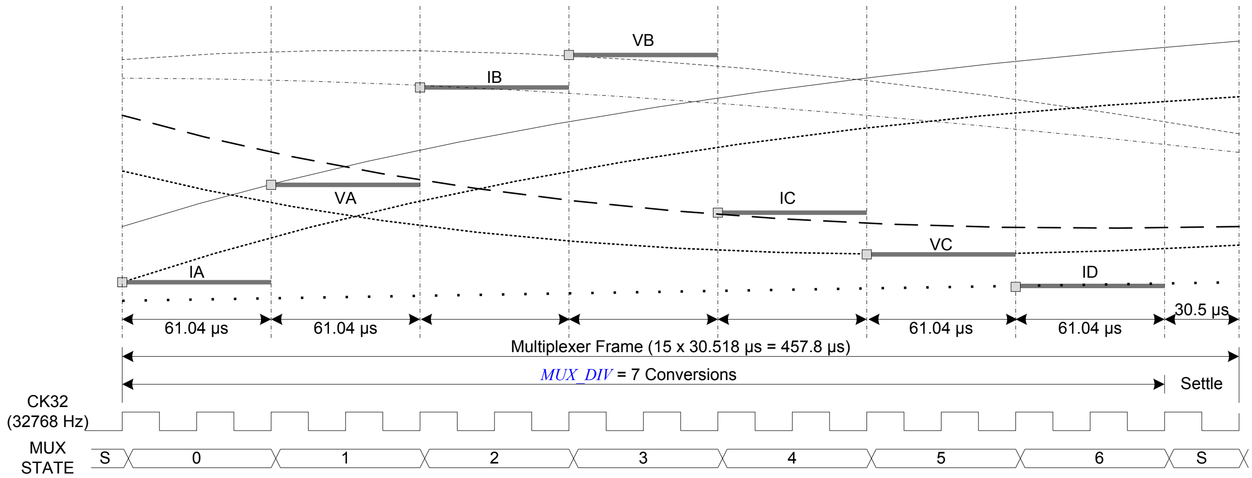


Figure 10: Samples from Multiplexer Cycle (Frame)

The end of each multiplexer cycle is signaled to the MPU by the CE_BUSY interrupt. At the end of each multiplexer cycle, status information, such as sag data and the digitized input signal, is available to the MPU.

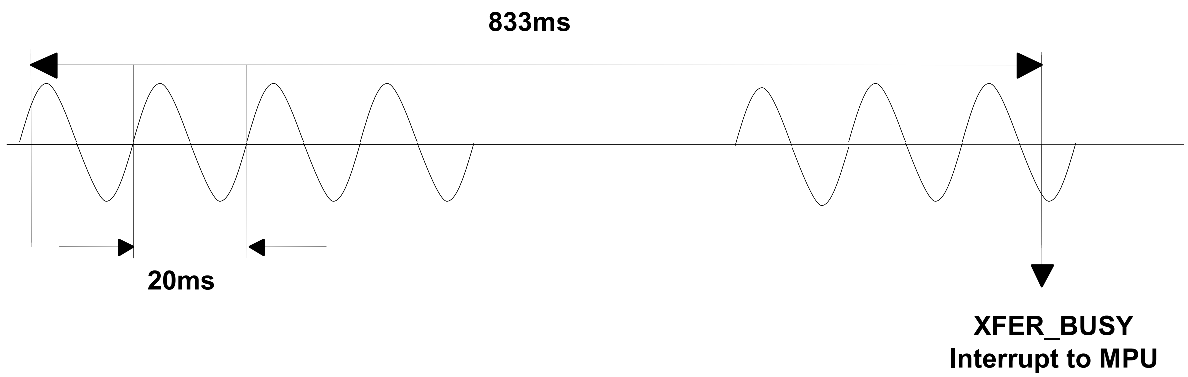


Figure 11: Accumulation Interval

Figure 11 shows the accumulation interval resulting from *SUM_SAMPS[12:0]* = 1819 (I/O RAM *0x2107[4:0]* and *0x2108[7:0]*), consisting of 1819 samples of 457.8 µs each, followed by the XFER_BUSY interrupt. The sampling in this example is applied to a 50 Hz signal. There is no correlation between the line signal frequency and the choice of *SUM_SAMPS[12:0]*. Furthermore, sampling does not have to start when the line voltage crosses the zero line, and the length of the accumulation interval need not be an integer multiple of the signal cycles.

2.4 80515 MPU Core

The 71M6543 include an 80515 MPU (8-bit, 8051-compatible) that processes most instructions in one clock cycle. Using a 4.9 MHz clock results in a processing throughput of 4.9 MIPS. The 80515 architecture eliminates redundant bus states and implements parallel execution of fetch and execution phases. Normally, a machine cycle is aligned with a memory fetch, therefore, most of the 1-byte instructions are performed in a single machine cycle (MPU clock cycle). This leads to an 8x average performance improvement (in terms of MIPS) over the Intel® 8051 device running at the same clock frequency.

Table 8 shows the CKMPU frequency as a function of the MCK clock (19.6608 MHz) divided by the MPU clock divider *MPU_DIV[2:0] (I/O RAM 0x2200[2:0])*. Actual processor clocking speed can be adjusted to the total processing demand of the application (metering calculations, AMR management, memory management, LCD driver management and I/O management) using *MPU_DIV[2:0]*, as shown in Table 8.

Table 8: CKMPU Clock Frequencies

<table>
<tr><th>MPU_DIV [2:0]</th><th>CKMPU Frequency</th></tr>
<tr><td>000</td><td>4.9152 MHz</td></tr>
<tr><td>001</td><td>2.4576 MHz</td></tr>
<tr><td>010</td><td>1.2288 MHz</td></tr>
<tr><td>011</td><td>614.4 kHz</td></tr>
<tr><td>100</td><td rowspan="4">307.2 kHz</td></tr>
<tr><td>101</td></tr>
<tr><td>110</td></tr>
<tr><td>111</td></tr>
</table>

Typical measurement and metering functions based on the results provided by the internal 32-bit compute engine (CE) are available for the MPU as part of the Maxim demonstration code, which is provided to help reduce the product design cycle.

2.4.1 Memory Organization and Addressing

The 80515 MPU core incorporates the Harvard architecture with separate code and data spaces. Memory organization in the 80515 is similar to that of the industry standard 8051. There are three memory areas: Program memory (Flash, shared by MPU and CE), external RAM (Data RAM, shared by the CE and MPU, Configuration or I/O RAM), and internal data memory (Internal RAM). Table 9 shows the memory map.

Program Memory

The 80515 can address up to 64 KB of program memory space (0x0000 to 0xFFFF). Program memory is read when the MPU fetches instructions or performs a MOVC operation.

After reset, the MPU starts program execution from program memory location 0x0000. The lower part of the program memory includes reset and interrupt vectors. The interrupt vectors are spaced at 8-byte intervals, starting from 0x0003.

MPU External Data Memory (XRAM)

Both internal and external memory is physically located on the 71M6543 device. The external memory referred to in this documentation is only external to the 80515 MPU core.

5 KB of RAM starting at address 0x0000 is shared by the CE and MPU. The CE normally uses the first 1 KB, leaving 4 KB for the MPU. Different versions of the CE code use varying amounts. Consult the documentation for the specific code version being used for the exact limit.

To change the slot assignments established by *MUXn_SEL[3:0]*, first set *MUX_DIV[3:0]* to zero, then change the *MUXn_SEL[3:0]* slot assignments, and finally set *MUX_DIV[3:0]* to the number of active MUX frame slots.

The 80515 writes into external data memory when the MPU executes a MOVX @Ri,A or MOVX @DPTR,A instruction. The MPU reads external data memory by executing a MOVX A,@Ri or MOVX A,@DPTR instruction (*PDATA, SFR 0xBF*, provides the upper 8 bytes for the MOVX A,@Ri instruction).

Internal and External Memory Map

Table 9 shows the address, type, use and size of the various memory components.

Table 9: Memory Map

Address (hex)	Memory Technology	Memory Type	Name	Typical Usage	Memory Size (bytes)
0000-FFFF	Flash Memory	Non-volatile	Program memory	MPU Program and non-volatile data	64 KB
				CE program (on 1 KB boundary)	3 KB max.
0000-13FF	Static RAM	Volatile	External RAM (XRAM)	Shared by CE and MPU	5 KB
2000-27FF	Static RAM	Volatile	Configuration RAM (I/O RAM)	Hardware control	2 KB
2800-287F	Static RAM	Non-volatile (battery)	Configuration RAM (I/O RAM)	Battery-buffered memory	128
0000-00FF	Static RAM	Volatile	Internal RAM	Part of 80515 Core	256

MOVX Addressing

There are two types of instructions differing in whether they provide an 8-bit or 16-bit indirect address to the external data RAM.

In the first type, MOVX A,@Ri, the contents of R0 or R1 in the current register bank provide the eight lower-ordered bits of address. The eight high-ordered bits of the address are specified with the *PDATA* SFR. This method allows the user paged access (256 pages of 256 bytes each) to all ranges of the external data RAM.

In the second type of MOVX instruction, MOVX A,@DPTR, the data pointer generates a 16-bit address. This form is faster and more efficient when accessing very large data arrays (up to 64 KB), since no additional instructions are needed to set up the eight high ordered bits of the address.

It is possible to mix the two MOVX types. This provides the user with four separate data pointers, two with direct access and two with paged access, to the entire 64 KB of external memory range.

Dual Data Pointer

The Dual Data Pointer accelerates the block moves of data. The standard *DPTR* is a 16-bit register that is used to address external memory or peripherals. In the 80515 core, the standard data pointer is called *DPTR*, the second data pointer is called *DPTR1*. The data pointer select bit, located in the LSB of the *DPS* register (*DPS*[0], *SFR 0x92*), chooses the active pointer. *DPTR* is selected when *DPS*[0] = 0 and *DPTR1* is selected when *DPS*[0] = 1.

The user switches between pointers by toggling the LSB of the *DPS* register. The values in the data pointers are not affected by the LSB of the *DPS* register. All *DPTR* related instructions use the currently selected *DPTR* for any activity.

The second data pointer may not be supported by certain compilers.

DPTR1 is useful for copy routines, where it can make the inner loop of the routine two instructions faster compared to the reloading of *DPTR* from registers. Any interrupt routine using *DPTR1* must save and restore *DPS*, *DPTR* and *DPTR1*, which increases stack usage and slows down interrupt latency.

By selecting the Evatronics R80515 core in the Keil compiler project settings and by using the compiler directive "MODC2", dual data pointers are enabled in certain library routines.

An alternative data pointer is available in the form of the *PDATA* register (*SFR 0xBF*), sometimes referred to as *USR2*). It defines the high byte of a 16-bit address when reading or writing XDATA with the instruction MOVX A,@Ri or MOVX @Ri,A.

Internal Data Memory Map and Access

The Internal data memory provides 256 bytes (0x00 to 0xFF) of data memory. The internal data memory address is always 1 byte wide. Table 10 shows the internal data memory map.

The Special Function Registers (SFR) occupy the upper 128 bytes. The SFR area of internal data memory is available only by direct addressing. Indirect addressing of this area accesses the upper 128 bytes of Internal RAM. The lower 128 bytes contain working registers and bit addressable memory. The lower 32 bytes form four banks of eight registers (R0-R7). Two bits on the program memory status word (*PSW, SFR 0xD0*) select which bank is in use. The next 16 bytes form a block of bit addressable memory space at addresses 0x00-0x7F. All of the bytes in the lower 128 bytes are accessible through direct or indirect addressing.

Table 10: Internal Data Memory Map

Address Range		Direct Addressing	Indirect Addressing
0x80	0xFF	Special Function Registers (SFRs)	RAM
0x30	0x7F	Byte addressable area	
0x20	0x2F	Bit addressable area	
0x00	0x1F	Register banks R0…R7	

2.4.2 Special Function Registers (SFRs)

A map of the Special Function Registers is shown in Table 11.

Only a few addresses in the SFR memory space are occupied, the others are not implemented. A read access to unimplemented addresses returns undefined data, while a write access has no effect. SFRs specific to the 71M6543 are shown in **bold** print on a gray field. The registers at 0x80, 0x88, 0x90, etc., are bit addressable, all others are byte addressable.

Table 11: Special Function Register Map

Hex/ Bin	Bit Addressable	Byte Addressable						Bin/ Hex
	X000	X001	X010	X011	X100	X101	X110	X111	
F8	***FLAG1***	***VSTAT***			***REMOTE0***	***SPI1***			FF
F0	*B*								F7
E8	***IFLAGS***								EF
E0	*A*								E7
D8	*WDCON*								DF
D0	*PSW*								D7
C8	*T2CON*								CF
C0	*IRCON*								C7
B8	*IEN1*	*IP1*	*S0RELH*	*S1RELH*				*PDATA*	BF
B0	***P3***		***FLSHCTL***				***FL_BANK***	***PGADR***	B7
A8	*IEN0*	*IP0*	*S0RELL*						AF
A0	***P2***	***DIR2***	***DIR0***						A7
98	*S0CON*	*S0BUF*	*IEN2*	*S1CON*	*S1BUF*	*S1RELL*	***EEDATA***	***EECTRL***	9F
90	***P1***	***DIR1***	*DPS*		***ERASE***				97
88	*TCON*	*TMOD*	*TL0*	*TL1*	*TH0*	*TH1*	*CKCON*		8F
80	*P0*	*SP*	*DPL*	*DPH*	*DPL1*	*DPH1*		*PCON*	87

2.4.3 Generic 80515 Special Function Registers

Table 12 shows the location, description and reset or power-up value of the generic 80515 SFRs. Additional descriptions of the registers can be found at the page numbers listed in the table.

Table 12: Generic 80515 SFRs - Location and Reset Values

Name	Address (Hex)	Reset value (Hex)	Description	Page(s)
P0	0x80	0xFF	Port 0	35
SP	0x81	0x07	Stack Pointer	34
DPL	0x82	0x00	Data Pointer Low 0	34
DPH	0x83	0x00	Data Pointer High 0	34
DPL1	0x84	0x00	Data Pointer Low 1	34
DPH1	0x85	0x00	Data Pointer High 1	34
PCON	0x87	0x00	Power Reduction Modes, UART Speed Control	38
TCON	0x88	0x00	Timer/Counter Control	41
TMOD	0x89	0x00	Timer Mode Control	39
TL0	0x8A	0x00	Timer 0, low byte	38
TL1	0x8B	0x00	Timer 1, high byte	38
TH0	0x8C	0x00	Timer 0, low byte	38
TH1	0x8D	0x00	Timer 1, high byte	38
CKCON	0x8E	0x01	Clock Control (Stretch=1)	35
P1	0x90	0xFF	Port 1	35
DPS	0x92	0x00	Data Pointer select Register	31
S0CON	0x98	0x00	Serial Port 0, Control Register	37
S0BUF	0x99	0x00	Serial Port 0, Data Buffer	35
IEN2	0x9A	0x00	Interrupt Enable Register 2	41
S1CON	0x9B	0x00	Serial Port 1, Control Register	37
S1BUF	0x9C	0x00	Serial Port 1, Data Buffer	35
S1RELL	0x9D	0x00	Serial Port 1, Reload Register, low byte	35
P2	0xA0	0xFF	Port 2	35
IEN0	0xA8	0x00	Interrupt Enable Register 0	40
IP0	0xA9	0x00	Interrupt Priority Register 0	43
S0RELL	0xAA	0xD9	Serial Port 0, Reload Register, low byte	35
P3	0xB0	0xFF	Port 3	35
IEN1	0xB8	0x00	Interrupt Enable Register 1	40
IP1	0xB9	0x00	Interrupt Priority Register 1	43
S0RELH	0xBA	0x03	Serial Port 0, Reload Register, high byte	35
S1RELH	0xBB	0x03	Serial Port 1, Reload Register, high byte	35
PDATA	0xBF	0x00	High address byte for MOVX@Ri - also called *USR2*	31
IRCON	0xC0	0x00	Interrupt Request Control Register	41
T2CON	0xC8	0x00	Polarity for INT2 and INT3	41
PSW	0xD0	0x00	Program Status Word	34
WDCON	0xD8	0x00	Baud Rate Control Register (only WDCON[7] bit used)	35
A	0xE0	0x00	Accumulator	34
B	0xF0	0x00	B Register	34

Accumulator (*ACC, A, SFR 0x E0*):

ACC is the accumulator register. Most instructions use the accumulator to hold the operand. The mnemonics for accumulator-specific instructions refer to accumulator as *A*, not *ACC*.

***B* Register (*SFR 0xF0*):**

The *B* register is used during multiply and divide instructions. It can also be used as a scratch-pad register to hold temporary data.

Program Status Word (*PSW, SFR 0xD0*):

This register contains various flags and control bits for the selection of the register banks (see Table 13).

Table 13: *PSW* Bit Functions (SFR 0xD0)

<table>
<tr><th>PSW Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>7</td><td>CV</td><td>Carry flag.</td></tr>
<tr><td>6</td><td>AC</td><td>Auxiliary Carry flag for BCD operations.</td></tr>
<tr><td>5</td><td>F0</td><td>General purpose Flag 0 available for user.
F0 is not to be confused with the F0 flag in the CESTATUS register.</td></tr>
<tr><td>4</td><td>RS1</td><td rowspan="2">Register bank select control bits. The contents of RS1 and RS0 select the working register bank:
<table>
<tr><th>RS1/RS0</th><th>Bank selected</th><th>Location</th></tr>
<tr><td>00</td><td>Bank 0</td><td>0x00 – 0x07</td></tr>
<tr><td>01</td><td>Bank 1</td><td>0x08 – 0x0F</td></tr>
<tr><td>10</td><td>Bank 2</td><td>0x10 – 0x17</td></tr>
<tr><td>11</td><td>Bank 3</td><td>0x18 – 0x1F</td></tr>
</table></td></tr>
<tr><td>3</td><td>RS0</td></tr>
<tr><td>2</td><td>OV</td><td>Overflow flag.</td></tr>
<tr><td>1</td><td>–</td><td>User defined flag.</td></tr>
<tr><td>0</td><td>P</td><td>Parity flag, affected by hardware to indicate odd or even number of one bits in the Accumulator, i.e. even parity.</td></tr>
</table>

Stack Pointer (*SP, SFR 0x81*):

The stack pointer is a 1-byte register initialized to 0x07 after reset. This register is incremented before PUSH and CALL instructions, causing the stack to begin at location 0x08.

Data Pointer:

The data pointers (*DPTR and DPRT1*) are 2 bytes wide. The lower part is *DPL (SFR 0x82)* and *DPL1 (SFR 0x84),* respectively. The highest is *DPH (SFR 0x83)* and *DPH1 (SFR 0x85),* respectively. The data pointers can be loaded as two registers (e.g. MOV DPL,#data8). They are generally used to access external code or data space (e.g. MOVC A,@A+DPTR or MOVX A,@DPTR respectively).

Program Counter:

The program counter (*PC*) is 2 bytes wide and initialized to 0x0000 after reset. This register is incremented when fetching operation code or when operating on data from program memory.

Port Registers:

SEGDIO0 through SEGDIO15 are controlled by Special Function Registers *P0*, *P1, P2*, and *P3* as shown in Table 14. Above SEGDIO15, the *LCD_SEGDIOn[ ]* registers in I/O RAM are used. Since the direction bits are contained in the upper nibble of each SFR *Pn* register and the DIO bits are contained in the lower nibble, it is possible to configure the direction of a given DIO pin and set its output value with a single write operation, thus facilitating the implementation of bit-banged interfaces. Writing a 1 to a *DIO_DIR* bit configures the corresponding DIO as an output, while writing a 0 configures it as an input. Writing a 1 to a DIO bit causes the corresponding pin to be at high level (V3P3), while writing a 0 causes the corresponding pin to be held at a low level (GND). See 2.5.10 Digital I/O for additional details.

Table 14: Port Registers (SEGDIO0-15)

SFR Name	SFR Address	D7	D6	D5	D4	D3	D2	D1	D0
P0	80	*DIO_DIR[3:0]*				*DIO[3:0]*			
P1	90	*DIO_DIR[7:4]*				*DIO[7:4]*			
P2	A0	*DIO_DIR[11:8]*				*DIO[11:8]*			
P3	B0	*DIO_DIR[15:12]*				*DIO[15:11]*			

All DIO ports on the chip are bi-directional. Each of them consists of a latch (SFR *P0* to *P3*), an output driver and an input buffer, therefore the MPU can output or read data through any of these ports. Even if a DIO pin is configured as an output, the state of the pin can still be read by the MPU, for example when counting pulses issued via DIO pins that are under CE control.

CAUTION: At power-up SEGDIO0-15 are configured as outputs, but the pins are in a high-impedance state because *PORT_E* = 0 (*I/O RAM 0x270C[5]*). Host firmware should first configure SEGDIO0-15 to the desired state, then set *PORT_E* = 1 to enable the function.

Clock Stretching (*CKCON[2:0], SFR 0x8E*)

The *CKCON[2:0]* field defines the stretch memory cycles that are used for MOVX instructions when accessing external peripherals. The practical value of this register for the 71M6543 is to guarantee access to XRAM between CE, MPU, and SPI. The default setting of *CKCON[2:0]* (001) should be changed to 000 for best performance.

Table 15 shows how the signals of the External Memory Interface change when stretch values are set from 0 to 7. The widths of the signals are counted in MPU clock cycles. The post-reset state of the *CKCON[2:0]* field (001), which is shown in **bold** in the table, performs the MOVX instructions with a stretch value equal to 1.

Table 15: Stretch Memory Cycle Width

CKCON[2:0]	Stretch Value	Read Signal Width		Write Signal Width	
		memaddr	memrd	memaddr	memwr
000	0	1	1	2	1
001	**1**	**2**	**2**	**3**	**1**
010	2	3	3	4	2
011	3	4	4	5	3
100	4	5	5	6	4
101	5	6	6	7	5
110	6	7	7	8	6
111	7	8	8	9	7

2.4.4 Instruction Set

All instructions of the generic 8051 microcontroller are supported. A complete list of the instruction set and of the associated op-codes is contained in the *71M654x Software User's Guide (SUG)*.

2.4.5 UARTs

The 71M6543 include a UART (UART0) that can be programmed to communicate with a variety of AMR modules and other external devices. A second UART (UART1) is connected to the optical port, as described in the 2.5.9 UART and Optical Interface on page 56.

The UARTs are dedicated 2-wire serial interfaces, which can communicate with an external host processor at up to 38,400 bits/s (with MPU clock = 1.2288 MHz). The operation of the RX and TX UART0 pins is as follows:

- UART0 RX: Serial input data are applied at this pin. Conforming to RS-232 standard, the bytes are input LSB first.
- UART0 TX: This pin is used to output the serial data. The bytes are output LSB first.

The 71M6543 has several UART-related registers for the control and buffering of serial data.

A single SFR register serves as both the transmit buffer and receive buffer (*S0BUF*, *SFR 0x99* for UART0 and *S1BUF*, *SFR 0x9C* for UART1). When written by the MPU, *SxBUF* acts as the transmit buffer, and when read by the MPU, it acts as the receive buffer. Writing data to the transmit buffer starts the transmission by the associated UART. Received data are available by reading from the receive buffer. Both UARTs can simultaneously transmit and receive data.

WDCON[7] (SFR 0xD8) selects whether timer 1 or the internal baud rate generator is used. All UART transfers are programmable for parity enable, parity, 2 stop bits/1 stop bit and XON/XOFF options for variable communication baud rates from 300 to 38400 bps. Table 16 shows how the baud rates are calculated. Table 17 shows the selectable UART operation modes.

Table 16: Baud Rate Generation

	Using Timer 1 (*WDCON[7]* = 0)	Using Internal Baud Rate Generator (*WDCON[7]* = 1)
UART0	$2^{smod} * f_{CKMPU} / (384 * (256\text{-}TH1))$	$2^{smod} * f_{CKMPU} / (64 * (2^{10}\text{-}S0REL))$
UART1	N/A	$f_{CKMPU} / (32 * (2^{10}\text{-}S1REL))$

S0REL and *S1REL* are 10-bit values derived by combining bits from the respective timer reload registers. (*S0RELL, S0RELH, S1RELL, S1RELH* are *SFR 0xAA, SFR 0xBA, SFR 0x9D* and *SFR 0xBB*, respectively) *SMOD* is the *SMOD* bit in the SFR *PCON* register (*SFR 0x87*). *TH1 (SFR 0x8D)* is the high byte of timer 1.

Table 17: UART Modes

	UART 0	UART 1
Mode 0	N/A	Start bit, 8 data bits, parity, stop bit, variable baud rate (internal baud rate generator)
Mode 1	Start bit, 8 data bits, stop bit, variable baud rate (internal baud rate generator or timer 1)	Start bit, 8 data bits, stop bit, variable baud rate (internal baud rate generator)
Mode 2	Start bit, 8 data bits, parity, stop bit, fixed baud rate 1/32 or 1/64 of f_{CKMPU}	N/A
Mode 3	Start bit, 8 data bits, parity, stop bit, variable baud rate (internal baud rate generator or timer 1)	N/A

Parity of serial data is available through the P flag of the accumulator. 7-bit serial modes with parity, such as those used by the FLAG protocol, can be simulated by setting and reading bit 7 of 8-bit output data. 7-bit serial modes without parity can be simulated by setting bit 7 to a constant 1. 8-bit serial modes with parity can be simulated by setting and reading the 9th bit, using the control bits *TB80* (*S0CON[3]*) and *TB81* (*S1CON[3]*) in the *S0CON* (*SFR 0x98*) and *S1CON* (*SFR 0x9B*) registers for transmit and *RB81* (*S1CON[2]*) for receive operations.

All supported operation modes use oversampling for the incoming bit stream when receiving data. Each bit is sampled three times at the projected middle of the bit duration. This technique allows for deviations of the received baud rate from nominal of up to 3.5%.

The feature of receiving 9 bits (Mode 3 for UART0, Mode A for UART1) can be used as handshake signals for inter-processor communication in multi-processor systems. In this case, the slave processors have bit *SM20* (*S0CON[5]*) for UART0, or *SM21* (*S1CON[5]* for UART1, set to 1. When the master processor outputs the slave's address, it sets the 9th bit to 1, causing a serial port receive interrupt in all the slaves. The slave processors compare the received byte with their address. If there is a match, the addressed slave clears *SM20* or *SM21* and receive the rest of the message. The rest of the slaves ignore the message. After addressing the slave, the host outputs the rest of the message with the 9th bit set to 0, so no additional serial port receive interrupts is generated.

UART Control Registers:

The functions of UART0 and UART1 depend on the setting of the Serial Port Control Registers *S0CON* and *S1CON* shown in Table 18 and Table 19, respectively, and the *PCON* register shown in Table 20.

Since the *TI0*, *RI0*, *TI1* and *RI1* bits are in an SFR bit addressable byte, common practice would be to clear them with a bit operation, but this must be avoided. The hardware implements bit operations as a byte wide read-modify-write hardware macro. If an interrupt occurs after the read, but before the write, its flag is cleared unintentionally.

The proper way to clear these flag bits is to write a byte mask consisting of all ones except for a zero in the location of the bit to be cleared. The flag bits are configured in hardware to ignore ones written to them.

Table 18: The *S0CON* (UART0) Register (SFR 0x98)

<table>
<tr><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>S0CON[7]</td><td>SM0</td><td rowspan="2">The SM0 and SM1 bits set the UART0 mode:<table><tr><th>Mode</th><th>Description</th><th>SM0</th><th>SM1</th></tr><tr><td>0</td><td>N/A</td><td>0</td><td>0</td></tr><tr><td>1</td><td>8-bit UART</td><td>0</td><td>1</td></tr><tr><td>2</td><td>9-bit UART</td><td>1</td><td>0</td></tr><tr><td>3</td><td>9-bit UART</td><td>1</td><td>1</td></tr></table></td></tr>
<tr><td>S0CON[6]</td><td>SM1</td></tr>
<tr><td>S0CON[5]</td><td>SM20</td><td>Enables the inter-processor communication feature.</td></tr>
<tr><td>S0CON[4]</td><td>REN0</td><td>If set, enables serial reception. Cleared by software to disable reception.</td></tr>
<tr><td>S0CON[3]</td><td>TB80</td><td>The 9th transmitted data bit in Modes 2 and 3. Set or cleared by the MPU, depending on the function it performs (parity check, multiprocessor communication etc.)</td></tr>
<tr><td>S0CON[2]</td><td>RB80</td><td>In Modes 2 and 3 it is the 9th data bit received. In Mode 1, SM20 is 0, RB80 is the stop bit. In mode 0, this bit is not used. Must be cleared by software.</td></tr>
<tr><td>S0CON[1]</td><td>TI0</td><td>Transmit interrupt flag; set by hardware after completion of a serial transfer. Must be cleared by software (see Caution above).</td></tr>
<tr><td>S0CON[0]</td><td>RI0</td><td>Receive interrupt flag; set by hardware after completion of a serial reception. Must be cleared by software (see Caution above).</td></tr>
</table>

Table 19: The *S1CON* (UART1) Register (SFR 0x9B)

<table>
<tr><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>S1CON[7]</td><td>SM</td><td>Sets the baud rate and mode for UART1.<table><tr><th>SM</th><th>Mode</th><th>Description</th><th>Baud Rate</th></tr><tr><td>0</td><td>A</td><td>9-bit UART</td><td>variable</td></tr><tr><td>1</td><td>B</td><td>8-bit UART</td><td>variable</td></tr></table></td></tr>
<tr><td>S1CON[5]</td><td>SM21</td><td>Enables the inter-processor communication feature.</td></tr>
<tr><td>S1CON[4]</td><td>REN1</td><td>If set, enables serial reception. Cleared by software to disable reception.</td></tr>
<tr><td>S1CON[3]</td><td>TB81</td><td>The 9th transmitted data bit in Mode A. Set or cleared by the MPU, depending on the function it performs (parity check, multiprocessor communication etc.)</td></tr>
<tr><td>S1CON[2]</td><td>RB81</td><td>In Modes A and B, it is the 9th data bit received. In Mode B, if SM21 is 0, RB81 is the stop bit. Must be cleared by software</td></tr>
<tr><td>S1CON[1]</td><td>TI1</td><td>Transmit interrupt flag, set by hardware after completion of a serial transfer. Must be cleared by software (see Caution above).</td></tr>
<tr><td>S1CON[0]</td><td>RI1</td><td>Receive interrupt flag, set by hardware after completion of a serial reception. Must be cleared by software (see Caution above).</td></tr>
</table>

Table 20: *PCON* Register Bit Description (*SFR 0x87*)

Bit	Symbol	Function
PCON[7]	*SMOD*	The *SMOD* bit doubles the baud rate when set

2.4.6 Timers and Counters

The 80515 has two 16-bit timer/counter registers: Timer 0 and Timer 1. These registers can be configured for counter or timer operations.

In timer mode, the register is incremented every machine cycle, i.e. it counts up once for every 12 periods of the MPU clock. In counter mode, the register is incremented when the falling edge is observed at the corresponding input signal T0 or T1 (T0 and T1 are the timer gating inputs derived from certain DIO pins, see 2.5.10 Digital I/O). Since it takes 2 machine cycles to recognize a 1-to-0 event, the maximum input count rate is 1/2 of the clock frequency (CKMPU). There are no restrictions on the duty cycle, however to ensure proper recognition of the 0 or 1 state, an input should be stable for at least 1 machine cycle.

Four operating modes can be selected for Timer 0 and Timer 1, as shown in Table 21 and Table 22. The *TMOD* (*SFR 0x89*) register, shown in
Table 23, is used to select the appropriate mode. The timer/counter operation is controlled by the *TCON* (*SFR 0x88*) register, which is shown in Table 24. Bits *TR1* (*TCON[6]*) and *TR0* (*TCON[4]*) in the *TCON* register start their associated timers when set.

Table 21: Timers/Counters Mode Description

M1	M0	Mode	Function
0	0	Mode 0	13-bit Counter/Timer mode with 5 lower bits in the *TL0* or *TL1* (*SFR 0x8A or SFR 0x8B*) register and the remaining 8 bits in the *TH0* or *TH1* (*SFR 0x8C or SFR 0x8D*) register (for Timer 0 and Timer 1, respectively). The 3 high order bits of *TL0* and *TL1* are held at zero.
0	1	Mode 1	16-bit Counter/Timer mode.
1	0	Mode 2	8-bit auto-reload Counter/Timer. The reload value is kept in *TH0* or *TH1*, while *TL0* or *TL1* is incremented every machine cycle. When *TL(*x) overflows, a value from *TH(*x) is copied to *TL*(x) (where x is 0 for counter/timer 0 or 1 for counter/timer 1.
1	1	Mode 3	If Timer 1 *M1* and *M0* bits are set to 1, Timer 1 stops. If Timer 0 *M1* and *M0* bits are set to 1, Timer 0 acts as two independent 8-bit Timer/Counters.

In Mode 3, *TL0* is affected by *TR0* and gate control bits, and sets the *TF0* flag on overflow, while *TH0* is affected by the *TR1* bit, and the *TF1* flag is set on overflow.

Table 22 specifies the combinations of operation modes allowed for Timer 0 and Timer 1.

Table 22: Allowed Timer/Counter Mode Combinations

	Timer 1		
	Mode 0	**Mode 1**	**Mode 2**
Timer 0 - mode 0	Yes	Yes	Yes
Timer 0 - mode 1	Yes	Yes	Yes
Timer 0 - mode 2	Not allowed	Not allowed	Yes

Table 23: *TMOD* Register Bit Description (SFR 0x89)

Bit	Symbol	Function
Timer/Counter 1:		
TMOD[7]	*Gate*	If *TMOD[7]* is set, external input signal control is enabled for Counter 1. The *TR0* bit in the *TCON* register (*SFR 0x88*) must also be set in order for Counter 0 to increment. With these settings, Counter 0 increments on every falling edge of the logic signal applied to one or more of the SEGDIO2-11 pins, as specified by the contents of the *DIO_R2* through *DIO_R11* registers. See 2.5.10 Digital I/O and LCD Segment Drivers and Table 46.
TMOD[6]	*C/T*	Selects timer or counter operation. When set to 1, a counter operation is performed. When cleared to 0, the corresponding register functions as a timer.
TMOD[5:4]	*M1:M0*	Selects the mode for Timer/Counter 0 as shown in Table 21.
Timer/Counter 0		
TMOD[3]	*Gate*	If *TMOD[3]* is set, external input signal control is enabled for Counter 0. The *TR1* bit in the *TCON* register (*SFR 0x88*) must also be set in order for Counter 1 to increment. With these settings, Counter 1 increments on every falling edge of the logic signal applied to one or more of the SEGDIO2-11 pins, as specified by the contents of the *DIO_R2* through *DIO_R11* registers. See 2.5.10 Digital I/O and LCD Segment Drivers and Table 46.
TMOD[2]	*C/T*	Selects timer or counter operation. When set to 1, a counter operation is performed. When cleared to 0, the corresponding register functions as a timer.
TMOD[1:0]	*M1:M0*	Selects the mode for Timer/Counter 1, as shown in Table 21.

Table 24: The *TCON* Register Bit Functions (SFR 0x88)

Bit	Symbol	Function
TCON[7]	*TF1*	The Timer 1 overflow flag is set by hardware when Timer 1 overflows. This flag can be cleared by software and is automatically cleared when an interrupt is processed.
TCON[6]	*TR1*	Timer 1 run control bit. If cleared, Timer 1 stops.
TCON[5]	*TF0*	Timer 0 overflow flag set by hardware when Timer 0 overflows. This flag can be cleared by software and is automatically cleared when an interrupt is processed.
TCON[4]	*TR0*	Timer 0 Run control bit. If cleared, Timer 0 stops.
TCON[3]	*IE1*	Interrupt 1 edge flag is set by hardware when the falling edge on external pin int1 is observed. Cleared when an interrupt is processed.
TCON[2]	*IT1*	Interrupt 1 type control bit. Selects either the falling edge or low level on input pin to cause an interrupt.
TCON[1]	*IE0*	Interrupt 0 edge flag is set by hardware when the falling edge on external pin int0 is observed. Cleared when an interrupt is processed.
TCON[0]	*IT0*	Interrupt 0 type control bit. Selects either the falling edge or low level on input pin to cause interrupt.

2.4.7 WD Timer (Software Watchdog Timer)

There is no internal software watchdog timer. Use the standard hardware watchdog timer instead (see 2.5.13 Hardware Watchdog Timer).

2.4.8 Interrupts

The 80515 provides 11 interrupt sources with four priority levels. Each source has its own interrupt request flag(s) located in a special function register (*TCON, IRCON, and SCON*). Each interrupt requested by the corresponding flag can be individually enabled or disabled by the enable bits in *IEN0 (SFR 0xA8), IEN1 (SFR 0xB8)*, and *IEN2 (SFR 0x9A)*. Figure 12 shows the device interrupt structure.

Referring to Figure 12, interrupt sources can originate from within the 80515 MPU core (referred to as Internal Sources) or can originate from other parts of the 71M6543 SoC (referred to as External Sources). There are seven external interrupt sources, as seen in the leftmost part of Figure 12, and in Table 25 and Table 26 (i.e., *EX0-EX6*).

Interrupt Overview

When an interrupt occurs, the MPU vectors to the predetermined address as shown in Table 37. Once the interrupt service has begun, it can be interrupted only by a higher priority interrupt. The interrupt service is terminated by a return from instruction, RETI. When an RETI is performed, the processor returns to the instruction that would have been next when the interrupt occurred.

When the interrupt condition occurs, the processor also indicates this by setting a flag bit. This bit is set regardless of whether the interrupt is enabled or disabled. Each interrupt flag is sampled once per machine cycle, then samples are polled by the hardware. If the sample indicates a pending interrupt when the interrupt is enabled, then the interrupt request flag is set. On the next instruction cycle, the interrupt is acknowledged by hardware forcing an LCALL to the appropriate vector address, if the following conditions are met:

- No interrupt of equal or higher priority is already in progress.
- An instruction is currently being executed and is not completed.
- The instruction in progress is not RETI or any write access to the registers *IEN0, IEN1, IEN2, IP0* or *IP1*.

Special Function Registers for Interrupts

The following SFR registers control the interrupt functions:

- The interrupt enable registers: *IEN0, IEN1* and *IEN2* (see Table 25, Table 26 and Table 27).
- The Timer/Counter control registers, *TCON* and *T2CON* (see Table 28 and Table 29).
- The interrupt request register, *IRCON* (see Table 30).
- The interrupt priority registers: *IP0* and *IP1* (see Table 35).

Table 25: The *IEN0* Bit Functions (SFR 0xA8)

Bit	Symbol	Function
IEN0[7]	*EAL*	*EAL* = 0 disables all interrupts.
IEN0[6]	–	Not used.
IEN0[5]	–	Not used.
IEN0[4]	*ES0*	*ES0* = 0 disables serial channel 0 interrupt.
IEN0[3]	*ET1*	*ET1* = 0 disables timer 1 overflow interrupt.
IEN0[2]	*EX1*	*EX1* = 0 disables external interrupt 1.
IEN0[1]	*ET0*	*ET0* = 0 disables timer 0 overflow interrupt.
IEN0[0]	*EX0*	*EX0* = 0 disables external interrupt 0.

Table 26: The *IEN1* Bit Functions (SFR 0xB8)

Bit	Symbol	Function
IEN1[7]	–	Not used.
IEN1[6]	–	Not used.
IEN1[5]	*EX6*	*EX6* = 0 disables external interrupt 6.
IEN1[4]	*EX5*	*EX5* = 0 disables external interrupt 5.
IEN1[3]	*EX4*	*EX4* = 0 disables external interrupt 4.
IEN1[2]	*EX3*	*EX3* = 0 disables external interrupt 3.
IEN1[1]	*EX2*	*EX2* = 0 disables external interrupt 2.
IEN1[0]	–	Not used.

Table 27: The *IEN2* Bit Functions (SFR 0x9A)

Bit	Symbol	Function
IEN2[0]	*ES1*	*ES1* = 0 disables the serial channel 1 interrupt.

Table 28: *TCON* Bit Functions (SFR 0x88)

Bit	Symbol	Function
TCON[7]	*TF1*	Timer 1 overflow flag.
TCON[6]	*TR1*	Not used for interrupt control.
TCON[5]	*TF0*	Timer 0 overflow flag.
TCON[4]	*TR0*	Not used for interrupt control.
TCON[3]	*IE1*	External interrupt 1 flag.
TCON[2]	*IT1*	External interrupt 1 type control bit: 0 = interrupt on low level. 1 = interrupt on falling edge.
TCON[1]	*IE0*	External interrupt 0 flag
TCON[0]	*IT0*	External interrupt 0 type control bit: 0 = interrupt on low level. 1 = interrupt on falling edge.

Table 29: The *T2CON* Bit Functions (SFR 0xC8)

Bit	Symbol	Function
T2CON[7]	–	Not used.
T2CON[6]	*I3FR*	Polarity control for INT3: 0 = falling edge. 1 = rising edge.
T2CON[5]	*I2FR*	Polarity control for INT2: 0 = falling edge. 1 = rising edge.
T2CON[4:0]	–	Not used.

Table 30: The *IRCON* Bit Functions (SFR 0xC0)

Bit	Symbol	Function
IRCON[7]	–	Not used.
IRCON[6]	–	Not used.
IRCON[5]	*IEX6*	1 = External interrupt 6 flag.
IRCON[4]	*IEX5*	1 = External interrupt 5 flag.
IRCON[3]	*IEX4*	1 = External interrupt 4 flag.
IRCON[2]	*IEX3*	1 = External interrupt 3 flag.
IRCON[1]	*IEX2*	1 = External interrupt 2 flag.
IRCON[0]	–	Not used.

✓ *TF0* and *TF1* (Timer 0 and Timer 1 overflow flags) is automatically cleared by hardware when the service routine is called (Signals T0ACK and T1ACK – port ISR – active high when the service routine is called). IE0, IE1, and IEX2-IEX6 are cleared automatically when hardware causes execution to vector to the interrupt service routine.

External MPU Interrupts

The seven external interrupts are the interrupts external to the 80515 core, i.e. signals that originate in other parts of the 71M6543, for example the CE, DIO, RTC, or EEPROM interface.

The external interrupts are connected as shown in Table 31. The polarity of interrupts 2 and 3 is programmable in the MPU via the *I3FR* and *I2FR* bits in *T2CON (SFR 0xC8)*. Interrupts 2 and 3 should be programmed for falling sensitivity (*I3FR* = *I2FR* = 0). The generic 8051 MPU literature states that interrupts 4 through 6 are defined as rising-edge sensitive. Thus, the hardware signals attached to interrupts 5 and 6 are inverted to achieve the edge polarity shown in Table 31.

Table 31: External MPU Interrupts

External Interrupt	Connection	Polarity	Flag Reset
0	Digital I/O (IE0)	see 2.5.10	automatic
1	Digital I/O (IE1)	see 2.5.10	automatic
2	CE_PULSE (IE_XPULSE, IE_YPULSE, IE_WPULSE, IE_VPULSE)	rising	manual
3	CE_BUSY (IE3)	falling	automatic
4	VSTAT (VSTAT[2:0] changed) (IE4)	rising	automatic
5	EEPROM busy (falling), SPI (rising) (IE_EEX, IE_SPI)	—	manual
6	XFER_BUSY (falling), RTC_1SEC, RTC_1MIN, RTC_T (IE_XFER, IE_RTC1S, IE_RTC1M, IE_RTCT)	falling	manual

External interrupt 0 and 1 can be mapped to pins on the device using DIO resource maps. See 2.5.10 Digital I/O for more information.

SFR enable bits must be set to permit any of these interrupts to occur. Likewise, each interrupt has its own flag bit, which is set by the interrupt hardware, and reset by the MPU interrupt handler. XFER_BUSY, RTC_1SEC, RTC_1MIN, RTC_T, SPI, PLLRISE and PLLFALL have their own enable and flag bits in addition to the interrupt 6, 4 and enable and flag bits (see Table 32: Interrupt Enable and Flag Bits).

CAUTION

IE0 through IEX6 are cleared automatically when the hardware vectors to the interrupt handler. The other flags, IE_XFER through IE_VPULSE, are cleared by writing a zero to them.

Since these bits are in an SFR bit addressable byte, common practice would be to clear them with a bit operation, but this must be avoided. The hardware implements bit operations as a byte wide read-modify-write hardware macro. If an interrupt occurs after the read, but before the write, its flag is cleared unintentionally.

The proper way to clear the flag bits is to write a byte mask consisting of all ones except for a zero in the location of the bit to be cleared. The flag bits are configured in hardware to ignore ones written to them.

Table 32: Interrupt Enable and Flag Bits

Interrupt Enable		Interrupt Flag		Interrupt Description
Name	Location	Name	Location	
EX0	SFR A8[[0]	IE0	SFR 88[1]	External interrupt 0
EX1	SFR A8[2]	IE1	SFR 88[3]	External interrupt 1
EX2	SFR B8[1]	IEX2	SFR C0[1]	External interrupt 2
EX3	SFR B8[2]	IEX3	SFR C0[2]	External interrupt 3
EX4	SFR B8[3]	IEX4	SFR C0[3]	External interrupt 4
EX5	SFR B8[4]	IEX5	SFR C0[4]	External interrupt 5
EX6	SFR B8[5]	IEX6	SFR C0[5]	External interrupt 6
EX_XFER *EX_RTC1S*	2700[0] 2700[1]	IE_XFER IE_RTC1S	SFR E8[0] SFR E8[1]	XFER_BUSY interrupt (int 6) RTC_1SEC interrupt (int 6)

Interrupt Enable		Interrupt Flag		Interrupt Description
Name	Location	Name	Location	
EX_RTC1M	2700[2]	IE_RTC1M	SFR E8[2]	RTC_1MIN interrupt (int 6)
EX_RTCT	2700[4]	IE_RTCT	SFR E8[4]	RTC_T interrupt (int 6)
EX_SPI	2701[7]	IE_SPI	SFR F8[7]	SPI interrupt
EX_EEX	2700[7]	IE_EEX	SFR E8[7]	EEPROM interrupt
EX_XPULSE	2700[6]	IE_XPULSE	SFR E8[6]	CE_Xpulse interrupt (int 2)
EX_YPULSE	2700[5]	IE_YPULSE	SFR E8[5]	CE_Ypulse interrupt (int 2)
EX_WPULSE	2701[6]	IE_WPULSE	SFR F8[6]	CE_Wpulse interrupt (int 2)
EX_VPULSE	2701[5]	IE_VPULSE	SFR F8[5]	CE_Vpulse interrupt (int 2)

Interrupt Priority Level Structure

All interrupt sources are combined in groups, as shown in Table 33.

Table 33: Interrupt Priority Level Groups

Group	Group Members	
0	External interrupt 0	Serial channel 1 interrupt
1	Timer 0 interrupt	External interrupt 2
2	External interrupt 1	External interrupt 3
3	Timer 1 interrupt	External interrupt 4
4	Serial channel 0 interrupt	External interrupt 5
5	–	External interrupt 6

Each group of interrupt sources can be programmed individually to one of four priority levels (as shown in Table 34) by setting or clearing one bit in the SFR interrupt priority register *IP0* (*SFR 0xA9*) and one in *IP1(SFR 0xB9)* (Table 35). If requests of the same priority level are received simultaneously, an internal polling sequence as shown in Table 36 determines which request is serviced first.

✓ Changing interrupt priorities while interrupts are enabled can easily cause software defects. It is best to set the interrupt priority registers only once during initialization before interrupts are enabled.

Table 34: Interrupt Priority Levels

IP1[x]	*IP0*[x]	Priority Level
0	0	Level 0 (lowest)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest)

Table 35: Interrupt Priority Registers (*IP0* and *IP1*)

Register	Address	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
IP0	SFR 0xA9	–	–	*IP0[5]*	*IP0[4]*	*IP0[3]*	*IP0[2]*	*IP0[1]*	*IP0[0]*
IP1	SFR 0xB9	–	–	*IP1[5]*	*IP1[4]*	*IP1[3]*	*IP1[2]*	*IP1[1]*	*IP1[0]*

Table 36: Interrupt Polling Sequence

External interrupt 0	Polling sequence
Serial channel 1 interrupt	
Timer 0 interrupt	
External interrupt 2	
External interrupt 1	
External interrupt 3	
Timer 1 interrupt	
External interrupt 4	
Serial channel 0 interrupt	
External interrupt 5	
External interrupt 6	

Interrupt Sources and Vectors

Table 37 shows the interrupts with their associated flags and vector addresses.

Table 37: Interrupt Vectors

Interrupt Request Flag	Description	Interrupt Vector Address
IE0	External interrupt 0	0x0003
TF0	Timer 0 interrupt	0x000B
IE1	External interrupt 1	0x0013
TF1	Timer 1 interrupt	0x001B
RI0/TI0	Serial channel 0 interrupt	0x0023
RI1/TI1	Serial channel 1 interrupt	0x0083
IEX2	External interrupt 2	0x004B
IEX3	External interrupt 3	0x0053
IEX4	External interrupt 4	0x005B
IEX5	External interrupt 5	0x0063
IEX6	External interrupt 6	0x006B

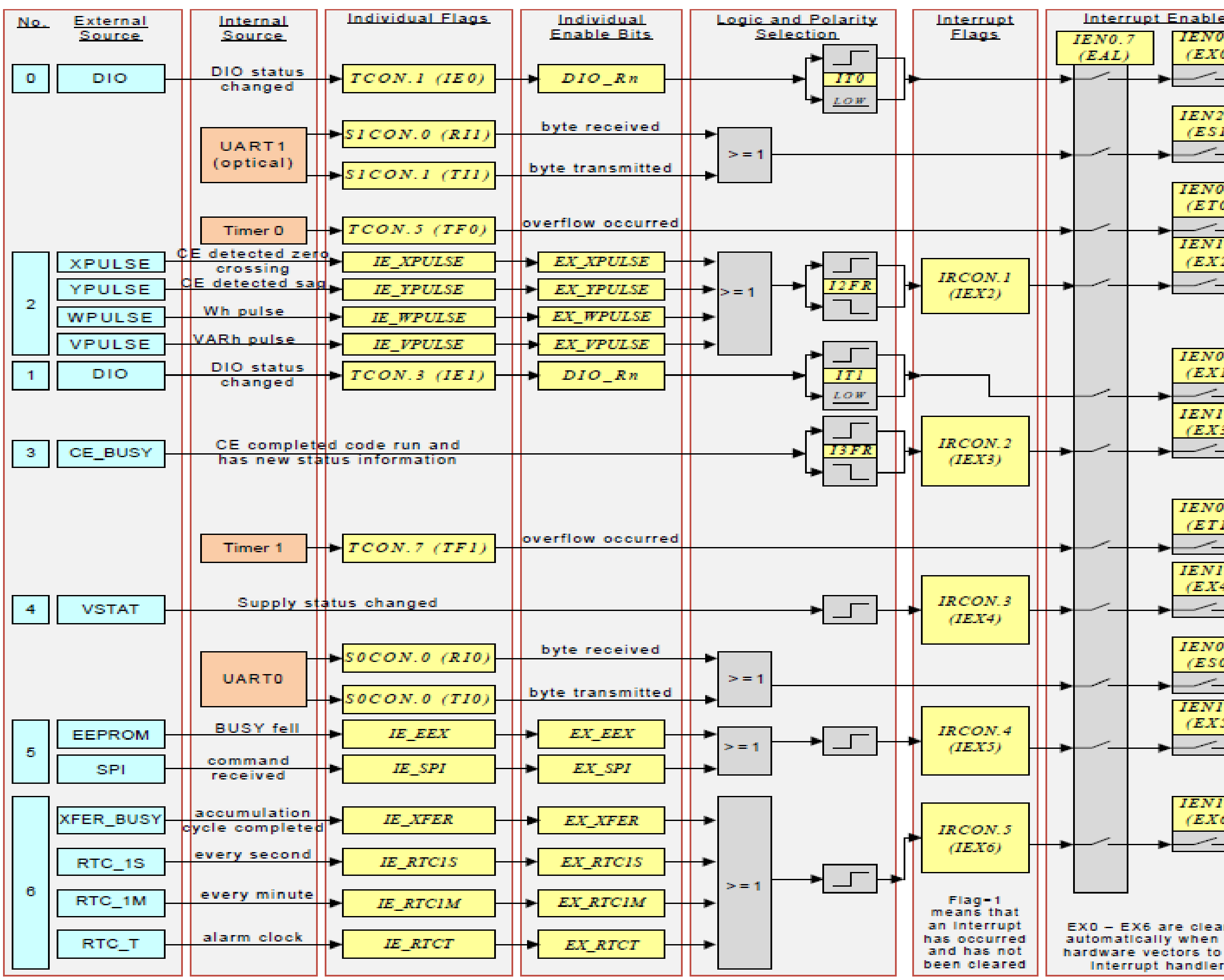


Figure 12: Interrupt Structure

2.5 On-Chip Resources

2.5.1 Physical Memory

2.5.1.1 Flash Memory

The device includes 64 KB (71M6543F) or 128 KB (71M6543G) of on-chip flash memory. The flash memory primarily contains MPU and CE program code. It also contains images of the CE RAM and I/O RAM. On power-up, before enabling the CE, the MPU copies these images to their respective locations.

Flash space allocated for the CE program is limited to 4096 16-bit words (8 KB). The CE program must begin on a 1-KB boundary of the flash address space. The *CE_LCTN[6/5:0]* (*I/O RAM 0x2109[5:0]*) field on the 71M6543F and the *CE_LCTN[6:0]* (*I/O RAM 0x2109[6:0]*) field on the 71M6543G define which 1-KB boundary contains the CE code. Thus, the first CE instruction is located at 1024**CE_LCTN[6/5:0]* on the 71M6543F and at 1024**CE_LCTN[6:0]* on the 71M6543G.

Flash memory can be accessed by the MPU, the CE, and by the SPI interface (R/W).

Table 38: Flash Memory Access

Access by	Access Type	Condition
MPU	R/W/E	W/E only if CE is disabled.
CE	R	
SPI	R/W/E	Access only when SFM is invoked (MPU halted).

<u>Flash Write Procedures</u>

If the *FLSH_UNLOCK[3:0] (I/O RAM 0x2702[7:4])* key is correctly programmed, the MPU may write to the flash memory. This is one of the non-volatile storage options available to the user in addition to external EEPROM.

The flash program write enable bit, *FLSH_PSTWR (SFR 0xB2[0]),* differentiates 80515 data store instructions (MOVX@DPTR,A) between Flash and XRAM writes. This bit is automatically cleared by hardware after each byte write operation. Write operations to this bit are inhibited when interrupts are enabled.

If the CE is enabled (*CE_E* = 1, *I/O RAM 0x2106[0]*), flash write operations must not be attempted unless *FLSH_PSTWR* is set. This bit enables the “posted flash write” capability. *FLSH_PSTWR* has no effect when *CE_E* = 0). When *CE_E* = 1, however, *FLSH_PSTWR* delays a flash write until the time interval between the CE code passes. During this delay time, the *FLSH_PEND* (*SFR 0xB2[3]*) bit is high, and the MPU continues to execute commands. When the CE code pass ends (CE_BUSY falls), the *FLSH_PEND* bit falls and the write operation occurs. The MPU can query the *FLSH_PEND* bit to determine when the write operation has been completed. While *FLSH_PEND* = 1, further flash write requests are ignored.

<u>Updating Individual Bytes in Flash Memory</u>

The original state of a flash byte is 0xFF (all bits are 1). Once a value other than 0xFF is written to a flash memory cell, overwriting with a different value usually requires that the cell be erased first. Since cells cannot be erased individually, the page has to be first copied to RAM, followed by a page erase. After this, the page can be updated in RAM and then written back to the flash memory.

<u>Flash Erase Procedures</u>

Flash erasure is initiated by writing a specific data pattern to specific SFR registers in the proper sequence. These special pattern/sequence requirements prevent inadvertent erasure of the flash memory.

The mass erase sequence is:

- Write 1 to the *FLSH_MEEN* bit (*SFR 0xB2[1]*).
- Write the pattern 0xAA to the *FLSH_ERASE* (*SFR 0x94*) register.

The mass erase cycle can only be initiated when the ICE port is enabled.

The page erase sequence is:

- Write the page address to *FLSH_PGADR[5:0]* (*SFR 0xB7[7:2]*).
- Write the pattern 0x55 to the *FLSH_ERASE* register (*SFR 0x94*).

Bank-Switching in the 71M6543G

The 128 KB program memory in the 71M6543G consists of a fixed lower bank of 32 KB, addressable at 0x0000 to 0x7FFF plus an upper banked area of 32 KB, addressable at 0x8000 to 0xFFFF. The I/O RAM register *FL_BANK[1:0] (SFR 0xB6[1:0])* is used to switch four memory banks of 32 KB each into the address range from 0x8000 to 0xFFFF. Note that when *FL_BANK[1:0] (SFR 0xB6[1:0])* = 0, the upper bank is the same as the lower bank.

Table 39: Bank Switching with *FL_BANK[1:0] (SFR 0xB6[1:0])*in the 71M6543G

71M6543G *FL_BANK[1:0]*	Address Range for Lower Bank (0x0000-0x7FFF)	Address Range for Upper Bank (0x8000-0xFFFF)
00	0x0000-0x7FFF	0x0000-0x7FFF
01	0x0000-0x7FFF	0x8000-0xFFFF
10	0x0000-0x7FFF	0x10000-0x17FFF
11	0x0000-0x7FFF	0x18000-0x1FFFF

In the 71M6543G, the address that the *FLSH_PGADR[6:0] (SFR 0xB7[7:1])* points to in the program address space can reference different flash memory locations, depending on the setting of the *FL_BANK[1:0] (SFR 0xB6[1:0])* bits. The *CE_LCTN[6:0]* (*I/O RAM 0x2109[6:0]*) field on the 71M6543G on the other hand, points directly to a location in the flash memory are not affected by the *FL_BANK[1:0] (SFR 0xB6[1:0])* bits

Program Security

When enabled, the security feature limits the ICE to global flash erase operations only. All other ICE operations, such as reading via the SPI or ICE port, are blocked. This guarantees the security of the user's MPU and CE program code. Security is enabled by MPU code that is executed in a 64 CKMPU cycle pre-boot interval before the primary boot sequence begins. Once security is enabled, the only way to disable it is to perform a global erase of the flash, followed by a chip reset.

The first 64 cycles of the MPU boot code are called the pre-boot phase because during this phase the ICE is inhibited. A read-only status bit, *PREBOOT (SFR 0xB2[7])*, identifies these cycles to the MPU. Upon completion of pre-boot, the ICE can be enabled and is permitted to take control of the MPU.

The security enable bit, *SECURE (SFR 0xB2[6]),* is reset whenever the chip is reset. Hardware associated with the bit allows only ones to be written to it. Thus, pre-boot code may set *SECURE* to enable the security feature but may not reset it. Once *SECURE* is set, the pre-boot and CE code are protected from erasure, and no external read of program code is possible.

Specifically, when the *SECURE* bit is set, the following applies:

- The ICE is limited to bulk flash erase only.
- Page zero of flash memory, the preferred location for the user's pre-boot code, may not be page-erased by either MPU or ICE. Page zero may only be erased with global flash erase.
- Write operations to page zero, whether by MPU or ICE are inhibited.

The 71M6543 also includes hardware to protect against unintentional Flash write and erase. To enable flash write and erase operations, a 4-bit hardware key that must be written to the *FLSH_UNLOCK[3:0]* field. The key is the binary number '0010'. If *FLSH_UNLOCK[3:0]* is not '0010', the Flash erase and write operation is inhibited by hardware. Proper operation of this security key requires that there be no firmware function that writes '0010' to *FLSH_UNLOCK[3:0]*. The key should be written by the external SPI master, in the case of SPI flash programming (SFM mode), or through the ICE interface in the case of ICE flash programming. When a boot loader is used, the key should be sent to the boot load code which then writes it to

FLSH_UNLOCK[3:0]. *FLSH_UNLOCK[3:0]* is not automatically reset. It should be cleared when the SPI or ICE has finished changing the Flash. Table 40 summarizes the I/O RAM registers used for flash security.

Table 40: Flash Security

Name	Location	Rst	Wk	Dir	Description
FLSH_UNLOCK[3:0]	2702[7:4]	0	0	R/W	Must be a 2 to enable any flash modification. See the description of Flash security for more details.
SECURE	SFR B2[6]	0	0	R/W	Inhibits erasure of page 0 and flash addresses above the beginning of CE code as defined by *CE_LCTN[6/5:0]* *(I/O RAM 0x2109[5:0])* on the 71M6543F and *CE_LCTN[6:0]* *I/O RAM 0x2109[6:0])* on the 71M6543G. Also inhibits the read of flash via the ICE and SPI ports.

SPI Flash Mode

In normal operation, the SPI slave interface cannot read or write the flash memory. However, the 71M6543 contains a Special Flash Mode (SFM) that facilitates initial (production) programming of the flash memory. When the 71M6543 is in SFM mode, the SPI interface can erase, read, and write the flash. Other memory elements such as XRAM and I/O RAM are not accessible to the SPI in this mode. In order to protect the flash contents, several operations are required before the SFM mode is successfully invoked.

When the 71M6543G is operating SFM, SPI single-byte transactions are used to write to *FL_BANK[1:0] (SFR 0xB6[1:0])*. During an SPI single-byte transaction, SPI_CMD[1:0] will over-write the contents of *FL_BANK[1:0] (SFR 0xB6[1:0])*. This will allow for access of the entire 128 KB flash memory while operating in SFM.

If the SPI port is used for code updates (in lieu of a programmer that uses the ICE port), then a code that disables the flash access via SPI can potentially lock out flash program updates.

Details on the SFM can be found in 2.5.12 SPI Slave Port.

2.5.1.2 MPU/CE RAM

The 71M6543 includes 5 KB of static RAM memory on-chip (XRAM) plus 256 bytes of internal RAM in the MPU core. The 5KB of static RAM are used for data storage by both MPU and CE and for the communication between MPU and CE.

2.5.1.3 I/O RAM (Configuration RAM)

The I/O RAM can be seen as a series of hardware registers that control basic hardware functions. I/O RAM address space starts at 0x2000. The registers of the I/O RAM are listed in Table 68.

The 71M6543 includes 128 bytes non-volatile RAM memory on-chip in the I/O RAM address space (addresses 0x2800 to 0x287F). This memory section is supported by the voltage applied at VBAT_RTC, and the data in it are preserved in BRN, LCD, and SLP modes as long as the voltage at VBAT_RTC is within specification.

2.5.2 Oscillator

The 71M6543 oscillator drives a standard 32.768 kHz watch crystal. This type of crystal is accurate and does not require a high-current oscillator circuit. The oscillator has been designed specifically to handle watch crystals and is compatible with their high impedance and limited power handling capability. The oscillator power dissipation is very low to maximize the lifetime of any battery attached to VBAT_RTC.

Oscillator calibration can improve the accuracy of both the RTC and metering. Refer to 2.5.4, Real-Time Clock (RTC) for more information.

The oscillator is powered from the V3P3SYS pin or from the VBAT_RTC pin, depending on the *V3OK* internal bit (i.e., *V3OK* = 1 if V3P3SYS ≥ 2.8 VDC and *V3OK* = 0 if V3P3SYS < 2.8 VDC). The oscillator requires approximately 100 nA, which is negligible compared to the internal leakage of a battery.

Although the oscillator may appear to work when VBAT is not connected, this mode of operation is not recommended.

If VBAT_RTC is connected to a drained battery or disconnected, a battery test that sets *TEMP_BAT* may drain the supply connected to VBAT_RTC and cause the oscillator to stop. A stopped oscillator may force the device to reset. Therefore, an unexpected reset during a battery test should be interpreted as a battery failure.

2.5.3 PLL and Internal Clocks

Timing for the device is derived from the 32.768 kHz crystal oscillator output that is multiplied by a PLL by 600 to obtain 19.660800 MHz, the master clock (MCK). All on-chip timing, except for the RTC clock, is derived from MCK. Table 41 provides a summary of the clock functions and their controls.

The two general-purpose counter/timers contained in the MPU are controlled by CKMPU (see 2.4.6 Timers and Counters).

The master clock can be boosted to 19.66 MHz by setting the *PLL_FAST* bit = 1 (*I/O RAM 0x2200[4]*) and can be reduced to 6.29 MHz by *PLL_FAST* = 0. The MPU clock frequency CKMPU is determined by another divider controlled by the I/O RAM control field *MPU_DIV[2:0] (I/O RAM 0x2200[2:0])* and can be set to MCK*$2^{-(MPU\_DIV+2)}$ where *MPU_DIV[2:0]* may vary from 0 to 4. When the ICE_E pin is high, the circuit also generates the 9.83 MHz clock for use by the emulator.

The PLL is only turned off in SLP mode or in LCD mode when *LCD_BSTE* is disabled. The *LCD_BSTE* value depends on the setting of the *LCD_VMODE [1:0]* field (see Table 51).

When the part is waking up from SLP or LCD modes, the PLL is turned on in 6.29 MHz mode, and the PLL frequency is not be accurate until the *PLL_OK* (*SFR 0xF9[4]*) flag rises. Due to potential overshoot, the MPU should not change the value of *PLL_FAST* until *PLL_OK* is true.

Table 41: Clock System Summary

Clock	Derived From	Fixed Frequency or Range			Function
		PLL_FAST=1	*PLL_FAST*=0	Controlled by	
OSC	Crystal	32.768 kHz		–	Crystal clock
MCK	Crystal/PLL	19.660800 MHz (600*CK32)	6.291456 MHz (192*CK32)	*PLL_FAST*	Master clock
CKCE	MCK	4.9152 MHz	1.5728 MHz	–	CE clock
CKADC	MCK	4.9152 MHz, 2.4576 MHz	1.572864 MHz, 0.786432 MHz	*ADC_DIV*	ADC clock
CKMPU	MCK	4.9152 MHz … 307.2 kHz	1.572864 MHz… 98.304 kHz	*MPU_DIV[2:0]*	MPU clock
CKICE	MCK	9.8304 MHz… 614.4 kHz	3.145728 MHz … 196.608 kHz	*MPU_DIV[2:0]*	ICE clock
CKOPTMOD	MCK	38.40 kHz	38.6 kHz	–	Optical UART Modulation
CK32	MCK	32.768 kHz		–	32 kHz clock

2.5.4 Real-Time Clock (RTC)

2.5.4.1 RTC General Description

The RTC is driven directly by the crystal oscillator and is powered by either the V3P3SYS pin or the VBAT_RTC pin, depending on the *V3OK* internal bit. The RTC consists of a counter chain and output registers. The counter chain consists of registers for seconds, minutes, hours, day of week, day of month, month, and year. The chain registers are supported by a shadow register that facilitates read and write operations.

Table 42 shows the I/O RAM registers for accessing the RTC.

2.5.4.2 Accessing the RTC

Two bits, *RTC_RD (I/O RAM 0x2890[6]*) and *RTC_WR (I/O RAM 0x2890[7])*, control the behavior of the shadow register.

When *RTC_RD* is low, the shadow register is updated by the RTC after each two milliseconds. When *RTC_RD* is high, this update is halted and the shadow register contents become stationary and are suitable to be read by the MPU. Thus, when the MPU wishes to read the RTC, it freezes the shadow register by setting the *RTC_RD* bit, reads the shadow register, and then lowers the *RTC_RD* bit to let updates to the shadow register resume. Since the RTC clock is only 500 Hz, there may be a delay of approximately 2 ms from when the *RTC_RD* bit is lowered until the shadow register receives its first update. Reads to *RTC_RD* continues to return a one until the first shadow update occurs.

When *RTC_WR* is high, the update of the shadow register is also inhibited. During this time, the MPU may overwrite the contents of the shadow register. When *RTC_WR* is lowered, the shadow register is written into the RTC counter on the next 500Hz RTC clock. A 'change' bit is included for each word in the shadow register to ensure that only programmed words are updated when the MPU writes a zero to *RTC_WR*. Reads of *RTC_WR* returns one until the counter has actually been updated by the register.

The sub-second register of the RTC, *RTC_SBSC (I/O RAM 0x2892)*, can be read by the MPU after the one second interrupt and before reaching the next one second boundary. *RTC_SBSC* contains the count since the last full second, in 1/128 second nominal clock periods, until the next one-second boundary. When the *RST_SUBSEC* bit is written, the *SUBSEC* counter is restarted, counting from 0 to 127. Reading and resetting the sub-second counter can be used as part of an algorithm to accurately set the RTC.

The RTC is capable of processing leap years. Each counter has its own output register. The RTC chain registers are not be affected by the reset pin, watchdog timer resets, or by transitions between the battery modes and mission mode.

Table 42: RTC Control Registers

Name	Location	Rst	Wk	Dir	Description
RTCA_ADJ[6:0]	2504[6:0]	40	--	R/W	Register for analog RTC frequency adjustment.
RTC_P[16:14] *RTC_P[13:6]* *RTC_P[5:0]*	289B[2:0] 289C[7:0] 289D[7:2]	4 0 0	4 0 0	R/W	Registers for digital RTC adjustment. 0x0FFBF ≤ *RTC_P* ≤ 0x10040
RTC_Q[1:0]	289D[1:0]	0	0	R/W	Register for digital RTC adjustment.
RTC_RD	2890[6]	0	0	R/W	Freezes the RTC shadow register so it is suitable for MPU reads. When *RTC_RD* is read, it returns the status of the shadow register: 0 = up to date, 1 = frozen. Writing 0 to RTC_RD bit to enable shadow register update, and writing 1 to RTC_RD to disable update
RTC_WR	2890[7]	0	0	R/W	Freezes the RTC shadow register so it is suitable for MPU write operations. When *RTC_WR* is cleared, the contents of the shadow register are written to the RTC counter on the next RTC clock (~1 kHz). When *RTC_WR* is read, it returns 1 as long as *RTC_WR* is set, and continues to return one until the RTC counter is updated. Writing 0 to RTC_WR bit to enable copying the shadow register contents to RTC counter, and writing 1 to RTC_WR to disable copying
RTC_FAIL	2890[4]	0	0	R/W	Indicates that a count error has occurred in the RTC and that the time is not trustworthy. This bit can be cleared by writing a 0.
RTC_SBSC[7:0]	2892[7:0]			R	Time remaining since the last 1 second boundary. LSB = 1/128 second.

2.5.4.3 RTC Rate Control

The 71M6543 has two rate adjustment mechanisms:

- The first rate adjustment mechanism is an analog rate adjustment, using the I/O RAM register *RTCA_ADJ[6:0],* that trims the crystal load capacitance.
- The second rate adjustment mechanism is a digital rate adjust that affects the way the clock frequency is processed in the RTC.

Setting *RTCA_ADJ[6:0]* to 00 minimizes the load capacitance, maximizing the oscillator frequency. Setting *RTCA_ADJ[6:0]* to 0x7F maximizes the load capacitance, minimizing the oscillator frequency. The adjustable capacitance is approximately:

$$C_{ADJ} = \frac{RTCA\_ADJ}{128} \cdot 16.5pF$$

The precise amount of adjustment depends on the crystal properties, the PCB layout and the value of the external crystal capacitors (see CXS and CXS in Table 87). The adjustment may occur at any time, and the resulting clock frequency should be measured over a one-second interval.

The second rate adjustment is digital, and can be used to adjust the clock rate up to ±988ppm, with a resolution of 3.8 ppm. The rate adjustment is implemented starting at the next second-boundary following the adjustment. Since the LSB (define first) results in an adjustment every four seconds, the frequency should be measured over an interval that is a multiple of four seconds.

The clock rate is adjusted by writing the appropriate values to *RTC_P[16:0]* (*I/O RAM 0x289B[2:0], 0x289C, 0x289D[7:2]*) and *RTC_Q[1:0] (I/O RAM 0x289D[1:0]).* Updates to RTC rate adjust registers, *RTC_P* and *RTC_Q*, are done through the shadow register described above. The new values are loaded into the counters when *RTC_WR (I/O RAM 0x2890[7]*) is lowered.

The default frequency is 32,768 RTCLK cycles per second. To shift the clock frequency by Δ ppm, *RTC_P* and *RTC_Q* are calculated using the following equation:

$$4 \cdot \mathrm{RTC\_P} + \mathrm{RTC\_Q} = floor\left(\frac{32768 \cdot 8}{1 + \Delta \cdot 10^{-6}} + 0.5\right)$$

Conversely, the amount of ppm shift for a given value of *4RTC_P*+*RTC_Q* is:

$$\Delta(ppm) = \left(\frac{32768 \cdot 8}{4 \cdot RTC_P + RTC_Q} - 1\right) \cdot 10^6$$

For example, for a shift of -988 ppm, 4 · *RTC_P* + *RTC_Q* = 262403 = 0x40103. *RTC_P[16:0]* = 0x10040, (*I/O RAM 0x289B[2:0], 0x289C, 0x289D[7:2]*) and *RTC_Q[1:0]* = 0x03 (*I/O RAM 0x289D[1:0]*. The default values of *RTC_P[16:0]* and *RTC_Q[1:0]*, corresponding to zero adjustment, are 0x10000 and 0x0, respectively.

Two settings for the TMUX2OUT test pin, PULSE_1S and PULSE_4S, are available for measuring and calibrating the RTC clock frequency. These are waveforms of approximately 25% duty cycle with 1s or 4s period.

✓ Default values for *RTCA_ADJ[6:0]*, *RTC_P[16:0]* and *RTC_Q[1:0]* should be nominal values, at the center of the adjustment range. Un-calibrated extreme values (zero, for example) can cause incorrect operation.

If the crystal temperature coefficient is known, the MPU can integrate temperature and correct the RTC time as necessary. Alternatively, the characteristics can be loaded into an NV RAM and the *OSC_COMP* (*I/O RAM 0x28A0[5*]) bit may be set. In this case, the oscillator is adjusted automatically, even in SLP mode. See 2.5.4.4 RTC Temperature Compensation for details.

2.5.4.4 RTC Temperature Compensation

The 71M6543 can be configured to regularly measure die temperature, including in SLP and LCD modes and while the MPU is halted. If enabled by *OSC_COMP*, this temperature information is automatically used to correct for the temperature variation of the crystal. A table lookup method is used.

Table 43 shows I/O RAM registers involved in automatic RTC temperature compensation.

Table 43: I/O RAM Registers for RTC Temperature Compensation

Name	Location	Rst	Wk	Dir	Description
OSC_COMP	28A0[5]	0	0	R/W	Enables the automatic update of *RTC_P[16:0]* and *RTC_Q[1:0]* every time the temperature is measured.
STEMP[10:3] *STEMP[2:0]*	2881[7:0] 2882[7:5]	–	–	R	The result of the temperature measurement (10-bits of magnitude data plus a sign bit).
LKPADDR[6:0]	2887[6:0]	0	0	R/W	The address for reading and writing the RTC lookup RAM.
LKPAUTOI	2887[7]	0	0	R/W	Auto-increment flag. When set, *LKPADDR[6:0]* auto increments every time *LKP_RD* or *LKP_WR* is pulsed. The incremented address can be read at *LKPADDR[6:0]*.
LKPDAT[7:0]	2888[7:0]	0	0	R/W	The data for reading and writing the RTC lookup RAM.
LKP_RD *LKP_WR*	2889[1] 2889[0]	0 0	0 0	R/W R/W	Strobe bits for the RTC lookup RAM read and write. When set, the *LKPADDR[6:0]* and *LKPDAT* registers are used in a read or write operation. When a strobe is set, it stays set until the operation completes, at which time the strobe is cleared and *LKPADDR[6:0]* is incremented if *LKPAUTOI* is set.

Referring to Figure 13 the table lookup method uses the 10-bits plus sign-bit value in *STEMP[10:0]* right-shifted by two bits to obtain an 8-bit plus sign value (i.e., NV RAM Address = *STEMP[10:0]*/4). A limiter ensures that the resulting look-up address is in the 6-bit plus sign range of -64 to +63 (decimal). The 8-bit NV RAM content pointed to by the address is added as a 2's complement value to 0x40000, the nominal value of 4**RTC_P[16:0]* + *RTC_Q[1:0]*.

Refer to 2.5.4.3 RTC Rate Control for information on the rate adjustments performed by registers *RTC_P[16:0]* and *RTC_Q[1:0]*. The 8-bit values loaded in to NV RAM must be scaled correctly to produce rate adjustments that are consistent with the equations given in 2.5.4.3 RTC Rate Control for *RTC_P[16:0]* and *RTC_Q[1:0]*. Note that the sum of the looked-up 8-bit 2's complement value and 0x40000 form a 19-bit value, which is equal to 4**RTC_P[16:0]* + *RTC_Q[1:0]*, as shown in Figure 13. The output of the Temperature Compensation is automatically loaded into the *RTC_P[16:0]* and *RTC_Q[1:0]* locations after each look-up and summation operation.

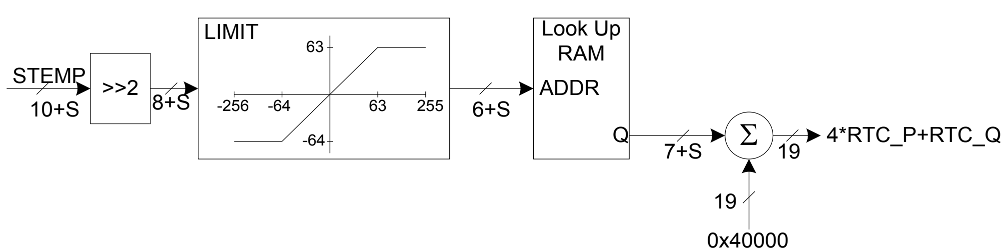


Figure 13: Automatic Temperature Compensation

The 128 NV RAM locations are organized in 2's complement format. As mentioned above, the *STEMP[10:0]* digital temperature values are scaled such that the corresponding NV RAM addresses are equal to *STEMP[10:0]*/4 (limited in the range of -64 to +63). See 2.5.5 71M6543 Temperature Sensor on page 53 for the equations to calculate temperature in degrees °C from the *STEMP[10:0]* reading.

For proper operation, the MPU has to load the lookup table with values that reflect the crystal properties with respect to temperature, which is typically done once during initialization. Since the lookup table is not directly addressable, the MPU uses the following procedure to load the NV RAM table:

1. Set the *LKPAUTOI* bit (*I/O RAM 0x2887[7]*) to enable address auto-increment.
2. Write zero into the I/O RAM register *LKPADDR[6:0]* (*I/O RAM 0x2887[6:0]*).
3. Write the 8-bit datum into I/O RAM register *LKPDAT* (*I/O RAM 0x2888*).
4. Set the *LKP_WR* bit (*I/O RAM 0x2889[0]*) to write the 8-bit datum into NV_RAM
5. Wait for *LKP_WR* to clear (*LKP_WR* auto-clears when the data has been copied to NV RAM).
6. Repeat steps 3 through 5 until all data has been written to NV RAM.

The NV RAM table can also be read by writing a 1 into the *LKP_RD* bit (*I/O RAM 0x2889[1]*). The process of reading from and writing to the NV RAM is accelerated by setting the *LKPAUTOI* bit (*I/O RAM 0x2887[7]*). When *LKPAUTOI* is set, *LKPADDR[6:0]* (*I/O RAM 0x2887[6:0]*) auto-increments every time *LKP_RD* or *LKP_WR* is pulsed. It is also possible to perform random access of the NV RAM by writing a 0 to the *LKPAUTOI* bit and loading the desired address into *LKPADDR[6:0]*.

If the oscillator temperature compensation feature is not being used, it is possible to use the NV RAM storage area as ordinary battery-backed NV storage space using the procedure described above to read and write NV RAM data. In this case, the *OSC_COMP* bit (*I/O RAM 0x28A0[5]*) is reset to disable the automatic oscillator temperature compensation feature.

2.5.4.5 RTC Interrupts

The RTC generates interrupts each second and each minute. These interrupts are called *RTC_1SEC* and *RTC_1MIN*. In addition, the RTC functions as an alarm clock by generating an interrupt when the minutes and hours registers both equal their respective target counts as defined in Table 44. The alarm clock interrupt is called *RTC_T*. All three interrupts appear in the MPU's external interrupt 6. See Table 32 in the interrupt section for the enable bits and flags for these interrupts.

The minute and hour target registers are listed in Table 44.

Table 44: I/O RAM Registers for RTC Interrupts

Name	Location	Rst	Wk	Dir	Description
RTC_TMIN[5:0]	289E[5:0]	0	0	R/W	The target minutes register. See below.
RTC_THR[4:0]	289F[4:0]	0	0	R/W	The target hours register. The *RTC_T* interrupt occurs when *RTC_MIN[5:0]* becomes equal to *RTC_TMIN[5:0]* and *RTC_HR[4:0]* becomes equal to *RTC_THR[4:0]*.

2.5.5 71M6543 Temperature Sensor

The 71M6543 includes an on-chip temperature sensor for determining the temperature of its bandgap reference. The primary use of the temperature data is to determine the magnitude of compensation required to offset the thermal drift in the system for the compensation of current, voltage and energy measurement and the RTC. See 4.5 Metrology Temperature Compensation on page 88. Also see 2.5.4.4 RTC Temperature Compensation on page 52.

Unlike earlier generation Maxim SoCs, the 71M6543 does not use the ADC to read the temperature sensor. Instead, it uses a technique that is operational in SLP and LCD mode, as well as BRN and MSN modes. This means that the temperature sensor can be used to compensate for the frequency variation of the crystal, even in SLP mode while the MPU is halted. See 2.5.4.4 RTC Temperature Compensation on page 52.

In MSN and BRN modes, the temperature sensor is awakened on command from the MPU by setting the *TEMP_START (I/O RAM 0x28B4[6])* control bit. In SLP and LCD modes, it is awakened at a regular rate set by *TEMP_PER[2:0] (I/O RAM 0x28A0[2:0])*.

The result of the temperature measurement is read from the two I/O RAM locations *STEMP[10:3]* (*I/O RAM 0x2881)* and *STEMP[2:0] (I/O RAM 0x2882[7:5])*. Note that both of these I/O RAM locations must be read and properly combined to form the *STEMP[10:0]* 11-bit value (see *STEMP* in Table 45). The resulting 11-bit value is in 2's complement form and ranges from -1024 to +1023 (decimal).

The equations below are used to calculate the sensed temperature. The first equation applies when the 71M6543F and 71M6543G are in MSN mode and *TEMP_PWR* = 1. The second equation applies when the 71M6543F and 71M6543G are in BRN mode, and in this case, the *TEMP_PWR* and *TEMP_BSEL* bits must both be set to the same value, so that the battery that supplies the temperature sensor is also the battery that is measured and reported in *BSENSE*. Thus, the second equation requires reading *STEMP* and *BSENSE*. In the second equation, *BSENSE* (the sensed battery voltage) is used to obtain a more accurate temperature reading when the IC is in BRN mode. The coefficients provided in the various *STEMP* equations below are typical.

For the 71M6543F and 71M6543G in MSN Mode (with *TEMP_PWR* = 1):

$$Temp(°C) = 0.325 \cdot STEMP + 22$$

For the 71M6543F and 71M6543G in BRN Mode, (with *TEMP_PWR*=*TEMP_BSEL*):

$$Temp(^{o}C) = 0.325 \cdot STEMP + 0.00218 \cdot BSENSE^2 - 0.609 \cdot BSENSE + 64.4$$

Table 45 shows the I/O RAM registers used for temperature and battery measurement.

If *TEMP_PWR* selects *VBAT_RTC* when the battery is nearly discharged, the temperature measurement may not finish. In this case, firmware may complete the measurement by selecting V3P3D (*TEMP_PWR* = 1).

Table 45: I/O RAM Registers for Temperature and Battery Measurement

<table>
<tr><th>Name</th><th>Location</th><th>Rst</th><th>Wk</th><th>Dir</th><th>Description</th></tr>
<tr><td>*TBYTE_BUSY*</td><td>28A0[3]</td><td>0</td><td>0</td><td>R</td><td>Indicates that hardware is still writing the 0x28A0 byte. Additional writes to this byte are locked out while it is one. Write duration could be as long as 6 ms.</td></tr>
<tr><td>*TEMP_PER[2:0]*</td><td>28A0[2:0]</td><td>0</td><td>–</td><td>R/W</td><td>Sets the period between temperature measurements. Automatic measurements can be enabled in any mode (MSN, BRN, LCD, or SLP).<table><tr><th>*TEMP_PER*</th><th>Time</th></tr><tr><td>0</td><td>Manual updates (see *TEMP_START*)</td></tr><tr><td>1-6</td><td>2 ^ (3+*TEMP_PER*) (seconds)</td></tr><tr><td>7</td><td>Continuous</td></tr></table></td></tr>
<tr><td>*TEMP_BAT*</td><td>28A0[4]</td><td>0</td><td>–</td><td>R/W</td><td>Causes VBAT to be measured whenever a temperature measurement is performed.</td></tr>
<tr><td>*TEMP_START*</td><td>28B4[6]</td><td>0</td><td>–</td><td>R/W</td><td>*TEMP_PER[2:0]* must be zero in order for *TEMP_START* to function. If *TEMP_PER[2:0]* = 0, then setting *TEMP_START* starts a temperature measurement. Ignored in SLP and LCD modes. Hardware clears *TEMP_START* when the temperature measurement is complete.</td></tr>
<tr><td>*TEMP_PWR*</td><td>28A0[6]</td><td>0</td><td>–</td><td>R/W</td><td>Selects the power source for the temperature sensor: 1 = V3P3D, 0 = VBAT_RTC. This bit is ignored in SLP and LCD modes, where the temperature sensor is always powered by VBAT_RTC.</td></tr>
<tr><td>*TEMP_BSEL*</td><td>28A0[7]</td><td>0</td><td>–</td><td>R/W</td><td>Selects which battery is monitored by the temperature sensor: 1 = VBAT, 0 = VBAT_RTC</td></tr>
<tr><td>*TEMP_TEST[1:0]*</td><td>2500[1:0]</td><td>0</td><td>–</td><td>R/W</td><td>Test bits for the temperature monitor VCO. *TEMP_TEST* must be 00 in regular operation. Any other value causes the VCO to run continuously with the control voltage described below.<table><tr><th>*TEMP_TEST*</th><th>Function</th></tr><tr><td>00</td><td>Normal operation</td></tr><tr><td>01</td><td>Reserved for factory test</td></tr><tr><td>1X</td><td>Reserved for factory test</td></tr></table></td></tr>
<tr><td>*STEMP[10:3]*
STEMP[2:0]</td><td>2881[7:0]
2882[7:5]</td><td></td><td></td><td>R
R</td><td>The result of the temperature measurement.
The STEMP[10:0] value may be obtained in C with a single 16-bit read and divide by 32 operation as follows:
volatile int16_t xdata STEMP _at_0x2881;
fa = (float)(STEMP/32);</td></tr>
<tr><td>*BSENSE[7:0]*</td><td>2885[7:0]</td><td>–</td><td>–</td><td>R</td><td>The result of the battery measurement.</td></tr>
<tr><td>*BCURR*</td><td>2704[3]</td><td>0</td><td>0</td><td>R/W</td><td>Connects a 100 μA load to the battery selected by *TEMP_BSEL*.</td></tr>
</table>

2.5.6 71M6xx3 Temperature Sensor

The 71M6xx3 includes an on-chip temperature sensor for determining the temperature of its bandgap reference. The primary use of the temperature data is to determine the magnitude of compensation required to offset the thermal drift in the system for the compensation of the current measurement performed by the71M6xx3. See the 71M6xxx Data Sheet for the equation to calculate temperature from the 71M6xx3 *STEMP[10:0]* reading. Also, see 4.5 Metrology Temperature Compensation on page 88.

See 2.2.8.3 Control of the 71M6xx3 Isolated Sensor on page 22 for information on how to read the *STEMP[10:0]* information from the 71M6xx3.

2.5.7 71M6543 Battery Monitor

The 71M6543 temperature measurement circuit can also monitor the batteries at the VBAT and VBAT_RTC pins. The battery to be tested (i.e., VBAT or VBAT_RTC pin) is selected by *TEMP_BSEL (I/O RAM 0x28A0[7])*.

When *TEMP_BAT* (*I/O RAM 0x28A0[4]*) is set, a battery measurement is performed as part of each temperature measurement. The value of the battery reading is stored in register *BSENSE[7:0] (I/O RAM 0x2885)*. The following equations are used to calculate the voltage measured on the VBAT pin (or VBAT_RTC pin) from the *BSENSE[7:0]* and *STEMP[10:0]* values. The result of the equation below is in volts. A slightly different equation is used for MSN mode and BRN mode, as follows.

In MSN mode, *TEMP_PWR* = 1 use:

$$VBAT(or VBAT\_RTC) = 3.3V + (BSENSE - 142) \cdot 0.0246V + STEMP \cdot 0.000297V$$

In BRN mode, *TEMP_PWR* = *TEMP_BSEL* use:

$$VBAT(or VBAT\_RTC) = 3.291V + (BSENSE - 142) \cdot 0.0255V + STEMP \cdot 0.000328V$$

In MSN mode, a 100 µA de-passivation load can be applied to the selected battery (i.e., selected by the *TEMP_BSEL* bit) by setting the *BCURR (I/O RAM 0x2704[3]*) bit. Battery impedance can be measured by taking a battery measurement with and without *BCURR*. Regardless of the *BCURR* bit setting, the battery load is never applied in BRN, LCD, and SLP modes.

2.5.8 71M6xx3 VCC Monitor

The 71M6xx3 monitors its VCC pin voltage. The voltage of the VCC pin can be obtained by the 71M6543 by issuing a read command to the 71M6xx3. The 71M6543 must request both the *VSENSE[7:0]* and *STEMP[10:0]* values from the 71M6xx3. See the 71M6xxx Data Sheet for the equation to calculate the 71M6xx3 VCC pin voltage from the *VSENSE[7:0]* and *STEMP[10:0]* values read from the 71M6xx3.

See 2.2.8.3 Control of the 71M6xx3 Isolated Sensor on page 22 for information on how to read *VSENSE[7:0]* and *STEMP[10:0]* from the 71M6xx3 remote sensors.

2.5.9 UART and Optical Interface

The 71M6543 provides two asynchronous interfaces, UART0 and UART1. Both can be used to connect to AMR modules, user interfaces, etc., and also support a mechanism for programming the on-chip flash memory.

Referring to Figure 14, UART1 includes an interface to implement an IR/optical port. The pin OPT_TX is designed to directly drive an external LED for transmitting data on an optical link. The pin OPT_RX has the same threshold as the RX pin, but can also be used to sense the input from an external photo detector used as the receiver for the optical link. OPT_TX and OPT_RX are connected to a dedicated UART port (UART1).

The OPT_TX and OPT_RX pins can be inverted with configuration bits *OPT_TXINV (I/O RAM 0x2456[0])* and *OPT_RXINV (I/O RAM 0x2457[1])*, respectively. Additionally, the OPT_TX output may be modulated at 38 kHz. Modulation is available in MSN and BRN modes (see Table 61). The *OPT_TXMOD* bit (*I/O RAM 0x2456[1]*) enables modulation. The duty cycle is controlled by *OPT_FDC[1:0] (I/O RAM 0x2457[5:4])* , which can select 50%, 25%, 12.5%, and 6.25% duty cycle. A 6.25% duty cycle means that OPT_TX is low for 6.25% of the period.

When not needed for UART1, OPT_TX can alternatively be configured as SEGDIO51. Configuration is via the *OPT_TXE[1:0] (I/O RAM 0x2456[3:2])* field and *LCD_MAP[51] (I/O RAM 0x2405[0])*. The *OPT_TXE[1:0]* field allows the MPU to select VPULSE, WPULSE, SEGDIO51 or the output of the pulse modulator to be sourced onto the OPT_TX pin. Likewise, the OPT_RX pin can alternately be configured as SEGDIO55, and its control is *OPT_RXDIS (I/O RAM 0x2457[2])* and *LCD_MAP[55] (I/O RAM 0x2405[4])*.

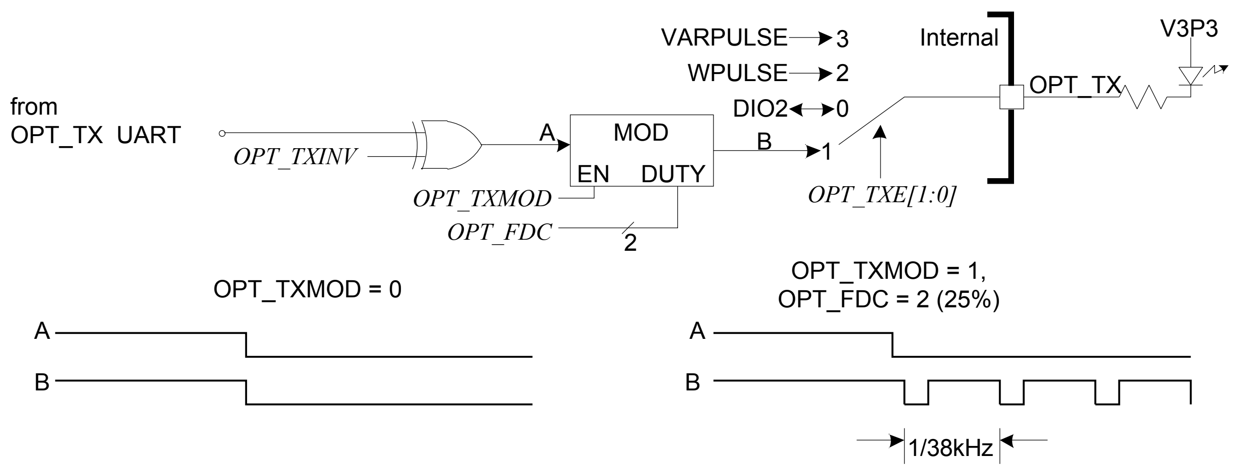


Figure 14: Optical Interface

Bit Banged Optical UART (Third UART)

As shown in Figure 15, the 71M6543 can also be configured to drive the optical UART with a DIO signal in a bit banged configuration. When control bit *OPT_BB* (*I/O RAM 0x2022[0]*) is set, the optical port is driven by DIO5 and the SEGDIO5 pin is driven by UART1_TX. This configuration is typically used when the two dedicated UARTs must be connected to high speed clients and a slower optical UART is permissible.

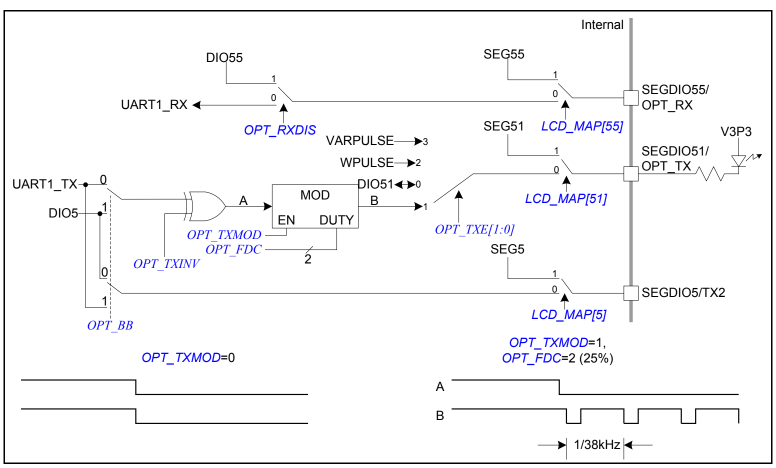


Figure 15: Optical Interface (UART1)

2.5.10 Digital I/O and LCD Segment Drivers

2.5.10.1 General Information

The 71M6543 combines most DIO pins with LCD segment drivers. Each SEG/DIO pin can be configured as a DIO pin or as a segment driver pin (SEG).

On reset or power-up, all DIO pins are DIO inputs (except for SEGDIO0-15, see caution note below) until they are configured as desired under MPU control. The pin function can be configured by the I/O RAM registers *LCD_MAPn (0x2405 – 0x240B)*. Setting the bit corresponding to the pin in *LCD_MAPn* to 1 configures the pin for LCD, setting *LCD_MAPn* to 0 configures it for DIO.

After reset or power up, pins SEGDIO0 through SEGDIO15 are initially DIO outputs, but are disabled by *PORT_E* = 0 *(I/O RAM 0x270C[5])* to avoid unwanted pulses during reset. After configuring pins SEGDIO0 through SEGDIO15 the MPU must enable these pins by setting *PORT_E*.

Once a pin is configured as DIO, it can be configured independently as an input or output. For SEGDIO0 to SEGDIO15, this is done with the SFR registers *P0 (SFR 0x80), P1 (SFR 0x90)*, *P2 (SFR 0xA0)* and *P3 (SFR 0xB0)*, as shown in Table 47.

Example: SEGDIO12 (pin 32 in Table 47) is configured as a DIO output pin with a value of 1 (high) by writing 0 to bit 4 of *LCD_MAP[15:8]*, and writing 1 to both *P3[4]and P3[0]*. The same pin is configured as an LCD driver by writing 1 to bit 4 of *LCD_MAP[15:8]*. The display information is written to bits 0 to 5 of *LCD_SEG12.*

The PB pin is a dedicated digital input and is not part of the SEGDIO system.

The CE features pulse counting registers and each pulse counter interrupt output is internally routed to the pulse interrupt logic. Thus, no routing of pulse signals to external pins is required in order to generate pulse interrupts. See interrupt source No. 2 in Figure 12.

A 3-bit configuration word, I/O RAM register *DIO_Rn* (*I/O RAM 0x2009[2:0]* through *0x200E[6:4]*) can be used for pins SEGDIO2 through SEGDIO11 (when configured as DIO) and PB to individually assign an internal resource such as an interrupt or a timer control (*DIO_RPB[2:0], I/O RAM 0x2450[2:0],* configures the PB pin). This way, DIO pins can be tracked even if they are configured as outputs. Table 47 lists the internal resources which can be assigned using *DIO_R2[2:0]* through *DIO_R11[2:0]* and *DIO_RPB[2:0]*. If more than one input is connected to the same resource, the resources are combined using a logical OR.

Table 46: Selectable Resources using the *DIO_Rn[2:0]* Bits

Value in *DIO_Rn[2:0]*	Resource Selected for SEGDIOn or PB Pin
0	None
1	Reserved
2	T0 (counter0 clock)
3	T1 (counter1 clock)
4	High priority I/O interrupt (INT0)
5	Low priority I/O interrupt (INT1)
Note: Resources are selectable only on SEGDIO2 through SEGDIO11 and the PB pin. See Table 48.	

When driving LEDs, relay coils etc., the DIO pins should sink the current into GNDD (as shown in Figure 16, right), not source it from V3P3D (as shown in Figure 16, left). This is due to the resistance of the internal switch that connects V3P3D to either V3P3SYS or VBAT. See 6.4.6 V3P3D Switch on page 136.

Sourcing current in or out of DIO pins other than those dedicated for wake functions, for example with pullup or pulldown resistors, must be avoided. Violating this rule leads to increased quiescent current in sleep and LCD modes.

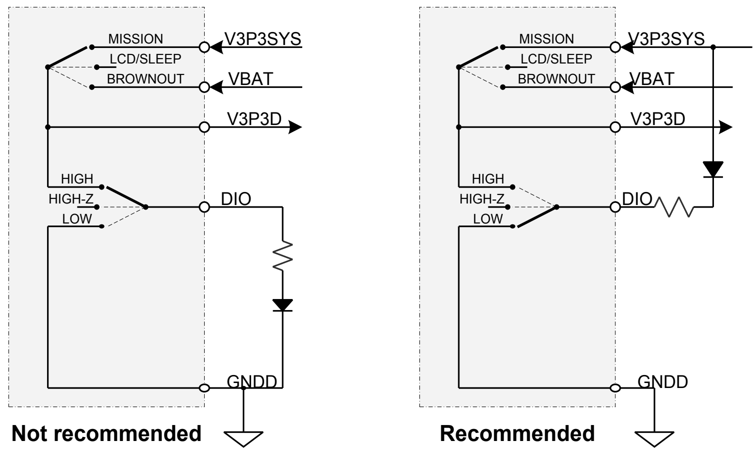


Figure 16: Connecting an External Load to DIO Pins

2.5.10.2 Combined DIO and SEG Pins

A total of 51 combined DIO/LCD pins are available. These pins can be categorized as follows:

39 combined DIO/LCD segment pins:

- SEGDIO4…SEGDIO25 (22 pins)
- SEGDIO28…SEGDIO35 (8 pins)
- SEGDIO40…SEGDIO45 (6 pins)
- SEGDIO52…SEGDIO54 (3 pins)

12 combined DIO/LCD segment pins shared with other functions:

- SEGDIO0/WPULSE, SEGDIO1/VPULSE (2 pins)
- SEGDIO2/SDCK, SEGDIO3/SDATA (2 pins)
- SEGDIO26/COM5, SEGDIO27/COM4 (2 pins)
- SEGDIO36/SPI_CSZ…SEGDIO39/SPI_CKI (4 pins)
- SEGDIO51/OPT_TX, SEGDIO55/OPT_RX (2 pins)

Additionally, 5 LCD segment (SEG) pins are available. These pins can be categorized as follows:

- 3 SEG pins combined with the ICE interface (SEG48/E_RXTX, SEG49/E_TCLK, SEG50/E_RST)
- 2 SEG pins combined with the test multiplexer outputs (SEG46/TMUX2OUT, SEG47/TMUXOUT)

Thus, a total of 51 DIO pins are available with minimum LCD configuration, and a total of 56 LCD pins are available with minimum DIO configuration.

Table 47: Data/Direction Registers and Internal Resources for SEGDIO0 to SEGDIO15

SEGDIO	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Pin #	**45**	**44**	**43**	**42**	**41**	**39**	**38**	**37**	**36**	**35**	**34**	**33**	**32**	**31**	**30**	**29**
Configuration: 0 = DIO, 1 = LCD	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
	LCD_MAP[7:0] *(I/O RAM 0x240B)*								***LCD_MAP[15:8]*** *(I/O RAM 0x240A)*							
SEG Data Register	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	LCD_SEG0[5:0] to ***LCD_SEG15[5:0]*** *(I/O RAM 0x2410[5:0]* to *0x241F[5:0]*															
DIO Data Register	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
	P0 *(SFR80)*				***P1*** *(SFR 0x90)*				***P2*** *(SFR 0xA0)*				***P3*** *(SFR 0xB0)*			
Direction Register: 0 = input, 1 = output	4	5	6	7	4	5	6	7	4	5	6	7	4	5	6	7
	P0 *(SFR 0x80)*				***P1*** *(SFR 0x90)*				***P2*** *(SFR 0xA0)*				***P3*** *(SFR 0xB0)*			
Internal Resources Configurable (see Table 46)	–	–	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	–	–	–

The configuration for pins SEGDIO16 to SEGDIO31 is shown in Table 48, and the configuration for pins SEGDIO32 to SEGDIO45 is shown in Table 49. The configuration for pins SEGDIO51 to SEGDIO55 is shown in Table 50.

Table 48: Data/Direction Registers for SEGDIO16 to SEGDIO31

SEGDIO	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Pin #	**28**	**27**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**11**	**10**	**9**	**8**
Configuration: 0 = DIO, 1 = LCD	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
	LCD_MAP[23:16] *(I/O RAM 0x2409)*								***LCD_MAP[31:24]*** *(I/O RAM 0x2408)*							
SEG Data Register	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	LCD_SEGDIO16[5:0] to ***LCD_SEGDIO31[5:0]*** *(I/O RAM 0x2420[5:0]* to *0x242F[5:0])*															
DIO Data Register	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	LCD_SEGDIO16[0] to ***LCD_SEGDIO31[0]*** *(I/O RAM 0x2420[0]* to *0x242F[0])*															
Direction Register: 0 = input, 1 = output	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	LCD_SEGDIO16[1] to ***LCD_SEGDIO31[1]*** *(I/O RAM 0x2420[1]* to *0x242F[1])*															

Table 49: Data/Direction Registers for SEGDIO32 to SEGDIO45

SEGDIO	32	33	34	35	36	37	38	39	40	41	42	43	44	45
Pin #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**100**	**99**	**98**	**97**	**96**	**95**	**94**
Configuration: 0 = DIO, 1 = LCD	0	1	2	3	4	5	6	7	0	1	2	3	4	5
	LCD_MAP[39:32] *(I/O RAM 0x2407)*								***LCD_MAP[45:40]*** *(I/O RAM 0x2406[5:0])*					
SEG Data Register	32	33	34	35	36	37	38	39	40	41	42	43	44	45
	LCD_SEGDIO32[5:0] to ***LCD_SEGDIO45[5:0]*** *(I/O RAM 0x2430[5:0] to 0x243D[5:0])*													
DIO Data Register	32	33	34	35	36	37	38	39	40	41	42	43	44	45
	LCD_SEGDIO32[0] to ***LCD_SEGDIO45[0]*** *(I/O RAM 0x2430[0] to 0x243D[0])*													
Direction Register: 0 = input, 1 = output	32	33	34	35	36	37	38	39	40	41	42	43	44	45
	LCD_SEGDIO32[1] to ***LCD_SEGDIO45[1]*** *(I/O RAM 0x2430[1] to 0x243D[1])*													

Table 50: Data/Direction Registers for SEGDIO51 to SEGDIO55

SEGDIO	**51**	**52**	**53**	**54**	**55**			
Pin #	**53**	**52**	**51**	**47**	**46**	**–**	**–**	**–**
Configuration: 0 = DIO, 1 = LCD	3	4	5	6	7	–	–	–
	LCD_MAP[55:48] *(I/O RAM 0x2405)*							
SEG Data Register	51	52	53	54	55	–	–	–
	LCD_SEGDIO51[5:0] to ***LCD_SEGDIO55[5:0]*** *(I/O RAM 0x2443[5:0] to 0x2447[5:0])*							
DIO Data Register	51	52	53	54	55	–	–	–
	LCD_SEGDIO51[0] to ***LCD_SEGDIO55[0]*** *(I/O RAM 0x2443[0] to 0x2447[0])*							
Direction Register: 0 = input, 1 = output	51	52	53	54	55	–	–	–
	LCD_SEGDIO51[1] to ***LCD_SEGDIO55[1]*** *(I/O RAM 0x2443[1] to 0x2447[1])*							

2.5.10.3 LCD Drivers

The LCD drivers are grouped into up to six commons (COM0 – COM5) and up to 56 segment drivers. The LCD interface is flexible and can drive 7-segment digits, 14-segment digits or enunciator symbols.

A voltage doubler and a contrast DAC generate VLCD from either VBAT or V3P3SYS, depending on the V3P3SYS voltage. The voltage doubler, while capable of driving into a 500 kΩ load, is able to generate a maximum LCD voltage that is within 1 V of twice the supply voltage. The doubler and DAC operate from a trimmed low-power reference.

The configuration of the VLCD generation is controlled by the I/O RAM field *LCD_VMODE[1:0] (I/O RAM 0x2401[7:6])*. It is decoded into *LCD_EXT, LDAC_E,* and *LCD_BSTE*. Table 51 details the *LCD_VMODE[1:0]* configurations.

Table 51: *LCD_VMODE* Configurations

LCD_VMODE[1:0]	***LCD_EXT***	***LDAC_E***	***LCD_BSTE***	**Description**
11	1	0	0	External VLCD connected to the VLCD pin.
10	0	1	1	LCD boost is enabled. Maximum VLCD voltage is 2*V3P3L-1. VLCD = max(2*V3P3L-1, 2.65(1+*LCD_DAC[4:0]*/31)
01	0	1	0	LCD boost is disabled. The maximum VLCD voltage is V3P3L. VLCD = max(V3P3L, 2.65(1+*LCD_DAC[4:0]*/31)
00	0	0	0	VLCD=V3P3L, the LCD DAC and LCD boost are disabled. In LCD mode, this setting causes the lowest battery current.

Notes:

1. LCD_EXT, LDAC_E and LCD_BSTE are 71M6543 internal signals which are decoded from the *LCD_VMODE[1:0]* control field setting (*I/O RAM 0x2401[7:6]*). Each of these decoded signals, when asserted, has the effect indicated in the description column above, and as summarized below.
   LCD_EXT : When set, the VLCD pin expects an external supply voltage
   LDAC_E : When set, LCD DAC is enabled
   LCD_BSTE : When set, the LCD boost circuit is enabled
2. V3P3L is an internal supply rail that is supplied from either the VBAT pin or the V3P3SYS pin, depending on the V3P3SYS pin voltage. When the V3P3SYS pin drops below 3.0 VDC, the 71M6543 switches to BRN mode and V3P3L is sourced from the VBAT pin, otherwise V3P3L is sourced from the V3P3SYS pin while in MSN mode.

When using the VLCD boost circuit, use care when setting the *LCD_DAC[4:0] (I/O RAM 0x240D[4:0])* value to ensure that the LCD manufacturer's recommended operating voltage specification is not exceeded.

The voltage doubler is active in all LCD modes including the LCD mode when *LCD_BSTE* = 1. Current dissipation in LCD mode can be reduced if the boost circuit is disabled and the LCD system is operated directly from VBAT.

The LCD DAC uses a low-power reference and, within the constraints of VBAT and the voltage doubler, generates a VLCD voltage of 2.65 VDC + 2.65 * *LCD_DAC[4:0]*/31. Two fuse bytes increase the accuracy of the LCD_DAC. LCDADJ12 and LCDADJ0 indicate the actual VLCD output voltage when the DAC is programmed to 12 and 0 respectively.

The *LCD_BAT (I/O RAM 0x2402[7])* bit causes the LCD system to use the battery voltage in all power modes. This may be useful when an external supply is available for the LCD system. The advantage of connecting the external supply to VBAT, rather than VLCD is that the LCD DAC is still active.

If *LCD_EXT* = 1, the VLCD pin must be driven from an external source. In this case, the LCD DAC has no effect.

The LCD system has the ability to drive up to six segments per SEG driver. If the display is configured with six back planes, the 6-way multiplexing reduces the number of SEG pins required to drive a display and therefore enhances the number of DIO pins available to the application. Refer to the *LCD_MODE[2:0]* field *(I/O RAM 0x2400[6:4])* settings (Table 52) for the different LCD multiplexing choices. If 5-state multiplexing is selected, SEGDIO27 is converted to COM4. If 6-state multiplexing is selected, SEGDIO26 is converted to COM5. These conversions override the SEG/DIO mapping of SEGDIO26 and SEGDIO27. Additionally, independent of *LCD_MODE[2:0],* if *LCD_ALLCOM* = 1 (*I/O RAM 0x2400[3])*, then SEGDIO26 and SEGDIO27 become COM4 and COM5 if their *LCD_MAP[ ]* bits are set.

The *LCD_ON* (*I/O RAM 0x240C[0]*) and *LCD_BLANK* (*I/O RAM 0x240C[1]*) bits are an easy way to either blank the LCD display or turn it fully on. Neither bit affects the contents of the LCD data stored in the *LCDSEG_DIO[ ]* registers. In comparison, *LCD_RST* (*I/O RAM 0x240C[2]*) clears all LCD data to zero. *LCD_RST* affects only pins that are configured as LCD.

A small amount of power can be saved by programming the LCD frequency to the lowest value that provides satisfactory LCD visibility over the required temperature range.

Table 52 shows all I/O RAM registers that control the operation of the LCD interface.

Table 52: LCD Configurations

<table>
<tr><th>Name</th><th>Location</th><th>Rst</th><th>Wk</th><th>Dir</th><th>Description</th></tr>
<tr><td>LCD_ALLCOM</td><td>2400[3]</td><td>0</td><td>–</td><td>R/W</td><td>Configures all 6 SEG/COM pins as COM. Has no effect on pins whose LCD_MAP bit is zero.</td></tr>
<tr><td>LCD_BAT</td><td>2402[7]</td><td>0</td><td>–</td><td>R/W</td><td>Connects the LCD power supply to VBAT in all modes.</td></tr>
<tr><td>LCD_E</td><td>2400[7]</td><td>0</td><td>–</td><td>R/W</td><td>Enables the LCD display. When disabled, VLC2, VLC1, and VLC0 are ground as are the COM and SEG outputs if their LCD_MAP bit is 1.</td></tr>
<tr><td>LCD_ON
LCD_BLANK</td><td>240C[0]
240C[1]</td><td>0
0</td><td>–
–</td><td>R/W
R/W</td><td>LCD_ON = 1 turns on all LCD segments without affecting the LCD data. Similarly, LCD_BLANK = 1 turns off all LCD segments without affecting the LCD data. If both bits are set, all LCD segments are turned on.</td></tr>
<tr><td>LCD_RST</td><td>240C[2]</td><td>0</td><td>–</td><td>R/W</td><td>Clear all bits of LCD data. These bits affect SEGDIO pins that are configured as LCD drivers.</td></tr>
<tr><td>LCD_DAC[4:0]</td><td>240D[4:0]</td><td>0</td><td>–</td><td>R/W</td><td>This register controls the LCD contrast DAC which adjusts the VLCD voltage and has an output range of 2.65 VDC to 5.3 VDC. The VLCD voltage is
VLCD = 2.65 + 2.65 * LCD_DAC[4:0]/31
Thus, the LSB of the DAC is 85.5 mV. The maximum DAC output voltage is limited by V3P3SYS, VBAT, and whether LCD_BSTE is set.</td></tr>
<tr><td>LCD_CLK[1:0]</td><td>2400[1:0]</td><td>0</td><td>–</td><td>R/W</td><td>Sets the LCD clock frequency (1/T). See definition of T in Figure 17. Note: fw = 32768 Hz
00-fw/2^9, 01-fw/2^8, 10-fw/2^7, 11-fw/2^6</td></tr>
<tr><td>LCD_MODE[2:0]</td><td>2400[6:4]</td><td>0</td><td>–</td><td>R/W</td><td>The LCD bias and multiplex mode.
<table>
<tr><th>LCD_MODE</th><th>Output</th></tr>
<tr><td>000</td><td>4 states, 1/3 bias</td></tr>
<tr><td>001</td><td>3 states, 1/3 bias</td></tr>
<tr><td>010</td><td>2 states, ½ bias</td></tr>
<tr><td>011</td><td>3 states, ½ bias</td></tr>
<tr><td>100</td><td>Static display</td></tr>
<tr><td>101</td><td>5 states, 1/3 bias</td></tr>
<tr><td>110</td><td>6 states, 1/3 bias</td></tr>
</table></td></tr>
<tr><td>LCD_VMODE[1:0]</td><td>2401[7:6]</td><td>00</td><td>00</td><td>R/W</td><td>This register specifies how VLCD is generated.
<table>
<tr><th>LCD_VMODE</th><th>Description</th></tr>
<tr><td>11</td><td>External VLCD</td></tr>
<tr><td>10</td><td>LCD boost and LCD DAC enabled</td></tr>
<tr><td>01</td><td>LCD DAC enabled</td></tr>
<tr><td>00</td><td>No boost and no DAC.
VLCD = VBAT or V3P3SYS</td></tr>
</table></td></tr>
</table>

The LCD can be driven in static, ½ bias, and 1/3 bias modes. Figure 17 defines the COM waveforms. Note that COM pins that are not required in a specific mode maintain a segment off state rather than GND, VCC, or high impedance.

The segment drivers SEGDIO22 and SEGDIO23 can be configured to blink at either 0.5 Hz or 1 Hz. The blink rate is controlled by *LCD_Y (I/O RAM 0x2400[2])*. There can be up to six pixels/segments connected to each of these driver pins. The I/O RAM fields *LCD_BLKMAP22[5:0] (I/O RAM 0x2402[5:0])* and *LCD_BLKMAP23[5:0] (I/O RAM 0x2401[5:0])* identify which pixels, if any, are to blink. *LCD_BLKMAP22[5:0] and LCD_BLKMAP23[5:0]* are non-volatile.

The LCD bias may be compensated for temperature using the *LCD_DAC[4:0]* field (*I/O RAM 0x240D[4:0]*). The bias may be adjusted from 1.4 V below the 3.3 V supply (V3P3SYS in MSN mode and VBAT in BRN and LCD modes). When the *LCD_DAC[4:0]* field is set to 000, the DAC is bypassed and powered down. This setting can be used to reduce current in LCD mode.

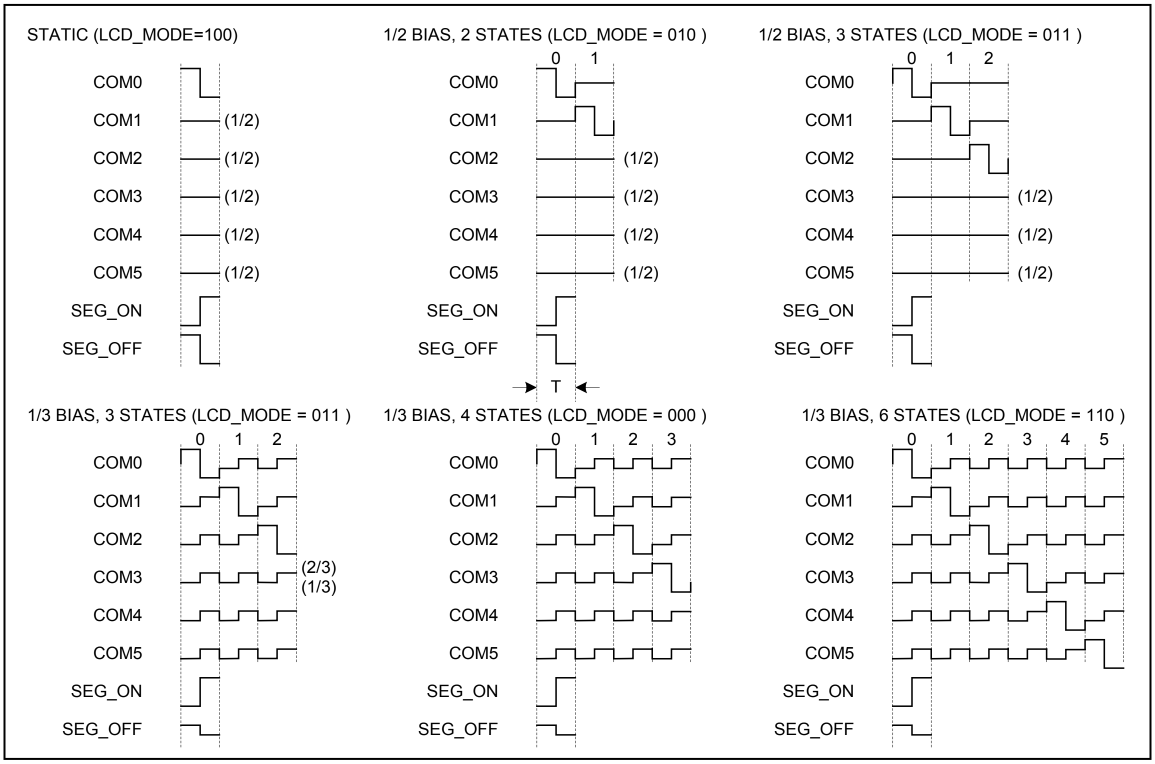


Figure 17: LCD Waveforms

SEG46 through SEG50 cannot be configured as DIO pins. Display data for these pins are written to I/O RAM registers *LCD_SEG46[5:0]* through *LCD_SEG50[5:0]* (see Table 53).

Table 53: LCD Data Registers for SEGDIO46 to SEGDIO55

SEGDIO	46	47	48	49	50	51	52	53	54	55
Pin #	93	92	58	57	56	53	52	51	47	46
Configuration:	Always LCD pins					See 2.5.10.2				
SEG Data Register	***LCD_SEGDIO46[5:0]*** *(I/O RAM 0x243E[5:0]*	***LCD_SEGDIO47[5:0]*** *(I/O RAM 0x243F[5:0])*	***LCD_SEGDIO48[5:0]*** *(I/O RAM 0x2440[5:0]*	***LCD_SEGDIO49[5:0]*** *(I/O RAM 0x2441[5:0])*	***LCD_SEGDIO50[5:0]*** *(I/O RAM 0x2442[5:0])*	***LCD_SEGDIO51[5:0]*** *(I/O RAM 0x2443[5:0])*	***LCD_SEGDIO52[5:0]*** *(I/O RAM 0x2444[5:0])*	***LCD_SEGDIO53[5:0]*** *(I/O RAM 0x2445[5:0])*	***LCD_SEGDIO54[5:0]*** *(I/O RAM 0x2446[5:0])*	***LCD_SEGDIO55[5:0]*** *(I/O RAM 0x2447[5:0])*

The *LCD_MAP[47:46]* (*I/O RAM 0x2406[7:6]*) bits are used to determine whether SEG46 and SEG47 are SEG pins or their alternate function (see pins 93 and 92 in Figure 42). If the *LCD_MAP[47:46]* bits are 1, then the pins are configured as SEG pins. If the *LCD_MAP[47:46]* bits are 0, then the pins are configured as their alternate functions (TMUX2OUT and TMUXOUT, respectively).

For example, if *LCD_MAP[46]* = 1, then pin 93 (TMUX2OUT/SEG46) is configured as SEG46, and if *LCD_MAP[46]=0*, then pin 93 is configured as TMUX2OUT.

The SEG pins with alternate ICE interface function (see pins 56-58 in Figure 42) are forced to their alternate ICE interface function (i.e., E_RXTX, E_TCLK and E_RST) if the ICE_E pin (pin 59) is driven high, and in this case, the bits *LCD_MAP[50:48]* (*I/O RAM 0x2405[2:0]*) bits are "don't care" bits. If the ICE_E pin is driven low, then *LCD_MAP[50:48]* bits ***must*** written with 1 in order to configure these pins as SEG pins. If the ICE_E pin is low and *LCD_MAP[50:48]* are written with 0, then these pins are tied to an internal pullup.

2.5.11 EEPROM Interface

The 71M6543 provides hardware support for either a two-pin or a three-wire (µ-wire) type of EEPROM interface. The interfaces use the *EECTRL (SFR 0x9F)* and *EEDATA (SFR 0x9E)* registers for communication.

2.5.11.1 Two-pin EEPROM Interface

The dedicated 2-pin serial interface communicates with external EEPROM devices. The interface is multiplexed onto the SEGDIO2 (SDCK) and SEGDIO3 (SDATA) pins and is selected by setting *DIO_EEX[1:0]* = 01 (*I/O RAM 0x2456[7:6]*). The MPU communicates with the interface through the SFR registers *EEDATA* and *EECTRL*. If the MPU wishes to write a byte of data to the EEPROM, it places the data in *EEDATA* and then writes the Transmit code to *EECTRL*. This initiates the transmit operation which is finished when the *BUSY* bit falls. INT5 is also asserted when *BUSY* falls. The MPU can then check the *RX_ACK* bit to see if the EEPROM acknowledged the transmission.

A byte is read by writing the Receive command to *EECTRL* and waiting for the *BUSY* bit to fall. Upon completion, the received data is in *EEDATA*. The serial transmit and receive clock is 78 kHz during each transmission, and then holds in a high state until the next transmission. The *EECTRL* bits when the two-pin interface is selected are shown in Table 54.

Table 54: *EECTRL* Bits for 2-pin Interface

<table>
<tr><th>Status Bit</th><th>Name</th><th>Read/ Write</th><th>Reset State</th><th>Polarity</th><th colspan="2">Description</th></tr>
<tr><td>7</td><td>ERROR</td><td>R</td><td>0</td><td>Positive</td><td colspan="2">1 when an illegal command is received.</td></tr>
<tr><td>6</td><td>BUSY</td><td>R</td><td>0</td><td>Positive</td><td colspan="2">1 when serial data bus is busy.</td></tr>
<tr><td>5</td><td>RX_ACK</td><td>R</td><td>1</td><td>Positive</td><td colspan="2">1 indicates that the EEPROM sent an ACK bit.</td></tr>
<tr><td>4</td><td>TX_ACK</td><td>R</td><td>1</td><td>Positive</td><td colspan="2">1 indicates when an ACK bit has been sent to the EEPROM.</td></tr>
<tr><td rowspan="8">3:0</td><td rowspan="8">CMD[3:0]</td><td rowspan="8">W</td><td rowspan="8">0000</td><td rowspan="8">Positive</td><td>CMD[3:0]</td><td>Operation</td></tr>
<tr><td>0000</td><td>No-op command. Stops the I^2C clock (SDCK). If not issued, SDCK keeps toggling.</td></tr>
<tr><td>0010</td><td>Receive a byte from the EEPROM and send ACK.</td></tr>
<tr><td>0011</td><td>Transmit a byte to the EEPROM.</td></tr>
<tr><td>0101</td><td>Issue a STOP sequence.</td></tr>
<tr><td>0110</td><td>Receive the last byte from the EEPROM and do not send ACK.</td></tr>
<tr><td>1001</td><td>Issue a START sequence.</td></tr>
<tr><td>Others</td><td>No operation, set the ERROR bit.</td></tr>
</table>

The EEPROM interface can also be operated by controlling the DIO2 and DIO3 pins directly. The direction of the DIO line can be changed from input to output and an output value can be written with a single write operation, thus avoiding collisions (see Table 14 Port Registers (SEGDIO0-15)). Therefore, no resistor is required in series SDATA to protect against collisions.

2.5.11.2 Three-Wire (µ-Wire) EEPROM Interface with Single Data Pin

A 500 kHz three-wire interface, using SDATA, SDCK, and a DIO pin for CS is available. The interface is selected by setting *DIO_EEX[1:0]* = 10. The *EECTRL* bits when the three-wire interface is selected are shown in Table 55. When *EECTRL* is written, up to 8 bits from *EEDATA* are either written to the EEPROM or read from the EEPROM, depending on the values of the *EECTRL* bits.

2.5.11.3 Three-Wire (µ-Wire/SPI) EEPROM Interface with Separate Di/DO Pins

If *DIO_EEX[1:0] =* 11, the 71M6543 three-wire interface is the same as above, except DI and DO are separate pins. In this case, SEGDIO3 becomes DO and SEGDIO8 becomes DI. The timing diagrams are the same as for *DIO_EEX[1:0] =* 10 except that all output data appears on DO and all input data is expected on DI. In this mode, DI is ignored while data is being received on DO. This mode is compatible with SPI modes 0,0 and 1,1 where data is shifted out on the falling edge of the clock and is strobed in on the rising edge of the clock.

Table 55: *EECTRL* Bits for the 3-wire Interface

Control Bit	Name	Read/ Write	Description
7	*WFR*	W	Wait for Ready. If this bit is set, the trailing edge of BUSY is delayed until a rising edge is seen on the data line. This bit can be used during the last byte of a Write command to cause the INT5 interrupt to occur when the EEPROM has finished its internal write sequence. This bit is ignored if HiZ=0.
6	*BUSY*	R	Asserted while the serial data bus is busy. When the BUSY bit falls, an INT5 interrupt occurs.
5	*HiZ*	W	Indicates that the SD signal is to be floated to high impedance immediately after the last SDCK rising edge.
4	*RD*	W	Indicates that *EEDATA* (*SFR 0x9E*) is to be filled with data from EEPROM.
3:0	*CNT[3:0]*	W	Specifies the number of clocks to be issued. Allowed values are 0 through 8. If *RD* = 1, CNT bits of data are read MSB first, and right justified into the low order bits of *EEDATA*. If *RD* = 0, CNT bits are sent MSB first to the EEPROM, shifted out of the MSB of *EEDATA*. If *CNT[3:0]* is zero, SDATA simply obeys the HiZ bit.

The timing diagrams in Figure 18 through Figure 22 describe the 3-wire EEPROM interface behavior. All commands begin when the *EECTRL* register is written. Transactions start by first raising the DIO pin that is connected to CS. Multiple 8-bit or less commands such as those shown in Figure 18 through Figure 22 are then sent via *EECTRL* and *EEDATA*.

When the transaction is finished, CS must be lowered. At the end of a Read transaction, the EEPROM drives SDATA, but transitions to HiZ (high impedance) when CS falls. The firmware should then immediately issue a write command with CNT=0 and HiZ=0 to take control of SDATA and force it to a low-Z state.

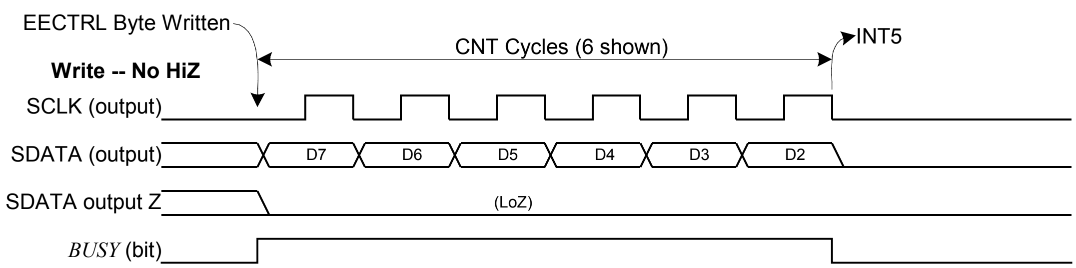


Figure 18: 3-wire Interface. Write Command, HiZ=0.

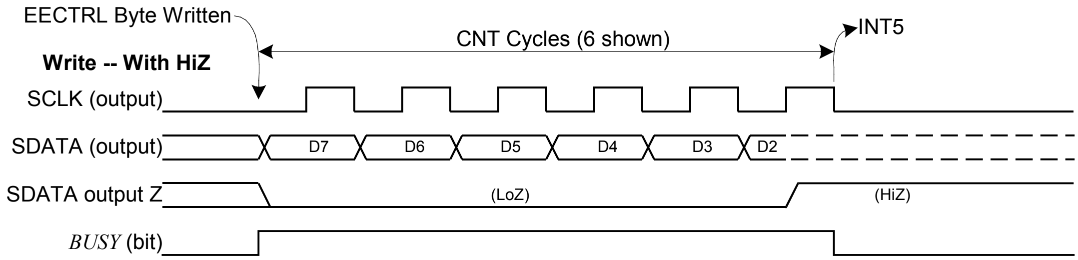


Figure 19: 3-wire Interface. Write Command, HiZ=1

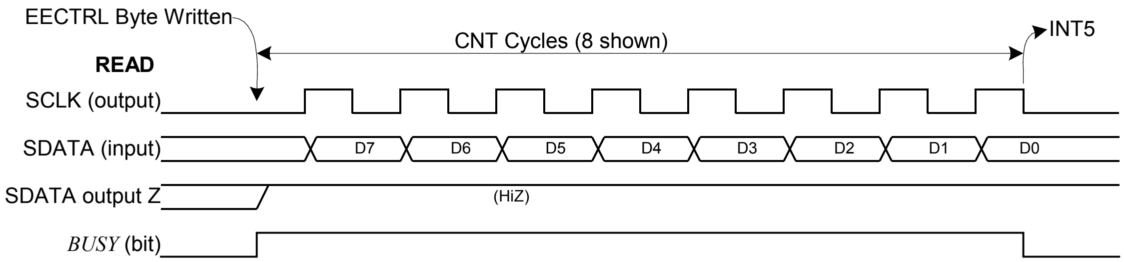


Figure 20: 3-wire Interface. Read Command.

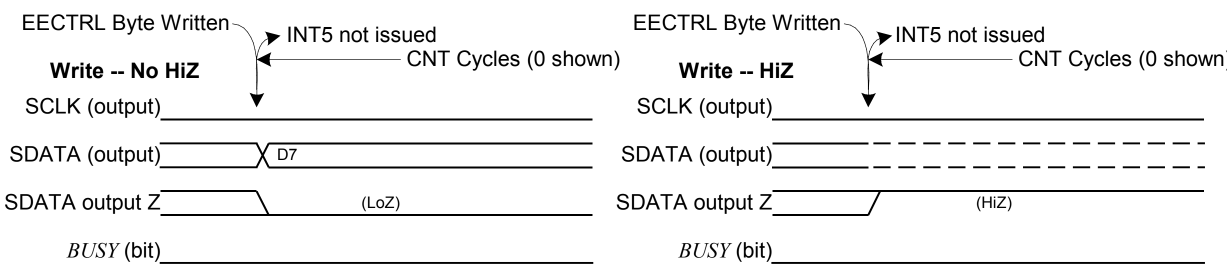


Figure 21: 3-Wire Interface. Write Command when CNT=0

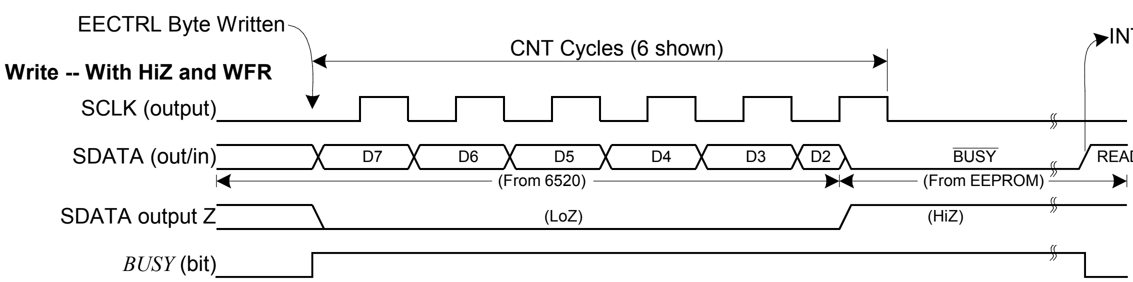


Figure 22: 3-wire Interface. Write Command when HiZ=1 and WFR=1.

2.5.12 SPI Slave Port

The slave SPI port communicates directly with the MPU data bus and is able to read and write Data RAM and Configuration RAM (I/O RAM) locations. It is also able to send commands to the MPU. The interface to the slave port consists of the SPI_CSZ, SPI_CKI, SPI_DI and SPI_DO pins. These pins are multiplexed with the combined DIO/LCD segment driver pins SEGDIO36 to SEGDIO39 (pins 3, 2, 1 and 100).

Additionally, the SPI interface allows flash memory to be read and to be programmed. To facilitate flash programming, cycling power or asserting RESET causes the SPI port pins to default to SPI mode. The SPI port is disabled by clearing the *SPI_E* bit *(I/O RAM 0x270C[4])*.

Possible applications for the SPI interface are:

1) An external host reads data from CE locations to obtain metering information. This can be used in applications where the 71M6543 function as a smart front-end with preprocessing capability. Since the addresses are in 16-bit format, any type of XRAM data can be accessed: CE, MPU, I/O RAM, but not SFRs or the 80515-internal register bank.
2) A communication link can be established via the SPI interface: By writing into MPU memory locations, the external host can initiate and control processes in the 71M6543 MPU. Writing to a CE or MPU location normally generates an interrupt, a function that can be used to signal to the MPU that the byte that had just been written by the external host must be read and processed. Data can also be inserted by the external host without generating an interrupt.
3) An external DSP can access front-end data generated by the ADC. This mode of operation uses the 71M6543 as an analog front-end (AFE).
4) Flash programming by the external host (SPI Flash Mode).

SPI Transactions

A typical SPI transaction is as follows. While SPI_CSZ is high, the port is held in an initialized/reset state. During this state, SPI_DO is held in high impedance state and all transitions on SPI_CLK and SPI_DI are ignored. When SPI_CSZ falls, the port begins the transaction on the first rising edge of SPI_CLK. As shown in Table 56, a transaction consists of an optional 16 bit address, an 8 bit command, an 8 bit status byte, followed by one or more bytes of data. The transaction ends when SPI_CSZ is raised. Some transactions may consist of a command only.

When SPI_CSZ rises, SPI command bytes that are not of the form x0000000 cause the *SPI_CMD (SFR 0xFD)* register to be updated and then cause an interrupt to be issued to the MPU. The exception is if the transaction was a single byte. In this case, the *SPI_CMD* byte is always updated and the interrupt issued. *SPI_CMD* is not cleared when SPI_CSZ is high.

The SPI port supports data transfers up to 10 Mb/s. A serial read or write operation requires at least 8 clocks per byte, guaranteeing SPI access to the RAM is no faster than 1.25 MHz, thus ensuring that SPI access to DRAM is always possible.

Table 56: SPI Transaction Fields

Field Name	Required	Size (bytes)	Description
Address	Yes, except single byte transaction	2	16-bit address. The address field is not required if the transaction is a simple SPI command.
Command	Yes	1	8-bit command. This byte can be used as a command to the MPU. In multi-byte transactions, the MSB is the R/W bit. Unless the transaction is multi-byte and *SPI_CMD* is exactly 0x80 or 0x00, the *SPI_CMD* register is updated and an SPI interrupt is issued. Otherwise, the *SPI_CMD* register is unchanged and the interrupt is not issued.
Status	Yes, if transaction includes DATA	1	8-bit status field, indicating the status of the previous transaction. This byte is also available in the MPU memory map as *SPI_STAT (I/O RAM 0x2708)*. See Table 58 for the contents.
Data	Yes, if transaction includes DATA	1 or more	The read or write data. Address is auto incremented for each new byte.

The *SPI_STAT* byte is output on every SPI transaction and indicates the parity of the previous transaction and the error status of the previous transaction. Potential error sources are:

- 71M6543 not ready
- Transaction not ending on a byte boundary.

SPI Safe Mode

Sometimes it is desirable to prevent the SPI interface from writing to arbitrary RAM locations and thus disturbing MPU and CE operation. This is especially true in AFE applications. For this reason, the SPI SAFE mode was created. In SPI SAFE mode, SPI write operations are disabled except for a 16 byte transfer region at address 0x400 to 0x40F. If the SPI host needs to write to other addresses, it must use the *SPI_CMD* register to request the write operation from the MPU. SPI SAFE mode is enabled by the *SPI_SAFE* bit *(I/O RAM 0x270C[3])*.

Single-Byte Transaction

If a transaction is a single byte, the byte is interpreted as SPI_CMD. Regardless of the byte value, single-byte transactions always update the *SPI_CMD* register and cause an SPI interrupt to be generated.

Multi-Byte Transaction

As shown in Figure 23, multi-byte operations consist of a 16 bit address field, an 8 bit CMD, a status byte, and a sequence of data bytes. A multi byte transaction is three or more bytes.

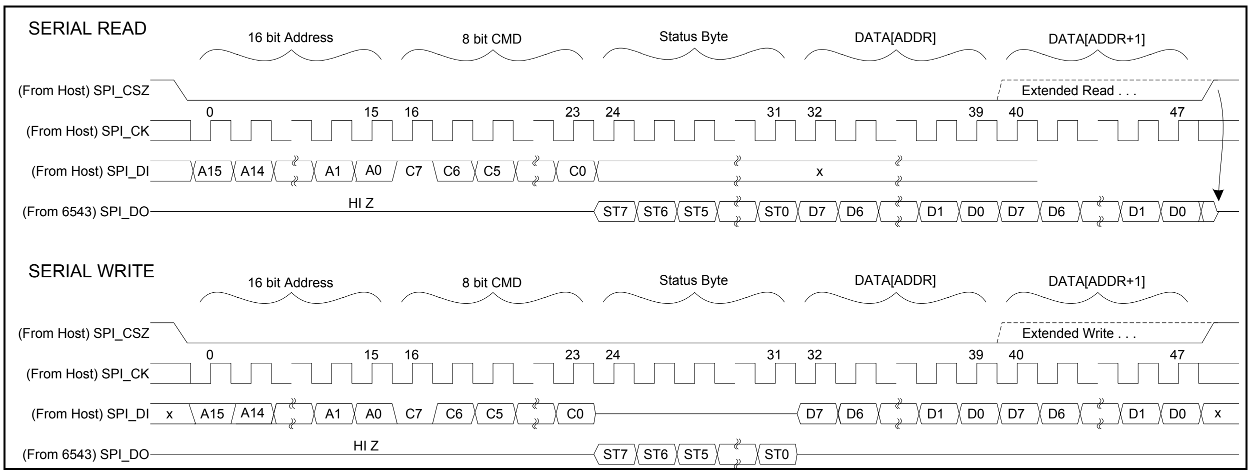


Figure 23: SPI Slave Port - Typical Multi-Byte Read and Write operations

Table 57: SPI Command Sequences

Command Sequence	Description
ADDR 1xxx xxxx STATUS Byte0 ... ByteN	Read data starting at ADDR. ADDR is auto-incremented until SPI_CSZ is raised. Upon completion, *SPI_CMD (SFR 0xFD)* is updated to 1xxx xxxx and an SPI interrupt is generated. The exception is if the command byte is 1000 0000. In this case, no MPU interrupt is generated and *SPI_CMD* is not updated.
ADDR 0xxx xxxx STATUS Byte0 ... ByteN	Write data starting at ADDR. ADDR is auto-incremented until SPI_CSZ is raised. Upon completion, *SPI_CMD* is updated to 0xxx xxxx and an SPI interrupt is generated. The exception is if the command byte is 0000 0000. In this case, no MPU interrupt is generated and *SPI_CMD* is not updated.

Table 58: SPI Registers

Name	Location	Rst	Wk	Dir	Description
EX_SPI	2701[7]	0	0	R/W	SPI interrupt enable bit.
SPI_CMD	SFR FD[7:0]	–	–	R	SPI command. The 8-bit command from the bus master.
SPI_E	270C[4]	1	1	R/W	SPI port enable bit. It enables the SPI interface on pins SEGDIO36 – SEGDIO39.
IE_SPI	SFR F8[7]	0	0	R/W	SPI interrupt flag. Set by hardware, cleared by writing a 0.

Name	Location	Rst	Wk	Dir	Description
SPI_SAFE	270C[3]	0	0	R/W	Limits SPI writes to *SPI_CMD* and a 16 byte region in DRAM when set. No other write operations are permitted.
SPI_STAT	2708[7:0]	0	0	R	*SPI_STAT* contains the status results from the previous SPI transaction Bit 7 - 71M6543 ready error: the 71M6543 was not ready to read or write as directed by the previous command. Bit 6 - Read data parity: This bit is the parity of all bytes read from the 71M6543 in the previous command. Does not include the SPI_STAT byte. Bit 5 - Write data parity: This bit is the overall parity of the bytes written to the 71M6543 in the previous command. It includes CMD and ADDR bytes. Bit 4:2 - Bottom 3 bits of the byte count. Does not include ADDR and CMD bytes. One, two, and three byte instructions return 111. Bit 1 - SPI FLASH mode: This bit is zero when the TEST pin is zero. Bit 0 - SPI FLASH mode ready: Used in SPI FLASH mode. Indicates that the flash is ready to receive another write instruction.

SPI Flash Mode (SFM)

In normal operation, the SPI slave interface cannot read or write the flash memory. However, the 71M6543 supports a special flash mode (SFM) which facilitates initial programming of the flash memory. When the 71M6543 is in this mode, the SPI can erase, read, and write the flash memory. Other memory elements such as XRAM and IO RAM are not accessible in this mode. In order to protect the flash contents, several operations are required before the SFM mode is successfully invoked.

In SFM mode, the 71M6543 supports n byte reads and dual-byte writes to flash memory. See the SPI Transaction description on Page 68 for the format of read and write commands. Since the flash write operation is always based on a two-byte word, the initial address must always be even. Data is written to the 16-bit flash memory bus after the odd word is written.

When the 71M6543G is operating SFM, SPI single-byte transactions are used to write to *FL_BANK[1:0] (SFR 0xB6[1:0])*. During an SPI single-byte transaction, SPI_CMD[1:0] will over-write the contents of *FL_BANK[1:0] (SFR 0xB6[1:0])*. This will allow for access of the entire 128 KB flash memory while operating in SFM.

In SFM mode, the MPU is completely halted. For this reason, the interrupt feature described in the SPI Transaction section above is not available in SFM mode. The 71M6543 must be reset by the WD timer or by the RESET pin in order to exit SFM mode.

Invoking SFM

The following conditions must be met prior to invoking SFM:

- ICE_E = 1. This disables the watchdog and adds another layer of protection against inadvertent Flash corruption.
- The external power source (V3P3SYS, V3P3A) is at the proper level (> 3.0 VDC).
- *PREBOOT* = 0 (*SFR 0xB2[7]*). This validates the state of the *SECURE* bit *(SFR 0xB2[6])*.
- *SECURE* = 0. This I/O RAM register indicates that SPI secure mode is not enabled. Operations are limited to SFM Mass Erase mode if the *SECURE* bit = 1 (Flash read back is not allowed in Secure mode).
- *FLSH_UNLOCK[3:0]* = 0010 (*I/O RAM 0x2702[7:4]*).

The I/O RAM registers *SFMM* (*I/O RAM 0x2080*) and *SFMS (I/O RAM 0x2081)* are used to invoke SFM. Only the SPI interface has access to these two registers. This eliminates an indirect path from the MPU for disabling the watchdog. *SFMM* and *SFMS* need to be written to in sequence in order to invoke SFM. This sequential write process prevents inadvertent entering of SFM. The sequence for invoking SFM is:

- First, write to *SFMM* (*I/O RAM 0x2080*) register. The value written to this register defines the SFM mode.
    - 0xD1: Mass Erase mode. A Flash Mass erase cycle is invoked upon entering SFM.
    - 0x2E: Flash Read back mode. SFM is entered for Flash read back purposes. Flash writes will not be blocked and it is up to the user to guarantee that only previously unwritten locations are written. This mode is not accessible when SPI secure mode is set.
    - SFM is not invoked if any other pattern is written to the *SFMM* register.
- Next, write 0x96 to the *SFMS* (*I/O RAM 0x2081*) register. This write invokes SFM provided that the previous write operation to *SFMM* met the requirements. Writing any other pattern to this register does not invoke SFM. Additionally, any write operations to this register automatically reset the previously written *SFMM* register values to zero.

SFM Details

The following occurs upon entering SFM.

- The CE is disabled.
- The MPU is halted. Once the MPU is halted it can only be restarted with a reset. This reset can be accomplished with the RESET pin, a watchdog reset, or by cycling power (without battery at the VBAT pin).
- The Flash control logic is reset in case the MPU was in the middle of a Flash write operation or Erase cycle.
- Mass erase is invoked if specified in the *SFMM (I/O RAM 0x2080)* register (see Invoking SFM, above). The *SECURE* bit (*SFR 0xB2[6]*) is cleared at the end of this and all Mass Erase cycles.
- All SPI read and write operations now refer to Flash instead of XRAM space.

The SPI host can access the current state of the pending multi-cycle Flash access by performing a 4-byte SPI write of any address and checking the status field.

All SPI write operations in SFM mode must be 6-byte write transactions that write two bytes to an even address. The write transactions must contain a command byte of 0x00 which is the form that does not create an MPU interrupt. Auto incrementing is disabled for write operations.

SPI read transactions can make use of auto increment and may access single bytes. The command byte must always be 0x80 in SFM read transactions.

SPI commands in SFM

Interrupts are not generated in SFM since the MPU is halted. The format of the commands is shown in the SPI Transactions description on Page 68.**SPI Transactions**

2.5.13 Hardware Watchdog Timer

An independent, robust, fixed-duration, watchdog timer (WDT) is included in the 71M6543. It uses the RTC crystal oscillator as its time base and must be refreshed by the MPU firmware at least every 1.5 seconds. When not refreshed on time, the WDT overflows and the part is reset as if the RESET pin were pulled high, except that the I/O RAM bits are in the same state as after a wake-up from SLP or LCD modes (see the I/O RAM description in 5.2 for a list of I/O RAM bit states after RESET and wake-up). Four thousand, one hundred CK32 cycles (or 125 ms) after the WDT overflow, the MPU is launched from program address 0x0000.

The watchdog timer is also reset when the internal signal WAKE=0 (see 3.4 Wake-Up Behavior). The WDT is disabled when the ICE_E pin is pulled high.

For details, see 3.3.4 Watchdog Timer (WDT) Reset.

2.5.14 Test Ports (TMUXOUT and TMUX2OUT Pins)

Two independent multiplexers allow the selection of internal analog and digital signals for the TMUXOUT and TMUX2OUT pins. These pins are multiplexed with the SEG47 and SEG46 function. In order to function as test pins, *LCD_MAP[46]* (*I/O RAM 0x2406[6])* and *LCD_MAP[47]* (*I/O RAM 0x2406[7]*) must be 0.

One of the digital or analog signals listed in Table 60 can be selected to be output on the TMUXOUT pin. The function of the multiplexer is controlled with the I/O RAM register *TMUX[4:0] (I/O RAM 0x2502[4:0]*, as shown in Table 59.

One of the digital or analog signals listed in Table 60 can be selected to be output on the TMUX2OUT pin. The function of the multiplexer is controlled with the I/O RAM register *TMUX2[4:0] (I/O RAM 0x2503[4:0])*, as shown in.

The TMUX and TMUX2 I/O RAM locations are non-volatile and their contents are preserved by battery power and across resets.

The TMUXOUT and TMUX2OUT pins may be used for diagnosis purposes or in production test. The RTC 1-second output may be used to calibrate the crystal oscillator. The RTC 4-second output provides even higher precision.

Table 59: *TMUX[4:0]* Selections

TMUX[5:0]	Signal Name	Description
1	RTCLK	32.768 kHz clock waveform
9	WD_RST	Indicates when the MPU has reset the watchdog timer. Can be monitored to determine spare time in the watchdog timer.
A	CKMPU	MPU clock – see Table 8
D	V3AOK bit	Indicates that the V3P3A pin voltage is ≥ 3.0 V. The V3P3A and V3P3SYS pins are expected to be tied together at the PCB level. The 71M6543 monitors the V3P3A pin voltage only.
E	V3OK bit	Indicates that the V3P3A pin voltage is ≥ 2.8 V. The V3P3A and V3P3SYS pins are expected to be tied together at the PCB level. The 71M654 monitors the V3P3A pin voltage only.
1B	MUX_SYNC	Internal multiplexer frame SYNC signal. See Figure 4 and Figure 5.
1C	CE_BUSY interrupt	See 2.3.3 on page 25 and Figure 12 on page 45
1D	CE_XFER interrupt	
1F	RTM output from CE	See 2.3.5 on page 26
Note: All *TMUX[5:0]* values which are not shown are reserved.		

Table 60: *TMUX2[4:0]* Selections

TMUX2[4:0]	Signal Name	Description
0	WD_OVF	Indicates when the watchdog timer has expired (overflowed).
1	PULSE_1S	One second pulse with 25% Duty Cycle. This signal can be used to measure the deviation of the RTC from an ideal 1 second interval. Multiple cycles should be averaged together to filter out jitter.
2	PULSE_4S	Four second pulse with 25% Duty Cycle. This signal can be used to measure the deviation of the RTC from an ideal 4 second interval. Multiple cycles should be averaged together to filter out jitter. The 4 second pulse provides a more precise measurement than the 1 second pulse.
3	RTCLK	32.768 kHz clock waveform
8	SPARE[1] bit – *I/O RAM 0x2704[1]*	Copies the value of the bit stored in 0x2704[1]. For general purpose use.
9	SPARE[2] bit – *I/O RAM 0x2704[2]*	Copies the value of the bit stored in 0x2704[2]. For general purpose use.
A	WAKE	Indicates when a WAKE event has occurred.
B	MUX_SYNC	Internal multiplexer frame SYNC signal. See Figure 4 and Figure 5.
C	MCK	See 2.5.3 on page 49.
E	GNDD	Digital GND. Use this signal to make the TMUX2OUT pin static.
12	INT0 – DIG I/O	Interrupt 0. See 2.4.8 on page 39. Also see Figure 12 on page 45.
13	INT1 – DIG I/O	
14	INT2 – CE_PULSE	
15	INT3 – CE_BUSY	
16	INT4 - VSTAT	
17	INT5 – EEPROM/SPI	
18	INT6 – XFER, RTC	
1F	RTM_CK (flash)	See 2.3.5 on page 26.

Note:
All *TMUX2[4:0]* values which are not shown are reserved.

3 Functional Description

3.1 Theory of Operation

The energy delivered by a power source into a load can be expressed as:

$$E = \int_0^t V(t) I(t) dt$$

Assuming phase angles are constant, the following formulae apply:

- P = Real Energy [Wh] = V * A * cos φ* t
- Q = Reactive Energy [VARh] = V * A * sin φ * t
- S = Apparent Energy [VAh] = $\sqrt{P^2 + Q^2}$

For a practical meter, not only voltage and current amplitudes, but also phase angles and harmonic content may change constantly. Thus, simple RMS measurements are inherently inaccurate. A modern solid-state electricity meter IC such as the 71M6543 functions by emulating the integral operation above, i.e. it processes current and voltage samples through an ADC at a constant frequency. As long as the ADC resolution is high enough and the sample frequency is beyond the harmonic range of interest, the current and voltage samples, multiplied with the time period of sampling yields an accurate quantity for the momentary energy. Summing-up the momentary energy quantities over time results in accumulated energy.

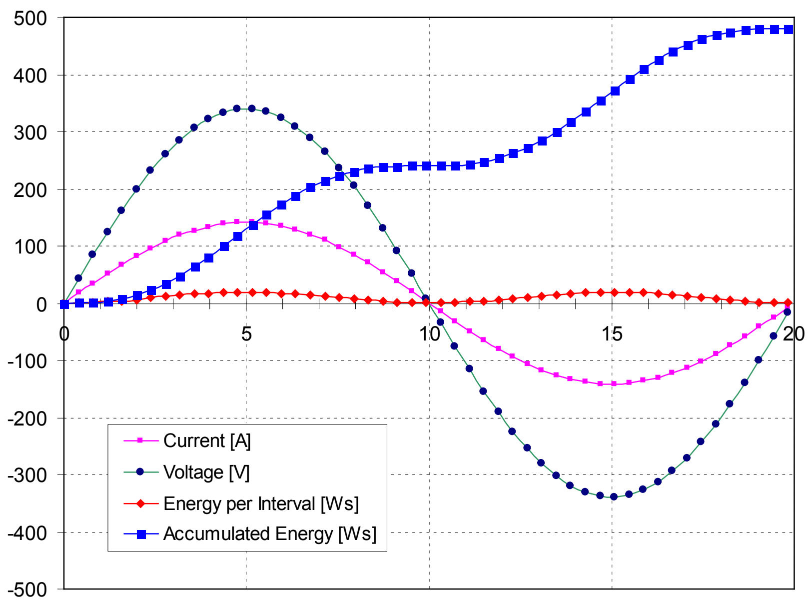


Figure 24: Voltage, Current, Momentary and Accumulated Energy

Figure 24 shows the shapes of V(t), I(t), the momentary power and the accumulated power, resulting from 50 samples of the voltage and current signals over a period of 20 ms. The application of 240 VAC and 100 A results in an accumulation of 480 Ws (= 0.133 Wh) over the 20 ms period, as indicated by the accumulated power curve. The described sampling method works reliably, even in the presence of dynamic phase shift and harmonic distortion.

3.2 Battery Modes

Shortly after system power (V3P3SYS) is applied, the 71M6543 is in mission mode (MSN mode). MSN mode means that the part is operating with system power and that the internal PLL is stable. This mode is the normal operating mode where the part is capable of measuring energy.

When system power is not available, the 71M6543 is in one of three battery modes:

- BRN mode (brownout mode)
- LCD mode (LCD-only mode)
- SLP mode (sleep mode).

An internal comparator monitors the voltage at the V3P3SYS pin (note that V3P3SYS and V3P3A are typically connected together at the PCB level). When the V3P3SYS dc voltage drops below 2.8 VDC, the comparator resets an internal power status bit called *V3OK* . As soon as system power is removed and *V3OK* = 0, the 71M6543 is forced to BRN mode. The MPU continues to execute code when the system transitions from MSN to BRN mode or from BRN to MSN mode. A soft reset should be executed when returning from BRN to MSN mode in order to re-initialize the I/O RAM. Depending on the MPU code, the MPU can choose to stay in BRN mode, or transition to LCD or to SLP mode (via the I/O RAM bits *LCD_ONLY*, *I/O RAM 0x28B2[6]* and *SLEEP, I/O RAM 0x28B2[7]*). BRN mode is similar to MSN mode except that resources powered by system power, such as the ADC and the CE, are not available (see Table 61), and that the supply current is drawn from the VBAT pin. In BRN mode, the PLL continues to function at the same frequency as in MSN mode. The MPU can configure BRN mode as it desires. For instance, it may choose to minimize battery power by reducing the PLL or MPU clock speed (see 3.2.1 BRN Mode, for the recommended settings to realize minimum power consumption in BRN mode).

When system power is restored, the 71M6543 automatically transitions from any of the battery modes (BRN, LCD, SLP) back to MSN mode.

Figure 25 shows a state diagram of the various operating modes, with the possible transitions between modes.

When the part wakes-up under battery power, the part automatically enters BRN mode (see 3.4 Wake-Up Behavior). From BRN mode, the part may enter either LCD mode or SLP mode, as controlled by the MPU.

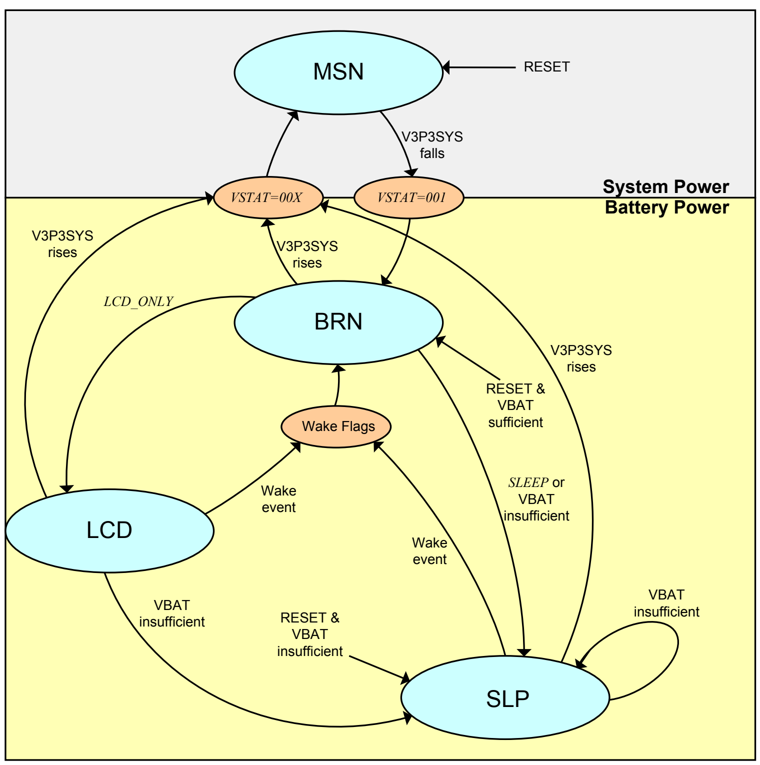


Figure 25: Operation Modes State Diagram

Transitions from both LCD and SLP mode to BRN mode can be initiated by the following events:

- Wake-up timer timeout.
- Pushbutton (PB) is activated.
- A rising edge on SEGDIO4, or a high logic level on SEGDIO52 or SEGDIO55.
- Activity on the RX or OPT_RX pins.

The MPU has access to a variety of registers that signal the event that caused the wake up. See 3.4 Wake-Up Behavior for details.

Table 61 shows the circuit functions available in each operating mode.

Table 61: Available Circuit Functions

Circuit Function	System Power		Battery Power			
	MSN (Mission Mode)		BRN (Brownout Mode)		LCD	SLEEP
	PLL_FAST=1	PLL_FAST=0	PLL_FAST=1	PLL_FAST=0		
CE (Computation Engine)	Yes	Yes	--[1]	--	--	--
FIR	Yes	Yes	--	--	--	--
ADC, VREF	Yes	Yes	--	--	--	--
PLL	Yes	Yes	Yes	Yes	Boost[2]	--
Battery Measurement	Yes	Yes	Yes	Yes	--	--
Temperature sensor	Yes	Yes	Yes	Yes	Yes	Yes
Max MPU clock rate	4.92MHz (from PLL)	1.57MHz (from PLL)	4.92MHz (from PLL)	1.57MHz (from PLL)	--	--
MPU_DIV clk. divider	Yes	Yes	Yes	Yes	--	--
ICE	Yes	Yes	Yes	Yes	--	--
DIO Pins	Yes	Yes	Yes	Yes	--	--
Watchdog Timer	Yes	Yes	Yes	Yes	--	--
LCD	Yes	Yes	Yes	Yes	Yes	--
LCD Boost	Yes	Yes	Yes	Yes	Yes	
EEPROM Interface (2-wire)	Yes	Yes	Yes	Yes	--	--
EEPROM Interface (3-wire)	Yes	Yes	Yes	Yes	--	--
UART (full speed)	Yes	Yes	Yes	Yes	--	--
Optical TX modulation	38.4kHz	38.9kHz	38.4kHz	38.9kHz	--	--
Flash Read	Yes	Yes	Yes	Yes	--	--
Flash Page Erase	Yes	Yes	Yes	Yes	--	--
Flash Write	Yes	Yes	Yes	Yes	--	--
RAM Read and Write	Yes	Yes	Yes	Yes	--	--
Wakeup Timer	Yes	Yes	Yes	Yes	Yes	Yes
OSC and RTC	Yes	Yes	Yes	Yes	Yes	Yes
DRAM data preservation	Yes	Yes	Yes	Yes	--	--
NV RAM data preservation	Yes	Yes	Yes	Yes	Yes	Yes

Notes:

1. "--" indicates that the corresponding circuit is not active
2. "Boost" implies that the LCD boost circuit is active (i.e., *LCD_VMODE[1:0]* = 10 (*I/O RAM 0x2401[7:6]*)). The LCD boost circuit requires a clock from the PLL to function. Thus, the PLL is automatically kept active if LCD boost is active while in LCD mode, otherwise the PLL is de-activated.

3.2.1 BRN Mode

In BRN mode, most non-metering digital functions are active (as shown in Table 61) including ICE, UART, EEPROM, LCD and RTC. In BRN mode, the PLL continues to function at the same frequency as MSN mode. It is up to the MPU to scale down the PLL (using *PLL_FAST, I/O RAM 0x2200[4]*) or the MPU frequency (using *MPU_DIV[2:0], I/O RAM 0x2200[2:0]*) in order to save power.

From BRN mode, the MPU can choose to enter LCD or SLP modes. When system power is restored while the 71M6543 is in BRN mode, the part automatically transitions to MSN mode.

The recommended minimum power configuration for BRN mode is as follows:

- *RCE0* = 0x00 (*I/O RAM 0x2709[7:0]*) - remote sensors disabled
- *LCD_BAT* = 1 (*I/O RAM 0x2402[7]*) - LCD powered from VBAT
- *LCD_VMODE[1:0]* = 0 (*I/O RAM 0x2401[7:6]*) - 5V LCD boost disabled
- *CE6* = 0x00 (*I/O RAM 0x2106*) - CE, RTM and CHOP are disabled
- *MUX_DIV[3:0]* = 0(*I/O RAM 0x2100[7:4])* - the ADC multiplexer is disabled
- *ADC_E* = 0 (*I/O RAM 0x2704[4]*) - ADC disabled
- *VREF_CAL* = 0 (*I/O RAM 0x2704[7]*) – Vref not driven out
- *VREF_DIS* = 1 (*I/O RAM 0x2704[6]*) - Vref disabled
- *PRE_E* = 0 (*I/O RAM 0x2704[5]* - pre-amp disabled
- *BCURR* = 0 (*I/O RAM 0x2704[3]*) - battery 100µA current load OFF
- *TMUX[5:0]* = 0x0E (*I/O RAM 0x2502[5:0]*) – TMUXOUT output set to a dc value
- *TMUX2[4:0]* = 0x0E (*I/O RAM 0x2503[4:0]*) – TMUXOUT2 output set to a dc value
- *CKGN* = 0x24 (*I/O RAM 0x2200*) - PLL set slow, and *MPU_DIV[2:0] (I/O RAM 0x2200[2:0])* set to maximum
- *TEMP_PER[2:0]* = 6 (*I/O RAM 0x28A0[2:0]*) - temp measurement set to automatic every 512 s
- *TEMP_BSEL* = 1 (*I/O RAM 0x28A0[7]*) - temperature sensor monitors VBAT
- *PCON* |= 1 (*SFR 0x87*) - at the end of the main BRN loop, halt the MPU and wait for an interrupt
- The baud rate registers are adjusted as needed
- All unused interrupts are disabled

3.2.2 LCD Mode

LCD mode may be commanded by the MPU at any time by setting the *LCD_ONLY* control bit (*I/O RAM 0x28B2[6]*). However, it is recommended that the *LCD_ONLY* control bit be set by the MPU only after the 71M6543 has entered BRN mode. For example, if the 71M6543 is in MSN mode when *LCD_ONLY* is set, the duration of LCD mode is very brief and the 71M6543 immediately 'wakes'.

In LCD mode, V3P3D is disabled, and the VBAT pin supplies the LCD current. Before asserting *LCD_ONLY* mode, it is recommended that the MPU minimize PLL current by reducing the output frequency of the PLL to 6.29 MHz (i.e., write *PLL_FAST* = 0, *I/O RAM 0x2200[4]*). The LCD boost system requires a clock from the PLL for its operation. Thus, if the LCD boost system is enabled (i.e., *LCD_VMODE[1:0]* = 10, *I/O RAM 0x2401[7:6]*), then the PLL is automatically kept active during LCD mode, otherwise the PLL is de-activated.

In LCD mode, the data contained in the *LCD_SEG* registers is displayed using the segment driver pins. Up to two LCD segments connected to the pins SEGDIO22 and SEGDIO23 can be made to blink without the involvement of the MPU, which is disabled in LCD mode. To minimize battery power consumption, only segments that are used should be enabled.

After the transition from LCD mode to MSN or BRN mode, the *PC* (Program Counter) is at 0x0000, the XRAM is in an undefined state, and configuration I/O RAM bits are reset (see Table 70 for I/O RAM state upon wake). The data stored in non-volatile I/O RAM locations is preserved in LCD mode (the shaded locations in Table 70 are non-volatile).

3.2.3 SLP Mode

The SLP mode may be commanded by the MPU whenever main system power is absent by asserting the *SLEEP* bit *(I/O RAM 0x28B2[7])*. The purpose of the SLP mode is to consume the least power while still maintaining the RTC, temperature compensation of the RTC, and the non-volatile portions of the I/O RAM.

In SLP mode, the V3P3D pin is disconnected, removing all sources of leakage from VBAT and V3P3SYS. The non-volatile memory domain and the basic functions, such as temperature sensor, oscillator, and RTC, are powered by the VBAT_RTC input. In this mode, the I/O configuration bits, LCD configuration bits, and NV RAM values are preserved and RTC and oscillator continue to run. This mode can be exited only by system power-up or one of the wake methods described in 3.4 Wake-Up Behavior.

If the *SLEEP* bit is asserted when V3P3SYS pin power is present (i.e., while in MSN mode), the 71M6543 enters SLP mode, resetting the internal WAKE signal, at which point the 71M6543 begins the standard wake from sleep procedures as described in 3.4 Wake-Up Behavior.

After the transition from SLP mode to MSN or BRN mode the *PC* is at 0x0000, the XRAM is in an undefined state, and the I/O RAM is only partially preserved (see the description of I/O RAM states in 5.2). The non-volatile sections of the I/O RAM are preserved unless RESET goes high.

3.3 Fault and Reset Behavior

3.3.1 Events at Power-Down

Power fault detection is performed by internal comparators that monitor the voltage at the V3P3A pin and also monitor the internally generated VDD pin voltage (2.5 VDC). The V3P3SYS and V3P3A pins must be tied together at the PCB level, so that the comparators, which are internally connected only to the V3P3A pin, are able to simultaneously monitor the common V3P3SYS and V3P3A pin voltage. The following discussion assumes that the V3P3A and V3P3SYS pins are tied together at the PCB level.

During a power failure, as V3P3A falls, two thresholds are detected:

- The first threshold, at 3.0 VDC (*VSTAT[2:0]* = 001, *SFR 0xF9[2:0]*), warns the MPU that the analog modules are no longer accurate. Other than warning the MPU, the hardware takes no action when this threshold is crossed. This comparison produces an internal bit named *V3OKA*.
- The second threshold, at 2.8 VDC, causes the 71M6543 to switch to battery power. This switching happens while the FLASH and RAM systems are still able to read and write. This comparison produces an internal bit named *V3OK*.

The power quality is reflected by the *VSTAT[2:0]* register in I/O RAM space, as shown in Table 62. The *VSTAT[2:0]* register is located at SFR address F9 and occupies bits 2:0. The *VSTAT[2:0]* field can only be read.

In addition to the state of the main power, the *VSTAT[2:0]* register provides information about the internal VDD voltage under battery power. Note that if system power (V3P3A) is above 2.8 VDC, the 71M6543 always switches from battery to system power.

Table 62: *VSTAT[2:0]* (SFR 0xF9[2:0])

VSTAT[2:0]	Description
000	System Power OK. V3P3A > 3.0 VDC. Analog modules are functional and accurate.
001	System Power is low. 2.8 VDC < V3P3A < 3.0 VDC. Analog modules not accurate. Switch over to battery power is imminent.
010	The IC is on battery power and VDD is OK. VDD > 2.25 VDC. The IC has full digital functionality.
011	The IC is on battery power and 2.25 VDC > VDD > 2.0 VDC. Flash write operations are inhibited.
101	The IC is on battery power and VDD < 2.0, which means that the MPU is nearly out of voltage. A reset occurs in 4 cycles of the crystal clock CK32.

The response to a system power fault is almost entirely controlled by firmware. During a power failure, system power slowly falls. This fall in power is monitored by internal comparators that cause the hardware to automatically switch over to taking power from the VBAT input. An interrupt notifies the MPU that the part is now battery powered. At this point, it is the MPU’s responsibility to reduce power by slowing the clock rate, disabling the PLL, etc.

Precision analog components such as the bandgap reference, the bandgap buffer, and the ADC are powered only by the V3P3A pin and become inaccurate and ultimately unavailable as the V3P3A pin voltage continues to drop (i.e., circuits powered by the V3P3A pin are not backed by the VBAT pin). When the V3P3A pin falls below 2.8 VDC, the ADC clocks are halted and the amplifiers are unbiased. Meanwhile, control bits such as *ADC_E* bit *(I/O RAM 0x2704[4])* are not affected, since their I/O RAM storage is powered from the VDD pin (2.5 VDC). The VDD pin is supplied with power through an internal 2.5 VDC regulator that is connected to the V3P3D pin. In turn, the V3P3D pin is switched to receive power from the VBAT pin when the V3P3SYS pin drops below 3.0 VDC. Note that the V3P3SYS and V3P3A pins are typically tied together at the PCB level.

3.3.2 IC Behavior at Low Battery Voltage

When system power is not present, the 71M6543 relies on the VBAT pin for power. If the VBAT voltage is not sufficient to maintain VDD at 2.0 VDC or greater, the MPU cannot operate reliably. Low VBAT voltage can occur while the part is operating in BRN mode, or while it is dormant in SLP or LCD mode. Two cases can be distinguished, depending on MPU code:

- Case 1: System power is not present, and the part is waking from SLP or LCD mode. In this case, the hardware checks the value of VDD to determine if processor operation is possible. If it is not possible, the part configures itself for BRN operation, and holds the processor in reset (WAKE=0). In this mode, VBAT powers the 1.0 VDC reference for the LCD system, the VDD regulator, the PLL, and the fault comparator. The part remains in this waiting mode until VDD becomes high due to system power being applied or the VBAT battery being replaced or recharged.
- Case 2: The part is operating under VBAT power and *VSTAT[2:0] (SFR 0xF9[2:0])* becomes 101, indicating that VDD falls below 2.0 VDC. In this case, the firmware has two choices:
  1) One choice is to assert the *SLEEP* bit (*I/O RAM 0x28B2[7])* immediately. This assertion preserves the remaining charge in VBAT. Of course, if the battery voltage is not increased, the 71M6543 enters Case 1 as soon as it tries to wake up.
  2) The alternative choice is to enter the waiting mode described in Case 1 immediately. Specifically, if the firmware does not assert the *SLEEP* bit, the hardware resets the processor four CE32 clock cycles (i.e. 122 μs) after *VSTAT[2:0]* becomes 101 and, as described in Case 1, it begins waiting for VDD to become greater than 2.0 VDC. The MPU wakes up when system power returns, or when VDD becomes greater than 2.0 VDC.

In either case, when VDD recovers, and when the MPU wakes up, the *WF_BADVDD* flag (*I/O RAM 0x28B0[2]*) can be read to determine that the processor is recovering from a bad VBAT condition. The *WF_BADVDD* flag remains set until the next time WAKE falls. This flag is independent of the other WF flags.

In all cases, low VBAT voltage does not corrupt RTC operation, the state of NV memory, or the state of non-volatile memory. These circuits depend on the VBAT_RTC pin for power.

3.3.3 Reset Sequence

When the RESET pin is pulled high, all digital activity in the chip stops, with the exception of the oscillator and RTC. Additionally, all I/O RAM bits are forced to their RST state. A reliable reset does not occur until RESET has been high at least for 2 μs. Note that TMUX and the RTC are not reset unless the TEST pin is pulled high while RESET is high.

The *RESET* control bit (*I/O RAM 0x 2200[3]*) performs an identical reset to the RESET pin except that a significantly shorter reset timer is used.

Once initiated, the reset sequence waits until the reset timer times out. The time out occurs in 4100 CE32 cycles (125 ms), at which time the MPU begins executing its pre-boot and boot sequences from address 0x0000. See 2.5.1.1 for a detailed description of the pre-boot and boot sequences.

If system power is not present, the reset timer duration is two CE32 cycles, at which time the MPU begins executing in BRN mode, starting at address 0x0000.

A softer form of reset is initiated when the E_RST pin of the ICE interface is pulled low. This event causes the MPU and other registers in the MPU core to be reset but does not reset the remainder of the 71M6543. It does not trigger the reset sequence. This type of reset is intended to reset the MPU program, but not to make other changes to the chip's state.

3.3.4 Watchdog Timer (WDT) Reset

The watchdog timer (WDT) is described in 2.5.13.

A status bit, *WF_OVF (I/O RAM 0x28B0[4])*, is set when a WDT overflow occurs. Similar to the other wake flags, this bit is powered by the non-volatile supply and can be read by the MPU to determine if the part is initializing after a WD overflow event or after a power-up. The *WF_OVF* bit is cleared by the RESET pin.

There is no internal digital state that could deactivate the WDT. For debug purposes, however, the WDT can be disabled by raising the ICE_E pin to 3.3 VDC.

In normal operation, the WDT is reset by periodically writing a one to the *WD_RST* control bit *I/O RAM 0x28B4[7])*. The watchdog timer is also reset when the 71M6543 wakes from LCD or SLP mode, and when ICE_E=1.

3.4 Wake-Up Behavior

As described above, the part always wakes up in MSN mode when system power is restored. As stated in 3.2 Battery Modes, transitions from both LCD and SLP mode to BRN mode can be initiated by a wake-up timer timeout, when the pushbutton (PB) input is activated, a rising edge on SEGDIO4, or a high logic level on SEGDIO52 or SEGDIO55, or by activity on the RX or OPT_RX pins.

3.4.1 Wake on Hardware Events

The following pin signal events wake the 71M6543 from SLP or LCD mode: a high level on the PB pin, either edge on the RX pin, a rising edge on the SEGDIO4 pin, a high level on the SEGDIO52 pin, or a high level on the SEGDIO55 pin or either edge on the OPT_RX pin. See Table 63 for de-bounce details on each pin and for further details on the OPT_RX/SEGDIO55 pin. The SEGDIO4, SEGDIO52, and SEGDIO55 pins must be configured as DIO inputs and their wake enable (*EW_x* bits) must be set. In SLP and LCD modes, the MPU is held in reset and cannot poll pins or react to interrupts. When one of the hardware wake events occurs, the internal WAKE signal rises and within three CK32 cycles the MPU begins to execute. The MPU can determine which one of the pins awakened it by checking the *WF_PB*, *WF_RX*, *WF_SEGDIO4*, *WF_DIO52*, or *WF_DIO55* flags (see Table 63).

If the part is in SLP or LCD mode, it can be awakened by a high level on the PB pin. This pin is normally pulled to GND and can be connected externally so it may be pulled high by a push button depression.

Some pins are de-bounced to reject EMI noise. Detection hardware ignores all transitions after the initial transition. Table 63 shows which pins are equipped with de-bounce circuitry.

Pins that do not have de-bounce circuits must still be high for at least 2 µs to be recognized.

The wake enable and flag bits are shown in Table 63. The wake flag bits are set by hardware when the MPU wakes from a wake event. Note that the PB flag is set whenever the PB is pushed, even if the part is already awake. Table 65 lists the events that clear the WF flags.

In addition to push buttons and timers, the part can also reboot due to the RESET pin, the *RESET* bit *(I/O RAM 0x2200[3])*, the WDT, the cold start detector, and E_RST. As seen in Table 63, each of these mechanisms has a flag bit to alert the MPU to the source of the wakeup. If the wakeup is caused by return of system power, there is no active WF flag and the *VSTAT[2:0]* field (*SFR 0xF9[2:0])* indicates that system power is stable.

Table 63: Wake Enable and Flag Bits

Wake Enable		Wake Flag		De-bounce	Description
Name	Location	Name	Location		
WAKE_ARM	28B2[5]	*WF_TMR*	28B1[5]	No	Wake on Timer.
EW_PB	28B3[3]	*WF_PB*	28B1[3]	Yes	Wake on PB.*
EW_RX	28B3[4]	*WF_RX*	28B1[4]	2 µs	Wake on either edge of RX.
EW_DIO4	28B3[2]	*WF_DIO4*	28B1[2]	2 µs	Wake on SEGDIO4.
EW_DIO52	28B3[1]	*WF_DIO52*	28B1[1]	Yes	Wake on SEGDIO52.*
EW_DIO55	28B3[0]	*WF_DIO55*	28B1[0]	Yes	*OPT_RXDIS* = 1: Wake on DIO55 with 64 ms de-bounce.* *OPT_RXDIS* = 0: Wake on either edge of OPT_RX with 2 µs de-bounce. *OPT_RXDIS: I/O RAM 0x2457[2]*
Always Enabled		*WF_RST*	28B0[6]	2 µs	Wake after *RESET*.
Always Enabled		*WF_RSTBIT*	28B0[5]	No	Wake after *RESET* bit.
Always Enabled		*WF_ERST*	28B0[3]	2 µs	Wake after E_RST. (ICE must be enabled)

Wake Enable		Wake Flag		De-bounce	Description
Name	Location	Name	Location		
Always Enabled		*WF_OVF*	28B0[4]	No	Wake after WD reset.
Always Enabled		*WF_CSTART*	28B0[7]	No	Wake after cold start - the first application of power.
Always Enabled		*WF_BADVDD*	28B0[2]	No	Wake after insufficient VBAT voltage.

**This pin is sampled every 2 ms and must remain high for 64 ms to be declared a valid high level. This pin is high-level sensitive.*

Table 64: Wake Bits

Name	Location	RST	WK	Dir	Description
EW_DIOR	28B3[2]	0	–	R/W	Connects SEGDIO4 to the WAKE logic and permits SEGDIO4 rising to wake the part. This bit has no effect unless SEGDIO4 is configured as a digital input.
EW_DIO52	28B3[1]	0	–	R/W	Connects DIO52 to the WAKE logic and permits DIO52 high level to wake the part. This bit has no effect unless DIO52 is configured as a digital input.
EW_DIO55	28B3[0]	0	–	R/W	Connects DIO55 to the WAKE logic and permits DIO55 high level to wake the part. This bit has no effect unless DIO55 is configured as a digital input.
WAKE_ARM	28B2[5]	0	–	R/W	Arms the WAKE timer and loads it with the value in *WAKE_TMR* (*I/O RAM 0x2880*) register. When SLP or LCD mode is asserted by the MPU, the WAKE timer becomes active.
EW_PB	28B3[3]	0	–	R/W	Connects the PB pin to the WAKE logic and permits PB high level to wake the part. PB is always configured as an input.
EW_RX	28B3[4]	0	–	R/W	Connects the RX pin to the WAKE logic and permits RX rising to wake the part. See 3.4.1 for de-bounce issues.
WF_DIO4	28B1[2]	0	–	R	SEGDIO4 flag bit. If SEGDIO4 is configured to wake the part, this bit is set whenever SEGDIO4 rises. It is held in reset if SEGDIO4 is not configured for wakeup.
WF_DIO52	28B1[1]	0	–	R	SEGDIO52 flag bit. If SEGDIO52 is configured to wake the part, this bit is set whenever SEGDIO52 is a high level. It is held in reset if SEGDIO52 is not configured for wakeup.
WF_DIO55	28B1[0]	0	–	R	SEGDIO55 flag bit. If SEGDIO55 is configured to wake the part, this bit is set whenever SEGDIO55 is a high level. It is held in reset if SEGDIO55 is not configured for wakeup.
WF_TMR	28B1[5]	0	–	R	Indicates that the Wake timer caused the part to wake up.
WF_PB	28B1[3]	0	–	R	Indicates that the PB pin caused the part to wake.
WF_RX	28B1[4]	0	–	R	Indicates that RX pin caused the part to wake.
WF_RST *WF_RSTBIT* *WF_ERST* *WF_CSTART* *WF_BADVDD*	28B0[6] 28B0[5] 28B0[3] 28B0[7] 28B0[2]	* * * * *	–	R	Indicates that the RST pin, E_RST pin, *RESET* bit (*I/O RAM 0x2200[3]*), the cold start detector, or low voltage on the VBAT pin caused the part to reset. *See Table 65 for details.

Table 65: Clear Events for WAKE flags

Flag	Wake on:	Clear Events
WF_TMR	Timer expiration	WAKE falls
WF_PB	PB pin high level	WAKE falls
WF_RX	Either edge RX pin	WAKE falls
WF_DIO4	SEGDIO4 rising edge	WAKE falls
WF_DIO52	SEGDIO52 high level	WAKE falls
WF_DIO55	If *OPT_RXDIS* = 1 (*I/O RAM 0x2457[2]*), wake on SEGDIO55 high If *OPT_RXDIS* = 0 wake on either edge of OPT_RX	WAKE falls
WF_RST	RESET pin driven high	WAKE falls, WF_CSTART, WF_RSTBIT, WF_OVF, WF_BADVDD
WF_RSTBIT	*RESET* bit is set (*I/O RAM 0x2200[3]*)	WAKE falls, WF_CSTART, WF_OVF, WF_BADVDD, WF_RST
WF_ERST	E_RST pin driven high and the ICE interface must be enabled by driving the ICE_E pin high.	WAKE falls, WF_CSTART, WF_RST, WF_OVF, WF_RSTBIT
WF_OVF	Watchdog (WD) reset	WAKE falls, WF_CSTART, WF_RSTBIT, WF_BADVDD, WF_RST
WF_CSTART	Cold-start (i.e., after the application of first power)	WAKE falls, WF_RSTBIT, WF_OVF, WF_BADVDD, WF_RST

Note:
"WAKE falls" implies that the internal WAKE signal has been reset, which happens automatically upon entry into LCD mode or SLEEP mode (i.e., when the MPU sets the *LCD_ONLY* bit (*I/O RAM 0x28B2[6]*) or the *SLEEP* (*I/O RAM 0x28B2[7]*) bit). When the internal *WAKE* signal resets, all wake flags are reset. Since the various wake flags are automatically reset when *WAKE* falls, it is not necessary for the MPU to reset these flags before entering LCD mode or SLEEP mode. Also, other wake events can cause the wake flag to reset, as indicated above (e.g., the *WF_RST* flag can also be reset by any of the following flags setting: *WF_CSTART*, *WS_RSTBIT*, *WF_OVF*, *WF_BADVDD*)

3.4.2 Wake on Timer

If the part is in SLP or LCD mode, it can be awakened by the Wake Timer. Until this timer times out, the MPU is in reset due to the internal WAKE signal being low. When the Wake Timer times out, WAKE rises and within three CK32 cycles, the MPU begins to execute. The MPU can determine that the timer woke it by checking the *WF_TMR (I/O RAM 0x28B1[2]*) wake flag.

The Wake Timer begins timing when the part enters LCD or SLP mode. Its duration is controlled by the *WAKE_TMR[7:0]* register *(I/O RAM 0x2880)*. The timer duration is *WAKE_TMR[7:0]* +1 seconds.

The Wake Timer is armed by setting *WAKE_ARM* = 1 (*I/O RAM 0x28B2[5]*). It must be armed at least three RTC cycles before either SLP or LCD modes are initiated. Setting *WAKE_ARM* presets the timer with the value in *WAKE_TMR* and readies the timer to start when the MPU writes to the *SLEEP* (*I/O RAM 0x28B2[7]*) or *LCD_ONLY (I/O RAM 0x28B2[6])* bits. The timer is neither reset nor disarmed when the MPU wakes-up. Thus, once armed and set, the MPU continues to be awakened *WAKE_TMR[7:0]* seconds after it requests SLP mode or LCD mode (i.e., once written, the *WAKE_TMR[7:0]* register holds its value and does not have to be re-written each time the MPU enters SLP or LCD mode. Also, since *WAKE_TMR[7:0]* is non-volatile, it also holds its value through resets and power failures).

3.5 Data Flow and MPU/CE Communication

The data flow between the Compute Engine (CE) and the MPU is shown in Figure 26. In a typical application, the 32-bit CE sequentially processes the samples from the ADC inputs, performing calculations to measure active power (Wh), reactive power (VARh), A^2h, and V^2h for four-quadrant metering. These measurements are then accessed by the MPU, processed further and output using the peripheral devices available to the MPU.

Both the CE and multiplexer are controlled by the MPU via shared registers in the I/O RAM and in RAM.

The CE outputs a total of six discrete signals to the MPU. These consist of four pulses and two interrupts:

- CE_BUSY
- XFER_BUSY
- WPULSE, VPULSE (pulses for active and reactive energy)
- XPULSE, YPULSE (auxiliary pulses)

These interrupts are connected to the MPU interrupt service inputs as external interrupts. CE_BUSY indicates that the CE is actively processing data. This signal occurs once every multiplexer cycle (typically 396 μs), and indicates that the CE has updated status information in its *CESTATUS* register *(CE RAM 0x80).*

XFER_BUSY indicates that the CE is updating data to the output region of the RAM. This update occurs whenever the CE has finished generating a sum by completing an accumulation interval determined by *SUM_SAMPS[12:0], I/O RAM 0x2107[4:0], 2108[7:0],* (typically every 1000 ms). Interrupts to the MPU occur on the falling edges of the XFER_BUSY and CE_BUSY signals.

WPULSE and VPULSE are typically used to signal energy accumulation of real (Wh) and reactive (VARh) energy. Tying WPULSE and VPULSE into the MPU interrupt system can support pulse counting.

XPULSE and YPULSE can be used to signal events such as sags and zero crossings of the mains voltage to the MPU. Tying these outputs into the MPU interrupt system relieves the MPU from having to read the *CESTATUS* register at every occurrence of the CE_BUSY interrupt in order to detect sag or zero crossing events.

Refer to 5.3 CE Interface Description on page 116 for additional information on setting up the device using the MPU firmware.

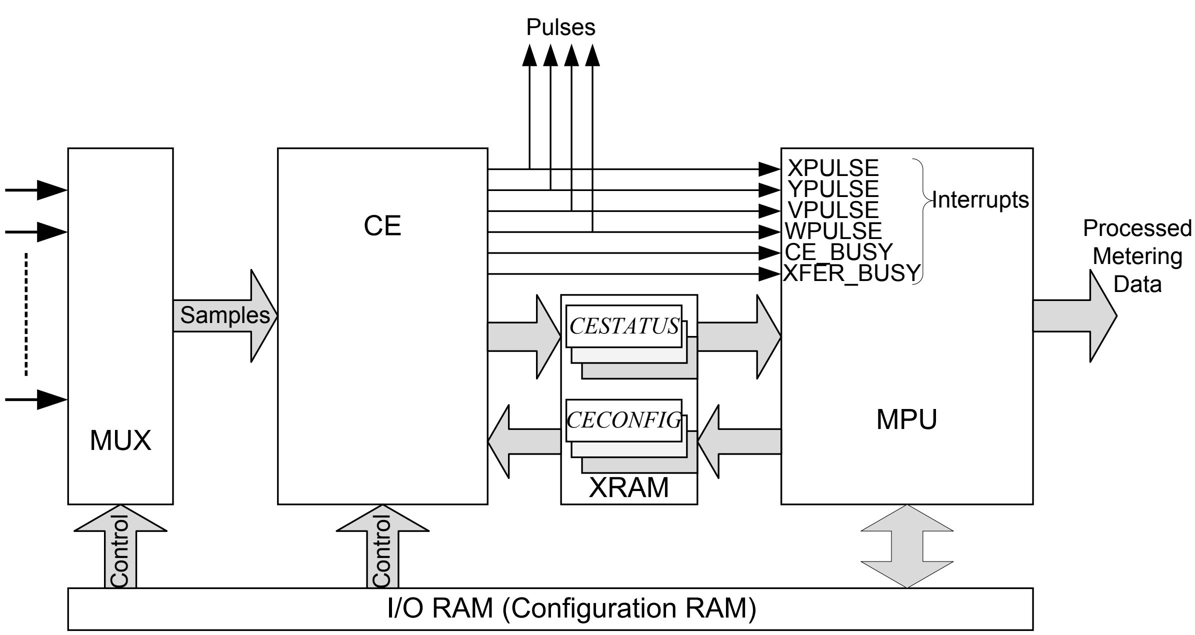


Figure 26: MPU/CE Data Flow

4 Application Information

4.1 Connecting 5 V Devices

All digital input pins of the 71M6543 are compatible with external 5 V devices. I/O pins configured as inputs do not require current-limiting resistors when they are connected to external 5 V devices.

4.2 Directly Connected Sensors

Figure 27 through Figure 30 show voltage-sensing resistive dividers, current-sensing current transformers (CTs) and current-sensing resistive shunts and how they are connected to the voltage and current inputs of the 71M6543. All input signals to the 71M6543 sensor inputs are voltage signals providing a scaled representation of either a sensed voltage or current.

CAUTION: The analog input pins of the 71M6543 are designed for sensors with low source impedance. RC filters with resistance values higher than those implemented in the Demo Boards must not be used. Refer to the Demo Board schematics for complete sensor input circuits and corresponding component values.

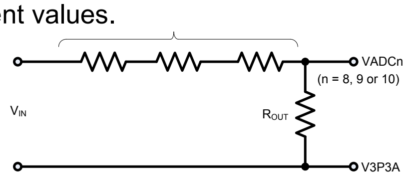


Figure 27: Resistive Voltage Divider (Voltage Sensing)

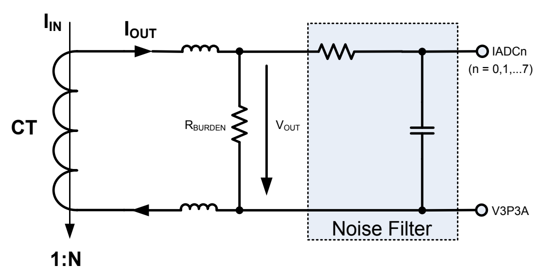


Figure 28. CT with Single-Ended Input Connection (Current Sensing)

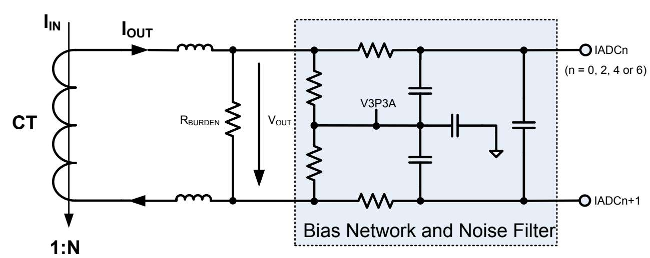


Figure 29: CT with Differential Input Connection (Current Sensing)

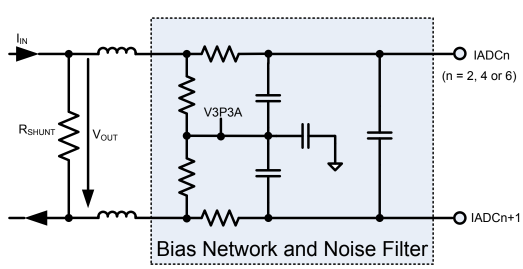


Figure 30: Differential Resistive Shunt Connections (Current Sensing)

4.3 Systems Using 71M6xx3 Isolated Sensors and Current Shunts

Figure 31 shows a typical connection for current shunt sensors; using the 71M6xx3 (polyphase) isolated sensors. Note that one shunt current sensor is connected without isolation, which is the neutral current sensor in this example (connected to pins IADC0-IADC1). Each 71M6xx3 device is electrically isolated by a low-cost pulse transformer. The 71M6543 current sensor inputs must be configured for remote sensor communications, as described in 2.2.8 71M6xx3 Isolated Sensor Interface (page 22). Flexible remapping using the I/O RAM registers *MUXn_SEL[3:0]* allows the sequence of analog input pins to be different from the standard configuration (a corresponding CE code must be used). See Figure 2 for the AFE configuration corresponding to Figure 31.

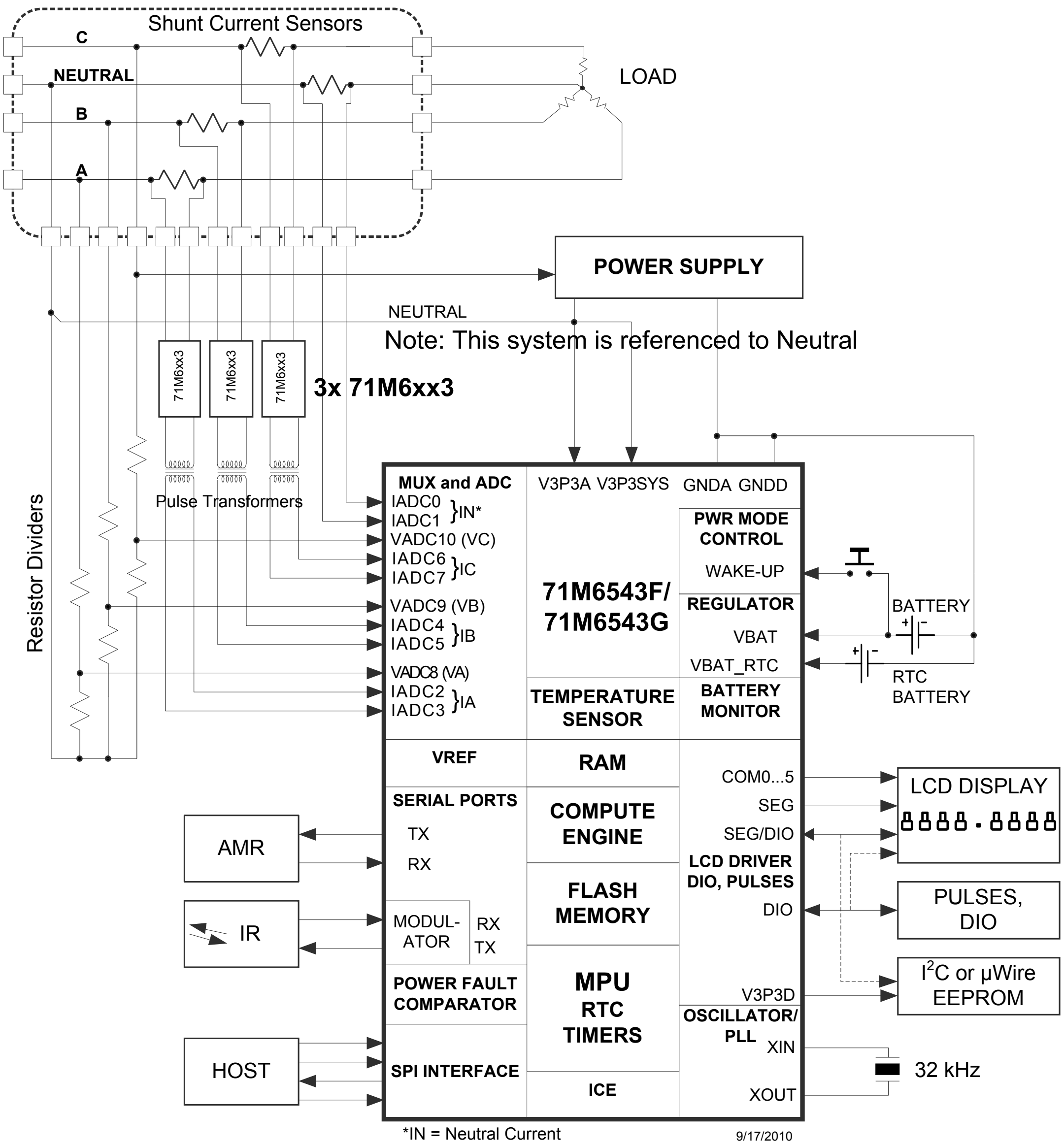


Figure 31: System Using Three-Remotes and One-Local (Neutral) Sensor

4.4 System Using Current Transformers

Figure 32 shows a polyphase system using four current transformers to support optional Neutral current sensing for anti-tamper purposes. The Neutral current sensing CT can be omitted if Neutral current sensing is not required. The system is referenced to Neutral (i.e., the Neutral rail is tied to V3P3A and V3P3SYS).

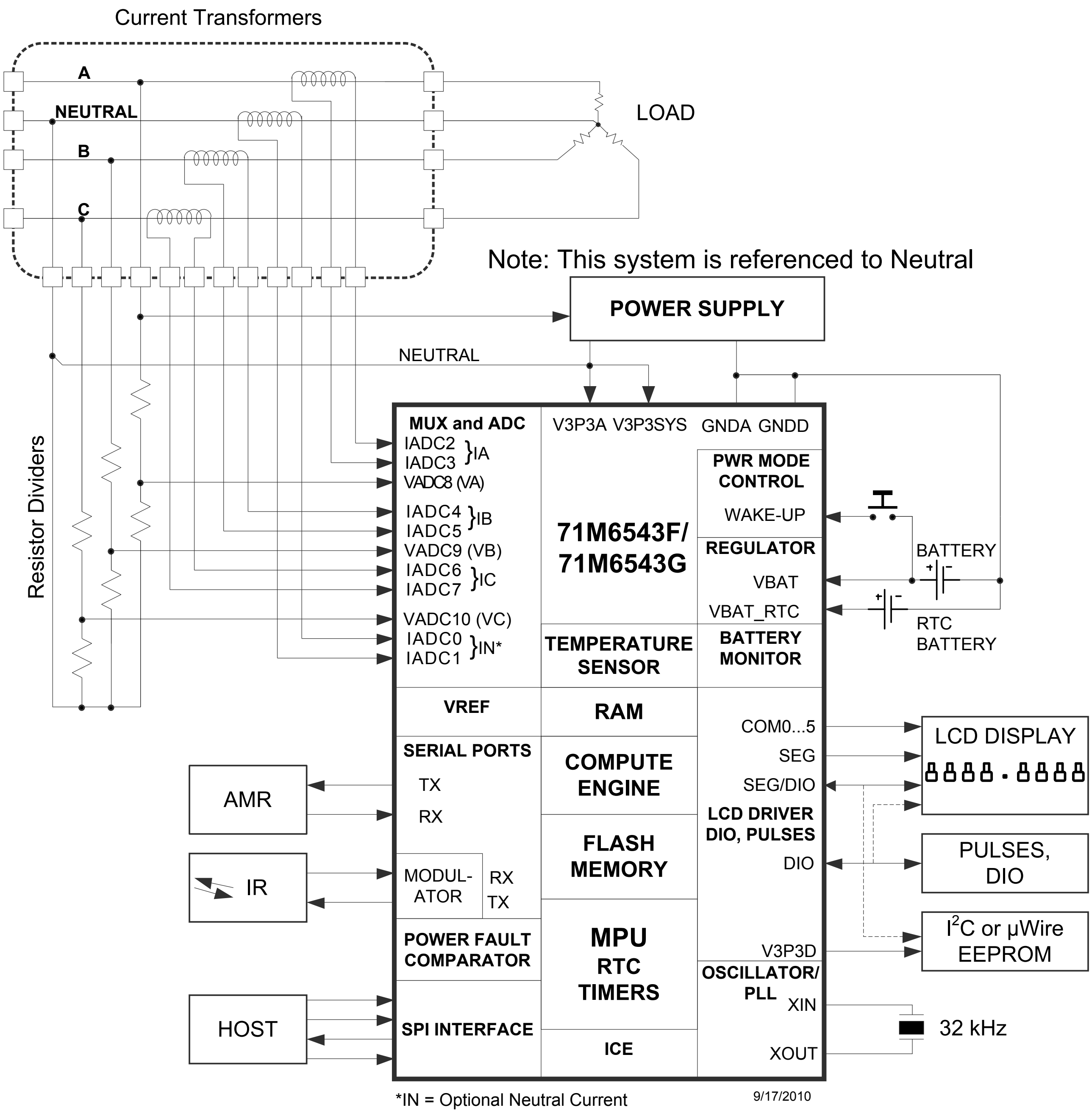


Figure 32. System Using Current Transformers

4.5 Metrology Temperature Compensation

4.5.1 Temperature Compensation

Since the VREF band-gap amplifier is chopper-stabilized, as set by the *CHOP_E[1:0] (I/O RAM 0x2106[3:2])* control field, the dc offset voltage, which is the most significant long-term drift mechanism in the voltage references (VREF), is automatically removed by the chopper circuit. Both the 71M6543 and the 71M6xx3 feature chopper circuits for their respective VREF voltage reference.

Since the variation in the bandgap reference voltage (VREF) is the major contributor to measurement error across temperatures, Maxim implements a two-step procedure to trim and characterize the VREF voltage reference during the device manufacturing process.

The first step in the process is applied to all parts (71M6543F, 71M6543G). In this first step, the reference voltage (VREF) is trimmed to a target value of 1.195V. During this trimming process, the *TRIMT[7:0]* (*I/O RAM 0x2309*) value is stored in non-volatile fuses. *TRIMT[7:0]* is trimmed to a value that results in minimum VREF variation with temperature.

For the 71M6543F and 71M6543G devices, the *TRIMT[7:0]* value can be read by the MPU during initialization in order to calculate parabolic temperature compensation coefficients suitable for each individual 71M6543F and 71M6543G device. The resulting temperature coefficient for VREF in the 71M6543F and 71M6543G is ±40 ppm/°C.

Considering the factory calibration temperature of VREF to be +22°C and the industrial temperature range (-40°C to +85°C), the VREF error at the temperature extremes for the 71M6543F and 71M6543G devices can be calculated as:

$$(85^o C - 22^o C) \cdot 40\, ppm/^o C = +2520\, ppm = +0.252\%$$

and

$$(-40^o C - 22^o C) \cdot 40\, ppm/^o C = -2480\, ppm = -0.248\%$$

The above calculation implies that both the voltage and the current measurements are individually subject to a theoretical maximum error of approximately ±0.25%. When the voltage sample and current sample are multiplied together to obtain the energy per sample, the voltage error and current error combine resulting in approximately ±0.5% maximum energy measurement error. However, this theoretical ±0.5% error considers only the voltage reference (VREF) as an error source. In practice, other error sources exist in the system. The principal remaining error sources are the current sensors (shunts or CTs) and their corresponding signal conditioning circuits, and the resistor voltage divider used to measure the voltage. The 71M6543F and 71M6543G devices should be used in Class 1% designs, to allow margin for the other error sources in the system.

The preceding discussion in this section also applies to the 71M6603 (0.5%), 71M6113 (0.5%) and 71M6203 (0.1%) remote sensors. Refer to the 71M6xxx Data Sheet for details.

4.5.2 Temperature Coefficients for the 71M6543F and 71M6543G

The equations provided below for calculating TC1 and TC2 apply to the 71M6543F and 71M6543G. In order to obtain TC1 and TC2, the MPU reads *TRIMT[7:0]* (*I/O RAM 0x2309*) and uses the TC1 and TC2 equations provided. PPMC and PPMC2 are then calculated from TC1 and TC2, as shown. The resulting tracking of the reference voltage (VREF) is within ±40 ppm/°C.

$$TC1(\mu V/°C) = 275 - 4.95 \cdot TRIMT$$

$$TC2(\mu V/°C^2) = -0.557 - 0.00028 \cdot TRIMT$$

$$PPMC = 22.4632 \cdot TC1$$

$$PPMC2 = 1150.116 \cdot TC2$$

See 4.5.4 and 4.5.5 below for further temperature compensation details.

4.5.3 Temperature Coefficients for the 71M6xx3

Refer to the 71M6xxx Data sheet for the equations that are applicable to each 71M6xx3 part number and the corresponding temperature coefficients.

4.5.4 Temperature Compensation for VREF and Shunt Sensors

This section discusses metrology temperature compensation for the meter designs where current shunt sensors are used in conjunction with the 71M6xx3 remote isolated sensors, as shown in Figure 31.

Sensors that are directly connected to the 71M6543 are affected by the voltage variation in the 71M6543 VREF due to temperature. On the other hand, shunt sensors that are connected to 71M6xx3 remote sensor are affected by the VREF in the 71M6xx3. The VREF in both the 71M6543 and 71M6xx3 can be compensated digitally using a second-order polynomial function of temperature. The 71M6543 and 71M6xx3 feature temperature sensors for the purposes of temperature compensating their corresponding VREF. The compensation computations must be implemented in MPU firmware.

Referring to Figure 31, the VADC8 (VA), VADC9 (VB) and VADC10 (VC) voltage sensors are always directly connected to the 71M6543. Thus, the precision of the voltage sensors is primarily affected by VREF in the 71M6543. The temperature coefficient of the resistors used to implement the voltage dividers for the voltage sensors (see Figure 27) determine the behavior of the voltage division ratio with respect to temperature. It is recommended to use resistors with low temperature coefficients, while forming the entire voltage divider using resistors belonging to the same technology family, in order to minimize the temperature dependency of the voltage division ratio. The resistors must also have suitable voltage ratings.

The 71M6543 also may have one local current shunt sensor that is connected directly to it via the IADC0-IADC1 input pins, and therefore this local current sensor is also affected by the VREF in the 71M6543. The shunt current sensor resistance has a temperature dependency, which also may require compensation, depending on the required accuracy class.

The IADC2-IADC3, IADC4-IADC5 and IADC6-IADC7 current sensors are isolated by the 71M6xx3 and depend on the VREF of the 71M6xx3, plus the variation of the corresponding remote shunt current sensor with temperature.

The MPU has the responsibility of computing the necessary sample gain compensation values required for each sensor channel based on the sensed temperature. Maxim provides demonstration code that implements the *GAIN_ADJx* compensation equation shown below. The resulting *GAIN_ADJx* values are stored by the MPU in five CE RAM locations *GAIN_ADJ0-GAIN_ADJ5* (*CE RAM 0x40-0x44*). The demonstration code thus provides a suitable implementation of temperature compensation, but other methods are possible in MPU firmware by utilizing the on-chip temperature sensors while storing the sample gain adjustment results in the CE RAM *GAIN_ADJx* storage locations for use by the CE. The demonstration code maintains five separate sets of *PPMC* and *PPMC2* coefficients and computes five separate *GAIN_ADJx* values based on the sensed temperature using the equation below:

$$GAIN\_ADJx = 16385 + \frac{10 \cdot TEMP\_X \cdot PPMC}{2^{14}} + \frac{100 \cdot TEMP\_X^2 \cdot PPMC2}{2^{23}}$$

The *GAIN_ADJx* values stored by the MPU in CE RAM are used by the CE to gain adjust (i.e., multiply) the sample in each corresponding sensor channel. A *GAIN_ADJx* value of 16,384 (i.e., 2^{14})corresponds to unity gain, while values less than 16,384 attenuate the samples and values greater than 16,384 amplify the samples.

In the above equation, *TEMP_X* is the deviation from nominal or calibration temperature expressed in multiples of 0.1 °C. The 10x and 100x factors seen in the above equation are due to 0.1 °C scaling of *TEMP_X*. For example, if the calibration (reference) temperature is 22 °C and the measured temperature is 27 °C, then 10**TEMP_X* = (27-22) x 10 = 50 (decimal), which represents a +5 °C deviation from 22°C. In the demonstration code, *TEMP_X* is calculated in the MPU from the *STEMP[10:0]* temperature sensor reading using the equation provided below and is scaled in 0.1°C units. See 2.5.5 71M6543 Temperature Sensor on page 53 for the equation to calculate temperature in degrees °C from the *STEMP[10:0]* value.

Table 66 shows the five *GAIN_ADJx* equation output storage locations and the voltage or current sensor channels for which they compensate for the 1 Local / 3 Remote configuration shown in Figure 31.

Table 66: GAIN_ADJn Compensation Channels (Figure 2, Figure 31, Table 1)

Gain Adjustment Output	CE RAM Address	Sensor Channel(s) (pin names)	Compensation For:
GAIN_ADJ0	0x40	VADC8 (VA) VADC9 (VB) VADC10 (VC)	VREF in 71M6543 and Voltage Divider Resistors
GAIN_ADJ1	0x41	IADC0-IADC1	VREF in 71M6543 and Shunt (Neutral Current)
GAIN_ADJ2	0x42	IADC2-IADC3	VREF in 71M6xx3 and Shunt (Phase A)
GAIN_ADJ3	0x43	IADC4-IADC5	VREF in 71M6xx3 and Shunt (Phase B)
GAIN_ADJ4	0x44	IADC6-IADC7	VREF in 71M6xx3 and Shunt (Phase C)

In the demonstration code, the shape of the temperature compensation second-order parabolic curve is determined by the values stored in the *PPMC* (1st order coefficient) and *PPMC2* (2nd order coefficient), which are typically setup by the MPU at initialization time from values that are stored in EEPROM.

To disable temperature compensation in the demonstration code, *PPMC* and *PPMC2* are both set to zero for each of the five *GAIN_ADJx* channels. To enable temperature compensation, the *PPMC* and *PPMC2* coefficients are set with values that match the expected temperature variation of the shunt current sensor (if required) and the corresponding VREF voltage reference (summed together).

The shunt sensor requires a second order polynomial compensation which is determined by the *PPMC* and *PPMC2* coefficients for the corresponding current measurement channel. The corresponding VREF voltage reference also requires the *PPMC* and *PPMC2* coefficients to match the second order temperature behavior of the voltage reference. The PPMC and PPMC2 values associated with the shunt and with the corresponding VREF are summed together to obtain the compensation coefficients for a given current-sensing channel (i.e., the 1st order PPMC coefficients are summed together, and the 2nd order PPMC2 coefficients are summed together).

In the 71M6543F and 71M6543G, the required VREF compensation coefficients *PPMC* and *PPMC2* are calculated from readable on-chip non-volatile fuses (see 4.5.2 Temperature Coefficients for the 71M6543F). These coefficients are designed to achieve ±40 ppm/°C for VREF in the 71M6543F and 71M6543G. PPMC and PPMC2 coefficients are similarly calculated for the 71M6xx3 remote sensor (see 4.5.3 Temperature Coefficients for the 71M6xx3).

For the current channels, to determine the *PPMC* and *PPMC2* coefficients for the shunt current sensors, the designer must either know the average temperature curve of the shunt from its manufacturer's data sheet or obtain these coefficients by laboratory characterization of the shunt used in the design.

4.5.5 Temperature Compensation of VREF and Current Transformers

This section discusses metrology temperature compensation for meter designs where Current Transformer (CT) sensors are used, as shown in Figure 32.

Sensors that are directly connected to the 71M6543 are affected by the voltage variation in the 71M6543 VREF due to temperature. The VREF in the 71M6543 can be compensated digitally using a second-order polynomial function of temperature. The 71M6543 features a temperature sensor for the purposes of temperature compensating its VREF. The compensation computations must be implemented in MPU firmware and written to the corresponding *GAIN_ADJx* CE RAM location.

Referring to Figure 32, the VADC8 (VA), VADC9 (VB) and VADC10 (VC) voltage sensors are directly connected to the 71M6543. Thus, the precision of the voltage sensors is primarily affected by VREF in the 71M6543. The temperature coefficient of the resistors used to implement the voltage dividers for the voltage sensors (see Figure 27) determine the behavior of the voltage division ratio with respect to temperature. It is recommended to use resistors with low temperature coefficients, while forming the entire voltage divider using resistors belonging to the same technology family, in order to minimize the temperature dependency of the voltage division ratio. The resistors must also have suitable voltage ratings.

The Current Transformers are directly connected to the 71M6543 and are therefore primarily affected by the VREF temperature dependency in the 71M6543. For best performance, it is recommended to use the differential signal conditioning circuit, as shown in Figure 29, to connect the CTs to the 71M6543. Current transformers may also require temperature compensation. The copper wire winding in the CT has dc resistance with a temperature coefficient, which makes the voltage delivered to the burden resistor temperature dependent, and the burden resistor also has a temperature coefficient. Thus, each CT sensor channel needs to compensate for the 71M6543 VREF, and optionally for the temperature dependency of the CT and its burden resistor depending on the required accuracy class.

The MPU has the responsibility of computing the necessary sample gain compensation values required for each sensor channel based on the sensed temperature. Maxim provides demonstration code that implements the *GAIN_ADJx* compensation equation shown below. The resulting *GAIN_ADJx* values are stored by the MPU in five CE RAM locations *GAIN_ADJ0-GAIN_ADJ5* (*CE RAM 0x40-0x44*). The demonstration code thus provides a suitable implementation of temperature compensation, but other methods are possible in MPU firmware by utilizing the on-chip temperature sensor while storing the sample gain adjustment results in the CE RAM *GAIN_ADJn* storage locations. The demonstration code maintains five separate sets of *PPMC* and *PPMC2* coefficients and computes five separate *GAIN_ADJn* values based on the sensed temperature using the equation below:

$$GAIN\_ADJx = 16385 + \frac{10 \cdot TEMP\_X \cdot PPMC}{2^{14}} + \frac{100 \cdot TEMP\_X^2 \cdot PPMC2}{2^{23}}$$

The *GAIN_ADJn* values stored by the MPU in CE RAM are used by the CE to gain adjust (i.e., multiply) the sample in each corresponding sensor channel. A *GAIN_ADJx* value of 16,384 (i.e., 2^{14})corresponds to unity gain, while values less than 16,384 attenuate the samples and values greater than 16,384 amplify the samples.

In the above equation, *TEMP_X* is the deviation from nominal or calibration temperature expressed in multiples of 0.1 °C. The 10x and 100x factors seen in the above equation are due to 0.1 °C scaling of *TEMP_X*. For example, if the calibration (reference) temperature is 22 °C and the measured temperature is 27 °C, then 10**TEMP_X* = (27-22) x 10 = 50 (decimal), which represents a +5 °C deviation from 22 °C. In the demonstration code, *TEMP_X* is calculated in the MPU from the *STEMP[10:0]* temperature sensor reading using the equation provided below and is scaled in 0.1°C units. See 2.5.5 71M6543 Temperature Sensor on page 53 for the equation to calculate temperature in °C from the *STEMP[10:0]* reading.

Table 67 shows the five *GAIN_ADJx* equation output storage locations and the voltage or current measurements for which they compensate.

Table 67: GAIN_ADJx Compensation Channels (Figure 3, Figure 32, Table 2)

Gain Adjustment Output	CE RAM Address	Sensor Channel(s) (pin names)	Compensation For:
GAIN_ADJ0	0x40	VADC8 (VA) VADC9 (VB) VADC10 (VC)	VREF in 71M6543 and Voltage Divider Resistors
GAIN_ADJ1	0x41	IADC0-IADC1	VREF in 71M6543, CT and Burden Resistor (Neutral Current)
GAIN_ADJ2	0x42	IADC2-IADC3	VREF in 71M6543, CT and Burden Resistor (Phase A)
GAIN_ADJ3	0x43	IADC4-IADC5	VREF in 71M6543, CT and Burden Resistor (Phase B)
GAIN_ADJ4	0x44	IADC6-IADC7	VREF in 71M6543, CT and Burden Resistor (Phase C)

In the demonstration code, the shape of the temperature compensation second-order parabolic curve is determined by the values stored in the *PPMC* (1st order coefficient) and *PPMC2* (2nd order coefficient), which are typically setup by the MPU at initialization time from values that are stored in EEPROM.

To disable temperature compensation in the demonstration code, *PPMC* and *PPMC2* are both set to zero for each of the five *GAIN_ADJx* channels. To enable temperature compensation, the *PPMC* and *PPMC2* coefficients are set with values that match the expected VREF temperature variation and optionally the corresponding sensor circuit (i.e., the CT and burden resistor for current channels or the resistor divider network for the voltage channels).

In the 71M6543F and 71M6543G, the required VREF compensation coefficients *PPMC* and *PPMC2* are calculated from readable on-chip non-volatile fuses (see 4.5.2Temperature Coefficients for the 71M6543F). These coefficients are designed to achieve ±40 ppm/°C for VREF.

4.6 Connecting I²C EEPROMs

I²C EEPROMs or other I²C compatible devices should be connected to the DIO pins SEGDIO2 and SEGDIO3, as shown in Figure 33.

Pullup resistors of roughly 10 kΩ to V3P3D (to ensure operation in BRN mode) should be used for both SDCK and SDATA signals. The *DIO_EEX* (*I/O RAM 0x2456[7:6]*) field must be set to 01 in order to convert the DIO pins SEGDIO2 and SEGDIO3 to I²C pins SCL and SDATA.

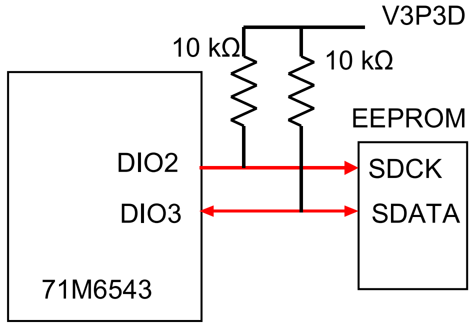


Figure 33: I²C EEPROM Connection

4.7 Connecting Three-Wire EEPROMs

µWire EEPROMs and other compatible devices should be connected to the DIO pins SEGDIO2 and SEGDIO3, as described in 2.5.11 EEPROM Interface on page 65.

4.8 UART0 (TX/RX)

The UART0 RX pin should be pulled down by a 10 kΩ resistor and additionally protected by a 100 pF ceramic capacitor, as shown in Figure 34.

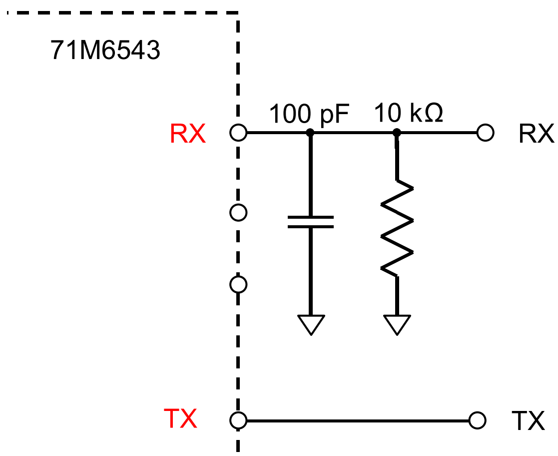


Figure 34: Connections for UART0

4.9 Optical Interface (UART1)

The OPT_TX and OPT_RX pins can be used for a regular serial interface (by connecting a RS_232 transceiver for example), or they can be used to directly operate optical components (for example, an infrared diode and phototransistor implementing a FLAG interface). Figure 35 shows the basic connections for UART1. The OPT_TX pin becomes active when the control field *OPT_TXE* (*I/O RAM 0x2456[3:2]*) is set to 01.

The polarity of the OPT_TX and OPT_RX pins can be inverted with the configuration bits, *OPT_TXINV (I/O RAM 0x2456[0])* and *OPT_RXINV (I/O RAM 0x2457[1])*, respectively.

The OPT_TX output may be modulated at 38 kHz when system power is present. Modulation is not available in BRN mode. The *OPT_TXMOD* bit (*I/O RAM 0x2456[1]*) enables modulation. The duty cycle is controlled by *OPT_FDC[1:0] (I/O RAM 0x2457[5:4])*, which can select 50%, 25%, 12.5%, and 6.25% duty cycle. A 6.25% duty cycle means OPT_TX is low for 6.25% of the period. The OPT_RX pin uses digital signal thresholds. It may need an analog filter when receiving modulated optical signals.

With modulation, an optical emitter can be operated at higher current than nominal, enabling it to increase the distance along the optical path.

If operation in BRN mode is desired, the external components should be connected to V3P3D. However, it is recommended to limit the current to a few mA.

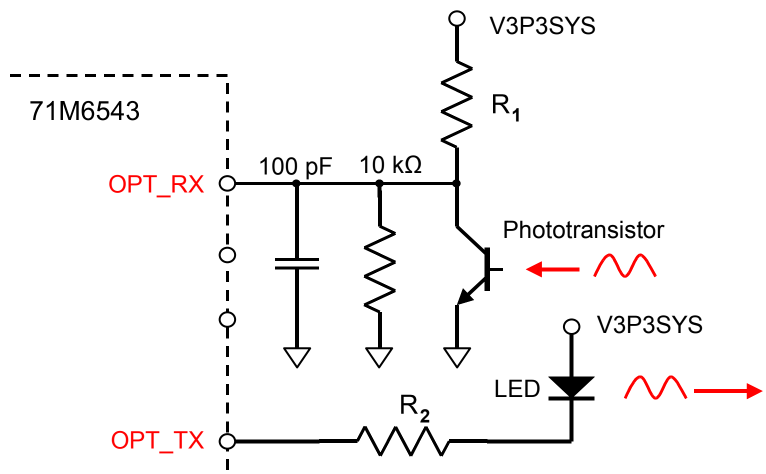


Figure 35: Connection for Optical Components

4.10 Connecting the Reset Pin

Even though a functional meter does not necessarily need a reset switch, it is useful to have a reset pushbutton for prototyping as shown in Figure 36, left side. The RESET signal may be sourced from V3P3SYS (functional in MSN mode only), V3P3D (MSN and BRN modes), or VBAT (all modes, if a battery is present), or from a combination of these sources, depending on the application.

For a production meter, the RESET pin should be protected by the by the external components shown in Figure 36, right side. R1 should be in the range of 100Ω and mounted as closely as possible to the IC.

Since the 71M6543 generates its own power-on reset, a reset button or circuitry, as shown in Figure 36, is only required for test units and prototypes.

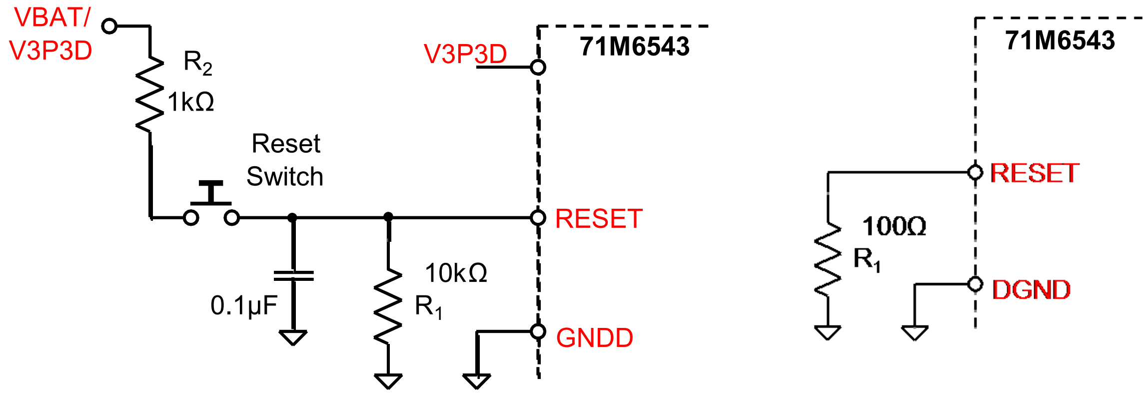


Figure 36: External Components for the RESET Pin: Push-Button (Left), Production Circuit (Right)

4.11 Connecting the Emulator Port Pins

Even when the emulator is not used, small shunt capacitors to ground (22 pF) should be used for protection from EMI as illustrated in Figure 37. Production boards should have the ICE_E pin connected to ground.

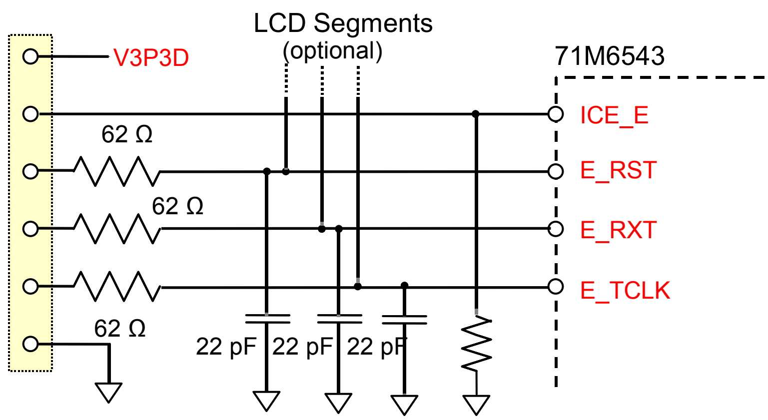


Figure 37: External Components for the Emulator Interface

4.12 Flash Programming

4.12.1 Flash Programming via the ICE Port

Operational or test code can be programmed into the flash memory using either an in-circuit emulator or the Flash Programmer Module (TFP-2) available from Maxim. The flash programming procedure uses the E_RST, E_RXTX, and E_TCLK pins.

4.12.2 Flash Programming via the SPI Port

It is possible to erase, read and program the flash memory of the 71M6543 via the SPI port. See 2.5.12 for a detailed description.

4.13 MPU Demonstration Code

All application-specific MPU functions mentioned in 4 Application Information are featured in the demonstration C source code supplied by Maxim. The code is available as part of the Demonstration Kit for the 71M6543. The Demonstration Kits come with the 71M6543 preprogrammed with demonstration firmware and mounted on a functional sample meter Demo Board. The Demo Boards allow for quick and efficient evaluation of the IC without having to write firmware or having to supply an in-circuit emulator (ICE).

4.14 Crystal Oscillator

The oscillator of the 71M6543 drives a standard 32.768 kHz watch crystal. The oscillator has been designed specifically to handle these crystals and is compatible with their high impedance and limited power handling capability. The oscillator power dissipation is very low to maximize the lifetime of any battery backup device attached to the VBAT_RTC pin.

Board layouts with minimum capacitance from XIN to XOUT require less battery current. Good layouts have XIN and XOUT shielded from each other and also keep the XIN and XOUT traces short and away from LCD and digital signals.

Since the oscillator is self-biasing, an external resistor must not be connected across the crystal.

4.15 Meter Calibration

Once the 71M6543 energy meter device has been installed in a meter system, it must be calibrated. A complete calibration includes the following:

- Establishment of the reference temperature for factory calibration (e.g., typically 22 °C).
- Calibration of the metrology section, i.e., calibration for errors of the current sensors, voltage dividers and signal conditioning components as well as of the internal reference voltage (VREF) at the reference temperature (e.g., typically 22 °C).
- Calibration of the oscillator frequency using the *RTCA_ADJ* register (*I/O RAM 0x2504*).

The metrology section can be calibrated using the gain and phase adjustment factors accessible to the CE. The gain adjustment is used to compensate for tolerances of components used for signal conditioning, especially the resistive components. Phase adjustment is provided to compensate for phase shifts introduced by the current sensors or by the effects of reactive power supplies.

Due to the flexibility of the MPU firmware, any calibration method, such as calibration based on energy, or current and voltage can be implemented. It is also possible to implement segment-wise calibration (depending on current range).

The 71M6543 supports common industry standard calibration techniques, such as single-point (energy-only), multi-point (energy, Vrms, Irms), and auto-calibration.

Maxim provides a calibration spreadsheet file to facilitate the calibration process. Contact your Maxim representative to obtain a copy of the latest calibration spreadsheet file for the 71M6543.

5 Firmware Interface

5.1 I/O RAM Map –Functional Order

In Table 68 and Table 69, unimplemented (U) and reserved (R) bits are shaded in light gray. Unimplemented bits are ident
Unimplemented bits have no memory storage, writing them has no effect, and reading them always returns zero. Reserved
an 'R', and must always be written with a zero. Writing values other than zero to reserved bits may have undesirable side e
avoided. Non-volatile bits are shaded in dark gray. Non-volatile bits are backed-up during power failures if the system inclu
to the VBAT pin.

The I/O RAM locations listed in Table 68 have sequential addresses to facilitate reading by the MPU (e.g., in order to verify
I/O RAM locations are usually modified only at boot-up. The addresses shown in Table 68 are an alternative sequential ad
from Table 69 which are used throughout this document. For instance, *EQU[2:0]* can be accessed at *I/O RAM 0x2000[7:5]*
0x2106[7:5].

Table 68: I/O RAM Map – Functional Order, Basic Configuration

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	B
CE6	2000	*EQU[2:0]*			*U*	*CHOP_E[1:0]*		*RT*
CE5	2001	*U*			*SUM_SAMPS[12:8]*			
CE4	2002	*SUM_SAMPS[7:0]*						
CE3	2003	*U*	*CE_LCTN[6/5:0]*					
CE2	2004	*PLS_MAXWIDTH[7:0]*						
CE1	2005	*PLS_INTERVAL[7:0]*						
CE0	2006	*DIFF6_E*	*DIFF4_E*	*DIFF2_E*	*DIFF0_E*	*RFLY_DIS*	*FIR_LEN[1:0]*	
RCE0	2007	*CHOPR[1:0]*		*RMT6_E*	*RMT4_E*	*RMT2_E*	*TMUX*	
RTMUX	2008	*U*	*TMUXR4[2:0]*			*U*	*TMUX*	
FOVRD	2009	*U*	*U*	*R*	*U*	*U*	*U*	
MUX5	200A	*MUX_DIV[3:0]*				*MUX10_SEL*		
MUX4	200B	*MUX9_SEL*				*MUX8_SEL*		
MUX3	200C	*MUX7_SEL*				*MUX6_SEL*		
MUX2	200D	*MUX5_SEL*				*MUX4_SEL*		
MUX1	200E	*MUX3_SEL*				*MUX2_SEL*		
MUX0	200F	*MUX1_SEL*				*MUX0_SEL*		
TEMP	2010	*TEMP_BSEL*	*TEMP_PWR*	*OSC_COMP*	*TEMP_BAT*	*TBYTE_BUSY*	*TEMP_*	
LCD0	2011	*LCD_E*	*LCD_MODE[2:0]*			*LCD_ALLCOM*	*LCD_Y*	
LCD1	2012	*LCD_VMODE[1:0]*		*LCD_BLNKMAP23[5:0]*				

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	B
LCD2	2013	*LCD_BAT*	*R*	*LCD_BLNKMAP22[5:0]*				
LCD_MAP6	2014	*LCD_MAP[55:48]*						
LCD_MAP5	2015	*LCD_MAP[47:40]*						
LCD_MAP4	2016	*LCD_MAP[39:32]*						
LCD_MAP3	2017	*LCD_MAP[31:24]*						
LCD_MAP2	2018	*LCD_MAP[23:16]*						
LCD_MAP1	2019	*LCD_MAP[15:8]*						
LCD_MAP0	201A	*LCD_MAP[7:0]*						
DIO_R5	201B	*U*	*U*	*U*	*U*	*U*	*DIO_*	
DIO_R4	201C	*U*	*DIO_R11[2:0]*			*U*	*DIO_*	
DIO_R3	201D	*U*	*DIO_R9[2:0]*			*U*	*DIO_*	
DIO_R2	201E	*U*	*DIO_R7[2:0]*			*U*	*DIO_*	
DIO_R1	201F	*U*	*DIO_R5[2:0]*			*U*	*DIO_*	
DIO_R0	2020	*U*	*DIO_R3[2:0]*			*U*	*DIO_*	
DIO0	2021	*DIO_EEX[1:0]*		*U*	*U*	*OPT_TXE[1:0]*		*OPT_*
DIO1	2022	*DIO_PW*	*DIO_PV*	*OPT_FDC[1:0]*		*U*	*OPT_RXDIS*	*OPT_*
DIO2	2023	*DIO_PX*	*DIO_PY*	*U*	*U*	*U*	*U*	
INT1_E	2024	*EX_EEX*	*EX_XPULSE*	*EX_YPULSE*	*EX_RTCT*	*U*	*EX_RTC1M*	*EX_*
INT2_E	2025	*EX_SPI*	*EX_WPULSE*	*EX_VPULSE*				
WAKE_E	2026				*EW_RX*	*EW_PB*	*EW_DIO4*	*EW_*
SFMM	2080	*SFMM[7:0]**						
SFMS	2081	*SFMS[7:0]**						

Notes:
**SFMM* and *SFMS* are accessible only through the SPI slave port. See 2.5.1.1 Flash Memory for details.

Table 69 lists bits and registers that may have to be accessed on a frequent basis. Reserved bits have lighter gray backgr
bits have a darker gray background.

Table 69: I/O RAM Map – Functional Order

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	B
CE and ADC								
MUX5	2100	*MUX_DIV[3:0]*				*MUX10_SEL[3:*		
MUX4	2101	*MUX9_SEL[3:0]*				*MUX8_SEL[3:0*		
MUX3	2102	*MUX7_SEL[3:0]*				*MUX6_SEL[3:0*		
MUX2	2103	*MUX5_SEL[3:0]*				*MUX4_SEL[3:0*		
MUX1	2104	*MUX3_SEL[3:0]*				*MUX2_SEL[3:0*		
MUX0	2105	*MUX1_SEL[3:0]*				*MUX0_SEL[3:0*		
CE6	2106	*EQU[2:0]*			*U*	*CHOP_E[1:0]*	*RTM_E*	
CE5	2107	*U*			*SUM_SAMPS[12:8]*			
CE4	2108	*SUM_SAMPS[7:0]*						
CE3	2109	*U*	*CE_LCTN[6:0] (71M6543G), CE_LCTN[5:0] (71M6543F)*					
CE2	210A	*PLS_MAXWIDTH[7:0]*						
CE1	210B	*PLS_INTERVAL[7:0]*						
CE0	210C	*DIFF6_E*	*DIFF4_E*	*DIFF2_E*	*DIFF0_E*	*RFLY_DIS*	*FIR_LEN[1:0]*	
RTM0	210D	*U*	*U*	*U*	*U*	*U*	*U*	
RTM0	210E	*RTM0[7:0]*						
RTM1	210F	*RTM1[7:0]*						
RTM2	2110	*RTM2[7:0]*						
RTM3	2111	*RTM3[7:0]*						
CLOCK GENERATION								
CKGN	2200	*U*	*U*	*ADC_DIV*	*PLL_FAST*	*RESET*	*MPU_*	
VREF TRIM FUSES								
TRIMT	2309	*TRIMT[7:0]*						
LCD/DIO								
LCD0	2400	*LCD_E*	*LCD_MODE[2:0]*			*LCD_ALLCOM*	*LCD_Y*	
LCD1	2401	*LCD_VMODE[1:0]*		*LCD_BLNKMAP23[5:0]*				
LCD2	2402	*LCD_BAT*	*R*	*LCD_BLNKMAP22[5:0]*				
LCD_MAP6	2405	*LCD_MAP[55:48]*						
LCD_MAP5	2406	*LCD_MAP[47:40]*						
LCD_MAP4	2407	*LCD_MAP[39:32]*						
LCD_MAP3	2408	*LCD_MAP[31:24]*						

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	B
LCD_MAP2	2409	*LCD_MAP[23:16]*						
LCD_MAP1	240A	*LCD_MAP[15:8]*						
LCD_MAP0	240B	*LCD_MAP[7:0]*						
LCD4	240C	*U*	*U*	*U*	*U*	*U*	*LCD_RST*	*LCD_*
LCD_DAC	240D	*U*	*U*	*U*	*LCD_DAC[4:0]*			
SEGDIO0	2410	*U*	*U*	*LCD_SEG0[5:0]*				
…	…	*U*	*U*	...				
SEGDIO15	241F	*U*	*U*	*LCD_SEG15[5:0]*				
SEGDIO16	2420	*U*	*U*	*LCD_SEGDIO16[5:0]*				
…	…	*U*	*U*	...				
SEGDIO45	243D	*U*	*U*	*LCD_SEGDIO45[5:0]*				
SEGDIO46	243E	*U*	*U*	*LCD_SEG46[5:0]*				
…	…	*U*	*U*	...				
SEGDIO50	2442	*U*	*U*	*LCD_SEG50[5:0]*				
SEGDIO51	2443	*U*	*U*	*LCD_SEGDIO51[5:0]*				
…	…	*U*	*U*	...				
SEGDIO55	2447	*U*	*U*	*LCD_SEGDIO55[5:0]*				
DIO_R5	2450	*U*	*R*	*R*	*R*	*U*	*DIO_R*	
DIO_R4	2451	*U*	*DIO_R11[2:0]*			*U*	*DIO_I*	
DIO_R3	2452	*U*	*DIO_R9[2:0]*			*U*	*DIO_*	
DIO_R2	2453	*U*	*DIO_R7[2:0]*			*U*	*DIO_*	
DIO_R1	2454	*U*	*DIO_R5[2:0]*			*U*	*DIO_*	
DIO_R0	2455	*U*	*DIO_R3[2:0]*			*U*	*DIO_*	
DIO0	2456	*DIO_EEX[1:0]*		*U*	*U*	*OPT_TXE[1:0]*		*OPT_*
DIO1	2457	*DIO_PW*	*DIO_PV*	*OPT_FDC[1:0]*		*U*	*OPT_RXDIS*	*OPT_*
DIO2	2458	*DIO_PX*	*DIO_PY*	*U*	*U*	*U*	*U*	
NV BITS								
SPARENV	2500	*U*	*U*	*U*	*U*	*R*		
FOVRD	2501	*U*	*U*	*R*	*U*	*U*	*U*	
TMUX	2502	*U*	*U*	*TMUX[5:0]*				
TMUX2	2503	*U*	*U*	*U*	*TMUX2[4:0]*			
RTC1	2504	*U*	*RTCA_ADJ[6:0]*					
71M6xx3 Interface								

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	B
REMOTE2	2602	*RMT_RD[15:8]*						
REMOTE1	2603	*RMT_RD[7:0]*						
RBITS								
INT1_E	2700	*EX_EEX*	*EX_XPULSE*	*EX_YPULSE*	*EX_RTCT*	*U*	*EX_RTC1M*	*EX_*
INT2_E	2701	*EX_SPI*	*EX_WPULSE*	*EX_VPULSE*	*U*	*U*	*U*	
SECURE	2702	*FLSH_UNLOCK[3:0]*				*R*	*FLSH_RDE*	*FLSI*
Analog0	2704	*VREF_CAL*	*VREF_DIS*	*PRE_E*	*ADC_E*	*BCURR*	*SPAR*	
VERSION	2706	*VERSION[7:0]*						
INTBITS	2707	*U*	*INT6*	*INT5*	*INT4*	*INT3*	*INT2*	*I*
FLAG0	SFR E8	*IE_EEX*	*IE_XPULSE*	*IE_YPULSE*	*IE_RTCT*	*U*	*IE_RTC1M*	*IE_*
FLAG1	SFR F8	*IE_SPI*	*IE_WPULSE*	*IE_VPULSE*	*U*	*U*	*U*	
STAT	SFR F9	*U*	*U*	*U*	*PLL_OK*	*U*	*VSTA*	
REMOTE0	SFR FC	*U*	*PERR_RD*	*PERR_WR*	*RCMD[4:0]*			
SPI1	SFR FD	*SPI_CMD[7:0]*						
SPI0	2708	*SPI_STAT[7:0]*						
RCE0	2709	*CHOPR[1:0]*		*RMT6_E*	*RMT4_E*	*RMT2_E*	*TMUX*	
RTMUX	270A	*U*	*TMUXR4[2:0]*			*U*	*TMUX*	
DIO3	270C	*U*	*U*	*PORT_E*	*SPI_E*	*SPI_SAFE*	*U*	
NV RAM and RTC								
NVRAMxx	2800-287F	*NVRAM[0] – NVRAM[7F]* – Direct Access						
WAKE	2880	*WAKE_TMR[7:0]*						
STEMP1	2881	*STEMP[10:3]*						
STEMP0	2882	*STEMP[2:0]*			*U*	*U*	*U*	
BSENSE	2885	*BSENSE[7:0]*						
LKPADDR	2887	*LKPAUTOI*	*LKPADDR[6:0]*					
LKPDATA	2888	*LKPDAT[7:0]*						
LKPCTRL	2889	*U*	*U*	*U*	*U*	*U*	*U*	*LK*
RTC0	2890	*RTC_WR*	*RTC_RD*	*U*	*RTC_FAIL*	*U*	*U*	
RTC2	2892	*RTC_SBSC[7:0]*						
RTC3	2893	*U*	*U*	*RTC_SEC[5:0]*				
RTC4	2894	*U*	*U*	*RTC_MIN[5:0]*				
RTC5	2895	*U*	*U*	*U*	*RTC_HR[4:0]*			

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	B
RTC6	2896	*U*	*U*	*U*	*U*	*U*	*RTC_*	
RTC7	2897	*U*	*U*	*U*	*RTC_DATE[4:0]*			
RTC8	2898	*U*	*U*	*U*	*U*	*RTC_MO[3:0]*		
RTC9	2899	*RTC_YR[7:0]*						
RTC10	289B	*U*	*U*	*U*	*U*	*U*	*RTC_*	
RTC11	289C	*RTC_P[13:6]*						
RTC12	289D	*RTC_P[5:0]*						
RTC13	289E	*U*	*U*	*RTC_TMIN[5:0]*				
RTC14	289F	*U*	*U*	*U*	*RTC_THR[4:0]*			
TEMP	28A0	*TEMP_BSEL*	*TEMP_PWR*	*OSC_COMP*	*TEMP_BAT*	*TBYTE_BUSY*	*TEMP_*	
WF1	28B0	*WF_CSTART*	*WF_RST*	*WF_RSTBIT*	*WF_OVF*	*WF_ERST*	*WF_BADVDD*	
WF2	28B1	*U*	*U*	*WF_TMR*	*WF_RX*	*WF_PB*	*WF_DIO4*	*WF_*
MISC	28B2	*SLEEP*	*LCD_ONLY*	*WAKE_ARM*	*U*	*U*	*U*	
WAKE_E	28B3	*U*	*U*	*U*	*EW_RX*	*EW_PB*	*EW_DIO4*	*EW_*
WDRST	28B4	*WD_RST*	*TEMP_START*	*U*	*U*	*U*	*U*	
MPU PORTS								
PORT3	SFR B0	*DIO_DIR[15:12]*				*DIO[15:12]*		
PORT2	SFR A0	*DIO_DIR[11:8]*				*DIO[11:8]*		
PORT1	SFR 90	*DIO_DIR[7:4]*				*DIO[7:4]*		
PORT0	SFR 80	*DIO_DIR[3:0]*				*DIO[3:0]*		
FLASH								
ERASE	SFR 94	*FLSH_ERASE[7:0]*						
FLSHCTL	SFR B2	*PREBOOT*	*SECURE*	*U*	*U*	*FLSH_PEND*	*FLSH_PSTWR*	*FLSH*
FL_BANK	SFR B6	*U*	*U*	*U*	*U*	*U*	*U*	
PGADR	SFR B7	*FLSH_PGADR[5:0]*						
I^2C								
EEDATA	SFR 9E	*EEDATA[7:0]*						
EECTRL	SFR 9F	*EECTRL[7:0]*						

5.2 I/O RAM Map – Alphabetical Order

Table 70 lists I/O RAM bits and registers in alphabetical order.

Bits with a write direction (W in column Dir) are written by the MPU into configuration RAM. Typically, they are initially stor copied to the configuration RAM by the MPU. Some of the more frequently programmed bits are mapped to the MPU SFR remaining bits are mapped to the address space 0x2XXX. Bits with R (read) direction can be read by the MPU. Column describe the bit values upon reset and wake, respectively. No entry in one of these columns means the bit is either read-c NV supply and is not initialized. Write-only bits return zero when they are read.

Locations that are shaded in grey are non-volatile (i.e., battery-backed).

Table 70: I/O RAM Map – Alphabetical Order

<table>
<tr><th>Name</th><th>Location</th><th>Rst</th><th>Wk</th><th>Dir</th><th>Description</th></tr>
<tr><td>ADC_E</td><td>2704[4]</td><td>0</td><td>0</td><td>R/W</td><td>Enables ADC and VREF. When disabled, reduces bias current.</td></tr>
<tr><td>ADC_DIV</td><td>2200[5]</td><td>0</td><td>0</td><td>R/W</td><td>ADC_DIV controls the rate of the ADC and FIR clocks.
The ADC_DIV setting determines whether MCK is divided by 4 or 8
0 = MCK/4
1 = MCK/8
The resulting ADC and FIR clock is as shown below.<table><tr><th></th><th>PLL_FAST = 0</th><th>PLL_FAST</th></tr><tr><td>MCK</td><td>6.291456 MHz</td><td>19.660800 M</td></tr><tr><td>ADC_DIV = 0</td><td>1.572864 MHz</td><td>4.9152 MH</td></tr><tr><td>ADC_DIV = 1</td><td>0.786432 MHz</td><td>2.4576 MH</td></tr></table></td></tr>
<tr><td>BCURR</td><td>2704[3]</td><td>0</td><td>0</td><td>R/W</td><td>Connects a 100 μA load to the battery selected by TEMP_BSEL.</td></tr>
<tr><td>BSENSE[7:0]</td><td>2885[7:0]</td><td>–</td><td>–</td><td>R</td><td>The result of the battery measurement.
See 2.5.7 71M6543 Battery Monitor on page 56.</td></tr>
<tr><td>CE_E</td><td>2106[0]</td><td>0</td><td>0</td><td>R/W</td><td>CE enable.</td></tr>
<tr><td>CE_LCTN[6:0]</td><td>2109[6:0]</td><td>31</td><td>31</td><td>R/W</td><td>CE program location. The starting address for the CE program is 1
(CE_LCTN[6:0], 2109[6:0] for 71M6543G)
(CE_LCTN[5:0], 2109[5:0] for 71M6543F)</td></tr>
<tr><td>CHIP_ID[15:8]
CHIP_ID[7:0]</td><td>2300[7:0]
2301[7:0]</td><td>0
0</td><td>0
0</td><td>R
R</td><td>These bytes contain the chip identification as shown below.<table><tr><th></th><th>CHIP_ID[15:8]</th><th>CHIP_ID[7:0]</th></tr><tr><td>71M6543F</td><td>0x04</td><td>0x10</td></tr><tr><td>71M6543G</td><td>0x05</td><td>0x10</td></tr></table></td></tr>
<tr><td>CHOP_E[1:0]</td><td>2106[3:2]</td><td>0</td><td>0</td><td>R/W</td><td>Chop enable for the reference bandgap circuit. The value of CHOP rising edge of the internal MUXSYNC signal according to the value
00 = toggle[1] 01 = positive 10 = reversed 11 = toggle
[1]except at the mux sync edge at the end of an accumulation interva</td></tr>
</table>

<table>
<tr><th>Name</th><th>Location</th><th>Rst</th><th>Wk</th><th>Dir</th><th>Description</th></tr>
<tr><td>CHOPR[1:0]</td><td>2709[7:6]</td><td>00</td><td>00</td><td>R/W</td><td>The CHOP settings for the remote sensor.
00 = Auto chop. Change every MUX frame.
01 = Positive
10 = Negative
11 = Auto chop (same as 00)</td></tr>
<tr><td>DIFF0_E</td><td>210C[4]</td><td>0</td><td>0</td><td>R/W</td><td>Enables IADC0-IADC1 differential configuration.</td></tr>
<tr><td>DIFF2_E</td><td>210C[5]</td><td>0</td><td>0</td><td>R/W</td><td>Enables IADC2-IADC3 differential configuration.</td></tr>
<tr><td>DIFF4_E</td><td>210C[6]</td><td>0</td><td>0</td><td>R/W</td><td>Enables IADC4-IADC5 differential configuration.</td></tr>
<tr><td>DIFF6_E</td><td>210C[7]</td><td>0</td><td>0</td><td>R/W</td><td>Enables IADC6-IADC7 differential configuration.</td></tr>
<tr><td>DIO_R2[2:0]
DIO_R3[2:0]
DIO_R4[2:0]
DIO_R5[2:0]
DIO_R6[2:0]
DIO_R7[2:0]
DIO_R8[2:0]
DIO_R9[2:0]
DIO_R10[2:0]
DIO_R11[2:0]
DIO_RPB[2:0]</td><td>2455[2:0]
2455[6:4]
2454[2:0]
2454[6:4]
2453[2:0]
2453[6:4]
2452[2:0]
2452[6:4]
2451[2:0]
2451[6:4]
2450[2:0]</td><td>0
0
0
0
0
0
0
0
0
0
0</td><td>–</td><td>R/W</td><td>Connects PB and dedicated I/O pins DIO2 through DIO11 to intern
than one input is connected to the same resource, the MULTIPLE co
how they are combined.
<table>
<tr><th>DIO_Rx</th><th>Resource</th><th>MULTIPLE</th></tr>
<tr><td>0</td><td>NONE</td><td>–</td></tr>
<tr><td>1</td><td>Reserved</td><td>OR</td></tr>
<tr><td>2</td><td>T0 (Timer0 clock or gate)</td><td>OR</td></tr>
<tr><td>3</td><td>T1 (Timer1 clock or gate)</td><td>OR</td></tr>
<tr><td>4</td><td>IO interrupt (int0)</td><td>OR</td></tr>
<tr><td>5</td><td>IO interrupt (int1)</td><td>OR</td></tr>
</table></td></tr>
<tr><td>DIO_DIR[15:12]
DIO_DIR[11:8]
DIO_DIR[7:4]
DIO_DIR[3:0]</td><td>SFR B0[7:4]
SFR A0[7:4]
SFR 90[7:4]
SFR 80[7:4]</td><td>F</td><td>F</td><td>R/W</td><td>Programs the direction of the first 16 DIO pins. 1 indicates output.
not configured as I/O. See DIO_PV and DIO_PW for special option
outputs. See DIO_EEX[1:0] for special option for SEGDIO2 and S
the direction of DIO pins above 15 is set by SEGDIOx[1]. See POR
up spikes.</td></tr>
<tr><td>DIO[15:12]
DIO[11:8]
DIO[7:4]
DIO[3:0]</td><td>SFR B0[3:0]
SFR A0[3:0]
SFR 90[3:0]
SFR 80[3:0]</td><td>F</td><td>F</td><td>R/W</td><td>The value on the first 16 DIO pins. Pins configured as LCD read z
changes data on pins configured as outputs. Pins configured as
writes. Note that the data for DIO pins above 15 is set by SEGDI</td></tr>
</table>

<table>
<tr><th>Name</th><th>Location</th><th>Rst</th><th>Wk</th><th>Dir</th><th>Description</th></tr>
<tr><td>DIO_EEX[1:0]</td><td>2456[7:6]</td><td>0</td><td>–</td><td>R/W</td><td>When set, converts SEGDIO3 and SEGDIO2 to interface with exte
SEGDIO2 becomes SDCK and SEGDIO3 becomes bi-directional S
LCD_MAP[2] and LCD_MAP[3] are cleared.
<table>
<tr><th>DIO_EEX[1:0]</th><th>Function</th></tr>
<tr><td>00</td><td>Disable EEPROM interface</td></tr>
<tr><td>01</td><td>2-Wire EEPROM interface</td></tr>
<tr><td>10</td><td>3-Wire EEPROM interface</td></tr>
<tr><td>11</td><td>3-Wire EEPROM interface with separate DO (SE
(SEGDIO8) pins.</td></tr>
</table></td></tr>
<tr><td>DIO_PV</td><td>2457[6]</td><td>0</td><td>–</td><td>R/W</td><td>Causes VPULSE to be output on SEGDIO1, if LCD_MAP[1]=0.</td></tr>
<tr><td>DIO_PW</td><td>2457[7]</td><td>0</td><td>–</td><td>R/W</td><td>Causes WPULSE to be output on SEGDIO0, if LCD_MAP[0]=0.</td></tr>
<tr><td>DIO_PX</td><td>2458[7]</td><td>0</td><td>–</td><td>R/W</td><td>Causes XPULSE to be output on SEGDIO6 , if LCD_MAP[6]=0.</td></tr>
<tr><td>DIO_PY</td><td>2458[6]</td><td>0</td><td>–</td><td>R/W</td><td>Causes YPULSE to be output on SEGDIO7 , if LCD_MAP[7]=0.</td></tr>
<tr><td>EEDATA[7:0]</td><td>SFR 9E</td><td>0</td><td>0</td><td>R/W</td><td>Serial EEPROM interface data.</td></tr>
<tr><td>EECTRL[7:0]</td><td>SFR 9F</td><td>0</td><td>0</td><td>R/W</td><td>Serial EEPROM interface control.
<table>
<tr><th>Status Bit</th><th>Name</th><th>Read/ Write</th><th>Reset State</th><th>Polarity</th><th>Description</th></tr>
<tr><td>7</td><td>ERROR</td><td>R</td><td>0</td><td>Positive</td><td>1 when an illegal co</td></tr>
<tr><td>6</td><td>BUSY</td><td>R</td><td>0</td><td>Positive</td><td>1 when serial data</td></tr>
<tr><td>5</td><td>RX_ACK</td><td>R</td><td>1</td><td>Positive</td><td>1 indicates that the
ACK bit.</td></tr>
</table></td></tr>
<tr><td>EQU[2:0]</td><td>2106[7:5]</td><td>0</td><td>0</td><td>R/W</td><td>Specifies the power equation.
<table>
<tr><th>EQU[2:0]</th><th>Description</th><th>Element 0</th><th>Element 1</th><th>Elemen 2</th></tr>
<tr><td>3</td><td>2 element, 4W, 3ϕ Delta</td><td>VA(IA-IB)/2</td><td>0</td><td>VC IC</td></tr>
<tr><td>4</td><td>2 element, 4W, 3ϕ Wye</td><td>VA(IA-IB)/2</td><td>VB(IC-IB)/2</td><td>0</td></tr>
<tr><td>5*</td><td>3 element, 4W, 3ϕ Wye</td><td>VA IA</td><td>VB IB</td><td>VC IC</td></tr>
<tr><td colspan="5">Note:
*The available CE codes implements only equation 5. Contact your local Maxim re
CE code for equation 3 and 4.</td></tr>
</table></td></tr>
</table>

Name	Location	Rst	Wk	Dir	Description
EX_XFER *EX_RTC1S* *EX_RTC1M* *EX_RTCT* *EX_SPI* *EX_EEX* *EX_XPULSE* *EX_YPULSE* *EX_WPULSE* *EX_VPULSE*	2700[0] 2700[1] 2700[2] 2700[3] 2701[7] 2700[7] 2700[6] 2700[5] 2701[6] 2701[5]	0	0	R/W	Interrupt enable bits. These bits enable the XFER_BUSY, the RTC bits are set by hardware and cannot be set by writing a 1. The bits 0. Note that if one of these interrupts is to enabled, its correspondi bit must also be set. See 2.4.8 Interrupts, for details.
EW_DIO4	28B3[2]	0	–	R/W	Connects SEGDIO4 to the WAKE logic and permits SEGDIO4 risir This bit has no effect unless DIO4 is configured as a digital input.
EW_DIO52	28B3[1]	0	–	R/W	Connects SEGDIO52 to the WAKE logic and permits SEGDIO52 ri This bit has no effect unless SEGDIO52 is configured as a digital in
EW_DIO55	28B3[0]	0	–	R/W	Connects SEGDIO55 to the WAKE logic and permits the SEGDIO5 awaken the part. This bit has no effect unless SEGDIO55 is config input.
EW_PB	28B3[3]	0	–	R/W	Connects PB to the WAKE logic and permits a high level on PB to is always configured as an input.
EW_RX	28B3[4]	0	–	R/W	Connects RX to the WAKE logic and permits the RX rising edge to See the WAKE description in 3.4 Wake on Timer for de-bounce iss
FIR_LEN[1:0]	210C[2:1]	0	0	R/W	Determines the number of ADC cycles in the ADC decimation FIR *PLL_FAST* = 1: *FIR_LEN[1:0]* / ADC Cycles: 00 = 141; 01 = 288; 10 = 384 *PLL_FAST* = 0: *FIR_LEN[1:0]* / ADC Cycles: 00 = 135; 01 = 276; 10 = Not Allowed The ADC LSB size and full-scale values depend on the *FIR_LEN[1* Table 81 on page 122 and Table 103 on page 141 for details.

<table>
<tr><th>Name</th><th>Location</th><th>Rst</th><th>Wk</th><th>Dir</th><th>Description</th></tr>
<tr><td>FL_BANK[1:0]</td><td>SFR B6[1:0]</td><td>01</td><td>01</td><td>R/W</td><td><u>Flash Bank Selection (71M6543G only)</u>
The program memory of the 71M6543G consists of a fixed lower b
addressable at 0x0000 to 0x7FFF plus an upper banked area of 32
0x8000 to 0xFFFF. The I/O RAM register FL_BANK is used to swit
memory banks of 32 KB each into the address range from 0x8000
when FL_BANK = 0, the upper bank is the same as the lower bank
<table>
<tr><td>FL_BANK[1:0]</td><td>Address Range for Lower Bank (0x0000-0x7FFF)</td><td>Address Ra (0x80</td></tr>
<tr><td>00</td><td>0x0000-0x7FFF</td><td>0x00</td></tr>
<tr><td>01</td><td>0x0000-0x7FFF</td><td>0x80</td></tr>
<tr><td>10</td><td>0x0000-0x7FFF</td><td>0x100</td></tr>
<tr><td>11</td><td>0x0000-0x7FFF</td><td>0x180</td></tr>
</table></td></tr>
<tr><td>FLSH_ERASE[7:0]</td><td>SFR 94[7:0]</td><td>0</td><td>0</td><td>W</td><td><u>Flash Erase Initiate</u>
FLSH_ERASE is used to initiate either the Flash Mass Erase cycle o
Erase cycle. Specific patterns are expected for FLSH_ERASE in or
appropriate Erase cycle. (default = 0x00).
0x55 – Initiate Flash Page Erase cycle. Must be proceeded by a v
FLSH_PGADR[5:0] (SFR 0xB7).
0xAA – Initiate Flash Mass Erase cycle. Must be proceeded by a v
FLSH_MEEN (SFR 0xB2) and the debug (CC) port must be
Any other pattern written to FLSH_ERASE has no effect.</td></tr>
<tr><td>FLSH_MEEN</td><td>SFR B2[1]</td><td>0</td><td>0</td><td>W</td><td><u>Mass Erase Enable</u>
0 = Mass Erase disabled (default).
1 = Mass Erase enabled.
Must be re-written for each new Mass Erase cycle.</td></tr>
<tr><td>FLSH_PEND</td><td>SFR B2[3]</td><td>0</td><td>0</td><td>R</td><td>Indicates that a posted flash write is pending. If another flash write
ignored.</td></tr>
<tr><td>FLSH_PGADR[5:0]</td><td>SFR B7[7:2]</td><td>0</td><td>0</td><td>W</td><td><u>Flash Page Erase Address</u>
Flash Page Address (page 0 thru 63) that is erased during the Pag
(default = 0x00).
Must be re-written for each new Page Erase cycle.</td></tr>
<tr><td>FLSH_PSTWR</td><td>SFR B2[2]</td><td>0</td><td>0</td><td>R/W</td><td>Enables posted flash writes. When 1, and if CE_E = 1, flash write r
a one element deep FIFO and are executed when CE_BUSY falls.
read to determine the status of the FIFO. If FLSH_PSTWR = 0 or if CE
are immediate.</td></tr>
</table>

Name	Location	Rst	Wk	Dir	Description
FLSH_PWE	SFR B2[0]	0	0	R/W	Program Write Enable 0 = MOVX commands refer to External RAM Space, normal operation 1 = MOVX @*DPTR*,A moves A to External Program Space (Flash) This bit is automatically reset after each byte written to flash. Write inhibited when interrupts are enabled.
FLSH_RDE	2702[2]	–	–	R	Indicates that the flash may be read by ICE or SPI slave. *FLSH_RDE*
FLSH_UNLOCK[3:0]	2702[7:4]	0	0	R/W	Must be a 2 to enable any flash modification. See the description more details.
FLSH_WRE	2702[1]	–	–	R	Indicates that the flash may be written through ICE or SPI slave po
IE_XFER *IE_RTC1S* *IE_RTC1M* *IE_RTCT* *IE_SPI* *IE_EEX* *IE_XPULSE* *IE_YPULSE* *IE_WPULSE* *IE_VPULSE*	SFR E8[0] SFR E8[1] SFR E8[2] SFR E8[3] SFR F8[7] SFR E8[7] SFR E8[6] SFR E8[5] SFR F8[6] SFR F8[5]	0	0	R/W	Interrupt flags for external interrupts 2 and 6. These flags monitor and int2 interrupts (external interrupts to the MPU core). These fla hardware and must be cleared by the software interrupt handler. Th *0xC0[1]*) and *IEX6* (*SFR 0xC0[5]*) interrupt flags are automatically cl core when it vectors to the interrupt handler. *IEX2* and *IEX6* must b zero to their corresponding bit positions in SFR 0xC0, while writing positions that are not being cleared.
INTBITS	2707[6:0]	–	–	R	Interrupt inputs. The MPU may read these bits to see the input to INT0, INT1, up to INT6. These bits do not have any memory and a for debug use.
LCD_ALLCOM	2400[3]	0	–	R/W	Configures SEG/COM bits as COM. Has no effect on pins whose *L*
LCD_BAT	2402[7]	0	–	R/W	Connects the LCD power supply to VBAT in all modes.
LCD_BLNKMAP23[5:0] *LCD_BLNKMAP22[5:0]*	2401[5:0] 2402[5:0]	0	–	R/W	Identifies which segments connected to SEG23 and SEG22 should blink. The most significant bit corresponds to COM5, the least signific
LCD_CLK[1:0]	2400[1:0]	0	–	R/W	Sets the LCD clock frequency. Note: f_{XTAL} = 32768 Hz *LCD_CLK[1:0]* — LCD Clock Frequency 00 — $f_{XTAL}/2^9$ 01 — $f_{XTAL}/2^8$ 10 — $f_{XTAL}/2^7$ 11 — $f_{XTAL}/2^6$

Name	Location	Rst	Wk	Dir	Description
LCD_DAC[4:0]	240D[4:0]	0	–	R/W	The LCD contrast DAC. This DAC controls the VLCD voltage and ha 2.65 V to 5.3 V. The VLCD voltage is VLCD = 2.65 + 2.65 * *LCD_DAC[4:0]*/31 Thus, the LSB of the DAC is 85.5 mV. The maximum DAC output V3P3SYS, VBAT, and whether *LCD_BSTE* = 1.
LCD_E	2400[7]	0	–	R/W	Enables the LCD display. When disabled, VLC2, VLC1, and VLC0 the COM and SEG outputs if their *LCD_MAP* bit is 1.
LCD_MAP[55:48] *LCD_MAP[47:40]* *LCD_MAP[39:32]* *LCD_MAP[31:24]* *LCD_MAP[23:16]* *LCD_MAP[15:8]* *LCD_MAP[7:0]*	2405[7:0] 2406[7:0] 2407[7:0] 2408[7:0] 2409[7:0] 240A[7:0] 240B[7:0]	0 0 0 0 0 0 0	– – – – – – –	R/W R/W R/W R/W R/W R/W R/W	Enables LCD segment driver mode of combined SEGDIO pins. Pi configured as outputs (SEG48 through SEG50) become inputs with when their *LCD_MAP* bit is zero. Also, note that SEG48 through SE with the in-circuit emulator signals. When the ICE_E pin is high, the enabled, and SEG48 through SEG50 become E_RXTX, E_TCLK a respectively.
LCD_MODE[2:0]	2400[6:4]	0	–	R/W	Selects the LCD bias and multiplex mode. ***LCD_MODE*** — **Output** 000 — 4 states, 1/3 bias 001 — 3 states, 1/3 bias 010 — 2 states, 1/2 bias 011 — 3 states, 1/2 bias 100 — Static display 101 — 5 states, 1/3 bias 110 — 6 states, 1/3 bias
LCD_ON *LCD_BLANK*	240C[0] 240C[1]	0 0	– –	R/W R/W	Turns on or off all LCD segments without changing LCD data. If bo LCD display is turned on.
LCD_ONLY	28B2[6]	0	0	W	Puts the 71M6543 to sleep, but with LCD display still active. Ignored present. It awakens when the Wake Timer times out, when certain or when system power returns (see 3.2 Battery Modes).
LCD_RST	240C[2]	0	–	R/W	Clear all bits of LCD data. These bits affect SEGDIO pins that are drivers. This bit does not auto clear.
LCD_SEG0[5:0] *to* *LCD_SEG15[5:0]*	2410[5:0] to 241F[5:0]	0	–	R/W	SEG Data for SEG0 through SEG15. DIO data for these pins is in
LCD_SEGDIO16[5:0] *to* *LCD_SEGDIO45[5:0]*	2420[5:0] to 243D[5:0]	0	–	R/W	SEG and DIO data for SEGDIO16 through SEGDIO45. If configure direction (1 is output, 0 is input), bit 0 is data, and the other bits a

Name	Location	Rst	Wk	Dir	Description
LCD_SEG46[5:0] *to* *LCD_SEG50[5:0]*	243E[5:0] to 2442[5:0]	0	–	R/W	SEG data for SEG46 through SEG50. These pins cannot be confi
LCD_SEGDIO51[5:0] *to* *LCD_SEGDIO55[5:0]*	2443[5:0] to 2447[5:0]	0	–	R/W	SEG and DIO data for SEGDIO51 through SEGDIO55. If configure direction (1 is output, 0 is input), bit 0 is data, and the other bits a
LCD_VMODE[1:0]	2401[7:6]	00	00	R/W	Specifies how VLCD is generated. See 2.5.10.3 for the definition c ***LCD_VMODE*** — **Description** 11 — External VLCD 10 — LCD boost and LCD DAC enabled 01 — LCD DAC enabled 00 — No boost and no DAC. VLCD=V3P3L.
LCD_Y	2400[2]	0	–	R/W	LCD Blink Frequency (ignored if blink is disabled). 1 = 1 Hz, 0 = 0.5 Hz
LKPADDR[6:0]	2887[6:0]	0	0	R/W	The address for reading and writing the RTC lookup RAM.
LKPAUTOI	2887[7]	0	0	R/W	Auto-increment flag. When set, *LKPADDR[6:0]* auto increments ev *LKP_WR* is pulsed. The incremented address can be read at LKPA
LKPDAT[7:0]	2888[7:0]	0	0	R/W	The data for reading and writing the RTC lookup RAM.
LKP_RD *LKP_WR*	2889[1] 2889[0]	0 0	0 0	R/W R/W	Strobe bits for the RTC lookup RAM read and write. When set, the *LKPDAT* registers is used in a read or write operation. When a stro until the operation completes, at which time the strobe is cleared a incremented if *LKPAUTOI* is set.
MPU_DIV[2:0]	2200[2:0]	0	0	R/W	MPU clock rate is: $MPU\ Rate = MCK\ Rate * 2^{-(2+MPU\_DIV[2:0])}$. The maximum value for *MPU_DIV[2:0]* is 4. Based on the default va bit and *MPU_DIV[2:0]*, the power-up MPU rate is 6.29 MHz / 4 = 1.57 minimum MPU clock rate is 38.4 kHz when *PLL_FAST* = 1.
MUX0_SEL[3:0]	2105[3:0]	0	0	R/W	Selects which ADC input is to be converted during time slot 0.
MUX1_SEL[3:0]	2105[7:4]	0	0	R/W	Selects which ADC input is to be converted during time slot 1.
MUX2_SEL[3:0]	2104[3:0]	0	0	R/W	Selects which ADC input is to be converted during time slot 2.
MUX3_SEL[3:0]	2104[7:4]	0	0	R/W	Selects which ADC input is to be converted during time slot 3.
MUX4_SEL[3:0]	2103[3:0]	0	0	R/W	Selects which ADC input is to be converted during time slot 4.
MUX5_SEL[3:0]	2103[7:4]	0	0	R/W	Selects which ADC input is to be converted during time slot 5.
MUX6_SEL[3:0]	2102[3:0]	0	0	R/W	Selects which ADC input is to be converted during time slot 6.
MUX7_SEL[3:0]	2102[7:4]	0	0	R/W	Selects which ADC input is to be converted during time slot 7.

Name	Location	Rst	Wk	Dir	Description
MUX8_SEL[3:0]	2101[3:0]	0	0	R/W	Selects which ADC input is to be converted during time slot 8.
MUX9_SEL[3:0]	2101[7:4]	0	0	R/W	Selects which ADC input is to be converted during time slot 9.
MUX10_SEL[3:0]	2100[3:0]	0	0	R/W	Selects which ADC input is to be converted during time slot 10.
MUX_DIV[3:0]	2100[7:4]	0	0	R/W	*MUX_DIV[3:0]* is the number of ADC time slots in each MUX frame number of time slots is 11.
OPT_BB	2457[0]	0	–	R/W	Configures the input of the optical port to be a DIO pin to allow it t bit-banged. In this case, DIO5 becomes a third high speed UART. and Optical Interface =under the "**Bit Banged Optical UART (Thi** heading on page 56.
OPT_FDC[1:0]	2457[5:4]	0	–	R/W	Selects OPT_TX modulation duty cycle ***OPT_FDC*** | **Function** 00 | 50% Low 01 | 25% Low 10 | 12.5% Low 11 | 6.25% Low
OPT_RXDIS	2457[2]	0	–	R/W	OPT_RX can be configured as an input to the optical UART or as S *OPT_RXDIS* = 0 and *LCD_MAP[55]* = 0: OPT_RX *OPT_RXDIS* = 1 and *LCD_MAP[55]* = 0: DIO55 *OPT_RXDIS* = 0 and *LCD_MAP[55]* = 1: SEG55 *OPT_RXDIS* = 1 and *LCD_MAP[55]* = 1: SEG55
OPT_RXINV	2457[1]	0	–	R/W	Inverts result from OPT_RX comparator when 1. Affects only the U effect when OPT_RX is used as a DIO input.
OPT_TXE [1,0]	2456[3:2]	00	–	R/W	Configures the OPT_TX output pin. If *LCD_MAP[51]* = 0: 00 = DIO51, 01 = OPT_TX, 10 = WPULSE, 11 = VPULSE If *LCD_MAP[51]* = 1: xx = SEG51
OPT_TXINV	2456[0]	0	–	R/W	Invert OPT_TX when 1. This inversion occurs before modulation.
OPT_TXMOD	2456[1]	0	–	R/W	Enables modulation of OPT_TX. When *OPT_TXMOD* is set, OPT when it would otherwise have been zero. The modulation is applied caused by *OPT_TXINV*.
OSC_COMP	28A0[5]	0	–	R/W	Enables the automatic update of *RTC_P[16:0]* and *RTC_Q* [1:0]every is measured.
PB_STATE	SFR F8[0]	0	0	R	The de-bounced state of the PB pin.
PERR_RD *PERR_WR*	SFR FC[6] SFR FC[5]	0	0	R/W	The 71M6543 sets these bits to indicate that a parity error on the re been detected. Once set, the bits are remembered until they are c

Name	Location	Rst	Wk	Dir	Description
PLL_OK	SFR F9[4]	0	0	R	Indicates that the clock generation PLL is settled.
PLL_FAST	2200[4]	0	0	R/W	Controls the speed of the PLL and MCK. 1 = 19.66 MHz (XTAL * 600) 0 = 6.29 MHz (XTAL * 192)
PLS_MAXWIDTH[7:0]	210A[7:0]	FF	FF	R/W	*PLS_MAXWIDTH[7:0]* determines the maximum width of the pulse *PLS_INV*=0 or high-going pulse if *PLS_INV*=1). The maximum pulse (2**PLS_MAXWIDTH[7:0]* + 1)*T_I. Where T_I is *PLS_INTERVAL[7:0]* clock cycles. If *PLS_INTERVAL[7:0]* = 0 or *PLS_MAXWIDTH[7:0]* width checking is performed and the output pulses have 50% duty VPULSE and WPULSE.
PLS_INTERVAL[7:0]	210B[7:0]	0	0	R/W	*PLS_INTERVAL[7:0]* determines the interval time between pulses. output pulses is *PLS_INTERVAL[7:0]**4 in units of CK_FIR clock cycle *PLS_INTERVAL[7:0]* = 0, the FIFO is not used and pulses are output issues them. *PLS_INTERVAL[7:0]* is calculated as follows: *PLS_INTERVAL[7:0]* = Floor (Mux frame duration in CK_FIR cycles / CE frame / 4) For example, since the 71M6543 CE code is written to generate 6 pu interval, when the FIFO is enabled (i.e., *PLS_INTERVAL[7:0]* ≠ 0) and duration is 1950 CK_FIR clock cycles, *PLS_INTERVAL[7:0]* should b Floor(1950 / 6 / 4) = 81 so that the five pulses are evenly spaced i integration interval and the last pulse is issued just prior to the end 2.3.6.2 VPULSE and WPULSE.
PLS_INV	210C[0]	0	0	R/W	Inverts the polarity of WPULSE, VARPULSE, XPULSE, and YPUL pulses are active low. When inverted, they become active high.
PORT_E	270C[5]	0	0	R/W	Enables outputs from the SEGDIO0-SEGDIO15 pins. *PORT_E* = 0 b output pulse that occurs when SEGDIO0-SEGDIO15 are reset on p
PRE_E	2704[5]	0	0	R/W	Enables the 8x pre-amplifier.
PREBOOT	SFRB2[7]	–	–	R	Indicates that pre-boot sequence is active.
RCMD[4:0]	SFR FC[4:0]	0	0	R/W	When the MPU writes a non-zero value to *RCMD*, the 71M6543 iss the appropriate remote sensor. When the command is complete, t RCMD.
RESET	2200[3]	0	0	W	When set, writes a one to *WF_RSTBIT* and then causes a reset.
RFLY_DIS	210C[3]	0	0	R/W	Controls how the 71M6543 drives the power pulse for the 71M6xxx power pulse is driven high and low. When cleared, it is driven high circuit fly-back interval.

Name	Location	Rst	Wk	Dir	Description
RMT2_E *RMT4_E* *RMT6_E*	2709[3] 2709[4] 2709[5]	0	0	R/W	Enables the remote interface.
RMT_RD[15:8] *RMT_RD[7:0]*	2602[7:0] 2603[7:0]	0	0	R	Response from remote read request.
RTCA_ADJ[6:0]	2504[6:0]	40	–	R/W	Register for analog RTC frequency adjustment.
RTC_FAIL	2890[4]	0	0	R	Indicates that a count error has occurred in the RTC and that the ti This bit can be cleared by writing a 0.
RTC_P[16:14] *RTC_P[13:6]* *RTC_P[5:0]*	289B[2:0] 289C[7:0] 289D[7:2]	4 0 0	4 0 0	R/W	RTC adjust. See 2.5.4 Real-Time Clock (RTC). 0x0FFBF ≤ *RTC_P* ≤ 0x10040 Note: *RTC_P[16:0]* and *RTC_Q[1:0]* form a single 19-bit RTC adjus
RTC_Q[1:0]	289D[1:0]	0	0	R/W	RTC adjust. See 2.5.4 Real-Time Clock (RTC). Note: *RTC_P[16:0]* and *RTC_Q[1:0]* form a single 19-bit RTC adjus
RTC_RD	2890[6]	0	0	R/W	Freezes the RTC shadow register so it is suitable for MPU reads. read, it returns the status of the shadow register: 0 = up to date, 1 = frozen.
RTC_SBSC[7:0]	2892[7:0]	–	–	R	Time remaining since the last 1 second boundary. LSB=1/128 sec
RTC_TMIN[5:0]	289E[5:0]	0	–	R/W	The target minutes register. See RTC_THR below.
RTC_THR[4:0]	289F[4:0]	0	–	R/W	The target hours register. The RTC_T interrupt occurs when *RTC_M* equal to *RTC_TMIN[5:0]* and *RTC_HR[4:0]* becomes equal to *RTC_TH*
RTC_WR	2890[7]	0	0	R/W	Freezes the RTC shadow register so it is suitable for MPU writes. cleared, the contents of the shadow register are written to the RTC RTC clock (~1 kHz). When *RTC_WR* is read, it returns 1 as long as continues to return one until the RTC counter actually updates.
RTC_SEC[5:0] *RTC_MIN[5:0]* *RTC_HR[4:0]* *RTC_DAY[2:0]* *RTC_DATE[4:0]* *RTC_MO[3:0]* *RTC_YR[7:0]*	2893[5:0] 2894[5:0] 2895[4:0] 2896[2:0] 2897[4:0] 2898[3:0] 2899[7:0]	– – – – – – –	– – – – – – –	R/W	The RTC interface. These are the year, month, day, hour, minute an for the RTC. The RTC is set by writing to these registers. Year 00 ar by 4 are defined as a leap year. SEC 00 to 59 MIN 00 to 59 HR 00 to 23 (00=Midnight) DAY 01 to 07 (01=Sunday) DATE 01 to 31 MO 01 to 12 YR 00 to 99 Each write operation to one of these registers must be preceded by
RTM_E	2106[1]	0	0	R/W	Real Time Monitor enable. When 0, the RTM output is low.

Name	Location	Rst	Wk	Dir	Description
RTM0[9:8] *RTM0[7:0]* *RTM1[7:0]* *RTM2[7:0]* *RTM3[7:0]*	210D[1:0] 210E[7:0] 210F[7:0] 2110[7:0] 2111[7:0]	0 0 0 0 0	0 0 0 0 0	R/W	Four RTM probes. Before each CE code pass, the values of these output on the RTM pin. The RTM registers are ignored when *RTM_* RTM0 is 10 bits wide. The others assume the upper two bits are 0
SECURE	SFR B2[6]	0	0	R/W	Inhibits erasure of page 0 and flash memory addresses above the be as defined by *CE_LCTN[6/5:0]*. Also inhibits the reading of flash mem devices (SPI or ICE port).
SLEEP	28B2[7]	0	0	W	Puts the 71M6543 to sleep. Ignored if system power is present. T when the Wake timer times out, when push button is pushed, or wh returns.
SPI_CMD	SFR FD[7:0]	–	–	R	SPI command. 8-bit command from the bus master.
SPI_E	270C[4]	1	1	R/W	SPI port enable. Enables the SPI interface on pins SEGDIO36 – S that *LCD_MAP[36-39]* = 0.
SPI_SAFE	270C[3]	0	0	R/W	Limits SPI writes to *SPI_CMD* and a 16 byte region in DRAM. No permitted.
SPI_STAT	2708[7:0]	0	0	R	*SPI_STAT* contains the status results from the previous SPI transac Bit 7 - 71M6543 ready error: the 71M6543 was not ready to read c the previous command. Bit 6 - Read data parity: This bit is the parity of all bytes read from previous command. Does not include the SPI_STAT byte. Bit 5 - Write data parity: This bit is the overall parity of the bytes wr in the previous command. It includes CMD and ADDR bytes. Bit 4:2 - Bottom 3 bits of the byte count. Does not include ADDR One, two, and three byte instructions return 111. Bit 1 - SPI FLASH mode: This bit is zero when the TEST pin is zer Bit 0 - SPI FLASH mode ready: Used in SPI FLASH mode. Indicates that receive another write instruction.
STEMP[10:3] *STEMP[2:0]*	2881[7:0] 2882[7:5]	– –	– –	R R	The result of the temperature measurement.
SUM_SAMPS[12:8] *SUM_SAMPS[7:0]*	2107[4:0] 2108[7:0]	0	0	R/W	The number of multiplexer cycles (frames) per XFER_BUSY interrup 8191 cycles.
TBYTE_BUSY	28A0[3]	0	0	R	Indicates that hardware is still writing the 0x28A0 byte. Additional w locked out while it is one. Write duration could be as long as 6 ms.
TEMP_22[10:8] *TEMP_22[7:0]*	230A[2:0] 230B[7:0]	0	–	R	Storage location for *STEMP[10:0]* at 22C. *STEMP[10:0]* is an 11 bit

<table>
<tr><th>Name</th><th>Location</th><th>Rst</th><th>Wk</th><th>Dir</th><th>Description</th></tr>
<tr><td>TEMP_BAT</td><td>28A0[4]</td><td>0</td><td>–</td><td>R/W</td><td>Causes VBAT to be measured whenever a temperature measure</td></tr>
<tr><td>TEMP_BSEL</td><td>28A0[7]</td><td>0</td><td>–</td><td>R/W</td><td>Selects which battery is monitored by the temperature sensor:
1 = VBAT, 0 = VBAT_RTC</td></tr>
<tr><td>TEMP_PER[2:0]</td><td>28A0[2:0]</td><td>0</td><td>–</td><td>R/W</td><td>Sets the period between temperature measurements. Automatic me
enabled in any mode (MSN, BRN, LCD, or SLP). TEMP_PER = 0 d
temperature updates, in which case TEMP_START may be used by
one-shot temperature measurement.
<table>
<tr><th>TEMP_PER</th><th>Time (seconds)</th></tr>
<tr><td>0</td><td>No temperature updates</td></tr>
<tr><td>1-6</td><td>$2^{(3+TEMP\_PER)}$</td></tr>
<tr><td>7</td><td>Continuous updates</td></tr>
</table></td></tr>
<tr><td>TEMP_PWR</td><td>28A0[6]</td><td>0</td><td>–</td><td>R/W</td><td>Selects the power source for the temp sensor:
1 = V3P3D, 0 = VBAT_RTC.
This bit is ignored in SLP and LCD modes, where the temp sensor
by VBAT_RTC.</td></tr>
<tr><td>TEMP_START</td><td>28B4[6]</td><td>0</td><td>0</td><td>R/W</td><td>When TEMP_PER = 0 automatic temperature measurements are
TEMP_START may be set by the MPU to initiate a one-shot tempe
measurement. TEMP_START is ignored in SLP and LCD modes.
TEMP_START when the temperature measurement is complete.</td></tr>
<tr><td>TMUX[5:0]</td><td>2502[5:0]</td><td>–</td><td>–</td><td>R/W</td><td>Selects one of 32 signals for TMUXOUT. See 2.5.14 for details.</td></tr>
<tr><td>TMUX2[4:0]</td><td>2503[4:0]</td><td>–</td><td>–</td><td>R/W</td><td>Selects one of 32 signals for TMUX2OUT. See 2.5.14 for details.</td></tr>
<tr><td>TMUXR2[2:0]
TMUXR4[2:0]
TMUXR6[2:0]</td><td>270A[2:0]
270A[6:4]
2709[2:0]</td><td>000</td><td>000</td><td>R/W</td><td>The TMUX setting for the remote isolated sensors (71M6xx3).</td></tr>
<tr><td>VERSION[7:0]</td><td>2706[7:0]</td><td>–</td><td>–</td><td>R</td><td>The silicon version index. This word may be read by firmware to d
version.
<table>
<tr><th>VERSION[7:0]</th><th>71M6543F
Silicon Version</th><th>71M6543G
Silicon Version</th></tr>
<tr><td>0001 0001</td><td>A01</td><td>A01</td></tr>
<tr><td>0001 0011</td><td>A03</td><td>N/A</td></tr>
<tr><td>0001 0011</td><td>B01</td><td>N/A</td></tr>
<tr><td>0010 0010</td><td>B02</td><td>N/A</td></tr>
</table></td></tr>
<tr><td>VREF_CAL</td><td>2704[7]</td><td>0</td><td>0</td><td>R/W</td><td>Brings the ADC reference voltage out to the VREF pin. This feature
VREF_DIS=1.</td></tr>
<tr><td>VREF_DIS</td><td>2704[6]</td><td>0</td><td>1</td><td>R/W</td><td>Disables the internal ADC voltage reference.</td></tr>
</table>

Name	Location	Rst	Wk	Dir	Description
VSTAT[2:0]	SFR F9[2:0]	–	–	R	This word describes the source of power and the status of the VDD **VSTAT[2:0]** — **Description** 000 — System Power OK. V3P3A>3.0v. Analog modules accurate. [V3AOK,V3OK]=11 001 — System Power Low. 2.8v<V3P3A<3.0v. Analog m Switch over to battery power is imminent. [V3AOK, 010 — Battery power and VDD OK. VDD>2.25v. Full digi [V3AOK,V3OK]=00, [VDDOK,VDDgt2]=11 011 — Battery power and VDD>2.0. Flash writes are inhib TRIMVDD[5] fuse is blown, *PLL_FAST* is cleared. [V3AOK,V3OK]=00, [VDDOK,VDDgt2]=01 101 — Battery power and VDD<2.0. When VSTAT=101, p out of voltage. Processor failure is imminent. [V3AOK,V3OK]=00, [VDDOK,VDDgt2]=00
WAKE_ARM	28B2[5]	0	–	R/W	Arms the WAKE timer and loads it with WAKE_TMR[7:0]. When S is asserted by the MPU, the WAKE timer becomes active.
WAKE_TMR	2880[7:0]	0	–	R/W	Timer duration is WAKE_TMR+1 seconds.
WD_RST	28B4[7]	0	0	W	Reset the WD timer. The WD is reset when a 1 is written to this bi clears and restarts the watch dog timer.
WF_DIO4	28B1[2]	0	–	R	DIO4 wake flag bit. If DIO4 is configured to wake the part, this bit de-bounced version of DIO4 rises. It is held in reset if DI04 is not wakeup.
WF_DIO52	28B1[1]	0	–	R	DIO52 wake flag bit. If DIO52 is configured to wake the part, this b de-bounced version of DIO52 rises. It is held in reset if DI052 is not
WF_DIO55	28B1[0]	0	–	R	DIO55 wake flag bit. If DIO55 is configured to wake the part, this b de-bounced version of DIO55 rises. It is held in reset if DI055 is not
WF_TMR	28B1[5]	0	–	R	Indicates that the wake timer caused the part to wake up.
WF_PB	28B1[3]	0	–	R	Indicates that the PB caused the part to wake.
WF_RX	28B1[4]	0	–	R	Indicates that RX caused the part to wake.
WF_CSTART *WF_RST* *WF_RSTBIT* *WF_OVF* *WF_ERST* *WF_BADVDD*	28B0[7] 28B0[6] 28B0[5] 28B0[4] 28B0[3] 28B0[2]	0 1 0 0 0 0	–	R	Indicates that the Reset pin, Reset bit, ERST pin, Watchdog timer, t or bad VBAT caused the part to reset.

5.3 CE Interface Description

5.3.1 CE Program

The CE performs the precision computations necessary to accurately measure power. These computations include offset cancellation, phase compensation, product smoothing, product summation, frequency detection, VAR calculation, sag detection and voltage phase measurement. All data computed by the CE is dependent on the selected meter equation as given by *EQU[2:0]* (*I/O RAM 0x2106[7:5]*).

The standard CE program is supplied by Maxim as a data image that can be merged with the MPU operational code for meter applications. Typically, this CE program covers most applications and does not need to be modified. Other variations of CE code may be available from Maxim. The description in this section applies to CE code revision CE43A01A.

5.3.2 CE Data Format

All CE words are 4 bytes. Unless specified otherwise, they are in 32-bit two's complement format (-1 = 0xFFFFFFFF). Calibration parameters are defined in flash memory (or external EEPROM) and must be copied to CE data memory by the MPU before enabling the CE. Internal variables are used in internal CE calculations. Input variables allow the MPU to control the behavior of the CE code. Output variables are outputs of the CE calculations. The corresponding MPU address for the most significant byte is given by 0x0000 + 4 x CE_address and by 0x0003 + 4 x CE_address for the least significant byte.

5.3.3 Constants

Constants used in the CE Data Memory tables are:

- Sampling Frequency: F_S = 32768 Hz/15 = 2184.53 Hz.
- F_0 is the fundamental frequency of the mains phases.
- IMAX is the external rms current corresponding to 250 mV pk at each IADC input.
- VMAX is the external rms voltage corresponding to 250 mV pk at each VADC input.
- NACC, the accumulation count for energy measurements is *SUM_SAMPS[12:0] (I/O RAM 0x2107[4:0], 0x2108[7:0])*. This value also resides in *SUM_PRE* (*CE RAM 0x23*) where it is used for phase angle measurement.
- The duration of the accumulation interval for energy measurements is *SUM_SAMPS[12:0]* /F_S.
- X is a gain constant of the pulse generators. Its value is determined by *PULSE_FAST* and *PULSE_SLOW* (see Table 76).
- Voltage LSB = VMAX * 7.879810^{-9} V.
- VMAX = 600 V, IMAX = 208 A, and kH = 3.2 Wh/pulse are assumed as default settings.

The system constants IMAX and VMAX are used by the MPU to convert internal digital quantities (as used by the CE) to external, i.e. metering quantities. Their values are determined by the scaling of the voltage and current sensors used in an actual meter. The LSB values used in this document relate digital quantities at the CE or MPU interface to external meter input quantities. For example, if a SAG threshold of 80 V peak is desired at the meter input, the digital value that should be programmed into *SAG_THR (CE RAM 0x24)* would be 80 V/SAG_THR_{LSB}, where SAG_THR_{LSB} is the LSB value in the description of *SAG_THR* (Table 77).

The parameters *EQU[2:0], CE_E,* and *SUM_SAMPS[12:0]* , essential to the function of the CE are stored in I/O RAM (see 5.2 for details).

5.3.4 Environment

Before starting the CE using the *CE_E* bit (*I/O RAM 0x2106[0])*, the MPU has to establish the proper environment for the CE by implementing the following steps:

- Locate the CE code in Flash memory using *CE_LCTN[5:0]* (*I/O RAM 0x2109[5:0]*) in the 71M6543F and *CE_LCTN[6:0]* (*I/O RAM 0x2109[6:0]*) in the 71M6543G.
- Load the CE data into RAM.
- Establish the equation to be applied in *EQU[2:0] (I/O RAM 0x2106[7:5])*.
- Establish the accumulation period and number of samples in *SUM_SAMPS[12:0] (I/O RAM 0x2107[4:0], 0x2108[7:0])*.
- Establish the number of cycles per ADC multiplexer frame (*MUX_DIV[3:0] (I/O RAM 0x2100[7:4])*).
- Apply proper values to *MUXn_SEL*, as well as proper selections for *DIFFn_E* (*I/O RAM 0x210C[ ])* and *RMTn_E* (*I/O RAM 0x2709[ ]* in order to configure the analog inputs.
- Initialize any MPU interrupts, such as CE_BUSY, XFER_BUSY, or the power-failure detection interrupt.

When different CE codes are used, a different set of environment parameters need to be established. The exact values for these parameters are listed in the Application Notes and other documentation which accompanies the CE code.

Operating CE codes with environment parameters deviating from the values specified by Maxim leads to unpredictable results.

Typically, there are fifteen 32768 Hz cycles per ADC multiplexer frame (see 2.2.2). This means that the product of the number of cycles per frame and the number of conversions per frame must be 14 (allowing for one settling cycle). The default configuration is *FIR_LEN* = 01, *I/O RAM 0x210C[1]* (two cycles per conversion) and *MUX_DIV[3:0]* = 7 (7 conversions per multiplexer cycle).

Sample configurations can be copied from Demo Code provided by Maxim with the Demo Kits.

5.3.5 CE Calculations

Referring to Table 71, The MPU selects the desired equation by writing the *EQU[2:0]* (*I/O RAM 0x2106[7:5]*).

Table 71: CE *EQU[2:0]* Equations and Element Input Mapping

*EQU [2:0]**	Watt & VAR Formula (*WSUM/VARSUM)*	*W0SUM/ VAR0SUM*	*W1SUM/ VAR1SUM*	*W2SUM/ VAR2SUM*	*I0SQ SUM*	*I1SQ SUM*	*I2SQ SUM*
2	VA*IA + VB*IB (2-element, 3-W, 3ϕ Delta)	VA * IA	VB * IB	N/A	IA	IB	–
3	VA*(IA-IB)/2 + VC*IC (2 element, 4W 3ϕ Delta)	VA*(IA-IB)/2	–	VC*IC	IA-IB	IB	IC
4	VA*(IA-IB)/2 + VB*(IC-IB)/2 (2 element, 4W 3ϕ Wye)	VA*(IA-IB)/2	VB*(IC-IB)/2	–	IA-IB	IC-IB	IC
5	VA*IA + VB*IB + VC*IC (3 element, 4W 3ϕ Wye)	VA*IA	VB*IB	VC*IC	IA	IB	IC

Note:

* Only *EQU[2:0]* = 5 is supported by the currently available CE code versions for the 71M6543. Contact your local Maxim representative for CE codes that support equations 2, 3 and 4.

5.3.6 CE Front-End Data (Raw Data)

Access to the raw data provided by the AFE is possible by reading CE RAM addresses 0 through A, as shown in Table 72. In the expression *MUXn_SEL[3:0]* = x, 'n' refers to the multiplexer frame time slot number and 'x' refers to the desired ADC input number or ADC handle (i.e., IADC0 to VADC10, or simply 0 to 10 decimal).

The 71M6543 can support up to eleven sensor inputs, when all the current sensors are configured as single-ended inputs. If all the current sensor inputs are configured as differential (recommended for best performance), the number of input sensor channels is reduced to seven (i.e., IADC0-1, IADC2-3, IADC4-5, IADC6-7, VADC8, VADC9 and VADC10). The *MUXn_SEL[3:0]* column in Table 72 shows the *MUXn_SEL* handles for the various sensor input pins. For example, if differential mode is enabled via control bit *DIFF0_E* = 1 (*I/O RAM 0x210C[4]*), then the IADC0-IADC1 input pins are combined together to form a single differential input and the corresponding *MUXn_SEL* handle is 0 (i.e., handle 1 is then unused). Similarly, the CE RAM location column provides the CE RAM address where the corresponding sample data is stored. Continuing with the same example, if *DIFF0_E* = 1, the corresponding *CE RAM* location where the samples for the IADC0-IADC1 differential input are stored is *CE RAM* 0.

The IADC2-3, IADC4-5 and IADC6-7 inputs can be configured as direct-connected sensors (i.e., directly connected to the 71M6543) or as remote sensors (i.e., using a 71M6xx3 Isolated Sensor). For example, if the IADC2-3 remote sensor is disabled by *RMT2_E* = 0 (*I/O RAM 0x2007[3]*) and differential mode is enabled by *DIFF2_E* = 1 (*I/O RAM 0x210C[4]*), then IADC2-IADC3 form a differential input with a *MUXn_SEL* handle of 2 (i.e., handle 3 is then unused), and the corresponding samples are stored in CE RAM location 2. If the remote sensor enable bit *RMT2_E* = 1, *DIFF2_E* = x (don't care), then the *MUXn_SEL* handle is not required (i.e., the sensor is not connected to the 71M6543 multiplexer, so *MUXn_SEL* does not apply), and the samples corresponding to this remote differential IADC2-IADC3 input are stored in CE RAM location 2 directly by the digital isolation interface (see Figure 2).

The voltage sensor inputs (VADC8, VADC9 and VADC10) are always single-ended inputs and cannot be configured as remotes, so they do not have any associated configuration bits. VADC8 (VA) has a *MUXn_SEL* handle value of 8, and its samples are stored in CE RAM location 8. VADC9 (VB) has a *MUXn_SEL* handle value of 9 and its samples are stored in CE RAM location 9. VADC10 (VC) has a *MUXn_SEL* handle value of 10 and its samples are stored in CE RAM location 10.

Table 72: CE Raw Data Access Locations

Pin	***MUXn_SEL* Handle**				**CE RAM Location**			
	DIFF0_E				*DIFF0_E*			
	0	1			0	1		
IADC0	0	0			0	0		
IADC1	1				1			
	RMT2_E, DIFF2_E				*RMT2_E, DIFF2_E*			
	0,0	0,1	1,0	1,1	0,0	0,1	1,0	1,1
IADC2	2	2	-	-	2	2	2*	2*
IADC3	3				3			
	RMT4_E, DIFF4_E				*RMT4_E, DIFF4_E*			
	0,0	0,1	1,0	1,1	0,0	0,1	1,0	1,1
IADC4	4	4	-	-	4	4	4*	4*
IADC5	5				5			
	RMT6_E, DIFF6_E				*RMT6_E, DIFF6_E*			
	0,0	0,1	1,0	1,1	0,0	0,1	1,0	1,1
IADC6	6	6	-	-	6	6	6*	6*
IADC7	7				7			
	There are no configuration bits for VADC8, 9, 10							
VADC8 (VA)	8				8			
VADC9 (VB)	9				9			
VADC10 (VC)	10				10			

*Remote interface data

5.3.7 CE Status and Control

The CE Status Word is useful for generating early warnings to the MPU (Table 73). It contains sag warnings for phase A, B, and C, as well as *F0*, the derived clock operating at the fundamental input frequency. The MPU can read the CE status word at every CE_BUSY interrupt. Since the CE_BUSY interrupt occurs at the sample rate (i.e., 2520.6 Hz for *MUX_DIV[3:0]*=6 or 2184.5 Hz for *MUX_DIV[3:0]*=7), it is desirable to minimize the computation required in the interrupt handler of the MPU.

Table 73: *CESTATUS* Register

CE Address	Name	Description
0x80	*CESTATUS*	See description of *CESTATUS* bits in Table 74.

CESTATUS provides information about the status of voltage and input AC signal frequency, which are useful for generating an early power fail warning to initiate necessary data storage. *CESTATUS* represents the status flags for the preceding CE code pass (CE_BUSY interrupt). The significance of the bits in *CESTATUS* is shown in Table 74.

Table 74: *CESTATUS* Bit Definitions

***CESTATUS* bit**	Name	Description
31:4	Not Used	These unused bits are always zero.
3	*F0*	*F0* is a square wave at the exact fundamental input frequency.
2	*SAG_C*	Normally zero. Becomes one when VADC10 (VC) remains below *SAG_THR (CE RAM 0x24)* for *SAGCNT* samples. Does not return to zero until VADC10 (VC) rises above *SAG_THR*.
1	*SAG_B*	Normally zero. Becomes one when VADC9 (VB) remains below *SAG_THR* for *SAG_CNT* samples. Does not return to zero until VADC9 (VB) rises above *SAG_THR*.
0	*SAG_A*	Normally zero. Becomes one when VADC8 (VA) remains below *SAG_THR* for *SAG_CNT* samples. Does not return to zero until VADC8 (VA) rises above *SAG_THR*.

The CE is initialized by the MPU using *CECONFIG* (Table 75). This register contains in packed form *SAG_CNT, FREQSEL0, FREQSEL1, EXT_PULSE, PULSE_SLOW,* and *PULSE_FAST*. The *CECONFIG* bit definitions are given in Table 76.

Table 75: *CECONFIG* Register

CE Address	Name	Data	Description
0x20	*CECONFIG*	0x0030DA20	See description of the *CECONFIG* bits in Table 76.

The *EXT_TEMP* bit enables temperature compensation by the MPU, when set to 1. When 0, internal (CE) temperature compensation is enabled.

The CE pulse generator can be controlled by either the MPU (external) or CE (internal) variables. Control is by the MPU if *EXT_PULSE* = 1. In this case, the MPU controls the pulse rate by placing values into *APULSEW* and *APULSER (CE RAM 0x45 and 0x49)*. By setting *EXT_PULSE* = 0, the CE controls the pulse rate based on *WSUM_X (CE RAM 0x84)* and *VARSUM_X (CE RAM 0x88).*

✓ The 71M6543 Demo Code creep function halts both internal and external pulse generation.

Table 76: *CECONFIG* Bit Definitions (CE RAM 0x20)

<table>
<tr><th>CECONFIG bit</th><th>Name</th><th>Default</th><th>Description</th></tr>
<tr><td>23</td><td>Reserved</td><td>0</td><td>Reserved (can be used by the MPU to indicate that the 71M6x03 is being used; CE does not use this).</td></tr>
<tr><td>22</td><td>EXT_TEMP</td><td>0</td><td>When 1, the MPU controls temperature compensation via the GAIN_ADJn (CE RAM 0x40-0x42), when 0, the CE is in control.</td></tr>
<tr><td>21</td><td>EDGE_INT</td><td>1</td><td>When 1, XPULSE produces a pulse for each zero-crossing of the mains phase selected by FREQSEL[1:0] , which can be used to interrupt the MPU.</td></tr>
<tr><td>20</td><td>SAG_INT</td><td>1</td><td>When 1, activates the YPULSE/SEGDIO7 output when a sag is detected (see 2.5.10) on the phase selected with FREQSEL[1:0].</td></tr>
<tr><td>19:8</td><td>SAG_CNT</td><td>218 (0xDA)</td><td>The number of consecutive voltage samples below SAG_THR (CE RAM 0x24) before a sag alarm is declared. The default value is equivalent to 100 ms.</td></tr>
<tr><td>7:6</td><td>FREQSEL[1:0]</td><td>0</td><td>FREQSEL[1:0] selects the phase to be used for the frequency monitor, sag detection, the phase-to-phase lag calculation and for the zero crossing counter (MAINEDGE_X, CE RAM 0x83).
<table>
<tr><th colspan="2" rowspan="2">FREQ SEL[1:0]</th><th rowspan="2">Phase Selected</th><th colspan="2">Phases Selected</th></tr>
<tr><th>PH_AtoB_X</th><th>PH_AtoC_X</th></tr>
<tr><td>0</td><td>0</td><td>A</td><td>A-B</td><td>A-C</td></tr>
<tr><td>0</td><td>1</td><td>B</td><td>B-C</td><td>B-A</td></tr>
<tr><td>1</td><td>0</td><td>C</td><td>C-A</td><td>C-B</td></tr>
<tr><td>1</td><td>1</td><td colspan="3">Not allowed</td></tr>
</table></td></tr>
<tr><td>5</td><td>EXT_PULSE</td><td>1</td><td>When zero, causes the pulse generators to respond to internal data. WPULSE = WSUM_X (CE RAM 0x84), VPULSE = VARSUM_X (CE RAM 0x88.) Otherwise, the generators respond to values the MPU places in APULSEW and APULSER (CE RAM 0x45 and 0x49)</td></tr>
<tr><td>4:2</td><td>Reserved</td><td>0</td><td>Reserved.</td></tr>
<tr><td>1</td><td>PULSE_FAST</td><td>0</td><td rowspan="2">When PULSE_FAST = 1, the pulse generator input is increased 16x. When PULSE_SLOW = 1, the pulse generator input is reduced by a factor of 64. These two parameters control the pulse gain factor X (see table below). Allowed values are either 1 or 0. Default is 0 for both (X = 6).
<table>
<tr><th>PULSE_FAST</th><th>PULSE_SLOW</th><th>X</th></tr>
<tr><td>0</td><td>0</td><td>$1.5 * 2^2 = 6$</td></tr>
<tr><td>0</td><td>1</td><td>$1.5 * 2^{-4} = 0.09375$</td></tr>
<tr><td>1</td><td>0</td><td>$1.5 * 2^6 = 96$</td></tr>
<tr><td>1</td><td>1</td><td>Do not use</td></tr>
</table></td></tr>
<tr><td>0</td><td>PULSE_SLOW</td><td>0</td></tr>
</table>

The FREQSEL[1:0] field in *CECONFIG* (*CE RAM 0x20[7:6]*) selects the phase that is utilized to generate a sag interrupt. Thus, a *SAG_INT* event occurs when the selected phase has satisfied the sag event criteria as set by the *SAG_THR* (*CE RAM 0x24*) register and the *SAG_CNT* field in *CECONFIG (CE RAM 0x20[19:8]).* When the *SAG_INT* bit (*CE RAM 0x20[20]*) is set to 1, a sag event generates a transition on the YPULSE output. After a sag interrupt, the MPU should change the *FREQSEL[1:0]* setting to select the other phase, if it is powered. Even though a sag interrupt is only generated on the selected phase, all three phases are simultaneously checked for sag. The presence of power on a given phase can be sensed by directly checking the *SAG_A*, *SAG_B* and *SAG_C* bits in *CESTATUS* (*CE RAM 0x80[0:1]).*

The *EXT_TEMP* bit enables temperature compensation by the MPU, when set to 1. When 0, internal (CE) temperature compensation is enabled.

The CE pulse generator can be controlled by either the MPU (external) or CE (internal) variables. Control is by the MPU if the *EXT_PULSE* bit = 1 (*CE RAM 0x20[5]*). In this case, the MPU controls the pulse rate (external pulse generation) by placing values into *APULSEW* and *APULSER (CE RAM 0x45 and 0x49)*. By setting *EXT_PULSE* = 0, the CE controls the pulse rate based on *WSUM_X (CE RAM 0x84)* and *VARSUM_X (CE RAM 0x88).*

✓ The 71M6543 Demo Code creep function halts both internal and external pulse generation.

Table 77: Sag Threshold, Phase Measurement, and Gain Adjust Control

CE Address	Name	Default	Description
0x24	*SAG_THR*	$2.39*10^7$	The voltage threshold for sag warnings. The default value is equivalent to 80VRMS if VMAX = 600V. $SAG\_THR = \frac{V_{rms} * \sqrt{2}}{VMAX * 7.8798 * 10^{-9}}$
0x40	*GAIN_ADJ0*	16384	The assignments of these gain adjustments depends on the meter design. See 4.5.4 Temperature Compensation for VREF and Shunt Sensors on page 89 or 4.5.5 Temperature Compensation of VREF and Current Transformers on page 90. The default value of 16384 corresponds to unity gain.
0x41	*GAIN_ADJ1*	16384	
0x42	*GAIN_ADJ2*	16384	
0x43	*GAIN_ADJ3*	16384	
0x44	*GAIN_ADJ4*	16384	

5.3.8 CE Transfer Variables

When the MPU receives the XFER_BUSY interrupt, it knows that fresh data is available in the transfer variables. CE transfer variables are modified during the CE code pass that ends with an XFER_BUSY interrupt. They remain constant throughout each accumulation interval. In this data sheet, the names of CE transfer variables always end with _X. The transfer variables can be categorized as:

- Fundamental energy measurement variables
- Instantaneous (RMS) values
- Other measurement parameters

Fundamental Energy Measurement Variables

Table 78 describes each transfer variable for fundamental energy measurement. All variables are signed 32-bit integers. Accumulated variables such as WSUM are internally scaled so they have at least 2x margin before overflow when the integration time is one second. Additionally, the hardware does not permit output values to fold back upon overflow.

Table 78: CE Transfer Variables (with Shunts)

CE Address	Name	Description	Configuration
0x84	*WSUM_X*	The signed sum: *W0SUM_X+W1SUM_X+W2SUM_X*.	Figure 31 (page 86)
0x85	*W0SUM_X*	The sum of Wh samples from each wattmeter element. $LSB_W = 7.7562*10^{-13}$ VMAX * IMAX Wh.	
0x86	*W1SUM_X*		
0x87	*W2SUM_X*		
0x88	*VARSUM_X*	The signed sum: *VAR0SUM_X+VAR1SUM_X+VAR2SUM_X.*	
0x89	*VAR0SUM_X*	The sum of VARh samples from each wattmeter element. $LSB_W = 7.7562*10^{-13}$ VMAX * IMAX VARh.	
0x8A	*VAR1SUM_X*		
0x8B	*VAR2SUM_X*		

Table 79: CE Transfer Variables (with CTs)

CE Address	Name	Description	Configuration
0x84	*WSUM_X*	The signed sum: *W0SUM_X+W1SUM_X+W2SUM_X*.	Figure 32 (page 87)
0x85	*W0SUM_X*	The sum of Wh samples from each wattmeter element. $LSB_W = 1.0856*10^{-12}$ VMAX IMAX Wh.	
0x86	*W1SUM_X*		
0x87	*W2SUM_X*		
0x88	*VARSUM_X*	The signed sum: *VAR0SUM_X+VAR1SUM_X+VAR2SUM_X*.	
0x89	*VAR0SUM_X*	The sum of VARh samples from each wattmeter element. $LSB_W = 1.0856*10^{-12}$ VMAX IMAX VARh.	
0x8A	*VAR1SUM_X*		
0x8B	*VAR2SUM_X*		

WSUM_X and *VARSUM_X* are the signed sum of Phase-A, Phase-B and Phase-C Wh or VARh values according to the metering equation specified in the control field *EQU[2:0] (I/O RAM 0x2106[7:5])*. *WnSUM_X* is the Wh value accumulated for phase n in the last accumulation interval and can be computed based on the specified LSB value.

For example, with VMAX = 600 V and IMAX = 208 A, the LSB for *WnSUM_X* is 0.135 µWh.

5.3.8.1 Instantaneous Energy Measurement Variables

InSQSUM_X and *VnSQSUM* are the squared current and voltage samples acquired during the last accumulation interval. *INSQSUM_X* can be used for computing the neutral current.

Table 80: CE Energy Measurement Variables (with Shunts)

CE Address	Name	Description	Configuration
0x8C	*I0SQSUM_X*	Neutral Current: $LSB_I = 9.9045*10^{-13} * IMAX^2\ A^2h$ (*PRE_E*=0) $LSB_I = 6.1903125*10^{-14} * IMAX^2\ A^2h$ (*PRE_E*=1)	Figure 31 (page 86)
0x8D	*I1SQSUM_X*	$LSB_I = 6.3968*10^{-13} * (IMAX^2)\ A^2h$	
0x8E	*I2SQSUM_X*		
0x8F	*I3SQSUM_X*		
0x90	*V0SQSUM_X*	$LSB_V = 9.4045*10^{-13}*VMAX^2\ V^2h$	
0x91	*V1SQSUM_X*		
0x92	*V2SQSUM_X*		

Table 81: CE Energy Measurement Variables (with CTs)

CE Address	Name	Description	Configuration
0x8C	*I0SQSUM_X*	$LSB_I = 1.0856*10^{-12} * (IMAX^2)\ A^2h$	Figure 32 (page 87)
0x8D	*I1SQSUM_X*		
0x8E	*I2SQSUM_X*		
0x8F	*I3SQSUM_X*		
0x90	*V0SQSUM_X*	$LSB_V = 1.0856*10^{-12} * VMAX^2\ V^2h$	
0x91	*V1SQSUM_X*		
0x92	*V2SQSUM_X*		

The RMS values can be computed by the MPU from the squared current and voltage samples as follows:

$$Ix_{RMS} = \sqrt{\frac{IxSQSUM \cdot LSB_I \cdot 3600 \cdot F_S}{N_{ACC}}} \qquad Vx_{RMS} = \sqrt{\frac{VxSQSUM \cdot LSB_V \cdot 3600 \cdot F_S}{N_{ACC}}}$$

Other transfer variables include those available for frequency and phase measurement, and those reflecting the count of the zero-crossings of the mains voltage and the battery voltage. These transfer variables are listed in Table 82.

MAINEDGE_X reflects the number of half-cycles accounted for in the last accumulated interval for the AC signal of the phase specified in the *FREQSEL[1 :0]* field of the *CECONFIG* register (*CE RAM 0x20[7:6])* . *MAINEDGE_X* is useful for implementing a real-time clock based on the input AC signal.

Table 82: Other Transfer Variables

CE Address	Name	Description
0x82	*FREQ_X*	Fundamental frequency: LSB $\equiv \frac{2184Hz}{2^{32}} \approx 0.509 \cdot 10^{-6}$ *Hz(for CT)* LSB $\equiv \frac{2520Hz}{2^{32}} \approx 0.587 \cdot 10^{-6}$ *Hz(for Shunt)*
0x83	*MAINEDGE_X*	The number of edge crossings of the selected voltage in the previous accumulation interval. Edge crossings are either direction and are debounced.
0x94	*PH_AtoB_X*	Voltage phase lag. The selection of the reference phase is based on *FREQSEL[1:0]* in the *CECONFIG* register: If *FREQSEL[1:0]* selects phase A: Phase lag from A to B. If *FREQSEL[1:0]* selects phase B: Phase lag from B to C. If *FREQSEL[1:0]* selects phase C: Phase lag from C to A. Angle in degrees is (0 to 360): *PH_AtoB_X* * 360/N_{ACC} + 2.4*15/13 (for CT) Angle in degrees is (0 to 360): *PH_AtoB_X* * 360/N_{ACC} + 2.4 (for Shunt)
0x95	*PH_AtoC_X*	If *FREQSEL[1:0]* selects phase A: Phase lag from A to C. If *FREQSEL[1:0]* selects phase B: Phase lag from B to A. If *FREQSEL[1:0]* selects phase C: Phase lag from C to B. Angle in degrees is (0 to 360): *PH_AtoC_X* * 360/N_{ACC} + 4.8*15/13 (for CT) Angle in degrees is (0 to 360): *PH_AtoC_X* * 360/N_{ACC} + 4.8*15/13 (for Shunt)

✓ Phase angle measurement accuracy can be increased by writing values > 1 into *V_ANG_CNT* (*V_ANG_CNT* indicates how many accumulation periods to sum PH_AtoB_X and PH_AtoC_X over. The MPU then has to divide by that number. For standard CE codes that support shunts with remotes, *V_ANG_CNT* is at CE address 0x53. For standard CE codes that support shunts with CT, *V_ANG_CNT* is at CE address 0x55. For other than standard CE codes, please contact Maxim for information).

5.3.9 Pulse Generation

Table 83 describes the CE pulse generation parameters.

The combination of the *CECONFIG PULSE_SLOW (CE RAM 0x20[0]*) and *PULSE_FAST (CE RAM 0x20[1]*) bits controls the speed of the pulse rate. The default values of 0 and 0 maintain the original pulse rate given by the Kh equation.

WRATE (*CE RAM 0x21*) controls the number of pulses that are generated per measured Wh and VARh quantities. The lower *WRATE* is the slower the pulse rate for measured energy quantity. The metering constant Kh is derived from *WRATE* as the amount of energy measured for each pulse. That is, if Kh =

1Wh/pulse, a power applied to the meter of 120 V and 30 A results in one pulse per second. If the load is 240 V at 150 A, ten pulses per second are generated.

Control is transferred to the MPU for pulse generation if *EXT_PULSE* = 1 *(CE RAM 0x20[5])*. In this case, the pulse rate is determined by *APULSEW* and *APULSER (CE RAM 0x45 and 0x49)*. The MPU has to load the source for pulse generation in *APULSEW* and *APULSER* to generate pulses. Irrespective of the *EXT_PULSE* status, the output pulse rate controlled by *APULSEW* and *APULSER* is implemented by the CE only. By setting *EXT_PULSE* = 1, the MPU is providing the source for pulse generation. If *EXT_PULSE* is 0, *W0SUM_X* and *VAR0SUM_X* are the default pulse generation sources. In this case, creep cannot be controlled since it is an MPU function.

The maximum pulse rate is $3*F_S$ = 7.5 kHz.

See 2.3.6.2 VPULSE and WPULSE (page 27) for details on how to adjust the timing of the output pulses.

The maximum time jitter is 1/6 of the multiplexer cycle period (nominally 67 µs) and is independent of the number of pulses measured. Thus, if the pulse generator is monitored for one second, the peak jitter is 67 ppm. After 10 seconds, the peak jitter is 6.7 ppm. The average jitter is always zero. If it is attempted to drive either pulse generator faster than its maximum rate, it simply outputs at its maximum rate without exhibiting any rollover characteristics. The actual pulse rate, using *WSUM* as an example, is:

$$RATE = \frac{WRATE \cdot WSUM \cdot F_S \cdot X}{2^{46}} Hz,$$

where F_S = sampling frequency (2184.53 Hz), X = Pulse speed factor derived from the CE variables *PULSE_SLOW (CE RAM 0x20[0])* and *PULSE_FAST (CE RAM 0x20[1])*.

Table 83: CE Pulse Generation Parameters

CE Address	Name	Default	Description
0x21	*WRATE*	227	Kh = VMAX*IMAX*K / (*WRATE**N_{ACC}*X) Wh/pulse where: K = 76.3594 when used with local sensors (CT or shunt) K = 54.5793 when used with 71M6xx3 remote sensors
0x22	*KVAR*	6444	Scale factor for VAR measurement.
0x23	*SUM_PRE*	2184	Number of samples per accumulation interval, as specified in *SUM_SAMPS[12:0], I/O RAM 0x2107[4:0], 0x2108[7:0]* (N_{ACC}).
0x45	*APULSEW*	0	Wh pulse (WPULSE) generator input to be updated by the MPU when using external pulse generation. The output pulse rate is: *APULSEW* * F_S * 2^{-32} * *WRATE* * *X* * 2^{-14}. This input is buffered and can be updated by the MPU during a conversion interval. The change takes effect at the beginning of the next interval.
0x46	*WPULSE_CTR*	0	Counter for WPULSE output.
0x47	*WPULSE_ FRAC*	0	Unsigned numerator, containing a fraction of a pulse. The value in this register always counts up towards the next pulse.
0x48	*WSUM_ ACCUM*	0	Roll-over accumulator for WPULSE.
0x49	*APULSER*	0	VARh (VPULSE) pulse generator input.
0x4A	*VPULSE_CTR*	0	Counter for VPULSE output.
0x4B	*VPULSE_ FRAC*	0	Unsigned numerator, containing a fraction of a pulse. The value in this register always counts up towards the next pulse.
0x4C	*VSUM_ACCUM*	0	Roll-over accumulator for VPULSE.

Other CE Parameters

Table 84 shows the QUANT CE parameters used for suppression of noise due to scaling and truncation effects. The equations for calculating the LSB weight of each QUANT parameter are provided at the bottom of Table 84.

Table 84: CE Parameters for Noise Suppression and Code Version

CE Address	Name	Default	Description
0x26	*QUANT_IA*	0	Compensation factors for truncation and noise in current, real energy and reactive energy for phase A.
0x27	*QUANT_WA*	0	
0x28	*QUANT_VARA*	0	
0x2A	*QUANT_IB*	0	Compensation factors for truncation and noise in current, real energy and reactive energy for phase B.
0x2B	*QUANT_WB*	0	
0x2C	*QUANT_VARB*	0	
0x2E	*QUANT_IC*	0	Compensation factors for truncation and noise in current, real energy and reactive energy for phase C.
0x2F	*QUANT_WC*	0	
0x30	*QUANT_VARC*	0	
0x31	*QUANT_ID*	0	Compensation factors for truncation and noise in current for phase D.

LSB weights for use with the 71M6xx3 isolated sensors:

$$QUANT\_Ix\_LSB = 5.20864 \cdot 10^{-10} \cdot IMAX^2 (Amps^2)$$

$$QUANT\_Wx\_LSB = 8.59147 \cdot 10^{-10} \cdot VMAX \cdot IMAX (Watts)$$

$$QUANT\_VARx\_LSB = 8.59147 \cdot 10^{-10} \cdot VMAX \cdot IMAX (Vars)$$

LSB weights for use with Current Transformers (CTs):

$$QUANT\_Ix\_LSB = 5.08656 \cdot 10^{-13} \cdot IMAX^2 (Amps^2)$$

$$QUANT\_Wx\_LSB = 1.04173 \cdot 10^{-9} \cdot VMAX \cdot IMAX (Watts)$$

$$QUANT\_VARx\_LSB = 1.04173 \cdot 10^{-9} \cdot VMAX \cdot IMAX (Vars)$$

5.3.10 CE Calibration Parameters

Table 85 lists the parameters that are typically entered to effect calibration of meter accuracy.

Table 85: CE Calibration Parameters

<table>
<tr><th>CE Address</th><th>Name</th><th>Default</th><th>Description</th></tr>
<tr><td>0x10</td><td>CAL_IA</td><td>16384</td><td rowspan="7">These constants control the gain of their respective channels. The nominal value for each parameter is 2^{14} = 16384. The gain of each channel is directly proportional to its CAL parameter. Thus, if the gain of a channel is 1% low, CAL should be increased by 1%.</td></tr>
<tr><td>0x11</td><td>CAL_VA</td><td>16384</td></tr>
<tr><td>0x13</td><td>CAL_IB</td><td>16384</td></tr>
<tr><td>0x14</td><td>CAL_VB</td><td>16384</td></tr>
<tr><td>0x16</td><td>CAL_IC</td><td>16384</td></tr>
<tr><td>0x17</td><td>CAL_VC</td><td>16384</td></tr>
<tr><td>0x19</td><td>CAL_ID</td><td>16384</td></tr>
<tr><td>0x12</td><td>PHADJ_A</td><td>0</td><td rowspan="3">These constants control the CT phase compensation. No compensation occurs when PHADJ_X = 0. As PHADJ_X is increased, more compensation (lag) is introduced. The range is $\pm 2^{15} - 1$. If it is desired to delay the current by the angle Φ, the equations are:
$$PHADJ\_X = 2^{20}\frac{0.029615 TAN\Phi}{0.1714 - 0.0168 \cdot TAN\Phi}$$ at 60Hz
$$PHADJ\_X = 2^{20}\frac{0.0206 \cdot TAN\Phi}{0.1430 - 0.01226 \cdot TAN\Phi}$$ at 50Hz</td></tr>
<tr><td>0x15</td><td>PHADJ_B</td><td>0</td></tr>
<tr><td>0x18</td><td>PHADJ_C</td><td>0</td></tr>
<tr><td>0x12</td><td>DLYADJ_A</td><td>0</td><td rowspan="3">The shunt delay compensation is obtained using the equation provided below:
$$DLYADJ\_X = \Delta_{degrees}\left(1 + 0.1\Delta_{degrees}\right)2^{14}\frac{2\pi}{360}\frac{a^2\cos^2\left(\frac{2\pi f}{f_s}\right) + 2ab\cos\left(\frac{2\pi f}{f_s}\right) + b}{c\sin\left(\frac{2\pi f}{f_s}\right)}$$
where:
$$a = 2A$$
$$b = A^2 + 1$$
$$c = 2A^2 + 4A\cos\left(\frac{2\pi f}{f_s}\right) + 2$$
f is the mains frequency
f_s is the sampling frequency

The table below provides the value of A for each channel:
<table><tr><th>Channel</th><th>Value of A (decimal)</th></tr><tr><td>D YADJ_A</td><td>13840</td></tr><tr><td>DLYADJ_B</td><td>11693</td></tr><tr><td>DLYADJ_C</td><td>9359</td></tr></table></td></tr>
<tr><td>0x15</td><td>DLYADJ_B</td><td>0</td></tr>
<tr><td>0x18</td><td>DLYADJ_C</td><td>0</td></tr>
<tr><td colspan="4">Note:
The current sensor inputs are not assigned to the A, B and C phases in a fixed manner. The assignments of phases A, B and C depends on how the IADC0-1, IADC2-3, IADC4-5, IADC6-7 current sensing inputs are connected in the meter design. The CE code must be aware of these connections. See Figure 31 and Figure 32 for typical meter configurations. VADC8, VADC9 and VADC10 are assigned to voltage phases VA, VB and VC in a fixed manner, respectively.
The CE addresses listed in this table are assigned to phases A, B and C as indicated by their names.</td></tr>
</table>

5.3.11 CE Flow Diagrams

Figure 38 through Figure 40 show the data flow through the CE in simplified form. Functions not shown include delay compensation, sample interpolation, scaling and the processing of meter equations.

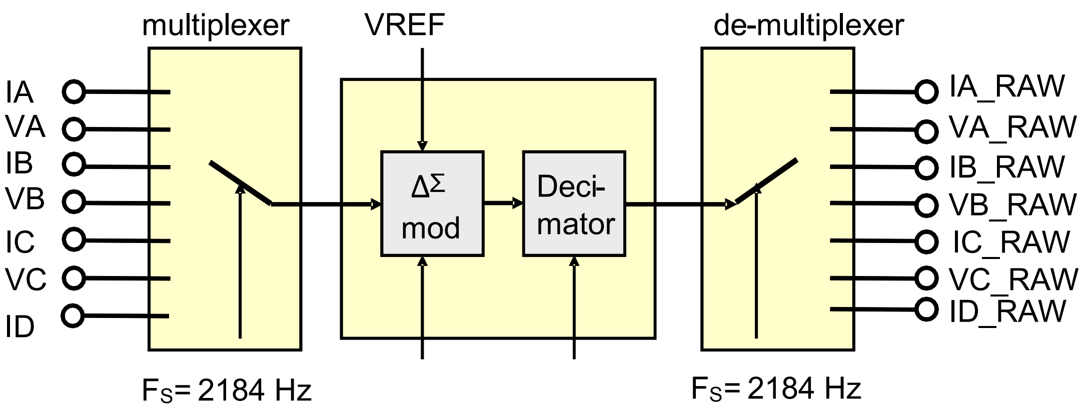


Figure 38: CE Data Flow: Multiplexer and ADC

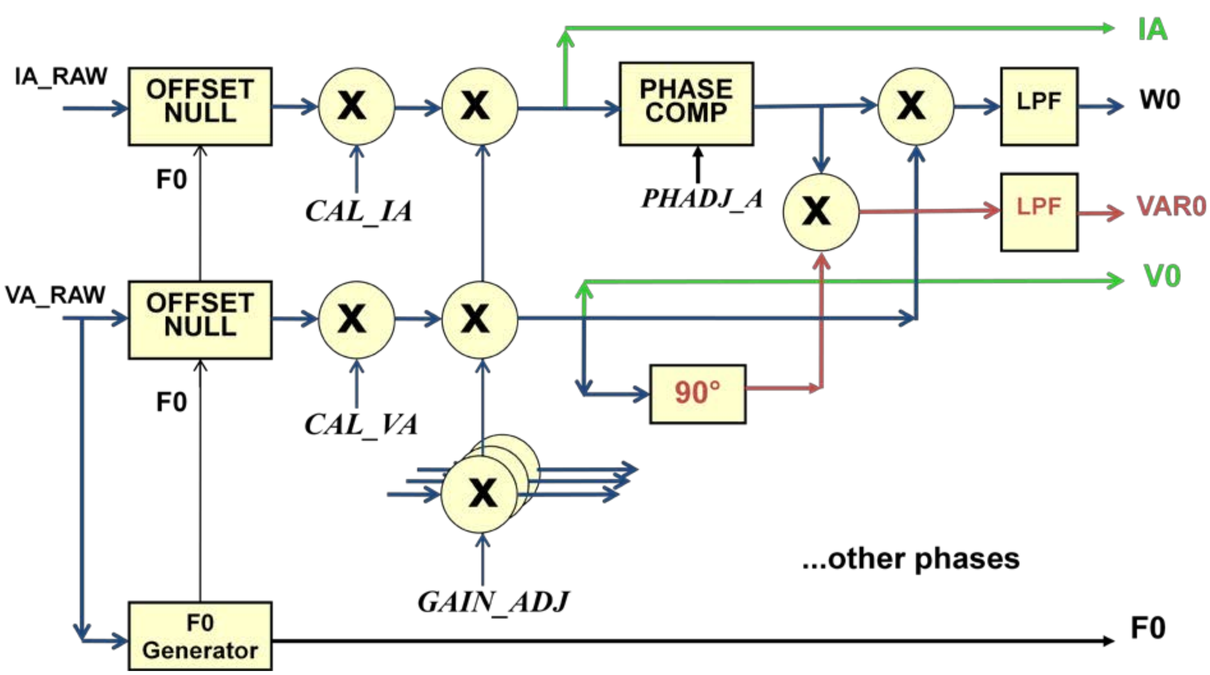


Figure 39: CE Data Flow: Scaling, Gain Control, Intermediate Variables for one Phase

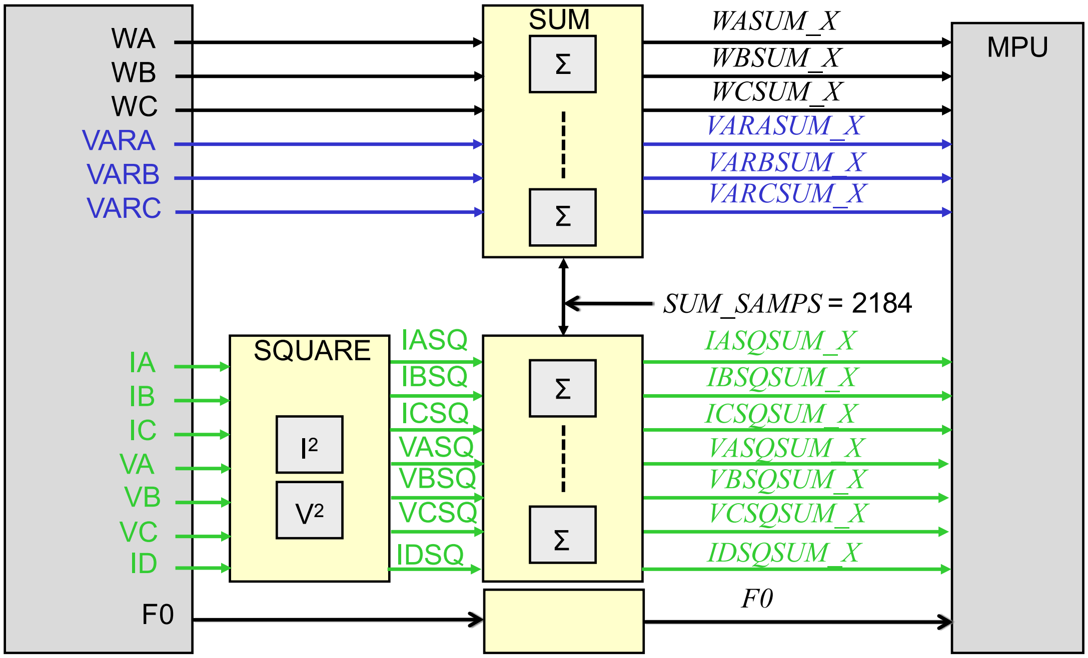


Figure 40: CE Data Flow: Squaring and Summation Stages

6 71M6543 Specifications

This section provides the electrical specifications for the 71M6543. Please refer to the 71M6xxx Data Sheet for the 71M6xx3 electrical specifications, pin-out and package mechanical data.

6.1 Absolute Maximum Ratings

Table 86 shows the absolute maximum ratings for the device. Stresses beyond Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation at these or any other conditions beyond those indicated under recommended operating conditions (See 6.3) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GNDA.

Table 86: Absolute Maximum Ratings

Voltage and Current	
Supplies and Ground Pins	
V3P3SYS, V3P3A	–0.5 V to +4.6 V
VBAT, VBAT_RTC	-0.5 V to +4.6 V
GNDD	-0.1 V to +0.1 V
Analog Output Pins	
VREF	-10 mA to +10 mA, -0.5 V to V3P3A+0.5 V
VDD	-10 mA to +10 mA, -0.5 to +3.0 V
V3P3D	-10 mA to +10 mA, -0.5 V to 4.6 V
VLCD	-10 mA to +10 mA, -0.5 V to +6 V
Analog Input Pins	
IADC0, IADC1, IADC2, IADC3, IADC4, IADC5, IADC6, IADC7, VADC8, VADC9 and VADC10	-10 mA to +10 mA -0.5 V to V3P3A+0.5 V
XIN, XOUT	-10 mA to +10 mA -0.5 V to +3.0 V
SEG and SEGDIO Pins	
Configured as SEG or COM drivers	-1 mA to +1 mA, -0.5 V to VLCD+0.5 V
Configured as Digital Inputs	-10 mA to +10 mA, -0.5 V to +6 V
Configured as Digital Outputs	-10 mA to +10 mA, -0.5 V to V3P3D+0.5 V
Digital Pins	
Inputs (PB, RESET, RX, ICE_E, TEST)	-10 mA to +10 mA, -0.5 to 6 V
Outputs (TX)	-10 mA to +10 mA, -0.5 V to V3P3D+0.5 V
Temperature	
Operating junction temperature (peak, 100ms)	140 °C
Operating junction temperature (continuous)	125 °C
Storage temperature	–45 °C to +165 °C
Soldering temperature – 10 second duration	250 °C

6.2 Recommended External Components

Table 87: Recommended External Components

Name	From	To	Function	Value	Unit
C1	V3P3A	GNDA	Bypass capacitor for 3.3 V supply	≥0.1 ±20%	µF
C2	V3P3D	GNDD	Bypass capacitor for 3.3 V output	0.1 ±20%	µF
CSYS	V3P3SYS	GNDD	Bypass capacitor for V3P3SYS	≥1.0 ±30%	µF
CVDD	VDD	GNDD	Bypass capacitor for VDD	0.1 ±20%	µF
CVLCD	VLCD	GNDD	Bypass capacitor for VLCD pin	≥0.1 ±20%	µF
XTAL	XIN	XOUT	32.768 kHz crystal – electrically equivalent to ECS .327-12.5-17X or Vishay XT26T, load capacitance 12.5 pF	32.768	kHz
CXS	XIN	GNDA	Load capacitor values for crystal depend on crystal specifications and board parasitics. Nominal values are based on 4 pF board capacitance and include an allowance for chip capacitance.	15 ±10%	pF
CXL	XOUT	GNDA		10 ±10%	pF

6.3 Recommended Operating Conditions

Unless otherwise specified, all parameters listed under 6.4 Performance Specifications and 6.5 Timing Specifications are valid over the Recommended Operating Conditions provided in Table 88 below.

Table 88: Recommended Operating Conditions

Parameter	Condition	Min	Typ	Max	Unit
V3P3SYS and V3P3A Supply Voltage for precision metering operation (MSN mode). Voltages at VBAT and VBAT_RTC need not be present.	VBAT=0 V to 3.8 V VBAT_RTC =0 V to 3.8 V	3.0		3.6	V
VBAT Voltage (BRN mode). V3P3SYS is below the 2.8 V comparator threshold. Either V3P3SYS or VBAT_RTC must be high enough to power the RTC module.	V3P3SYS < 2.8 V and Max(VBAT_RTC, V3P3SYS) > 2.0 V	2.5		3.8	V
VBAT_RTC Voltage. VBAT_RTC is not needed to support the RTC and non-volatile memory unless V3P3SYS<2.0 V	V3P3SYS<2.0 V	2.0		3.8	V
Operating Temperature		-40		+85	ºC

Notes:

1. GNDA and GNDD must be connected together.
2. V3P3SYS and V3P3A must be connected together.

6.4 Performance Specifications

6.4.1 Input Logic Levels

Table 89: Input Logic Levels

Parameter	Condition	Min	Typ	Max	Unit
Digital high-level input voltage[1], V_{IH}		2			V
Digital low-level input voltage[1], V_{IL}				0.8	V
Input pullup current, I_{IL} E_RXTX, E_RST, E_TCLK OPT_RX, OPT_TX SPI_CSZ (SEGDIO36) Other digital inputs	VIN=0 V, ICE_E=3.3 V	10 10 10 -1	 0	100 100 100 1	μA μA μA μA
Input pull down current, I_{IH} ICE_E, RESET, TEST Other digital inputs	VIN=V3P3D	10 -1	 0	100 1	μA μA

Note:

1. In battery powered modes, digital inputs should be below 0.1 V or above VBAT – 0.1 V to minimize battery current.

6.4.2 Output Logic Levels

Table 90: Output Logic Levels

Parameter	Condition	Min	Typ	Max	Unit
Digital high-level output voltage V_{OH}	I_{LOAD} = 1 mA	V3P3D–0.4			V
	I_{LOAD} = 15 mA (see notes 1, 2)	V3P3D-0.6			V
Digital low-level output voltage V_{OL}	I_{LOAD} = 1 mA	0		0.4	V
	I_{LOAD} = 15 mA (see note 1)	0		0.8	V

Note:

1. Guaranteed by design; not production tested.
2. **Caution:** The sum of all pull up currents must be compatible with the on-resistance of the internal V3P3D switch. See 6.4.6 V3P3D Switch on page 136.

6.4.3 Battery Monitor

Table 91: Battery Monitor Performance Specifications ($TEMP\_BAT$ = 1)

Parameter	Condition	Min	Typ	Max	Unit
BV: Battery Voltage (definition)	MSN mode, $TEMP\_PWR$ = 1 BRN mode, $TEMP\_PWR$=$TEMP\_BSEL$	$BV = 3.3V + (BSENSE - 142)\cdot 0.0246V + STEMP \cdot 297\mu V$ $BV = 3.291V + (BSENSE - 142)\cdot 0.0255V + STEMP \cdot 328\mu V$			V
Measurement Error $100\cdot\left(\frac{BV}{VBAT}-1\right)$	VBAT = 2.0 V 2.5 V 3.0 V 4.0 V	-7.5 -5 -3 -3		7.5 5 3 5	% % % %
Input impedance in continuous measurement, MSN mode. V(VBAT_RTC)/I(VBAT_RTC)	V3P3 = 3.3 V, $TEMP\_BSEL$ = 0, $TEMP\_PER$ = 111, VBAT_RTC = 3.6 V,	1			MΩ
Load applied with $BCURR$ IBAT($BCURR$=1) - IBAT($BCURR$=0)	V3P3 = 3.3 V	50	100	140	μA

6.4.4 Temperature Monitor

Table 92: Temperature Monitor

Parameter	Condition	Min	Typ	Max	Unit
Temperature Measurement Equation for 71M6543F and 71M6543G (see notes 2 and 3)	In MSN, *TEMP_PWR*=1: $$Temp = 0.325 \cdot STEMP + 22$$ In BRN, *TEMP_PWR* = *TEMP_BSEL*: $$Temp = 0.325 \cdot STEMP + 0.00218 \cdot BSENSE^2 - 0.609 \cdot BSENSE + 64.4$$				°C
Temperature Error (71M6543) (see note 1)	T_A = 22ºC	-2		2	°C
VBAT_RTC charge per measurement	*TEMP_BSEL* = 0, *TEMP_PWR*=0, SLP Mode, VBAT_RTC = 3.6 V		16		µC
Duration of temperature measurement after setting *TEMP_START* (see note 1)			15	60	ms

Notes:

1. Guaranteed by design; not production tested.
2. For the 71M6543F and 71M6543G, *TEMP_85* fuses read 0.
3. The coefficients provided in these equations are typical.

6.4.5 Supply Current

The supply currents provided in Table 93 below include only the current consumed by the 71M6543. Refer to the *71M6xxx Data Sheet* for additional current required when using a 71M6x03 remote sensor.

Table 93: Supply Current Performance Specifications

Parameter	Condition	Device	Min	Typ	Max	Unit
I1: **V3P3A + V3P3SYS** current, Normal Operation	**Polyphase: 4 Currents, 3 Voltages** **V3P3A = V3P3SYS** = 3.3 V, *MPU_DIV [2:0]*= 3 (614 kHz MPU clock), No Flash memory write, *RTM_E*=0, *PRE_E*=0, *CE_E*=1, *ADC_E*=1, *ADC_DIV*=0, *MUX_DIV[3:0]*=7, *FIR_LEN[1:0]*=1, *PLL_FAST*=1	71M6543F		7.2	8.5	mA
		71M6543G		7.5	8.8	mA
I1a: **V3P3A + V3P3SYS** current, ADC Half Rate (*ADC_DIV=1*)	Same as I1, except *ADC_DIV*=1, *FIR_LEN*=0	71M6543F		6.4	7.3	mA
		71M6543G		6.7	7.7	mA
I1b: **V3P3A + V3P3SYS** current, Normal Operation *PLL_FAST*=0	Same as I1, except *PLL_FAST*=0	71M6543F		2.9	3.8	mA
		71M6543G		3.0	3.9	mA
I1c: **V3P3A + V3P3SYS** current, Normal Operation *PRE_E*=1	Same as I1, except *PRE_E*=1	71M6543F		7.3	8.7	mA
		71M6543G		7.7	9.1	mA
I1d: **V3P3A + V3P3SYS** current, Normal Operation *PRE_E*=1, *ADC_DIV*=1, *FIR_LEN*=0. (see note 1)	Same as I1, except *PRE_E*=1, *ADC_DIV*=1, *FIR_LEN*=0.	71M6543F		6.5	7.5	mA
		71M6543G		6.9	7.9	mA
I1e: **V3P3A + V3P3SYS** current, Normal Operation *PLL_FAST*=0, *PRE_E*=1. (see note 1)	Same as I1, except *PRE_E*=1, *PLL_FAST*=0.	71M6543F		3.0	3.9	mA
		71M6543G		3.1	3.9	mA
I2: **V3P3A + V3P3SYS** dynamic current	Same as I1, except with variation of *MPU_DIV[2:0]*. $\frac{I_{MPU\_DIV=0} - I_{MPU\_DIV=3}}{4.3}$	71M6543F		0.4	0.6	mA/MHz
		71M6543G		0.5	0.65	mA/MHz
VBAT current						
I3: MSN Mode		71M6543	-300	0	300	nA
I4: BRN Mode	*CE_E*=0	71M6543F		2.4	3.2	mA
		71M6543G		2.6	3.5	mA
I5: LCD Mode (ext. VLCD)	*LCD_VMODE[1:0]*=3, also see note 3	71M6543		0.4	108	nA
I6: LCD Mode (boost, DAC)	*LCD_VMODE[1:0]*=2, also see notes 1, 2	71M6543		24	36	µA
I7: LCD Mode (DAC)	*LCD_VMODE[1:0]*=1, also see notes 1, 2	71M6543		3.0	11	µA
I8: LCD Mode (VBAT)	*LCD_VMODE[1:0]*=0, also see notes 1, 2	71M6543		1.1	3.4	µA
I9: SLP Mode	SLP Mode	71M6543	-300	0	+300	nA
VBAT_RTC current						
I10: MSN		71M6543	-300	0	300	nA
I11: BRN		71M6543F/G		240	410	nA
		71M6543G		260	420	nA
I12: LCD Mode	*LCD_VMODE[1:0]*=2, also see note 3	71M6543		1.8	4.1	µA
I13: SLP Mode	$T_A \le 25$ °C	71M6543		0.7	1.7	µA
I14: SLP Mode (see note 1)	$T_A = 85$ °C	71M6543		1.5	3.2	µA
I15: **V3P3A + V3P3SYS** current, Write Flash with ICE	Same as I1, except write Flash at maximum rate, *CE_E*=0, *ADC_E*=0.	71M6543F/G		7.1	8.7	mA
		71M6543G		7.3	8.7	mA

Notes:

1. Guaranteed by design; not production tested.
2. *LCD_DAC[4:0]*=5 (2.9V), *LCD_CLK[1:0]*=2, *LCD_MODE[2:0]*=6, all *LCD_MAPn* bits = 0.
3. *LCD_DAC[4:0]*=5 (2.9V), *LCD_CLK[1:0]*=2, *LCD_MODE[2:0]*=6, *LCD_BLANK*=0, *LCD_ON*=1, all *LCD_MAPn* bits = 1 and VLCD pin = 3.3V.

6.4.6 V3P3D Switch

Table 94: V3P3D Switch Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
On resistance – V3P3SYS to V3P3D	$\lvert I_{V3P3D} \rvert \le 1$ mA			10	Ω
On resistance – VBAT to V3P3D	$\lvert I_{V3P3D} \rvert \le 1$ mA, VBAT>2.5V			10	Ω
V3P3D I_{OH}, MSN	V3P3SYS = 3V V3P3D = 2.9V	10			mA
V3P3D I_{OH}, BRN	VBAT = 2.6V V3P3D = 2.5V	10			mA

6.4.7 Internal Power Fault Comparators

Table 95: Internal Power Fault Comparators Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
Overall response time	100mV overdrive, falling 100mV overdrive, rising	20		200 200	µs µs
Falling Threshold 3.0 V Comparator 2.8 V Comparator Difference 3.0V and 2.8V Comparators	V3P3 falling	 2.83 2.75 50	 2.93 2.81 136	 3.03 2.87 220	 V V mV
Falling Threshold 2.25 V Comparator 2.0 V Comparator VDD (@VBAT=3.0V) – 2.25V Comparator Difference 2.25V and 2.0V Comparators	VDD falling	 2.2 1.90 0.25 0.15	 2.25 2.00 0.35 0.25	 2.5 2.20 0.45 0.35	 V V V V
Hysteresis, (Rising Threshold - Falling Threshold) 3.0 V Comparator 2.8 V Comparator 2.25 V Comparator 2.0 V Comparator	T_A = 22 °C	 22 25 10 10	 45 42 33 28	 65 60 60 60	 mV mV mV mV

6.4.8 2.5 V Voltage Regulator – System Power

Table 96: 2.5 V Voltage Regulator Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
V2P5	V3P3 = 3.0 V - 3.8 V I_{LOAD} = 0 mA	2.55	2.65	2.75	V
V2P5 load regulation	V3P3 = 3.3 V I_{LOAD} = 0 mA to 5 mA			40	mV
Voltage overhead V3P3SYS-V2P5	I_{LOAD} = 5 mA, Reduce V3P3D until V2P5 drops 200 mV			440	mV

6.4.9 2.5 V Voltage Regulator – Battery Power

Table 97: Low-Power Voltage Regulator Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
V2P5	VBAT = 3.0 V - 3.8 V, V3P3 = 0 V, I_{LOAD} = 0 mA	2.55	2.65	2.75	V
V2P5 load regulation	VBAT = 3.3 V, V3P3 = 0 V, I_{LOAD} = 0 mA to 1 mA			40	mV
Voltage Overhead 2V − VBAT-VDD	I_{LOAD} = 0ma, VBAT = 2.0 V, V3P3 = 0 V.			200	mV

6.4.10 Crystal Oscillator

Table 98: Crystal Oscillator Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
Maximum Output Power to Crystal	Crystal connected, see note 1			1	μW
XIN to XOUT Capacitance (see note 1)				3	pF
Capacitance change on XOUT	*RTCA_ADJ* = 7F to 0, Bias voltage = unbiased Vpp = 0.1 V		15		pF
Note: 1. Guaranteed by design; not production tested.					

6.4.11 Phase-Locked Loop (PLL)

Table 99: PLL Performance Specifications

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
PLL Power-up Settling Time	*PLL_FAST* =0, V3P3 = 0 to 3.3 V step Measured from first edge of MCK (TMUX2OUT pin)		3		ms
PLL_FAST settling time PLL_FAST rise PLL_FAST fall	V3P3=0, VBAT=3.8 to 2.0 V		 3 3		 ms ms
PLL SLP to MSN Settling Time	*PLL_FAST* =0		3		ms

6.4.12 LCD Drivers

Table 100: LCD Drivers Performance Specifications

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
VLCD Current	VLCD=3.3, all LCD map bits=0 VLCD=5.0, all LCD map bits=0			2 3	uA uA
Note: 1. These specifications apply to all COM and SEG pins. 1. *LCD_VMODE*=3, *LCD_ON*=1, *LCD_BLANK*=0, *LCD_MODE*=6, *LCD_CLK*=2. 2. Output load is 74 pF per SEG and COM pin.					

6.4.13 VLCD Generator

Table 101: VLCD Generator Specifications

Parameter	Condition	Min	Typ	Max	Unit
VSYS to VLCD switch impedance	V3P3 = 3.3 V, RVLCD=removed, *LCD_BAT*=0, *LCD_VMODE[1:0]*=0, ΔILCD=10 µA			750	Ω
VBAT to VLCD switch impedance	V3P3 = 0 V, VBAT = 2.5 V, RVLCD =removed, *LCD_BAT* =1, *LCD_VMODE[1:0]*=0, ΔILCD=10 µA			700	Ω
LCD Boost Frequency	*LCD_VMODE[1:0]* = 2, RVLCD = removed, CVLCD = removed *PLL_FAST*=1 *PLL_FAST*=0		 820 786		 kHz kHz
VLCD IOH current (VLCD(0)-VLCD(IOH)<0.25)	*LCD_VMODE[1:0]* = 2, *LCD_CLK[1:0]* = 2, RVLCD = removed, V3P3 = 3.3V, *LCD_DAC[4:0]* = 1F	10			µA
From *LCDADJ0* and *LCDADJ12* fuses: $LCDADJ(LCD\_DAC) = 5mV\left[LCDADJ0 + \frac{LCDADJ12 - LCDADJ0}{12} LCD\_DAC\right]$ $VLCD_{NOM}(LCD\_DAC) = 2.65 + 2.65\frac{LCD\_DAC}{31} + LCDADJ(LCD\_DAC)$ The above equations describe the nominal value of VLCD for a specific LCD_DAC value. The specifications below list the maximum deviation between actual VLCD and VLCDnom. Note that when VCC and boost are insufficient, the LCD DAC will not reach its target value and a large negative error will occur.					
LCD_DAC Error. VLCD-VLCDnom Full Scale, with Boost V3P3 =3.6 V V3P3 =3.0 V VBAT=4.0 V, V3P3=0, BRN Mode VBAT=2.5 V, V3P3=0, BRN Mode	*LCD_VMODE* = 10, *LCD_DAC[4:0]* = 1F, *LCD_CLK[1:0]*=2, *LCD_MODE[2:0]*=6	 -0.15 -0.4 -0.15 -1.3		 0.15 0.15 0.15	 V V V V
LCD_DAC Error. VLCD-VLCDnom DAC=12, with Boost V3P3 = 3.6 V V3P3 = 3.0 V VBAT = 2.5 V, V3P3 = 0 V, BRN Mode	*LCD_VMODE* = 10, *LCD_DAC[4:0]* = C, *LCD_CLK[1:0]*=2, *LCD_MODE[2:0]*=6	 -0.15 -0.15 -0.15		 0.15 0.15 0.15	 V V V
LCD_DAC Error. VLCD-VLCDnom Zero Scale, with Boost V3P3 = 3.6 V V3P3 = 3.0 V VBAT = 4.0 V, V3P3 = 0 V, BRN Mode VBAT = 2.5 V, V3P3 = 0 V, BRN Mode	*LCD_VMODE* = 2, *LCD_DAC[4:0]* =0, *LCD_CLK[1:0]*=2, *LCD_MODE[2:0]*=6	 -0.15 -0.15 -0.15 -0.15		 0.15 0.15 0.15 0.15	 V V V V
LCD_DAC Error. VLCD-VLCDnom Full Scale, no Boost V3P3 = 3.6 V (see note 1) V3P3 = 3.0 V (see note 1) VBAT = 4.0 V, V3P3 = 0 V, BRN Mode VBAT = 2.5 V, V3P3 = 0 V, BRN Mode	*LCD_VMODE* = 1, *LCD_DAC[4:0]* = 1F, *LCD_CLK[1:0]*=2, *LCD_MODE[2:0]*=6	 -2.1 -2.8 -1.8 -3.2			 V V V V
LCD_DAC Error. VLCD-VLCDnom DAC=12, no Boost V3P3 = 3.6 V V3P3 = 3.0 V VBAT = 4.0 V, V3P3 = 0 V, BRN Mode VBAT = 2.5 V, V3P3 = 0 V, BRN Mode	*LCD_VMODE* = 1, *LCD_DAC[4:0]* = C, *LCD_CLK[1:0]*=2, *LCD_MODE[2:0]*=6	 -0.5 -1.1 -0.15[1] -1.5[1]		 0.15[1]	 V V V V

Parameter	Condition	Min	Typ	Max	Unit
LCD_DAC Error. VLCD-VLCDnom Zero Scale, no Boost V3P3 = 3.6 V V3P3 = 3.0 V VBAT = 4.0 V, V3P3 = 0 V, BRN Mode VBAT = 2.5 V, V3P3 = 0 V, BRN Mode	*LCD_VMODE* = 01, *LCD_DAC[4:0]* = 0, *LCD_CLK[1:0]*=2, *LCD_MODE[2:0]*=6	 -0.15 -0.15 -0.15 -0.45		 0.15 0.15 0.15 0.15	 V V V V
LCD_DAC Error. VLCD-VLCDnom Full Scale, with Boost, LCD mode VBAT = 4.0 V, V3P3 = 0 V VBAT = 2.5 V, V3P3 = 0 V	*LCD_VMODE* = 1, *LCD_DAC[4:0]* = 1F, *LCD_CLK[1:0]*=2, *LCD_MODE[2:0]*=6	 -0.15 -1.3		 0.15	 V V

Note:

1. Guaranteed by design; not production tested.
2. The following test conditions also apply to all parameters provided in this table: bypass capacitor CVLCD ≥ 0.1 μF, test load RVLCD = 500 kΩ, no display, all SEGDIO pins configured as DIO.

6.4.14 71M6543 VREF

Table 102 shows the performance specifications for the 71M6543 ADC reference voltage (VREF).

Table 102: 71M6543 VREF Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
VREF output voltage, VREF(22)	T_A = 22 ºC	1.193	1.195	1.197	V
VREF output voltage, VREF(22)	*PLL_FAST*=0		1.195		V
VREF chop step, trimmed	VREF(CHOP=01) − VREF(CHOP=10)	-10		10	mV
VREF power supply sensitivity ΔVREF / ΔV3P3A	V3P3A = 3.0 to 3.6 V	-1.5		1.5	mV/V
VREF input impedance	*VREF_DIS* = 1, VREF = 1.3 V to 1.7 V	100			kΩ
VREF output impedance	*VREF_CAL* = 1, I_{LOAD} = 10 µA, -10 µA			3.2	kΩ
VNOM definition (see note 2)	$VNOM(T) = VREF(22) + (T-22)TC1 + (T-22)^2 TC2$				V
If temperature characterization trim information is not available (71M6543F and 71M6543G)					
VNOM temperature coefficients: TC1 = TC2 =	$275 - 4.95 \cdot TRIMT$ $-0.557 - 0.00028 \cdot TRIMT$				µV/°C µV/°C²
VREF(T) deviation from VNOM(T) (see note 1): $\frac{VREF(T)-VNOM(T)}{VNOM(T)} \frac{10^6}{62}$		-40		+40	ppm/°C
VREF aging			±25		ppm/ year

Notes:

1. Guaranteed by design; not production tested.
2. This relationship describes the nominal behavior of VREF at different temperatures, as governed by a second order polynomial of 1st and 2nd order coefficients TC1 and TC2.
3. For the parameters in this table, unless otherwise specified, *VREF_DIS* = 0, *PLL_FAST*=1

6.4.15 ADC Converter

Table 103: ADC Converter Performance Specifications

<table>
<tr><th>Parameter</th><th>Condition</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>Recommended Input Range
(Vin - V3P3A)</td><td></td><td>-250</td><td></td><td>250</td><td>mV
peak</td></tr>
<tr><td>Voltage to Current Crosstalk
$\frac{10^6 * Vcrosstalk}{Vin} \cos(\angle Vin - \angle Vcrosstalk)$
(see note 1)</td><td>Vin = 200 mV peak,
65 Hz, on VADC8 (VA) or VADC9 (VB) or VADC10 (VC).
$Vcrosstalk$ = largest measurement on IADC0-1 or IADC2-3 or IADC4-5 or IADC6-7</td><td>-10</td><td></td><td>10</td><td>μV/V</td></tr>
<tr><td>Input Impedance, no pre-amp</td><td>Vin=65 Hz</td><td>40</td><td></td><td>90</td><td>kΩ</td></tr>
<tr><td>ADC Gain Error vs %Power Supply Variation
$\frac{10^6 \, \Delta Nout_{PK} \, 357nV / V_{IN}}{100 \Delta V3P3A / 3.3}$</td><td>Vin=200 mV pk, 65 Hz
V3P3A=3.0 V, 3.6 V</td><td></td><td></td><td>50</td><td>ppm / %</td></tr>
<tr><td>Input Offset
IADC0=IADC1=V3P3A
IADC0=V3P3A</td><td>
$DIFF0\_E$=1, PRE_E=0
$DIFF0\_E$=0, PRE_E=0</td><td>
-10
-10</td><td></td><td>
10
10</td><td>
mV
mV</td></tr>
<tr><td>THD @ 250mVpk
<table>
<tr><th>Name</th><th>FIR_LEN</th><th>ADC_DIV</th><th>PLL_FAST</th><th>MUX_DIV</th></tr>
<tr><td>A</td><td>0</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td>B</td><td>1</td><td>0</td><td>0</td><td>2</td></tr>
<tr><td>C</td><td>0</td><td>0</td><td>1</td><td>11</td></tr>
<tr><td>D</td><td>1</td><td>0</td><td>1</td><td>6</td></tr>
<tr><td>E</td><td>2</td><td>0</td><td>1</td><td>4</td></tr>
<tr><td>F</td><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>G</td><td>0</td><td>1</td><td>1</td><td>6</td></tr>
<tr><td>H</td><td>1</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>J</td><td>2</td><td>1</td><td>1</td><td>2</td></tr>
</table></td><td>V_{IN} = 65Hz, 250mVpk,
64kpts FFT, Blackman Harris Window.</td><td></td><td>
<table>
<tr><td>A</td><td></td></tr>
<tr><td>B</td><td>-82</td></tr>
<tr><td>C</td><td></td></tr>
<tr><td>D</td><td>-84</td></tr>
<tr><td>E</td><td></td></tr>
<tr><td>F</td><td>-83</td></tr>
<tr><td>G</td><td></td></tr>
<tr><td>H</td><td>-86</td></tr>
<tr><td>J</td><td></td></tr>
</table></td><td>
<table>
<tr><td>A</td><td>-75</td></tr>
<tr><td>B</td><td>-75</td></tr>
<tr><td>C</td><td>-75</td></tr>
<tr><td>D</td><td>-75</td></tr>
<tr><td>E</td><td>-75</td></tr>
<tr><td>F</td><td>-75</td></tr>
<tr><td>G</td><td>-75</td></tr>
<tr><td>H</td><td>-75</td></tr>
<tr><td>J</td><td>-75</td></tr>
</table></td><td>dB</td></tr>
<tr><td>THD @ 20mVpk
<table>
<tr><th>Name</th><th>FIR_LEN</th><th>ADC_DIV</th><th>PLL_FAST</th><th>MUX_DIV</th></tr>
<tr><td>A</td><td>0</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td>B</td><td>1</td><td>0</td><td>0</td><td>2</td></tr>
<tr><td>C</td><td>0</td><td>0</td><td>1</td><td>11</td></tr>
<tr><td>D</td><td>1</td><td>0</td><td>1</td><td>6</td></tr>
<tr><td>E</td><td>2</td><td>0</td><td>1</td><td>4</td></tr>
<tr><td>F</td><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>G</td><td>0</td><td>1</td><td>1</td><td>6</td></tr>
<tr><td>H</td><td>1</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>J</td><td>2</td><td>1</td><td>1</td><td>2</td></tr>
</table></td><td>V_{IN} = 65Hz, 20mVpk,
64kpts FFT, Blackman Harris Window.</td><td></td><td>
<table>
<tr><td>A</td><td>-85</td></tr>
<tr><td>B</td><td>-91</td></tr>
<tr><td>C</td><td>-85</td></tr>
<tr><td>D</td><td>-91</td></tr>
<tr><td>E</td><td>-93</td></tr>
<tr><td>F</td><td>-85</td></tr>
<tr><td>G</td><td>-85</td></tr>
<tr><td>H</td><td>-91</td></tr>
<tr><td>J</td><td>-93</td></tr>
</table></td><td></td><td>dB</td></tr>
<tr><td>LSB Size:
<table>
<tr><th>Name</th><th>FIR_LEN</th><th>ADC_DIV</th><th>PLL_FAST</th><th>MUX_DIV</th></tr>
<tr><td>A</td><td>0</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td>B</td><td>1</td><td>0</td><td>0</td><td>2</td></tr>
<tr><td>C</td><td>0</td><td>0</td><td>1</td><td>11</td></tr>
<tr><td>D</td><td>1</td><td>0</td><td>1</td><td>6</td></tr>
<tr><td>E</td><td>2</td><td>0</td><td>1</td><td>4</td></tr>
<tr><td>F</td><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>G</td><td>0</td><td>1</td><td>1</td><td>6</td></tr>
<tr><td>H</td><td>1</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>J</td><td>2</td><td>1</td><td>1</td><td>2</td></tr>
</table></td><td>Vin=65Hz, 20mVpk,
64kpts FFT, Blackman-Harris window</td><td></td><td>
<table>
<tr><td>A</td><td>3470</td></tr>
<tr><td>B</td><td>406</td></tr>
<tr><td>C</td><td>3040</td></tr>
<tr><td>D</td><td>357</td></tr>
<tr><td>E</td><td>151</td></tr>
<tr><td>F</td><td>3470</td></tr>
<tr><td>G</td><td>3040</td></tr>
<tr><td>H</td><td>357</td></tr>
<tr><td>J</td><td>151</td></tr>
</table></td><td></td><td>nV</td></tr>
<tr><td>Digital Full-Scale:
<table>
<tr><th>Name</th><th>FIR_LEN</th><th>ADC_DIV</th><th>PLL_FAST</th><th>MUX_DIV</th></tr>
<tr><td>A</td><td>0</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td>B</td><td>1</td><td>0</td><td>0</td><td>2</td></tr>
<tr><td>C</td><td>0</td><td>0</td><td>1</td><td>11</td></tr>
<tr><td>D</td><td>1</td><td>0</td><td>1</td><td>6</td></tr>
<tr><td>E</td><td>2</td><td>0</td><td>1</td><td>4</td></tr>
<tr><td>F</td><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>G</td><td>0</td><td>1</td><td>1</td><td>6</td></tr>
<tr><td>H</td><td>1</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>J</td><td>2</td><td>1</td><td>1</td><td>2</td></tr>
</table></td><td></td><td></td><td>A: ±91125
B: ±778688
C: ±103823
D: ±884736
E: ±2097152
F: ±91125
G: ±103823
H: ±884736
J: ±2097152</td><td></td><td>LSB</td></tr>
</table>

Parameter	Condition	Min	Typ	Max	Unit
Note: 1. Guaranteed by design; not production tested. 2. Unless stated otherwise, the following test conditions apply to all the parameters provided in this table: *FIR_LEN[1:0]*=1, *VREF_DIS*=0, *PLL_FAST*=1, *ADC_DIV*=0, *MUX_DIV*=6, LSB values do not include the 9-bit left shift at CE input.					

6.4.16 Pre-Amplifier for IADC0-IADC1

Table 104: Pre-Amplifier Performance Specifications

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Differential Gain Vin=30mV differential Vin=15mV differential (see note 1)	T_A= 5ºC, V3P3=3.3 V, *PRE_E*=1, *FIR_LEN*=2, *DIFF0_E*=1, 2520Hz sample rate	7.8 7.8	7.92 7.92	8.0 8.0	V/V V/V
Gain Variation vs V3P3 Vin=30mV differential (see note 1)	V3P3 = 2.97 V, 3.63 V	-100		100	ppm/%
Gain Variation vs Temp Vin=30mV differential (see note 1)	T_A = -40ºC, 85ºC	10	-25	-80	ppm/C
Phase Shift, Vin=30mV differential (see note 1)	T_A=25ºC, V3P3=3.3 V	-6		6	mº
Preamp input current IADC0 IADC1	*PRE_E*=1, *FIR_LEN*=10, *DIFF0_E*=1 2520Hz sample rate, IADC0=IADC1=V3P3	4 4	9 9	16 16	uA uA
Preamp+ADC THD Vin=30mV differential Vin=15mV differential	T_A=25ºC, V3P3=3.3 V, *PRE_E*=1, *FIR_LEN*=2, *DIFF0_E*=1, 2520Hz sample rate.		-82 -86		dB dB
Preamp Offset IADC0=IADC1=V3P3+30mV IADC0=IADC1= V3P3+15mV IADC0=IADC1= V3P3 IADC0=IADC1= V3P3-15mV IADC0=IADC1= V3P3-30mV	T_A=25ºC, V3P3=3.3 V, *PRE_E*=1, *FIR_LEN*=10, *DIFF0_E*=1, 2520Hz sample rate		-0.63 -0.57 -0.56 -0.56 -0.55		mV mV mV mV mV
Note: 1. Guaranteed by design; not production tested.					

6.5 Timing Specifications

6.5.1 Flash Memory

Table 105: Flash Memory Timing Specifications

Parameter	Condition	Min	Typ	Max	Unit
Flash write cycles	-40 °C to +85 °C	20,000			Cycles
Flash data retention	25 °C 85 °C	100 10			Years
Flash byte writes between page or mass erase operations				2	Cycles
Write Time per Byte				21	µs
Page Erase (1024 bytes)				21	ms
Mass Erase				21	ms

6.5.2 SPI Slave

Table 106. SPI Slave Timing Specifications

Parameter	Condition	Min	Typ	Max	Unit
SPI Setup Time	SPI_DI to SPI_CK rise	10			ns
SPI Hold Time	SPI_CK rise to SPI_DI	10			ns
SPI Output Delay	SPI_CK fall to SPI_D0			40	ns
SPI Recovery Time	SPI_CSZ fall to SPI_CK	10			ns
SPI Removal Time	SPI_CK to SPI_CSZ rise	15			ns
SPI Clock High		40			ns
SPI Clock Low		40			ns
SPI Clock Freq	SPI Freq/MPU Freq			2.0	MHz/MHz
SPI Transaction Space	SPI_CSZ rise to SPI_CSZ fall	4.5			MPU Cycles

6.5.3 EEPROM Interface

Table 107: EEPROM Interface Timing

Parameter	Condition	Min	Typ	Max	Unit
Write Clock frequency (I^2C)	CKMPU = 4.9 MHz, Using interrupts		310		kHz
	CKMPU = 4.9 MHz, bit-banging DIO2/3 *PLL_FAST* = 0		100		kHz
Write Clock frequency (3-wire)	CKMPU = 4.9 MHz *PLL_FAST* = 0 *PLL_FAST* = 1		 160 500		kHz

6.5.4 RESET Pin

Table 108: RESET Pin Timing

Parameter	Condition	Min	Typ	Max	Unit
Reset pulse width		5			µs
Reset pulse fall time (see note 1)				1	µs
Note: 1. Guaranteed by design; not production tested.					

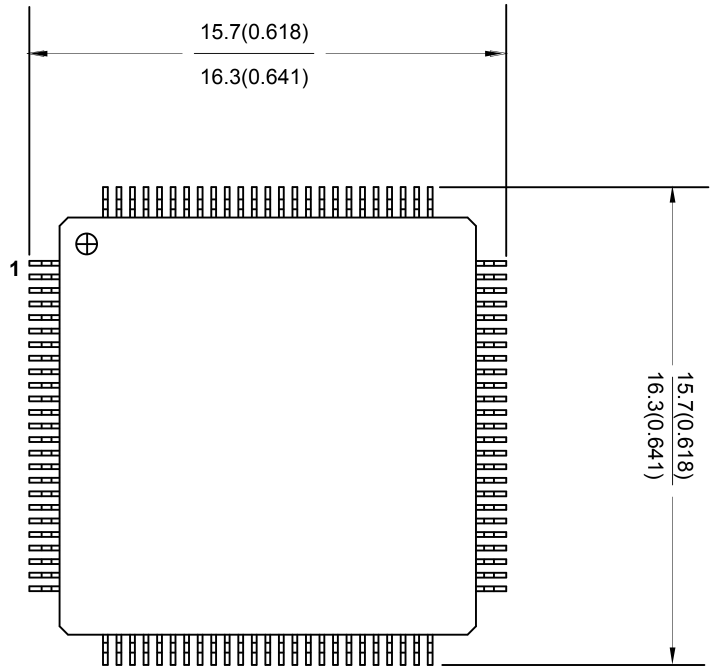
6.5.5 Real-Time Clock (RTC)

Table 109: RTC Range for Date

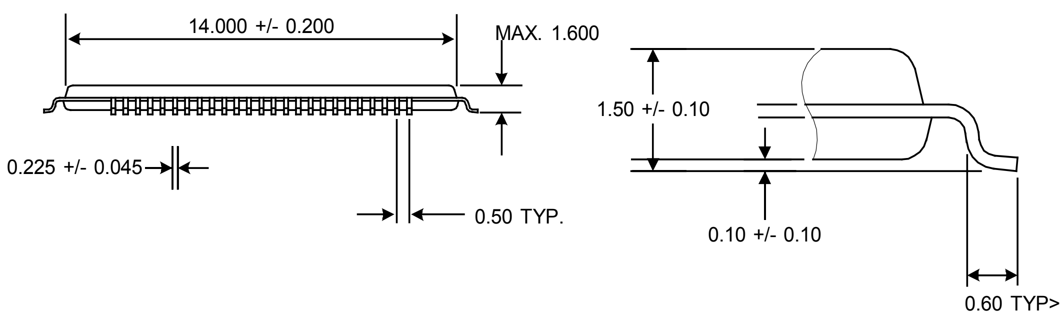
Parameter	Condition	Min	Typ	Max	Unit
Range for date		2000	–	2255	year

6.6 100-Pin LQFP Package Outline Drawing

Controlling dimensions are in mm.



Top View



Side View

Figure 41: 100-pin LQFP Package Outline

6.7 71M6543 Pinout

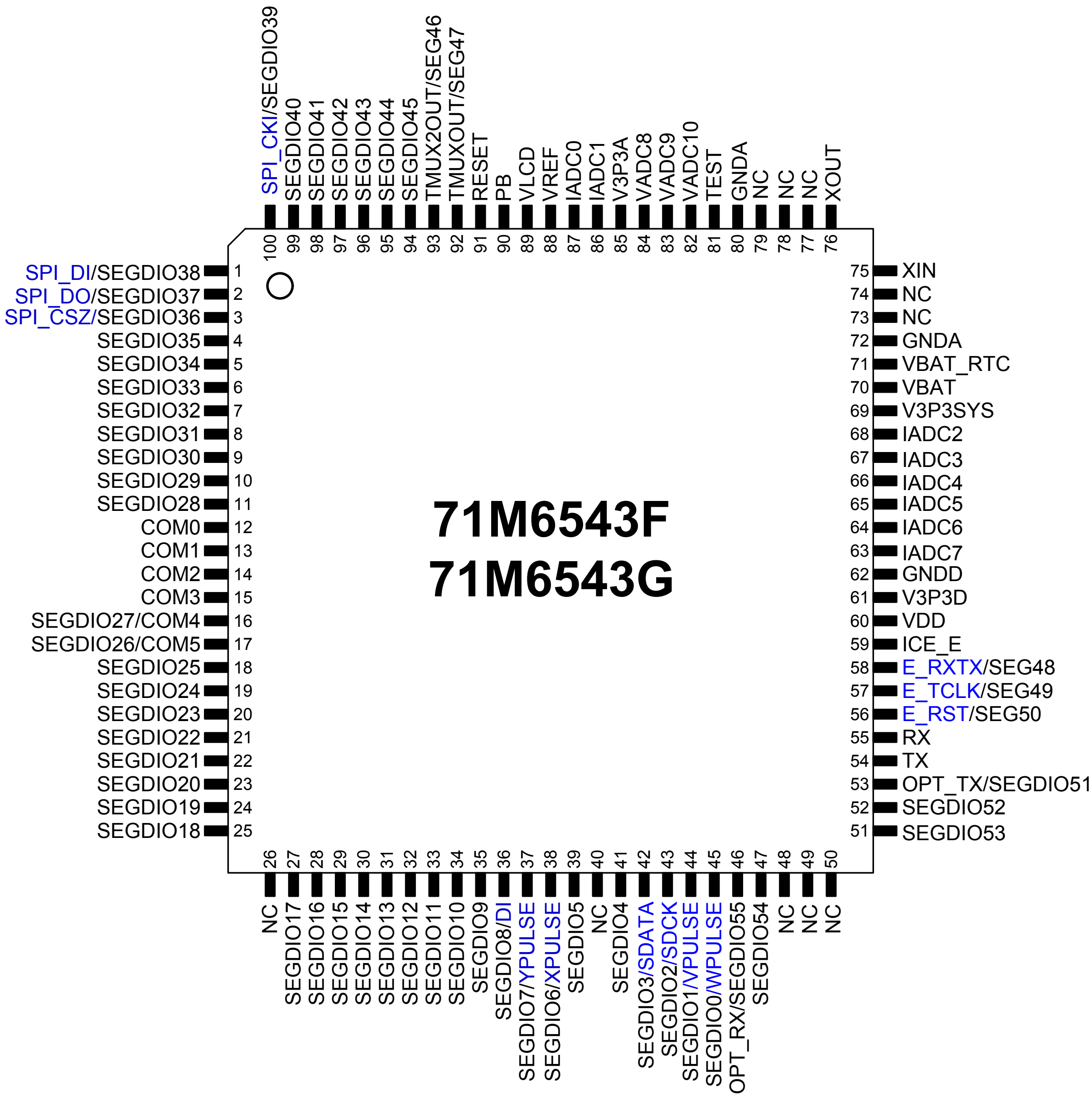


Figure 42: Pinout for the LQFP-100 Package

6.8 71M6543 Pin Descriptions

6.8.1 71M6543 Power and Ground Pins

Pin types: P = Power, O = Output, I = Input, I/O = Input/Output. The circuit number denotes the equivalent circuit, as specified under Section 6.8.4 I/O Equivalent Circuits.

Table 110: 71M6543 Power and Ground Pins

Pin	Name	Type	Circuit	Function
72, 80	GNDA	P	—	Analog Ground. This pin should be connected directly to the ground plane.
62	GNDD	P	—	Digital Ground. This pin should be connected directly to the ground plane.
85	V3P3A	P	—	Analog Power Supply. A 3.3 V power supply should be connected to this pin. V3P3A must be the same voltage as V3P3SYS.
69	V3P3SYS	P	—	System 3.3 V Supply. This pin should be connected to a 3.3 V power supply.
61	V3P3D	O	13	Auxiliary Voltage Output of the Chip. In mission mode, this pin is connected to V3P3SYS by the internal selection switch. In BRN mode, it is internally connected to VBAT. V3P3D is floating in LCD and sleep mode. A bypass capacitor to ground should not exceed 0.1 µF.
60	VDD	O	—	Output of the 2.5 V Regulator. This pin is powered in MSN and BRN modes. A 0.1 µF bypass capacitor to ground should be connected to this pin.
89	VLCD	O	—	Output of the LCD DAC. A 0.1 µF bypass capacitor to ground should be connected to this pin.
70	VBAT	P	12	Battery Backup Pin to Support the Battery Modes (BRN, LCD). A battery or super capacitor is to be connected between VBAT and GNDD. If no battery is used, connect VBAT to V3P3SYS.
71	VBAT_RTC	P	12	RTC and Oscillator Power Supply. A battery or super-capacitor is to be connected between VBAT and GNDD. If no battery is used, connect VBAT_RTC to V3P3SYS.

6.8.2 71M6543 Analog Pins

Pin types: P = Power, O = Output, I = Input, I/O = Input/Output. The circuit number denotes the equivalent circuit, as specified in Section 6.8.4.

Table 111: 71M6543 Analog Pins

Pin	Name	Type	Circuit	Function
87 86	IADC0 IADC1	I	6	Differential or Single-Ended Analog Line Current Sense Inputs. These pins are voltage inputs to the internal A/D converter. Typically, they are connected to the outputs of current sensors. **Unused pins must be connected to V3P3A**. When configured as differential inputs (i.e., by setting the *DIFFx_E* control bits, where x = 0, 2, 4, 6) pins are paired to form differential inputs pairs: IADC0-IADC1, IADC2-IADC3, IADC4-IADC5, and IADC6-IADC7. IADC2-IADC3, IADC4-IADC5, and IADC6-IADC7 can be configured for communication with the 71M6xx3 remote isolated sensor interface (i.e., by setting the *RMTx_E* control bits, where x = 2, 4, 6). When configured as remote sensor interfaces, these pins form balanced digital pairs for bidirectional digital communications with a 71M6xx3 remote isolated sensor.
68 67	IADC2 IADC3			
66 65	IADC4 IADC5			
64 63	IADC6 IADC7			
84	VADC8 (VA)	I	6	Line Voltage Sense Inputs. These pins are voltage inputs to the internal A/D converter. Typically, they are connected to the outputs of resistor dividers. **Unused pins must be connected to V3P3A.**
83	VADC9 (VB)			
82	VADC10 (VC)			
88	VREF	O	9	Voltage Reference for the ADC. This pin should be left unconnected (floating).
75	XIN	I	8	Crystal Inputs. A 32 kHz crystal should be connected across these pins. Typically, a 15 pF capacitor is also connected from XIN to GNDA and a 10 pF capacitor is connected from XOUT to GNDA. It is important to minimize the capacitance between these pins. See the crystal manufacturer data sheet for details. If an external clock is used, a 150 mV (p-p) clock signal should be applied to XIN, and XOUT should be left unconnected.
76	XOUT	O		

6.8.3 71M6543 Digital Pins

Pin types: P = Power, O = Output, I = Input, I/O = Input/Output, N/C = no connect. The circuit number denotes the equivalent circuit, as specified in Section 6.8.4.

Table 112: 71M6543 Digital Pins

<table>
<tr><th>Pin</th><th>Name</th><th>Type</th><th>Circuit</th><th>Function</th></tr>
<tr><td>12–15</td><td>COM0–COM3</td><td>O</td><td>5</td><td>LCD Common Outputs. These four pins provide the select signals for the LCD display.</td></tr>
<tr><td>45</td><td>SEGDIO0/WPULSE</td><td rowspan="16">I/O</td><td rowspan="16">3, 4, 5</td><td rowspan="16">Multiple-Use Pins. Configurable as either LCD segment driver or DIO. Alternative functions with proper selection of associated I/O RAM registers are:
SEGDIO0 = WPULSE (45)
SEGDIO1 = VPULSE (44)
SEGDIO2 = SDCK (43)
SEGDIO3 = SDATA (42)
SEGDIO6 = XPULSE (38)
SEGDIO7 = YPULSE (37)
SEGDIO8 = DI (36)

Unused pins must be configured as outputs or terminated to V3P3/GNDD.</td></tr>
<tr><td>44</td><td>SEGDIO1/VPULSE</td></tr>
<tr><td>43</td><td>SEGDIO2/SDCK</td></tr>
<tr><td>42</td><td>SEGDIO3/SDATA</td></tr>
<tr><td>41</td><td>SEGDIO4</td></tr>
<tr><td>39</td><td>SEGDIO5</td></tr>
<tr><td>38</td><td>SEGDIO6/XPULSE</td></tr>
<tr><td>37</td><td>SEGDIO7/YPULSE</td></tr>
<tr><td>36</td><td>SEGDIO8/DI</td></tr>
<tr><td>35–27</td><td>SEGDIO[9:17]</td></tr>
<tr><td>25–18</td><td>SEGDIO[18:25]</td></tr>
<tr><td>11–4</td><td>SEGDIO[28:35]</td></tr>
<tr><td>99–94</td><td>SEGDIO[40:45]</td></tr>
<tr><td>52</td><td>SEGDIO52</td></tr>
<tr><td>51</td><td>SEGDIO53</td></tr>
<tr><td>47</td><td>SEGDIO54</td></tr>
<tr><td>17</td><td>SEGDIO26/COM5</td><td rowspan="2">I/O</td><td rowspan="2">3, 4, 5</td><td rowspan="2">Multiple-Use Pins. Configurable as either LCD segment driver or DIO with alternative function (LCD common drivers).</td></tr>
<tr><td>16</td><td>SEGDIO27/COM4</td></tr>
<tr><td>3</td><td>SPI_CSZ/SEGDIO36</td><td rowspan="4">I/O</td><td rowspan="4">3, 4, 5</td><td rowspan="4">Multiple-Use Pins. Configurable as either LCD segment driver or DIO with alternative function (SPI interface).</td></tr>
<tr><td>2</td><td>SPI_DO/SEGDIO37</td></tr>
<tr><td>1</td><td>SPI_DI/SEGDIO38</td></tr>
<tr><td>100</td><td>SPI_CKI/SEGDIO39</td></tr>
<tr><td>53</td><td>OPT_TX/SEGDIO51</td><td rowspan="2">I/O</td><td rowspan="2">3, 4, 5</td><td rowspan="2">Multiple-Use Pins, configurable as either LCD segment driver or DIO with alternative function (optical port/UART1)</td></tr>
<tr><td>46</td><td>OPT_RX/SEGDIO55</td></tr>
<tr><td>58</td><td>E_RXTX/SEG48</td><td rowspan="2">I/O</td><td rowspan="2">1, 4, 5</td><td rowspan="3">Multiuse Pins. Configurable as either emulator port pins (when ICE_E pulled high) or LCD segment drivers (when ICE_E tied to GND).</td></tr>
<tr><td>56</td><td>E_RST/SEG50</td></tr>
<tr><td>57</td><td>E_TCLK/SEG49</td><td>O</td><td>4, 5</td></tr>
<tr><td>59</td><td>ICE_E</td><td>I</td><td>2</td><td>ICE Enable. When zero, E_RST, E_TCLK, and E_RXTX become SEG50, SEG49, and SEG48 respectively. For production units, this pin should be pulled to GND to disable the emulator port.</td></tr>
<tr><td>92</td><td>TMUXOUT/SEG47</td><td rowspan="2">O</td><td rowspan="2">4, 5</td><td rowspan="2">Multiple-Use Pins. Configurable as either multiplexer/clock output or LCD segment driver using the I/O RAM registers.</td></tr>
<tr><td>93</td><td>TMUX2OUT/SEG46</td></tr>
</table>

Pin	Name	Type	Circuit	Function
91	RESET	I	2	Chip Reset. This input pin is used to reset the chip into a known state. For normal operation, this pin is pulled low. To reset the chip, this pin should be pulled high. This pin has an internal 30 μA (nominal) current source pulldown. No external reset circuitry is necessary.
55	RX	I	3	UART0 Input. **If this pin is unused it must be terminated to V3P3D or GNDD.**
54	TX	O	4	UART0 Output
81	TEST	I	7	Enables Production Test. **This pin must be grounded in normal operation.**
90	PB	I	3	Pushbutton Input. This pin must be at GNDD when not active or unused. A rising edge sets the *WF_PB* flag. It also causes the part to wake up if it is in SLP or LCD mode. PB does not have an internal pullup or pulldown resistor.
26, 40, 48, 49, 50, 73, 74, 77, 78, 79	NC	N/C	—	No Connection. Do not connect this pin.

6.8.4 I/O Equivalent Circuits

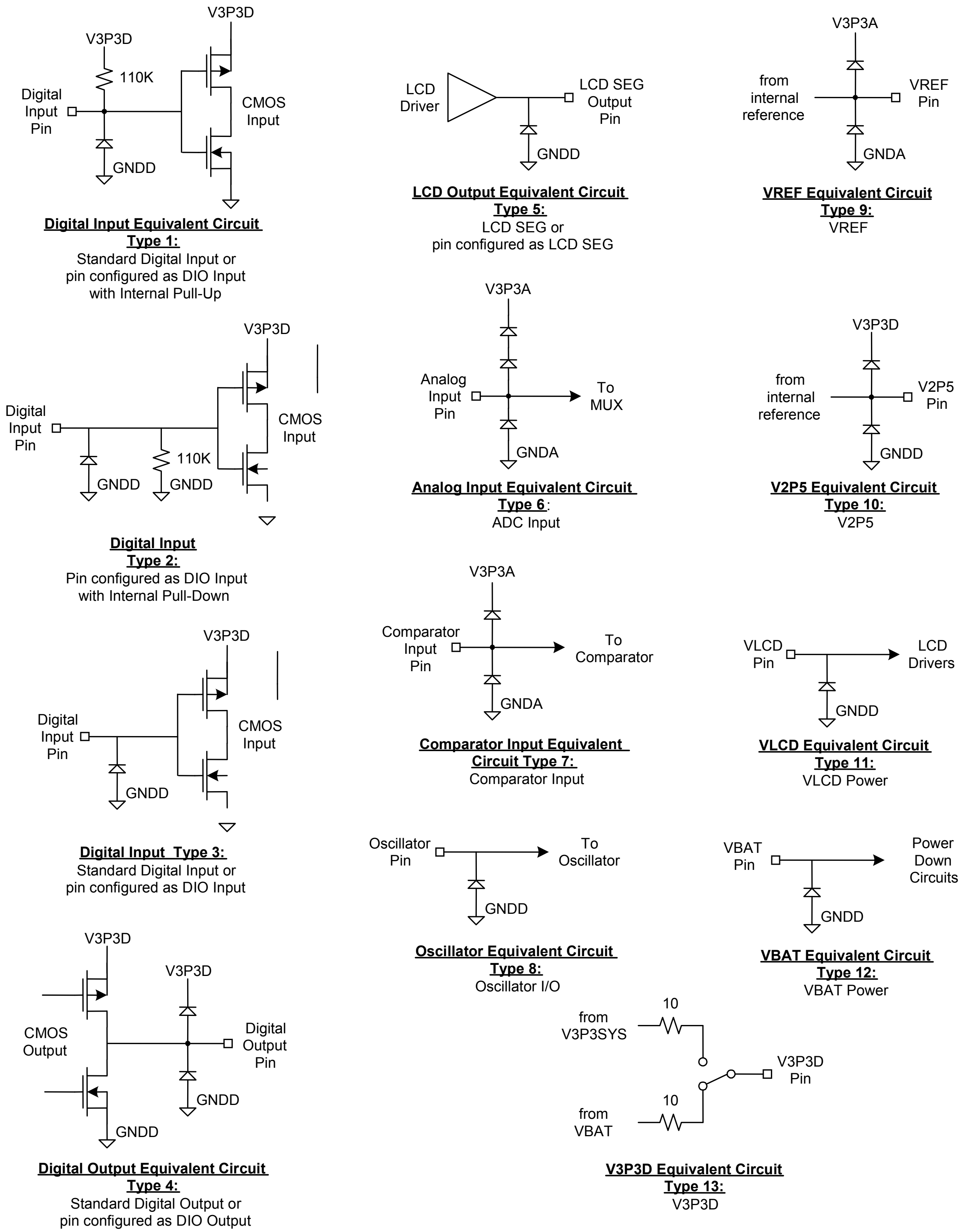


Figure 43: I/O Equivalent Circuits

7 Ordering Information

7.1 71M6543 Ordering Guide

Refer to the 71M6xxx data sheet for the 71M6xx3 ordering guide information.

Table 113. 71M6543 Ordering Guide

Part	Part Description (Package, TYP Accuracy)	Flash Size (KB)	Packaging	Order Number	Package Marking
71M6543F	100-pin LQFP Lead(Pb)-Free, 0.1%	64	bulk	71M6543F-IGT/F	71M6543F-IGT
71M6543F	100-pin LQFP Lead(Pb)-Free, 0.1%	64	tape and reel	71M6543F-IGTR/F	71M6543F-IGT
71M6543G	100-pin LQFP Lead(Pb)-Free, 0.1%	128	bulk	71M6543G-IGT/F	71M6543G-IGT
71M6543G	100-pin LQFP Lead(Pb)-Free, 0.1%	128	tape and reel	71M6543G-IGTR/F	71M6543G-IGT

8 Related Information

The following documents related to the 71M6543 and 71M6xx3 are available:

- *71M6543F/71M6543G Data Sheet* (this document)
- *71M6xxx Data Sheet*
- *71M654x Software User's Guide (SUG)*
- *71M6543 Demo Board User's Manual (DBUM)*

9 Contact Information

For technical support or more information about Maxim products, contact technical support at **www.maximintegrated.com/support**.

Appendix A: Acronyms

AFE	Analog Front-End
AMR	Automatic Meter Reading
ANSI	American National Standards Institute
CE	Compute Engine
DIO	Digital I /O
DSP	Digital Signal Processor
FIR	Finite Impulse Response
I^2C	Inter-IC Bus
ICE	In-Circuit Emulator
IEC	International Electrotechnical Commission
MPU	Microprocessor Unit (CPU)
PLL	Phase-Locked Loop
RMS	Root Mean Square
SFR	Special Function Register
SoC	System-on-Chip
SPI	Serial Peripheral Interface
TOU	Time of Use
UART	Universal Asynchronous Receiver/Transmitter

Appendix B: Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
1.0	1/11	Initial release	—
1.1	3/11	Added the 71M6543G, 71M6543GH	All
1.2	4/11	Removed the 17mW typ consumption at 3.3V for sleep mode from the *Features* section	1
2	10/13	Removed the 71M6543H, 71M6543GH; updated PLS_INV description on Table 70, added warning note on SPI Flash Mode section, updated IEN0 Bit Function and External MPU Interrupts table, removed INFO_PG from the register map, changed CECONFIG bit 23 to reserved, corrected SPI Slave port diagram (Figure 23), updated the text description of the Signal Input Pins section, combined columns 3 and 4 of Table 33, updated the Interrupt Structure diagram, corrected the OPT_TXE active definition, updated the required CE code and settings notes about MUX_DIV[3:0], added a note about V_ANG_CNT under Table 82	All

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