73S8014R
Smart Card Interface

Simplifying System Integration™

DATA SHEET

September 2008

ISO/IEC 7816-3

EMVCo

DESCRIPTION

The Teridian 73S8014R is a single smart card (ICC) interface circuit, firmware compatible with 8024-type devices for configurations where only asynchronous cards must be supported. It is derived from the 73S8024RN industry-standard electrical interface. The 73S8014R has been optimized to match most of the typical Set-Top-Box / A/V Conditional Access applications. Optimization essentially involved a smaller pin-count, support for single I/O, and maximum card current of 65mA (ISO-7816 / EMV compliance).

The 73S8014R interfaces with the host processor through the same bus (digital I/Os) as the 73S8024RN, which is compatible with any other 8024-type IC. **As a result, the 73S8014R is a very attractive cost-reduction path from traditional 8024 ICs.** The 73S8014R has been designed to provide full electrical compliance with ISO 7816-3 and EMV 4.0 specifications.

Interfacing with the system controller is done through a control bus, composed of digital inputs to control the interface, and one interrupt output to inform the system controller of the card presence and faults.

The card clock can be generated by an on-chip oscillator using an external crystal or by connection to an externally supplied clock signal.

The 73S8014R incorporates an ISO 7816-3 activation/deactivation sequencer that controls the card signals. Level-shifters drive the card signals with the selected card voltage (3V or 5V), coming from an internal Low Drop-Out (LDO) voltage regulator. This LDO regulator is powered by a dedicated power supply input V_{PC}. Digital circuitry is powered separately by a digital power supply V_{DD}. With its embedded LDO regulator, the 73S8024RN is a cost-effective solution for any application where a 5V (typically -5% +10%) power supply is available.

Emergency card deactivation is initiated upon card extraction or upon any fault detected by the protection circuitry. The fault can be a card over-current, VCC undervoltage or power supply fault (V_{DD}). The card over-current circuitry is a true current detection function, as opposed to V_{CC} voltage drop detection, as usually implemented in non-Teridian 8024 interface ICs.

The V_{DD} voltage fault has a threshold voltage that can be adjusted with an external resistor network. It allows automated card deactivation at a customized V_{DD} voltage threshold value. It can be used, for instance, to match the system controller operating voltage range.

APPLICATIONS

- **Set-Top-Box Conditional Access and Pay-per-View**
- **General purpose smart card readers**

ADVANTAGES

- **Same advantages as the Teridian 73S80xxR family:**
  - VCC card generated by an LDO regulator
  - Very low power dissipation (saves up to 1/2W)
  - Fewer external components are required
  - Better noise performance
- **True card over-current detection**
- **Firmware compatibility with all 8024 ICs**
- **Small format 20SO package**

FEATURES

- **Card Interface:**
  - Complies with ISO 7816-3 and EMV 4.0
  - Supports 3V / 5V cards
  - ISO 7816-3 Activation / Deactivation sequencer
  - Automated deactivation upon hardware fault (i.e. upon drop on V_{DD} power supply or card overcurrent)
  - The V_{DD} voltage supervisor threshold value (fault) can be externally adjusted
  - Over-current detection 130mA max
  - Card CLK clock frequency up to 20MHz
- **System Controller Interface:**
  - 3 Digital inputs control the card activation / deactivation, card reset and card voltage
  - 2 Digital inputs control the card clock frequency
  - 1 Digital output, interrupt to the system controller, reports to the host the card presence and faults
  - Crystal oscillator or host clock, up to 27MHz
- **Regulator Power Supply:**
  - 4.75V to 5.5V
- **Digital Interfacing: 2.7V to 5.5V**
- **6kV ESD protection on the card interface**
- **Package: SO 20-pin**
- **RoHS compliant (6/6) lead-free package**

FUNCTIONAL DIAGRAM

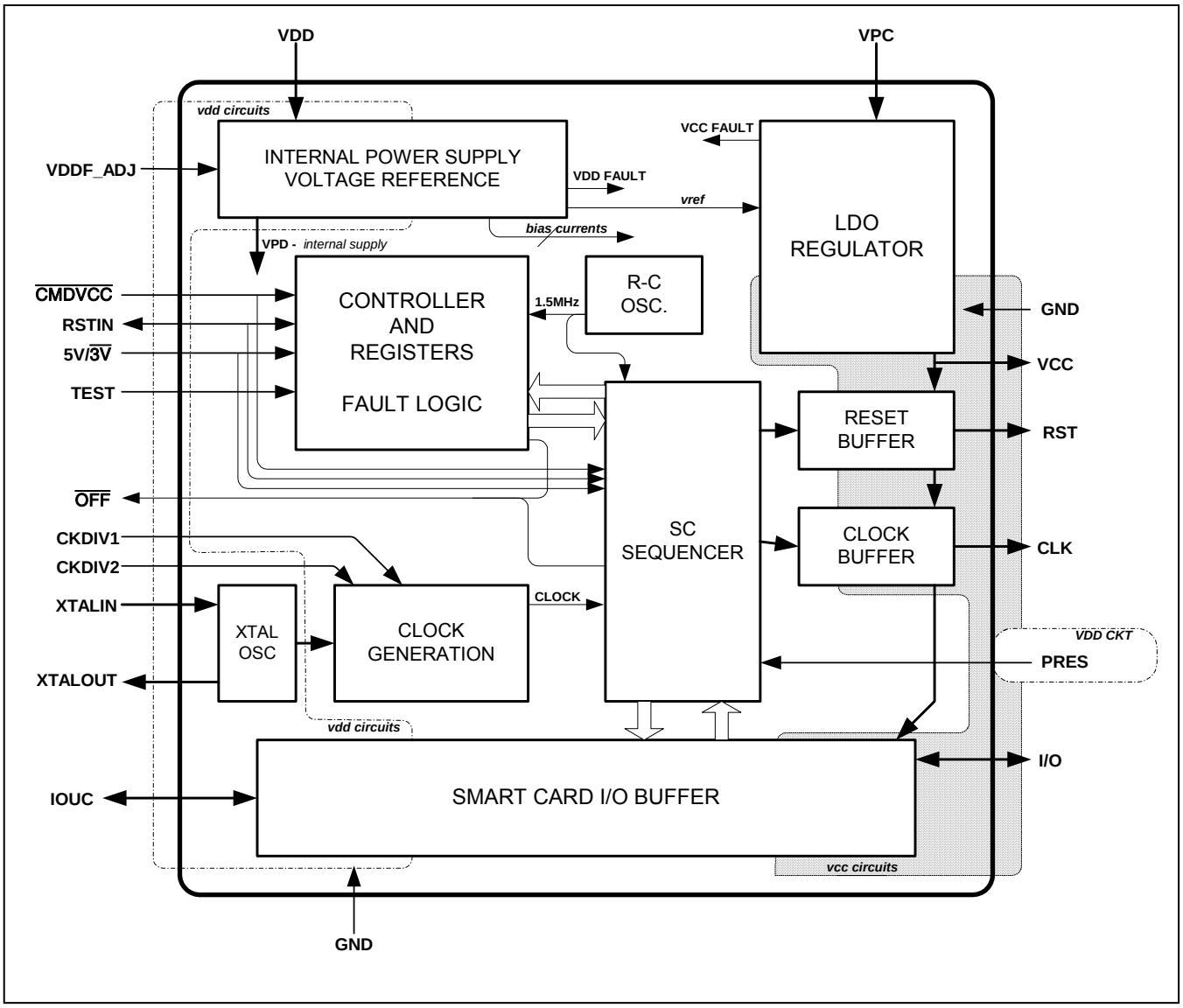

Figure 1: 73S8014R Block Diagram

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1 Pinout

The 73S8014R is supplied as a 20-pin SO package.

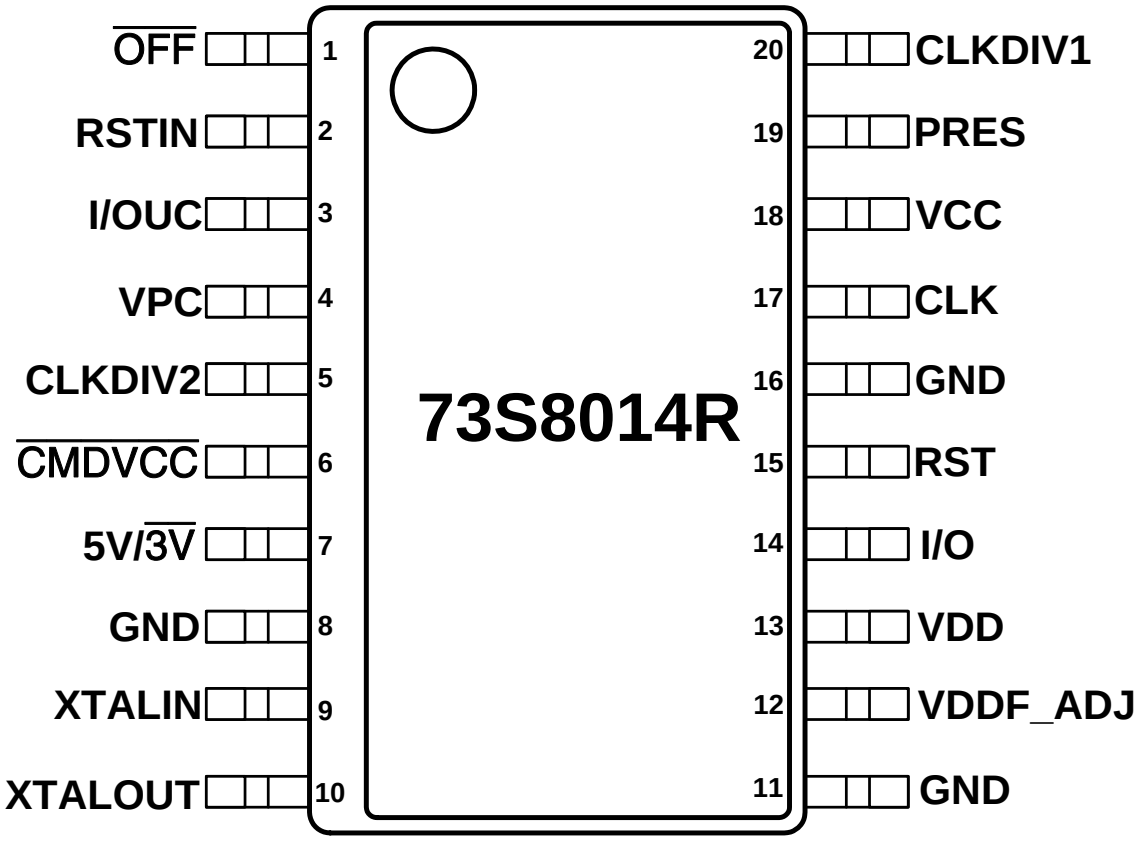


Figure 2: 73S8014R 20-SOP Pin Out

Table 1 provides the 73S8014R pin names, pin numbers, type, equivalent circuits and descriptions.

Table 1: 73S8014R 20-Pin SOP Pin Definitions

Pin Name	Pin Number	Type	Equivalent Circuit	Description
Card Interface				
I/O	14	IO	Figure 14	Card I/O: Data signal to/from card. Includes an 11k pull-up resistor to $V_{CC.}$
RST	15	O	Figure 13	Card reset: provides reset (RST) signal to card.
CLK	17	O	Figure 12	Card clock: provides clock signal (CLK) to card. The rate of this clock is determined by the external crystal frequency or frequency of the external clock signal applied on XTALIN and CLKDIV selections.
PRES	19	I	Figure 16	Card Presence switch: active high indicates card is present. Includes a high-impedance pull-down current source.
VCC	18	PSO	Figure 11	Card power supply – logically controlled by sequencer, output of LDO regulator. Requires an external filter capacitor to the card GND.
GND	16	GND	–	Card ground.
Host Processor Interface				
$\overline{\text{CMDVCC}}$	6	I	Figure 16	Command VCC (negative assertion): Logic low on this pin causes the LDO regulator to ramp the V_{CC} supply to the card and initiates a card activation sequence, if a card is present.
5V/$\overline{\text{3V}}$	7	I	Figure 16	5 volt / 3 volt card selection: Logic one selects 5 volts for V_{CC} and card interface, logic low selects 3 volt operation. When the part is to be used with a single card voltage, this pin should be tied to either GND or V_{DD}. However, it includes a high impedance pull-up resistor to default this pin high (selection of 5V card) when not connected. This pin shall not be changed when CMDVCC is low.
CLKDIV1 CLKDIV2	20 5	I	Figure 16	Sets the divide ratio from the XTAL oscillator (or external clock input) to the card clock. These pins include a pull-up resistor for CLKDIV1 and CLKLDIV2 to provide a default rate of divide by two. CLKDIV1 CLKDIV2 CLOCK RATE 0 0 XTALIN/8 0 1 XTALIN/4 1 1 XTALIN/2 1 0 XTALIN
$\overline{\text{OFF}}$	1	O	Figure 10	Interrupt signal to the processor. Active Low - Multi-function indicating fault conditions and card presence. Open drain output configuration – It includes an internal 20kΩ pull-up to $V_{DD.}$
RSTIN	2	I	Figure 16	Reset Input: This signal is the reset command to the card.
I/OUC	3	IO	Figure 15	System controller data I/O to/from the card. Includes an 11K pull-up resistor to $V_{DD.}$

Miscellaneous Inputs and Outputs				
XTALIN	9		Figure 17	Crystal oscillator input: can either be connected to crystal or driven as a source for the card clock. Note: When not using the crystal, the capacitors must be removed.
XTALOUT	10		Figure 17	Crystal oscillator output: connected to crystal. Left open if XTALIN is being used as external clock input. Note: When not using the crystal, the capacitors must be removed.
VDDF_ADJ	12		Figure 18	V_{DD} fault threshold adjustment input: this pin can be used to adjust the V_{DDF} value (that controls deactivation of the card). Must be left open if unused.
Power Supply and Ground				
VDD	13	PSO	Figure 11	System interface supply voltage and supply voltage for internal circuitry.
VPC	4	PSO	Figure 11	LDO regulator power supply source.
GND	8, 11	GND	–	Digital ground.

2 Electrical Specifications

This section provides the following:

- Absolute maximum ratings
- Recommended operating conditions
- Package thermal parameters
- Smart card interface requirements
- Digital signals characteristics
- DC Characteristics
- Voltage Fault Detection Circuits

2.1 Absolute Maximum Ratings

Table 2 lists the maximum operating conditions for the 73S8014R. Permanent device damage may occur if absolute maximum ratings are exceeded. Exposure to the extremes of the absolute maximum rating for extended periods may affect device reliability. The smart card interface pins are protected against short circuits to V_{CC}, ground, and each other.

Table 2: Absolute Maximum Device Ratings

Parameter	Rating
Supply Voltage V_{DD}	-0.5 to 6.0 VDC
Supply Voltage V_{PC}	-0.5 to 6.0 VDC
Input Voltage for Digital Inputs	-0.3 to (V_{DD} +0.5) VDC
Storage Temperature	-60 to 150°C
Pin Voltage (except card interface)	-0.3 to (V_{DD} +0.5) VDC
Pin Voltage (card interface)	-0.3 to (V_{CC} + 0.5) VDC
ESD Tolerance – Card interface pins	+/- 6kV
ESD Tolerance – Other pins	+/- 2kV

*Note: ESD testing on smart card pins is HBM condition, 3 pulses, each polarity referenced to ground.
Note: Smart Card pins are protected against shorts between any combinations of Smart Card pins.

2.2 Recommended Operating Conditions

Function operation should be restricted to the recommended operating conditions specified in Table 3.

Table 3: Recommended Operating Conditions

Parameter	Rating
Supply Voltage V_{DD}	2.7 to 5.5 VDC
Supply Voltage V_{PC}	4.75 to 5.5 VDC
Ambient Operating Temperature	-40°C to +85°C
Input Voltage for Digital Inputs	0V to V_{DD} + 0.3V

2.3 Package Thermal Parameters

Table 4 lists the 73S8014R Smart Card interface requirements.

Table 4: Package Thermal Parameters

Parameter	Rating
20 SO	50 °C / W

2.4 Smart Card Interface Requirements

Table 5 lists the 73S8014R Smart Card interface requirements.

Table 5: DC Smart Card Interface Requirements

Symbol	Parameter	Condition	Min	Nom	Max	Unit
Card Power Supply (V_{CC}) Regulator ***General conditions, -40°C < T < 85°C, 4.75V < V_{PC} < 5.5V, 2.7V < V_{DD} < 5.5V***						
V_{CC}	Card supply voltage including ripple and noise	Inactive mode	-0.1		0.1	V
		Inactive mode, I_{CC} = 1mA	-0.1		0.4	V
		Active mode; I_{CC} <65mA; 5V	4.65		5.25	V
		Active mode; I_{CC} <65mA; 3V	2.85		3.15	V
		Active mode; I_{CC} <40mA; 1.8V	1.68		1.92	V
		Active mode; single pulse of 100mA for 2μs; 5 volt, fixed load = 25mA	4.6		5.25	V
		Active mode; single pulse of 100mA for 2μs; 3v, fixed load = 25mA	2.76		3.2	V
		Active mode; current pulses of 40nAs with peak $\|I_{CC}\|$ <200mA, t <400ns; 5V	4.6		5.25	V
		Active mode; current pulses of 40nAs with peak $\|I_{CC}\|$ <200mA, t <400ns; 3V	2.7		3.15	V
V_{CCrip}	V_{CC} Ripple	f_{RIPPLE} = 20K – 200MHz			350	mV
I_{CCmax}	Card supply output current	Static load current, V_{CC}>4.6V or 2.7V as selected	65			mA
I_{CCF}	I_{CC} fault current		70		130	mA
V_{SR}	V_{CC} slew rate, rise	C_F = 1.0μF on V_{CC}	0.06	0.150	0.30	V/μs
V_{SF}	V_{CC} slew rate, fall	C_F = 1.0μF on V_{CC}	0.075	0.150	0.60	V/μs
C_F	External filter cap (V_{CC} to GND)	C_F should be ceramic with low ESR (<100mΩ).	0.5	1.0	1.5	μF

Symbol	Parameter	Condition	Min	Nom	Max	Unit
Interface Requirements – Data Signals: I/Oand host interfaces: I/OUC. I_{SHORTL}, I_{SHORTH}, and V_{INACT} requirements do not pertain to I/OUC.						
V_{OH}	Output level, high (I/O)	I_{OH} =0	0.9 V_{CC}		V_{CC}+0.1	V
		I_{OH} = -40µA	0.75 V_{CC}		V_{CC}+0.1	V
	Output level, high (I/OUC)	I_{OH} =0	0.9 V_{DD}		V_{DD}+0.1	V
		I_{OH} = -40µA	0.75 V_{DD}		V_{DD}+0.1	V
V_{OL}	Output level, low (I/O)				0.15 V_{CC}	V
	Output level, low (I/OUC)	I_{OL}=1mA			0.3	V
V_{IH}	Input level, high (I/O)		0.6 V_{CC}		V_{CC}+0.30	V
	Input level, high (I/OUC)		1.8		V_{DD} + 0.3	V
V_{IL}	Input level, low (I/O)		-0.15		0.2 V_{CC}	V
	Input level, low (I/OUC)		-0.3		0.8	V
V_{INACT}	Output voltage when outside of session	I_{OL} = 0			0.1	V
		I_{OL} = 1mA			0.3	V
I_{LEAK}	Input leakage	V_{IH} = V_{CC}			10	µA
I_{IL}	Input current, low	V_{IL} = 0			0.65	mA
I_{SHORTL}	Short circuit output current	For output low, shorted to V_{CC} through 33 Ω			15	mA
I_{SHORTH}	Short circuit output current	For output high, shorted to ground through 33 Ω			15	mA
t_R, t_F	Output rise time, fall times	C_L = 80pF, 10% to 90%.			100	ns
t_{IR}, t_{IF}	Input rise, fall times				1	µs
R_{PU}	Internal pull-up resistor	Output stable for >400ns	8	11	14	kΩ
FD_{MAX}	Maximum data rate				1	MHz
T_{FDIO}	Delay, I/O to I/OUC, I/OUC to I/O, (respectively falling edge to falling edge and rising edge to rising edge)	Edge from master to slave, measured at 50%	60	100	200	ns
T_{RDIO}				15		ns
C_{IN}	Input capacitance				10	pF

Symbol	Parameter	Condition	Min	Nom	Max	Unit
Reset and Clock for card interface, RST, CLK						
V_{OH}	Output level, high	I_{OH} =-200µA	0.9 V_{CC}		V_{CC}	V
V_{OL}	Output level, low	I_{OL}=200µA	0		0.15 V_{CC}	V
V_{INACT}	Output voltage when outside of session	I_{OL} = 0			0.1	V
		I_{OL} = 1mA			0.3	V
I_{RST_LIM}	Output current limit, RST				30	mA
I_{CLK_LIM}	Output current limit, CLK				70	mA
CLK_{SR3V}	CLK slew rate	Vcc = 3V	0.3			V/ns
CLK_{SR5V}	CLK slew rate	Vcc = 5V	0.5			V/ns
t_R, t_F	Output rise time, fall time	C_L = 35pF for CLK, 10% to 90%			8	ns
		C_L = 200pF for RST, 10% to 90%			100	ns
δ	Duty cycle for CLK	C_L =35pF, $F_{CLK} \leq$ 20MHz	45		55	%

2.5 Characteristics: Digital Signals

Table 6 lists the 73S8014R digital signals characteristics.

Table 6: Digital Signals Characteristics

Symbol	Parameter	Condition	Min	Nom	Max	Unit
Digital I/O except for XTALIN and XTALOUT						
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{IH}	Input High Voltage		1.8		V_{DD} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -1mA	V_{DD} - 0.45			V
R_{OUT}	Pull-up resistor, $\overline{OFF}$		16	20	24	kΩ
$\|I_{IL1}\|$	Input Leakage Current	GND < V_{IN} < V_{DD}	-5		5	µA

Oscillator (XTALIN) I/O Parameters						
V_{ILXTAL}	Input Low Voltage - XTALIN		-0.3		0.3 V_{DD}	V
V_{IHXTAL}	Input High Voltage - XTALIN		0.7 V_{DD}		V_{DD}+0.3	V
I_{ILXTAL}	Input Current - XTALIN	GND < V_{IN} < V_{DD}	-30		30	µA
f_{MAX}	Max freq. Osc or external clock				27	MHz
δin	External input duty cycle limit	$t_{R/F}$ < 10% f_{IN}, 45% < δ_{CLK} < 55%	48		52	%

2.6 DC Characteristics

Table 7 lists the 73S8014R DC characteristics.

Table 7: DC Characteristics

Symbol	Parameter	Condition	Min	Nom	Max	Unit
I_{DD}		12 MHz XTAL		2.7	7.0	mA
		Ext CLK, VDD = 2.7 – 3.6V, VCC Off		1.7		mA
	Supply Current	Ext CLK, VDD = 2.7 – 3.6V, VCC On		2.2		mA
		Ext CLK, VDD = 4.5 – 5.5V, VCC Off		2.7		mA
		Ext CLK, VDD = 4.5 – 5.5V, VCC On		3		mA
I_{PC}	Supply Current	V_{CC} on, ICC=0 I/O, AUX1, AUX2=high, Clock not toggling		450	700	µA
I_{PCOFF}	V_{PC} supply current when V_{CC} = 0	$\overline{CMDVCC}$ High		345	650	µA

2.7 Voltage Fault Detection Circuits

Table 8 lists the 73S8014R Voltage Fault Detection Circuits.

Table 8: Voltage Fault Detection Circuits

Symbol	Parameter	Condition	Min	Nom	Max	Unit
V_{DDF}	V_{DD} fault (V_{DD} Voltage supervisor threshold)	No external resistor on VDDF_ADJ pin	2.15		2.4	V
V_{CCF}	V_{CC} fault (V_{CC} Voltage supervisor threshold)	V_{CC} = 5v			4.6	V
		V_{CC}= 3v			2.7	V

3 Applications Information

This section provides general usage information for the design and implementation of the 73S8014R. The documents listed in Related Documentation provide more detailed information.

3.1 Example 73S8014R Schematics

Figure 3 shows a typical application schematic for the implementation of the 73S8014R. Note that minor changes may occur to the reference material from time to time and the reader is encouraged to contact Teridian for the latest information.

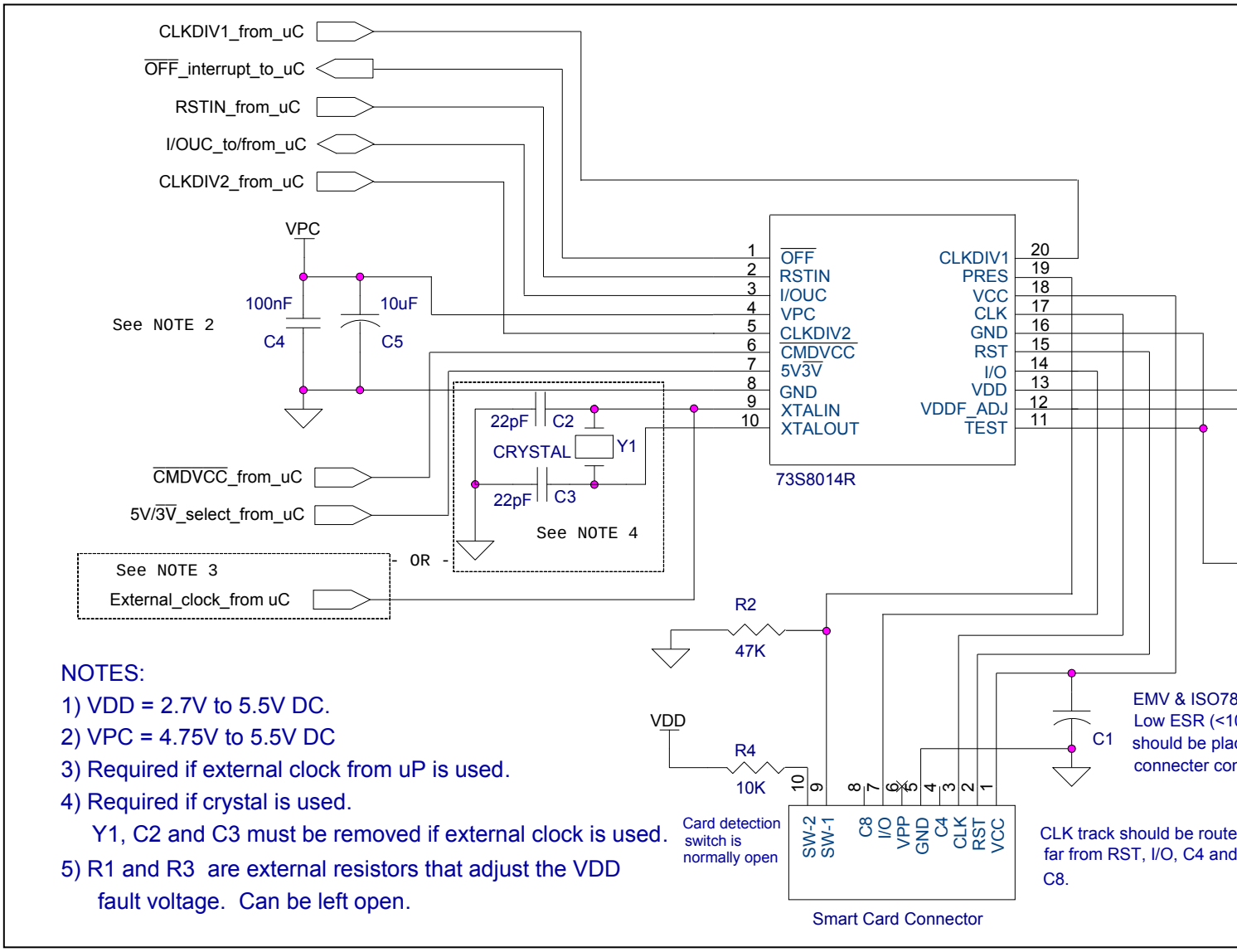


Figure 3: 73S8014R – Typical Application Schematic

3.2 System Controller Interface

Three digital inputs allow direct control of the card interface by the host. The 73S8014R is controlled as follows:

- Pin $\overline{\text{CMDVCC}}$: When asserted low, starts an activation sequence
- Pin RSTIN: controls the card RST signal (when enabled by the sequencer)
- Pin 5V/$\overline{\text{3V}}$: Defines the card VCC voltage (5V when high and 3V when low)

Card clock frequency can be controlled by 2 digital inputs:

- CLKDIV1 and CLKDIV2 define the division rate for the clock frequency, from the input clock frequency (crystal or external clock)

Note: The maximum CLK frequency is 20MHz. Therefore, if using an input clock source greater than 20MHz, a divisor rate of 2X or higher must be used.

Interrupt output to the host: As long as the card is not activated, the $\overline{\text{OFF}}$ pin informs the host about the card presence only (Low = No card in the reader). When $\overline{\text{CMDVCC}}$ is asserted low (Card activation sequence requested from the host), low level on $\overline{\text{OFF}}$ means a fault has been detected (e.g. card removal during card session, voltage fault, or over-current fault) that automatically initiates a deactivation sequence.

3.3 Power Supply and Voltage Supervision

The 73S8014R smart card interface IC incorporates a LDO voltage regulator. The voltage output is controlled by the digital input 5V/$\overline{\text{3V}}$ of the 73S8014R. This regulator is able to provide either 3V or 5V card voltage from the power supply applied on the VPC pin. The voltage regulator can provide a current of at least 65mA on VCC for both 3V and 5V that complies with EMV 4.0.

Digital circuitry is powered by the power supply applied on the VDD pin. VDD also defines the voltage range to interface with the system controller. A card deactivation sequence is forced upon fault of any of this voltage supervisor. One voltage supervisor constantly monitors the VDD voltage. It is used to initialize the ISO 7816-3 sequencer at power-on, and to deactivate the card at power-off or upon fault. The voltage threshold of the VDD voltage supervisor is internally set by default to 2.33V nominal. However, it may be desirable, in some applications, to modify this threshold value. The pin VDDF_ADJ is used to connect an external resistor R_{EXT} to ground to change the VDD fault voltage to another value, V_{DDF}. The resistor value is defined as follows:

$R_{EXT} = 56k\Omega / (V_{DDF} - 2.33)$

An alternative (more accurate) method of adjusting the VDD fault voltage is to use a resistive network of R3 from the pin to supply and R1 from the pin to ground (see Figure 3). In order to set the new threshold voltage, the equivalent resistance must be determined. This resistance value will be designated Kx. Kx is defined as R1/(R1+R3). Kx is calculated as:

$Kx = (2.789 / V_{TH}) - 0.6125$ where V_{TH} is the desired new threshold voltage.

To determine the values of R1 and R3, use the following formulas.

$R3 = 24000 / Kx$ $\quad R1 = R3*(Kx / (1 – Kx))$

Taking the example above, where a V_{DD} fault threshold voltage of 2.7V is desired, solving for Kx gives:
→ Kx = (2.789 / 2.7) - 0.6125 = 0.42046.
Solving for R3 gives: → R3 = 24000 / 0.42046 = 57080.
Solving for R1 gives: → R1 = 57080 *(0.42046 / (1 – 0.42046)) = 41412.
Using standard 1 % resistor values gives R3 = 57.6KΩ and R1 = 42.4KΩ.
These values give an equivalent resistance of Kx = 0.4228, a 0.6% error.

If the 2.33V default threshold is used, this pin must be left unconnected.

3.4 Card Power Supply

The card power supply is internally provided by the LDO regulator, and controlled by the digital ISO 7816-3 sequencer. Card voltage selection on the 73S8014R is carried out by the digital input 5V/$\overline{3V}$.

Choice of the VCC capacitor:

Depending on the application, the requirements in terms of both VCC minimum voltage and transient currents that the interface must be able to provide to the card are different. An external capacitor must be connected between the VCC pin and to the card ground in order to guarantee stability of the LDO regulator, and to handle the transient requirements. The type of capacitor should be an X5R/X7R with ERS<100 mΩ.

3.5 On-Chip Oscillator and Card Clock

The 73S8014R device has an on-chip oscillator that can generate the smart card clock using an external crystal (connected between the pins XTALIN and XTALOUT) to set the oscillator frequency. When the clock signal is available from another source, it can be connected to the pin XTALIN, and the pin XTALOUT should be left unconnected.

The card clock frequency may be chosen between 4 different division rates, defined by digital inputs CLKDIV 1 and CLKDIV 2, as per the following table:

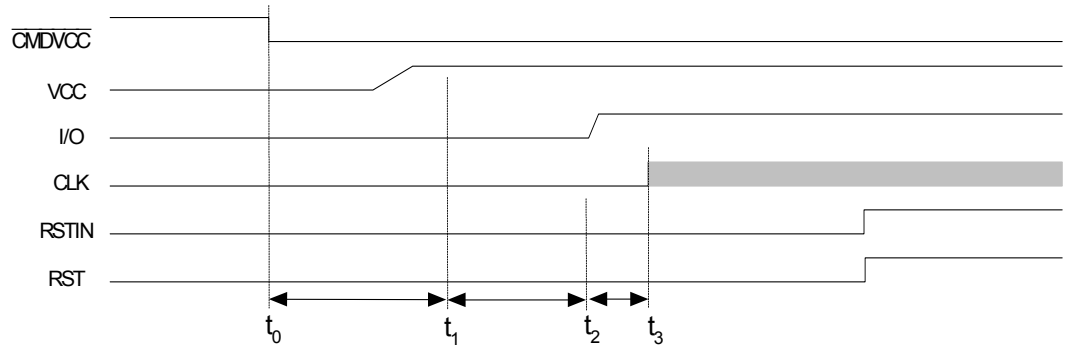
CLKDIV1	CLKDIV2	CLK	Max XTALIN
0	0	1/8 XTALIN	27MHz
0	1	¼ XTALIN	27MHz
1	0	XTALIN	20MHz
1	1	½ XTALIN	27MHz

3.6 Activation Sequence

The 73S8014R smart card interface ICs have an internal 10ms delay on the application of VDD where VDD > V_{DDF}. No activation is allowed during this 10ms period. The $\overline{CMDVCC}$ (edge triggered) signal must then be set low to activate the card. In order to initiate activation, the card must be present; there can be no VDD fault.

The following steps show the activation sequence and the timing of the card control signals when the system controller sets $\overline{CMDVCC}$ low while the RSTIN is low:

- $\overline{CMDVCC}$ is set low at t_0.
- VCC will rise to the selected level and then the internal VCC control circuit checks the presence of VCC at the end of t_1. In normal operation, the voltage VCC to the card becomes valid before t_1. If VCC is not valid at t_1, the $\overline{OFF}$ goes low to report a fault to the system controller, and VCC to the card is shut off.
- Turn I/O to reception mode at t_2.
- CLK is applied to the card at t_3.
- RST is a copy of RSTIN after t_3.

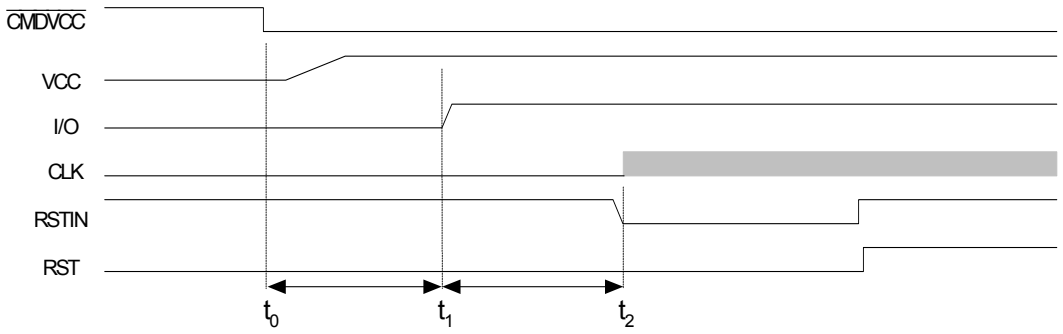


t_1 = 0.510 ms (timing by 1.5MHz internal Oscillator)
t_2 = 1.5μs, I/O goes to reception state
t_3 = >0.5μs, CLK starts, RST to become the copy of RSTIN

Figure 4: Activation Sequence – RSTIN Low When $\overline{CMDVCC}$ Goes Low

The following steps show the activation sequence and the timing of the card control signals when the system controller pulls the $\overline{CMDVCC}$ low while the RSTIN is high:

- $\overline{CMDVCC}$ is set low at t_0.
- VCC will rise to the selected level and then the internal VCC control circuit checks the presence of VCC at the end of t_1. In normal operation, the voltage VCC to the card becomes valid before t_1. If VCC is not valid at t_1, the $\overline{OFF}$ goes low to report a fault to the system controller, and VCC to the card is shut off.
- At the fall of RSTIN at t_2, CLK is applied to the card
- RST is a copy of RSTIN after t_2.



t_1 = 0.510 ms (timing by 1.5MHz internal oscillator, I/O goes to reception state)
t_2 = RSTIN goes low and CLK becomes active
t_3 = > 0.5µs, CLK active, RST to become the copy of RSTIN

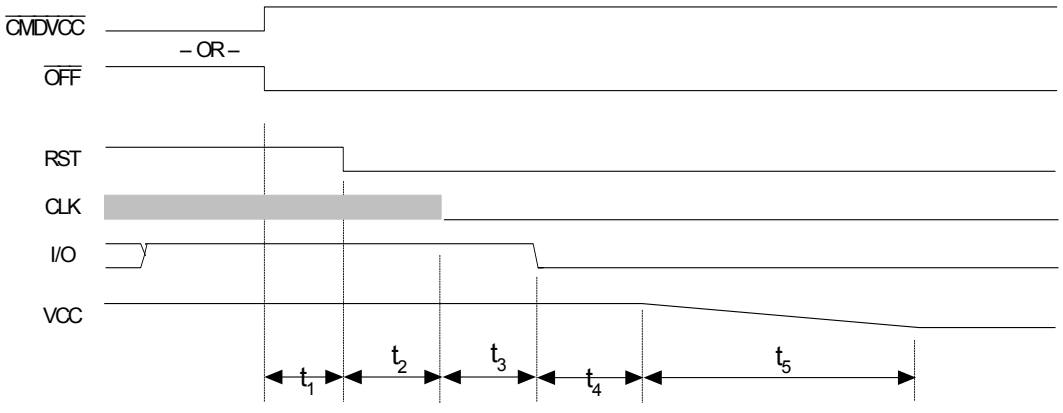
Figure 5: Activation Sequence – RSTIN High When $\overline{\text{CMDVCC}}$ Goes Low

3.7 Deactivation Sequence

Deactivation is initiated either by the system controller by setting the $\overline{\text{CMDVCC}}$ high, or automatically in the event of hardware faults. Hardware faults are over-current, VDD fault, VCC fault, and card extraction during the session.

The following steps show the deactivation sequence and the timing of the card control signals when the system controller sets the $\overline{\text{CMDVCC}}$ high or $\overline{\text{OFF}}$ goes low due to a fault or card removal:

- RST goes low at the end of t_1.
- CLK is set low at the end of t_2.
- I/O goes low at the end of t_3. Out of reception mode.
- VCC is shut down at the end of time t_4. After a delay t_5 (discharge of the VCC capacitor), VCC is low.



t_1 = > 0.5µs, timing by 1.5MHz internal Oscillator
t_2 = > 7.5µs
t_3 = > 0.5µs
t_4 = > 0.5µs
t_5 = depends on VCC filter capacitor.

Figure 6: Deactivation Sequence

3.8 Fault Detection and OFF

There are two different cases that the system controller can monitor the $\overline{OFF}$ signal: to query regarding the card presence outside card sessions, or for fault detection during card sessions.

Outside a card session: In this condition, $\overline{CMDVCC}$ is/are always high, $\overline{OFF}$ is low if the card is not present, and high if the card is present. Because it is outside a card session, any fault detection will not act upon the $\overline{OFF}$ signal. No deactivation is required during this time.

During a card session: $\overline{CMDVCC}$ is/are always low, and $\overline{OFF}$ falls low if the card is extracted or if any fault detection is detected. At the same time that $\overline{OFF}$ is set low, the sequencer starts the deactivation process.

Figure 7 shows the timing diagram for the signals $\overline{CMDVCC}$, PRES, and $\overline{OFF}$ during a card session and outside the card session:

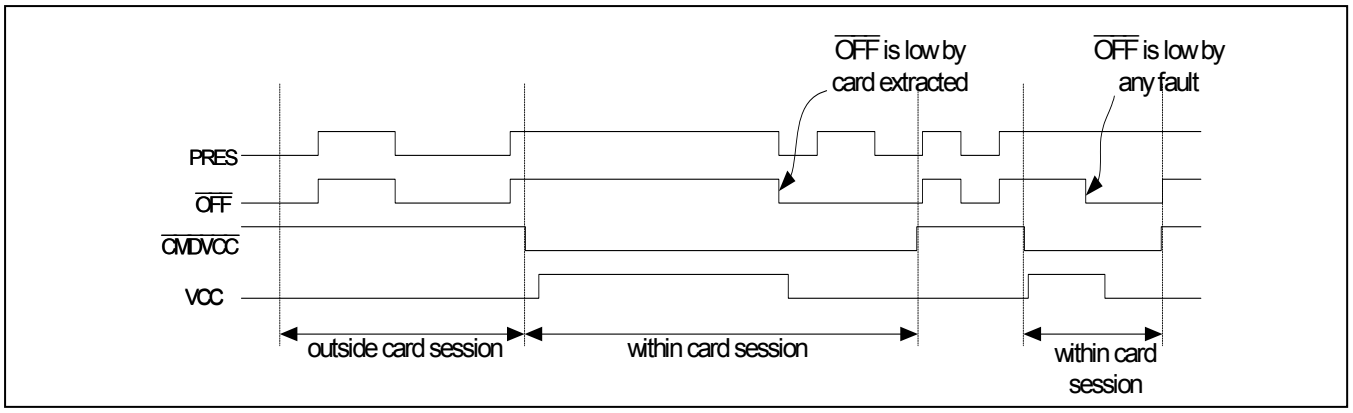


Figure 7: Timing Diagram – Management of the Interrupt Line $\overline{OFF}$

3.9 I/O Circuitry and Timing

The state of the I/O pin is low after power on reset and it goes high when the activation sequencer turns on the I/O reception state. See the Activation Sequence section for details on when the I/O reception is enabled. The state of I/OUC is high after power on reset.

Within a card session and when the I/O reception state is turned on, the first I/O line on which a falling edge is detected becomes the input I/O line and the other becomes the output I/O line. When the input I/O line rising edge is detected then both I/O lines return to their neutral state.

Figure 8 shows the state diagram of how the I/O and I/OUC lines are managed to become input or output. The delay between the I/O signals is shown in Figure 9.

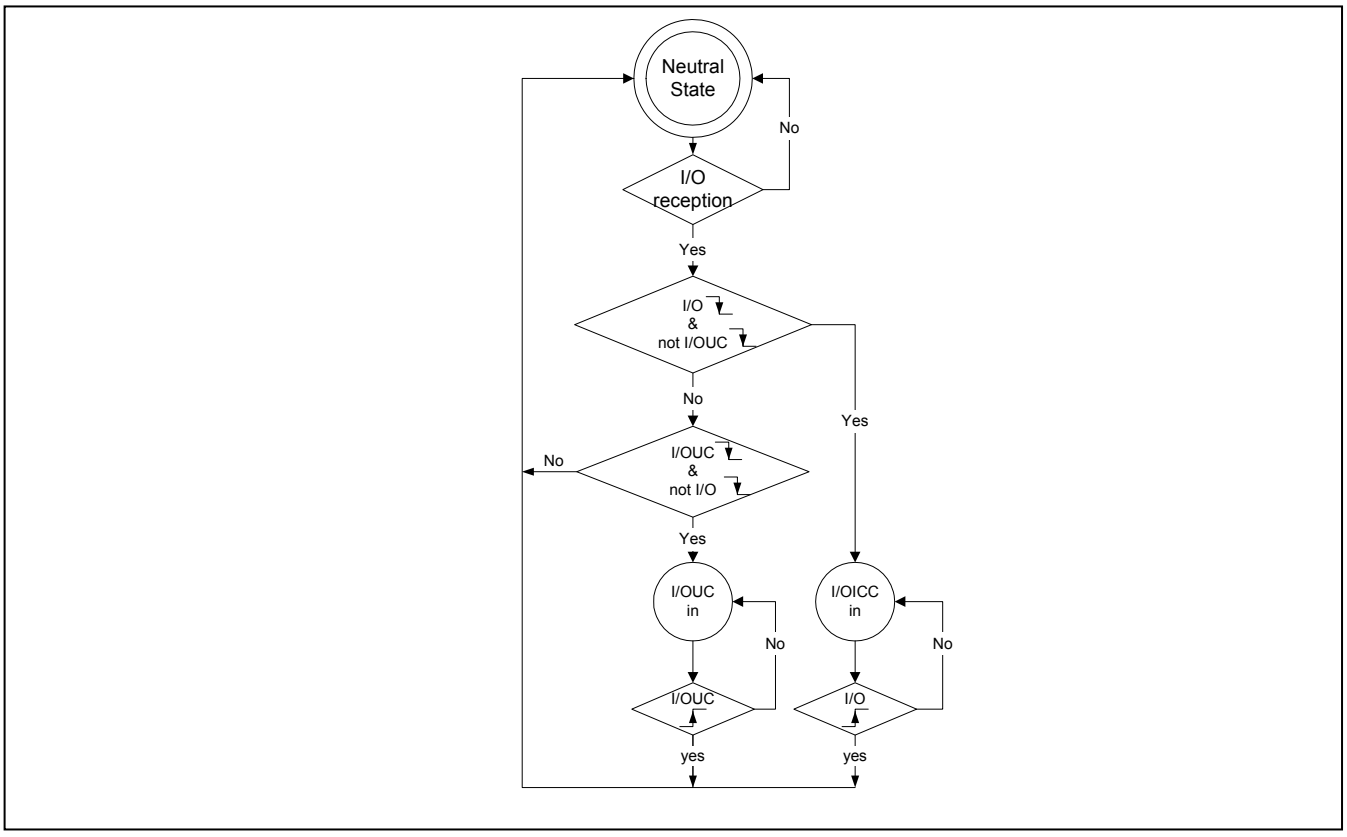


Figure 8: I/O and I/OUC State Diagram

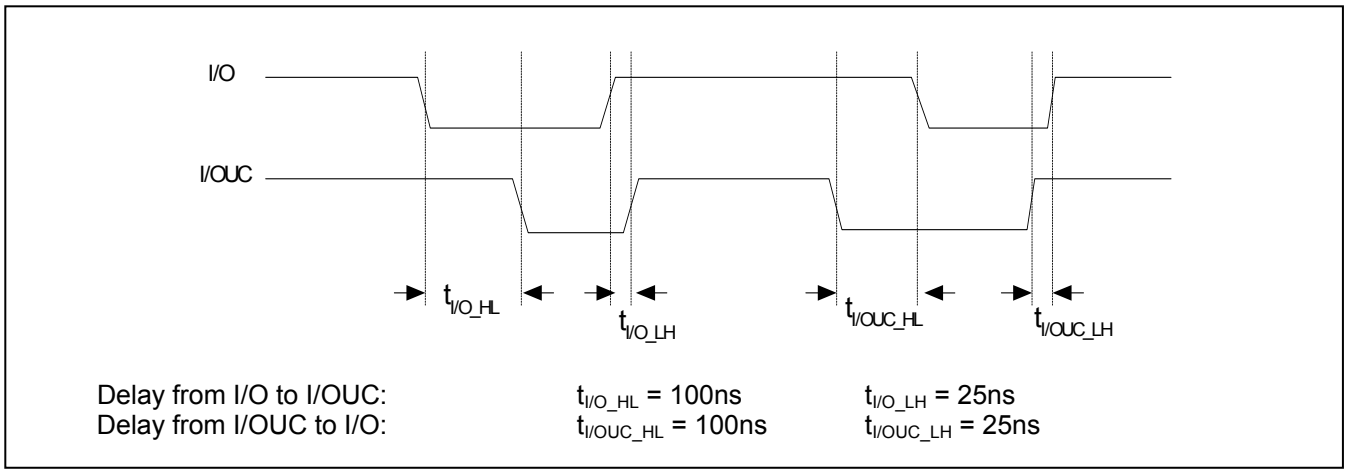


Figure 9: I/O – I/OUC Delays – Timing Diagram

4 Equivalent Circuits

This section provides illustrations of circuits equivalent to those described in the pinout section.

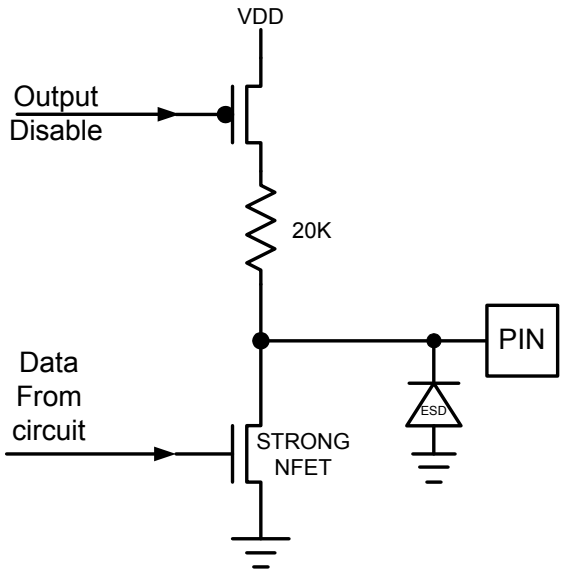


Figure 10: Open Drain type – $\overline{\text{OFF}}$

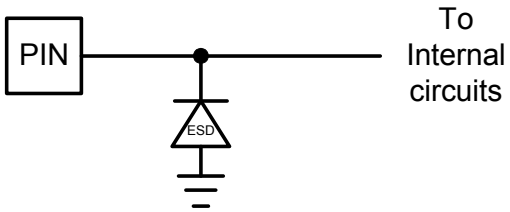


Figure 11: Power Input/Output Circuit, VDD, VPC, VCC

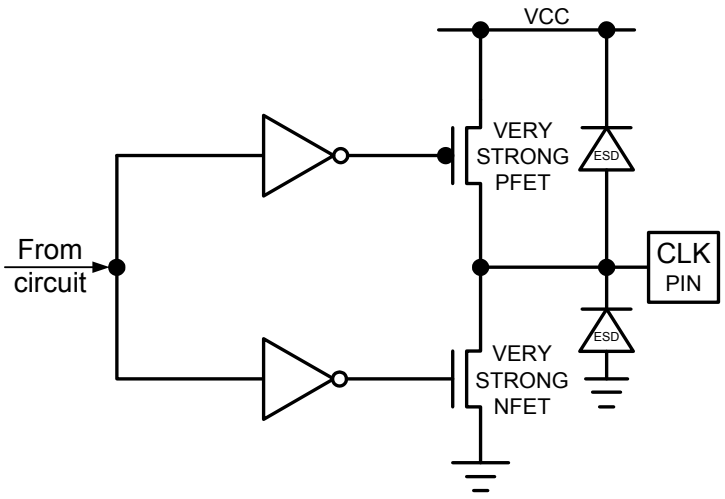


Figure 12: Smart Card CLK Driver Circuit

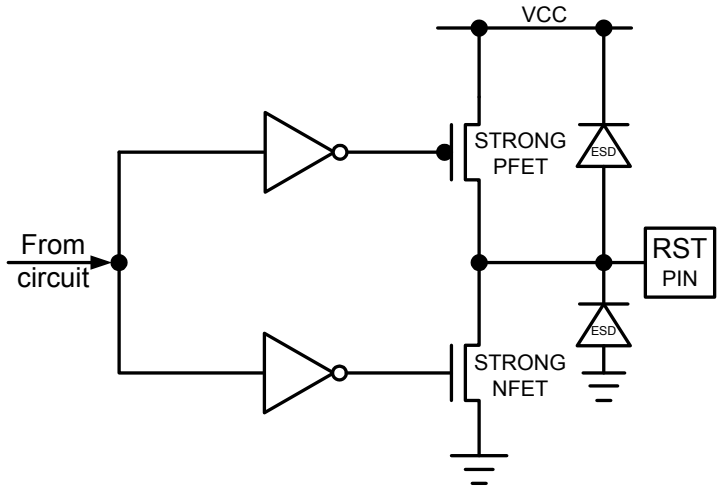


Figure 13: Smart Card RST Driver Circuit

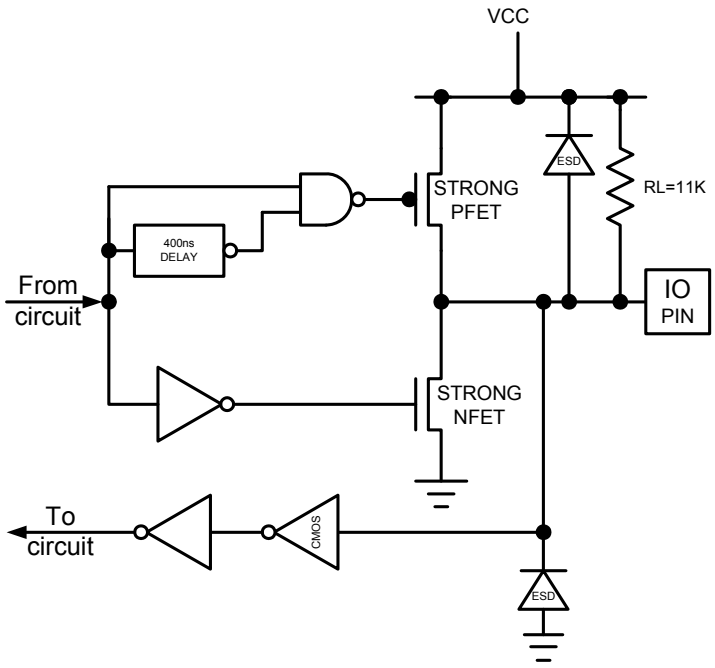


Figure 14: Smart Card IO Interface Circuit

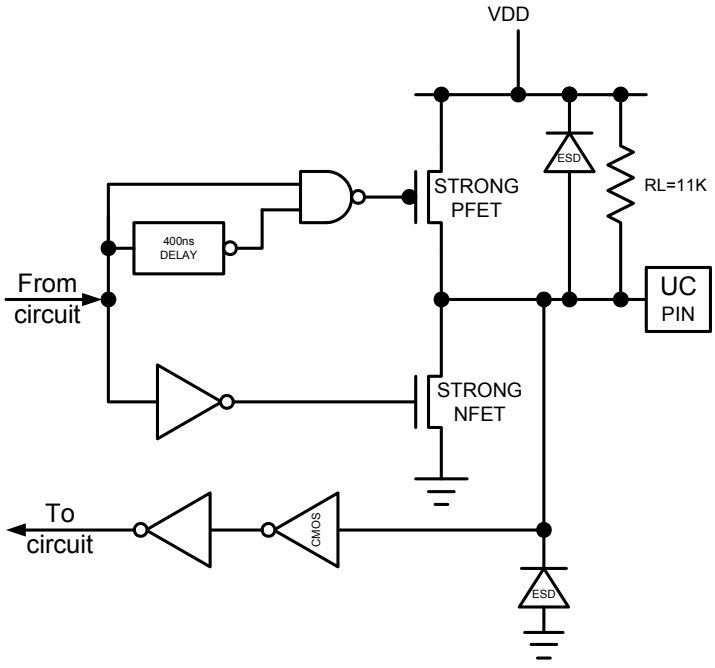
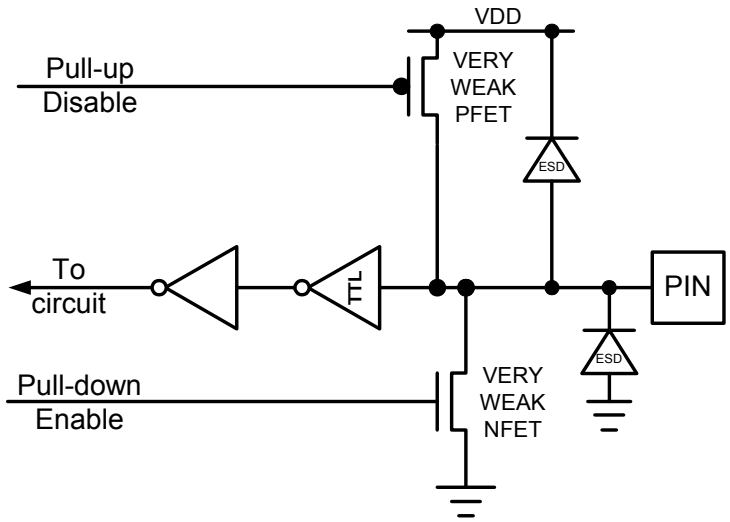


Figure 15: Smart Card IOUC Interface Circuit



Note: Pins $\overline{\text{CMDVCC}}$,5V/$\overline{\text{3V}}$, CLKDIV1 and CLKDIV2 have the pull-up enabled.
Pins RSTIN, CLKIN, PRES have the pull-down enabled.

Figure 16: General Input Circuit

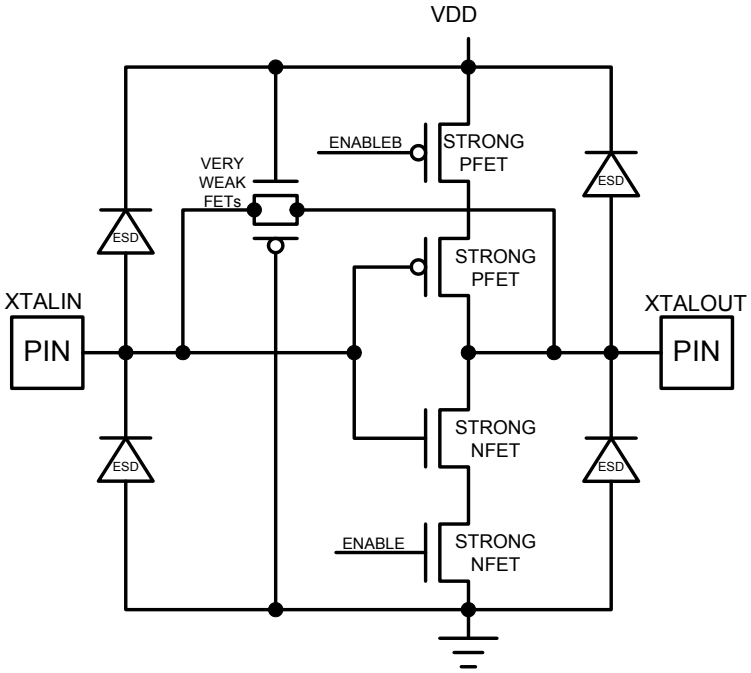


Figure 17: Oscillator Circuit

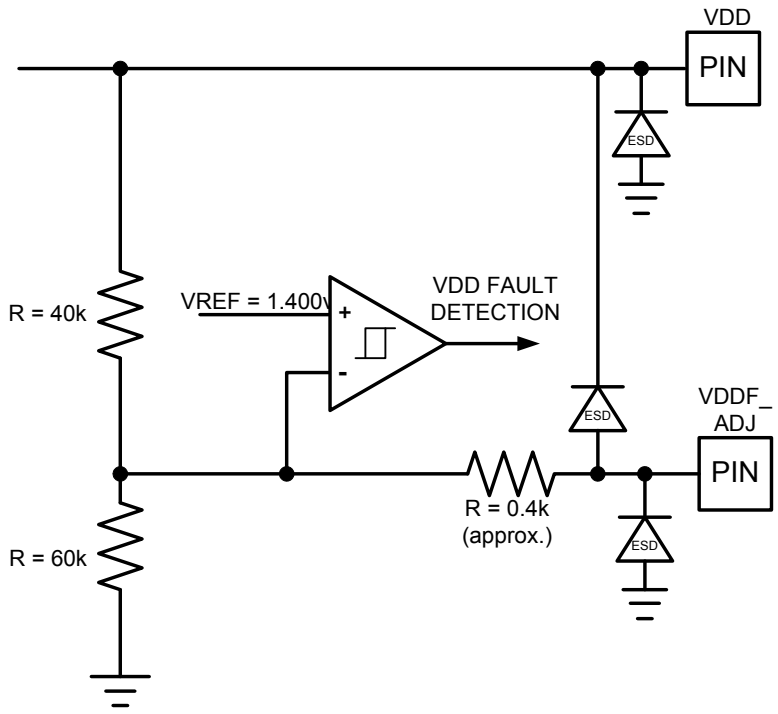


Figure 18: VDDF_ADJ

5 Mechanical Drawing

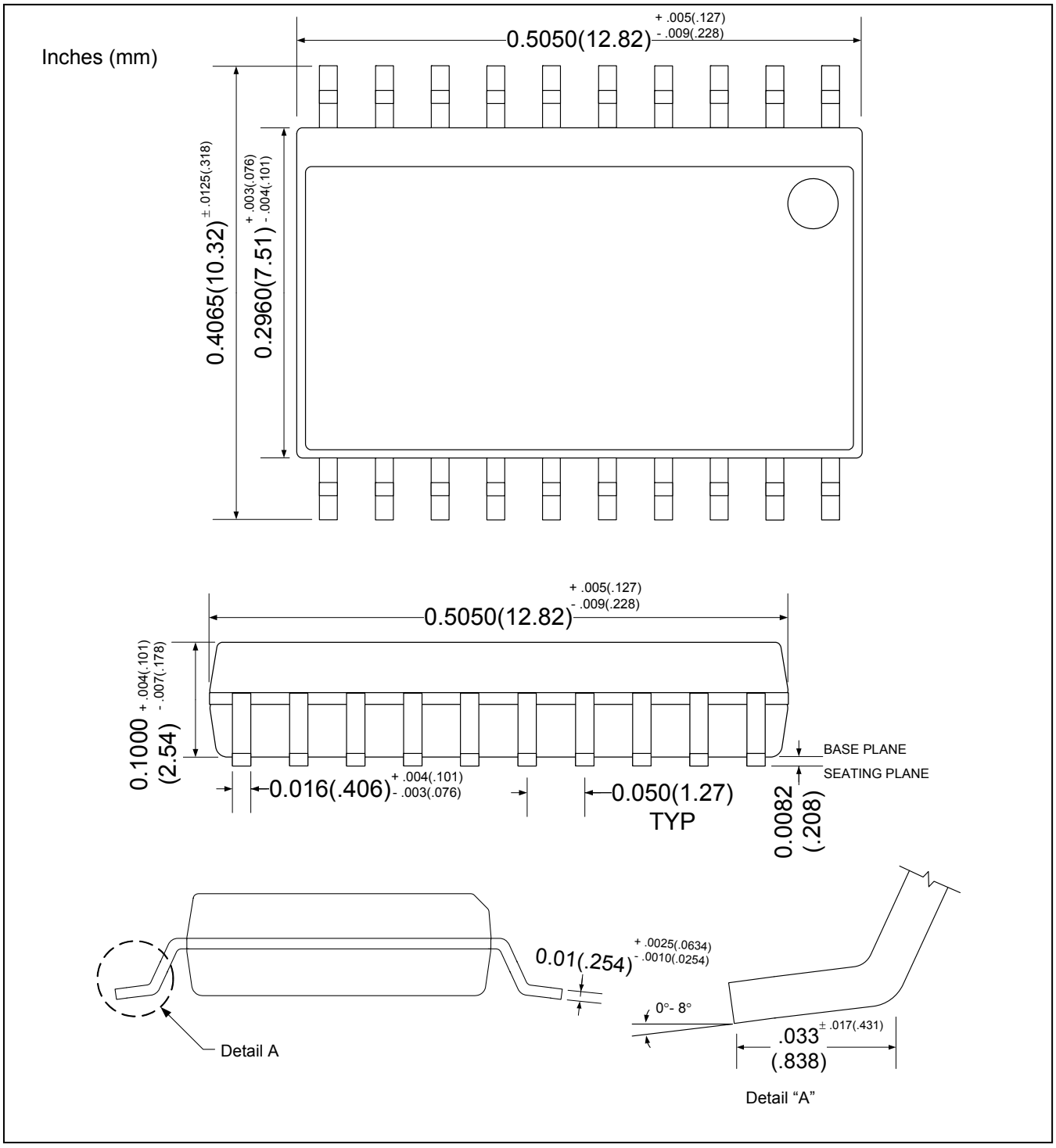


Figure 19: Mechanical Drawing 20-Pin SO Package

6 Ordering Information

Table 9 lists the order numbers and packaging marks used to identify 73S8014R products.

Table 9: Order Numbers and Packaging Marks

Part Description	Order Number	Packaging Mark
73S8014R 20-pin Lead-Free	73S8014R-IL/F	73S8014R
73S8014R 20-pin Lead-Free Tape / Reel	73S8014R-ILR/F	73S8014R

7 Related Documentation

The following 73S8014R document is available from Teridian Semiconductor Corporation:

73S8014R/RN/RT 20SO Demo Board User Manual

8 Contact Information

For more information about Teridian Semiconductor products or to check the availability of the 73S8014R, contact us at:

6440 Oak Canyon Road
Irvine, CA 92618-5201

Telephone: (714) 508-8800
FAX: (714) 508-8878
Email: scr.support@teridian.com

For a complete list of worldwide sales offices, go to http://www.teridian.com.

Revision History

Revision	Date	Description
1.0	9/3/2008	First publication.

Teridian Semiconductor Corp., 6440 Oak Canyon Rd., Suite 100, Irvine, CA 92618
TEL (714) 508-8800, FAX (714) 508-8877, http://www.Teridian.com

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