

SCOPE: QUAD SPST CMOS ANALOG SWITCHES

<u>Device Type</u>	<u>Generic Number</u>
01	DG201AA(x)/883B
02	DG202A(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

<u>Outline Letter</u>	<u>Mil-Std-1835</u>	<u>Case Outline</u>	<u>Package Code</u>
L	CDFP4-F16	16 LEAD FLATPACK	F16
K	GDIP1-T16 or CDIP2-T16	16 LEAD CERDIP	J16
Z	CQCC1-N20	20-Pin Ceramic LCC	L20

Absolute Maximum Ratings

Voltage Referenced to V-

V+	44V
GND	25V
Digital Inputs, V _S , V _D (Note 1)	-2V to (V ⁺ +2V) or 20mA, whichever occurs first
Current, Any terminal except S or D	30mA
Continuous Current, S or D	20mA
(Pulsed at 1ms, 10% duty cycle max)	70mA
Lead Temperature (soldering, 10 seconds)	+300°C
Storage Temperature	-65°C to +150°C

Continuous Power Dissipation	T _A =+70°C
16 lead Flatpack (derate 6.1mW/°C above +70°C)	485mW
16 lead CERDIP(derate 10mW/°C above +70°C)	800mW
20-Pin LCC (derate 9.1mW/°C above +70°C)	727mW
Junction Temperature T _J	+150°C
Thermal Resistance, Junction to Case, Θ _{JC} :	
Case Outline 16 lead Flatpack	65°C/W
Case Outline 16 lead CERDIP	50°C/W
Case Outline 20-Pin LCC	20°C/W
Thermal Resistance, Junction to Ambient, Θ _{JA} :	
Case Outline 16 lead Flatpack	165°C/W
Case Outline 16 lead CERDIP	100°C/W
Case Outline 20-Pin LCC	110°C/W

Recommended Operating Conditions.

Ambient Operating Range (T _A)	-55°C to +125°C
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NOTE 1: Signals on S_X, D_X, or IN_X exceeding V⁺ or V⁻ are clamped by internal diodes, and are also internally current limited to 25mA.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS

TEST	Symbol	CONDITIONS -55 °C ≤T _A ≤ +125°C V ₊ =+15V, V ₋ =-15V, GND=0V Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
SWITCH							
Analog-Signal Range	V _{ANALOG}	V _S =±15V	1,2,3	All	-15	15	V
Drain-Source ON Resistance	r _{DS(ON)}	I _S =1mA, V _D =10V, V _{IN} =0.8V	1,3 2	01		175 250	Ω
Drain-Source ON Resistance	r _{DS(ON)}	I _S =1mA, V _D =-10V, V _{IN} =0.8V	1,3 2	01		175 250	Ω
Drain-Source ON Resistance	r _{DS(ON)}	I _S =1mA, V _D =10V, V _{IN} =2.4V	1,3 2	02		175 250	Ω
Drain-Source ON Resistance	r _{DS(ON)}	I _S =1mA, V _D =-10V, V _{IN} =2.4V	1,3 2	02		175 250	Ω
Source OFF Leakage Current	I _{S(OFF)}	V _S =+/-14V, V _D =-/+14V, V _{IN} =2.4V	1 2,3	01	-1 -100	1 100	nA
Source OFF Leakage Current	I _{S(OFF)}	V _S =+/-14V, V _D =-/+14V, V _{IN} =0.8V	1 2,3	02	-1 -100	1 100	nA
Drain OFF Leakage Current	I _{D(OFF)}	V _S =+/-14V, V _D =-/-14V, V _{IN} =2.4V	1 2,3	01	-1 -100	1 100	nA
Drain OFF Leakage Current	I _{D(OFF)}	V _S =+/-14V, V _D =-/+14V, V _{IN} =0.8V	1 2,3	02	-1 -100	1 100	nA
Drain ON Leakage Current	I _{D(ON)}	V _D =V _S =±14V, V _{IN} =0.8V	1 2,3	01	-2 -200	2 200	nA
Drain ON Leakage Current	I _{D(ON)}	V _D =V _S =±14V, V _{IN} =2.4V	1 2,3	02	-2 -200	2 200	nA
INPUT							
Input Current/Voltage High	I _{INH}	V _{IN} = 2.4V	1,2,3	All	-1		μA
		V _{IN} =15V	1,3 2	All		1 10	
Input Current/Voltage Low	I _{INL}	V _{IN} =0V	1,3 2	All	-1 -10		μA
SUPPLY							
Positive Supply Current	I ₊	All channels on or off	1,2 3	All		0.5 1.0	mA
Negative Supply Current	I ₋	All channels on or off	1,3 2	All	-10 -100		μA
DYNAMIC							
Turn ON time	t _{ON}	Figure 1	9 10,11	All		600 1000	ns
Turn OFF time	t _{OFF}	Figure 1	9 10,11	All		450 650	ns

FIGURE 1: SWITCHING TIME TEST CIRCUIT: See Commercial Data Sheet

TRUTH TABLE

TERMINAL CONNECTION

Device Type	Logic	Switch		TERMINAL NUMBER	DG201A & DG202	DG201A & DG202
01	0	ON			J16 & F16	L20
01	1	OFF		1	IN ₁	NC
02	0	OFF		2	D ₁	IN ₁
02	1	ON		3	S ₁	D ₁
				4	V-	S ₁
				5	GND	V-
				6	S ₄	NC
				7	D ₄	GND
ORDERING	Information			8	IN ₄	S ₄
01	DG201AAK	/883B		9	IN ₃	D ₄
01	DG201AAL	/883B		10	D ₃	IN ₄
01	DG201AAZ	/883B		11	S ₃	NC
02	DG202AK	/883B		12	NC	IN ₃
				13	V+	D ₃
				14	S ₂	S ₃
				15	D ₂	NC
				16	IN ₂	NC
				17		V+
				18		S ₂
				19		D ₂
				20		IN ₂

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

- a. End-point electrical parameters shall be specified in Table 1.
- b. Steady-state life test, Method 1005 of Mil-Std-883:
 1. Test condition A, B, C, D.
 2. TA = +125°C, minimum.
 3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9
Group A Test Requirements Method 5005	1, 2, 3, 9, 10**, 11**
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.

** Subgroups 10 and 11, if not tested shall be guaranteed to the limits of Table 1.

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