Rev 1; 3/09

High-Voltage, NV, I²C POT

DS3502

General Description

The DS3502 is a 7-bit, nonvolatile (NV) digital potentiometer (POT) featuring an output voltage range of up to 15.5V. Programming is accomplished by an I²C-compatible interface, which can operate at speeds of up to 400kHz. External voltages are applied at the RL and RH inputs to define the lowest and highest potentiometer outputs.

Applications

TFT-LCD V_{COM} Calibration

Instrumentation and Industrial Controls

Mechanical POT Replacement

Pin Configuration and Typical Operating Circuit appear at end of data sheet.

Features

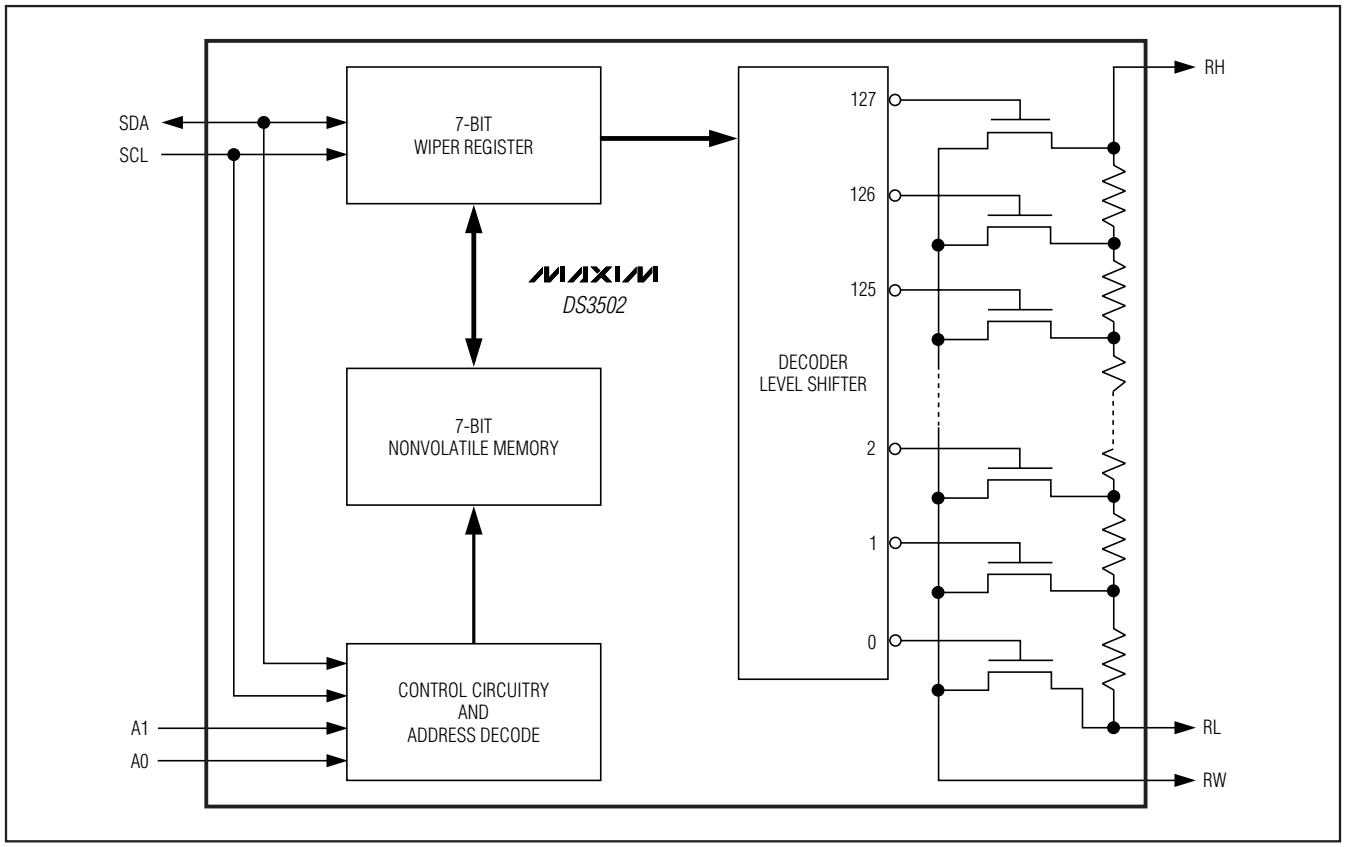
- **128 Wiper Tap Points**
- **Full-Scale Resistance: 10kΩ**
- **I²C-Compatible Serial Interface**
- **Address Pins Allow Up to Four DS3502s to Share the Same I²C Bus**
- **Digital Operating Voltage: 2.5V to 5.5V**
- **Analog Operating Voltage: 4.5V to 15.5V**
- **Operating Temperature: -40°C to +100°C**
- **10-Pin µSOP Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS3502U+	-40°C to +100°C	10 µSOP
DS3502U+T&R	-40°C to +100°C	10 µSOP

+Denotes a lead(Pb)-free/RoHS-compliant package.
T&R = Tape and reel.

Functional Diagram



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ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{CC} Relative to GND .....-0.5V to +6.0V
Voltage Range on V+ Relative to GND .....-0.5V to +17V
Voltage Range on SDA, SCL, A0, A1
Relative to GND.....-0.5V to (V_{CC} + 0.5V), not to exceed 6.0V
Voltage Range on RH, RL, RW.....-0.5V to V+
Voltage Range Across RH and RL Pins .....-0.5V to V+
Operating Temperature Range .....-40°C to +100°C
Programming Temperature Range .....0°C to +70°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature.....Refer to the IPC/JEDEC J-STD-020 Specification.
Maximum RW Current.....1mA

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +100°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	+2.5		+5.5	V
V+ Voltage	V+	V+ > V_{CC}	+4.5		+15.5	V
Input Logic 1 (SCL, SDA, A0, A1)	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.3	V
Input Logic 0 (SCL, SDA, A0, A1)	V_{IL}		-0.3		0.3 x V_{CC}	V
Resistor Inputs (RL, RW, RH)	V_{RES}		-0.3		+15.5	V
Wiper Current	I_{WIPER}				1	mA

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.5V to +5.5V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Supply Current	I_{CC}	(Note 2)		0.2	3	mA
Standby Supply Current	I_{STBY}	(Note 3)			10	µA
V+ Bias Current	I_{V+}				+1	µA
Input Leakage (SDA, SCL, A0, A1)	I_L		-1		+1	µA
Wiper Response Time	t_{WRS}				1	µs
Low-Level Output Voltage (SDA)	V_{OL}	3mA sink current	0.0		0.4	V
I/O Capacitance	$C_{I/O}$			5	10	pF
Power-Up Recall Voltage	V_{POR}	(Note 4)	1.2		2.4	V
Power-Up Memory Recall Delay	t_D	(Note 5)			3	ms
Wiper Resistance	R_W	V+ = 15.0V			5000	Ω
End-to-End Resistance (RH to RL)	R_{TOTAL}			10		kΩ
R_{TOTAL} Tolerance		T_A = +25°C	-20		+20	%
CH, CL, CW Capacitance	C_{POT}			10		pF

VOLTAGE-DIVIDER CHARACTERISTICS

(V_{CC} = +2.5V to +5.5V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Integral Nonlinearity	INL	(Note 6)	-1		+1	LSB
Differential Nonlinearity	DNL	(Note 7)	-0.5		+0.5	LSB
Zero-Scale Error	ZS_{ERROR}	V+ = 4.5V (Note 8)	0	0.5	2	LSB
Full-Scale Error	FS_{ERROR}	V+ = 4.5V (Note 9)	-2	-1	0	LSB
Ratiometric Temp Coefficient	TCV	WR/IVR register set to 40h		±4		ppm/°C

I²C AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.5V to +5.5V, T_A = -40°C to +100°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$. See Figure 2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 10)	0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$		0.6			µs
Low Period of SCL	t_{LOW}		1.3			µs
High Period of SCL	t_{HIGH}		0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			ns
START Setup Time	$t_{SU:STA}$		0.6			µs
SDA and SCL Rise Time	t_R	(Note 11)	$20 + 0.1C_B$		300	ns
SDA and SCL Fall Time	t_F	(Note 11)	$20 + 0.1C_B$		300	ns
STOP Setup Time	$t_{SU:STO}$		0.6			µs
SDA and SCL Capacitive Loading	C_B	(Note 11)			400	pF
EEPROM Write Time	t_W	(Note 12)		10	20	ms
Pulse-Width Suppression Time at SDA and SCL Inputs	t_{IN}	(Note 13)		50		ns
A0, A1 Setup Time	$t_{SU:A}$	Before START	0.6			µs
A0, A1 Hold Time	$t_{HD:A}$	After STOP	0.6			µs
SDA and SCL Input Buffer Hysteresis				0.05 x V_{CC}		V

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NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = +2.5V to +5.5V)

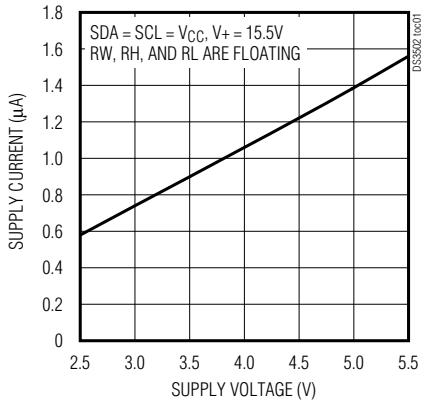
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Write Cycles		T_A = +70°C	50,000			Writes
		T_A = +25°C	200,000			

Note 1: All voltages are referenced to ground. Currents entering the IC are specified positive and currents exiting the IC are negative.
Note 2: I_{CC} is specified with the following conditions: SCL = 400kHz, SDA pulled up, and RL, RW, RH floating.
Note 3: I_{STBY} is specified with SDA = SCL = V_{CC} = 5.5V and resistor pins floating.
Note 4: This is the minimum V_{CC} voltage that causes NV memory to be recalled.
Note 5: This is the time from $V_{CC} > V_{POR}$ until initial memory recall is complete.
Note 6: Integral nonlinearity is the deviation of a measured resistor setting value from the expected values at each particular resistor setting. Expected value is calculated by connecting a straight line from the measured minimum setting to the measured maximum setting. $INL = [V(RW)_i - (V(RW)_0]/LSB(ideal) - i$, for i = 0...127.
Note 7: Differential nonlinearity is the deviation of the step-size change between two LSB settings from the expected step size. The expected LSB step size is the slope of the straight line from measured minimum position to measured maximum position. $DNL = [V(RW)_{i+1} - (V(RW)_i]/LSB(ideal) - 1$, for i = 0...126.
Note 8: ZS error = code 0 wiper voltage divided by one LSB (ideal).
Note 9: FS error = (code 127 wiper voltage - V+) divided by one LSB (ideal).
Note 10: I²C interface timing shown is for fast-mode (400kHz) operation. This device is also backward-compatible with I²C standard mode timing.
Note 11: CB—total capacitance of one bus line in picofarads.
Note 12: EEPROM write time begins after a STOP condition occurs.
Note 13: Pulses narrower than max are suppressed.

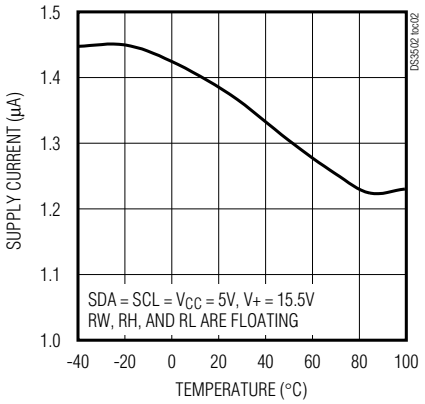
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

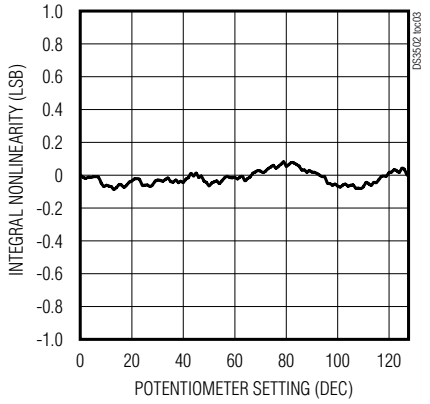
SUPPLY CURRENT vs. SUPPLY VOLTAGE



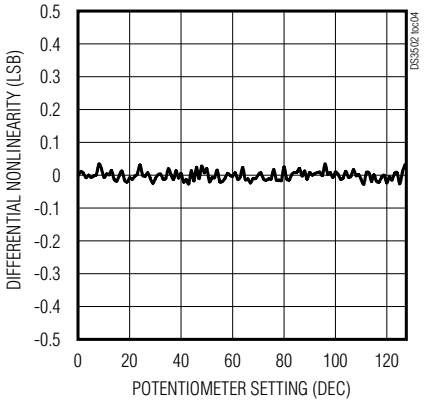
SUPPLY CURRENT vs. TEMPERATURE



INTEGRAL NONLINEARITY vs. POTENTIOMETER SETTING



DIFFERENTIAL NONLINEARITY vs. POTENTIOMETER SETTING



Pin Description

NAME	PIN	FUNCTION
SDA	1	I²C Serial Data. Input/output for I²C data.
GND	2	Ground Terminal
V_{CC}	3	Supply Voltage Terminal
A1, A0	4, 5	Address Select Inputs. Determines I²C slave address. Slave address is 01010A_1A_0X. (See the *Slave Address Byte and Address Pins* section for details).
RH	6	High Terminal of Potentiometer
RW	7	Wiper Terminal of Potentiometer
RL	8	Low Terminal of Potentiometer
V+	9	Wiper Bias Voltage
SCL	10	I²C Serial Clock. Input for I²C clock.

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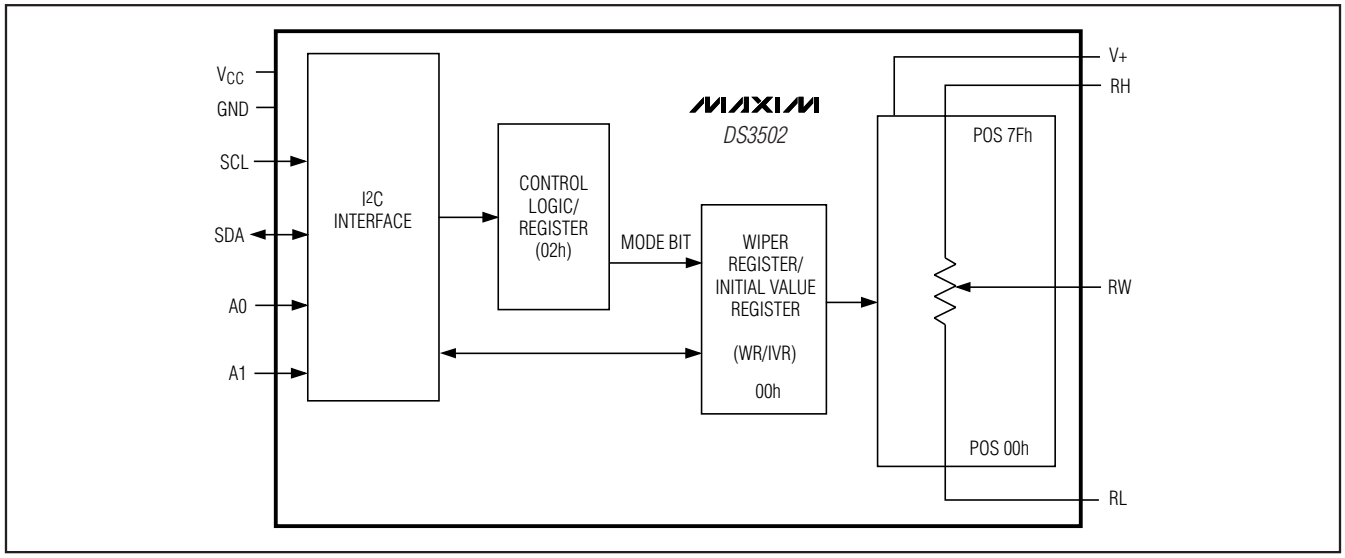
Simplified Functional Diagram



Detailed Description

The DS3502 contains a single potentiometer whose wiper position is controlled by the value in the Wiper Register (WR). The initial power-up value of the wiper position is set by programming the Initial Value Register (IVR). On power-up, the data stored in the IVR register is loaded into the WR register, which sets the position of the potentiometer's wiper.

Control Register

The Control Register (CR) located in register 02h contains the WR/IVR Address Mode bit (MODE bit). The MODE bit determines how I²C data is written to the WR and IVR data register as follows:

MODE = 0: (CR = 00h) I²C writes to memory address 00h write to both WR and IVR.

I²C reads from address 00h read from WR.

MODE = 1: (CR = 80h) I²C writes to memory address 00h write to WR.

I²C reads from address 00h read from WR.

Regardless of the setting of the MODE bit, all I²C reads of address 00h return the contents of the WR register. Setting MODE = 1 allows for quick writing of SRAM without the added delay of writing to the associated EEPROM register. The data that is stored in EEPROM and SRAM remains unchanged if the MODE bit is toggled. The volatile CR register powers up as 00h, setting the device into MODE = 0.

Digital Potentiometer Output

The potentiometer consists of 127 resistors in series connected between the RH and RL pins. Between each resistance and at the two endpoints, RH and RL, solid-state switches enable RW to be connected within the resistive network. The wiper position and the output on RW are decoded based on the value in WR. If RH, RL, and RW are externally connected in a voltage-divider configuration, then the voltage on RW can be easily calculated using the following equation:

$$V_{RW} = V_{RL} + \frac{WR}{127}(V_{RH} - V_{RL})$$

where WR is the wiper position in decimal (0–127).

Table 1. Memory Map

REGISTER	NAME	ADDRESS (HEX)	FACTORY/POWER-UP DEFAULT (HEX)
WR/IVR	Wiper Register/Initial Value Register	00	40
CR	Control Register	02	00 (Mode 0)

Slave Address Byte and Address Pins

The slave address byte consists of a 7-bit slave address plus a R/$\overline{W}$ bit (see Figure 1). The DS3502's slave address is determined by the state of the A0 and A1 address pins. These pins allow up to four devices to reside on the same I²C bus. Address pins tied to GND result in a 0 in the corresponding bit position in the slave address. Conversely, address pins tied to V_{CC} result in a 1 in the corresponding bit positions. For example, the DS3502's slave address byte is 50h when A0 and A1 pins are grounded. I²C communication is described in detail in the *I²C Serial Interface Description* section.

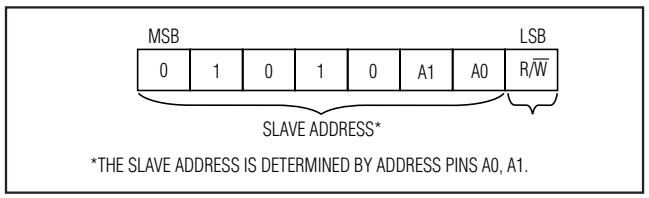


Figure 1. DS3502 Slave Address Byte

I²C Serial Interface Description

I²C Definitions

The following terminology is commonly used to describe I²C data transfers. (See Figure 2 and the *I²C AC Electrical Characteristics* table for additional information.)

Master device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses and START and STOP conditions.

Slave devices: Slave devices send and receive data at the master's request.

Bus idle or not busy: Time between STOP and START conditions when both SDA and SCL are inactive and in their logic-high states.

START condition: A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a START condition.

STOP condition: A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition.

Repeated START condition: The master can use a repeated START condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated STARTS are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated START condition is issued identically to a normal START condition.

Bit write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold time requirements. Data is shifted into the device during the rising edge of the SCL.

Bit read: At the end of a write operation, the master must release the SDA bus line for the proper amount of setup time before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the

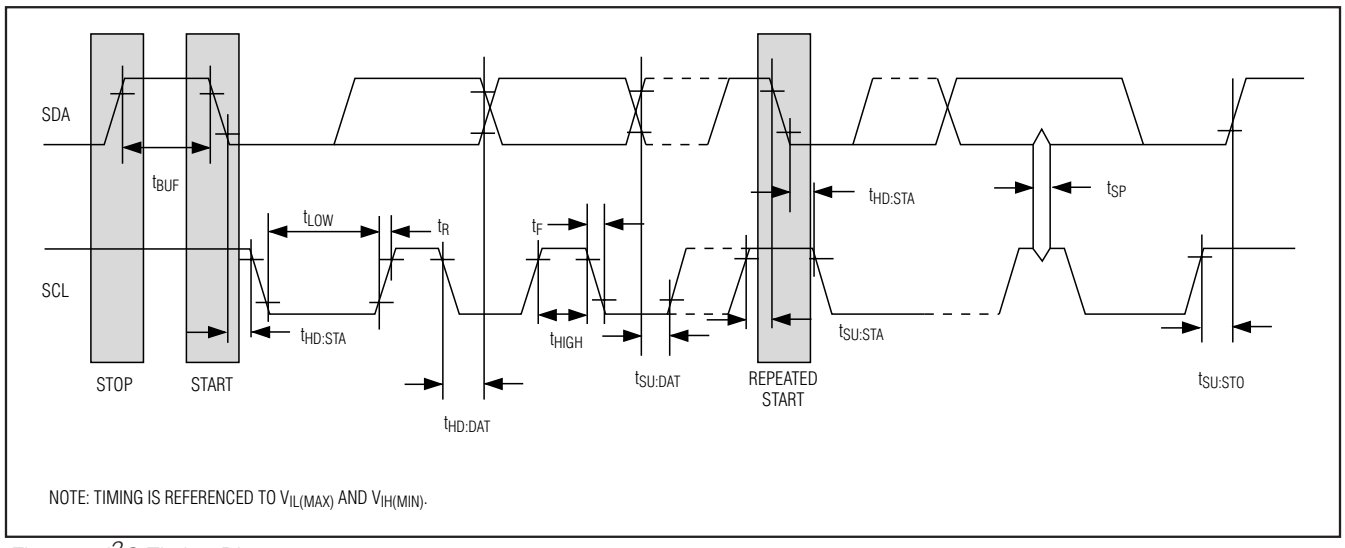


Figure 2. I²C Timing Diagram

data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses, including when it is reading bits from the slave.

Acknowledge (ACK and NACK): An Acknowledge (ACK) or Not Acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a 0 during the 9th bit. A device performs a NACK by transmitting a 1 during the 9th bit. Timing for the ACK and NACK is identical to all other bit writes. An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or indicates that the device is not receiving data.

Byte write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgment from the slave to the master. The 8 bits transmitted by the master are done according to the bit write definition and the acknowledgment is read using the bit read definition.

Byte read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition above, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminate communication so the slave will return control of SDA to the master.

Slave address byte: Each slave on the I²C bus responds to a slave address byte sent immediately following a START condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit. The slave address byte of the DS3502 is shown in Figure 1.

When the R/$\overline{W}$ bit is 0 (such as in 50h), the master is indicating it will write data to the slave. If R/$\overline{W}$ = 1 (51h in this case), the master is indicating it wants to read from the slave.

If an incorrect slave address is written, the DS3502 assumes the master is communicating with another I²C device and ignores the communication until the next START condition is sent.

Memory address: During an I²C write operation, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

I²C Communication

Writing a single byte to a slave: The master must generate a START condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data, and generate a STOP condition. Remember the master must read the slave's acknowledgment during all byte write operations.

When writing to the DS3502, the potentiometer adjusts to the new setting once it has acknowledged the new data that is being written, and the EEPROM is written following the STOP condition at the end of the write command. To change the setting without changing the EEPROM, terminate the write with a repeated START condition before the next STOP condition occurs. Using a repeated START condition prevents the t_W delay required for the EEPROM write cycle to finish.

Acknowledge polling: Any time a EEPROM byte is written, the DS3502 requires the EEPROM write time (t_W) after the STOP condition to write the contents of the byte to EEPROM. During the EEPROM write time, the device will not acknowledge its slave address because it is busy. It is possible to take advantage of this phenomenon by repeatedly addressing the DS3502, which allows communication to continue as soon as the DS3502 is ready. The alternative to acknowledge polling is to wait for a maximum period of t_W to elapse before attempting to access the device.

EEPROM write cycles: The DS3502's EEPROM write cycles are specified in the *Nonvolatile Memory Characteristics* table. The specification shown is at the worst-case temperature (hot) as well as at room temperature. Writing to the WR/IVR register with MODE = 1 does not count as a EEPROM write.

Reading a single byte from a slave: Unlike the write operation that uses the specified memory address byte to define where the data is to be written, the read operation occurs at the present value of the memory address counter. To read a single byte from the slave, the master generates a START condition, writes the slave address byte with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a STOP condition. However, since requiring the master to keep track of the memory address counter is impractical, the following method should be used to perform reads from a specified memory location.

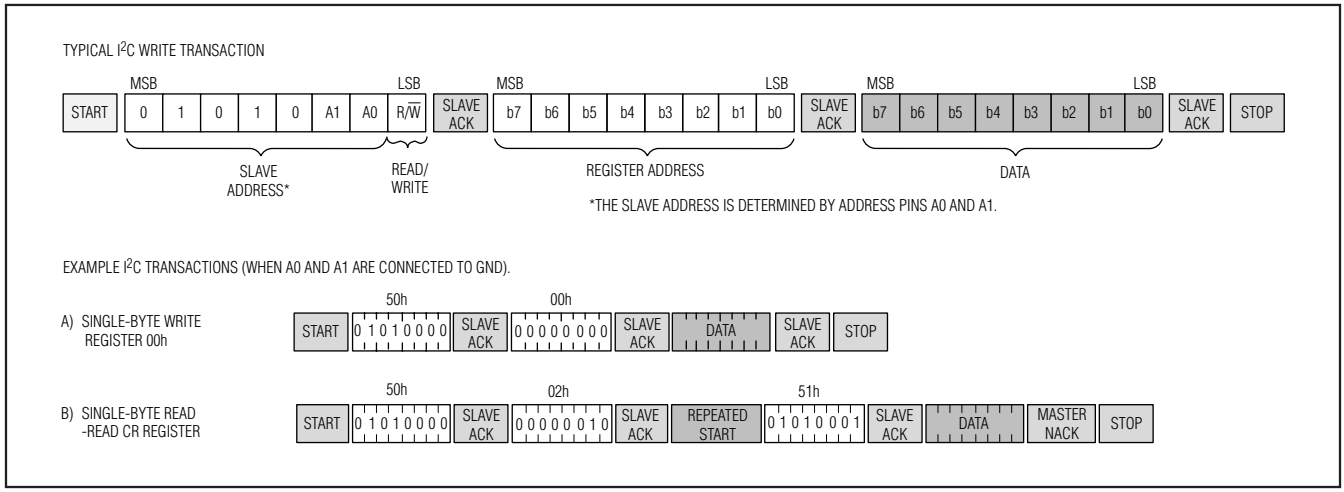


Figure 3. I²C Communication Examples

Manipulating the address counter for reads: A dummy write cycle can be used to force the address counter to a particular value. To do this the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address where it desires to read, generates a repeated START condition, writes the slave address byte (R/$\overline{W}$ = 1), reads data with ACK or NACK as applicable, and generates a STOP condition.

See Figure 3 for a read example using the repeated START condition to specify the starting memory location.

Applications Information

Power-Supply Decoupling

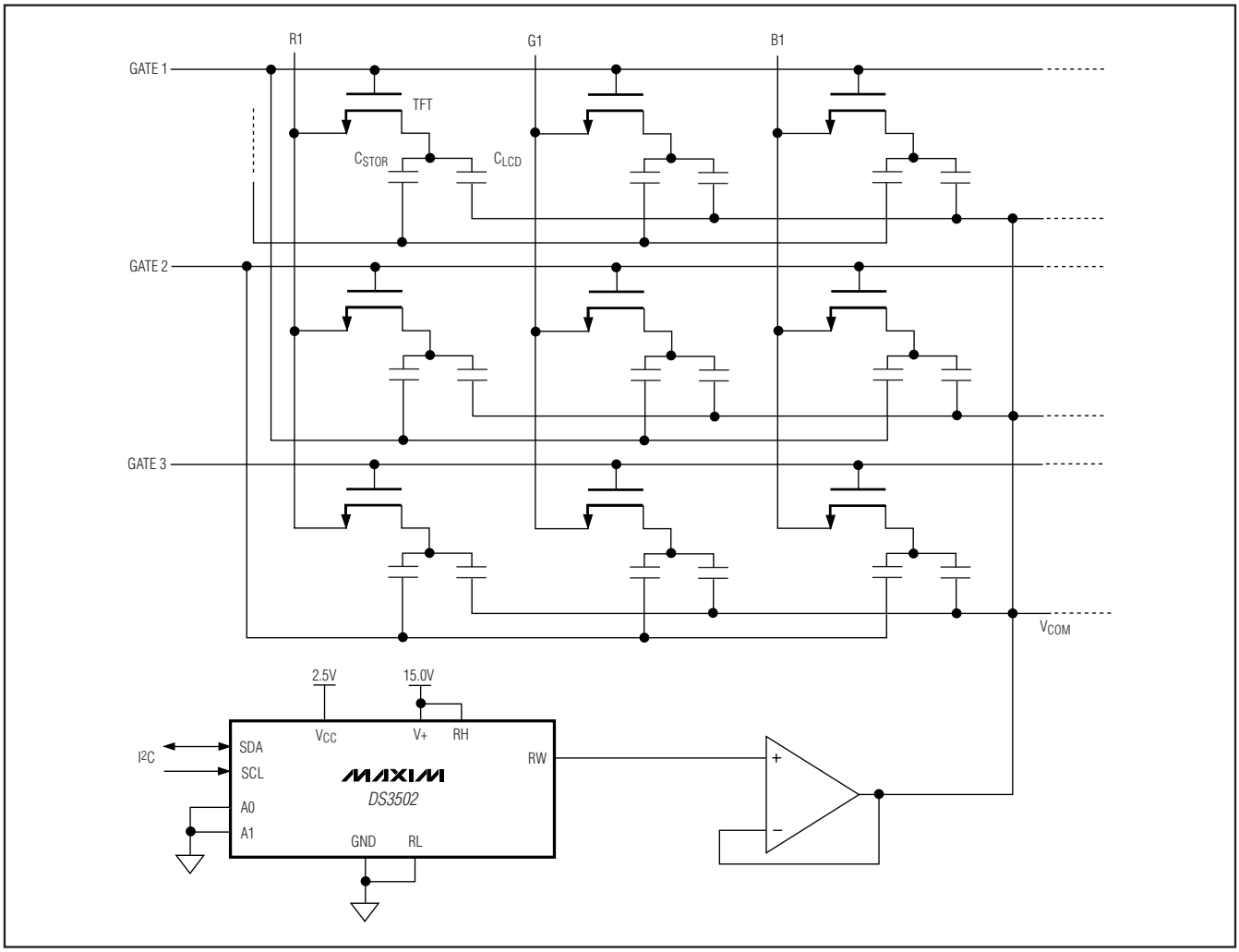
To achieve the best results when using the DS3502, decouple both the power-supply pin (V_{CC}) and the wiper-bias voltage pin (V+) with a 0.01µF or 0.1µF capacitor. Use a high-quality ceramic surface-mount capacitor if possible. Surface-mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high-frequency response for decoupling applications.

SDA and SCL Pullup Resistors

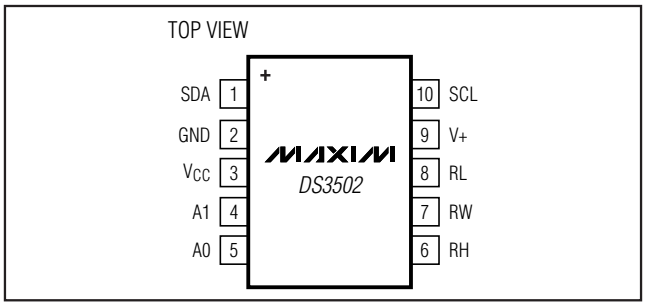
SDA is an I/O with an open-collector output that requires a pullup resistor to realize high-logic levels. A master using either an open-collector output with a pullup resistor or a push-pull output driver must be used for SCL. Pullup resistor values should be chosen to ensure that the rise and fall times listed in the *I²C AC Electrical Characteristics* are within specification. A typical value for the pullup resistors is 4.7kΩ.

High-Voltage, NV, I²C POT

Typical Operating Circuit



Pin Configuration



Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	DOCUMENT NO.
10 µSOP	21-0061

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/08	Initial release.	—
1	3/09	Changed the maximum value of the power-up recall voltage in the *Electrical Characteristics* table from 2.6V to 2.4V.	2

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