Rev 2; 4/08

106.25MHz/212.5MHz/425MHz Clock Oscillators

General Description

The DS4106, DS4212, and DS4425 ceramic surface-mount crystal oscillators are part of Maxim's DS4-XO series of crystal oscillators. These devices offer output frequencies at 106.25MHz, 212.5MHz, and 425MHz. The clock oscillators are suited for systems with tight tolerances because of the jitter, phase noise, and stability performance. The small package provides a format made for applications where PCB space is critical.

These clock oscillators are crystal based and use a fundamental crystal with PLL technology to provide the final output frequencies. Each device is offered with LVDS or LVPECL output types. The output enable pin is active-high logic.

These clock oscillators have very low phase jitter and phase noise. Typical phase jitter is < 0.9ps RMS from 12kHz to 20MHz. The devices are designed to operate with a 3.3V ±10% supply voltage, and are available in a 5.0mm x 3.2mm x 1.49mm, 10-pin LCCC surface-mount ceramic package.

Applications

Fibre Channel Hard Disk Drives

Host Bus Adapters

Raid Controllers

Fibre Channel Switches

Pin Configuration and Selector Guide appear at end of data sheet.

Features

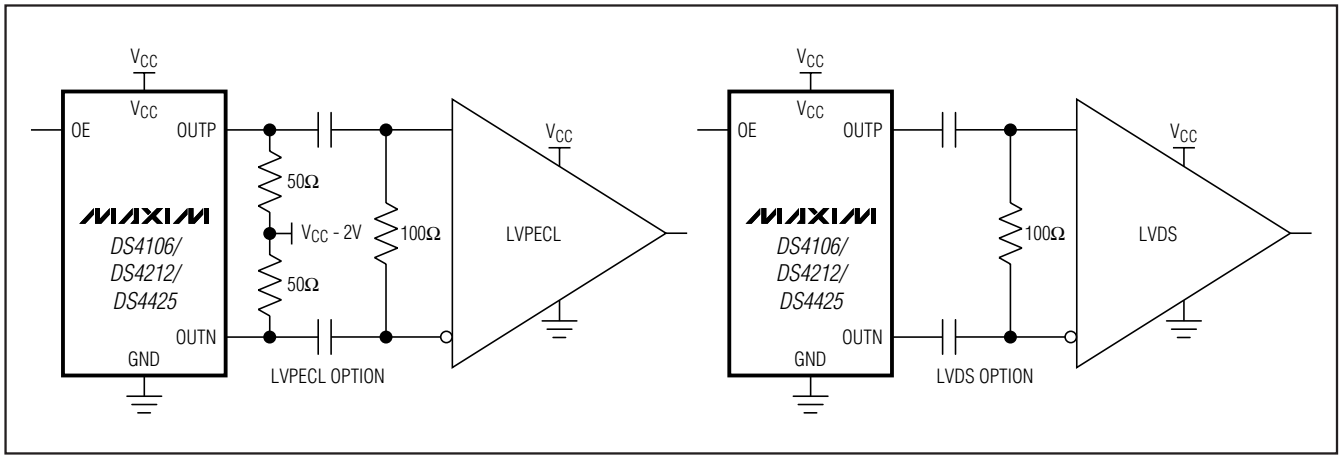
- **Clock Output Frequencies:**
  DS4106: 106.25MHz
  DS4212: 212.50MHz
  DS4425: 425.00MHz
- **Phase Jitter (RMS): 0.9ps Typical**
- **LVPECL or LVDS Output**
- **Supply Current:**
  50mA (Typical, Unloaded) at +3.3V Supply (LVPECL)
  53mA (Typical) at +3.3V Supply (LVDS)
- **-40°C to +85°C Temperature Range**
- **Output Disable**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS4106AN+	-40°C to +85°C	10 LCCC
DS4106BN+	-40°C to +85°C	10 LCCC
DS4212AN+	-40°C to +85°C	10 LCCC
DS4212BN+	-40°C to +85°C	10 LCCC
DS4425AN+	-40°C to +85°C	10 LCCC
DS4425BN+	-40°C to +85°C	10 LCCC

+Denotes a lead(Pb)-free package. The lead finish is JESD97 category e4 (Au over Ni) and is compatible with both lead-based and lead-free soldering processes.

Typical Operating Circuits



106.25MHz/212.5MHz/425MHz Clock Oscillators

ABSOLUTE MAXIMUM RATINGS

V_{CC}, GND, OE, OUTP, OUTN .....-0.3V, +4V
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-40°C to +125°C
Soldering Temperature Profile
(3 passes max) .....See IPC/JEDEC J-STD-020 Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 3.6V, T_A = -40°C to +85°C, typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 2)	3.0	3.3	3.6	V
Supply Current	I_{CC}	LVPECL (Note 3)		50	65	mA
		LVDS		53	67	
TTL Control Input-Voltage High (OE)	V_{IH}	(Note 2)	2		V_{CC}	V
TTL Control Input-Voltage Low (OE)	V_{IL}	(Note 2)	0		0.8	V
Input Leakage Current	I_{IL}	GND ≤ OE ≤ V_{CC}	-50		+10	µA
LVPECL OUTPUTS (Note 4)						
Output High Voltage	V_{OH}	(Note 2)	V_{CC} - 1.085		V_{CC} - 0.88	V
Output Low Voltage	V_{OL}	(Note 2)	V_{CC} - 1.825		V_{CC} - 1.62	V
Output Leakage Current (Absolute)	I_{OL}	OE = V_{IL}		100		µA
LVDS OUTPUTS (Figure 2)						
LVDS Output High Voltage	V_{OH}	(Note 2)			1.475	V
LVDS Output Low Voltage	V_{OL}	(Note 2)	0.925			V
LVDS Differential Output Voltage	$\|V_{OD}\|$		250		400	mV
LVDS Change in V_{OD} for Complementary States	$\Delta\|V_{OD}\|$				25	
LVDS Offset Output Voltage (Output Common-Mode Voltage)	V_{OS}	(Note 5)	1.125		1.275	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.0V to 3.6V, T_A = -40°C to +85°C, typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LVDS Change in V_{OS} for Complementary States	$\Delta\|V_{OS}\|$					150	mV
LVDS Differential Output Impedance	R_{OLVDSO}			80		140	Ω
LVDS Output Current	I_{LVDSO}	Outputs shorted together			12		mA
Output Current	$I_{VSSLVDSO}$	Short to ground				40	mA
CLOCK OUTPUT							
Clock Output Frequency	f_O	DS4106			106.25		MHz
		DS4212			212.5		
		DS4425			425.0		
Frequency Stability Total	$\Delta f / f_O$	Temperature, aging, load, and supply		-39		+39	ppm
Initial Frequency Tolerance	f_TOL	+25°C, ±3°C, V_{CC} = 3.3V			±20		ppm
Frequency Stability vs. Temperature	$\Delta f / f_O \|_{TA}$			-30		+30	ppm
Frequency Stability vs. V_{CC}	$\Delta f / f_O \|_V$	V_{CC} = 3.3V ±10%		-3		+3	ppm/V
Frequency Stability vs. Load	$\Delta f / f_O \|_{LOAD}$	±10% variation in termination resistance			±1		ppm
Aging (15 Years)	f_{AGING}			-7		+7	ppm
Phase Jitter (RMS)	PJ_{RMS}	12kHz to 20MHz			0.9		ps
Accumulated Deterministic Jitter Due to Power-Supply Noise (P-P)		10kHz			3		ps
		100kHz			27		
		200kHz			15		
		1MHz			7		
Clock Output Edge Speeds	t_R, t_F	20% to 80%	LVPECL		200		ps
			LVDS		175		
Clock Output Duty Cycle		+25°C		45		55	%
Oscillation Startup Time		(Note 6)			10		ms

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.0V to 3.6V, T_A = -40°C to +85°C, typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Clock Output SSB Phase Noise		DS4106 at 106.25MHz	100Hz		-90		dBc/Hz
			1kHz		-112		
			10kHz		-115		
			100kHz		-123		
			1MHz		-142		
			10MHz		-147		
		DS4212 at 212.50MHz	100Hz		-82		
			1kHz		-106		
			10kHz		-109		
			100kHz		-117		
			1MHz		-136		
			10MHz		-141		
		DS4425 at 425.00MHz	100Hz		-76		
			1kHz		-100		
			10kHz		-103		
			100kHz		-111		
			1MHz		-130		
			10MHz		-135		

Note 1: Limits at -40°C are guaranteed by design and are not production tested.
Note 2: Voltage referenced to ground.
Note 3: Outputs are enabled and unloaded.
Note 4: When the LVPECL output is disabled, the typical output off current is < 100µA for nominal LVPECL signal levels at the output.
Note 5: AC parameters are guaranteed by design and characterization.
Note 6: Including oscillator startup time and PLL acquisition time, measured after V_{CC} reaches 3.0V from power-on.

Pin Description

PIN	NAME	FUNCTION
1	OE	Output Enable. On-chip pullup resistor. Connect OE to logic-high, V_{CC}, or leave open to enable the output clock. Connect OE to logic-low or GND to disable the output clock. The LVPECL output clock is set to high impedance when disabled. The LVDS output clock is latched to a differential high when disabled.
2, 7–10	N.C.	No Connection
3	GND	Ground
4	OUTP	Positive Clock Output, LVPECL or LVDS
5	OUTN	Negative Clock Output, LVPECL or LVDS
6	V_{CC}	+3.3V Supply
—	EP	Exposed Paddle. Do not connect this pad or place exposed metal under the pad.

Detailed Description

The DS4106/DS4212/DS4425 combine a crystal and an IC to form a precision clock. Figure 1 shows a functional diagram of the devices. The IC consists of a crystal oscillator, a low-noise PLL, selectable clock-divider circuitry, and an output buffer. The PLL consists of a digital phase/frequency detector (PFD) and low-jitter generation VCO. The VCO signal is scaled by a clock-divider circuit and applied to the output buffer.

Output Drivers

All devices are available with either LVPECL (DS4106A/DS4212A/DS4425A) or LVDS (DS4106B/DS4212B/DS4425B) output buffers. When not needed, the output buffers can be disabled. When disabled, the LVPECL output buffer goes to a high-impedance state. However, the LVDS outputs go to a differential logic one (OUTP latched high and OUTN latched low) when the outputs are disabled.

Additional Information

For more available frequencies, refer to the DS4125 data sheet at **www.maxim-ic.com/DS4125**.

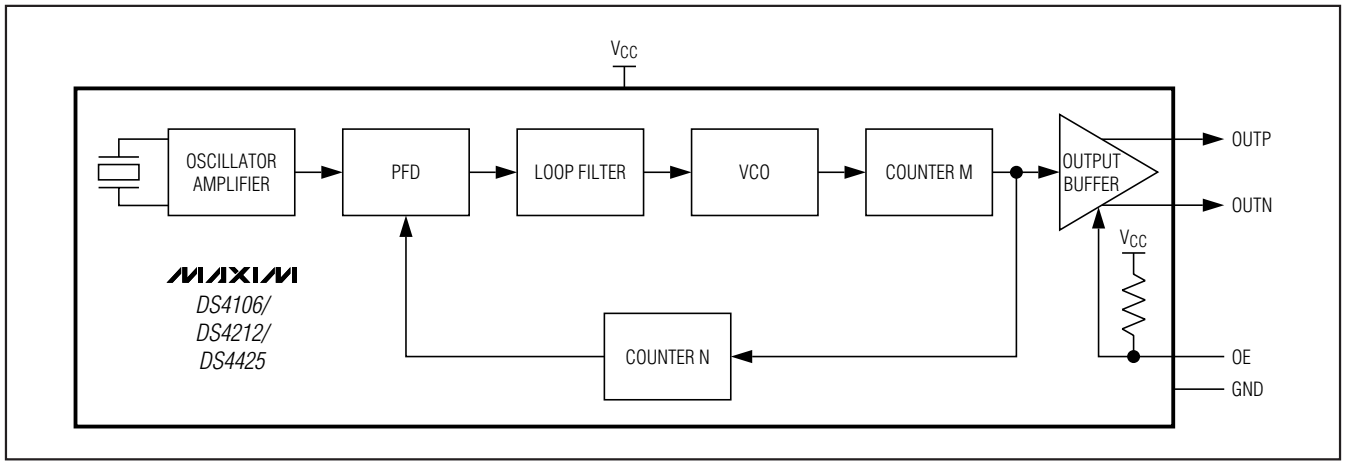


Figure 1. Functional Diagram

106.25MHz/212.5MHz/425MHz Clock Oscillators

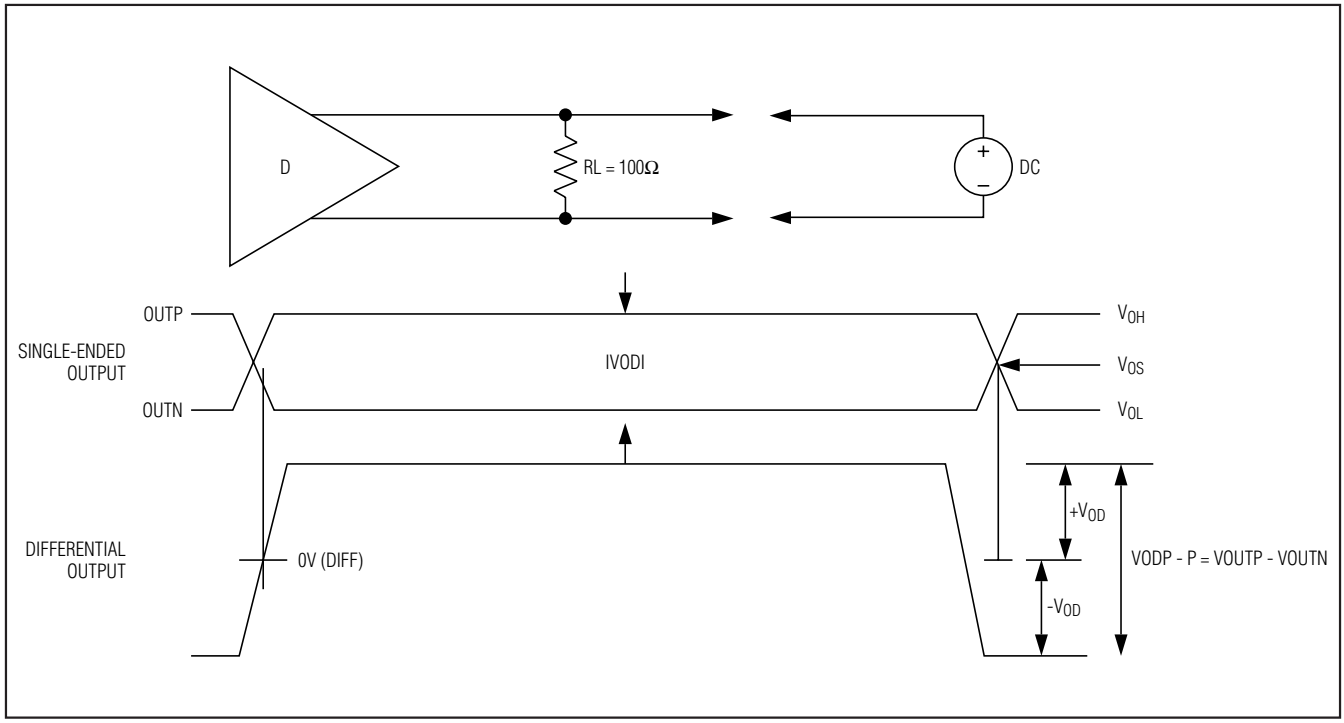


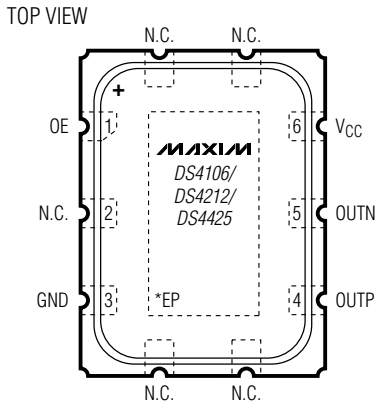
Figure 2. LVDS Level Definitions

Selector Guide

PART	OUTPUTS	FREQUENCY (MHz)	TOP MARK
DS4106AN+	LVPECL	106.25	06A
DS4106BN+	LVDS	106.25	06B
DS4212AN+	LVPECL	212.50	12A
DS4212BN+	LVDS	212.50	12B
DS4425AN+	LVPECL	425.00	42A
DS4425BN+	LVDS	425.00	42B

+Denotes a lead-free package. The lead finish is JESD97 category e4 (Au over Ni) and is compatible with both lead-based and lead-free soldering processes.

Pin Configuration



LCCC
(5.00mm × 3.20mm × 1.49mm)

*EXPOSED PAD

Thermal Information

THETA-JA (°C/W)
90

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
10 LCCC	L1053+H2	**21-0389**

106.25MHz/212.5MHz/425MHz Clock Oscillators

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/07	Initial release.	—
1	10/07	In the *General Description* section, corrected power-supply tolerance from 5% to 10%.	1
		In the Electrical Characteristics table, added the input voltage max value of V_{CC} and input voltage min of 0 for V_{IH} and V_{IL}; added GND ≤ OE ≤ V_{CC} for conditions on input leakage (I_{IL}); corrected Accumulated Deterministic Jitter Due to Reference Spurs parameter to Accumulated Deterministic Jitter Due to Power-Supply Noise.	2, 3
2	4/08	In the Electrical Characteristics table, changed the clock output frequency (f_O) typ from 106.2MHz to 106.25MHz.	3
		In the Pin Description, changed the exposed pad description to indicate that it should not be connected and to avoid placing exposed metal under the pad location.	5

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