19-3984; Rev 3; 1/10

Wired Remote Controller

General Description

The MAX11041 wired remote controller converts up to 30 different pushbuttons into an I²C register. Together with low-cost pushbutton switches and 1% resistors, the MAX11041 is a total solution over a single-wire interface. A wired remote controller easily piggybacks to a standard 3.5mm headphone jack using a fourth contact or one of the audio signals.

To conserve battery life, the MAX11041 consumes only 5µA (typ) while reading keypresses in real time without microprocessor (µP) polling. The device sends the debounced keypress along with key duration to the application processor over the I²C interface. An 8-word FIFO buffer records up to four keypress events to allow plenty of time for the application processor to respond to the MAX11041.

The MAX11041 includes ±15kV ESD protection devices on the FORCE and SENSE inputs to ensure IEC 61000-4-2 compliance without any external ESD devices.

The MAX11041 is available in a 12-pin TQFN package. The device is specified over the extended temperature range (-40°C to +85°C).

Applications

Multimedia Controls for Multimedia-Enabled Cell Phones

Keyboard Encoder for Slider, Flip, and other Cell Phones

Portable Media Players

MP3, CD, DVD Players

PDAs

Digital Still Cameras

PDA Accessory Keyboards

Multimedia Desktop Speakers

Portable Game Consoles

Features

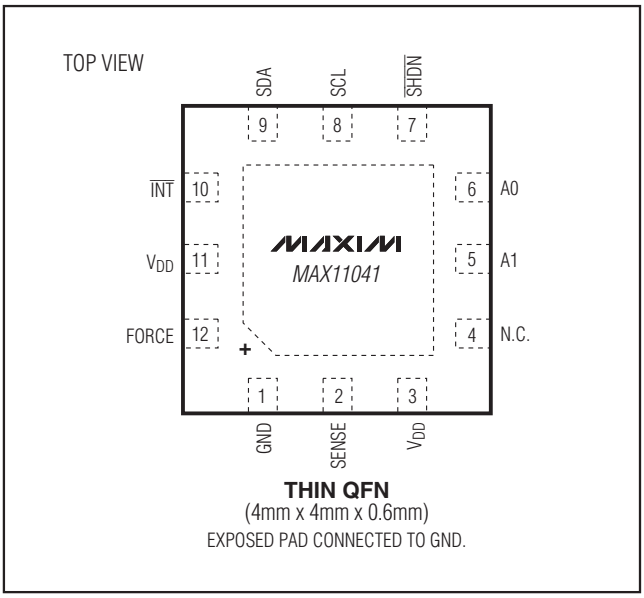
- **Detect Up to 30 Different Keys and Jack Insertion/Removal**
- **Works with Either 32Ω or 16Ω Headphones**
- **Adds Remote-Control Functionality to Devices Using a Simple Resistor and Switch Array**
- **Low-Power Operation Consuming a Supply Current of Only 5µA (typ)**
- **Works with Standard 2.5mm or 3.5mm 4-Pin Headphone Jacks**
- **Supports Hold Function to Lockout Keys**
- **100kHz/400kHz I²C Interface**
- **Single 1.6V to 3.6V Supply Voltage Range**
- **±15kV ESD Protection (IEC 61000-4-2)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX11041ETC+	-40°C to +85°C	12 TQFN-EP*

**EP = Exposed pad.*
+Denotes a lead(Pb)-free/RoHS-compliant package.

Pin Configuration



THIN QFN
(4mm x 4mm x 0.6mm)
EXPOSED PAD CONNECTED TO GND.

Wired Remote Controller

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +4.0V
$\overline{INT}$ to GND .....-0.3V to (V_{DD} + 0.3V)
SCL, SDA, A1, A0, $\overline{SHDN}$ to GND .....-0.3V to +4.0V
FORCE, SENSE to GND .....±6V
Current into Any Pin .....±50mA
Maximum ESD per IEC 61000-4-2
Human Body Model, FORCE, SENSE .....±15kV
FORCE, SENSE Short to GND .....Continuous
Junction Temperature .....+150°C
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +1.6V to 3.6V, C_{SENSE} = 10nF, R_{SENSE} = 10kΩ, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
KEY DETECTION CHARACTERISTICS						
Detectable Keys		Provided the keys meet the next three specifications; R_{JACK} connected; use recommended circuit	30			Keys
Maximum Switch Resistance		(Note 1)		100		Ω
Maximum Switch Bounce Time		(Note 1)		13		ms
External Resistor Tolerance		(Note 1)		±1		%
SWITCH DEBOUNCE						
Debounce Analog Time Constant		C_{SENSE} = 10nF, external resistor from FORCE to SENSE is 10kΩ (R_{SENSE})		0.4		ms
Chatter Rejection		Pulses shorter than this are ignored		18		ms
Rising Voltage Debounce Time	t_{CPW}	Time required for a new voltage (due to keypress) to be detected and stored in FIFO		18		ms
Falling Voltage Debounce Time	t_{LPWS}	Time required for detection of key release and final time duration to be stored in FIFO		18		ms
Jack Insertion Debounce Time		(Note 2)		18		ms
Jack Removal Debounce Time		(Note 2)		18		ms
DURATION COUNTER						
Duration-Counter Resolution		One tick		32		ms
Duration-Counter Range		MSB is overflow bit	0		127	Counts
Duration-Counter Accuracy					±20	%
DIGITAL INPUTS (SDA, SCL, $\overline{SHDN}$, A0, A1)						
Input High Voltage	V_{IH}		0.7 x V_{DD}			V
Input Low Voltage	V_{IL}				0.3 x V_{DD}	V
Input Leakage Current	I_{IH}, I_{IL}		-10		+10	µA
Input Hysteresis				9		%V_{DD}
Input Capacitance				10		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +1.6V to 3.6V, C_{SENSE} = 10nF, R_{SENSE} = 10kΩ, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL OUTPUTS (SDA, $\overline{INT}$)						
Output High Voltage ($\overline{INT}$)	V_{OH}	I_{SOURCE} ≤ 2mA	0.9 x V_{DD}			V
Output Low Voltage ($\overline{INT}$)	V_{OLINT}	I_{SINK} ≤ 2mA			0.1 x V_{DD}	V
Output High Leakage Current	I_{OHL}	V_{OUT} = V_{DD}			1	µA
Output Low Voltage (SDA)	V_{OLSDA}	I_{OL} = 3mA for V_{DD} > 2V			0.4	V
		I_{OL} = 3mA for V_{DD} < 2V			0.2 x V_{DD}	V
I^2C TIMING CHARACTERISTICS (see Figure 1)						
Serial Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD,STA}$		0.6			µs
SCL Pulse-Width Low	t_{LOW}		1.3			µs
SCL Pulse-Width High	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU,STA}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$		0		900	ns
Data Setup Time	$t_{SU,DAT}$		100			ns
SDA and SCL Receiving Rise Time	t_{RR}	(Note 3)	20 + C_b / 10		300	ns
SDA and SCL Receiving Fall Time	t_{FR}	(Note 3)	20 + C_b / 10		300	ns
SDA Transmitting Rise Time	t_{RT}	V_{DD} = 3.6V (Note 3)	20 + C_b / 10		250	ns
SDA Transmitting Fall Time	t_{FT}	V_{DD} = 2.4V to 3.6V	20 + C_b / 20		250	ns
		V_{DD} = 1.6V to 2.4V	20 + C_b / 20		375	
Setup Time for STOP Condition	$t_{SU,STO}$		0.6			µs
Bus Capacitance	C_b				400	pF
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +1.6V to 3.6V, C_{SENSE} = 10nF, R_{SENSE} = 10kΩ, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Power-Supply Voltage	V_{DD}		1.6		3.6	V
Average Operational Supply Current	I_{DDOP}	Excluding jack/key current		5	20	µA
		Jack inserted, R_{JACK} = 619kΩ		8		
Shutdown Power-Supply Current	I_{DDSHDN}	Excluding jack/key current			1	µA
Jack Current	I_{DDJACK}	Flowing when jack is inserted		4		µA
Key Current	$I_{DDBUTTON}$	Flowing when keys pressed (Note 4)		90		µA
$\overline{SHDN}$ High to Part Active		Wake-up time			5	ms

Note 1: Recommended properties of external switch for proper detection of 30 keys or key combinations.
Note 2: See the *Jack Insertion/Removal Detection* section.
Note 3: C_b is the bus capacitance in pF.
Note 4: Key current depends on external key resistors and is calculated by V_{DD} / (30.1kΩ + R_{SW}).

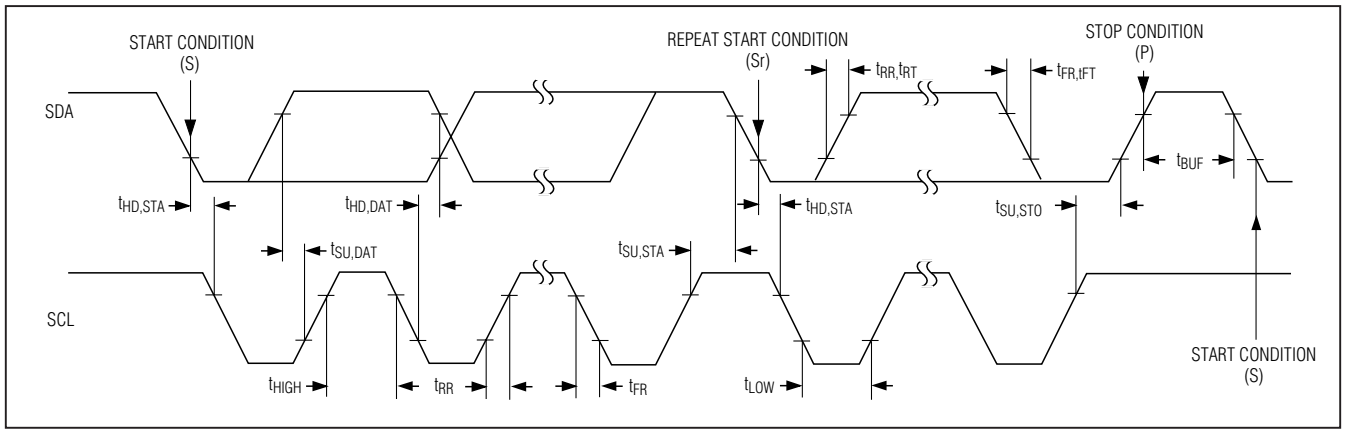
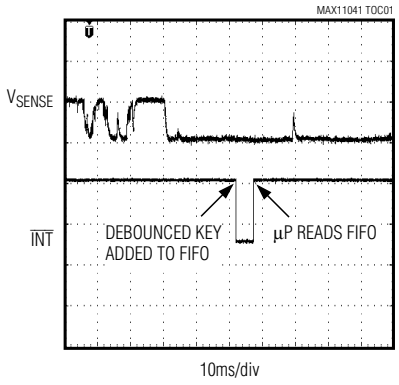


Figure 1. I²C Serial-Interface Timing

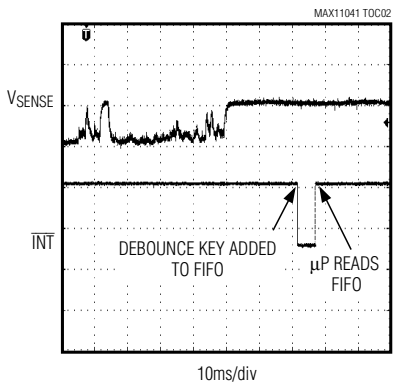
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

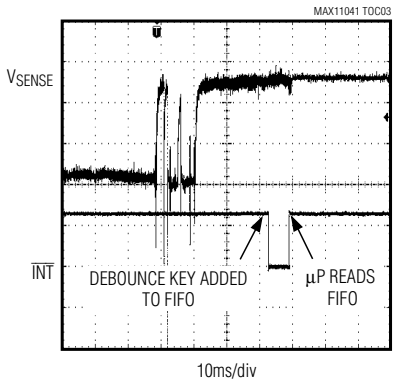
DEBOUNCE SCOPE SHOT (FALLING)



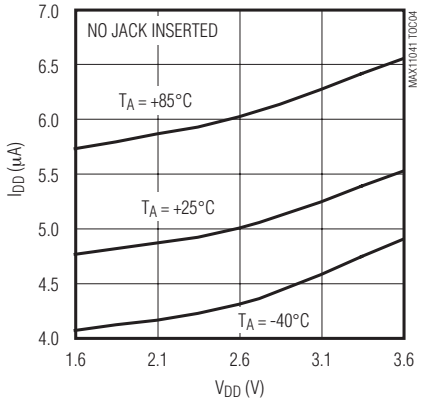
DEBOUNCE SCOPE SHOT (RISING)



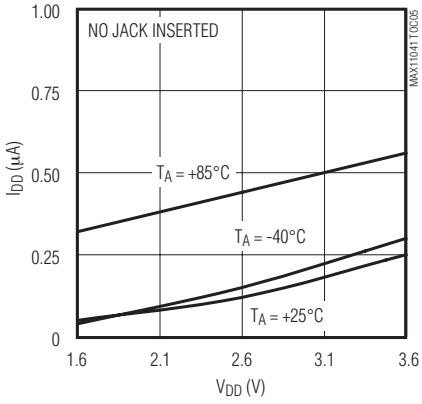
KEYPRESS RELEASE SCOPE SHOT*



V_{DD} SUPPLY CURRENT vs. VOLTAGE



V_{DD} SHUTDOWN SUPPLY CURRENT vs. VOLTAGE



**Oscilloscope shots are taken with simulated bounce and chatter. Real switches will exhibit different bounce and chatter characteristics.*

Wired Remote Controller

Pin Description

PIN	NAME	FUNCTION
1	GND	Ground
2	SENSE	Voltage Sense Input. Connect SENSE to FORCE through an external lowpass filter composed of R_{SENSE} and C_{SENSE} (see the *FORCE and SENSE* section). There is a ±15kV IEC 61000-4-2 ESD protection on SENSE.
3, 11	V_{DD}	Power-Supply Input. Connect both V_{DD} inputs together and bypass each V_{DD} with a 0.1µF capacitor to GND.
4	N.C.	No Connection. Leave unconnected or connect to V_{DD}.
5	A1	I^2C Address Input 1. Logic state represents bit 1 of the I^2C slave address.
6	A0	I^2C Address Input 0. Logic state represents bit 0 of the I^2C slave address.
7	$\overline{SHDN}$	Active-Low Shutdown Input. Bring $\overline{SHDN}$ low to put the MAX11041 in shutdown mode. FORCE is in a high-impedance state while $\overline{SHDN}$ is low.
8	SCL	I^2C Serial-Interface Clock Input. SCL requires a pullup resistor.
9	SDA	I^2C Serial-Interface Data Input/Output. SDA requires a pullup resistor.
10	$\overline{INT}$	Active-Low Interrupt Output. $\overline{INT}$ goes low when a valid keypress is detected at SENSE.
12	FORCE	Force Output. Connect FORCE to the external resistor array. Connect SENSE to FORCE through an external lowpass filter composed of R_{SENSE} = 10kΩ and C_{SENSE} = 10nF. There is a ±15kV IEC 61000-4-2 ESD protection on FORCE.
EP	EP	Exposed Pad. Connect EP to GND.

Detailed Description

The MAX11041 wired remote controller recognizes 30 different keypresses consisting of a resistor/switch array over a single connector. Designed for wired remote controllers on the headphone or headset cord, the MAX11041 contains debouncing circuitry and jack insertion/removal detection. During a keypress, the MAX11041 stores the key type and key duration in an 8-word FIFO and $\overline{INT}$ (interrupt output) goes low. The results stored in the FIFO are accessed through the I^2C interface.

FORCE and SENSE

During a keypress, a unique external resistor ($R_{SW\_}$) located in the remote controller connects SENSE to ground (Figure 2). This event changes the impedance seen by the SENSE line. The MAX11041 decodes this resistor value to an 8-bit result (see the *Required Resistor Set* section). FORCE and SENSE are ±15kV ESD (IEC 61000-4-2) protected.

Register Description

The MAX11041 contains one 8-bit control register, an 8-word FIFO (each word consists of an 8-bit key value and an 8-bit duration value), and an 8-bit chip ID.

Chip ID

The chip ID identifies the features and capabilities of the wired remote controller to the software. For the MAX11041, the chip ID is 0x00.

Control Register

The MAX11041 contains one control register (see Table 1). Bits C7, C6, and C5 control software shutdown. Set FORCE high-impedance and indicate if the FIFO is empty. Write/read to the control register through the I^2C-compatible serial interface (see the *Digital Serial Interface* section).

FIFO

The MAX11041 contains an 8-word FIFO that can hold enough information for four keypresses and releases. Each keypress and release results in two data words being stored into the FIFO. Each FIFO word consists of 2 bytes. The 1st byte is the decoded keypress or release (K7–K0) and the 2nd byte is the keypress or release duration time. Table 2 shows the format of a keypress entry into the FIFO. Read the FIFO through the I^2C-compatible serial interface (see the *Digital Serial Interface* section). At power-up, all the FIFO is reset such that K7–K0 are set to 0xFF hex and 0x0F, and T6–T0 are set to 0x00. See the *Applications Information* section for an example of how data is entered into the FIFO.

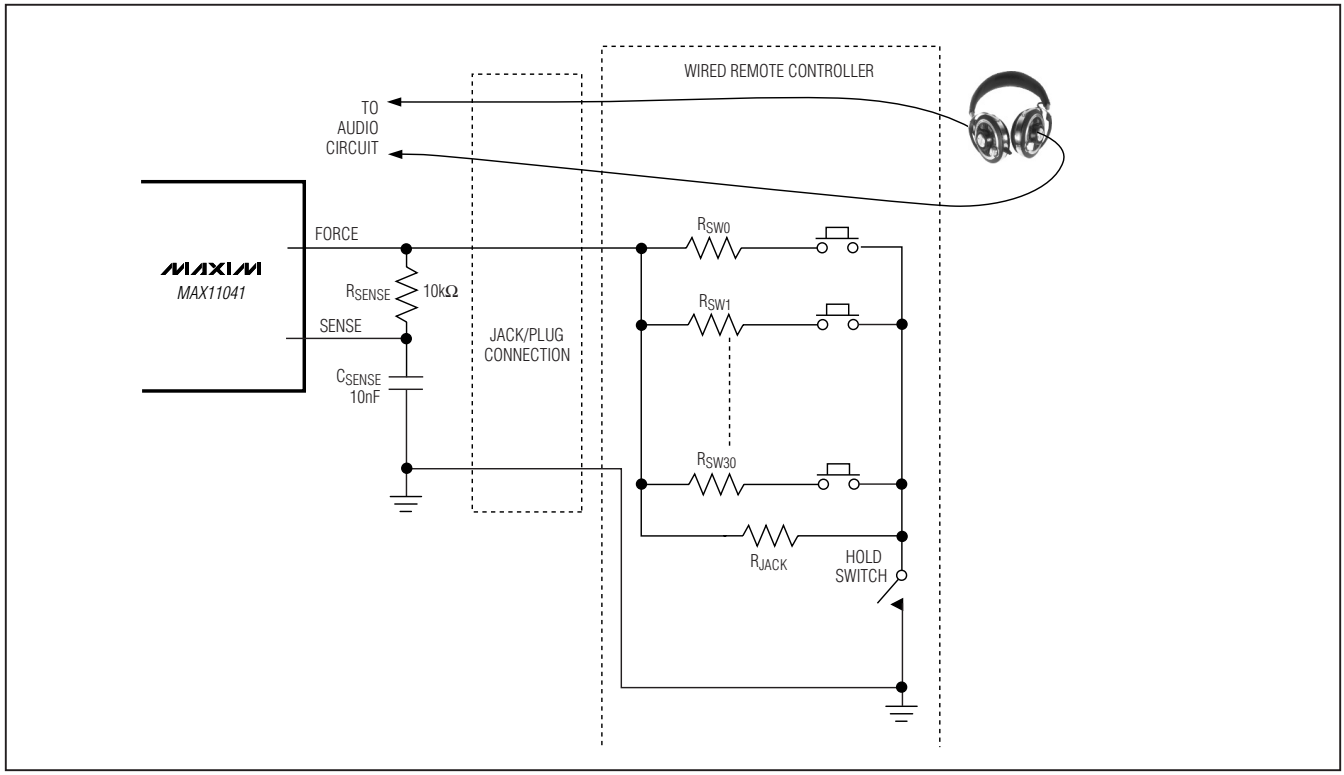


Figure 2. Recommended FORCE and SENSE Configuration

Table 1. Control Register

BITS	READ/WRITE	POWER-UP STATE	DESCRIPTION
C7	R/$\overline{W}$	1	0 = FORCE is high-impedance 1 = FORCE is not high-impedance (normal operation)
C6	R/$\overline{W}$	0	0 = Normal operation 1 = Power-down state, full reset
C5	R	1	1 = FIFO is empty 0 = FIFO is not empty
C4–C0	—	Not used	Reading/writing has no effect

Table 2. FIFO Data Format

FIFO DATA	BIT NAMES							
Keypress type (MAX11041)	K7	K6	K5	K4	K3	K2	K1	K0
Keypress duration	OF	T6	T5	T4	T3	T2	T1	T0

X = Don't care.

Table 3. Chip ID Data Format

CHIP ID	BIT NAMES							
	I7	I6	I5	I4	I3	I2	I1	I0
MAX11041	0	0	0	0	0	0	0	0

Keypress Detection and Debounce

At power-up, the MAX11041 begins to monitor the SENSE input for keypresses. When the MAX11041 detects a keypress at SENSE, it attempts to debounce the SENSE input. After successful debouncing of the input, the corresponding keypress result is inserted into the FIFO. In addition, $\overline{INT}$ goes low to signal a keypress to the µP.

Keypress FIFO and Time Duration

After detecting and debouncing a key, the decoded key is stored in one byte of the 8-word FIFO. A 7-bit internal timer starts counting the duration of the keypress (one count = 32ms) and the result is stored after each increment in another byte of the 8-word FIFO. The 8th bit in the time duration byte is an overflow bit that is set when the count reaches 128. After the count reaches 128, the 7-bit timer rolls over to 0 and continues to count while the 8th bit becomes set and stays set until the associated FIFO entry is cleared. For keypress durations longer than 8.16s, see the *Extended Keypresses* section.

When the device detects another change in resistance at SENSE (either by key release or another keypress), the count resets and the FIFO begin recording the next keypress/duration. This allows the 8-word FIFO to store time duration and key-type information for up to four keypresses and releases. When the FIFO is full and a key is pressed, the oldest keypress information in the FIFO is written over. Writing to the power-down bit (bit 6) in the control register or bringing $\overline{SHDN}$ low clears the FIFO to its power-on-reset (POR) state.

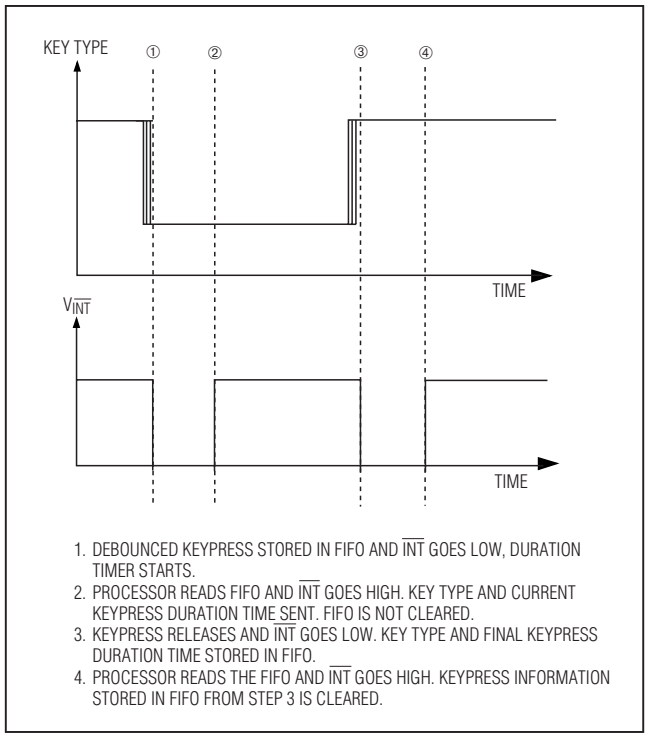


Figure 3. Reading the FIFO While the Key is Still Pressed

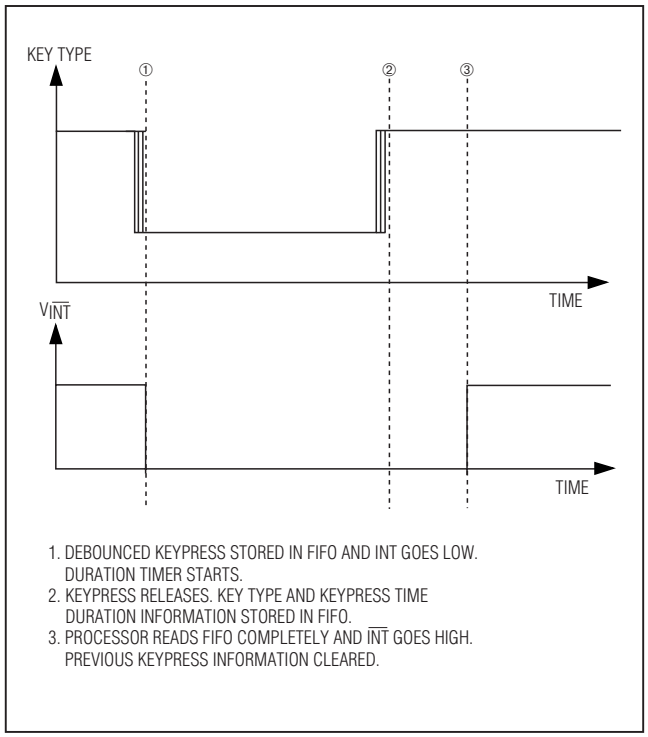


Figure 4. Reading the FIFO After the Key is Released

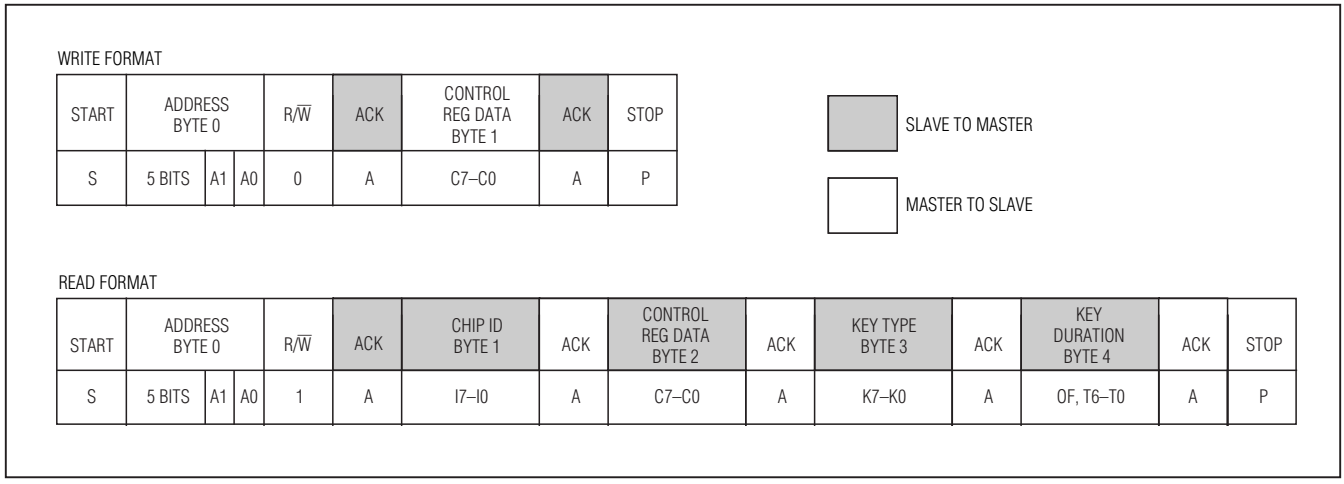


Figure 5. Read/Write Formats

Reading the FIFO While the Key is Still Pressed

When a valid keypress occurs, $\overline{INT}$ goes low, signaling to the processor that a key has been pressed (see Figure 3). If the processor reads the FIFO while the key is still pressed, the key type and current duration of the keypress is sent. The current keypress information in the FIFO is not cleared after a read operation if the key is still pressed. In addition, after a read operation, if the key is still pressed, $\overline{INT}$ goes high again until the device detects another keypress/release, freeing the processor from polling. Conversely, if the processor chooses to poll the duration of the keypress, $\overline{INT}$ stays high at this time no matter how many times the processor reads the FIFO. When $\overline{INT}$ goes low again (from another keypress/release), key type and final time duration of the keypress is available in the FIFO. When the FIFO is read after the key release, the information from that keypress is cleared and $\overline{INT}$ goes high again.

Reading the FIFO After the Key has Released

When a valid keypress occurs, $\overline{INT}$ goes low, signaling to the processor that a key has been pressed (see Figure 4). If the processor reads the FIFO after the key has already been released (or an additional key was pressed), the key type and final duration time of that keypress is sent. In addition, the information from the keypress is cleared and $\overline{INT}$ goes high again.

Digital Serial Interface

The MAX11041 contains an I^2C-compatible interface for data communication with a host processor (SCL and SDA). The interface supports a clock frequency up to 400kHz. SCL and SDA require pullup resistors that are connected to a positive supply. Figure 5 details the read and write formats.

Write Format

The only write to the MAX11041 that is possible is to the control register (C7–C0). Use the following sequence to write to the control register (see Figure 5):

1) After generating a START condition (S), address the MAX11041 by sending the appropriate slave address byte with its corresponding R/$\overline{W}$ bit set to a 0 (see the *Slave Address and* R/$\overline{W}$ *Bit* section). The MAX11041 answers with an ACK bit (see the *Acknowledge Bits* section).
2) Send the appropriate data bytes to program the control register (C7–C0). The MAX11041 answers with an ACK bit.
3) Generate a STOP condition (P).

Read Format

To read the control register and key type/duration stored in FIFO, use the following sequence (see Figure 5):

1) After generating a START condition (S), address the MAX11041 by sending the appropriate slave address byte with its corresponding R/$\overline{W}$ bit set to a 1 (see the *Slave Address and* R/$\overline{W}$ *Bit* section). The MAX11041 answers with an ACK bit (see the *Acknowledge Bits* section).
2) The MAX11041 sends the 8-bit chip ID I7–I0. Afterwards, the master must send an ACK bit.
3) The MAX11041 sends the contents of the control register (C7–C0) starting with the most significant bit. Afterwards, the master must send an ACK bit.

Wired Remote Controller

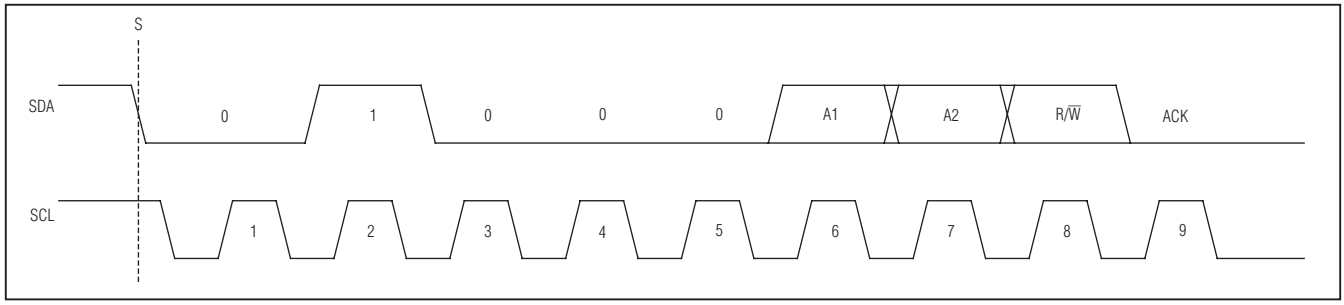


Figure 6. Slave Address and R/$\overline{W}$ Bit

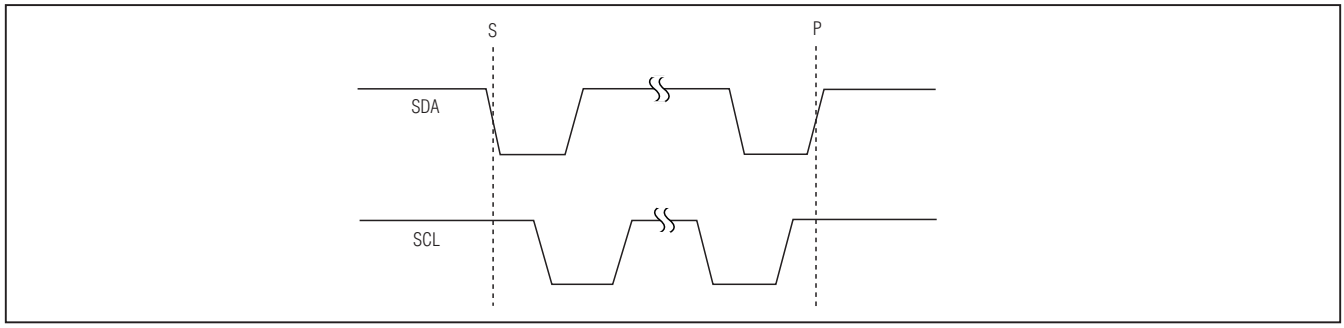


Figure 7. START and STOP Conditions

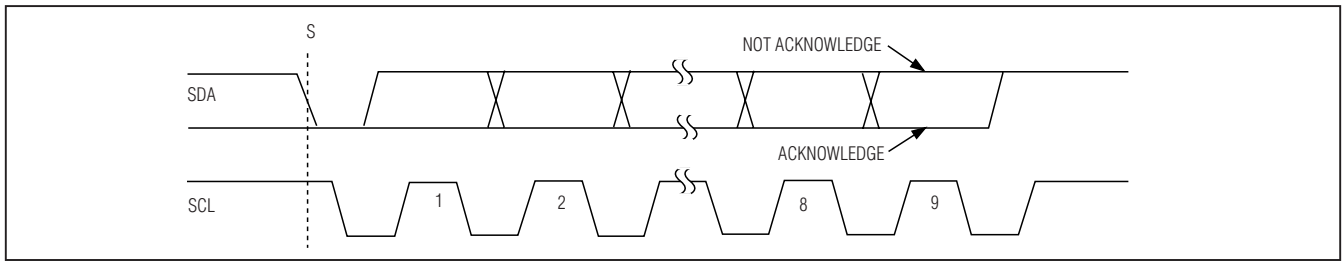


Figure 8. Acknowledge Bits

4) The MAX11041 sends the latest keypress type (K7–K0) stored in the FIFO starting with the most-significant bit. Afterwards the master must send an ACK bit.
5) The MAX11041 sends the corresponding keypress time duration (OF, T6–T0) stored in the FIFO starting with the most significant bit (OF). Afterwards the master must send an ACK bit.
6) The master must generate a STOP condition.

Slave Address and R/$\overline{W}$ Bit

The MAX11041 includes a 7-bit slave address. The first 5 bits (MSBs) of the slave address are factory-programmed and always 01000. The logic state of the address inputs (A1 and A0) determine the last two LSBs of the device address (see Figure 6). Connect A1 and A0 to V_{DD} (logic high) or GND (logic low). A maximum of four MAX11041 devices can be connected on the same bus at one time using these address inputs. The 8th bit of the address byte is a read/write bit (R/$\overline{W}$). If this bit is set to 0, the device expects to receive data. If this bit is set to 1, the device expects to send data.

Table 4. Required Resistor Set for the MAX11041

KEY	STANDARD 1% RESISTOR VALUE (Ω)	FIFO RESISTOR CODE*		FUNCTION
		LOWEST	HIGHEST	
0	0	0	1	Function 0
1	1470	11	13	Function 1
2	2550	19	21	Function 2
3	3740	27	30	Function 3
4	4990	35	38	Function 4
5	6340	42	46	Function 5
6	7680	50	53	Function 6
7	9310	58	62	Function 7
8	11000	66	70	Function 8
9	13000	74	78	Function 9
10	15000	82	86	Function 10
11	17400	90	94	Function 11
12	20000	98	102	Function 12
13	22600	105	110	Function 13
14	26100	114	119	Function 14
15	30100	123	127	Function 15
16	34000	130	135	Function 16
17	38300	137	142	Function 17
18	44200	146	150	Function 18
19	51100	154	159	Function 19
20	59000	162	166	Function 20
21	68100	170	174	Function 21
22	80600	178	182	Function 22
23	95300	186	190	Function 23
24	118000	194	198	Function 24
25	147000	202	206	Function 25
26	191000	211	214	Function 26
27	261000	218	222	Function 27
28	402000	226	229	Function 28
29	825000	235	237	Function 29
Jack inserted	619000	243	245	Jack inserted
Jack removed	∞	254	255	Jack removed

**Values outside FIFO resistor code are considered invalid.*

Bit Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the *START and STOP Conditions* section). Both SDA and SCL remain high when the bus is not active.

START and STOP Conditions

The master initiates a transmission with a START condition, a high-to-low transition on SDA while SCL is high. The master terminates a transmission with a STOP condition, a low-to-high transition on SDA while SCL is high (see Figure 7).

Acknowledge Bits

Data transfers are acknowledged with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX11041 generates ACK bits. To generate an ACK, pull SDA low before the rising edge of the ninth clock pulse and keep it low during the high period of the ninth clock pulse (see Figure 8). To generate a NACK, leave SDA high before the rising edge of the ninth clock pulse and keep it high for the duration of the ninth clock pulse. Monitoring NACK bits allows for detection of unsuccessful data transfers. The master can also use NACK bits to interrupt the current data transfer to start another data transfer. If the master uses NACK during a read from the FIFO, the FIFO word pointer is not incremented and the next FIFO read produces the same FIFO word. Thus, the master must provide the ACK bit to advance the FIFO word pointer.

Applications Information

Required Resistor Set

Table 4 shows the required resistor set for 30 key implementations. Resistors must have a 1% tolerance.

Jack Insertion/Removal Detection

During jack insertion there may be several false key entries written to the FIFO. When a jack insertion/removal is detected, it is necessary to read the FIFO repeatedly until the final change in jack state is located (see Figure 9).

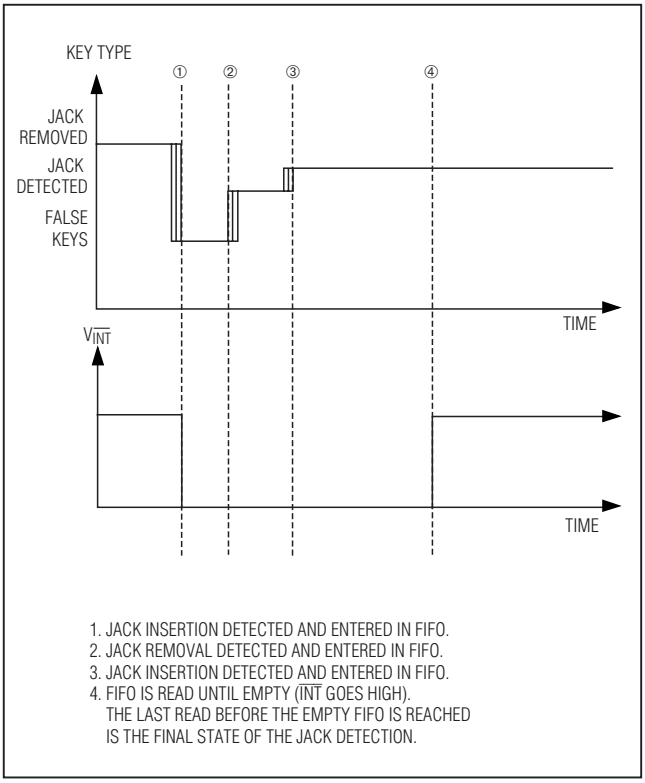


Figure 9. Jack Insertion Detection

Extended Keypresses

In certain applications, a key triggers different events depending on the duration of the keypress, simultaneous keypresses, or a specific order of keypresses.

Long Keypress Detection

In some applications, the duration of the keypress determines the event triggered. For example, TALK dials the entered phone number normally and initiates voice dialing if it is held down. A second common use of holding a key down is to generate a continuous stream of events, such as the volume control or fast forward.

Simultaneous Keypress Detection

Certain applications require the detection of simultaneous keypresses, such as <SHIFT+KEY> and <FUNCTION+KEY> combinations. This is done in software. For instance, the µP detects the SHIFT key is being pressed. When the µP detects an additional keypress instead of a key release, it knows the corresponding code is a result of two resistors in parallel.

Order of Keypress Detection

Some applications require detection of the specific sequence of keys in software by looking for unique key presses within 32 ticks (1s). If the duration between keypresses exceeds the allowed time, assume the keypress is in error and return to the previous known state.

Power-Up Jack Detect and Keypress Example

Figure 10 illustrates the FIFO entries during a typical sequence of events.

Layout, Grounding, and Bypassing

Position R_{SENSE} and C_{SENSE} as close to the device as possible. Bypass V_{DD} with a 0.1µF capacitor to GND as close to the device as possible. Connect GND to a quiet analog ground plane. Route digital lines away from SENSE and FORCE.

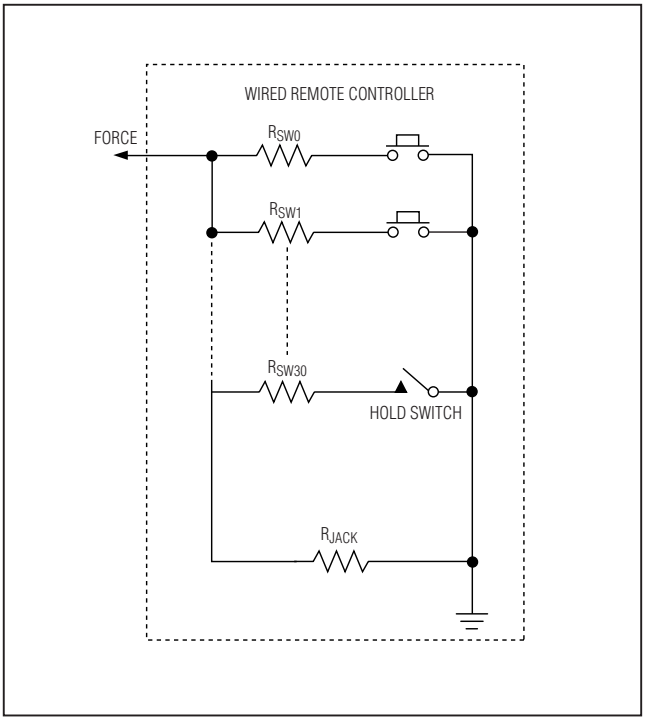


Figure 10. Software Implemented Hold-Switch Configuration

Wired Remote Controller

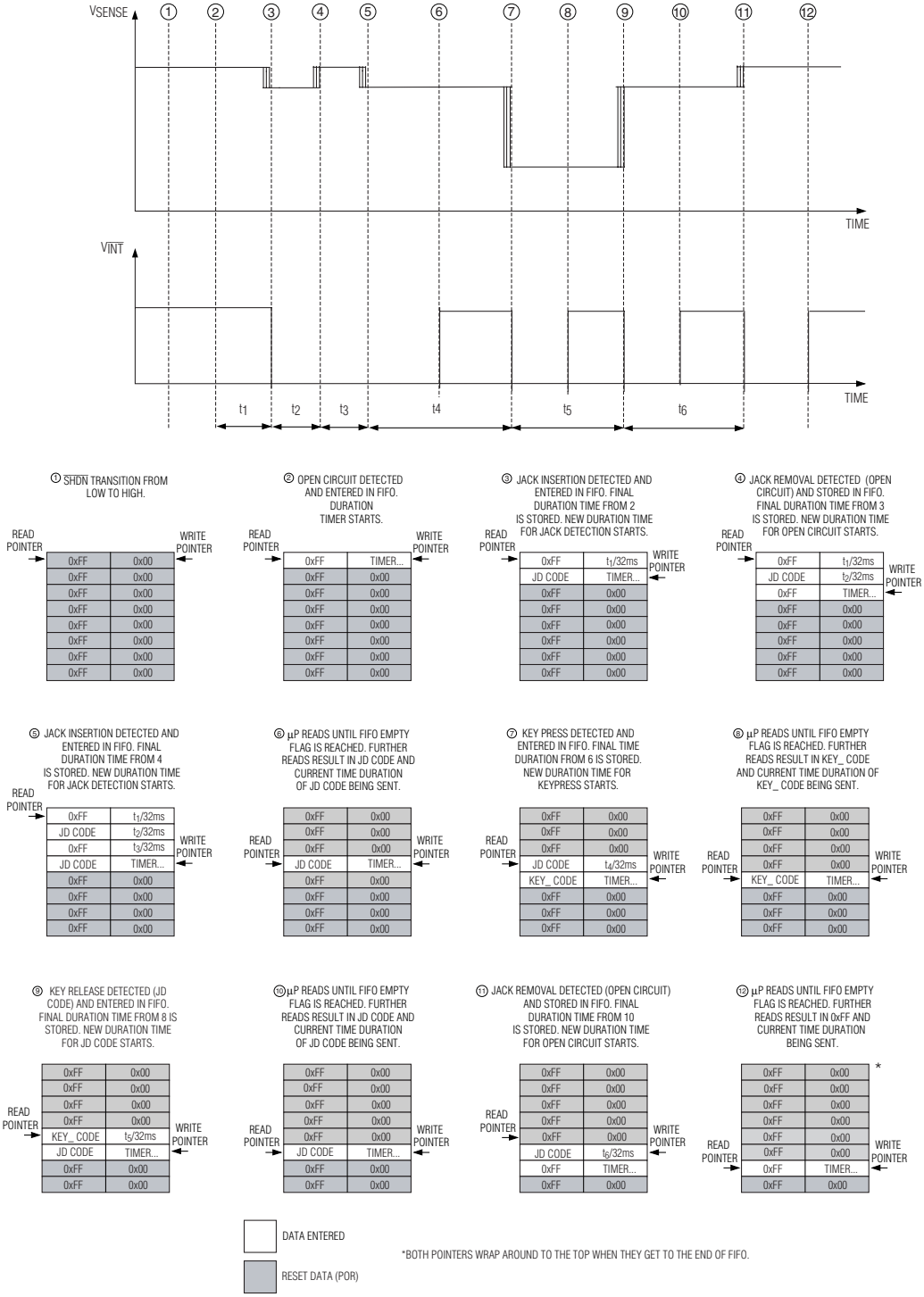
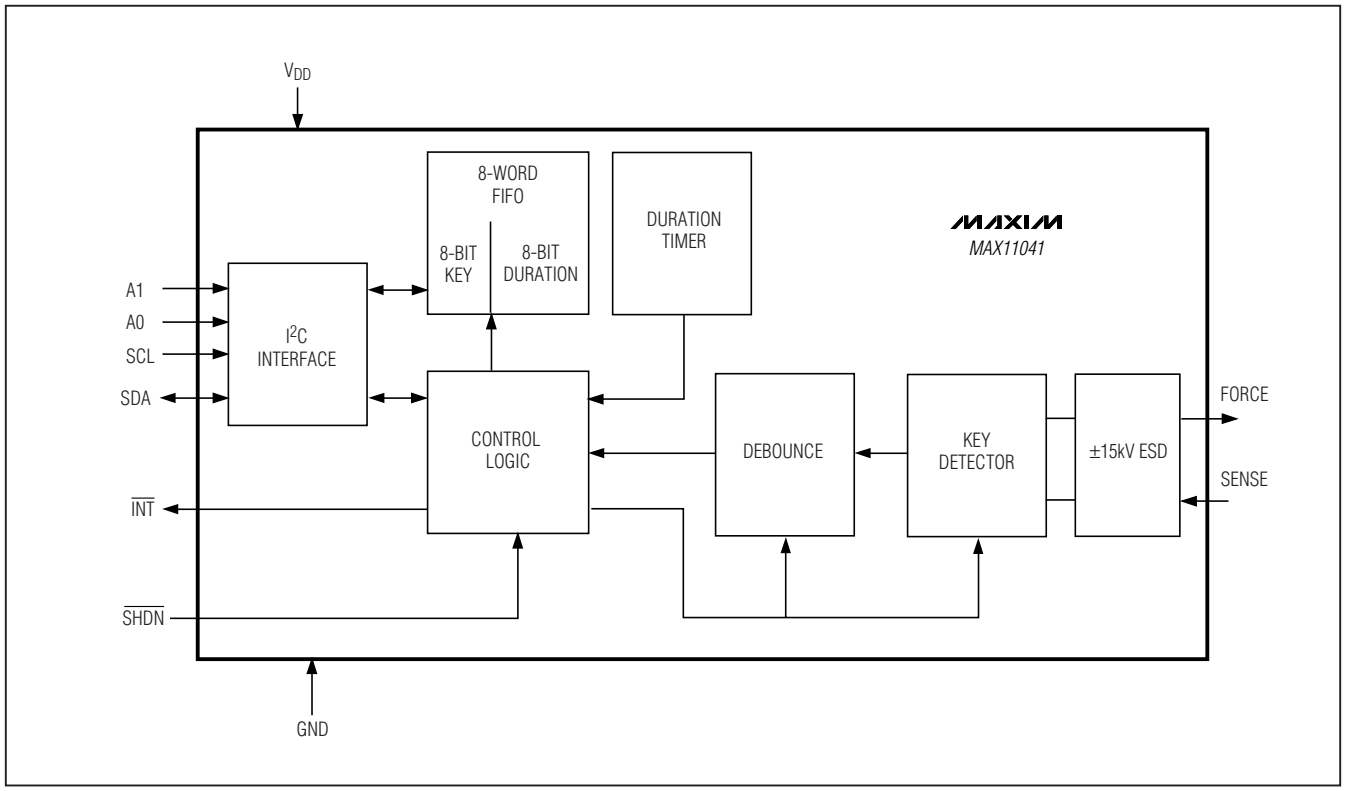


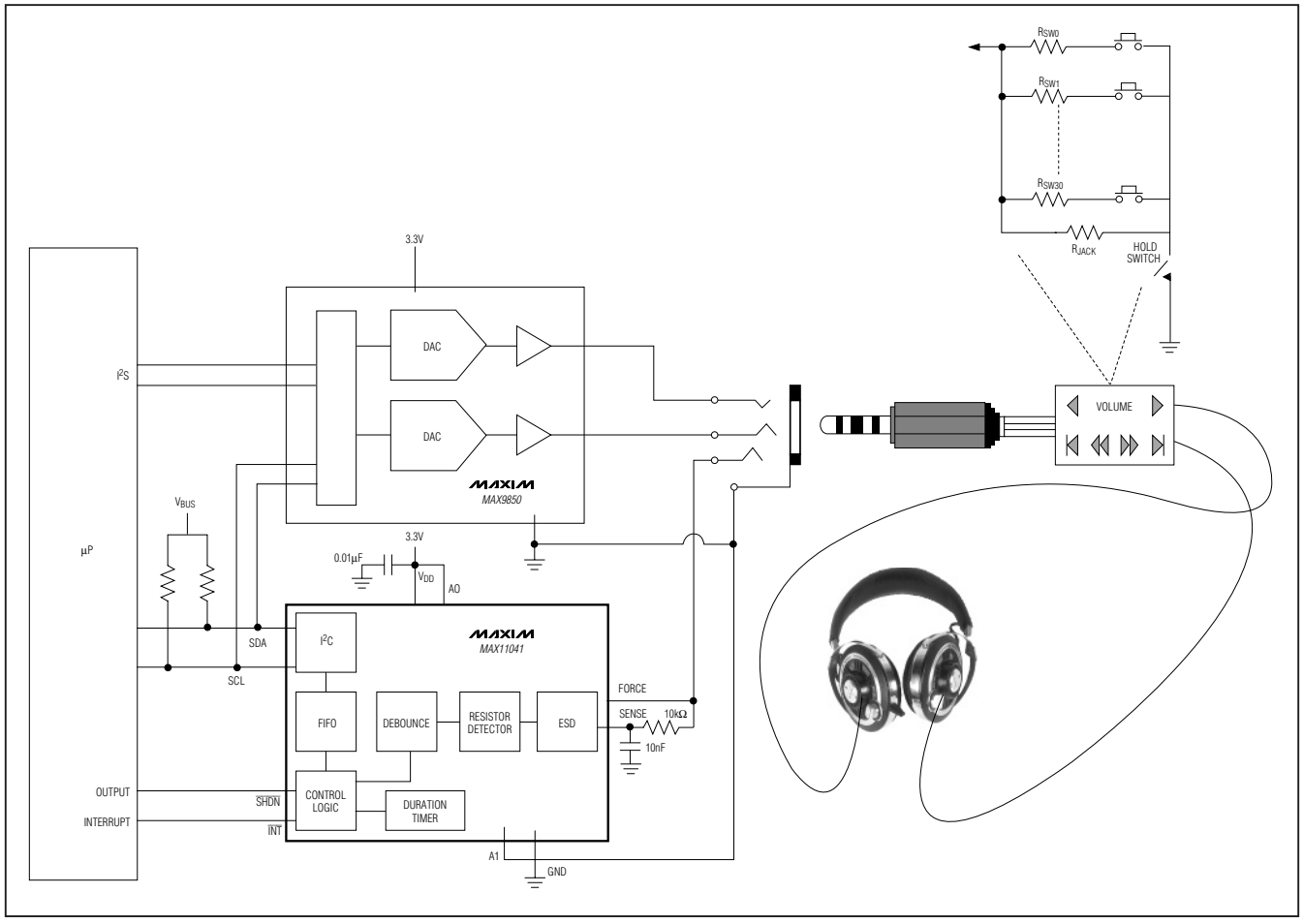
Figure 10. Power-Up, Jack Detect, and Keypress Example

Functional Diagram



Wired Remote Controller

Typical Operating Circuit



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
12 TQFN-EP	T1244+4	**21-0139**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
1	8/07	Removed leaded package types	—
2	11/08	Changed *FIFO Data Format* table	7
3	1/10	Removed the MAX11042 from the data sheet	1–17

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