

MAX11205PMB1 Peripheral Module

General Description

The MAX11205PMB1 peripheral module provides the necessary hardware to interface the MAX11205 16-bit ADC to any system that utilizes Pmod™-compatible expansion ports configurable for GPIO interface. The IC is an ultra-low-power (< 300µA max active current), high-resolution, serial-output ADC. This device provides the highest resolution per unit power in the industry and is optimized for applications that require very high dynamic range with low power, such as sensors on a 4mA to 20mA industrial control loop. The voltage reference for the IC is supplied by a MAX6037 (2.5V) that is also on the module. The filtered power-supply voltage from the host can be optionally passed (jumper selectable) through a MAX8510 ultra-low-noise LDO, allowing empirical evaluation of performance with different power sources.

Refer to the MAX11205 IC data sheet for detailed information regarding operation of the IC.

Features

- ◆ 16-Bit Full-Scale Resolution
- ◆ Internal System Clock
- ◆ 2-Wire Serial Interface
- ◆ On-Board Voltage Reference (MAX6037, 2.5V Version)
- ◆ Filtered Power Supply with Optional (Jumper-Selectable) Ultra-Low Noise LDO
- ◆ 6-Pin Pmod-Compatible Connector (GPIO)
- ◆ Example Software Written in C for Portability
- ◆ RoHS Compliant
- ◆ Proven PCB Layout
- ◆ Fully Assembled and Tested

[Ordering Information](#) appears at end of data sheet.

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Component List

DESIGNATION	QTY	DESCRIPTION
C1–C5	5	0.1µF ±10%, 16V X7R ceramic capacitors (0603) Murata GRM188R71C104KA01D
C6	1	10µF ±10%, 10V X5R ceramic capacitor (0603) TDK C2012X5R1A106K/1.25
C7, C8	2	0.01µF ±10%, 16V X7R ceramic capacitors (0603) Murata GRM188R71C103KA01D
C9, C10	2	2.2µF ±10%, 10V X5R ceramic capacitors (0603) TDK C1608X5R1A225K/0.80
F1	1	4.7µF EMI filter (3-terminal capacitor) Murata NFM21PC475B1A3D

DESIGNATION	QTY	DESCRIPTION
J1	1	6-pin right-angle male header
JP1	1	3-pin straight male header
R1, R2	2	150Ω ±5% resistors (0603)
R3, R4, R5	3	33Ω ±5% resistors (0603)
U1	1	Ultra-low-noise, high-PSRR linear regulator (5 SC70) Maxim MAX8510EXK29+
U2	1	16-bit delta-sigma ADC (10 µMAX®) Maxim MAX11205AEUB+
U3	1	Low-power fixed reference (5 SOT23) Maxim MAX6037AAUK25+
—	1	Shorting jumper
—	1	PCB: EPCB11205PM1

Component Suppliers

SUPPLIER	PHONE	WEBSITE
Murata Electronics North America, Inc.	770-436-1300	www.murata-northamerica.com
TDK Corp.	847-803-6100	www.component.tdk.com

Note: Indicate that you are using the MAX11205PMB1 when contacting these component suppliers.

Detailed Description

2-Wire Interface

The MAX11205PMB1 peripheral module interfaces with a host using a 2-wire serial interface. When an ADC conversion is complete, the IC pulls the data line low. The host must then supply a clock signal to shift out the conversion data. More information on the 2-wire interface can be found in the MAX11205 IC data sheet.

Connector J1 provides connection of the module to the Pmod host. See Table 1.

Jumper JP1 allows the user to select between two voltages for IC analog supply voltage (AVDD). This allows the option of applying additional power-supply filtering based on the noise content of the incoming voltage source (connector J1) and the performance requirements for the application. See Table 2.

Table 1. Connector J1 (2-Wire Communication)

PIN	SIGNAL	DESCRIPTION
1	N.C.	Not connected
2	N.C.	Not connected
3	MISO	Data-ready output/serial-data output. This output serves a dual function. In addition to the serial-data output function, the MISO pin also indicates that the data is ready when it is pulled logic-low by the IC. Output data changes on the falling edge of SCLK.
4	SCK	2-wire serial clock. The host must apply an external clock signal to shift data out from the IC.
5	GND	Ground
6	VCC	Power supply

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**Table 2. Jumper JP1
(Analog VDD Selection)**

PINS	SELECTION
2-1	AVDD supplied by output from MAX8510EXK29 (2.85V)
2-3	AVDD supplied by host, pin 6 of connector J1

Reference Voltage

The peripheral module contains a MAX6037 precision voltage reference for the REFP input of the ADC IC. The MAX6037 outputs a 2.5V reference.

Software and FPGA Code

Example software and drivers are available that execute directly without modification on several FPGA development boards that support an integrated or synthesized microprocessor. These boards include the Digilent Nexys 3, Avnet LX9, and Avnet ZEDBoard, although other plat-

forms can be added over time. Maxim provides complete Xilinx ISE projects containing HDL, Platform Studio, and SDK projects. In addition, a synthesized bitstream, ready for FPGA download, is provided for the demonstration application.

The software project (for the SDK) contains several source files intended to accelerate customer evaluation and design. These include a base application (maximModules.c) that demonstrates module functionality and uses an API interface (maximDeviceSpecificUtilities.c) to set and access Maxim device functions within a specific module.

The source code is written in standard ANSI C format, and all API documentation including theory/operation, register description, and function prototypes are documented in the API interface file (maximDeviceSpecificUtilities.h & .c).

The complete software kit is available for download at www.maxim-ic.com. Quick start instructions are also available as a separate document.

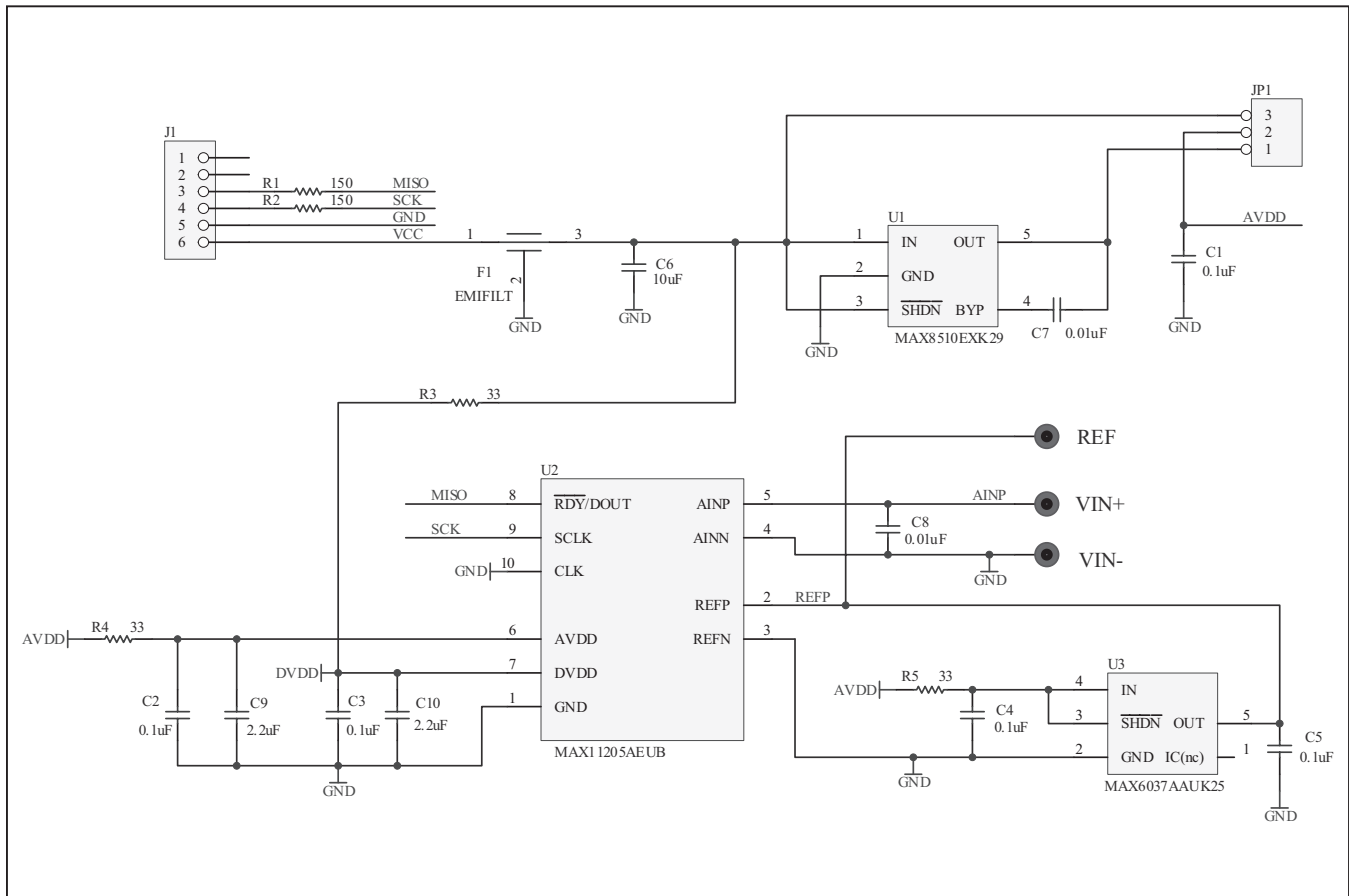


Figure 1. MAX11205PMB1 Peripheral Module Schematic

MAX11205PMB1 Peripheral Module

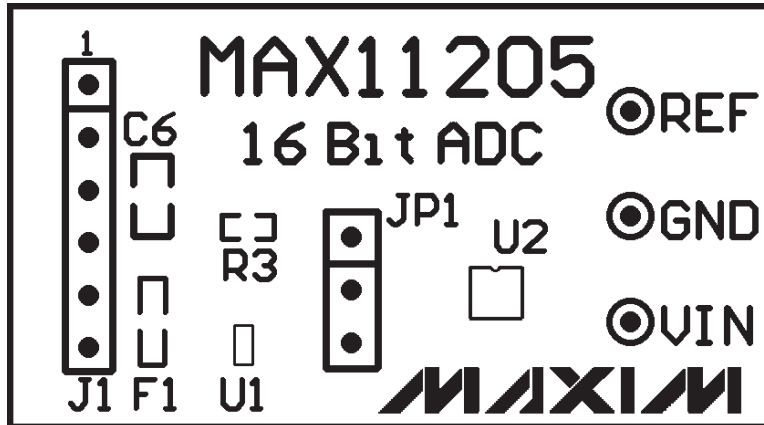


Figure 2. MAX11205PMB1 Peripheral Module Component Placement Guide—Component Side

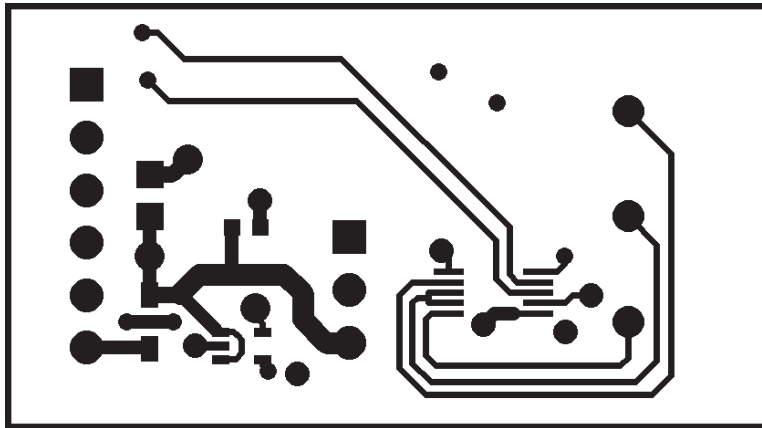


Figure 3. MAX11205PMB1 Peripheral Module PCB Layout—Component Side

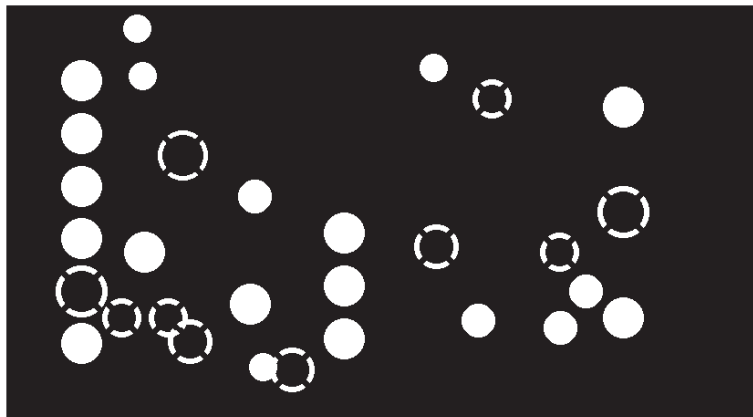


Figure 4. MAX11205PMB1 Peripheral Module PCB Layout—Inner Layer 1 (Ground)

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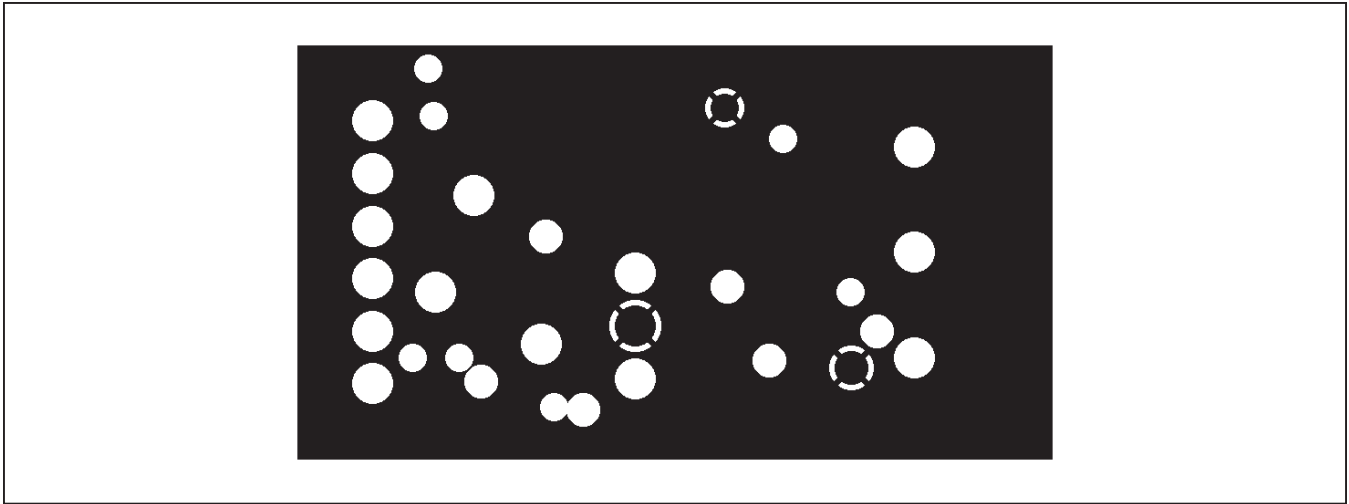


Figure 5. MAX11205PMB1 Peripheral Module PCB Layout—Inner Layer 2 (Power)

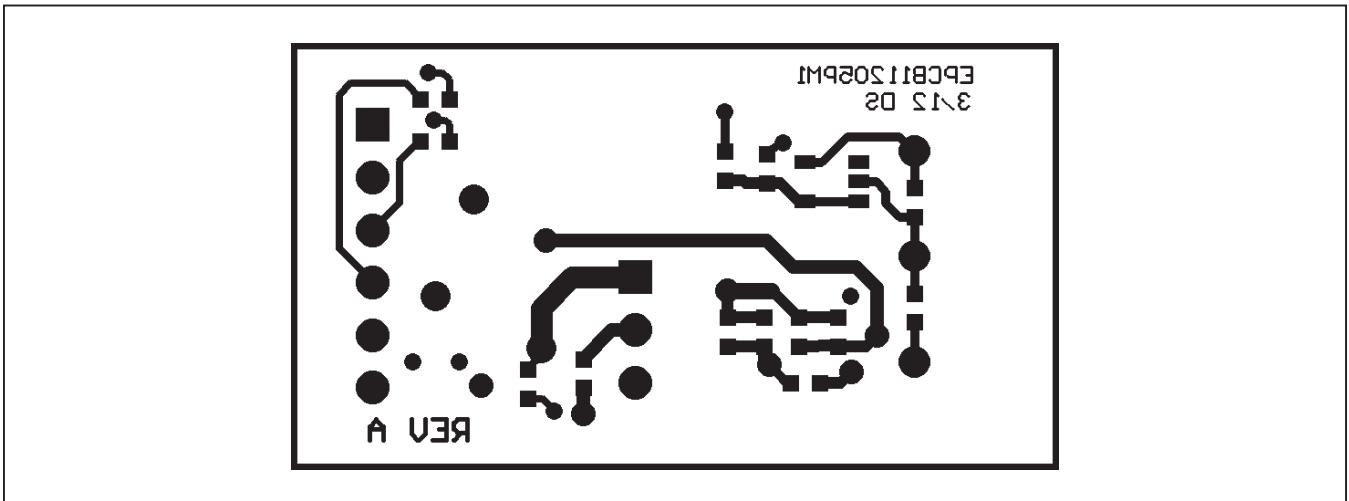


Figure 6. MAX11205PMB1 Peripheral Module PCB Layout—Solder Side

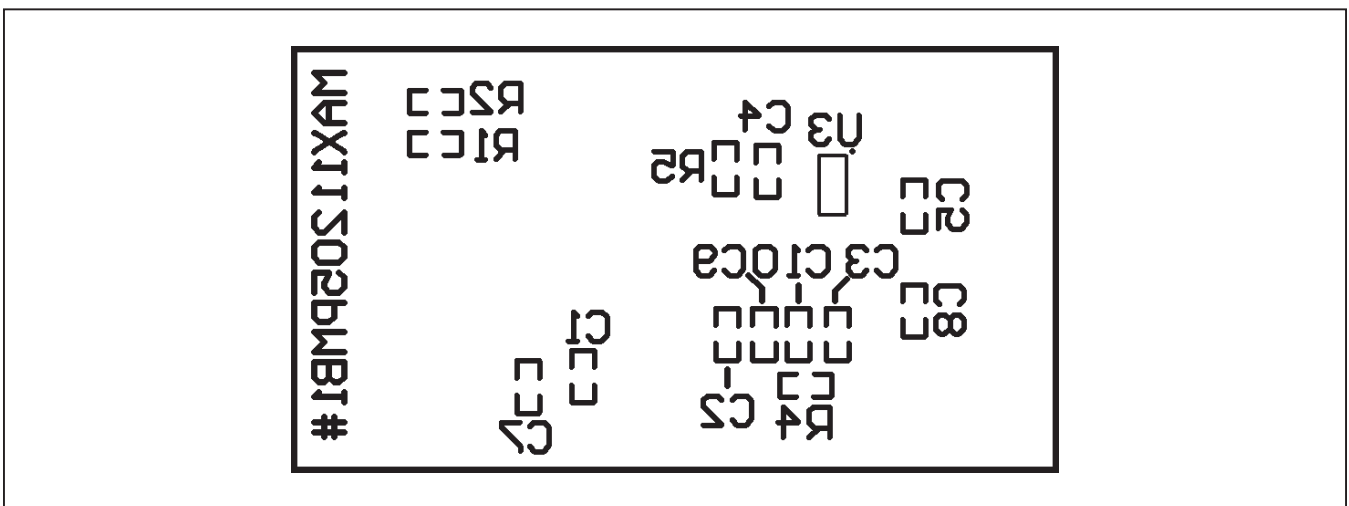


Figure 7. MAX11205PMB1 Peripheral Module Component Placement Guide—Solder Side

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Ordering Information

PART	TYPE
MAX11205PMB1#	Peripheral Module

#Denotes RoHS compliant.

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/12	Initial release	—

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