19-5961; Rev 1; 9/11

10-Bit, 300ksps ADCs with FIFO and Internal Reference

General Description

The MAX11618–MAX11621/MAX11624/MAX11625 are serial 10-bit analog-to-digital converters (ADCs) with an internal reference. These devices feature on-chip FIFO, scan mode, internal clock mode, internal averaging, and AutoShutdown™. The maximum sampling rate is 300ksps using an external clock. The MAX11624/MAX11625 have 16 input channels, the MAX11620/MAX11621 have 8 input channels, and the MAX11618/MAX11619 have 4 input channels. These six devices operate from either a +3V supply or a +5V supply, and contain a 10MHz SPI™-/QSPI™-/MICROWIRE™-compatible serial port.

The MAX11618–MAX11621 are available in 16-pin QSOP packages. The MAX11624/MAX11625 are available in 24-pin QSOP packages. All six devices are specified over the extended -40°C to +85°C temperature range.

Applications

System Supervision

Data-Acquisition Systems

Industrial Control Systems

Patient Monitoring

Data Logging

Instrumentation

Features

- **Analog Multiplexer with Track/Hold**
  - **16 Channels (MAX11624/MAX11625)**
  - **8 Channels (MAX11620/MAX11621)**
  - **4 Channels (MAX11618/MAX11619)**
- **Single Supply**
  - **2.7V to 3.6V (MAX11619/MAX11621/MAX11625)**
  - **4.75V to 5.25V (MAX11618/MAX11620/MAX11624)**
- **Internal Reference**
  - **2.5V (MAX11619/MAX11621/MAX11625)**
  - **4.096V (MAX11618/MAX11620/MAX11624)**
- **External Reference: 1V to V_{DD}**
- **16-Entry First-In/First-Out (FIFO)**
- **Scan Mode, Internal Averaging, and Internal Clock**
- **Accuracy: ±1 LSB INL, ±1 LSB DNL, No Missing Codes Over Temperature**
- **10MHz 3-Wire SPI-/QSPI-/MICROWIRE-Compatible Interface**
- **Small Packages**
  - **16-Pin QSOP (MAX11618–MAX11621)**
  - **24-Pin QSOP (MAX11624/MAX11625)**

Ordering Information

PART	NUMBER OF INPUTS	SUPPLY VOLTAGE RANGE (V)	PIN-PACKAGE
MAX11618EEE+T	4	4.75 to 5.25	16 QSOP
MAX11619EEE+T	4	2.7 to 3.6	16 QSOP
MAX11620EEE+T	8	4.75 to 5.25	16 QSOP
MAX11621EEE+T	8	2.7 to 3.6	16 QSOP
MAX11624EEG+T	16	4.75 to 5.25	24 QSOP
MAX11625EEG+T	16	2.7 to 3.6	24 QSOP

Note: *All devices are specified over the -40°C to +85°C operating temperature range.*
+Denotes a lead(Pb)-free/RoHS-compliant package.

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ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ....-0.3V to +6V
$\overline{CS}$, SCLK, DIN, $\overline{EOC}$, DOUT to GND.........-0.3V to (V_{DD} + 0.3V)
AIN0–AIN14, $\overline{CNVST}$/AIN_,
REF to GND..-0.3V to (V_{DD} + 0.3V)
Maximum Current into Any Pin...50mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8.3mW/°C above +70°C)...........667mW
24-Pin QSOP (derate 9.5mW/°C above +70°C)...........762mW

Operating Temperature Range ....-40°C to +85°C
Storage Temperature Range ....-60°C to +150°C
Junction Temperature ....+150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

16 QSOP
Junction-to-Ambient Thermal Resistance (θ_{JA})...............105°C/W
Junction-to-Case Thermal Resistance (θ_{JC})......................37°C/W

24 QSOP
Junction-to-Ambient Thermal Resistance (θ_{JA})................88°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).......................34°C/W

Note 1: Package thermal resistances were obtained usiˇng the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V to 3.6V (MAX11619/MAX11621/MAX11625); V_{DD} = 4.75V to 5.25V (MAX11618/MAX11620/MAX11624), f_{SAMPLE} = 300kHz, f_{SCLK} = 4.8MHz (external clock, 50% duty cycle), V_{REF} = 2.5V (MAX11619//MAX11621/MAX11625); V_{REF} = 4.096V (MAX11618/MAX11620/MAX11624), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 3)						
Resolution	RES		10			Bits
Integral Nonlinearity	INL				±1.0	LSB
Differential Nonlinearity	DNL	No missing codes over temperature			±1.0	LSB
Offset Error				±0.5	±2.0	LSB
Gain Error		(Note 4)		±0.5	±2.0	LSB
Offset Error Temperature Coefficient				±2		ppm/°C FSR
Gain Temperature Coefficient				±0.8		ppm/°C
Channel-to-Channel Offset Matching				±0.1		LSB
DYNAMIC SPECIFICATIONS (30kHz sine-wave input, 300ksps, f_{SCLK} = 4.8MHz)						
Signal-to-Noise Plus Distortion	SINAD			62		dB
Total Harmonic Distortion	THD	Up to the 5th harmonic		-79		dBc
Spurious-Free Dynamic Range	SFDR			-81		dBc
Intermodulation Distortion	IMD	f_{IN1} = 29.9kHz, f_{IN2} = 30.1kHz		-74		dBc
Full-Power Bandwidth		-3dB point		1		MHz
Full-Linear Bandwidth		S/(N + D) > 61dB		100		kHz

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 3.6V (MAX11619/MAX11621/MAX11625); V_{DD} = 4.75V to 5.25V (MAX11618/MAX11620/MAX11624), f_{SAMPLE} = 300kHz, f_{SCLK} = 4.8MHz (external clock, 50% duty cycle), V_{REF} = 2.5V (MAX11619//MAX11621/MAX11625); V_{REF} = 4.096V (MAX11618/MAX11620/MAX11624), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONVERSION RATE						
Power-Up Time	t_{PU}	External reference		0.8		µs
		Internal reference (Note 5)		65		
Acquisition Time	t_{ACQ}		0.6			µs
Conversion Time	t_{CONV}	Internally clocked		3.5		µs
		Externally clocked (Note 6)	2.7			
External Clock Frequency	f_{SCLK}	Externally clocked conversion	0.1		4.8	MHz
		Data I/O			10	
Aperture Delay				30		ns
Aperture Jitter				< 50		ps
ANALOG INPUT						
Input Voltage Range		Unipolar	0		V_{REF}	V
Input Leakage Current		V_{IN} = V_{DD}		±0.01	±1	µA
Input Capacitance		During acquisition time (Note 7)		24		pF
INTERNAL REFERENCE						
REF Output Voltage		MAX11618/MAX11620/MAX11624	4.024	4.096	4.168	V
		MAX11619/MAX11621/MAX11625	2.48	2.50	2.52	
REF Temperature Coefficient	TC_{REF}	MAX11618/MAX11620/MAX11624		±20		ppm/°C
		MAX11619/MAX11621/MAX11625		±30		
Output Resistance				6.5		kΩ
REF Output Noise				200		$µV_{RMS}$
REF Power-Supply Rejection	PSRR			-70		dB
EXTERNAL REFERENCE						
REF Input Voltage Range	V_{REF}		1.0		V_{DD} + 50mV	V
REF Input Current	I_{REF}	V_{REF} = 2.5V (MAX11619/MAX11621/ MAX11625); V_{REF} = 4.096V (MAX11618/MAX11620/MAX11624), f_{SAMPLE} = 300ksps		40	100	µA
		V_{REF} = 2.5V (MAX11619/MAX11621/ MAX11625); V_{REF} = 4.096V (MAX11618/MAX11620/MAX11624), f_{SAMPLE} = 0		±0.1	±5	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 3.6V (MAX11619/MAX11621/MAX11625); V_{DD} = 4.75V to 5.25V (MAX11618/MAX11620/MAX11624), f_{SAMPLE} = 300kHz, f_{SCLK} = 4.8MHz (external clock, 50% duty cycle), V_{REF} = 2.5V (MAX11619//MAX11621/MAX11625); V_{REF} = 4.096V (MAX11618/MAX11620/MAX11624), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$, $\overline{CNVST}$) (Note 8)							
Input-Voltage Low	V_{IL}	MAX11618/MAX11620/MAX11624				0.8	V
		MAX11619/MAX11621/MAX11625				V_{DD} x 0.3	
Input-Voltage High	V_{IH}	MAX11618/MAX11620/MAX11624		2.0			V
		MAX11619/MAX11621/MAX11625		V_{DD} x 0.7			
Input Hysteresis	V_{HYST}				200		mV
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}			±0.01	±1.0	µA
Input Capacitance	C_{IN}				15		pF
DIGITAL OUTPUTS (DOUT, $\overline{EOC}$)							
Output-Voltage Low	V_{OL}	I_{SINK} = 2mA				0.4	V
		I_{SINK} = 4mA				0.8	
Output-Voltage High	V_{OH}	I_{SOURCE} = 1.5mA		V_{DD} - 0.5			V
Three-State Leakage Current	I_L	$\overline{CS}$ = V_{DD}			±0.05	±1	µA
Three-State Output	C_{OUT}	$\overline{CS}$ = V_{DD}			15		pF
POWER REQUIREMENTS							
Supply Voltage	V_{DD}	MAX11618/MAX11620/MAX11624		4.75		5.25	V
		MAX11619/MAX11621/MAX11625		2.7		3.6	
MAX11619/MAX11621/ MAX11625 Supply Current (Note 9)	I_{DD}	Internal reference	f_{SAMPLE} = 300ksps		1750	2000	µA
			f_{SAMPLE} = 0, REF on		1000	1200	
			Shutdown		0.2	5	
		External reference	f_{SAMPLE} = 300ksps		1050	1200	
			Shutdown		0.2	5	
MAX11618/MAX11620/ MAX11624 Supply Current (Note 9)	I_{DD}	Internal reference	f_{SAMPLE} = 300ksps		2300	2550	µA
			f_{SAMPLE} = 0, REF on		1000	1350	
			Shutdown		0.2	5	
		External reference	f_{SAMPLE} = 300ksps		1550	1700	
			Shutdown		0.2	5	
Power-Supply Rejection	PSR	V_{DD} = 2.7V to 3.6V, full-scale input			±0.2	±1	mV
		V_{DD} = 4.75V to 5.25V, full-scale input			±0.2	±1.4	

Note 2: Limits at T_A = -40°C are guaranteed by design and not production tested.
Note 3: MAX11619/MAX11621/MAX11625 tested at V_{DD} = +3V. MAX11618/MAX11620/MAX11624 tested at V_{DD} = +5V.
Note 4: Offset nulled.
Note 5: Time for reference to power up and settle to within 1 LSB.
Note 6: Conversion time is defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle.
Note 7: See Figure 3 (Equivalent Input Circuit) and the Sampling Error vs. Source Impedance curve in the *Typical Operating Characteristics* section.
Note 8: When $\overline{CNVST}$ is configured as a digital input, do not apply a voltage between V_{IL} and V_{IH}.
Note 9: Supply current is specified depending on whether an internal or external reference is used for voltage conversions.

TIMING CHARACTERISTICS (Figure 1)

(V_{DD} = 2.7V to 3.6V (MAX11619/MAX11621/MAX11625); V_{DD} = 4.75V to 5.25V (MAX11618/MAX11620/MAX11624), f_{SAMPLE} = 300kHz, f_{SCLK} = 4.8MHz (50% duty cycle), V_{REF} = 2.5V (MAX11619/MAX11621/MAX11625); V_{REF} = 4.096V (MAX11618/MAX11620/MAX11624), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

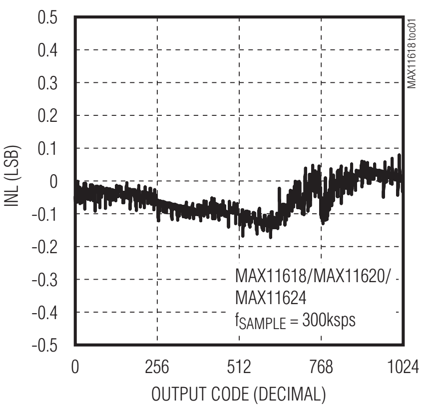
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Clock Period	t_{CP}	Externally clocked conversion	208			ns
		Data I/O	100			
SCLK Pulse-Width High	t_{CH}		40			ns
SCLK Pulse-Width Low	t_{CL}		40			ns
SCLK Fall to DOUT Transition	t_{DOT}	C_{LOAD} = 30pF			40	ns
$\overline{CS}$ Rise to DOUT Disable	t_{DOD}	C_{LOAD} = 30pF			40	ns
$\overline{CS}$ Fall to DOUT Enable	t_{DOE}	C_{LOAD} = 30pF			40	ns
DIN to SCLK Rise Setup	t_{DS}		40			ns
SCLK Rise to DIN Hold	t_{DH}		0			ns
$\overline{CS}$ Low to SCLK Setup	t_{CSS0}		40			ns
$\overline{CS}$ High to SCLK Setup	t_{CSS1}		40			ns
$\overline{CS}$ High After SCLK Hold	t_{CSH1}		0			ns
$\overline{CS}$ Low After SCLK Hold	t_{CSH0}		0		4	µs
$\overline{CNVST}$ Pulse Width Low	t_{CSPW}	CKSEL = 00	40			ns
		CKSEL = 01	1.4			µs
$\overline{CS}$ or $\overline{CNVST}$ Rise to $\overline{EOC}$ Low (Note 10)		Voltage conversion			7	µs
		Reference power-up			65	

Note 10: This time is defined as the number of clock cycles needed for conversion multiplied by the clock period. If the internal reference needs to be powered up, the total time is additive.

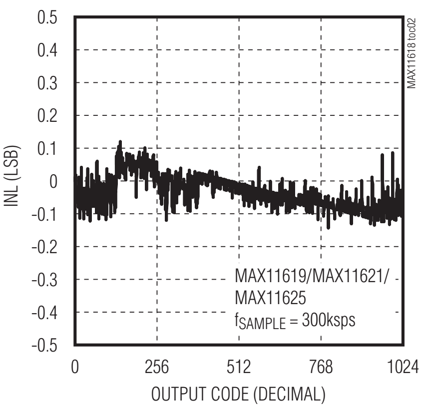
Typical Operating Characteristics

(V_{DD} = 3V (MAX11619/MAX11621/MAX11625); V_{DD} = 5V (MAX11618/MAX11620/MAX11624), f_{SCLK} = 4.8MHz, C_{LOAD} = 30pF, T_A = +25°C, unless otherwise noted.)

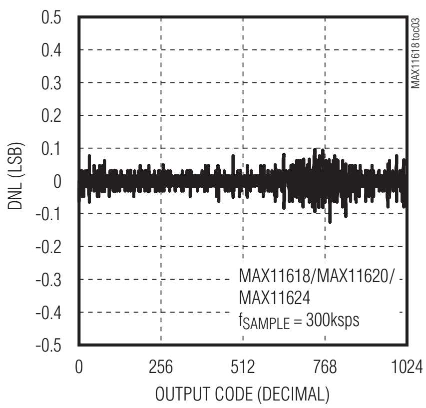
INTEGRAL NONLINEARITY vs. OUTPUT CODE



INTEGRAL NONLINEARITY vs. OUTPUT CODE



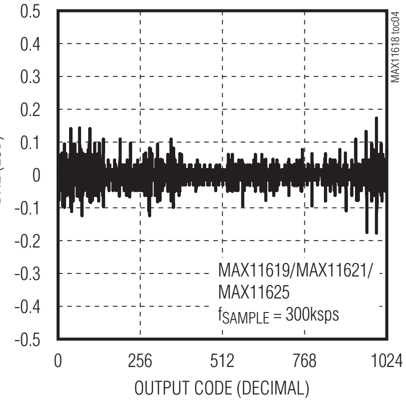
DIFFERENTIAL NONLINEARITY vs. OUTPUT CODE



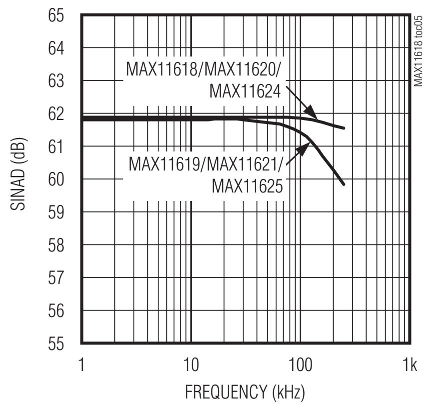
Typical Operating Characteristics (continued)

(V_{DD} = 3V (MAX11619/MAX11621/MAX11625); V_{DD} = 5V (MAX11618/MAX11620/MAX11624), f_{SCLK} = 4.8MHz, C_{LOAD} = 30pF, T_A = +25°C, unless otherwise noted.)

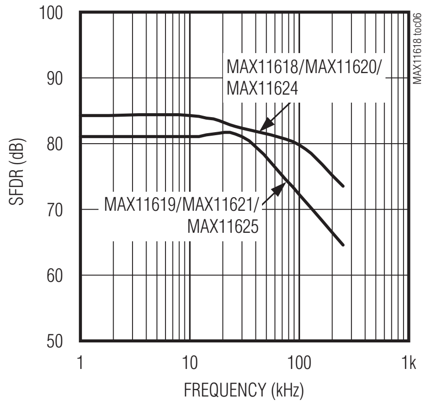
DIFFERENTIAL NONLINEARITY vs. OUTPUT CODE



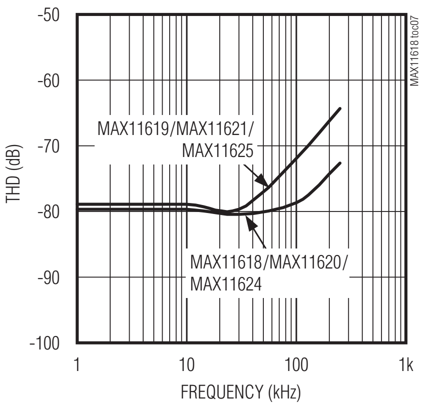
SINAD vs. FREQUENCY



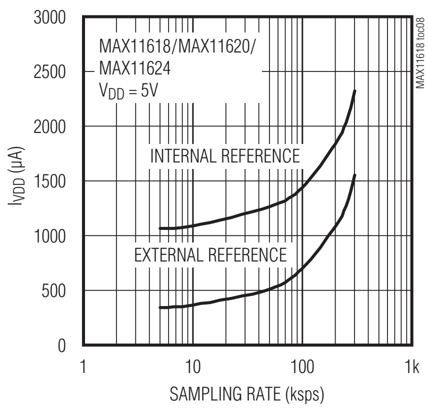
SFDR vs. FREQUENCY



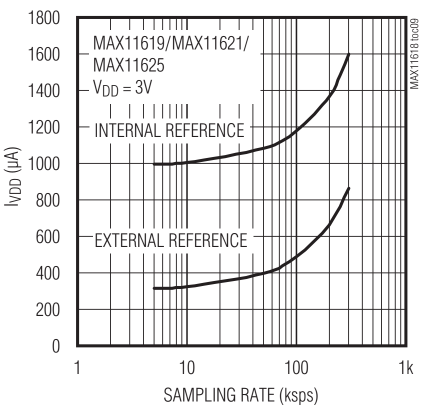
THD vs. FREQUENCY



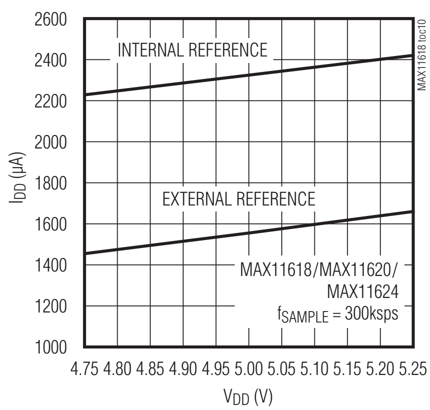
SUPPLY CURRENT vs. SAMPLING RATE



SUPPLY CURRENT vs. SAMPLING RATE



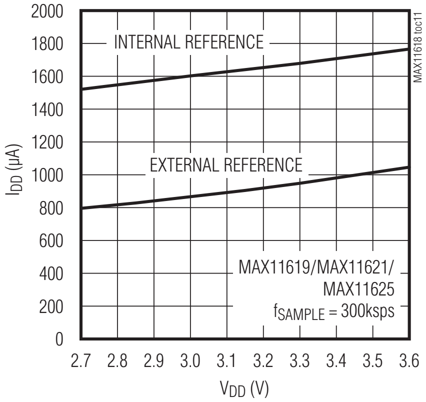
SUPPLY CURRENT vs. SUPPLY VOLTAGE



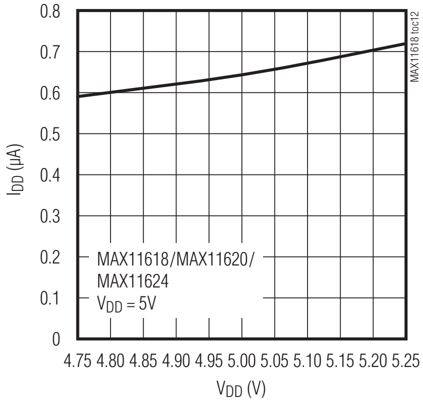
Typical Operating Characteristics (continued)

(V_{DD} = 3V (MAX11619/MAX11621/MAX11625); V_{DD} = 5V (MAX11618/MAX11620/MAX11624), f_{SCLK} = 4.8MHz, C_{LOAD} = 30pF, T_A = +25°C, unless otherwise noted.)

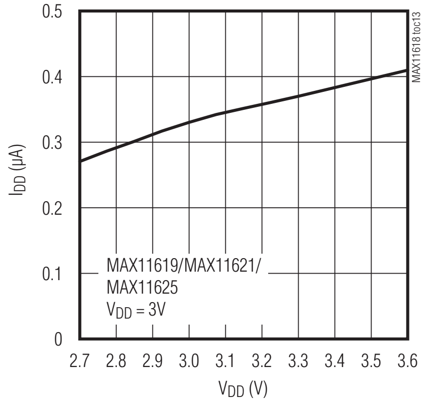
SUPPLY CURRENT vs. SUPPLY VOLTAGE



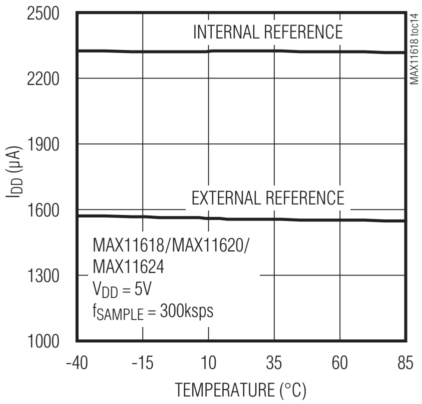
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



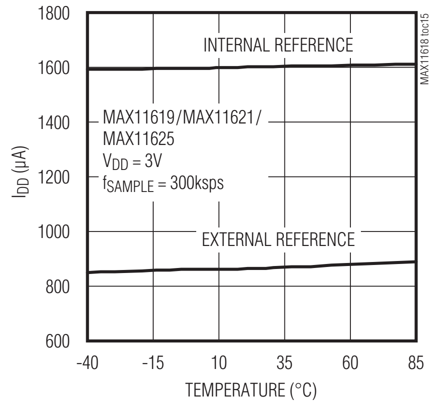
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



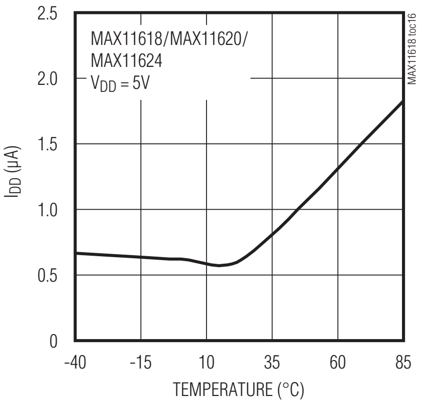
SUPPLY CURRENT vs. TEMPERATURE



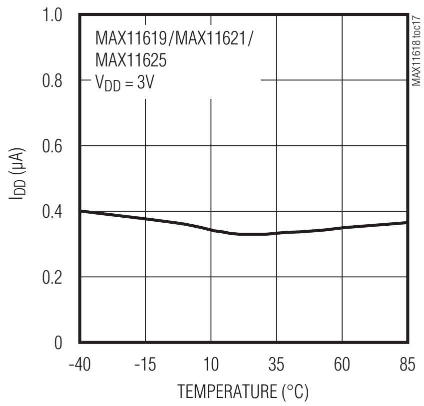
SUPPLY CURRENT vs. TEMPERATURE



SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE

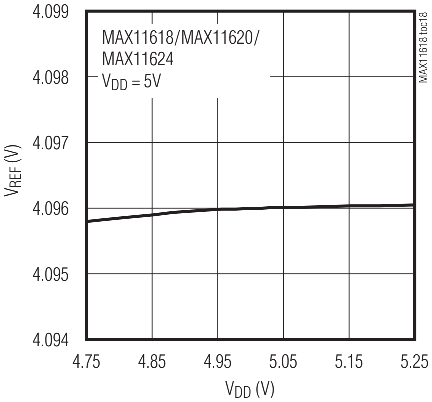


10-Bit, 300ksps ADCs with FIFO and Internal Reference

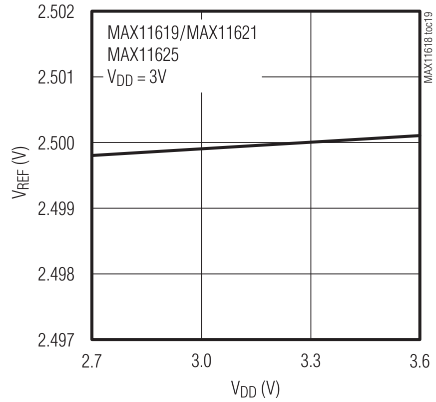
Typical Operating Characteristics (continued)

(V_{DD} = 3V (MAX11619/MAX11621/MAX11625); V_{DD} = 5V (MAX11618/MAX11620/MAX11624), f_{SCLK} = 4.8MHz, C_{LOAD} = 30pF, T_A = +25°C, unless otherwise noted.)

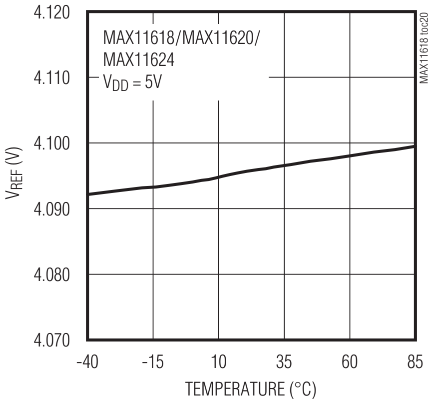
INTERNAL REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



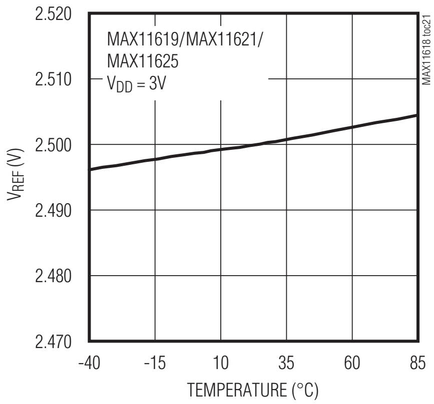
INTERNAL REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



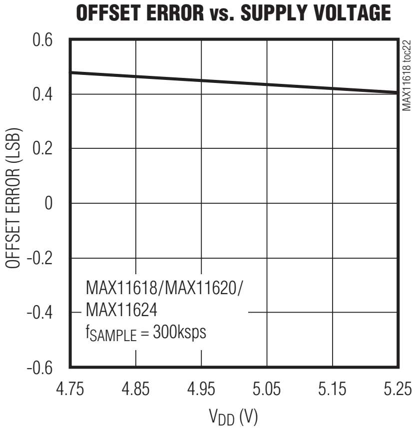
INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



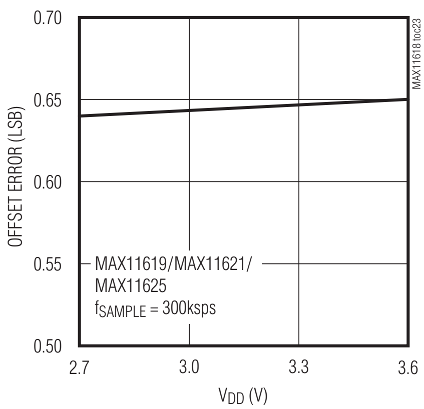
INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



OFFSET ERROR vs. SUPPLY VOLTAGE



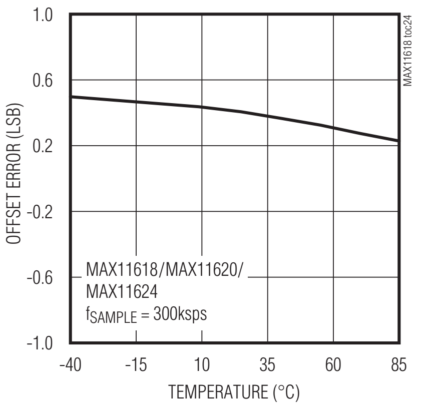
OFFSET ERROR vs. SUPPLY VOLTAGE



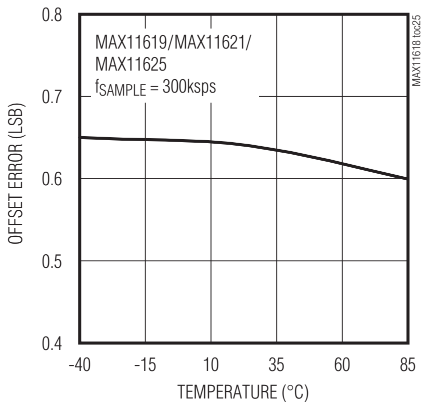
Typical Operating Characteristics (continued)

(V_{DD} = 3V (MAX11619/MAX11621/MAX11625); V_{DD} = 5V (MAX11618/MAX11620/MAX11624), f_{SCLK} = 4.8MHz, C_{LOAD} = 30pF, T_A = +25°C, unless otherwise noted.)

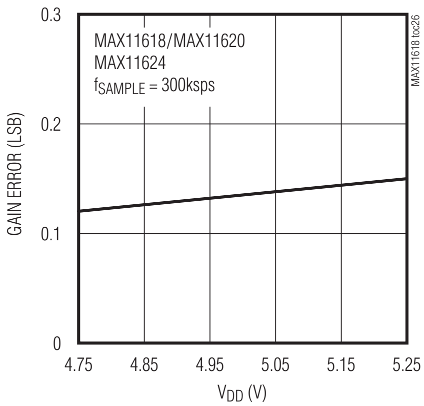
OFFSET ERROR vs. TEMPERATURE



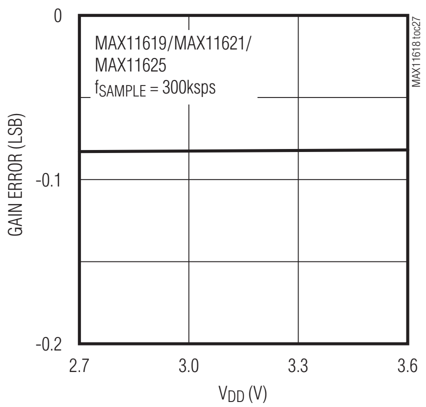
OFFSET ERROR vs. TEMPERATURE



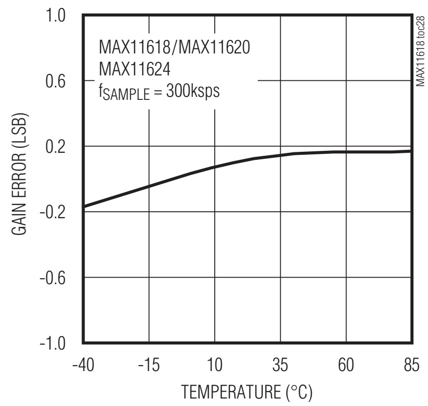
GAIN ERROR vs. SUPPLY VOLTAGE



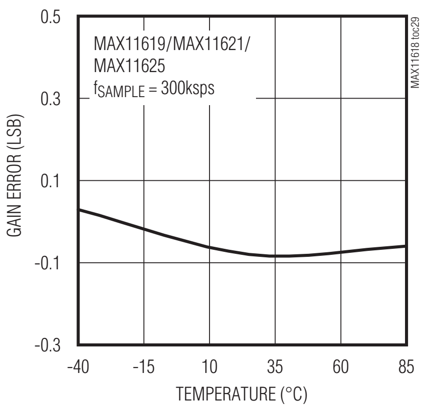
GAIN ERROR vs. SUPPLY VOLTAGE



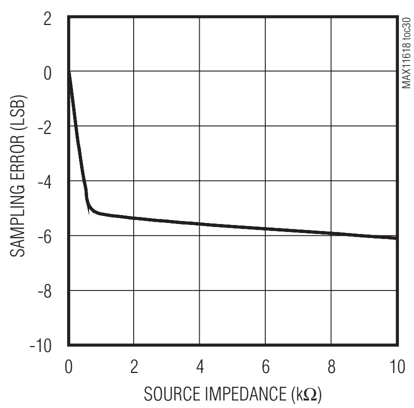
GAIN ERROR vs. TEMPERATURE



GAIN ERROR vs. TEMPERATURE

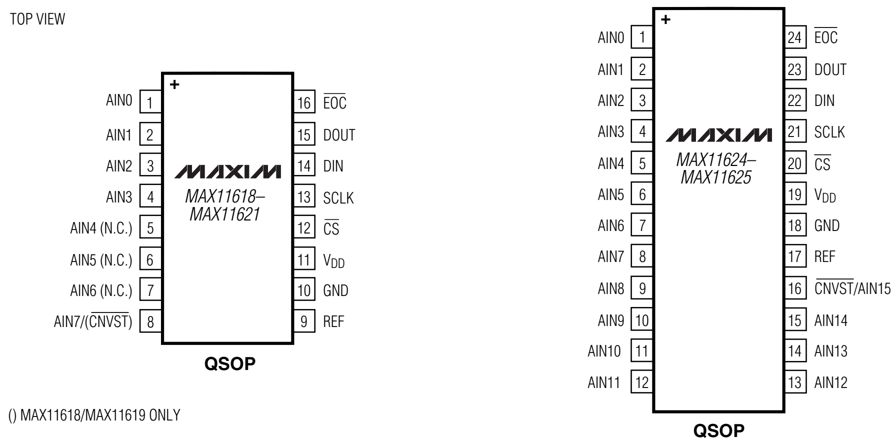


SAMPLING ERROR vs. SOURCE IMPEDANCE



10-Bit, 300ksps ADCs with FIFO and Internal Reference

Pin Configurations



Pin Description

PIN			NAME	FUNCTION
MAX11618 MAX11619 (4 CHANNELS)	MAX11620 MAX11621 (8 CHANNELS)	MAX11624 MAX11625 (16 CHANNELS)		
1–4	—	—	AIN0–AIN3	Analog Inputs
5, 6, 7	—	—	N.C.	No Connection. Not internally connected.
—	—	1–15	AIN0–AIN14	Analog Inputs
—	1–7	—	AIN0–AIN6	Analog Inputs
—	—	16	$\overline{\text{CNVST}}$/AIN15	Active-Low Conversion Start Input/Analog Input 15. See Table 3 for details on programming the setup register.
—	8	—	$\overline{\text{CNVST}}$/AIN7	Active-Low Conversion Start Input/Analog Input 7. See Table 3 for details on programming the setup register.
8	—	—	$\overline{\text{CNVST}}$	Active-Low Conversion Start Input. See Table 3 for details on programming the setup register.
9	9	17	REF	Reference Input. Bypass to GND with a 0.1µF capacitor.
10	10	18	GND	Ground
11	11	19	V_{DD}	Power Input. Bypass to GND with a 0.1µF capacitor.
12	12	20	$\overline{\text{CS}}$	Active-Low Chip-Select Input. When $\overline{\text{CS}}$ is low, the serial interface is enabled. When $\overline{\text{CS}}$ is high, DOUT is high impedance.
13	13	21	SCLK	Serial Clock Input. Clocks data in and out of the serial interface (duty cycle must be 40% to 60%). See Table 3 for details on programming the clock mode.
14	14	22	DIN	Serial Data Input. DIN data is latched into the serial interface on the rising edge of SCLK.
15	15	23	DOUT	Serial Data Output. Data is clocked out on the falling edge of SCLK. High impedance when $\overline{\text{CS}}$ is connected to V_{DD}.
16	16	24	$\overline{\text{EOC}}$	End of Conversion Output. Data is valid after $\overline{\text{EOC}}$ pulls low.

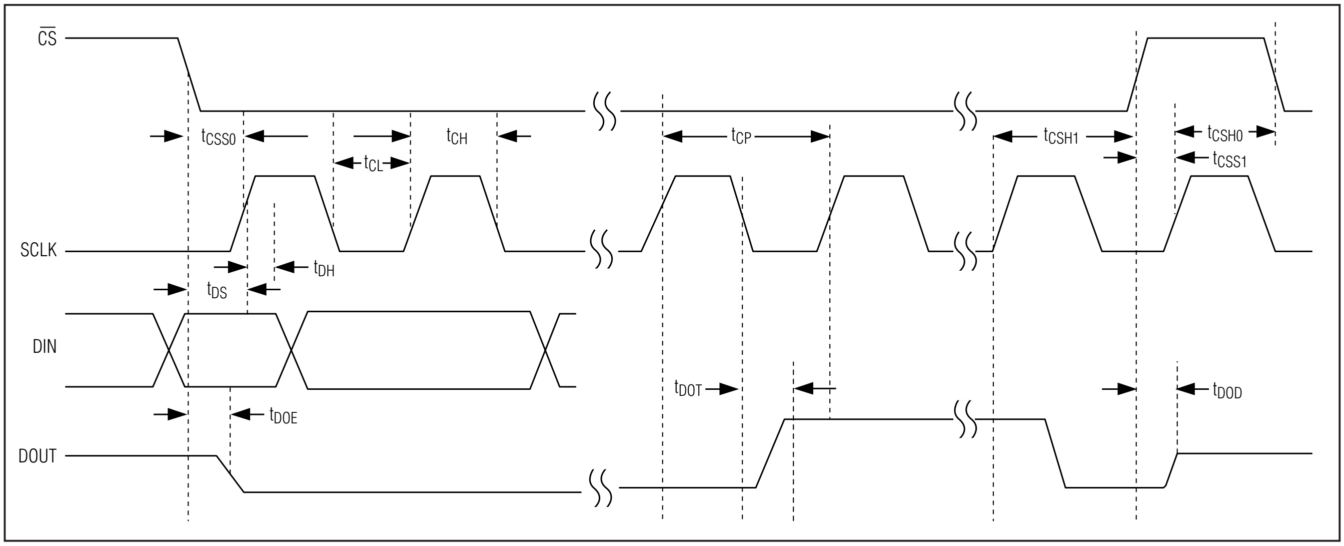


Figure 1. Detailed Serial-Interface Timing Diagram

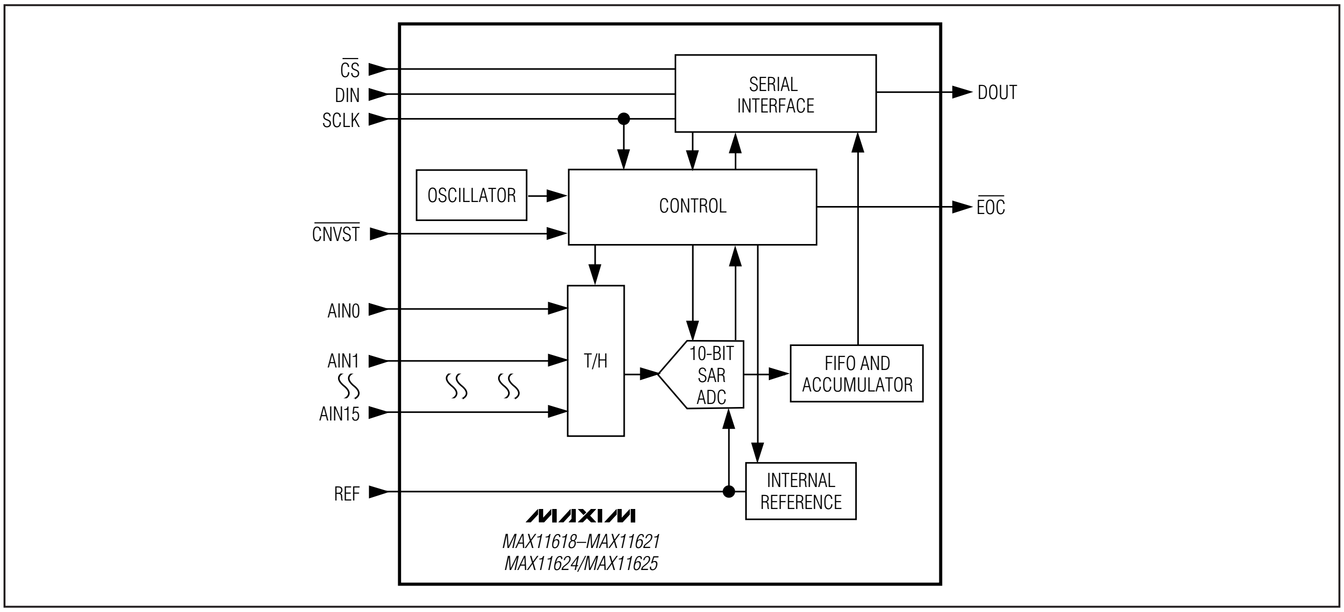


Figure 2. Functional Diagram

Detailed Description

The MAX11618–MAX11621/MAX11624/MAX11625 are low-power, serial-output, multichannel ADCs with FIFO capability for system monitoring, process-control, and instrumentation applications. These 10-bit ADCs have internal track and hold (T/H) circuitry supporting single-ended inputs. Data is converted from analog voltage sources in a variety of channel and data-acquisition configurations. Microprocessor (µP) control is made easy through a 3-wire SPI-/QSPI-/MICROWIRE-compatible serial interface.

Figure 2 shows a simplified functional diagram of the MAX11618–MAX11621/MAX11624/MAX11625 internal architecture. The MAX11624/MAX11625 have 16 single-ended analog input channels. The MAX11620/MAX11621 have 8 single-ended analog input channels. The MAX11618/MAX11619 have 4 single-ended analog input channels.

10-Bit, 300ksps ADCs with FIFO and Internal Reference

Converter Operation

The MAX11618–MAX11621/MAX11624/MAX11625 ADCs use a successive-approximation register (SAR) conversion technique and an on-chip T/H block to convert voltage signals into a 10-bit digital result. This single-ended configuration supports unipolar signal ranges.

Input Bandwidth

The ADC's input-tracking circuitry has a 1MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. Anti-alias prefiltering of the input signals is necessary to avoid high-frequency signals aliasing into the frequency band of interest.

Analog Input Protection

Internal ESD protection diodes clamp all pins to V_{DD} and GND, allowing the inputs to swing from (GND - 0.3V) to (V_{DD} + 0.3V) without damage. However, for accurate conversions near full scale, the inputs must not exceed V_{DD} by more than 50mV or be lower than GND by 50mV. If an off-channel analog input voltage exceeds the supplies, limit the input current to 2mA.

3-Wire Serial Interface

The MAX11618–MAX11621/MAX11624/MAX11625 feature a serial interface compatible with SPI/QSPI and MICROWIRE devices. For SPI/QSPI, ensure the CPU serial interface runs in master mode so it generates the serial clock signal. Select the SCLK frequency of 10MHz or less, and set clock polarity (CPOL) and phase (CPHA) in the µP control registers to the same value. The MAX11618–MAX11621/MAX11624/MAX11625 operate with SCLK idling high or low, and thus operate with CPOL = CPHA = 0 or CPOL = CPHA = 1. Set $\overline{CS}$ low to latch input data at DIN on the rising edge of SCLK. Output data at DOUT is updated on the falling edge of SCLK. Results are output in binary format.

Serial communication always begins with an 8-bit input data byte (MSB first) loaded from DIN. A high-to-low transition on $\overline{CS}$ initiates the data input operation. The input data byte and the subsequent data bytes are clocked from DIN into the serial interface on the rising edge of SCLK. Tables 1–5 detail the register descriptions. Bits 5 and 4, CKSEL1 and CKSEL0, respectively, control the clock modes in the setup register (see Table 3). Choose between four different clock modes for various ways to start a conversion and determine whether the acquisitions are internally or externally timed. Select clock mode 00 to configure $\overline{CNVST}$/AIN_ to act as a conversion start and use it to request the programmed, internally timed conversions without tying up the serial bus. In clock mode 01, use $\overline{CNVST}$ to request conversions one channel at a time, controlling the sampling speed without tying up the serial bus. Request and start internally timed conversions through the serial interface by writing to the conversion register in the default clock mode 10. Use clock mode 11 with SCLK up to 4.8MHz for externally timed acquisitions to achieve sampling rates up to 300ksps. Clock mode 11 disables scanning and averaging. See Figures 4–7 for timing specifications and how to begin a conversion.

These devices feature an active-low, end-of-conversion output. $\overline{EOC}$ goes low when the ADC completes the last requested operation and is waiting for the next input data byte (for clock modes 00 and 10). In clock mode 01, $\overline{EOC}$ goes low after the ADC completes each requested operation. $\overline{EOC}$ goes high when $\overline{CS}$ or $\overline{CNVST}$ goes low. $\overline{EOC}$ is always high in clock mode 11.

Single-Ended Inputs

The single-ended analog input conversion modes can be configured by writing to the setup register (see Table 3). Single-ended conversions are internally referenced to GND (see Figure 3).

AIN0–AIN3 are available on the MAX11618–MAX11621/MAX11624/MAX11625. AIN4–AIN7 are only available on the MAX11620–MAX11625. AIN8–AIN15 are only available on the MAX11624/MAX11625. See Tables 2–5 for more details on configuring the inputs. For the inputs that can be configured as $\overline{CNVST}$ or an analog input, only one can be used at a time.

Unipolar

The MAX11618–MAX11621/MAX11624/MAX11625 always operate in unipolar mode. The analog inputs are internally referenced to GND with a full-scale input range from 0 to V_{REF}.

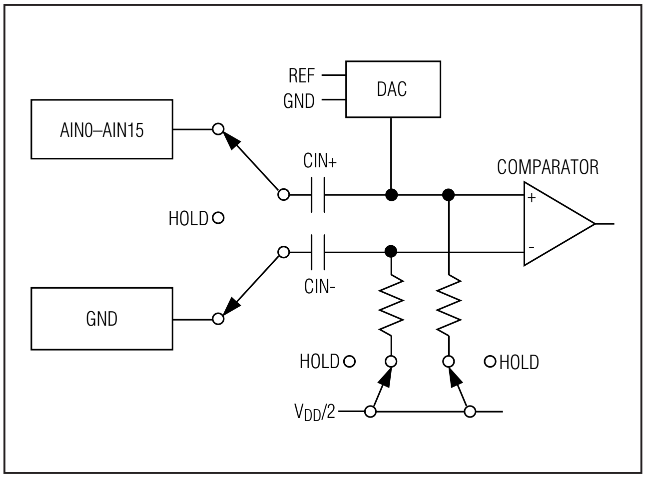


Figure 3. Equivalent Input Circuit

True Differential Analog Input T/H

The equivalent circuit of Figure 3 shows the MAX11618–MAX11621/MAX11624/MAX11625s' input architecture. In track mode, a positive input capacitor is connected to AIN0–AIN15. A negative input capacitor is connected to GND. For external T/H timing, use clock mode 01. After the T/H enters hold mode, the difference between the sampled positive and negative input voltages is converted. The time required for the T/H to acquire an input signal is determined by how quickly its input capacitance is charged. If the input signal's source impedance is high, the required acquisition time lengthens. The acquisition time, t_{ACQ}, is the maximum time needed for a signal to be acquired, plus the power-up time. It is calculated by the following equation:

$$t_{ACQ} = 9 \times (R_S + R_{IN}) \times 24pF + t_{PWR}$$

where R_{IN} = 1.5kΩ, R_S is the source impedance of the input signal, and t_{PWR} = 1µs, the power-up time of the device. The varying power-up times are detailed in the explanation of the clock mode conversions. When the conversion is internally timed, t_{ACQ} is never less than 1.4µs, and any source impedance below 300Ω does not significantly affect the ADC's AC performance. A high-impedance source can be accommodated either by lengthening t_{ACQ} or by placing a 1µF capacitor between the positive and negative analog inputs.

Internal FIFO

The MAX11618–MAX11621/MAX11624/MAX11625 contain a FIFO buffer that can hold up to 16 ADC results. This allows the ADC to handle multiple internally clocked conversions, without tying up the serial bus. If the FIFO is filled and further conversions are requested without reading from the FIFO, the oldest ADC results are overwritten by the new ADC results. Each result contains 2 bytes, with the MSB preceded by four leading zeros. After each falling edge of $\overline{CS}$, the oldest available byte of data is available at DOUT, MSB first. When the FIFO is empty, DOUT is zero.

Internal Clock

The MAX11618–MAX11621/MAX11624/MAX11625 operate from an internal oscillator, which is accurate within 10% of the 4.4MHz nominal clock rate. The internal oscillator is active in clock modes 00, 01, and 10. Read out the data at clock speeds up to 10MHz. See Figures 4–7 for details on timing specifications and starting a conversion.

Applications Information

Register Descriptions

The MAX11618–MAX11621/MAX11624/MAX11625 communicate between the internal registers and the external circuitry through the SPI-/QSPI-compatible serial interface. Table 1 details the registers and the bit names. Tables 2–5 show the various functions within the conversion register, setup register, averaging register, and reset register.

Conversion Time Calculations

The conversion time for each scan is based on a number of different factors: conversion time per sample, samples per result, results per scan, and if the external reference is in use.

Use the following formula to calculate the total conversion time for an internally timed conversion in clock modes 00 and 10 (see the *Electrical Characteristics* section as applicable):

$$\text{Total Conversion Time} = t_{CNV} \times n_{AVG} \times n_{RESULT} + t_{RP}$$

where:

$t_{CNV} = t_{ACQ}$ (max) + t_{CONV} (max).

n_{AVG} = samples per result (amount of averaging).

n_{RESULT} = number of FIFO results requested; determined by the number of channels being scanned or by NSCAN1, NSCAN0.

t_{RP} = internal reference wake-up; set to zero if internal reference is already powered up or external reference is being used .

In clock mode 01, the total conversion time depends on how long $\overline{CNVST}$ is held low or high, including any time required to turn on the internal reference. Conversion time in externally clocked mode (CKSEL1, CKSEL0 = 11) depends on the SCLK period and how long $\overline{CS}$ is held high between each set of eight SCLK cycles. In clock mode 01, the total conversion time does not include the time required to turn on the internal reference.

Table 1. Input Data Byte (MSB First)

REGISTER NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Conversion	1	CHSEL3	CHSEL2	CHSEL1	CHSEL0	SCAN1	SCAN0	X
Setup	0	1	CKSEL1	CKSEL0	REFSEL1	REFSEL0	X	X
Averaging	0	0	1	AVGON	NAVG1	NAVG0	NSCAN1	NSCAN0
Reset	0	0	0	1	$\overline{RESET}$	X	X	X

X = Don't care.

Conversion Register

Select active analog input channels per scan and scan modes by writing to the conversion register. Table 2 details channel selection and the four scan modes. Request a scan by writing to the conversion register when in clock mode 10 or 11, or by applying a low pulse to the $\overline{\text{CNVST}}$ pin when in clock mode 00 or 01.

A conversion is not performed if it is requested on a channel that has been configured as $\overline{\text{CNVST}}$. Do not request conversions on channels 8–15 on the MAX11618–MAX11621. Set CHSEL3:CHSEL0 to the lower channel's binary values.

Select scan mode 00 or 01 to return one result per single-ended channel within the requested range. Select scan mode 10 to scan a single input channel numerous times, depending on NSCAN1 and NSCAN0 in the averaging register (Table 4). Select scan mode 11 to return only one result from a single channel.

Setup Register

Write a byte to the setup register to configure the clock, reference, and power-down modes. Table 3 details the bits in the setup register. Bits 5 and 4 (CKSEL1 and CKSEL0) control the clock mode, acquisition and sampling, and the conversion start. Bits 3 and 2 (REFSEL1 and REFSEL0) control internal or external reference use.

Averaging Register

Write to the averaging register to configure the ADC to average up to 32 samples for each requested result, and to independently control the number of results requested for single-channel scans.

Table 2 details the four scan modes available in the conversion register. All four scan modes allow averaging as long as the AVGON bit, bit 4 in the averaging register, is set to 1. Select scan mode 10 to scan the same channel multiple times. Clock mode 11 disables averaging.

Reset Register

Write to the reset register (as shown in Table 5) to clear the FIFO or to reset all registers to their default states. Set the $\overline{\text{RESET}}$ bit to 1 to reset the FIFO. Set the reset bit to zero to return the MAX11618–MAX11621/MAX11624/MAX11625 to the default power-up state.

Table 2. Conversion Register*

BIT NAME	BIT	FUNCTION
—	7 (MSB)	Set to 1 to select conversion register.
CHSEL3	6	Analog input channel select.
CHSEL2	5	Analog input channel select.
CHSEL1	4	Analog input channel select.
CHSEL0	3	Analog input channel select.
SCAN1	2	Scan mode select.
SCAN0	1	Scan mode select.
—	0 (LSB)	Don't care.

*See below for bit details.

CHSEL3	CHSEL2	CHSEL1	CHSEL0	SELECTED CHANNEL (N)
0	0	0	0	AIN0
0	0	0	1	AIN1
0	0	1	0	AIN2
0	0	1	1	AIN3
0	1	0	0	AIN4
0	1	0	1	AIN5
0	1	1	0	AIN6
0	1	1	1	AIN7
1	0	0	0	AIN8
1	0	0	1	AIN9
1	0	1	0	AIN10
1	0	1	1	AIN11
1	1	0	0	AIN12
1	1	0	1	AIN13
1	1	1	0	AIN14
1	1	1	1	AIN15

SCAN1	SCAN0	SCAN MODE (CHANNEL N IS SELECTED BY BITS CHSEL3–CHSEL0)
0	0	Scans channels 0 through N.
0	1	Scans channels N through the highest numbered channel.
1	0	Scans channel N repeatedly. The averaging register sets the number of results.
1	1	No scan. Converts channel N once only.

Table 3. Setup Register*

BIT NAME	BIT	FUNCTION
—	7 (MSB)	Set to zero to select setup register.
—	6	Set to 1 to select setup register.
CKSEL1	5	Clock mode and $\overline{\text{CNVST}}$ configuration. Resets to 1 at power-up.
CKSEL0	4	Clock mode and $\overline{\text{CNVST}}$ configuration.
REFSEL1	3	Reference mode configuration.
REFSEL0	2	Reference mode configuration.
—	1	Don't care.
—	0 (LSB)	Don't care.

**See below for bit details.*

CKSEL1	CKSEL0	CONVERSION CLOCK	ACQUISITION/SAMPLING	$\overline{\text{CNVST}}$ CONFIGURATION
0	0	Internal	Internally timed	$\overline{\text{CNVST}}$
0	1	Internal	Externally timed through $\overline{\text{CNVST}}$	$\overline{\text{CNVST}}$
1	0	Internal	Internally timed	AIN15/AIN11/AIN7**
1	1	External (4.8MHz max)	Externally timed through SCLK	AIN15/AIN11/AIN7**

***For the MAX11618/MAX11619, $\overline{\text{CNVST}}$ has its own dedicated pin.*

REFSEL1	REFSEL0	VOLTAGE REFERENCE	AutoShutdown
0	0	Internal	Reference off after scan; need wake-up delay.
0	1	External single ended	Reference off; no wake-up delay.
1	0	Internal	Reference always on; no wake-up delay.
1	1	Reserved	Reserved. Do not use.

Table 4. Averaging Register*

BIT NAME	BIT	FUNCTION
—	7 (MSB)	Set to 0 to select averaging register.
—	6	Set to 0 to select averaging register.
—	5	Set to 1 to select averaging register.
AVGON	4	Set to 1 to turn averaging on. Set to zero to turn averaging off.
NAVG1	3	Configures the number of conversions for single-channel scans.
NAVG0	2	Configures the number of conversions for single-channel scans.
NSCAN1	1	Single-channel scan count. (Scan mode 10 only.)
NSCAN0	0 (LSB)	Single-channel scan count. (Scan mode 10 only.)

**See below for bit details.*

AVGON	NAVG1	NAVG0	FUNCTION
0	X	X	Performs 1 conversion for each requested result.
1	0	0	Performs 4 conversions and returns the average for each requested result.
1	0	1	Performs 8 conversions and returns the average for each requested result.
1	1	0	Performs 16 conversions and returns the average for each requested result.
1	1	1	Performs 32 conversions and returns the average for each requested result.

X = Don't care.

NSCAN1	NSCAN0	FUNCTION (APPLIES ONLY IF SCAN MODE 10 IS SELECTED)
0	0	Scans channel N and returns 4 results.
0	1	Scans channel N and returns 8 results.
1	0	Scans channel N and returns 12 results.
1	1	Scans channel N and returns 16 results.

Table 5. Reset Register

BIT NAME	BIT	FUNCTION
—	7 (MSB)	Set to 0 to select reset register.
—	6	Set to 0 to select reset register.
—	5	Set to 0 to select reset register.
—	4	Set to 1 to select reset register.
$\overline{\text{RESET}}$	3	Set to zero to reset all registers. Set to 1 to clear the FIFO only.
X	2	Don't care.
X	1	Don't care.
X	0 (LSB)	Don't care.

Power-Up Default State

The MAX11618–MAX11621/MAX11624/MAX11625 power up with all blocks in shutdown, including the reference. All registers power up in state 00000000, except for the setup register, which powers up in clock mode 10 (CKSEL1 = 1).

Output Data Format

Figures 4–7 illustrate the conversion timing for the MAX11618–MAX11621/MAX11624/MAX11625. The 10-bit conversion result is output in MSB-first format with four leading zeros followed by 10-bit data and two trailing zeros. DIN data is latched into the serial interface on the rising edge of SCLK. Data on DOUT transitions on the falling edge of SCLK. Conversions in clock modes 00 and 01 are initiated by $\overline{\text{CNVST}}$. Conversions in clock modes 10 and 11 are initiated by writing an input data byte to the conversion register. Data output is binary.

Internally Timed Acquisitions and Conversions Using $\overline{\text{CNVST}}$

Performing Conversions in Clock Mode 00

In clock mode 00, the wake-up, acquisition, conversion, and shutdown sequences are initiated through $\overline{\text{CNVST}}$ and performed automatically using the internal oscillator. Results are added to the internal FIFO to be read out later. See Figure 4 for clock mode 00 timing.

Initiate a scan by setting $\overline{\text{CNVST}}$ low for at least 40ns before pulling it high again. The MAX11618–MAX11621/MAX11624/MAX11625 then wake up, scan all requested channels, store the results in the FIFO, and shut down. After the scan is complete, $\overline{\text{EOC}}$ is pulled low and the results are available in the FIFO. Wait until $\overline{\text{EOC}}$ goes low before pulling $\overline{\text{CS}}$ low to communicate with the serial interface. $\overline{\text{EOC}}$ stays low until $\overline{\text{CS}}$ or $\overline{\text{CNVST}}$ is pulled low again.

Do not initiate a second $\overline{\text{CNVST}}$ before $\overline{\text{EOC}}$ goes low; otherwise, the FIFO can become corrupted.

Externally Timed Acquisitions and Internally Timed Conversions with $\overline{\text{CNVST}}$

Performing Conversions in Clock Mode 01

In clock mode 01, conversions are requested one at a time using $\overline{\text{CNVST}}$ and performed automatically using the internal oscillator. See Figure 5 for clock mode 01 timing.

Setting $\overline{\text{CNVST}}$ low begins an acquisition, wakes up the ADC, and places it in track mode. Hold $\overline{\text{CNVST}}$ low for at least 1.4µs to complete the acquisition. If the internal reference needs to wake up, an additional 65µs is required for the internal reference to power up.

Set $\overline{\text{CNVST}}$ high to begin a conversion. After the conversion is complete, the ADC shuts down and pulls $\overline{\text{EOC}}$ low. $\overline{\text{EOC}}$ stays low until $\overline{\text{CS}}$ or $\overline{\text{CNVST}}$ is pulled low again. Wait until $\overline{\text{EOC}}$ goes low before pulling $\overline{\text{CS}}$ or $\overline{\text{CNVST}}$ low.

If averaging is turned on, multiple $\overline{\text{CNVST}}$ pulses need to be performed before a result is written to the FIFO. Once the proper number of conversions has been performed to generate an averaged FIFO result, as specified by the averaging register, the scan logic automatically switches the analog input multiplexer to the next-requested channel. The result is available on DOUT once $\overline{\text{EOC}}$ has been pulled low.

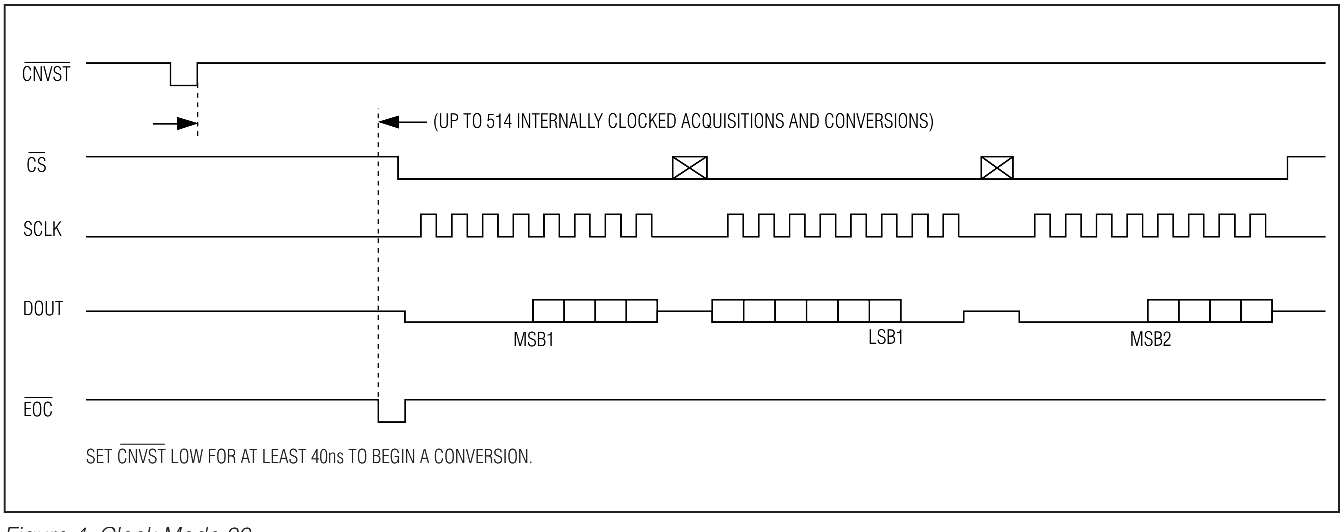


Figure 4. Clock Mode 00

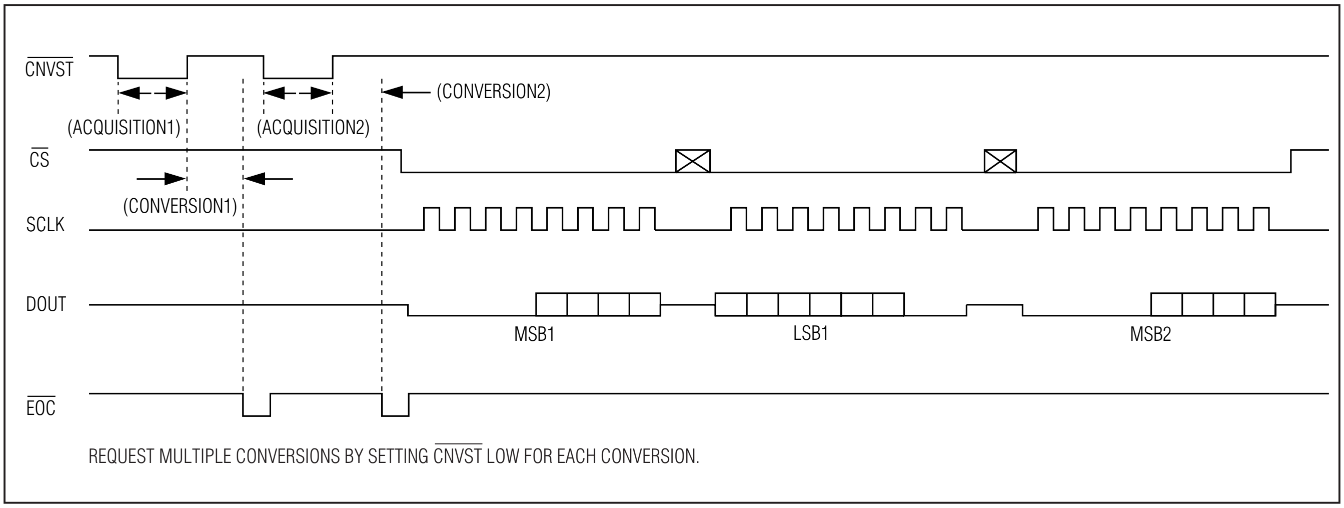


Figure 5. Clock Mode 01

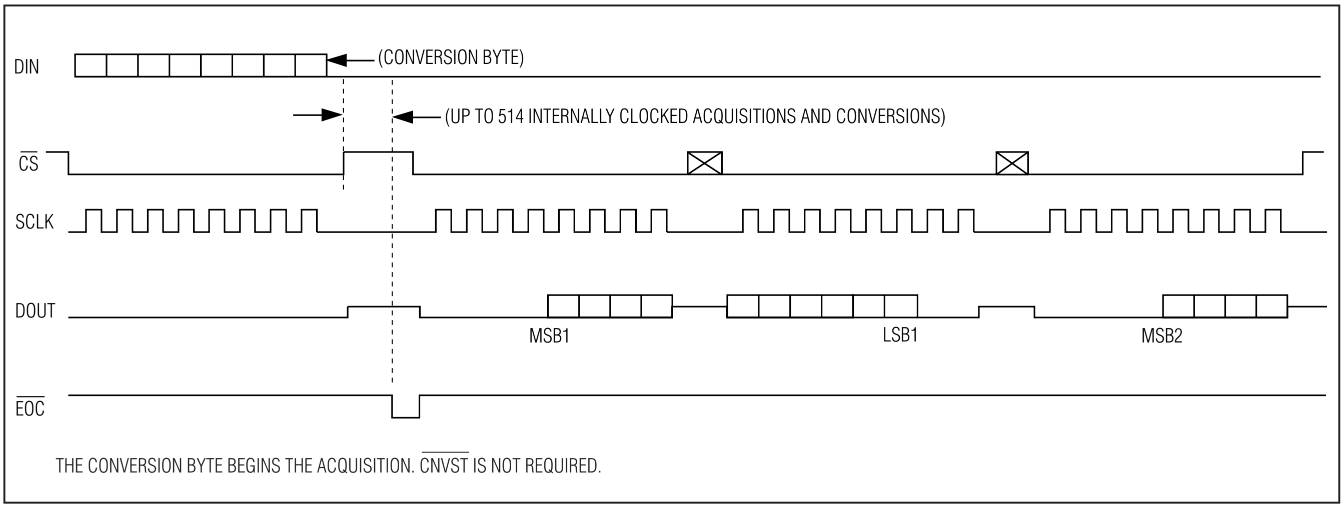


Figure 6. Clock Mode 10

Internally Timed Acquisitions and Conversions Using the Serial Interface

Performing Conversions in Clock Mode 10

In clock mode 10, the wake-up, acquisition, conversion, and shutdown sequences are initiated by writing an input data byte to the conversion register, and are performed automatically using the internal oscillator. This is the default clock mode upon power-up. See Figure 6 for clock mode 10 timing.

Initiate a scan by writing a byte to the conversion register. The MAX11618–MAX11621/MAX11624/MAX11625 then power up, scan all requested channels, store the results in the FIFO, and shut down. After the scan is complete, $\overline{EOC}$ is pulled low and the results are available in the FIFO. $\overline{EOC}$ stays low until $\overline{CS}$ is pulled low again.

Externally Clocked Acquisitions and Conversions Using the Serial Interface

Performing Conversions in Clock Mode 11

In clock mode 11, acquisitions and conversions are initiated by writing to the conversion register and are performed one at a time using the SCLK as the conversion clock. Scanning and averaging are disabled, and the conversion result is available at DOUT during the conversion. See Figure 7 for clock mode 11 timing.

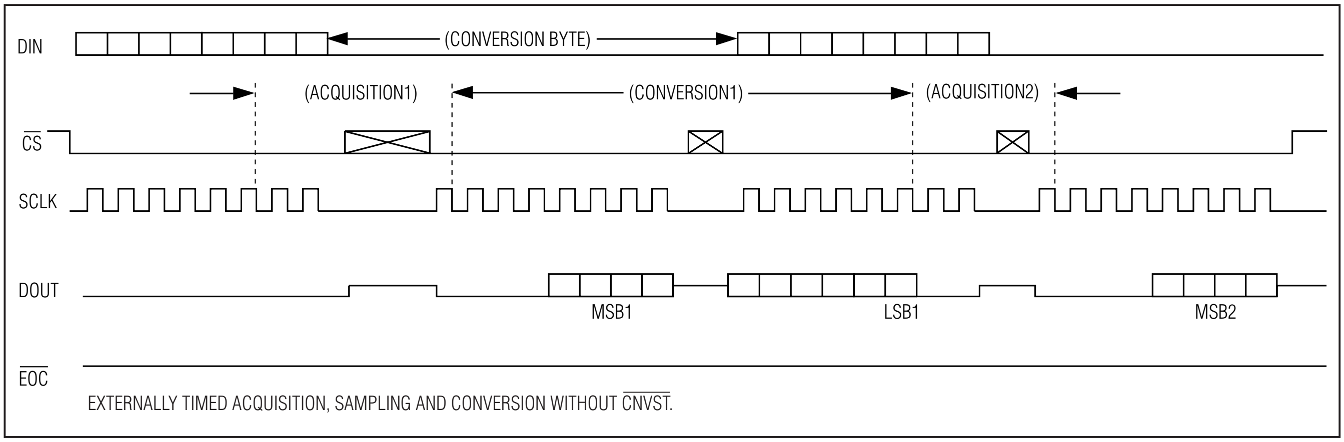


Figure 7. Clock Mode 11

Initiate a conversion by writing a byte to the conversion register followed by 16 SCLK cycles. If $\overline{CS}$ is pulsed high between the eight and ninth cycles, the pulse width must be less than 100µs. To continuously convert at 16 cycles per conversion, alternate 1 byte of zeros between each conversion byte.

If reference mode 00 is requested, wait 65µs with $\overline{CS}$ high after writing the conversion byte to extend the acquisition and allow the internal reference to power up.

Partial Reads and Partial Writes

If the first byte of an entry in the FIFO is partially read ($\overline{CS}$ is pulled high after fewer than eight SCLK cycles), the second byte of data that is read out contains the next 8 bits (not b7–b0). The remaining bits are lost for that entry. If the first byte of an entry in the FIFO is read out fully, but the second byte is read out partially, the rest of the entry is lost. The remaining data in the FIFO is uncorrupted and can be read out normally after taking $\overline{CS}$ low again, as long as the 4 leading bits (normally zeros) are ignored. Internal registers that are written partially through the SPI contain new values, starting at the MSB up to the point that the partial write is stopped. The part of the register that is not written contains previously written values. If $\overline{CS}$ is pulled low before $\overline{EOC}$ goes low, a conversion cannot be completed and the FIFO is corrupted.

Transfer Function

Figure 8 shows the unipolar transfer function for single-ended inputs. Code transitions occur halfway between successive-integer LSB values. Output coding is binary, with 1 LSB = V_{REF}/1024 for unipolar operation.

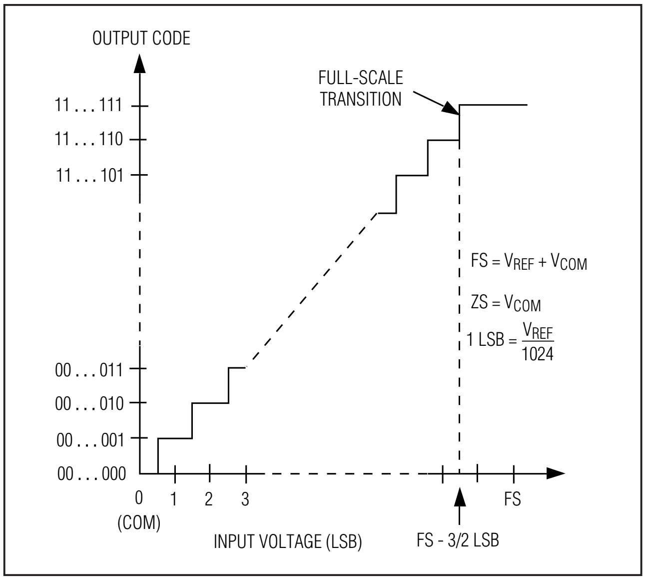


Figure 8. Unipolar Transfer Function, Full Scale (FS) = V_{REF}

Layout, Grounding, and Bypassing

For best performance, use PCBs. Do not use wire wrap boards. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) signals parallel to one another or run digital lines underneath the package. High-frequency noise in the V_{DD} power supply can affect performance. Bypass the V_{DD} supply with a 0.1µF capacitor to GND, close to the V_{DD} pin. Minimize capacitor lead lengths for best supply-noise rejection. If the power supply is very noisy, connect a 10Ω resistor in series with the supply to improve power-supply filtering.

Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. INL for the MAX11618–MAX11621/MAX11624/MAX11625 is measured using the end-point method.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes and a monotonic transfer function.

Aperture Jitter

Aperture jitter (t_{AJ}) is the sample-to-sample variation in the time between the samples.

Aperture Delay

Aperture delay (t_{AD}) is the time between the rising edge of the sampling clock and the instant when an actual sample is taken.

Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, signal-to-noise ratio (SNR) is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR = (6.02 \times N + 1.76)dB$$

In reality, there are other noise sources besides quantization noise, including thermal noise, reference noise, clock jitter, etc. Therefore, SNR is calculated by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to the RMS equivalent of all other ADC output signals:

$$SINAD\ (dB) = 20 \times \log (Signal_{RMS}/Noise_{RMS})$$

Effective Number of Bits

Effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, calculate the effective number of bits as follows:

$$ENOB = (SINAD - 1.76)/6.02$$

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log\left(\sqrt{\left(V2^2 + V3^2 + V4^2 + V5^2\right)}/V1\right)$$

where V1 is the fundamental amplitude, and V2–V5 are the amplitudes of the 2nd through 5th-order harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest distortion component.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 QSOP	E16+5	21-0055	90-0167
24 QSOP	E24+3	21-0055	90-0172

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/11	Initial release	—
1	9/11	Released MAX11618–MAX11621. Updated *Absolute Maximum Ratings*, *Transfer Function* section, and *Package Information*.	1, 2, 19, 20