



MAX1211 Evaluation Kit

General Description

The MAX1211 evaluation kit (EV kit) is a fully assembled and tested circuit board that contains all the components for evaluating the MAX1211, MAX1206–MAX1209, and MAX19538 12-bit, analog-to-digital converters (ADCs). The MAX1211 accepts differential or single-ended analog input signals. The EV kit allows for evaluation of each ADC with both types of signals from one single-ended analog signal source. The digital output produced by the ADC can be easily captured with a user-provided high-speed logic analyzer or data-acquisition system. The EV kit operates from 2.0V and 3.3V power supplies. It includes circuitry that generates a differential clock signal from an AC signal provided by the user. The EV kit comes with the MAX1211 installed. Contact the factory for free samples of the pin-compatible MAX1206–MAX1209 or MAX19538 to evaluate these parts.

Part Selection Table

PART	SPEED (Msps)	APPLICATION
MAX1206ETL	40	Baseband sampling
MAX1207ETL	65	Baseband sampling
MAX1208ETL	80	Baseband sampling
MAX1209ETL	80	IF sampling
MAX1211ETL	65	IF sampling
MAX19538ETL	95	IF/Baseband

Features

- ◆ Up to 65Msps Sampling Rate with the MAX1211
- ◆ Low Voltage and Power Operation
- ◆ Fully Differential or Single-Ended Signal Input Configuration
- ◆ Differential or Single-Ended Clock Configuration
- ◆ On-Board Clock-Shaping Circuit with Variable Duty Cycle
- ◆ Also Evaluates MAX1206–MAX1209 and MAX19538
- ◆ Fully Assembled and Tested

Ordering Information

PART	TEMP RANGE	IC PACKAGE
MAX1211EVKIT	0°C to +70°C	40 Thin QFN

Note: To evaluate the MAX1206–MAX1209 or MAX19538, request a free sample with the MAX1211 EV kit.

Component List

DESIGNATION	QTY	DESCRIPTION
C1, C2, C7, C55	4	22 μ F \pm 20%, 10V tantalum capacitors (B case) AVX TAJB226M010
C3–C6, C8–C12, C56	10	1.0 μ F \pm 20%, 10V X5R ceramic capacitors (0603) TDK C1608X5R1A105M
C13, C15, C17, C21–C29, C33, C44, C50–C53, C57	19	0.1 μ F \pm 20%, 10V X5R ceramic capacitors (0402) TDK C1005X5R1A104M
C14, C16, C18, C19, C20, C38	0	Not installed (0402)
C30, C31, C35, C36, C37, C61	6	2.2 μ F \pm 20%, 6.3V X5R ceramic capacitors (0603) TDK C1608X5R0J225M

DESIGNATION	QTY	DESCRIPTION
C32, C34, C40, C41, C45, C47	0	Not installed (0603)
C39, C58	2	4.7 μ F \pm 20%, 6.3V X5R ceramic capacitors (0603) TDK C1608X5R0J475M
C42, C43, C54	3	0.01 μ F \pm 20%, 25V X7R ceramic capacitors (0402) TDK C1005X7R1E103M
C46, C59	2	1.0 μ F \pm 20%, 6.3V X5R ceramic capacitor (0402) TDK C1005X5R0J105M
C48, C49	2	18pF \pm 5%, 50V C0G ceramic capacitors (0402) TDK C1005C0G1H180J

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Component List (continued)

DESIGNATION	QTY	DESCRIPTION
C60	1	10 μ F \pm 20%, 4V X5R ceramic capacitor (0603) TDK C1608X5R0G106M
D1	1	Dual Schottky diode (SOT23) Zetex BAS70-04
J1	1	Dual-row, 40-pin header
JU1, JU7, JU8	0	Not installed
JU2, JU4, JU5, JU6, JU9, JU10, JU11	6	Jumper, 3-pin headers
L1-L4	4	EMI filters Murata NFM41PC204F1H3B
R1, R8, R13-R24, R26, R32-R35	0	Not installed (0603)
R2, R11, R12	0	Not installed (0402)
R3, R4	2	75 Ω \pm 0.1% resistors (0603) IRC PFC-W0603R-03-75R0-B
R5, R6	2	1.0k Ω \pm 5% resistors (0402)
R7, R9	2	49.9 Ω \pm 0.1% resistors (0603) IRC PFC-W0603R-03-49R9-B
R10	1	10k Ω potentiometer, 12 turn, 1/4in
R27	1	51.1 Ω \pm 1% resistor (0603)
R30, R31	2	110 Ω \pm 0.1% resistors (0603) IRC PFC-W0603R-03-1100-B
RA1-RA4	4	220 Ω \pm 5% resistor arrays Panasonic EXB-2HV-221J

DESIGNATION	QTY	DESCRIPTION
T1, T2	2	1:1 RF transformers Mini-Circuits ADT1-1WT
T3	1	2:1 RF transformer Mini-Circuits T2-1T-KK81
TP1-TP5	5	Test points (black)
CLOCK4	0	Not installed (SMA)
CLOCK, AINP, AINN, ACOM	4	SMA PC-mount connectors
U1	1	Maxim MAX1211ETL (TQFN-40)
U2	1	Low-voltage 16-bit register (48-pin TSSOP) Texas Instruments SN74AVC16374DGG
U3	0	Not installed (5-pin SC70)
U4	1	TinyLogic UHS buffer (5-pin SC70) Fairchild NC7SZ125P5
U5	0	Not installed (8-pin SO)
U6	1	TinyLogic dual UHS inverter (6-pin SC70) Fairchild NC7WZ04P6
None	6	Shunts
None	1	MAX1211 PC board

Component Suppliers

SUPPLIER	PHONE	FAX	WEBSITE
AVX	843-946-0238	843-626-3123	www.avxcorp.com
Fairchild	888-522-5372	—	www.fairchildsemi.com
IRC	361-992-7900	361-992-3377	www.irctt.com
Mini-Circuits	718-934-4500	718-332-4661	www.minicircuits.com
Murata	770-436-1300	770-436-3030	www.murata.com
Panasonic	714-373-7366	714-737-7323	www.panasonic.com
TDK	847-803-6100	847-390-4405	www.component.tdk.com
Zetex	631-543-7100	631-864-7630	www.zetex.com

Note: Indicate that you are using the MAX1211 when contacting these component suppliers.

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Evaluates: MAX1211, MAX1206-MAX1209, MAX19538

Quick Start

Recommended Equipment

- DC power supplies:
 - Digital (VLDUT) 2.0V, 50mA
 - 1.8V, 50mA for the MAX19538
 - Logic (VL) 2.0V, 100mA
 - 1.8V, 100mA for the MAX19538
 - Analog (VDUT) 3.3V, 250mA
 - Clock (VCLK) 3.3V, 200mA
- Signal generator with low phase noise and low jitter for clock input (e.g., HP 8662A, HP 8644B)
- Signal generator for analog signal input (e.g., HP 8662A, HP 8644B)
- Logic analyzer or data-acquisition system (e.g., HP 16500C, TLA621, TLA5201)
- Analog bandpass filters (e.g., Allen Avionics, K&L Microwave) for input signal and clock signal
- Digital voltmeter

Procedure

The MAX1211 EV kit is a fully assembled and tested surface-mount board. Follow the steps below for board operation. **Do not turn on power supplies or enable signal generators until all connections are completed:**

- 1) Verify that shunts are installed across pins 2-3 of jumpers JU2 (MAX1211 enabled) and JU6 (two's complement digital output), and across pins 1-2 of JU5 (differential clock input) and JU4 (fixed for MAX1211).
- 2) Verify that shunts are installed across pins 2-3 of jumpers JU9 and JU10, and across pins 1-2 of JU11.
- 3) Connect the output of the 65MHz clock generator to the input of the clock bandpass filter.
- 4) Connect the output of the clock bandpass filter to the CLOCK SMA connector.
- 5) Connect the output of the analog signal generator to the input of the signal bandpass filter.
- 6) Connect the output of the signal bandpass filter to the AINP SMA connector.
- 7) Connect the logic analyzer to the square pin header (J1). See the *Output Signal* section for bit locations and J1 header designations. The system clock is available on pin J1-3.
- 8) Connect a 3.3V, 250mA power supply to VDUT. Connect the ground terminal of this supply to the corresponding GND pad.

- 9) Connect a 2.0V (1.8V, for the MAX19538), 100mA power supply to VL. Connect the ground terminal of this supply to the GND pad.
- 10) Connect a 2.0V (1.8V, for the MAX19538), 50mA power supply to VLDUT. Connect the ground terminal of this supply to the GND pad.
- 11) If evaluating the single-ended clock mode, connect a 3.3V, 200mA power supply to VCLK. Connect the ground terminal of this supply to the corresponding GND pad. If evaluating the differential clock mode, short VCLK to GND.
- 12) Turn on the 3.3V power supplies.
- 13) Turn on the 2.0V power supplies.
- 14) Enable the signal generators. Set the clock signal generator for an output amplitude of 2V_{P-P} or higher (10dBm or higher) and the frequency (f_{CLK}) to 65MHz. Set the analog input signal generators for an output amplitude of $\leq 1V_{P-P}$ and to the desired frequency. The two signal generators should be synchronized to each other. Adjust the input signal level to overcome cable and bandpass filter losses.
- 15) Enable the logic analyzer.
- 16) Collect data using the logic analyzer.

Detailed Description

The MAX1211 EV kit is a fully assembled and tested circuit board that contains all the components necessary to evaluate the performance of the MAX1211, MAX1206-MAX1209 and the MAX19538. Data generated by the MAX1211 is captured on a single 12-bit bus. The EV kit comes with the MAX1211 installed, which can be evaluated with a maximum clock frequency (f_{CLK}) of 65MHz. The MAX1211 accepts differential or single-ended analog input signals and differential or single-ended clock signals. With the proper board configuration (as specified below), the ADC can be evaluated with both types of signals by supplying only one single-ended analog signal to the EV kit.

The EV kit is designed as a four-layer PC board to optimize the performance of the MAX1211. For simple operation, the EV kit is specified to have 3.3V and 2.0V power supplies applied to analog and digital power planes, respectively. However, the digital plane can be operated down to 1.7V without compromising the board's performance. The logic analyzer's threshold must be adjusted accordingly.

Access to the digital outputs is provided through connector J1. The 40-pin connector easily interfaces directly with a user-provided logic analyzer or data-acquisition system. The DAV output clock signal is available at

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pin J1-3 (CLK), which can be used to synchronize the output data to the logic analyzer.

Power Supplies

The MAX1211 EV kit requires separate analog and digital power supplies for best performance. Separate 3.3V power supplies are used to power the analog portion of the MAX1211 (VDUT) and the clock-shaping circuit (VCLK). To evaluate the clock-shaping circuit, 3.3V must be supplied to VCLK. When evaluating the differential clock, reduce interference from the unused clock-shaping circuit by shorting VCLK to GND. Separate 2.0V power supplies are used to power the digital portion of the MAX1211 (VLDUT) and the buffer/driver (VL). The digital portions of the EV kit operate with voltage supplies as low as 1.7V and as high as 3.6V.

Clock

The MAX1211 allows for either differential or single-ended signals to drive the clock inputs. The MAX1211 EV kit supports both methods.

In single-ended operation, the signal is applied to the ADC through a buffer (U6). In differential mode, an on-board transformer takes the single-ended analog input and generates a differential analog signal at the ADC's input pins.

MAX1211 Clock Input

The MAX1211 is capable of accepting either differential or single-ended clock input signals. Jumper JU5 controls this feature. See Table 1 for jumper settings.

Transformer-Coupled Clock

A single-ended signal can be converted to a differential signal through transformer T3. In this mode, diode D1 limits the amplitude of the clock signal, thereby overdriving the CLOCK SMA input. This can increase the slew rate of the differential signal, thereby reducing clock jitter. See Table 2 for clock-drive jumper settings. Ensure that jumper JU5 (see the *MAX1211 Clock Input* section) is set correctly.

Clock-Shaping Circuit with Variable Duty Cycle

An on-board, variable duty cycle, clock-shaping circuit generates a single-ended clock signal from an AC-coupled sine wave applied to the CLOCK SMA connector.

Table 1. MAX1211 Clock Input Settings (JU5)

SHUNT POSITION	MAX1211 CLK TYP PIN	MAX1211 CLOCK INPUT
1-2*	Connected to VLDUT	Differential
2-3	Connected to GND	Single ended

*Default configuration: JU5 (1-2).

Measure the clock signal at pin 2 of JU7 and adjust potentiometer R10 to obtain the desired duty cycle. See Table 2 for shunt positions.

Input Signal

The MAX1211 accepts differential or single-ended analog input signals. However, the EV kit requires only a single-ended analog input signal. Because the amplitude of the received signal at the ADC depends on the actual cable loss and bandpass filter loss; account for these losses when configuring the signal input generator.

Direct-Connect Single-Ended Input

To evaluate the MAX1211 with a single-ended input signal directly connected to the ADC input terminal, modify the EV kit as follows:

- 1) Remove transformers T1 and T2.
- 2) Remove resistor R3.
- 3) Short resistor R20.
- 4) Install a 0.1 μ F capacitor at the location designated by R14.
- 5) Connect the input signal source to AINP.

MAX1211 Power-Down

Jumper JU2 controls the power-down function of the MAX1211 only. Other ICs on the MAX1211 EV kit continue to draw quiescent current from the power supplies. See Table 3 for power-down jumper settings.

Reference Voltage

The MAX1211 requires an input voltage reference at its REFIN pin to set the full-scale analog signal voltage input. The ADC has a stable on-chip voltage reference of 2.048V, which can be accessed at REFOUT. The EV kit was designed to use the on-chip voltage reference by shorting REFIN to REFOUT through resistor R12.

The user can externally adjust the reference level, and hence the full-scale range, by cutting the trace-short

Table 2. CLOCK SMA Drive Settings

JUMPER	SHUNT POSITION	DESCRIPTION
JU9	1-2	Single-ended clock mode (see the <i>Clock-Shaping Circuit with Variable Duty-Cycle</i> section)
JU10	1-2	
JU11	2-3	
JU9*	2-3	Differential lock mode; a single-ended signal is converted to a differential signal that drives the MAX1211 clock inputs
JU10*	2-3	
JU11*	1-2	

*Default configuration: JU9 (2-3), JU10 (2-3), JU11 (1-2).

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resistor R12 and installing resistors at locations R2 and R12 (located on the board's component side). Calculate the resistor values using the following equation:

$$R_{12} = R_2 \left(\frac{V_{REFOUT} - 1}{V_{REFIN}} \right)$$

where:

R2 = 10kΩ, ±1%.

VREFOUT = 2.048V.

VREFIN = desired REFIN voltage.

Alternatively, resistors R12 and R2 can be opened, and the ADC's full-scale range can be set by applying a stable, low-noise, external voltage reference directly at the REFIN pad.

Output Coding

The digital output coding of the MAX1211 can be chosen to be either in two's complement format or Gray code by configuring jumper JU6. See Table 4 for shunt positions.

Output Signal

The MAX1211 features a 12-bit, parallel, CMOS-compatible output bus. The outputs of the ADC are fed into a buffer capable of driving large capacitive loads, which may be present at the logic analyzer connection. The outputs of the buffer are connected to a 40-pin header (J1), located on the right side of the EV kit, where the user can connect a logic analyzer or data-acquisition system. See Table 5 for bit locations of header J1.

Duty-Cycle Equalizer (DCE)

A 50% duty cycle applied to the clock inputs of the MAX1211 EV kit is recommended to improve the dynamic performance. Enabling the DCE function can correct clock signals with less than ideal clock duty cycles ranging from 40% to 60%. Jumper JU4 configures the DCE function of the MAX1211 EV kit. See Table 6 for shunt positions.

Evaluating the MAX1206-MAX1209, MAX19538

To evaluate the MAX1206/MAX1207/MAX1208, MAX1209, or the MAX19538 remove IC U1 from the EV kit and install a free sample of the desired ADC.

Table 3. Power-Down Settings (JU2)

SHUNT POSITION	MAX1211 PD PIN	MAX1211 POWER-DOWN STATUS
1-2	Connected to VLDUT	Powered down
2-3*	Connected to GND	Normal operation

*Default configuration: JU2 (2-3).

Table 4. Output Code Settings (JU6)

SHUNT POSITION	MAX1211 G/T PIN	OPERATION
1-2	Connected to VLDUT	Digital output in Gray code
2-3*	Connected to GND	Digital output in two's complement

*Default configuration: JU6 (2-3).

Table 5. Output Bit Locations (J1)

CLOCK	DOR	BIT D11	BIT D10	BIT D9	BIT D8	BIT D7	BIT D6	BIT D5	BIT D4	BIT D3	BIT D2	BIT D1	BIT D0
J1-3 CLK ↑	J1-7	J1-11	J1-13	J1-15	J1-17	J1-19	J1-21	J1-23	J1-25	J1-27	J1-29	J1-31	J1-33

Table 6. Duty-Cycle-Equalizer Settings (JU4)

SHUNT POSITION	DCE PIN	DUTY-CYCLE EQUALIZER
1-2*	Connected to VDUT	Enabled
2-3	Connected to GND	Disabled

*Default configuration: JU4 (1-2).

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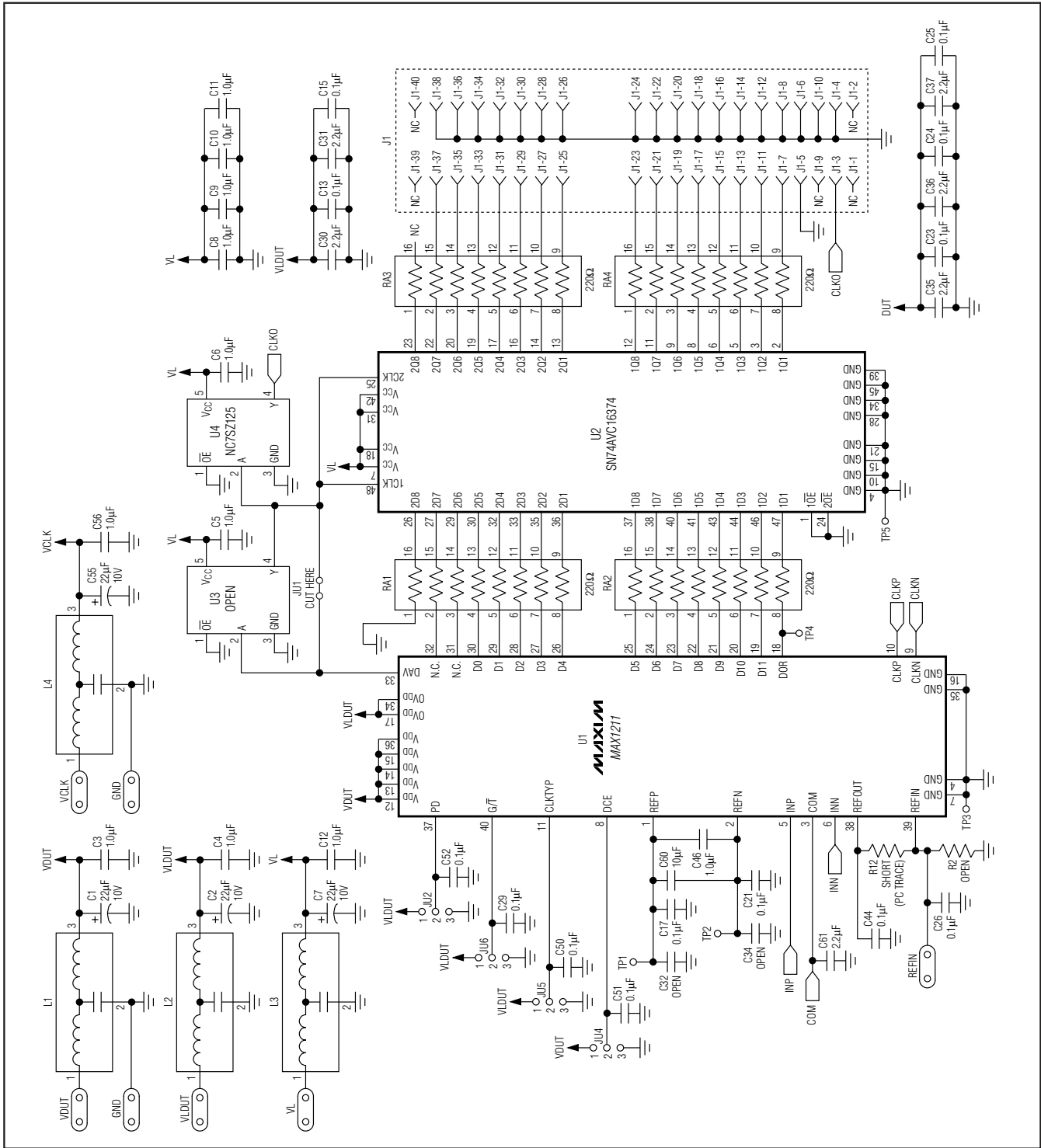


Figure 1. MAX1211 EV Kit Schematic (Sheet 1 of 2)

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Evaluates: MAX1211, MAX1206-MAX1209, MAX19538

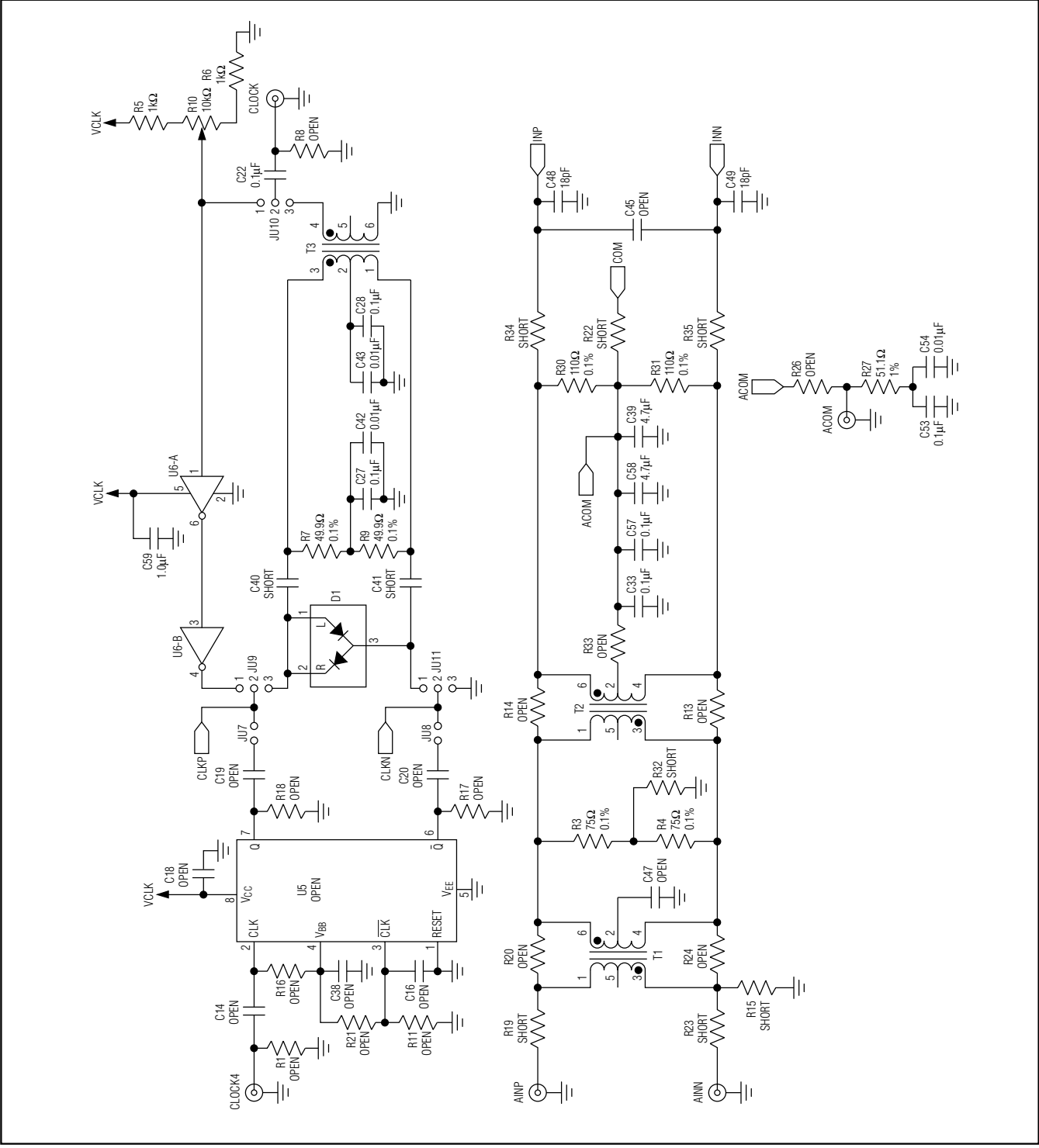


Figure 1. MAX1211 EV Kit Schematic (Sheet 2 of 2)

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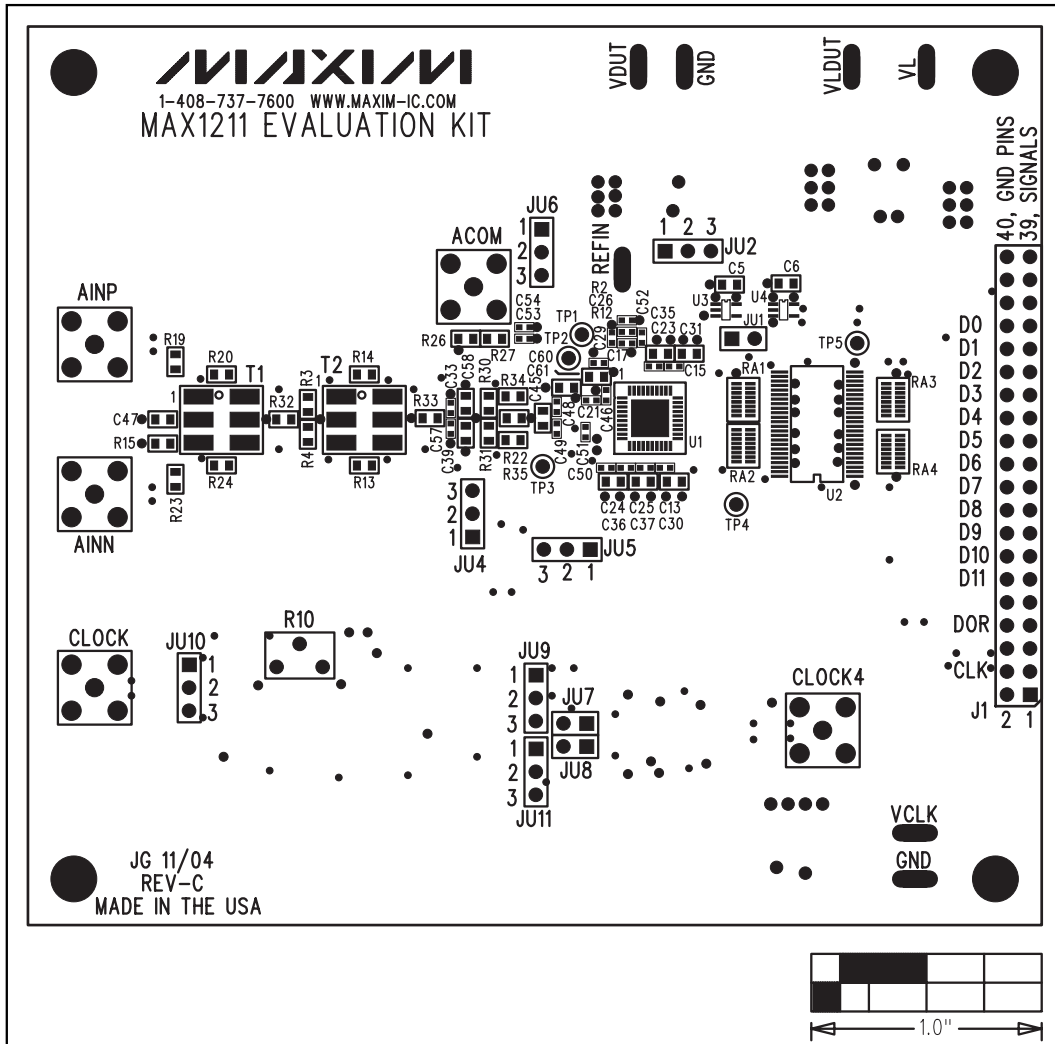


Figure 2. MAX1211 EV Kit Component Placement Guide—Component Side

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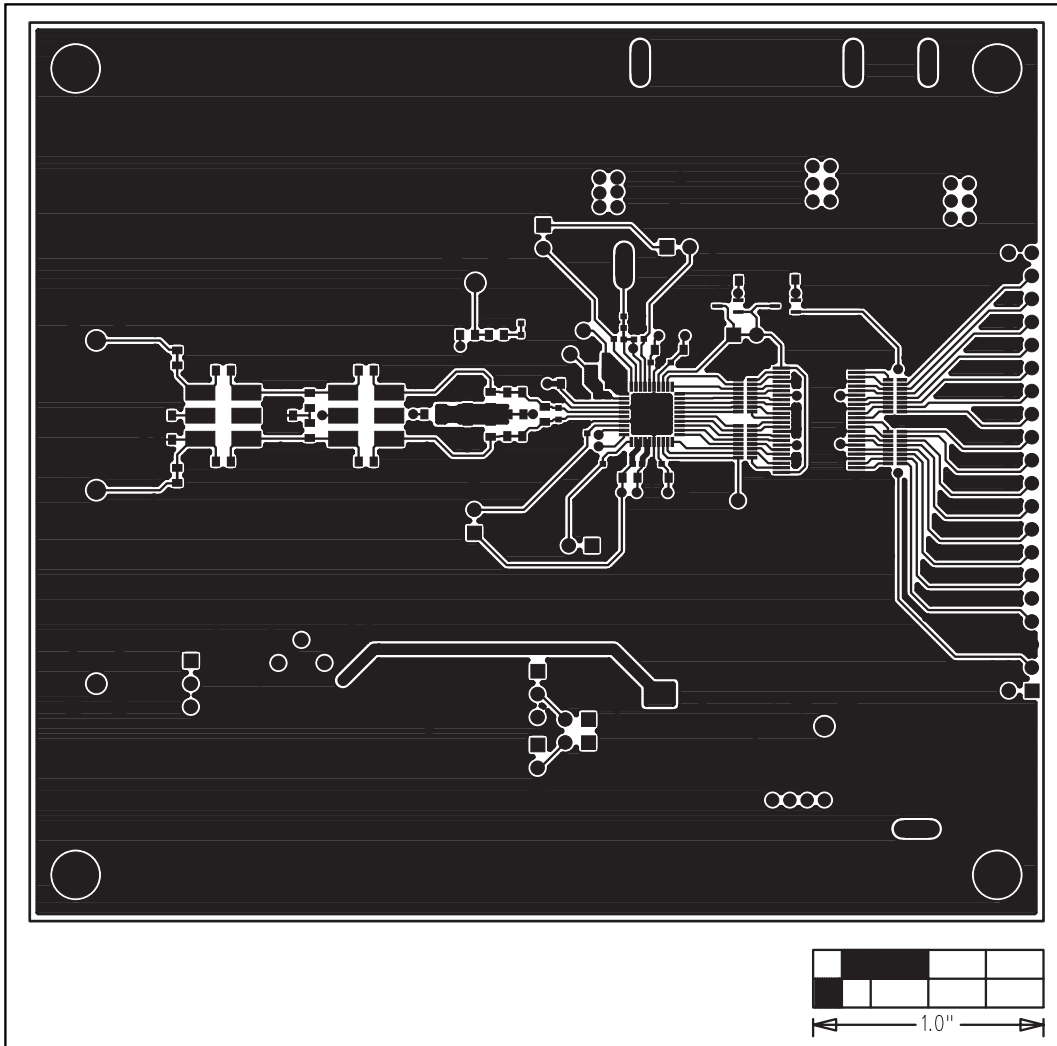


Figure 3. MAX1211 EV Kit PC Board Layout—Component Side

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Evaluates: MAX1211, MAX1206-MAX1209, MAX19538

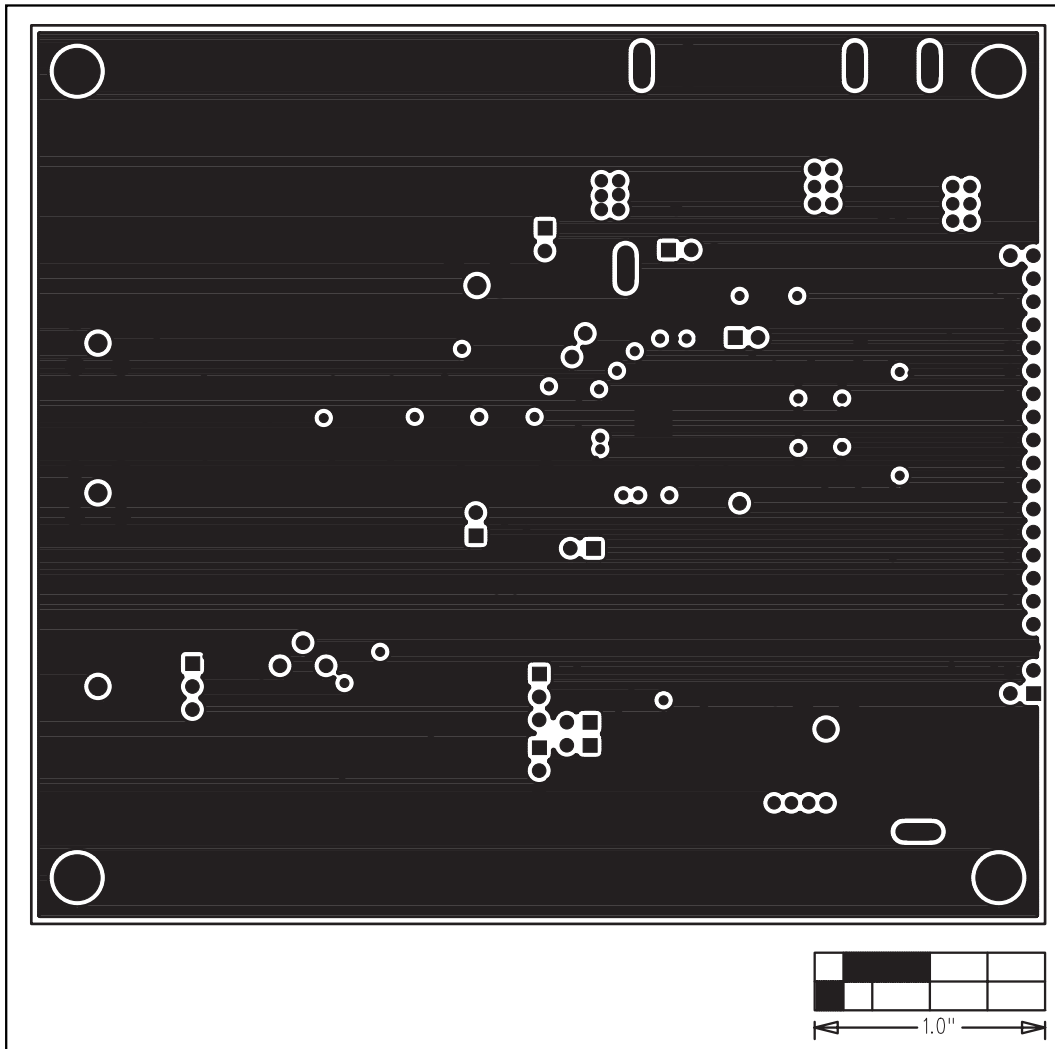


Figure 4. MAX1211 EV Kit PC Board Layout (Inner Layer 2)—Ground Planes

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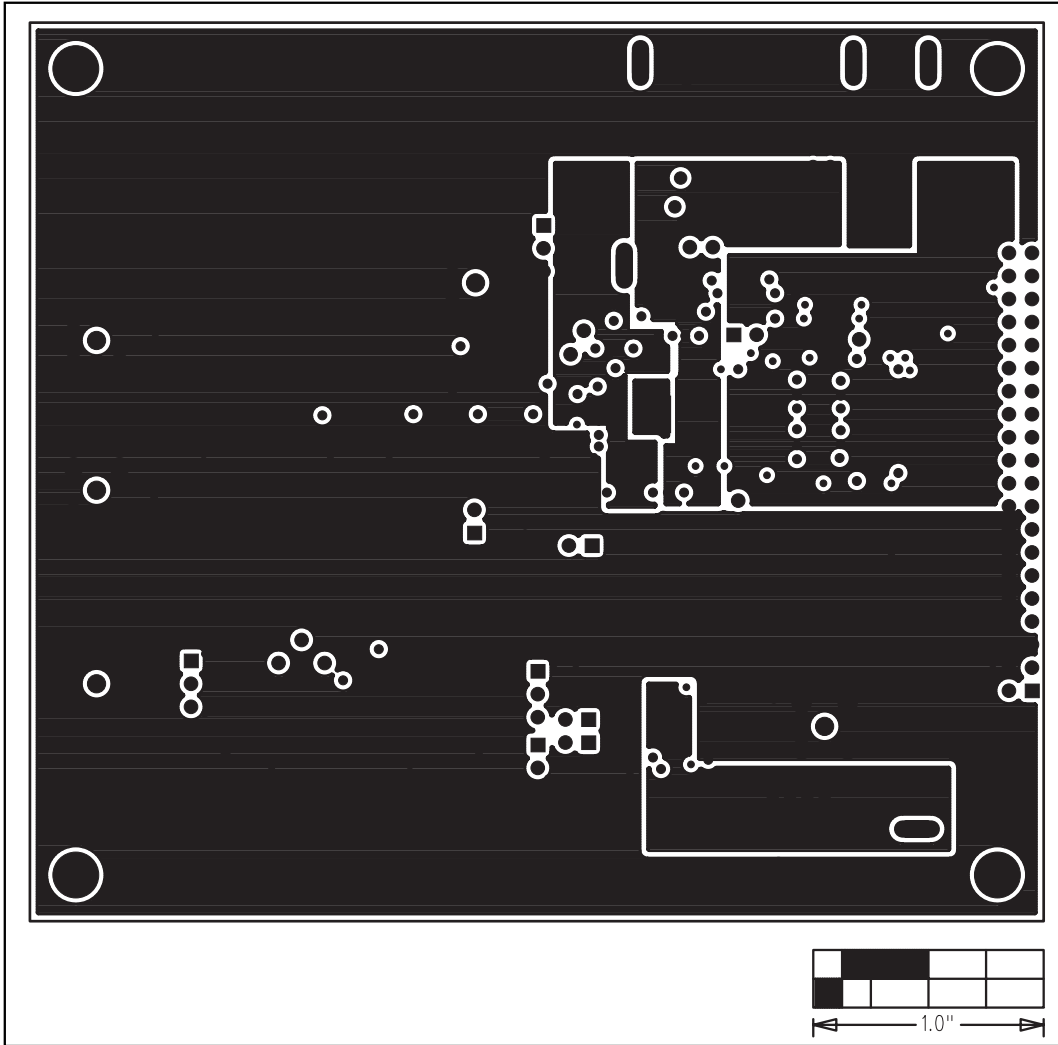


Figure 5. MAX1211 EV Kit PC Board Layout (Inner Layer 3)—Power Planes

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Evaluates: MAX1211, MAX1206-MAX1209, MAX19538

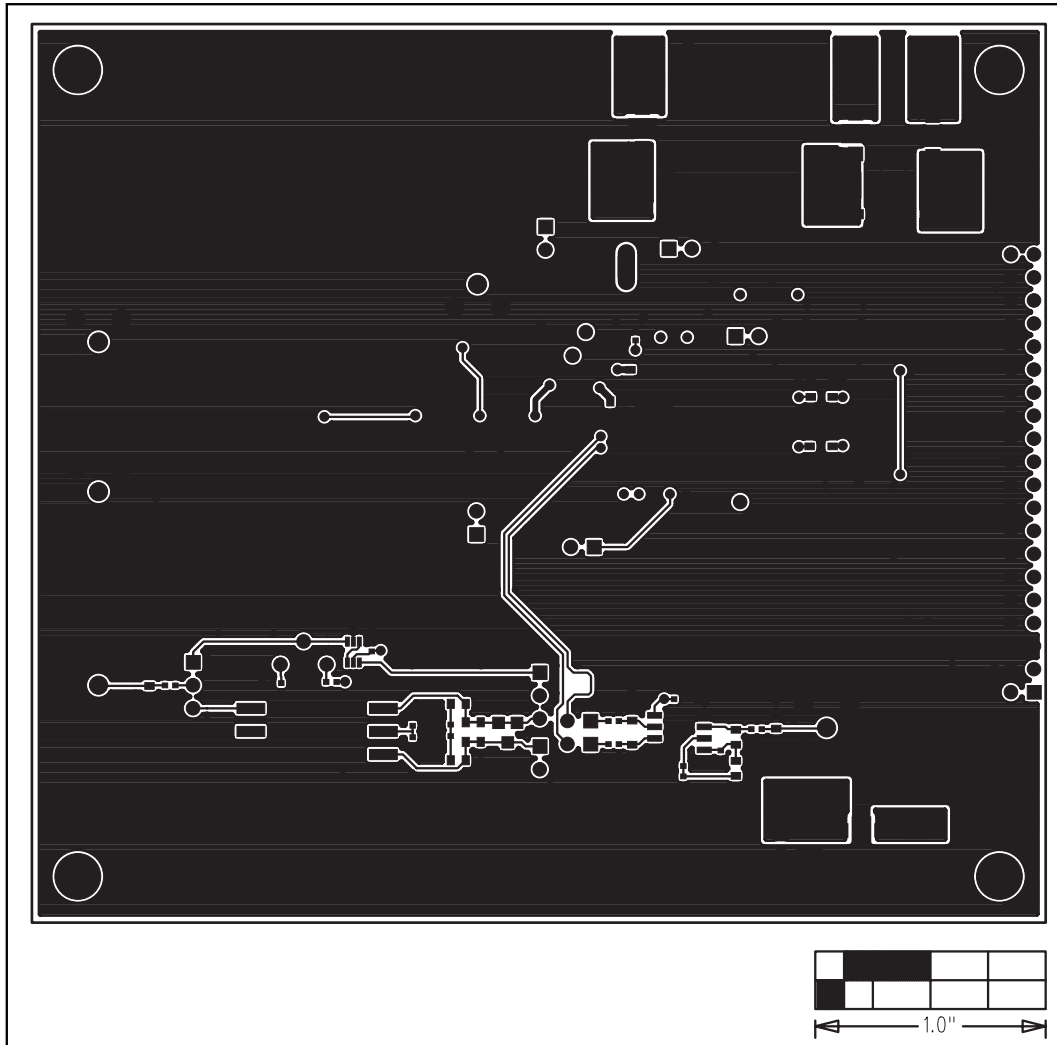


Figure 6. MAX1211 EV Kit PC Board Layout—Solder Side

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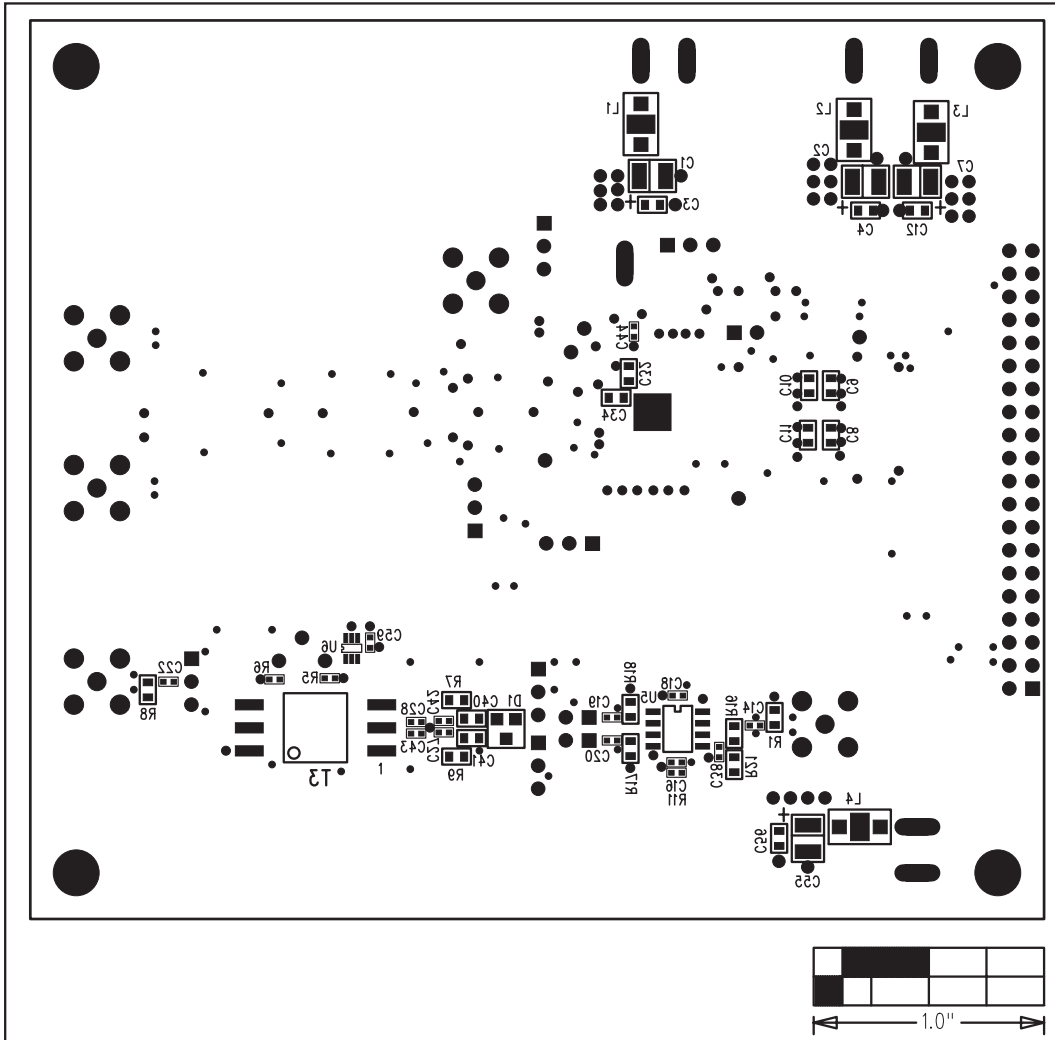


Figure 7. MAX1211 EV Kit Component Placement Guide—Solder Side

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