19-4595; Rev 3; 8/11

EVALUATION KIT AVAILABLE

Multiprotocol, Pin-Selectable Data Interface Chipset

General Description

The MAX13171E along with the MAX13173E/MAX13175E, form a complete pin-selectable data terminal equipment (DTE) or data communication equipment (DCE) interface port that support the V.28 (RS-232), V.10/V.11 (RS-449/V.36, RS-530, RS-530A, X.21), and V.35 protocols. The MAX13171E transceivers carry the high-speed clock and data signals, while the MAX13173E transceivers carry the control signals. The MAX13171E can be terminated by the MAX13175E pin-selectable resistor termination network. The MAX13175E contains six pin-selectable, multiprotocol cable termination networks.

The MAX13171E/MAX13173E have an internal charge pump and low-dropout transmitter output stages that allow V.10-, V.11-, V.28-, and V.35-compliant operation from a single supply. The MAX13171E/MAX13173E feature a no-cable mode that reduces supply current and disables all transmitter and receiver outputs (high impedance). Short-circuit current limiting and thermal shutdown circuitry protects the receiver and transmitter outputs against excessive power dissipation. The MAX13171E/MAX13173E have extended ESD protection for all the transmitter outputs and receivers inputs.

The MAX13171E/MAX13173E/MAX13175E operate over the +3.135V to +5.5V supply range and are available in 5mm x 7mm, 38-pin TQFN packages. These devices operate over the -40°C to +85°C extended temperature range.

Applications

Data Networking

PCI Cards

CSU and DSU

Telecommunication Equipment

Data Routers

Data Switches

Features

- **Supports V.28 (RS-232), V.10 (RS-423), V.11 (RS-449/V.36, RS-530, RS-530A, X.21) and V.35 Protocols**
- **Pin-Selectable Cable Termination Using the MAX13175E**
- **Pin-Selectable DCE/DTE Configurations**
- **20/40Mbps (max) Data Rate in RS-449, RS-530, RS-530A, X.21, and V.35**
- **True Fail-Safe Receivers while Maintaining V.11 and V.35 Compatibility**
- **Operates Over a Wide +3.135V to +5.5V V_{CC} Supply Range**
- **Flexible V_L Logic Reference Input Allows Interfacing Down to 1.62V**
- **Extended ESD Protection for All the Transmitter Outputs and Receivers Inputs to GND**
- **Small, 5mm x 7mm, 38-Pin TQFN Package**

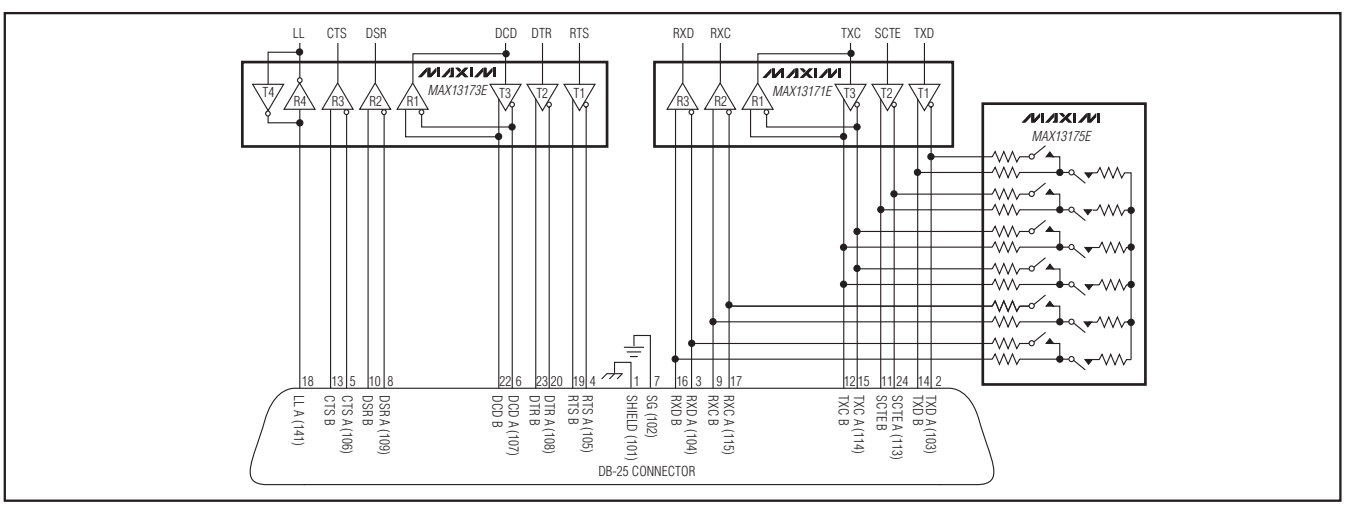
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX13171EETU+	-40°C to +85°C	38 TQFN-EP*
MAX13173EETU+	-40°C to +85°C	38 TQFN-EP*
MAX13175EETU+	-40°C to +85°C	38 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Multiprotocol, Pin-Selectable Data Interface Chipset

ABSOLUTE MAXIMUM RATINGS

(All voltages to GND, unless otherwise noted.)

Supply Voltages
- V_{CC} ..... -0.3V to +6V
- V_L ..... -0.3V to +6V
- V_{EE} ..... +0.3V to -7.1V
- V_{DD} ..... -0.3V to +7.1V
- V_{DD} to V_{CC} .....-0.3V to +6V

Logic-Input Voltages
- M0, M1, M2, DCE/$\overline{DTE}$, $\overline{LATCH}$, INVERT, T_IN..... -0.3V to +6V

Termination Network Inputs
- R_A, R_B, R_C.....-15V to +15V
- R_A to R_B (only for high-Z state) .....±14V
- R_A to R_B.....±6V
- R_A to R_C (only for high-Z state) .....±14V
- R_A to R_C.....±3V
- R_B to R_C (only for high-Z state) .....±3V

Logic-Output Voltages
- R_OUT .....-0.3V to (V_L + 0.3V)

Transmitter Outputs
- T_OUT_, T_OUT_/R_IN_ (no-cable, V.28, V.10 modes) .....-15V to +15V
- Short-Circuit Duration to GND.....Continuous

Receiver Inputs
- R_IN_, T_OUT_/R_IN .....-15V to +15V
- R_INA to R_INB, T3OUTA/R3INA to T3OUTB/R3INB .....-15V to +15V

Continuous Power Dissipation (T_A = +70°C)
- 38-Pin TQFN (derate 35.7mW/°C above +70°C) 2857mW

Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN
- Junction-to-Ambient Thermal Resistance (θ_{JA}) .....28°C/W
- Junction-to-Case Thermal Resistance (θ_{JC}) .....1°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **http://www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAX13171E ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.135V to +5.5V, V_L = +1.62V to +5.5V, C1 = C2 = 1µF, C3 = C4 = C5 = 4.7µF (Figure 15), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +1.8V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Operating Range	V_{CC}		3.135		5.5	V
V_L Operating Range	V_L		1.62		V_{CC}	V
V_L Supply Current	I_L	All inputs connected to GND, all receiver outputs low, V_L = +5.5V		550	800	µA
V_{CC} Supply Current (DCE Mode) (Digital Inputs = GND or V_{CC}) (Transmitter Outputs Static)	I_{CC}	RS-530, RS-530A, X.21, V.36/RS-449 mode (V.11), no load		15	28	mA
		RS-530, RS-530A, X.21, V.36/RS-449 mode (V.11), full load		150	200	mA
		V.35 mode, no load		21	38	mA
		V.35 mode, full load		150	210	mA
		V.28 mode, no load		15	30	mA
		V.28 mode, full load		28	42	mA
		No-cable mode		0.01	10	µA
Internal Power Dissipation (DCE Mode)(Static)	P_D	RS-530, RS-530A, X.21, V.36/RS-449 mode (V.11), full load		100		mW
		V.35 mode, full load		500		
		V.28 mode, full load		70		

MAX13171E ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.135V to +5.5V, V_L = +1.62V to +5.5V, C1 = C2 = 1µF, C3 = C4 = C5 = 4.7µF (Figure 15), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +1.8V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Positive Charge-Pump Output Voltage	V_{DD}	V.28, V.35 modes, no load (Note 3)		5.93	7.1	V
		V.28 mode, full load (Note 3)	5.6	5.86		
		V.35 mode, full load (Note 3)	4.6	5.1		
		RS-530, RS-530A, X.21, V.36/RS-449 mode (V.11) (Note 3)	4.9	5.26	5.7	
		No-cable mode		V_{CC}		
Negative Charge-Pump Output Voltage	V_{EE}	V.28, V.35 modes, no load (Note 3)		-5.89		V
		V.28 mode, full load (Note 3)		-5.74	-5.4	
		V.35 mode, full load, Note 3		-4.46	-3.8	
		RS-530, RS-530A, X.21, V.36/RS-449 mode (V.11) (Note 3)	-4.84	-4.47	-4.16	
		No-cable mode		0		
Charge-Pump Enable Time		Time until all V_{DD} and V_{EE} specifications meet		< 1		ms
Thermal Shutdown Protection	THSD			+145		°C
LOGIC INPUTS (M0, M1, M2, DCE/$\overline{DTE}$, T1IN, T2IN, T3IN)						
Input High Voltage	V_{IH}		0.66 x V_L			V
Input Low Voltage	V_{IL}				0.33 x V_L	V
Logic-Input Current	I_{IN}	T1IN, T2IN, T3IN	-1		+1	µA
Pullup Resistor	R_{PUIN}	M0, M1, M2, DCE/$\overline{DTE}$ to V_L	50	100	170	kΩ
LOGIC OUTPUTS (R1OUT, R2OUT, R3OUT)						
Output High Voltage	V_{OH}	I_{SOURCE} = 4mA	0.66 x V_L			V
Output Low Voltage	V_{OL}	I_{SINK} = 4mA			0.33 x V_L	V
Output Pullup Resistor	R_{PUY}	No-cable mode (to V_L)		71.4		kΩ
V.11 TRANSMITTER						
Open-Circuit Differential Output Voltage	V_{ODO}	Open circuit, R = 1.95kΩ, Figure 1	-V_{CC}		+V_{CC}	V
Loaded Differential Output Voltage	V_{ODL}	R = 50Ω, Figure 1	0.5 x V_{ODO}			V
		R = 50Ω, Figure 1	I2I			
Change in Magnitude of Output Differential Voltage	$\lvert\Delta V_{OD}\rvert$	R = 50Ω, Figure 1			0.2	V
Common-Mode Output Voltage	V_{OC}	R = 50Ω, Figure 1			3.0	V
Change in Magnitude of Common-Mode Output Voltage	$\lvert\Delta V_{OC}\rvert$	R = 50Ω, Figure 1 (Note 3)			0.2	V
Short-Circuit Current	I_{SC}	V_{OUT} = GND			150	mA
Rise Time	t_r	Figures 2, 6		4.5		ns
Fall Time	t_f	Figures 2, 6		6.5		ns

MAX13171E ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.135V to +5.5V, V_L = +1.62V to +5.5V, C1 = C2 = 1µF, C3 = C4 = C5 = 4.7µF (Figure 15), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +1.8V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Transmitter Input to Output Propagation Delay (Figures 2, 6)	t_{PHL}, t_{PLH}	Figures 2, 6		22	28	ns
		$V_L \geq$ +3V, Figures 2, 6		20	25	
Data Skew	$\lvert t_{PHL}-t_{PLH} \rvert$	Figures 2, 6 (Note 3)			2	ns
Channel-to-Channel Skew	t_{SKEW}	Figures 2, 6 (Notes 3, 4)			3	ns
V.11 RECEIVER						
Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ +7V	-200		-50	mV
Input Hysteresis	ΔV_{TH}	-7V ≤ V_{CM} ≤ +7V		15		mV
Receiver Input Current	I_{IN}	-10V ≤ $V_{A,B}$ ≤ +10V	-0.66		+0.66	mA
Receiver Input Resistance	R_{IN}	-10V ≤ $V_{A,B}$ ≤ +10V	15	30		kΩ
Rise or Fall Time	t_r, t_f	Figures 2, 7		3		ns
Receiver Input to Output Delay	t_{PHL}, t_{PLH}	Figures 2, 7			2.5	ns
Data Skew	$\lvert t_{PHL}-t_{PLH} \rvert$	Figures 2, 7 (Note 3)			3	ns
Channel-to-Channel Skew	t_{SKEWR}	Figures 2, 7 (Notes 3, 4)			3	ns
V.35 TRANSMITTER						
Differential Output Voltage	V_{OD}	Full load, -4V < V_{CM} < +4V, Figure 3	±0.44	±0.55	±0.66	V
Output High Current	I_{OH}	$V_{A,B}$ = 0V	-13	-11	-9	mA
Output Low Current	I_{OL}	$V_{A,B}$ = 0V	9	11	13	mA
Output Leakage Current	I_Z	-0.25V ≤ V_{OUT} ≤ +0.25V, power off or no-cable mode		±0.05	±5	µA
Rise or Fall Time	t_r, t_f	Figures 3, 6		5		ns
Transmitter Input to Output Delay	t_{PLH}, t_{PHL}	Figures 3, 6		19	35	ns
Data Skew	$\lvert t_{PLH} - t_{PHL} \rvert$	Figures 3, 6 (Note 3)			3	ns
Channel-to-Channel Skew	t_{SKEWR}	Figures 3, 6 (Notes 3, 4)			3	ns
V.35 RECEIVER						
Differential Threshold Voltage	V_{TH}	-2V ≤ V_{CM} ≤ +2V	-200		-50	mV
Input Hysteresis	ΔV_{TH}	-2V ≤ V_{CM} ≤ +2V		15		mV
Receiver Input Current	I_{IN}	-10V ≤ $V_{A,B}$ ≤ +10V	-0.66		+0.66	mA
Receiver Input Resistance	R_{IN}	-10V ≤ $V_{A,B}$ ≤ +10V	15	30		kΩ
Rise or Fall Time	t_r, t_f	Figures 3, 7		3		ns
Receiver Input to Output Delay	t_{PHL}, t_{PLH}	Figures 3, 7			25	ns
Data Skew	$\lvert t_{PHL}- t_{PLH} \rvert$	Figures 3, 7 (Note 3)			3	ns
Channel-to-Channel Skew	t_{SKEWR}	Figures 3, 7 (Notes 3, 4)			3	ns
V.28 TRANSMITTER						
Output-Voltage Swing	$\lvert V_{OD} \rvert$	Open circuit			7.1	V
		R_L = 3kΩ	5	6		
Short-Circuit Current	I_{OH}				85	mA

MAX13171E ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.135V to +5.5V, V_L = +1.62V to +5.5V, C1 = C2 = 1µF, C3 = C4 = C5 = 4.7µF (Figure 15), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +1.8V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Leakage Current	I_Z	-0.25V ≤ V_{OUT} ≤ +0.25V, power off or no-cable mode		±0.05	±5	µA
Output Slew Rate	$SR_{R/F}$	R_L = 3kΩ, C_L = 2500pF (swing in ±3V), Figures 4, 10	4		30	V/µs
Transmitter Input to Output Delay	t_{PHL}, t_{PLH}	R_L = 3kΩ, C_L = 2500pF, Figures 4, 10		1	2	µs
V.28 RECEIVER						
Input Threshold Low	V_{IL}		0.8	1.2		V
Input Threshold High	V_{IH}			1.2	2	V
Input Hysteresis	V_{HYST}			0.25		V
Input Resistance	R_{IN}	-15V ≤ V_{IN} ≤ +15V	3	5	7	kΩ
Rise or Fall Time	t_r, t_f	Figures 5, 11		3		ns
Receiver Input to Output Delay	t_{PHL}, t_{PLH}	Figures 5, 11			150	ns
ESD PROTECTION						
T_OUT, T3OUT_/R1IN_, R_IN to GND		Human Body Model		±15		kV
		Air Gap Discharge IEC 61000-4-2		±12		
		Contact Discharge IEC 61000-4-2		±8		

MAX13173E ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.135V to +5.5V, V_L = +1.62V to +5.5V, C1 = C2 = 1µF, C3 = C4 = C5 = 4.7µF (Figure 15), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +1.8V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Operating Range	V_{CC}		3.135		5.5	V
V_L Operating Range	V_L		1.62		V_{CC}	V
V_L Supply Current	I_L	All inputs connected to GND, all receiver outputs low, V_L = +5.5V		680	1100	µA
V_{CC} Supply Current	I_{CC}	RS-530A, no load		11	21	mA
		RS-530, X.21, V.36/RS-449, DCE mode, INVERT = low, full load, transmitter outputs static, digital inputs = GND or V_L		41	210	mA
		V.28 mode, no load		21	38	mA
		V.28 mode, full load		42	65	mA
		No-cable mode		0.01	10	µA
Internal Power Dissipation	P_D	RS-530, X.21, V.36/RS-449; DCE mode, INVERT = low, full load		120		mW
Positive Charge-Pump Output Voltage	V_{DD}	V.28 mode, no load (Note 3)		5.9	7.1	V
		V.28 mode with full load (Note 3)	5.6	5.79		
		RS-530 mode, full load (Note 3)	4.84	5.15	5.5	
		RS-530A mode, full load		5.15		
		No-cable mode		V_{CC}		

Multiprotocol, Pin-Selectable Data Interface Chipset

MAX13173E ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.135V to +5.5V, V_L = +1.62V to +5.5V, C1 = C2 = 1µF, C3 = C4 = C5 = 4.7µF (Figure 15), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +1.8V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Negative Charge-Pump Output Voltage	V_{EE}	V.28 mode, no load (Note 3)		-5.83		V
		V.28 mode with full load (Note 3)		-5.55	-5.3	
		RS-530 mode, full load (Note 3)	-4.71	-4.44	-4.17	
		RS-530A mode, full load		-4.44		
		No-cable mode		0		
Thermal Shutdown Protection	THSD			+145		°C
Charge-Pump Enable Time		Time until all V_{DD} and V_{EE} specifications meet		< 1		ms
LOGIC INPUTS (M0, M1, M2, DCE/$\overline{DTE}$, INVERT, T1IN, T2IN, T3IN, T4IN, T5IN/R5OUT)						
Input High Voltage	V_{IH}		0.66 x V_L			V
Input Low Voltage	V_{IL}				0.33 x V_L	V
Logic-Input Current	I_{IN}	T1IN, T2IN, T3IN, T4IN	-1		+1	µA
Pullup Resistor	R_{PUIN}	M0, M1, M2, DCE/$\overline{DTE}$, INVERT to V_L	50	100	170	kΩ
LOGIC OUTPUTS (R1OUT, R2OUT, R3OUT, R4OUT, T5IN/R5OUT)						
Output High Voltage	V_{OH}	I_{SOURCE} = 4mA	0.66 x V_L			V
Output Low Voltage	V_{OL}	I_{SINK} = 4mA			0.33 x V_L	V
Output Pullup Resistor	R_{PUY}	No-cable mode (to V_L)		71.4		kΩ
V.11 TRANSMITTER (T1, T2, T3)						
Open-Circuit Differential Output Voltage	V_{ODO}	Open circuit, R = 1.95kΩ, Figure 1	-V_{CC}		+V_{CC}	V
Loaded Differential Output Voltage	V_{ODL}	R = 50Ω, Figure 1	0.5 x V_{ODO}			V
		R = 50Ω, Figure 1	|2|			
Change in Magnitude of Output Differential Voltage	$\lvert\Delta V_{OD}\rvert$	R = 50Ω, Figure 1			0.2	V
Common-Mode Output Voltage	V_{OC}	R = 50Ω, Figure 1			3.0	V
Change in Magnitude of Common-Mode Output Voltage	$\lvert\Delta V_{OC}\rvert$	R = 50Ω, Figure 1 (Note 3)			0.2	V
Short-Circuit Current	I_{SC}	V_{OUT} = GND			150	mA
Output Leakage Current	I_Z	-0.25V ≤ V_{OUT} ≤ +0.25V, power-off or no-cable mode		±0.05	±5	µA
Rise Time	t_r	Figures 2, 6		4	10	ns
Fall Time	t_f	Figures 2, 6		6	10	ns
Transmitter Input to Output Prop Delay	t_{PHL}, t_{PLH}	Figures 2, 6		20	28	ns
		Figures 2, 6, V_L ≥ +3V			25	ns
Data Skew	$\lvert t_{PHL} - t_{PLH}\rvert$	Figures 2, 6 (Note 3)			2	ns
Channel-to-Channel Skew	t_{SKEW}	Figures 2, 6 (Notes 3, 4)			3	ns

MAX13173E ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.135V to +5.5V, V_L = +1.62V to +5.5V, C1 = C2 = 1µF, C3 = C4 = C5 = 4.7µF (Figure 15), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +1.8V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V.11 RECEIVER (R1, R2, R3)						
Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ +7V	-200		-50	mV
Input Hysteresis	ΔV_{TH}	-7V ≤ V_{CM} ≤ +7V		15		mV
Receiver Input Current	I_{IN}	-10V ≤ $V_{A,B}$ ≤ +10V	-0.66		+0.66	mA
Receiver Input Resistance	R_{IN}	-10V ≤ $V_{A,B}$ ≤ +10V	15	30		kΩ
Rise or Fall Time	t_r, t_f	Figures 2, 7		3		ns
Receiver Input to Output Delay	t_{PHL}, t_{PLH}	Figures 2, 7			27	ns
Data Skew	$\lvert t_{PHL} - t_{PLH} \rvert$	Figures 2, 7 (Note 3)			3	ns
Channel-to-Channel Skew	t_{SKEWR}	Figures 2, 7 (Notes 3, 4)			3	ns
V.10 TRANSMITTER (T2, T4, T5)						
Open-Circuit Output Voltage Swing	V_O	R_L = 3.9kΩ (out high)	4		6	V
		R_L = 3.9kΩ (out low)	-6		-4	
Output-Voltage Swing	V_T	R_L = 450Ω (out high)	3.6			V
		R_L = 450Ω (out low)			-3.6	
		R_L = 450Ω	0.9 x $\lvert V_O \rvert$			
Short-Circuit Current	I_{SC}	V_O = GND	-55		+55	mA
Output Leakage Current	I_Z	-0.25V ≤ V_{OUT} ≤ +0.25V, power-off or no-cable mode		±0.05	+5	µA
Rise or Fall Time	t_r, t_f	R_L = 450Ω, C_L = 100pF, Figure 8		2		µs
Transmitter Input to Output Delay	t_{PLH}, t_{PHL}	R_L = 450Ω, C_L = 100pF, Figure 8		1		µs
V.10 RECEIVER (R2, R4, R5)						
Input Threshold Voltage	V_{TH}		50		250	mV
Input Hysteresis	ΔV_{TH}			25		mV
Receiver Input Current	I_{IN}	-10V ≤ V_A ≤ +10V	-0.66		+0.66	mA
Receiver Input Resistance	R_{IN}	-10V ≤ V_A ≤ +10V	15	30		kΩ
Rise or Fall Time	t_r, t_f	Figures 5, 9		3		ns
Receiver Input to Output Delay	t_{PLH}	Figure 9		55		ns
	t_{PHL}	Figure 9		109		
Data Skew	$\lvert t_{PHL} - t_{PLH} \rvert$	Figures 5, 9 (Note 3)		60		ns
V.28 TRANSMITTER (All CHANNELS)						
Output-Voltage Swing	$\lvert V_{OD} \rvert$	Open circuit			7.1	V
		R_L = 3kΩ	5	6		
Short-Circuit Current	I_{OH}				90	mA
Output Leakage Current	I_Z	-0.25V ≤ V_{OUT} ≤ +0.25V, power-off or no-cable mode		±0.05	±5	µA

Multiprotocol, Pin-Selectable Data Interface Chipset

MAX13173E ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.135V to +5.5V, V_L = +1.62V to +5.5V, C1 = C2 = 1µF, C3 = C4 = C5 = 4.7µF, Figure 15, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +1.8V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Slew Rate	$SR_{R/F}$	R_L = 3kΩ, C_L = 2500pF (swing in ±3V) Figures 4, 10	4		30	V/µs
Transmitter Input to Output Delay	t_{PHL}, t_{PLH}	R_L = 3kΩ, C_L = 2500pF, Figures 4, 10		1	2	µs
V.28 RECEIVER (All CHANNELS)						
Input Threshold Low	V_{IL}		0.8	1.2		V
Input Threshold High	V_{IH}			1.2	2	V
Input Hysteresis	V_{HYST}			0.25		V
Input Resistance	R_{IN}	-15V ≤ V_{IN} ≤ +15V	3	5	7	kΩ
Rise or Fall Time	t_r, t_f	Figures 5, 11		3		ns
Receiver Input to Output Delay	t_{PHL}, t_{PLH}	Figures 5, 11			150	ns
ESD PROTECTION						
T_OUT, T_OUT/R_IN_, R_IN		Human Body Model		±15		kV
		Air Gap Discharge IEC 61000-4-2		±15		
		Contact Discharge		±5		

MAX13175E ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.135V to +5.5V, V_L = +1.62V to +5.5V, C1 = C2 = 1µF, C3 = C4 = C5 = 4.7µF, Figure 15, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +1.8V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Operating Range	V_{CC}		3.135		5.5	V
V_L Operating Range	V_L		1.62		V_{CC}	V
V_{DD} Operating Range	V_{DD}		4.5		7.1	V
V_{EE} Operating Range	V_{EE}		-7.1		-4	V
V_L POR Rising Threshold			0.7	1.06	1.46	V
V_{CC} POR Rising Threshold			1	1.88	2.75	V
V_{DD} Supply Current	I_{DD}	All inputs connected to GND or V_L, except no-cable mode		0.05	0.25	mA
V_{CC} Supply Current	I_{CC}	All inputs connected to GND or V_L, except no-cable mode		2.15	5.9	mA
	I_{CC_NOCAB}	V_{EE} = 0V, M[x] = 1111 (Note 5)		1.29	2.6	mA
V_L Supply Current	I_L	All inputs connected to GND or V_L	-1		+1	µA
V_{EE} Supply Current	I_{EE}	All inputs connected to GND or V_L	-3.5	-1		mA
TERMINATOR INPUTS						
Differential-Mode Impedance V.35 Mode		-2V ≤ V_{CM} ≤ +2V, all channels, Figure 12	90	104	110	Ω
Common-Mode Impedance V.35 Mode		-2V ≤ V_{CM} ≤ +2V, all channels, Figure 13	135	153	165	Ω

MAX13175E ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.135V to +5.5V, V_L = +1.62V to +5.5V, C1 = C2 = 1µF, C3 = C4 = C5 = 4.7µF, Figure 15, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +1.8V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential-Mode Impedance V.11 Mode		-7V ≤ V_{CM} ≤ +7V, all channels, except no-cable mode, Figure 12	100	104	110	Ω
		-7V ≤ V_{CM} ≤ +7V, no cable, V_{EE} = 0V, V_{AB} < 2V, Figure 12		115		
Differential Path Enable Time				50		µs
Differential Path Disable Time				300		µs
Common-Mode Path Enable Time				12		µs
Common-Mode Path Disable Time				2		µs
High-Impedance Leakage Current	I_Z	-15V ≤ V_{R_A} ≤ +15V	-50		+50	µA
LOGIC INPUTS (M0, M1, M2, $\overline{\text{LATCH}}$, DCE/$\overline{\text{DTE}}$)						
Input High Voltage	V_{IH}		0.66 x V_L			V
Input Low Voltage	V_{IL}				0.33 x V_L	V
Logic Input Current	I_{IN}	V_{IN} = GND or V_L	-1		+1	µA
ESD PROTECTION						
R_A, R_B to GND		Human Body Model		±15		kV
		Air Gap Discharge IEC 61000-4-2		±10		
		Contact Discharge IEC 61000-4-2		±6		
All Other Pins		Human Body Model		±2		kV

Note 2: All devices are 100% production tested at T_A = +85°C for the MAX13171E/MAX13173E and T_A = +25°C for the MAX13175E. Specifications over temperature are guaranteed by design.

Note 3: Guaranteed by design, not production tested.

Note 4: Output-to-output skews are evaluated as difference of propagation delays between different channels in the same condition and for the same polarity (LH or HL).

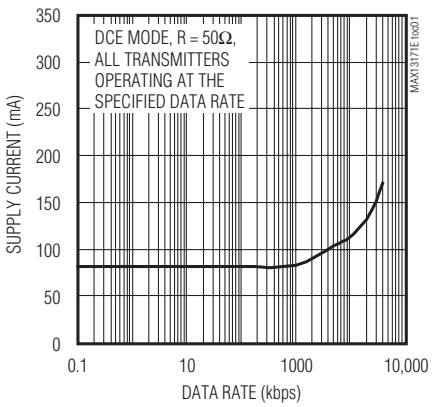
Note 5: M[x] is the input bus DTE/$\overline{\text{DCE}}$, M2, M1, M0.

Multiprotocol, Pin-Selectable Data Interface Chipset

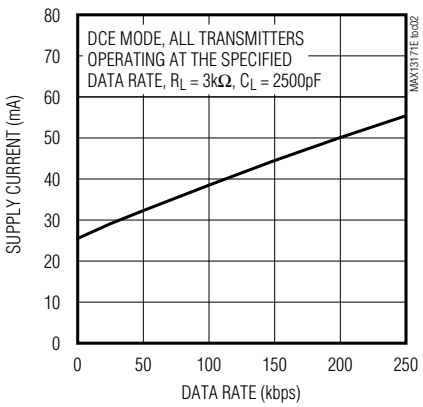
MAX13171E Typical Operating Characteristics

(V_{CC} = +3.3V, V_L = +1.8V, T_A = +25°C, unless otherwise noted.)

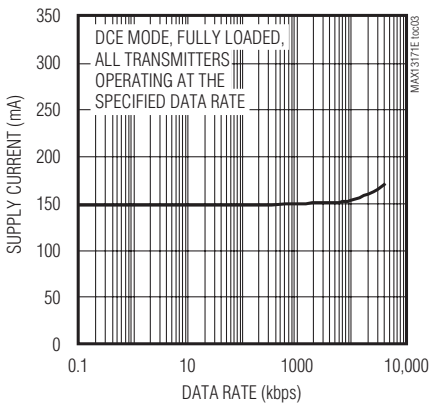
RS-530 SUPPLY CURRENT vs. DATA RATE



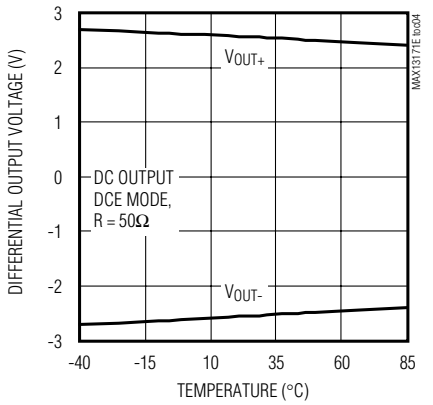
V.28 SUPPLY CURRENT vs. DATA RATE



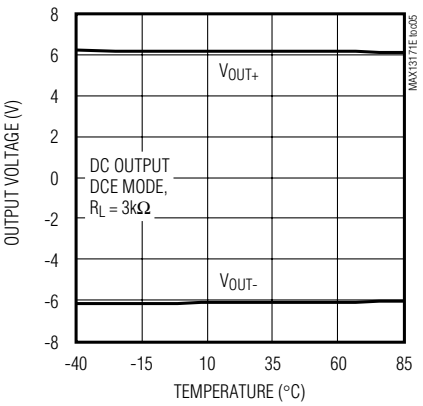
V.35 SUPPLY CURRENT vs. DATA RATE



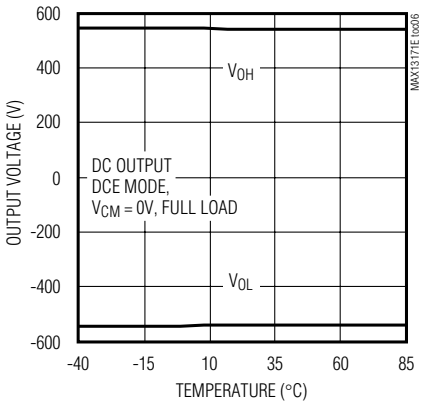
V.11 DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



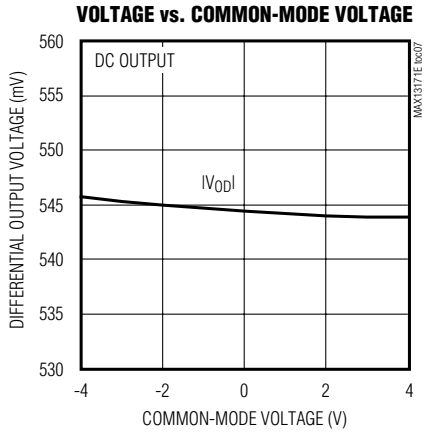
V.28 OUTPUT VOLTAGE vs. TEMPERATURE



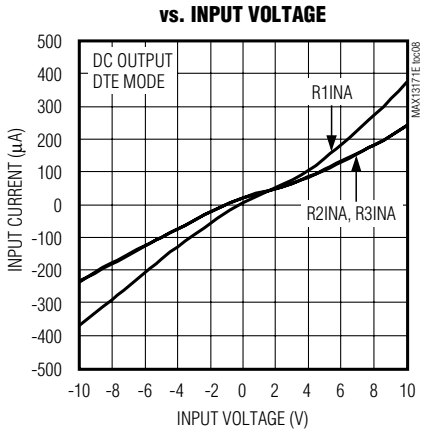
V.35 OUTPUT VOLTAGE vs. TEMPERATURE



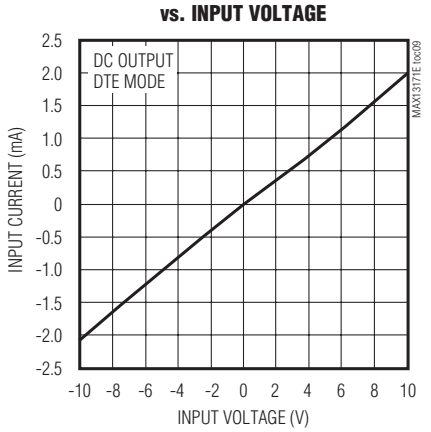
V.35 LOADED DIFFERENTIAL OUTPUT VOLTAGE vs. COMMON-MODE VOLTAGE



V.11/V.35 RECEIVER INPUT CURRENT vs. INPUT VOLTAGE



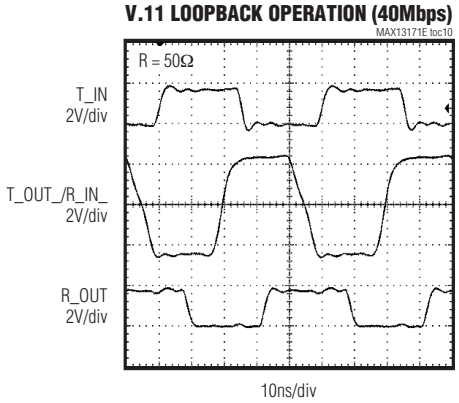
V.28 RECEIVER INPUT CURRENT vs. INPUT VOLTAGE



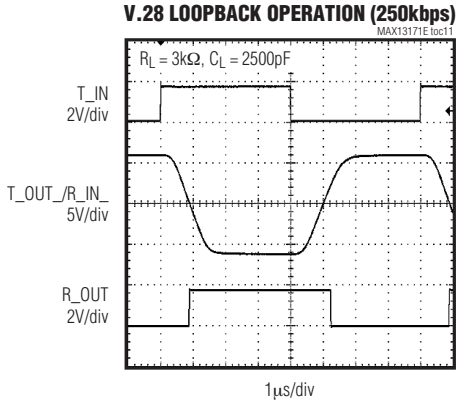
MAX13171E Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, V_L = +1.8V, T_A = +25°C, unless otherwise noted.)

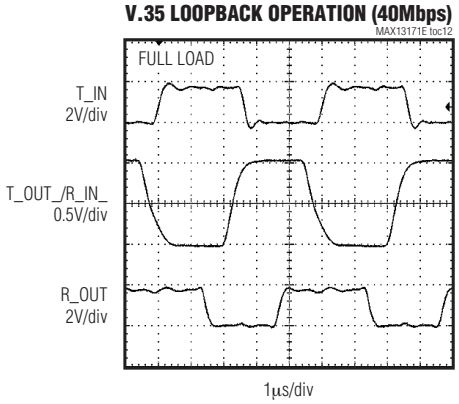
V.11 LOOPBACK OPERATION (40Mbps)



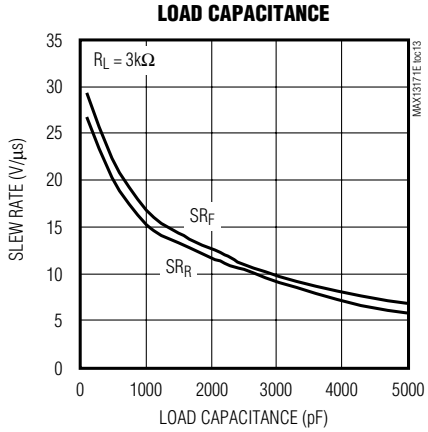
V.28 LOOPBACK OPERATION (250kbps)



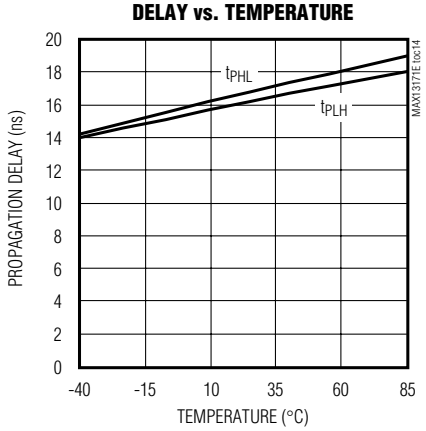
V.35 LOOPBACK OPERATION (40Mbps)



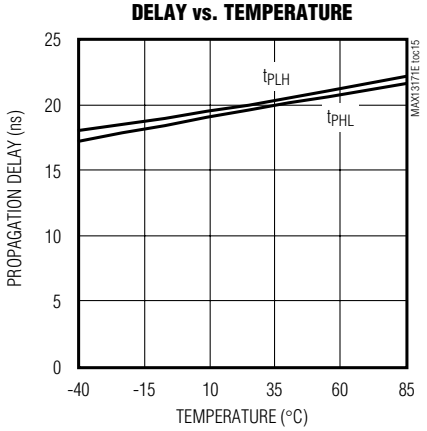
V.28 SLEW RATE vs. LOAD CAPACITANCE



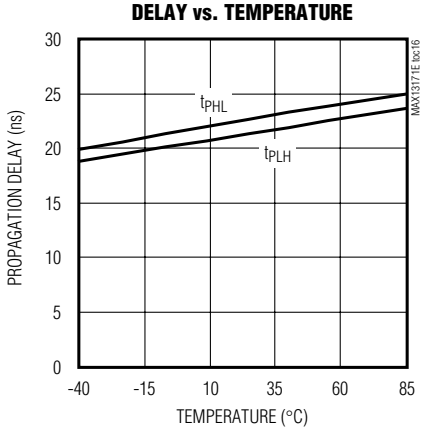
V.11/V.35 RECEIVER PROPAGATION DELAY vs. TEMPERATURE



V.11 TRANSMITTER PROPAGATION DELAY vs. TEMPERATURE



V.35 TRANSMITTER PROPAGATION DELAY vs. TEMPERATURE

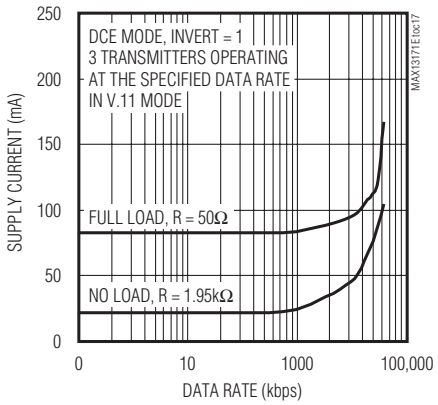


Multiprotocol, Pin-Selectable Data Interface Chipset

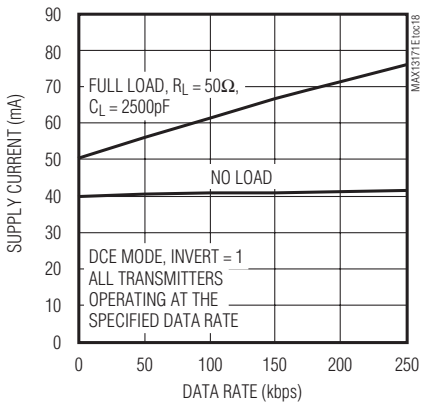
MAX13173E Typical Operating Characteristics

(V_{CC} = +3.3V, V_L = +1.8V, T_A = +25°C, unless otherwise noted.)

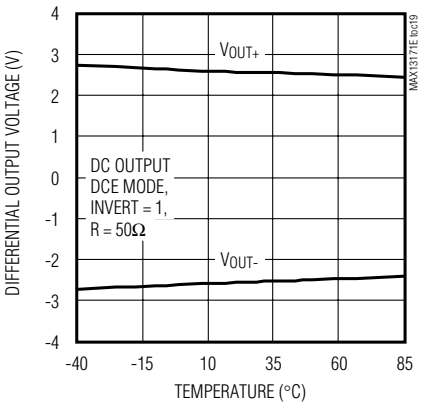
R-530 SUPPLY CURRENT vs. DATA RATE



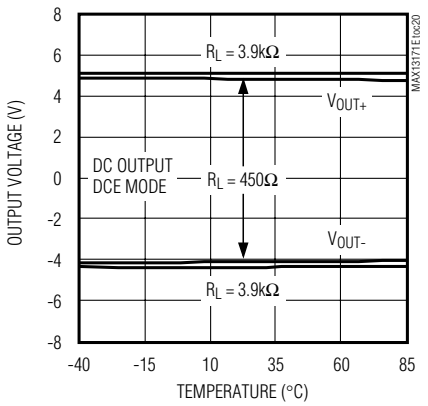
V.28 SUPPLY CURRENT vs. DATA RATE



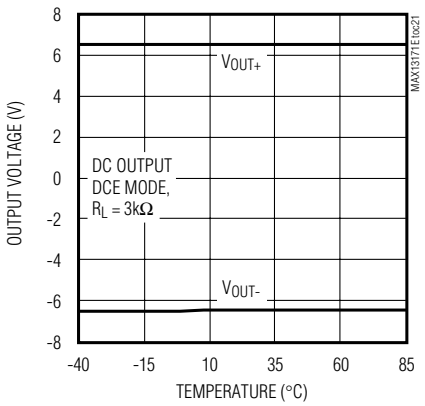
V.11 DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



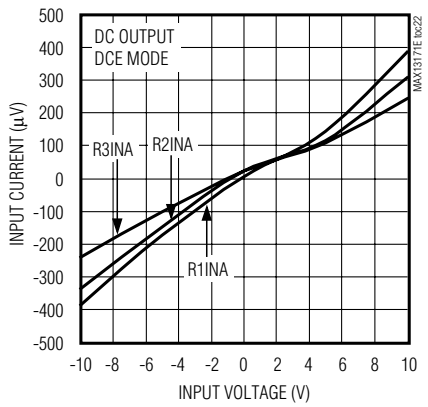
V.10 OUTPUT VOLTAGE vs. TEMPERATURE



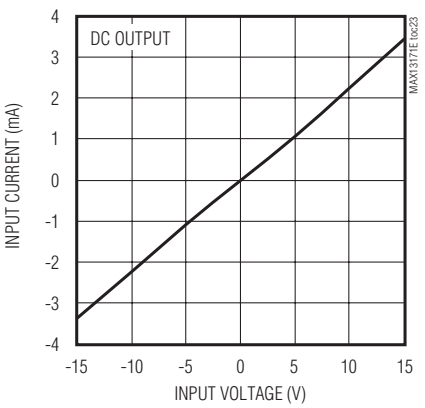
V.28 OUTPUT VOLTAGE vs. TEMPERATURE



V.11 RECEIVER INPUT CURRENT vs. INPUT VOLTAGE



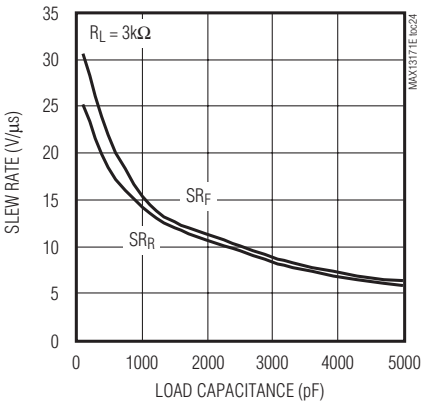
V.28 RECEIVER INPUT CURRENT vs. INPUT VOLTAGE



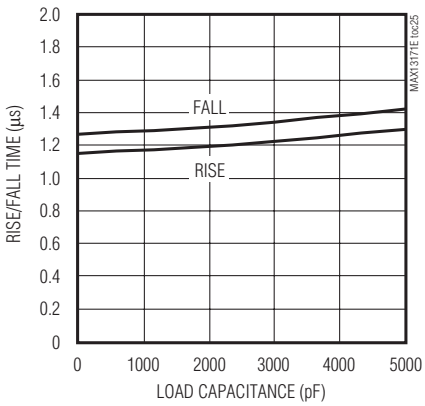
MAX13173E Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, V_L = +1.8V, T_A = +25°C, unless otherwise noted.)

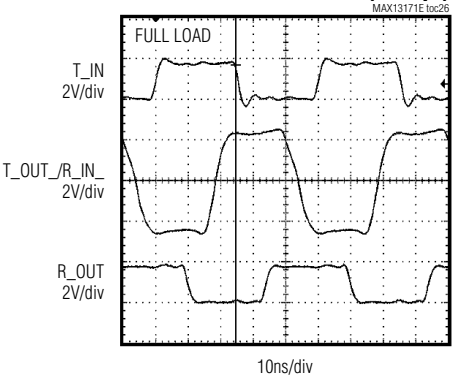
V.28 SLEW RATE vs. LOAD CAPACITANCE



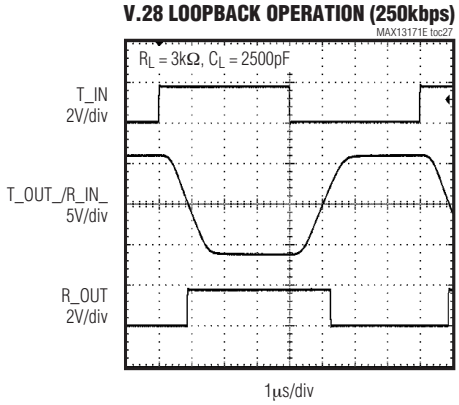
V.10 TRANSMITTER RISE/FALL TIME vs. LOAD CAPACITANCE



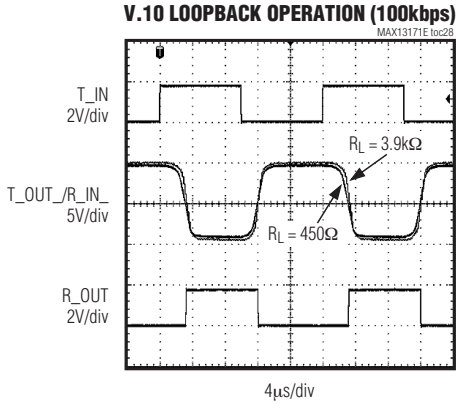
V.11 LOOPBACK OPERATION (40Mbps)



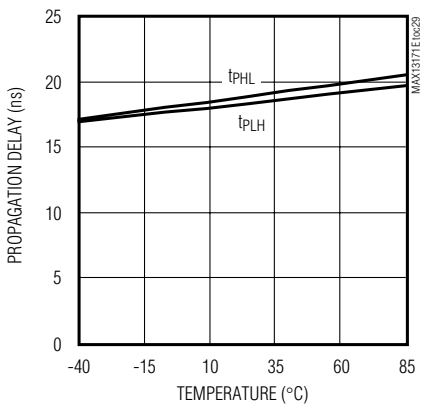
V.28 LOOPBACK OPERATION (250kbps)



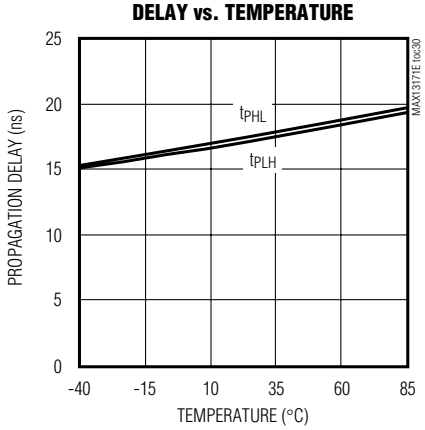
V.10 LOOPBACK OPERATION (100kbps)



V.11 RECEIVER PROPAGATION DELAY vs. TEMPERATURE



V.11 TRANSMITTER PROPAGATION DELAY vs. TEMPERATURE

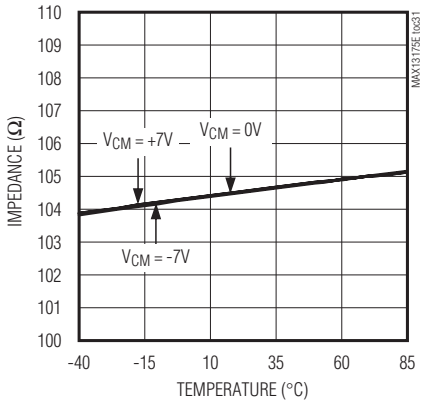


Multiprotocol, Pin-Selectable Data Interface Chipset

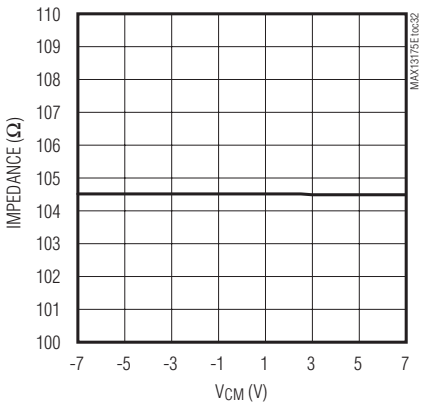
MAX13175E Typical Operating Characteristics

(V_{CC} = +3.3V, V_L = +1.8V, T_A = +25°C, unless otherwise noted.)

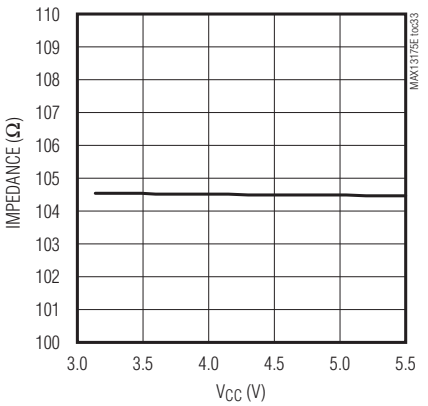
V.11 OR V.35 DIFFERENTIAL IMPEDANCE vs. TEMPERATURE



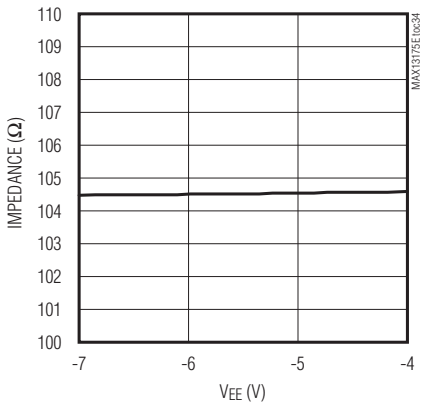
V.11 OR V.35 DIFFERENTIAL IMPEDANCE vs. COMMON-MODE VOLTAGE (V_{CM})



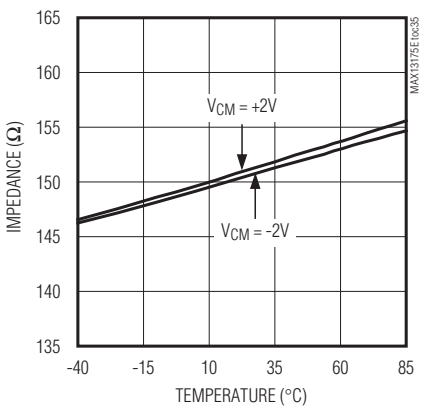
V.11 OR V.35 DIFFERENTIAL IMPEDANCE vs. SUPPLY VOLTAGE (V_{CC})



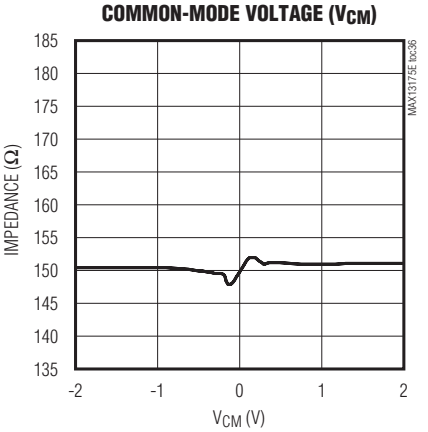
V.11 OR V.35 DIFFERENTIAL IMPEDANCE vs. SUPPLY VOLTAGE (V_{EE})



V.35 COMMON-MODE IMPEDANCE vs. TEMPERATURE



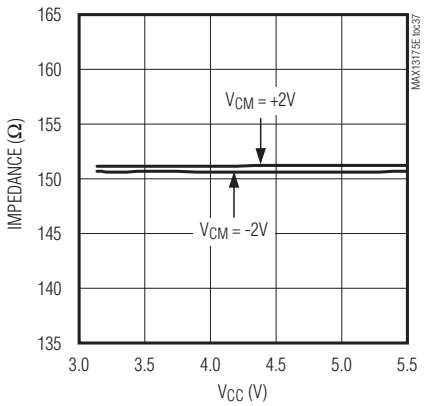
V.35 COMMON-MODE IMPEDANCE vs. COMMON-MODE VOLTAGE (V_{CM})



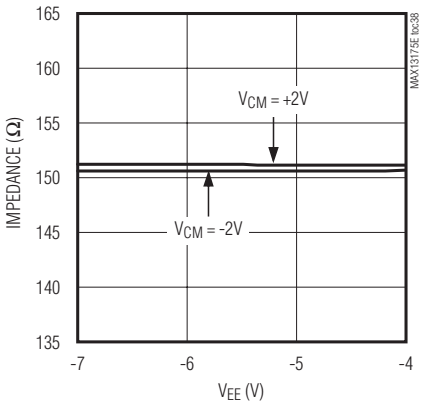
MAX13175E Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, V_L = +1.8V, T_A = +25°C, unless otherwise noted.)

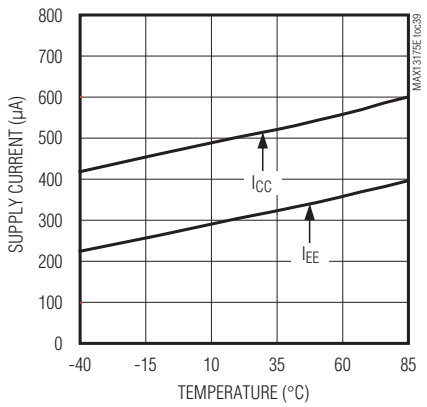
V.35 COMMON-MODE IMPEDANCE vs. SUPPLY VOLTAGE



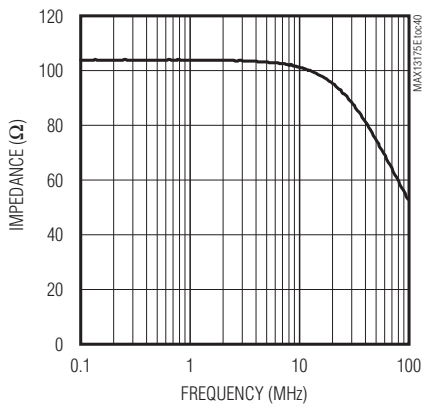
V.35 COMMON-MODE IMPEDANCE vs. SUPPLY VOLTAGE (V_{EE})



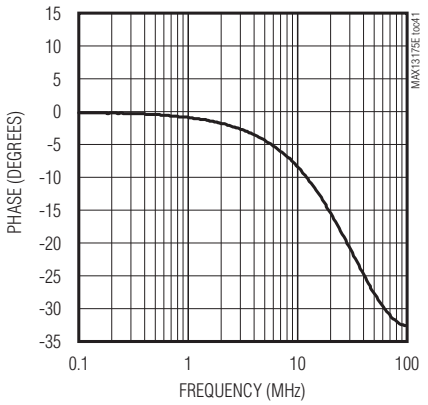
HI-Z MODE SUPPLY CURRENT vs. TEMPERATURE



V.11 OR V.35 DIFFERENTIAL IMPEDANCE MAGNITUDE vs. FREQUENCY



V.11 OR V.35 DIFFERENTIAL IMPEDANCE PHASE vs. FREQUENCY



MAX13171E Pin Description

PIN	NAME	FUNCTION
1, 2, 6, 30, 31	N.C.	No Connection. Not internally connected.
3, 16	V_{CC}	Device Supply Voltage. Bypass V_{CC} with a 4.7µF capacitor to ground as close as possible to pin 3.
4	T1IN	Transmitter 1 Logic Input
5	T2IN	Transmitter 2 Logic Input
7	T3IN	Transmitter 3 Logic Input
8	R1OUT	Receiver 1 Logic Output with Internal Pullup to V_L
9	R2OUT	Receiver 2 Logic Output with Internal Pullup to V_L
10	R3OUT	Receiver 3 Logic Output with Internal Pullup to V_L
11	M0	Mode-Select 0 Input with Internal Pullup to V_L
12	V_L	Logic-Supply Reference Input. V_L determines the voltage level of the logic interface. Bypass V_L with a 0.1µF capacitor to ground as close as possible to the device.
13	M1	Mode-Select 1 Input with Internal Pullup to V_L
14	M2	Mode-Select 2 Input with Internal Pullup to V_L
15	DCE/$\overline{\text{DTE}}$	DCE/$\overline{\text{DTE}}$ Mode-Select Input with Internal Pullup to V_L
17	R3INB	Receiver 3 Noninverting Input
18	R3INA	Receiver 3 Inverting Input
19, 24, 29, 35	GND	Ground
20	R2INB	Receiver 2 Noninverting Input
21	R2INA	Receiver 2 Inverting Input
22	T3OUTB/R1INB	Transmitter 3 Noninverting Output/Receiver 1 Noninverting Input
23	T3OUTA/R1INA	Transmitter 3 Inverting Output/Receiver 1 Inverting Input
25	T2OUTB	Transmitter 2 Noninverting Output
26	T2OUTA	Transmitter 2 Inverting Output
27	T1OUTB	Transmitter 1 Noninverting Output
28	T1OUTA	Transmitter 1 Inverting Output
32	V_{EE}	Charge-Pump Negative Supply Output. Connect a 4.7µF ceramic capacitor from V_{EE} to ground as close as possible to the device.
33	C2-	V_{EE} Charge-Pump Flying-Capacitor Negative Terminal. Connect a 1µF ceramic capacitor between C2+ and C2-.
34	C2+	V_{EE} Charge-Pump Flying-Capacitor Positive Terminal. Connect a 1µF ceramic capacitor between C2+ and C2-.
36	C1-	V_{DD} Charge-Pump Flying-Capacitor Negative Terminal. Connect a 1µF ceramic capacitor between C1+ and C1-.
37	C1+	V_{DD} Charge-Pump Flying-Capacitor Positive Terminal. Connect a 1µF ceramic capacitor between C1+ and C1-.
38	V_{DD}	Charge-Pump Positive-Supply Output. Connect a 4.7µF ceramic capacitor from V_{DD} to ground as close as possible to the device.
—	EP	Exposed Pad. Internally connected to V_{EE}. Connect to a large V_{EE} plane to maximize thermal performance. Not intended as an electrical connection point. Do not share the same plane as the MAX13173E.

MAX13173E Pin Description

PIN	NAME	FUNCTION
1	T1IN	Transmitter 1 Logic Input
2	V_{CC}	Device Supply Voltage. Bypass V_{CC} with a 4.7µF capacitor to ground as close as possible to the device.
3	T2IN	Transmitter 2 Logic Input
4	T3IN	Transmitter 3 Logic Input
5	V_L	Logic-Supply Reference Input. V_L determines the voltage level of the logic interface. Bypass V_L with a 0.1µF capacitor to ground, as close as possible to the device.
6	R1OUT	Receiver 1 Logic Output with Internal Pullup to V_L
7	R2OUT	Receiver 2 Logic Output with Internal Pullup to V_L
8	R3OUT	Receiver 3 Logic Output with Internal Pullup to V_L
9	R5OUT/T5IN	Receiver 5 Logic Output/Transmitter 5 Logic Input
10	T4IN	Transmitter 4 Logic Input
11	R4OUT	Receiver 4 Logic Output
12	M0	Mode-Select 0 Input with Internal Pullup to V_L
13	M1	Mode-Select 1 Input with Internal Pullup to V_L
14	M2	Mode-Select 2 Input with Internal Pullup to V_L
15	DCE/$\overline{DTE}$	DCE/$\overline{DTE}$ Mode-Select Input with Internal Pullup to V_L
16	INVERT	T4/R4 and T5/R5 Select Input with Internal Pullup to V_L. INVERT reverses the action of DCE/$\overline{DTE}$ for channels 4 and 5.
17	T4OUTA/R4INA	Transmitter 4 Inverting Output/Receiver 4 Inverting Input
18, 25, 31, 35	GND	Ground
19	R3INB	Receiver 3 Noninverting Input
20	R3INA	Receiver 3 Inverting Input
21	R2INB	Receiver 2 Noninverting Input
22	R2INA	Receiver 2 Inverting Input
23	T3OUTB/R1INB	Transmitter 3 Noninverting Output/Receiver 1 Noninverting Input
24	T3OUTA/R1INA	Transmitter 3 Inverting Output/Receiver 1 Inverting Input
26	T2OUTB	Transmitter 2 Noninverting Output
27	T2OUTA	Transmitter 2 Inverting Output
28	T1OUTB	Transmitter 1 Noninverting Output
29	T1OUTA	Transmitter 1 Inverting Output
30	T5OUTA/R5INA	Transmitter 5 Inverting Output/Receiver 5 Inverting Input
32	V_{EE}	Charge-Pump Negative-Supply Output. Connect a 4.7µF ceramic capacitor from V_{EE} to ground as close as possible to the device.
33	C2-	V_{EE} Charge-Pump Flying-Capacitor Negative Terminal. Connect a 1µF ceramic capacitor between C2+ and C2-.
34	C2+	V_{EE} Charge-Pump Flying-Capacitor Positive Terminal. Connect a 1µF ceramic capacitor between C2+ and C2-.
36	C1-	V_{DD} Charge-Pump Flying-Capacitor Negative Terminal. Connect a 1µF ceramic capacitor between C1+ and C1-.

MAX13173E Pin Description (continued)

PIN	NAME	FUNCTION
37	C1+	V_{DD} Charge-Pump Flying-Capacitor Positive Terminal. Connect a 1µF ceramic capacitor between C1+ and C1-.
38	V_{DD}	Charge-Pump Positive-Supply Output. Connect a 4.7µF ceramic capacitor from V_{DD} to ground as close as possible to the device.
—	EP	Exposed Pad. Internally connected to V_{EE}. Connect to a large V_{EE} plane to maximize thermal performance, not intended as an electrical connection point. Does not share the same plane as the MAX13171E.

MAX13175E Pin Description

PIN	NAME	FUNCTION
1, 38	R1B	Load 1, Node B
2, 3	R1A	Load 1, Node A
4, 5	R2A	Load 2, Node A
6, 7	R2B	Load 2, Node B
8	R2C	Load 2, Center Tap. Leave unconnected.
9, 10	R3A	Load 3, Node A
11, 12	R3B	Load 3, Node B
13, 18	GND	Ground
14	R3C	Load 3, Center Tap. Leave unconnected.
15	V_L	Logic-Supply Reference Input. V_L determines the voltage level of the logic interface.
16	V_{EE}	Negative Supply Voltage. Bypass V_{EE} to GND with a 0.1µF capacitor. Connect to V_{EE} from the MAX13173E.
17	V_{DD}	Positive Supply Voltage. Bypass V_{DD} to GND with a 0.1µF capacitor. Connect to V_{DD} from the MAX13173E.
19	V_{CC}	Supply Voltage. Bypass V_{CC} to GND with a 0.1µF capacitor as close as possible to the device.
20, 21	R4B	Load 4, Node B
22, 23	R4A	Load 4, Node A
24, 25	R5B	Load 5, Node B
26, 27	R5A	Load 5, Node A
28, 29	R6A	Load 6, Node A
30, 31	R6B	Load 6, Node B
32	DCE/$\overline{DTE}$	DCE/$\overline{DTE}$ Mode-Select Input
33	$\overline{LATCH}$	Latch Signal Input. When $\overline{LATCH}$ is low, the input latches are transparent. When $\overline{LATCH}$ is high, the data at the mode-select inputs are latched.
34	M2	Mode-Select Input 2
35	M1	Mode-Select Input 1
36	M0	Mode-Select Input 0
37	R1C	Load 1, Center Tap. Leave unconnected.
—	EP	Exposed Pad. Internally connected to V_{EE}. Connect to a large V_{EE} plane to maximize thermal performance, not intended as an electrical connection point. If V_{EE} is powered from the MAX13173E's V_{EE}, planes can be shared.

Test Circuits

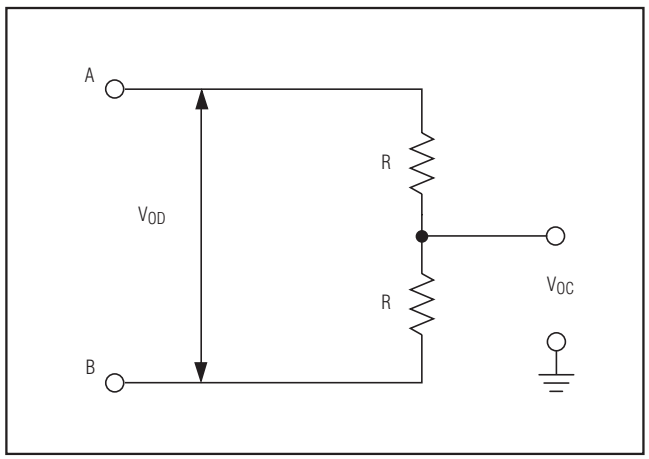


Figure 1. V.11 DC Test Circuit

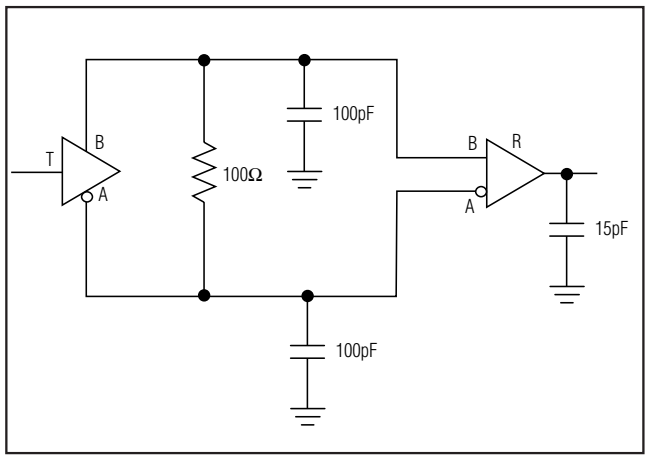


Figure 2. V.11 AC Test Circuit

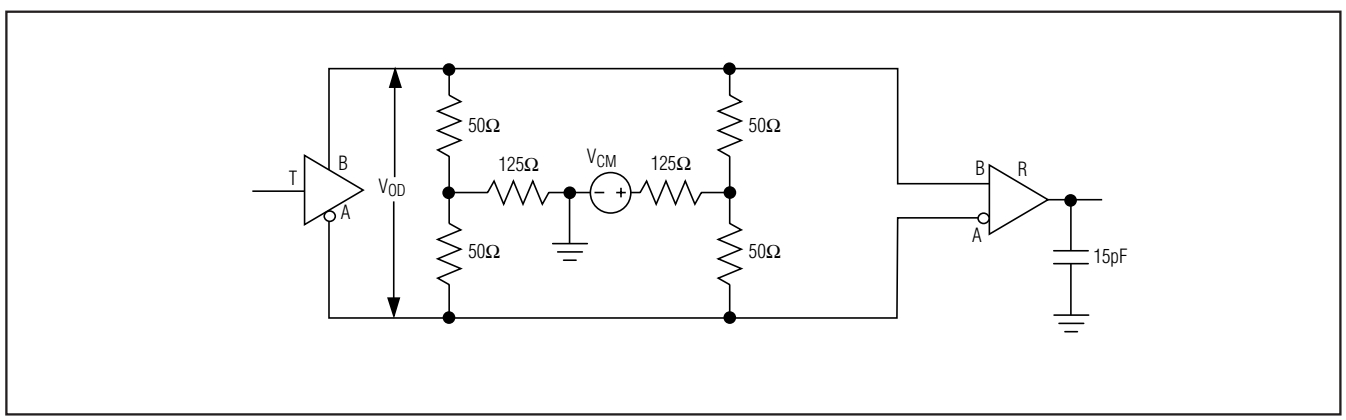


Figure 3. V.35 Transmitter/Receiver Test Circuit

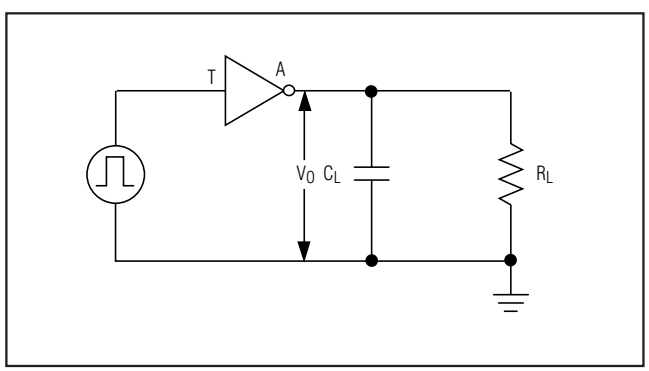


Figure 4. V.10/V.28 Transmitter Test Circuit

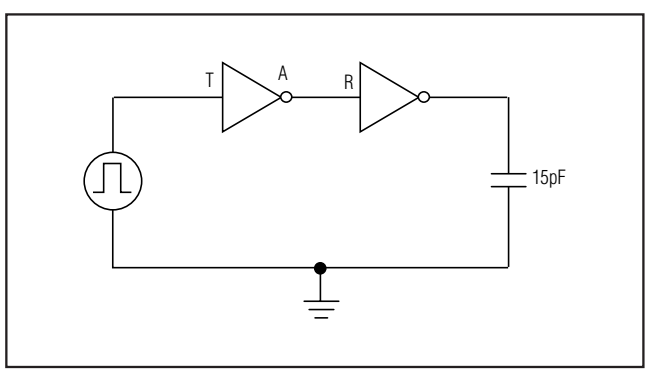


Figure 5. V.10/V.28 Receiver Test Circuit

Timing Diagrams

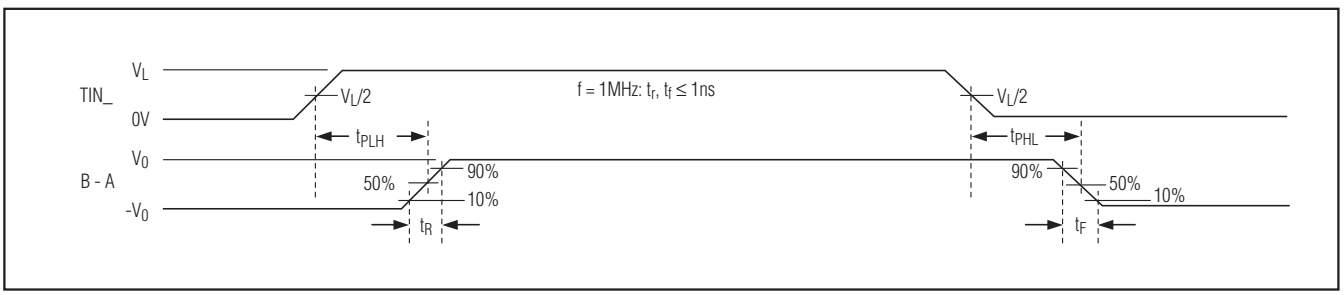


Figure 6. V.11 Transmitter Propagation Delays

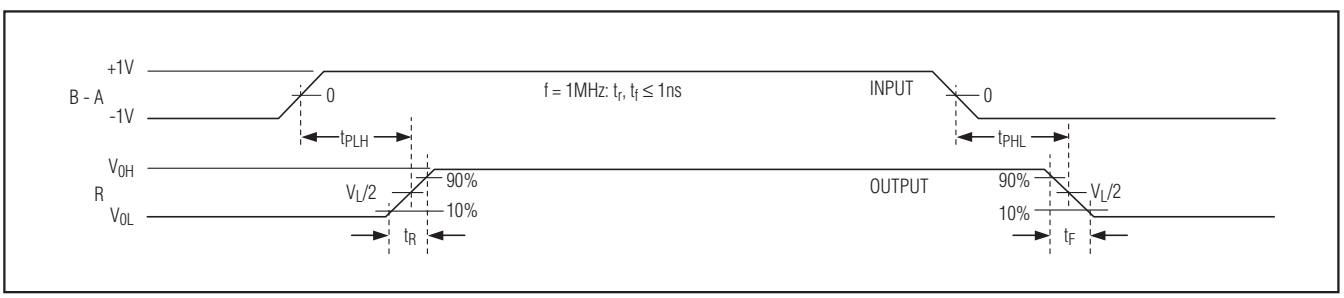


Figure 7. V.11 Receiver Propagation Delays

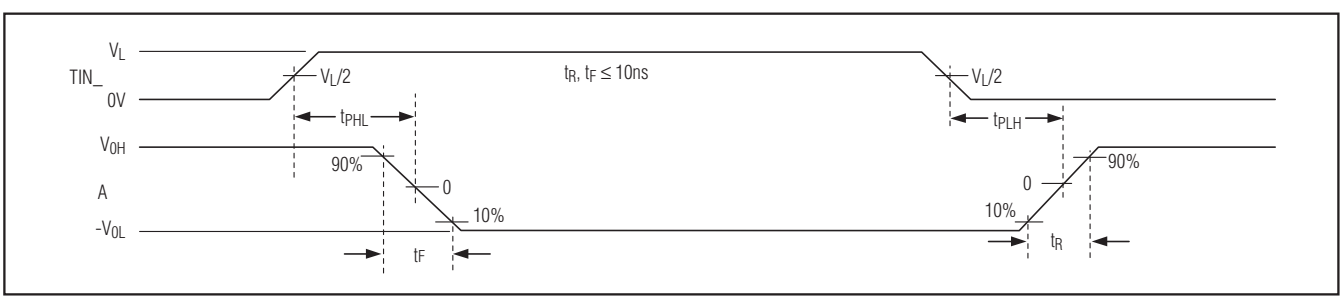


Figure 8. V.10 Transmitter Propagation Delay

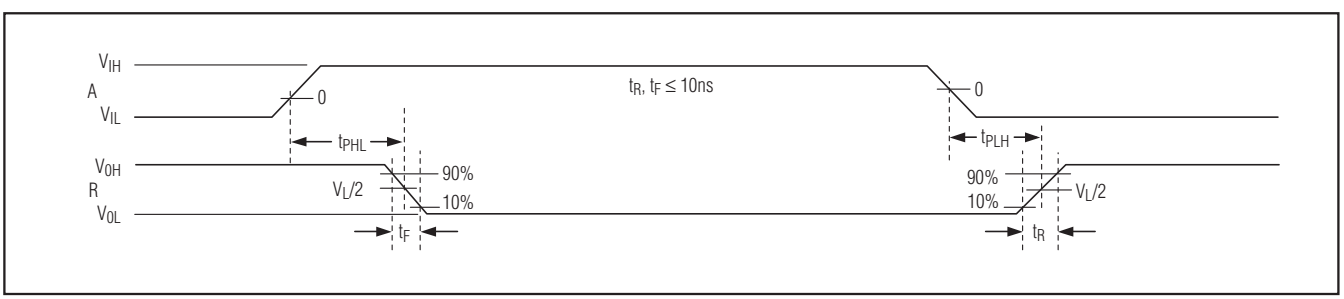


Figure 9. V.10 Receiver Propagation Delay

Timing Diagrams (continued)

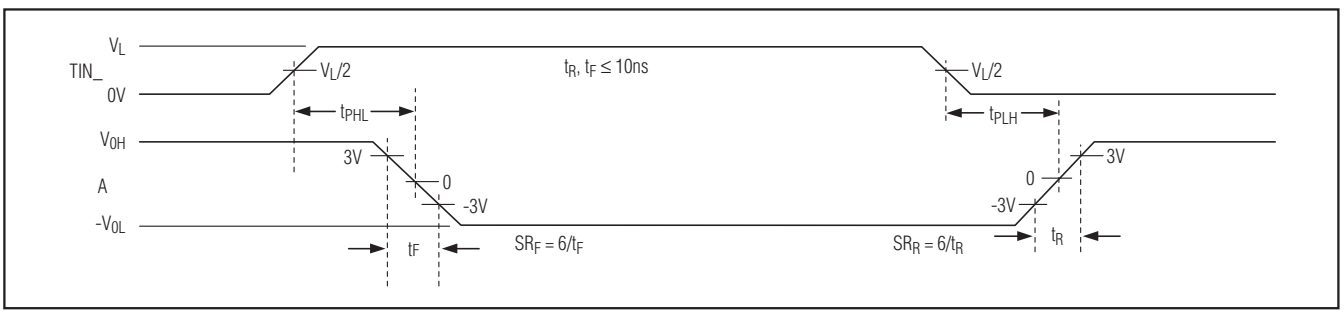


Figure 10. V.28 Transmitter Propagation Delay

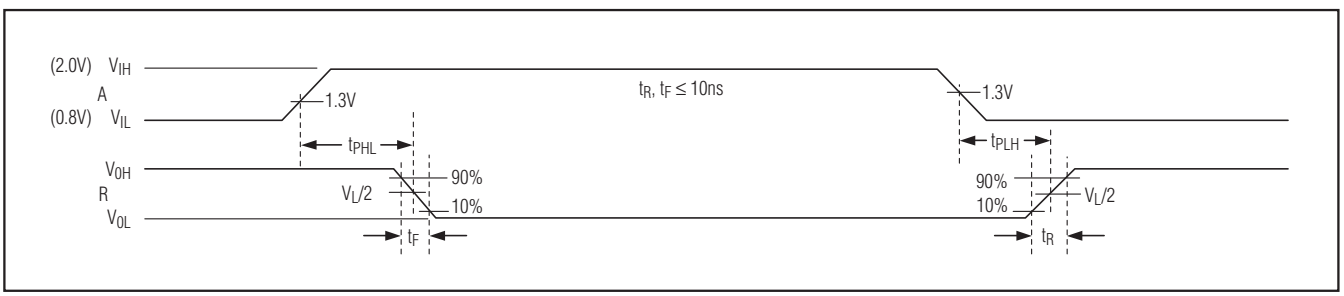


Figure 11. V.28 Receiver Propagation Delay

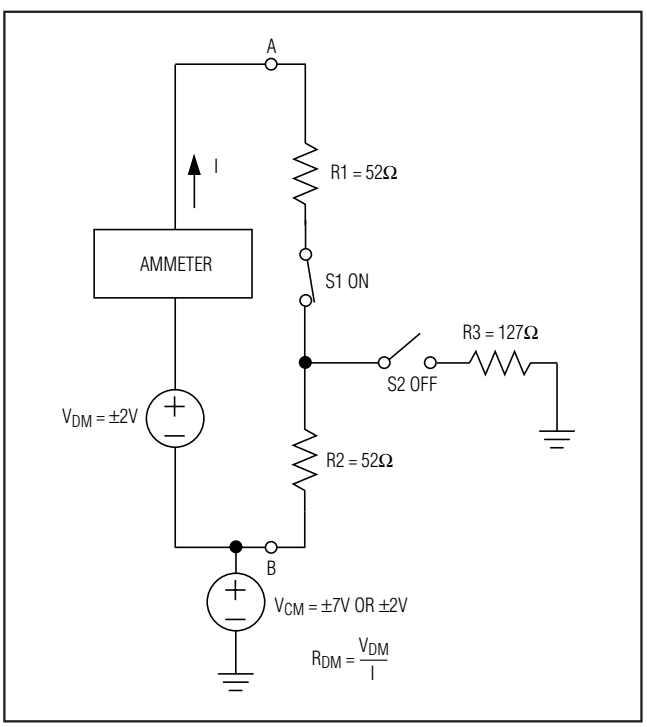


Figure 12. V.11 or V.35 Differential Impedance Measurement

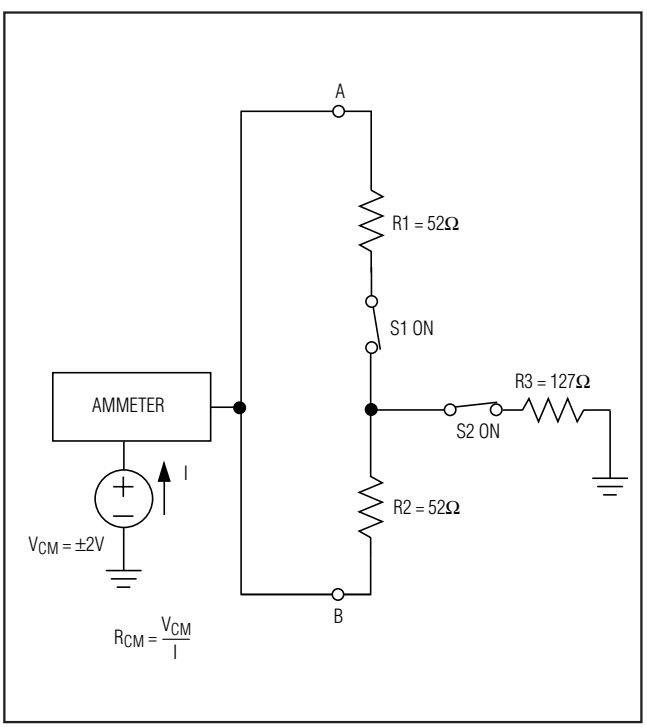


Figure 13. V.35 Common-Mode Impedance Measurement

Multiprotocol, Pin-Selectable Data Interface Chipset

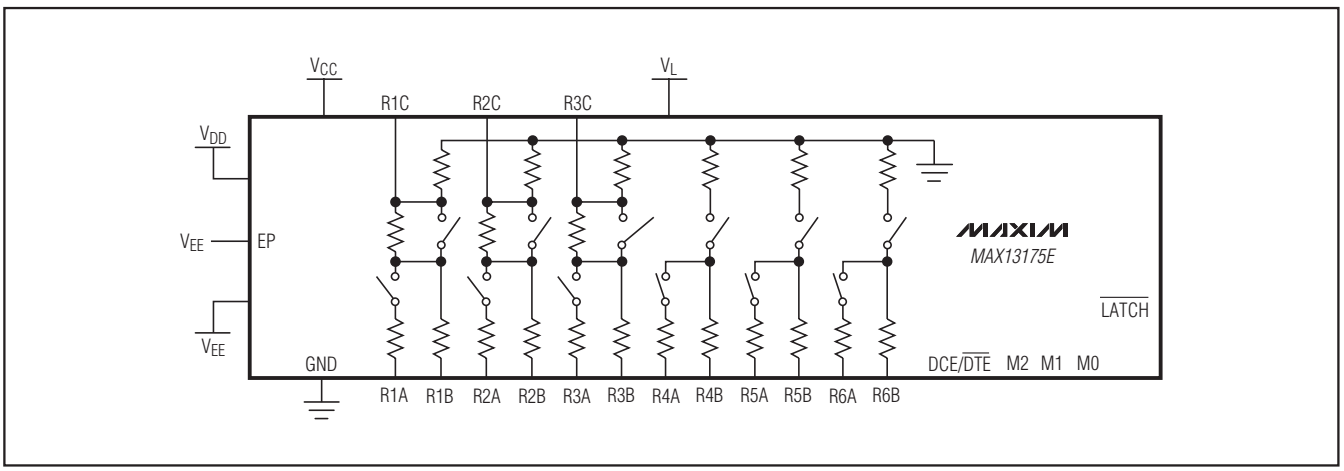


Figure 14. MAX13175E Block Diagram

Detailed Description

The MAX13171E/MAX13173E/MAX13175E form a complete pin-selectable DTE or DCE interface port that supports the V.28 (RS-232), V.10/V.11 (RS-449/V.36, RS-530, RS-530A, X.21), and V.35 protocols. The MAX13171E transceivers carry the high-speed clock and data signals, while the MAX13173E transceivers carry serial-interface control signaling. The MAX13171E can be terminated by the MAX13175E pin-selectable resistor termination network, or by a discrete termination network. The MAX13171E/MAX13173E feature a low supply current, no-cable mode, true fail-safe operation, and thermal-shutdown circuitry. Thermal shutdown protects the drivers against excessive power dissipation. When activated, the thermal-shutdown circuitry places the driver and receiver outputs into a high-impedance state.

The MAX13171E is a three-driver/three-receiver, multiprotocol transceiver that operates from a single +3.135V to +5.5V supply. The MAX13173E is a five-driver/five-receiver multiprotocol transceiver that operates from a single +3.135V to +5.5V supply. The MAX13175E contains six pin-selectable multiprotocol cable termination networks (Figure 14). Each network is capable of terminating V.11 (RS-422, RS-530, RS-530A, RS-449, V.36 and X.21) with a 100Ω differential load, V.35 with a T-network load, or V.28 (RS-232) and V.10 (RS-423) with an open-circuit load for use with transceivers having on-chip termination. The terminations and protocols are pin selectable. The MAX13175E replaces discrete resistor termination networks and expensive relays required for multiprotocol termination, saving space and cost.

Dual Charge-Pump Voltage Converter

The MAX13171E/MAX13173E have internal-regulated dual charge pumps that provide positive and negative output voltages from a single supply. The charge pump operates in discontinuous mode. If the output voltage is less than the regulated voltage, the charge pump is enabled. If the output voltage exceeds the regulated voltage, the charge pump is disabled. Each charge pump requires flying capacitors (C1, C2), and reservoir capacitors (C3, C5), to generate the V_{DD} and V_{EE} supplies. Figure 15 shows the charge-pump connections.

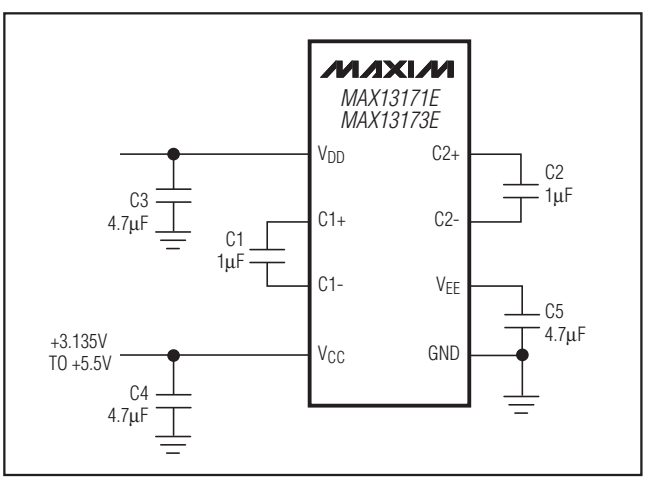


Figure 15. Charge Pump

Fail-Safe

The MAX13171E/MAX13173E guarantee a logic-high receiver output when the receiver inputs are open or shorted, or when they are connected to a terminated transmission line with all drivers disabled by setting the receiver threshold between -50mV and -200mV in the V.11 and V.35 modes. If the differential receiver input voltage (B - A) is ≥ -50mV, R_OUT is logic-high. If (B - A) is ≤ -200mV, R_OUT is logic-low. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to zero by the termination. This results in a logic-high with a 50mV minimum noise margin.

The V.10 receiver threshold is set between 50mV and 250mV. If the V.10 receiver input voltage is less than or equal to 50mV, R_OUT is logic-high. The V.28 receiver threshold is set between 0.8V and 2.0V. If the receiver input voltage is less than or equal to 0.8V, R_OUT is logic-high. In the case of a terminated bus with transmitters disabled, the receiver's input voltage is pulled to GND by the termination.

Mode Selection

The mode-select inputs M0, M1, and M2 determine which interface protocol is selected (Table 1 for the MAX13171E, Table 2 for the MAX13173E). The state of the DCE/$\overline{DTE}$ input determines whether the transceivers are configured as a DTE serial port or a DCE serial port. The INVERT input on the MAX13173E changes the DCE/$\overline{DTE}$ functionality regarding T4/T5 and R4/R5 only. M0, M1, M2, INVERT, and DCE/$\overline{DTE}$ are internally pulled up to V_L to ensure logic-high if left unconnected. If the M0, M1, and M2 mode inputs are all unconnected, the MAX13171E/MAX13173E enter no-cable mode.

The MAX13175E mode select inputs and DCE/$\overline{DTE}$ input do not have an internal pullup to V_L. They are pulled logic-high if their mode-select inputs are tied to the MAX13171E/MAX13173E's mode select inputs.

Termination Modes

The termination networks in the MAX13175E can be set to one of three modes, V.11, V.35, or high impedance.

Table 1. MAX13171E Mode Selection

MAX13171E MODE NAME	M2	M1	M0	DCE/$\overline{DTE}$	T1	T2	T3	R1	R2	R3
Not Used (Default V.11)	0	0	0	0	V.11	V.11	Z	V.11	V.11	V.11
RS-530A	0	0	1	0	V.11	V.11	Z	V.11	V.11	V.11
RS-530	0	1	0	0	V.11	V.11	Z	V.11	V.11	V.11
X.21	0	1	1	0	V.11	V.11	Z	V.11	V.11	V.11
V.35	1	0	0	0	V.35	V.35	Z	V.35	V.35	V.35
RS-449/V.36	1	0	1	0	V.11	V.11	Z	V.11	V.11	V.11
V.28/RS-232	1	1	0	0	V.28	V.28	Z	V.28	V.28	V.28
No Cable	1	1	1	0	Z	Z	Z	Z	Z	Z
Not Used (Default V.11)	0	0	0	1	V.11	V.11	V.11	Z	V.11	V.11
RS-530A	0	0	1	1	V.11	V.11	V.11	Z	V.11	V.11
RS-530	0	1	0	1	V.11	V.11	V.11	Z	V.11	V.11
X.21	0	1	1	1	V.11	V.11	V.11	Z	V.11	V.11
V.35	1	0	0	1	V.35	V.35	V.35	Z	V.35	V.35
RS-449/V.36	1	0	1	1	V.11	V.11	V.11	Z	V.11	V.11
V.28/RS-232	1	1	0	1	V.28	V.28	V.28	Z	V.28	V.28
No Cable	1	1	1	1	Z	Z	Z	Z	Z	Z

Table 2. MAX13173E Mode Selection

PROTOCOL	M2	M1	M0	DCE/$\overline{\text{DTE}}$	INVERT	T1	T2	T3	R1	R2	R3	T4	R4	T5	R5
Not Used (Default V.11)	0	0	0	0	0	V.11	V.11	Z	V.11	V.11	V.11	Z	V.10	Z	V.10
RS-530A	0	0	1	0	0	V.11	V.10	Z	V.11	V.10	V.11	Z	V.10	Z	V.10
RS-530	0	1	0	0	0	V.11	V.11	Z	V.11	V.11	V.11	Z	V.10	Z	V.10
X.21	0	1	1	0	0	V.11	V.11	Z	V.11	V.11	V.11	Z	V.10	Z	V.10
V.35	1	0	0	0	0	V.28	V.28	Z	V.28	V.28	V.28	Z	V.28	Z	V.28
RS-449/V.36	1	0	1	0	0	V.11	V.11	Z	V.11	V.11	V.11	Z	V.10	Z	V.10
V.28/RS-232	1	1	0	0	0	V.28	V.28	Z	V.28	V.28	V.28	Z	V.28	Z	V.28
No Cable	1	1	1	0	0	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
Not Used (Default V.11)	0	0	0	0	1	V.11	V.11	Z	V.11	V.11	V.11	V.10	Z	V.10	Z
RS-530A	0	0	1	0	1	V.11	V.10	Z	V.11	V.10	V.11	V.10	Z	V.10	Z
RS-530	0	1	0	0	1	V.11	V.11	Z	V.11	V.11	V.11	V.10	Z	V.10	Z
X.21	0	1	1	0	1	V.11	V.11	Z	V.11	V.11	V.11	V.10	Z	V.10	Z
V.35	1	0	0	0	1	V.28	V.28	Z	V.28	V.28	V.28	V.28	Z	V.28	Z
RS-449/V.36	1	0	1	0	1	V.11	V.11	Z	V.11	V.11	V.11	V.10	Z	V.10	Z
V.28/RS-232	1	1	0	0	1	V.28	V.28	Z	V.28	V.28	V.28	V.28	Z	V.28	Z
No Cable	1	1	1	0	1	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
Not Used (Default V.11)	0	0	0	1	0	V.11	V.11	V.11	Z	V.11	V.11	V.10	Z	V.10	Z
RS-530A	0	0	1	1	0	V.11	V.10	V.11	Z	V.10	V.11	V.10	Z	V.10	Z
RS-530	0	1	0	1	0	V.11	V.11	V.11	Z	V.11	V.11	V.10	Z	V.10	Z
X.21	0	1	1	1	0	V.11	V.11	V.11	Z	V.11	V.11	V.10	Z	V.10	Z
V.35	1	0	0	1	0	V.28	V.28	V.28	Z	V.28	V.28	V.28	Z	V.28	Z
RS-449/V.36	1	0	1	1	0	V.11	V.11	V.11	Z	V.11	V.11	V.10	Z	V.10	Z
V.28/RS-232	1	1	0	1	0	V.28	V.28	V.28	Z	V.28	V.28	V.28	Z	V.28	Z
No Cable	1	1	1	1	0	Z	Z	Z	Z	Z	Z	Z	Z	Z	V.10
Not Used (Default V.11)	0	0	0	1	1	V.11	V.11	V.11	Z	V.11	V.11	Z	V.10	Z	V.10
RS-530A	0	0	1	1	1	V.11	V.10	V.11	Z	V.10	V.11	Z	V.10	Z	V.10
RS-530	0	1	0	1	1	V.11	V.11	V.11	Z	V.11	V.11	Z	V.10	Z	V.10
X.21	0	1	1	1	1	V.11	V.11	V.11	Z	V.11	V.11	Z	V.10	Z	V.10
V.35	1	0	0	1	1	V.28	V.28	V.28	Z	V.28	V.28	Z	V.28	Z	V.28
RS-449/V.36	1	0	1	1	1	V.11	V.11	V.11	Z	V.11	V.11	Z	V.10	Z	V.10
V.28/RS-232	1	1	0	1	1	V.28	V.28	V.28	Z	V.28	V.28	Z	V.28	Z	V.28
No Cable	1	1	1	1	1	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

As shown in Figure 16, in V.11 mode, switch S1 is closed and switch S2 is open, presenting 104Ω across terminals A and B. In V.35 mode, switches S1 and S2 are both closed, presenting a T-network with 104Ω differential impedance and 153Ω common-mode impedance. In high-impedance mode, switches S1 and S2 are both open, presenting a high impedance across terminals A and B suitable for V.28 and V.10 modes.

The state of the MAX13175E's mode-select inputs, M0, M1, M2, and DCE/$\overline{\text{DTE}}$ determines the mode of each of the six termination networks. Table 3 shows a cross-reference of termination mode and select input state for each of the six termination networks within the MAX13175E.

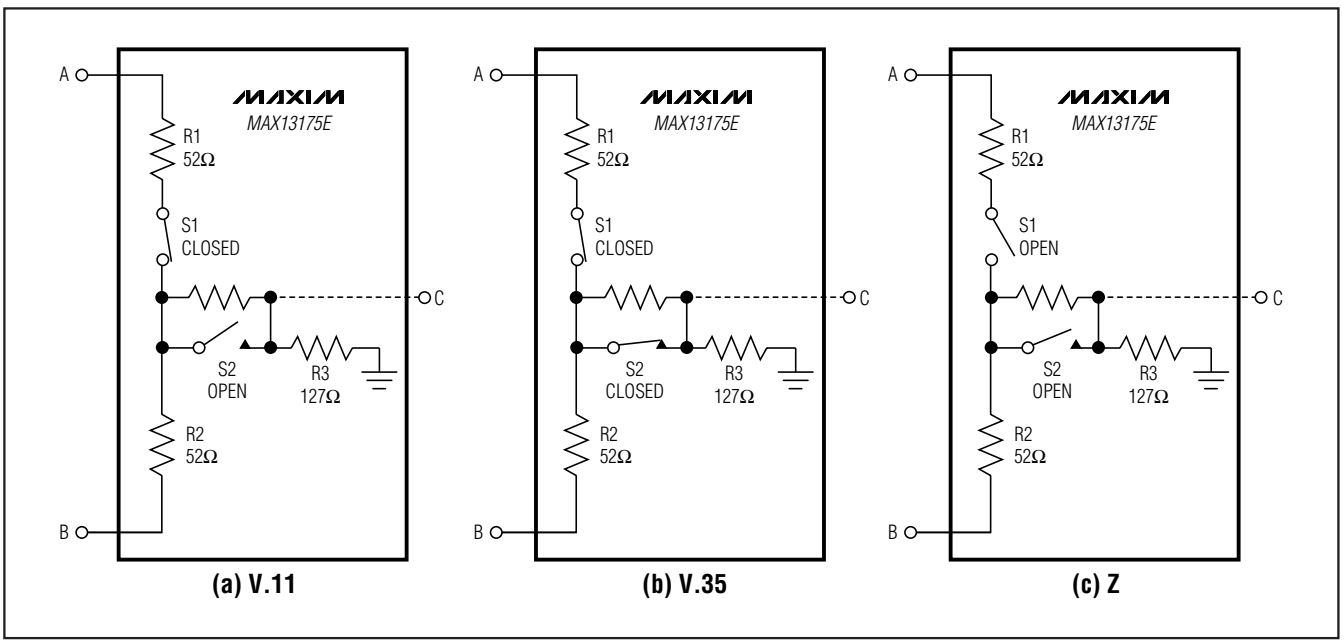


Figure 16. Termination Modes

Table 3. MAX13175E Termination Mode Selection

PROTOCOL	DCE/$\overline{\text{DTE}}$	M2	M1	M0	R1	R2	R3	R4	R5	R6
V.10/RS-423	0	0	0	0	Z	Z	Z	Z	Z	Z
RS-530A	0	0	0	1	Z	Z	Z	V.11	V.11	V.11
RS-530	0	0	1	0	Z	Z	Z	V.11	V.11	V.11
X.21	0	0	1	1	Z	Z	Z	V.11	V.11	V.11
V.35	0	1	0	0	V.35	V.35	Z	V.35	V.35	V.35
RS-449/V.36	0	1	0	1	Z	Z	Z	V.11	V.11	V.11
V.28/RS-232	0	1	1	0	Z	Z	Z	Z	Z	Z
No Cable	0	1	1	1	V.11	V.11	V.11	V.11	V.11	V.11
V.10/RS-423	1	0	0	0	Z	Z	Z	Z	Z	Z
RS-530A	1	0	0	1	Z	Z	Z	Z	V.11	V.11
RS-530	1	0	1	0	Z	Z	Z	Z	V.11	V.11
X.21	1	0	1	1	Z	Z	Z	Z	V.11	V.11
V.35	1	1	0	0	V.35	V.35	V.35	Z	V.35	V.35
RS-449/V.36	1	1	0	1	Z	Z	Z	Z	V.11	V.11
V.28/RS-232	1	1	1	0	Z	Z	Z	Z	Z	Z
No Cable	1	1	1	1	V.11	V.11	V.11	V.11	V.11	V.11

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No-Cable Mode

The MAX13171E/MAX13173E enter no-cable mode when the mode-select inputs are left unconnected or connected high (M0 = M1 = M2 = 1). The receiver outputs enter a high-impedance state in no-cable mode, allowing these output lines to be shared with other receiver outputs (the receiver outputs have an internal pullup resistor to pull the outputs high if not driven). Also, in no-cable mode, the transmitter outputs enter a high-impedance state, so these output lines can be shared with other devices.

The MAX13175E enters no-cable mode when the mode select inputs, M0, M1, and M2 are connected high. In no-cable mode, all six termination networks are placed in V.11 mode, with S1 closed and S2 open.

V_L Logic Supply

The MAX13171E/MAX13173E/MAX13175E include a V_L logic supply that allows user-defined interface logic-voltage levels referenced to V_L. V_L can go down to +1.62V and up to V_{CC}. All logic inputs and outputs are referred to V_L.

Data Rate

The MAX13171E/MAX13173E/MAX13175E support a maximum data rate of 40Mbps in RS-449/V.36, RS-530, RS-530A, X.21, V.35 if only one of the MAX13171E high-speed transceivers is operated at the maximum data rate. If two high-speed transceivers operate simultaneously, the maximum data rate is 20Mbps.

Applications Information

Capacitor Selection

The capacitors used for the charge pumps, as well as for supply bypassing, must have a low equivalent series resistance (ESR), low inductance (ESL), and low temperature coefficient. Multilayer ceramic capacitors with an X7R dielectric offer the best combination of performance, size, and cost. The flying capacitors (C1, C2) should have a value of 1µF, while the bypass capacitor (C4) and reservoir capacitors (C3, C5) should have a minimum value of 4.7µF (Figure 15). To reduce the ripple present on the transmitter outputs, capacitors C3, C4, and C5 can be increased. The values of C1 and C2 should not be increased.

Cable Mode-Select Application

A cable-selectable multiprotocol interface is shown in Figure 17. The mode control lines M0, M1, and DCE/$\overline{\text{DTE}}$ are wired to the DB-25 connector. To select the serial interface mode, the appropriate combination of M0, M1, and DCE/$\overline{\text{DTE}}$ are grounded within the cable wiring. The control lines that are not grounded are pulled high by the internal pullups on the MAX13171E/MAX13173E. The serial interface protocol of the MAX13171E/MAX13173E/MAX13175E is selected based on the cable that is connected to the DB-25 interface.

V.10 (RS-423) Interface (MAX13173E Only)

The V.10 interface (Figure 18) is an unbalanced single-ended interface capable of driving a 450Ω load. The V.10 driver generates a minimum V_O voltage of ±4V across A' and C' when unloaded, and a minimum voltage of 0.9 x V_O when loaded with 450Ω. The V.10 receiver has a single-ended input and does not reject common-mode differences between C and C'. The V.10 receiver-input trip threshold is defined between +50mV and +250mV with input impedance characteristic shown in Figure 19.

The MAX13173E V.10 mode receiver has a threshold between +50mV and +250mV. To ensure that the receiver has proper fail-safe operation, see the *Fail-Safe* section. To aid in rejecting system noise, the MAX13173E V.10 receiver has a typical hysteresis of 25mV. Switch S3 in Figures 20a and 20b is open in V.10 mode to disable the V.28 5kΩ termination at the receiver input. Switch S4 is closed and switch S5 is open to internally ground the receiver B input.

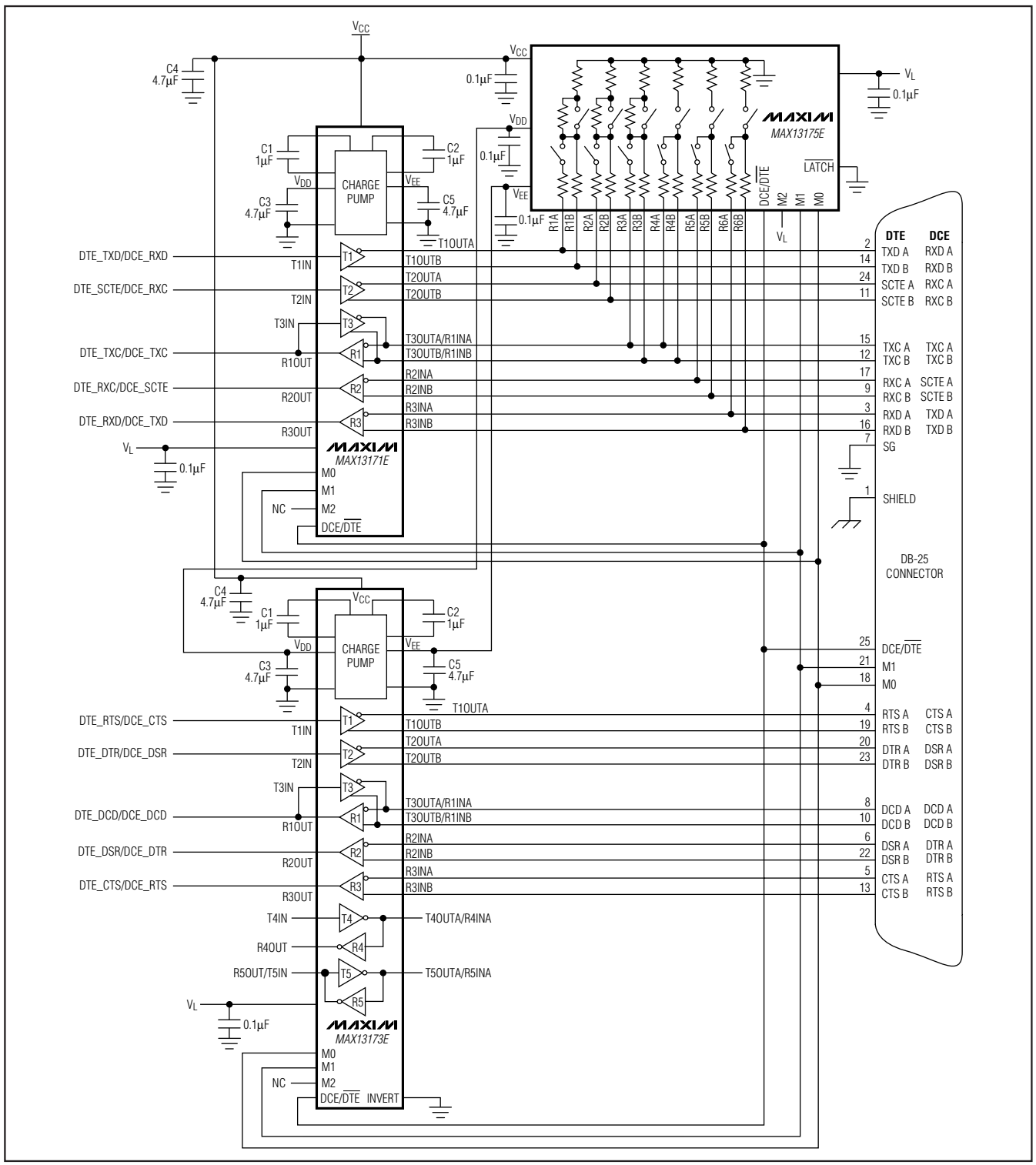

Figure 17. Cable-Selectable Multiprotocol DCE/DTE Port with DB-25 Connector

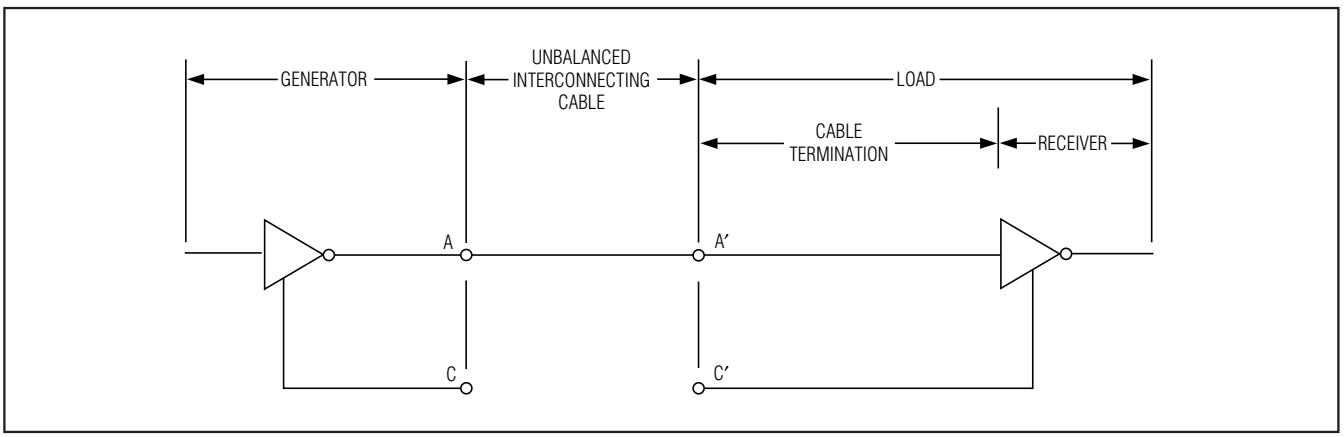

Figure 18. Typical V.10/V.28 Interface

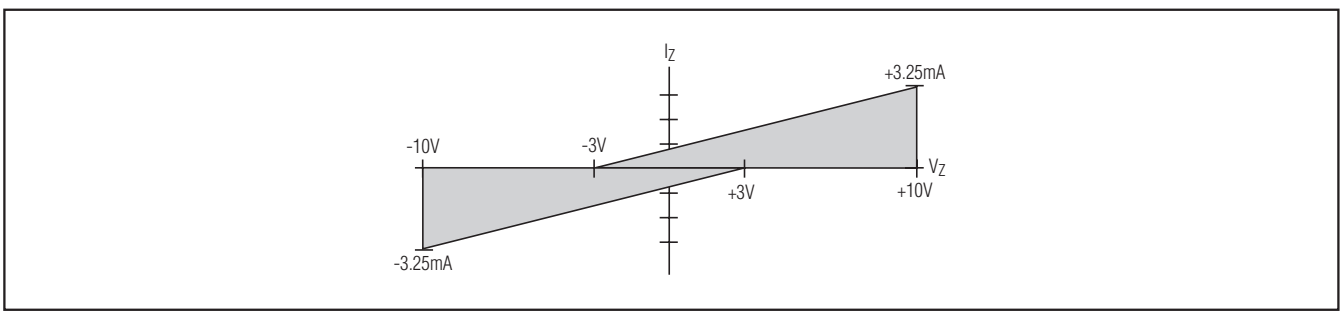

Figure 19. Receiver Input Impedance Curve

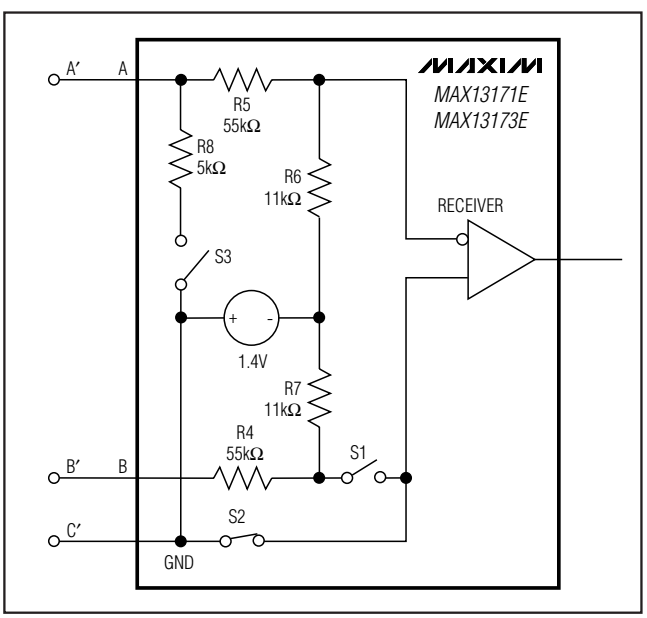

Figure 20a. V.10 Internal Resistance Network for Receivers 1, 2, and 3

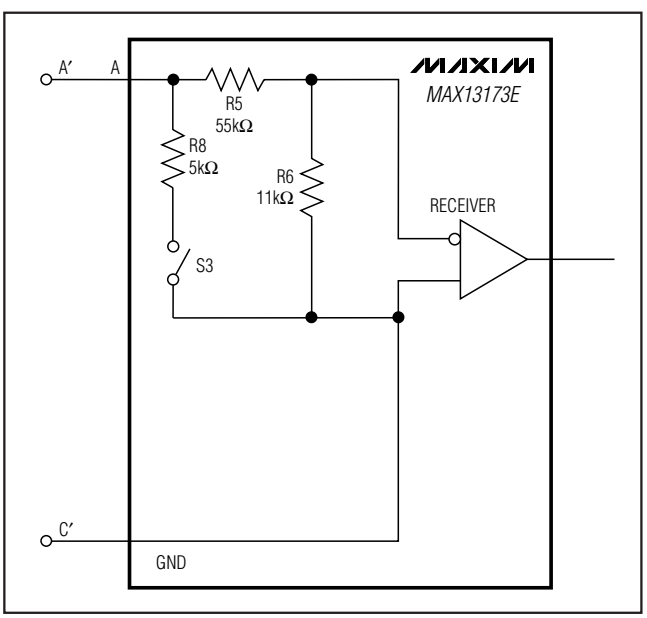

Figure 20b. V.10 Internal Resistance Network for Receivers 4 and 5

V.11 (RS-422) Interface

As shown in Figure 21, the V.11 protocol is a fully balanced differential interface. The V.11 driver generates a minimum of ±2V between nodes A and B when a 100Ω (min) resistance is present at the load. The V.11 receiver is sensitive to differential signals of ±200mV at receiver inputs A' and B'. The V.11 receiver input must comply with the impedance curve of Figure 22 and reject common-mode signals developed across the cable (referenced from C to C' in Figure 21) of up to ±7V.

The MAX13171E/MAX13173E V.11 mode receivers have a differential threshold between -50mV and -200mV to ensure that the receiver has fail-safe operation (see the *Fail-Safe* section.) To aid in rejecting system noise, the MAX13171E/MAX13173E V.11 receivers have a typical hysteresis of 15mV. Switch S3 in Figure 23 is open in V.11 mode to disable the V.28 5kΩ termination at the inverting receiver input. Because the control signals are slow (60kbps), 100Ω termination resistance is generally not required for the MAX13173E.

For high-speed data transmission, the V.11 specification recommends terminating the cable at the receiver with a 100Ω resistor. This resistor, although not required, prevents reflections from corrupting transmitted data. In Figure 23, the MAX13175E is used to terminate the V.11 receiver. Internal to the MAX13175E, S1 is closed and S2 is open to present a 100Ω minimum differential resistance. The MAX13171E's internal V.28 termination is disabled by opening S3.

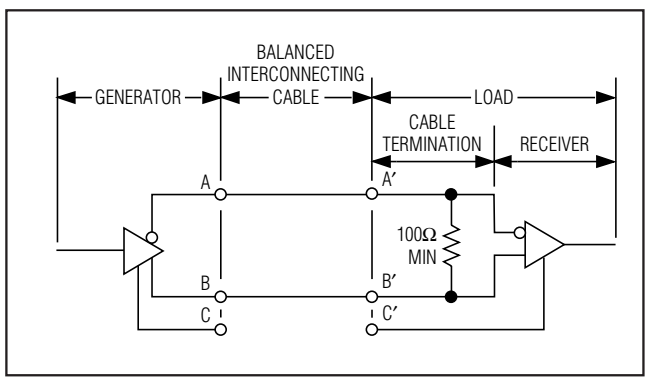

Figure 21. Typical V.11 Interface

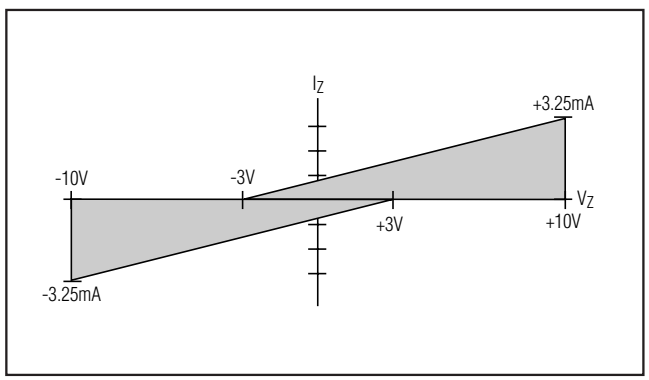

Figure 22. Receiver Input Impedance

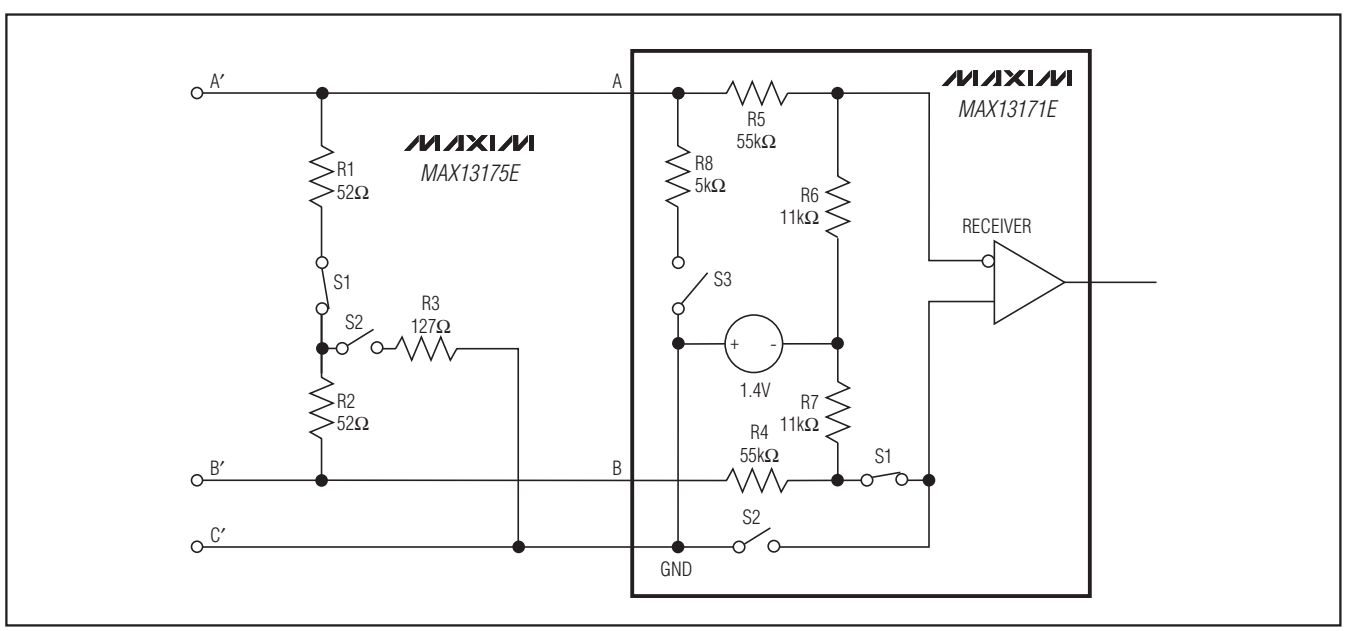

Figure 23. V.11 Termination and Internal Resistance Networks

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V.28 (RS-232) Interface

The V.28 interface is an unbalanced single-ended interface (Figure 18). The V.28 driver generates a minimum of ±5V across the 3kΩ load impedance between A' and C'. The V.28 receiver has a single-ended input.

The MAX13171E/MAX13173E V.28 mode receivers have a threshold between +0.8V and +2.0V. To aid in rejecting system noise, the MAX13171E/MAX13173E V.28 receivers have a typical hysteresis of 250mV. Switch S3 in Figures 24a and 24b is closed in V.28 mode to enable the 5kΩ V.28 termination at the receiver inputs.

V.35 Interface

Figure 25 shows a fully-balanced, differential standard V.35 interface. The generator and the load must both present a 100Ω ±10Ω differential impedance and a 150Ω ±15Ω common-mode impedance as shown by the resistive T-networks in Figure 26. The V.35 driver generates a current output (±11mA, typ) that develops an output voltage of ±550mV across the generator and load termination networks. The V.35 receiver is sensitive to ±200mV differential signals at receiver inputs A' and B'. The V.35 receiver rejects common-mode signals developed across the cable (referenced from C to C') of up to ±4V, allowing for error-free reception in noisy environments.

In Figure 26, the MAX13175E is used to implement the resistive T-network that is needed to properly terminate the V.35 driver and receiver. Internal to the MAX13175E, S1 and S2 are closed to connect the T-network resistors to the circuit. The V.28 termination resistor (internal to the MAX13171E) is disabled by opening S3 to avoid interference with the T-network impedance.

The V.35 specification allows for ±4V of ground difference between the V.35 generator and V.35 load. The MAX13174E maintains correct termination impedance over this condition.

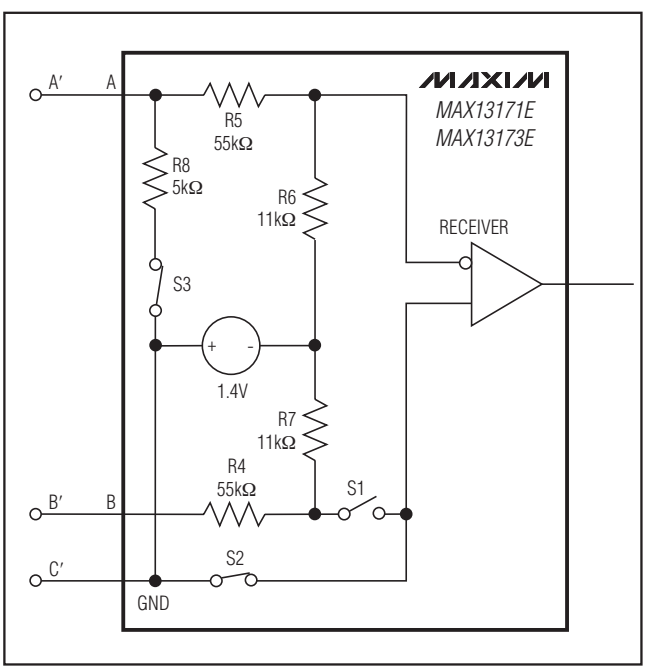

Figure 24a. V.28 Termination and Internal Resistance Network for Receiver 1, 2, and 3

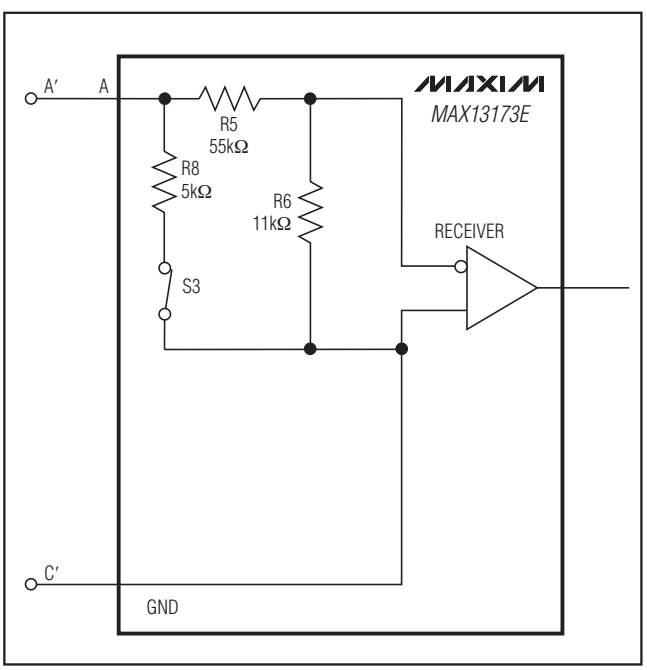

Figure 24b. V.28 Internal Resistance Network for Receiver 4 and 5

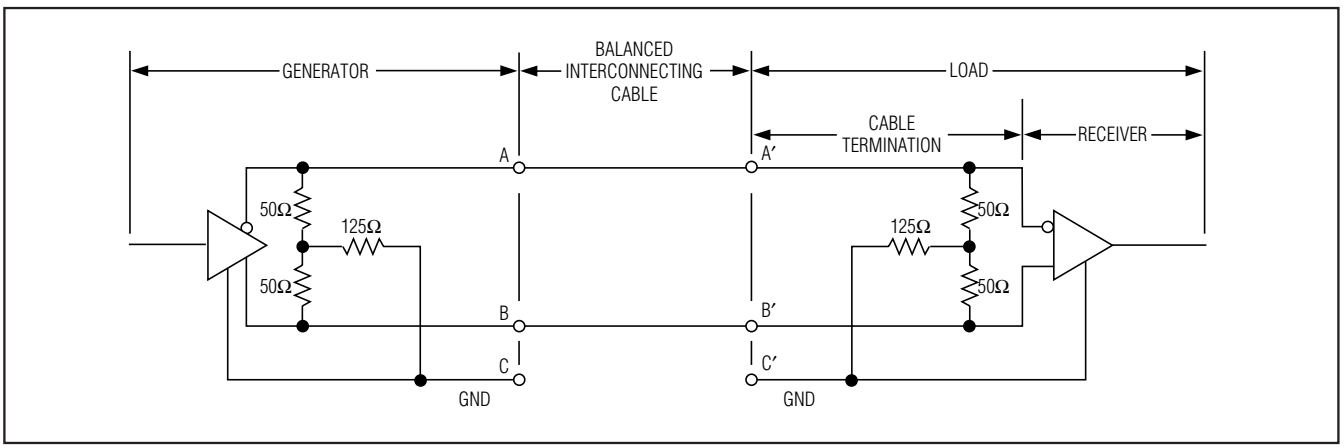

Figure 25. Typical V.35 Interface

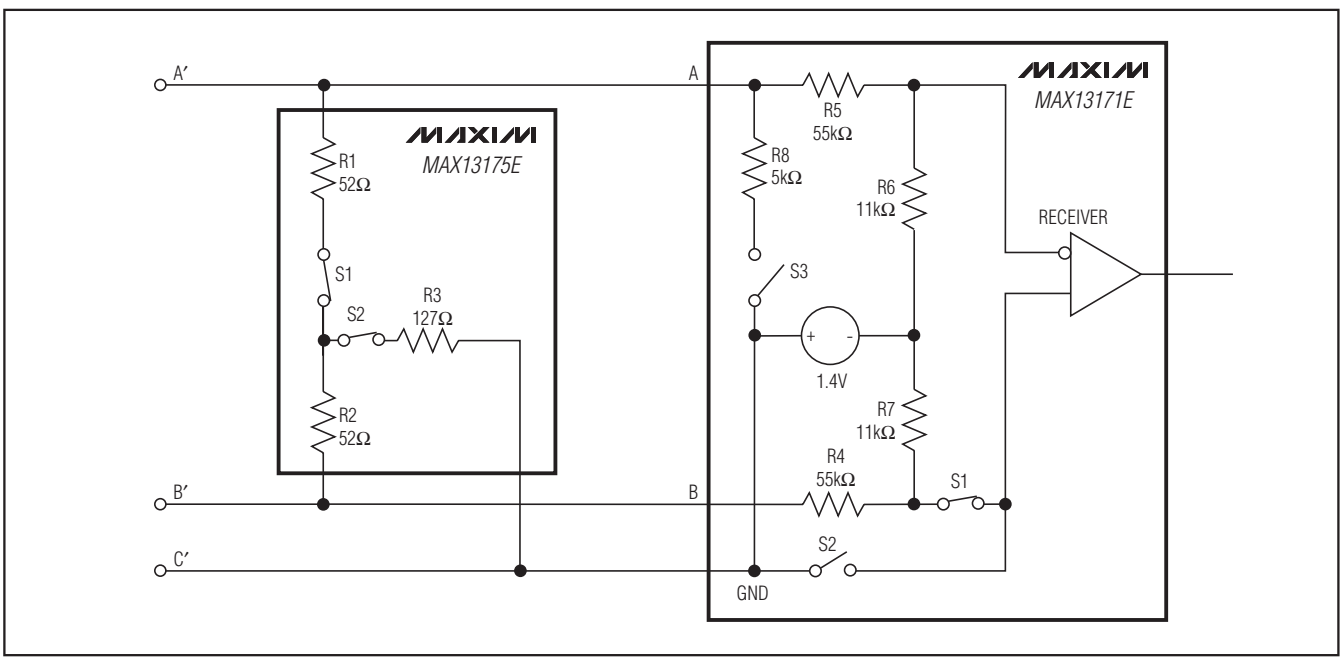

Figure 26. V.35 Termination and Internal Resistance Networks

DTE/DCE Mode Applications

The MAX13171E/MAX13173E can be hardwired for either DTE or DCE mode in one of two ways: a dedicated DTE or DCE port with an appropriate gender connector, or a port with a connector that can be configured for DTE or DCE operation by rerouting the signals to the MAX13171E and MAX13173E, using a dedicated DTE cable or dedicated DCE cable. The interface mode is selected by logic outputs from the controller or from jumpers to either V_L or GND on the mode select inputs.

A dedicated DCE port using a DB-25 female connector is shown in Figure 28. Figure 29 illustrates a dedicated DTE port using a DB-25 male connector.

Figure 27 shows an application circuit with one common DB-25 connector that can be configured for either DTE or DCE mode. The configuration requires separate cables for proper signal routing in DTE or DCE operation. Figure 27 illustrates a DCE or DTE controller-selectable interface. The DCE/$\overline{\text{DTE}}$ and INVERT inputs switch the port's mode of operation (Tables 1, 2).

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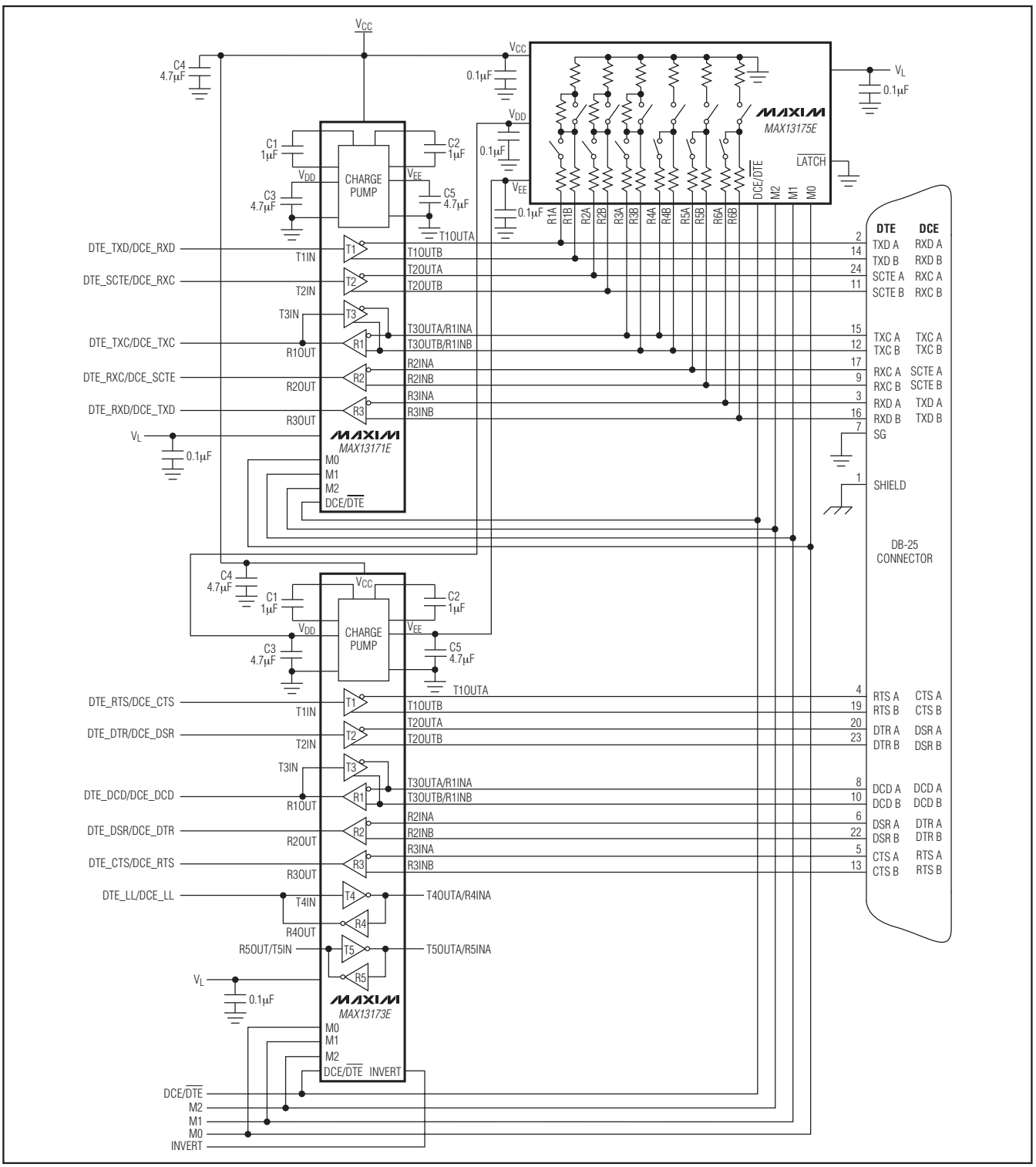


Figure 27. Controller-Selectable Multiprotocol DCE/DTE Port with DB-25 Connector

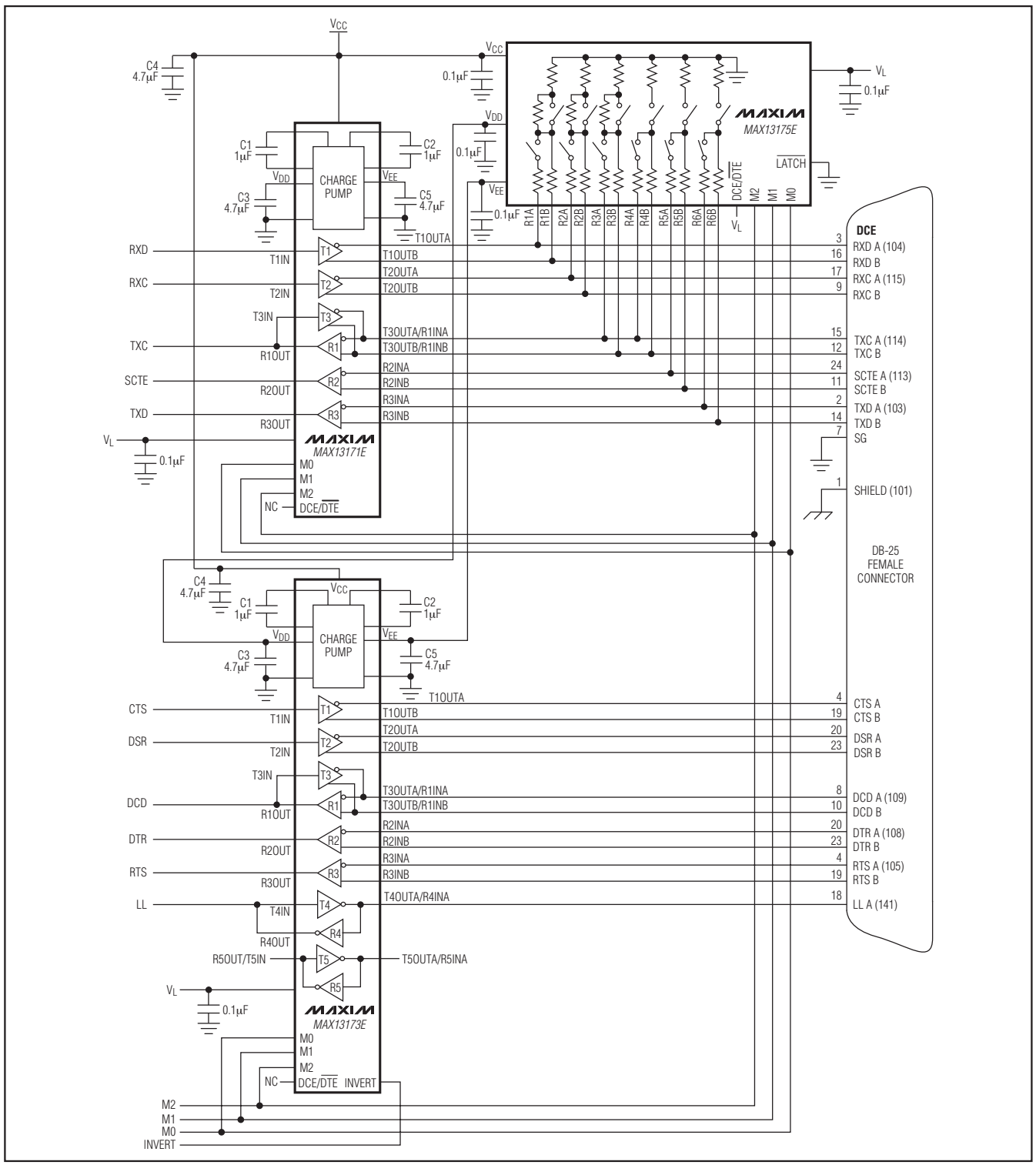


Figure 28. Controller-Selectable DCE Port with DB-25 Connector

Multiprotocol, Pin-Selectable Data Interface Chipset

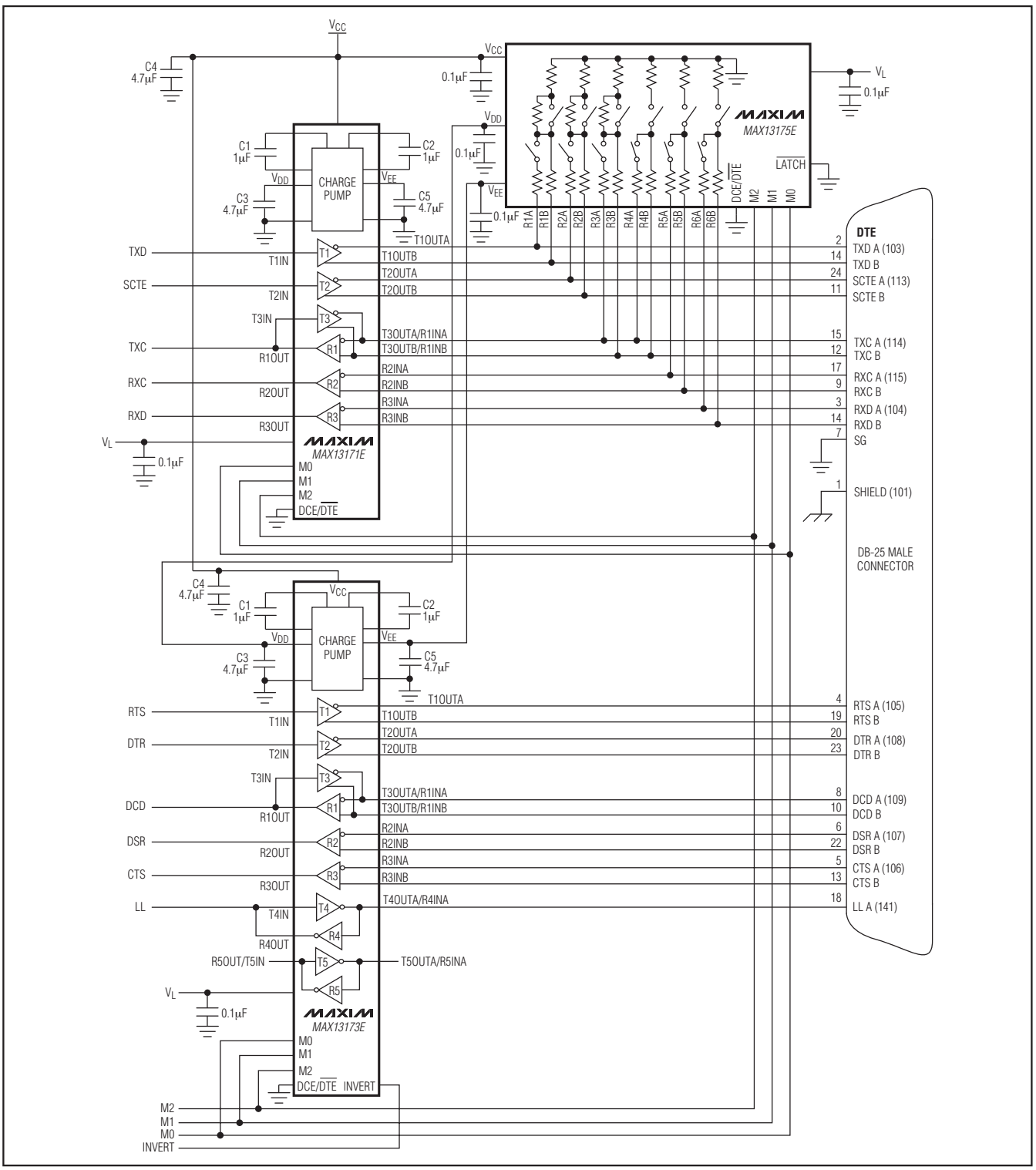


Figure 29. Controller-Selectable Multiprotocol DTE Port with DB-25 Connector

Complete Multiprotocol X.21 Interface

A complete DTE-to-DCE interface operating in X.21 mode is shown in Figure 30. The MAX13171E is used to generate the clock and data signals, and the MAX13173E generates the control signals and local loopback (LL). The MAX13175E is used to terminate the clock and data signals to support the V.11 protocol for cable termination. The control signals do not need external termination.

ESD Protection

ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs of the MAX13171E/MAX13173E have extra protection against static electricity. Maxim's engineers have developed state-of-the-art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, the MAX13171E/MAX13173E/MAX13175E keep working without latchup or damage. ESD protection can be tested in various ways. The *Electrical Characteristics* table shows the various limits for each device and they are characterized for protection to the following methods:

- Human Body Model
- Contact Method specified in IEC 61000-4-2
- Air-Gap Discharge Method specified in IEC 61000-4-2

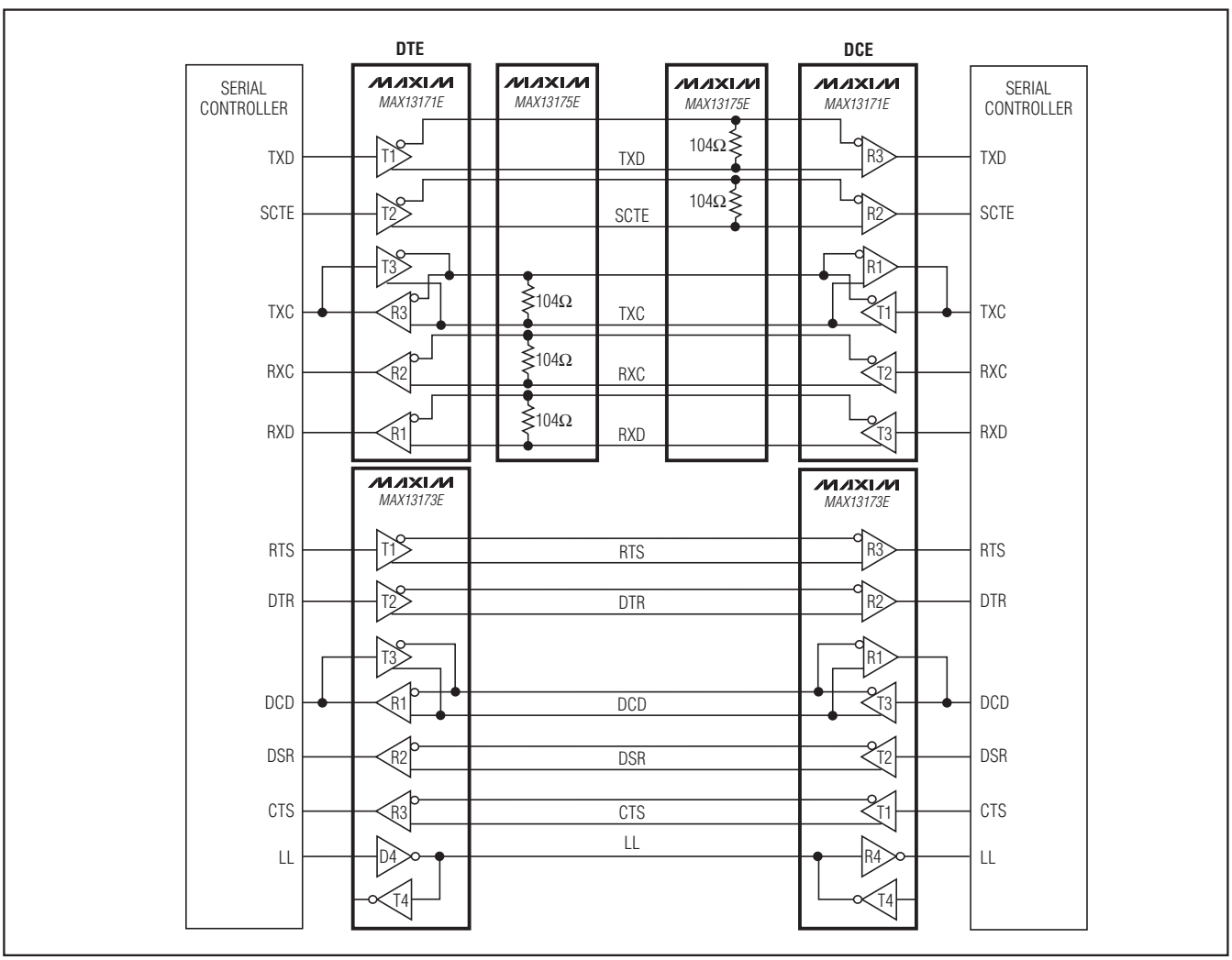


Figure 30. DCE-to-DTE X.21 Interface

Multiprotocol, Pin-Selectable Data Interface Chipset

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 31a shows the Human Body Model, and Figure 31b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The MAX13171E/MAX13173E/MAX13175E help equipment designs to meet IEC 61000-4-2, without the need for additional ESD-protection components.

The major difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Figure 31c shows the IEC 61000-4-2 model, and Figure 31d shows the current waveform for the IEC 61000-4-2 ESD Contact Discharge test.

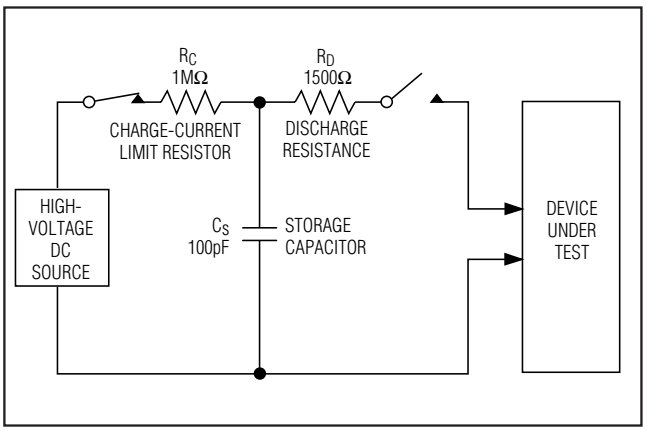


Figure 31a. Human Body ESD Test Model

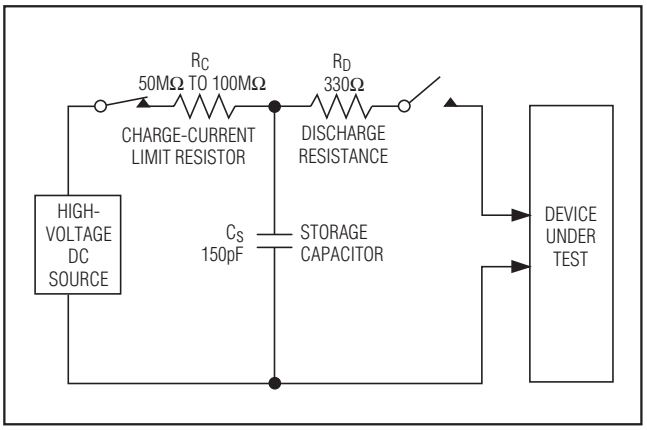


Figure 31c. ICE 61000-4-2 ESD Test Model

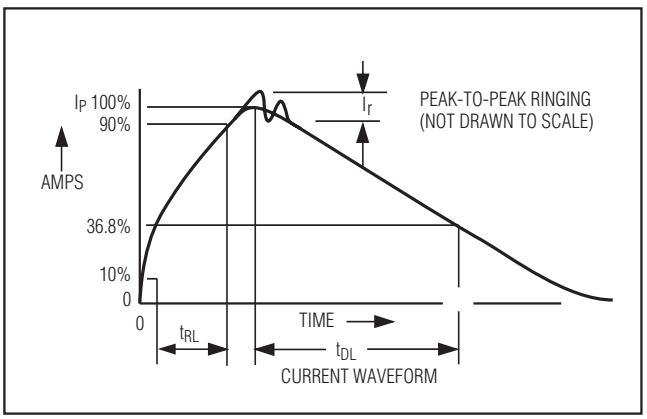


Figure 31b. Human Body Current Waveform

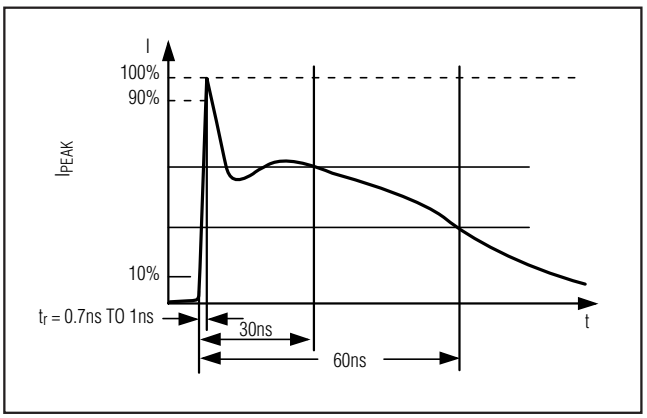
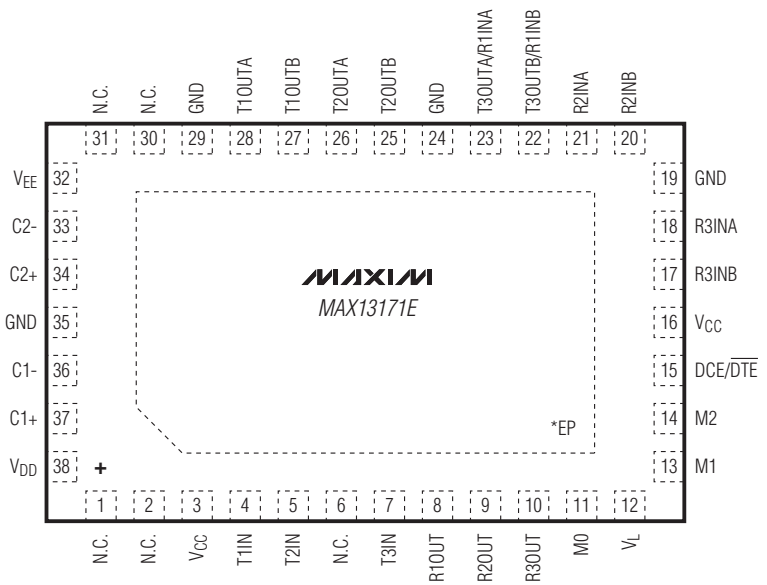


Figure 31d. IEC 61000-4-2 ESD Generator Current Waveform

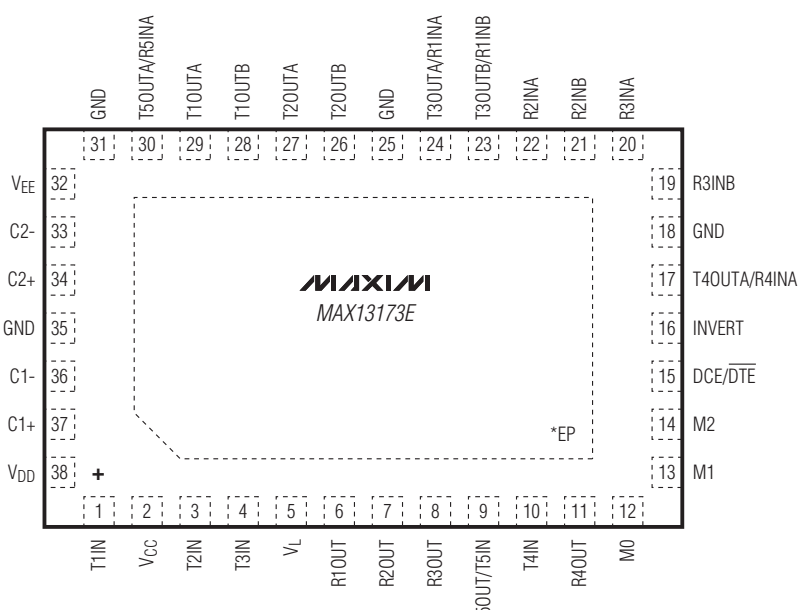
Pin Configurations

TOP VIEW



TQFN

*CONNECT EXPOSED PAD TO V_{EE}.



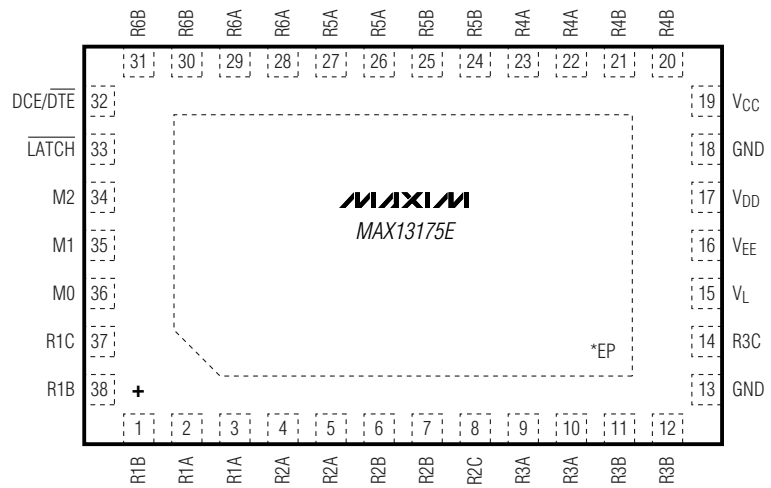
TQFN

*CONNECT EXPOSED PAD TO V_{EE}.

Multiprotocol, Pin-Selectable Data Interface Chipset

Pin Configurations (continued)

TOP VIEW



TQFN

*CONNECT EXPOSED PAD TO V_{EE}

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
38 TQFN-EP	T3857+1	21-0172	90-0076

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	4/10	Removed three external capacitors from Figure 17 and Figures 27–29	27, 32–34
3	8/11	Updated *Fail-Safe* and *Package Information* sections	23, 38

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