MAX14591 Evaluation Kit

Evaluates: MAX14591

General Description

The MAX14591 evaluation kit (EV kit) is a fully assembled and tested circuit board that demonstrates the functionality of the MAX14591 high-speed, open-drain capable logic-level translator in both the 8-bump WLP and 8-pin TDFN packages. Only the TDFN package device is installed in this EV kit. The EV kit enables direct evaluation of the device by multiple jumper-selectable methods. The highly configurable PCB allows the user to evaluate each package separately or both at once. Input power to the EV kit is provided by a micro-USB, type-B connector or an external 5V power supply. On-board LDO regulators provide the appropriate voltage for each component, and potentiometers allow the user to adjust the power supply for either side of the level translator independently.

Features and Benefits

- Proven PCB Layout
  - Decrease Evaluation Time
- Fully Assembled and Tested
- On-Board Adjustable Oscillators
  - Evaluate Without External Function Generator
- Jumper-Selectable Open-Drain and Push-Pull Buffers Enable Simple Evaluation

***Ordering Information* appears at end of data sheet.**

Quick Start

Required Equipment

- MAX14591 EV kit
- Digital voltmeter (DVM)
- USB power source or another 5V external power supply
- Oscilloscope and at least one scope probe

Procedure

The EV kit is fully assembled and tested. Follow the steps below to verify board operation and begin evaluation:

1) If using a USB bus to power the board, connect the included micro-USB cable between the micro-USB, type-B connector (J1) and the USB power source, such as a computer or dedicated USB charging port, and install a shunt on jumper JP4 shorting pins 1-2.
2) If using an external power source to power the board, connect the external power supply at the VBUS test point (TP26) and install a shunt on jumper JP4 shorting pins 2-3.
3) Connect the DVM between GND (TP6) and V_{CC} (TP24). Adjust the first potentiometer (POT1) until the desired voltage for V_{CC} appears on the DVM by turning the screw on the potentiometer to the right or to the left.
4) Connect the DVM between GND (TP6) and V_L (TP25). Adjust the second potentiometer (POT2) until the desired voltage for V_L appears on the DVM by turning the screw on the potentiometer to the right or to the left. Note that V_L should be lower than V_{CC}.
5) Connect the jumpers according to Table 1 to verify U2 (MAX14591ETA+) operation.
6) Connect the oscilloscope probe to TP19 I/OVCC2 and TP21 I/OVCC1 to observe the translated voltage of the input signal.

maxim integrated™

Table 1. Jumper Configuration (JP1–JP7, JP9–JP15, JP17–JP25)

JUMPER	SHUNT POSITION	DESCRIPTION
JP1	1-2*	Pullup resistor connect for I/OVL2 of U2. Connects a 1kΩ pullup resistor between V_L and I/OVL2.
	Not installed	Pullup resistor disconnect for I/OVL2 of U2. Disconnects the 1kΩ pullup resistor between V_L and I/OVL2.
JP2	1-2*	Connects open-drain buffer to driving signal bus for channel I/OVL1. The open-drain buffer is driven by the output of DS1090-16 (U4). The frequency of the signal is adjustable using POT3.
	1-3	Connects external source connected at TP9 to driving signal bus for channel I/OVL1.
	1-4	Connects push-pull buffer to driving signal bus for channel I/OVL1. The push-pull buffer is driven by the output of DS1090-1 (U5). The frequency of the signal is adjustable using POT4.
JP3	1-2*	Pullup resistor connect for I/OVCC2 of U2. Connects a 1kΩ pullup resistor between V_{CC} and I/OVCC2.
	Not installed	Pullup resistor disconnect for I/OVCC2 of U2. Disconnects the 1kΩ pullup resistor between V_{CC} and I/OVCC2.
JP4	1-2*	Power to the board supplied at the micro-USB connector (J1).
	2-3	Power to the board supplied at the external VBUS test point (TP26).
JP5	1-2*	Connects the open-drain buffer to driving signal bus for channel I/OVL2. The open-drain buffer is driven by the output of DS1090-16 (U4). The frequency of the signal is adjustable using POT3.
	1-3	Connects external source connected at TP13 to driving signal bus for channel I/OVL2.
	1-4	Connects push-pull buffer to driving signal bus for channel I/OVL2. The push-pull buffer is driven by the output of DS1090-1 (U5). The frequency of the signal is adjustable using POT4.
JP6	1-2*	Connects the $\overline{TS}$ pin of U1 to V_L, placing the device's I/O pins in normal operating mode.
	2-3	Connects the $\overline{TS}$ pin of U1 to GND, placing the device's I/O pins in high-impedance, three-state mode.
JP7	1-2	Pullup resistor connect for I/OVCC1 of U1. Connects a 1kΩ pullup resistor between V_{CC} and I/OVCC1.
	Not installed*	Pullup resistor disconnect for I/OVCC1 of U1. Disconnects the 1kΩ pullup resistor between V_{CC} and I/OVCC1.
JP9**	1-2	Connects I/OVCC1 of U1 to the driving signal bus for channel I/OVCC1.
	Not installed*	Disconnects I/OVCC1 of U1 from the driving signal bus for channel I/OVCC1.
JP10**	1-2	Connects I/OVCC1 of U2 to the driving signal bus for channel I/OVCC1.
	Not installed*	Disconnects I/OVCC1 of U2 from the driving signal bus for channel I/OVCC1.
JP11	1-2	Pullup resistor connect for I/OVL1 U1. Connects a 1kΩ pullup resistor between V_L and I/OVL1.
	Not installed*	Pullup resistor disconnect for I/OVL1 of U1. Disconnects the 1kΩ pullup resistor between V_L and I/OVL1.
JP12	1-2*	Connects open-drain buffer to driving signal bus for channel I/OVCC1. The open-drain buffer is driven by the output of DS1090-16 (U4). The frequency of the signal is adjustable using POT3.
	1-3	Connects external source connected at TP16 to driving signal bus for channel I/OVCC1.
	1-4	Connects push-pull buffer to driving signal bus for channel I/OVCC1. The push-pull buffer is driven by the output of DS1090-1 (U5). The frequency of the signal is adjustable using POT4.

Table 1. Jumper Configuration (JP1–JP7, JP9–JP15, JP17–JP25) (continued)

JUMPER	SHUNT POSITION	DESCRIPTION
JP13	1-2	Pullup resistor connect for I/OVL2 of MAX14591EWA+ (U1). Connects a 1kΩ pullup resistor between V_L and I/OVL2.
	Not installed*	Pullup resistor disconnect for I/OVL2 of MAX14591EWA+ (U1). Disconnects the 1kΩ pullup resistor between V_L and I/OVL2.
JP14	1-2	Pullup resistor connect for I/OVCC2 of MAX14591EWA+ (U1). Connects a 1kΩ pullup resistor between V_{CC} and I/OVCC2.
	Not installed*	Pullup resistor disconnect for I/OVCC2 of MAX14591EWA+ (U1). Disconnects the 1kΩ pullup resistor between V_{CC} and I/OVCC2.
JP15**	1-2	Connects I/OVCC2 of U1 to the driving signal bus for channel I/OVCC2.
	Not installed*	Disconnects I/OVCC2 of U1 from the driving signal bus for channel I/OVCC2.
JP17	1-2*	Connects open-drain buffer to driving signal bus for channel I/OVCC2. The open-drain buffer is driven by the output of DS1090-16 (U4). The frequency of the signal is adjustable using POT3.
	1-3	Connects external source connected at TP17 to driving signal bus for channel I/OVCC2.
	1-4	Connects push-pull buffer to driving signal bus for channel I/OVCC2. The push-pull buffer is driven by the output of DS1090-1 (U5). The frequency of the signal is adjustable using POT4.
JP18	1-2*	Pullup resistor connect for I/OVL1 of U2. Connects a 1kΩ pullup resistor between V_L and I/OVL1.
	Not installed	Pullup resistor disconnect for I/OVL1 of U2. Disconnects the 1kΩ pullup resistor between V_L and I/OVL1.
JP19	1-2*	Pullup resistor connect for I/OVCC1 of U2. Connects a 1kΩ pullup resistor between V_{CC} and I/OVCC1.
	Not installed	Pullup resistor disconnect for I/OVCC1 of U2. Disconnects the 1kΩ pullup resistor between V_{CC} and I/OVCC1.
JP20**	1-2	Connects I/OVCC2 of U2 to the driving signal bus for channel I/OVCC2.
	Not installed*	Disconnects I/OVCC2 of U2 from the driving signal bus for channel I/OVCC2.
JP21**	1-2	Connects I/OVL2 of U1 to the driving signal bus for channel I/OVL2.
	Not installed*	Disconnects I/OVL2 of U1 from the driving signal bus for channel I/OVL2.
JP22**	1-2*	Connects I/OVL2 of U2 to the driving signal bus for channel I/OVL2.
	Not installed	Disconnects I/OVL2 of U2 from the driving signal bus for channel I/OVL2.
JP23**	1-2	Connects I/OVL1 of U1 to the driving signal bus for channel I/OVL1.
	Not installed*	Disconnects I/OVL1 of U1 from the driving signal bus for channel I/OVL1.
JP24	1-2*	Connects $\overline{TS}$ pin of U2 to V_L, placing the device's I/O pins in normal operating mode.
	2-3	Connects $\overline{TS}$ pin of U2 to GND, placing the device's I/O pins in high-impedance three-state mode.
JP25**	1-2*	Connects I/OVL1 of U2 to the driving signal bus for channel I/OVL1.
	Not installed	Disconnects I/OVL1 of U2 from the driving signal bus for channel I/OVL1.

**Default jumper setting.*

***The following pairs are mutually exclusive. Do not connect both of any of the following pairs at the same time: JP9 and JP23, JP10 and JP25, JP15 and JP21, and JP20 and JP22.*

Detailed Description of Hardware

The MAX14591 EV kit is a fully assembled and tested circuit board that demonstrates the functionality of the MAX14591 high-speed, open-drain capable logic-level translator in both the 8-bump WLP and 8-pin TDFN packages. The EV kit features enables direct evaluation of the device by multiple jumper-selectable methods. The highly configurable PCB allows the user to evaluate each package separately or both at once. Input power to the EV kit is provided by a micro-USB, type-B connector or an external 5V power supply. On-board LDO regulators provide the appropriate voltage for each component, and potentiometers allow the user to adjust the power supply for either side of the level translator independently. The EV kit's PCB is designed with 1oz copper.

Power Supply

The EV kit is powered by a user-supplied 5V external DC power supply connected between the V_{BUS} test point (TP26) and GND, or the USB bus provided at the micro-USB connector (J1). The power supply is then converted into three independent voltages. The pin-selectable output voltage of the MAX8902A (U3) provides a 4.6V supply for peripherals such as the NC7WZ07 open-drain buffer, as well as for the DS1090 EconOscillators™. Two separate MAX8902B ICs are used to generate the power for the V_{CC} and V_L supplies on the MAX14591. The V_{CC} supply is generated by U6, which also provides power to the push-pull buffer for the V_{CC} channels (U10). The VL supply is generated by U7, which also provides power to the push-pull buffer for the V_L channels (U8).

On-Board Oscillators

The EV kit features two on-board oscillators to generate input signals to the device. The DS1090-1 (U5) is used to generate a potentiometer-adjustable clock from 4MHz to 8MHz, while the DS1090-16 (U4) generates a potentiometer adjustable clock from 250kHz to 500kHz. These clock signals can be connected to individual channels using 4-way jumpers JP2, JP5, JP12, and JP17 (Table 1).

Push-Pull and Open-Drain Evaluation

Each channel can be driven in either push-pull mode or open-drain mode. For evaluation of push-pull operation or low-speed open-drain operation, use the on-board oscillators. Simply connect the open-drain buffer or push-pullbuffer through one of the 4-way jumpers to the channel to be driven to begin evaluation. See Table 1 for jumper configurations. For high-speed open-drain operation, an external function generator is required.

Component Suppliers

SUPPLIER	WEBSITE
Hirose Electric Co., Ltd.	www.hirose-connectors.com
Murata Americas	www.murataamericas.com
Stanley Electric Co., Ltd.	www.stanley-components.com

Note: *Indicate that you are using the MAX14591 when contacting these component suppliers.*

EconOscillator is a trademark of Maxim Integrated Products, Inc.

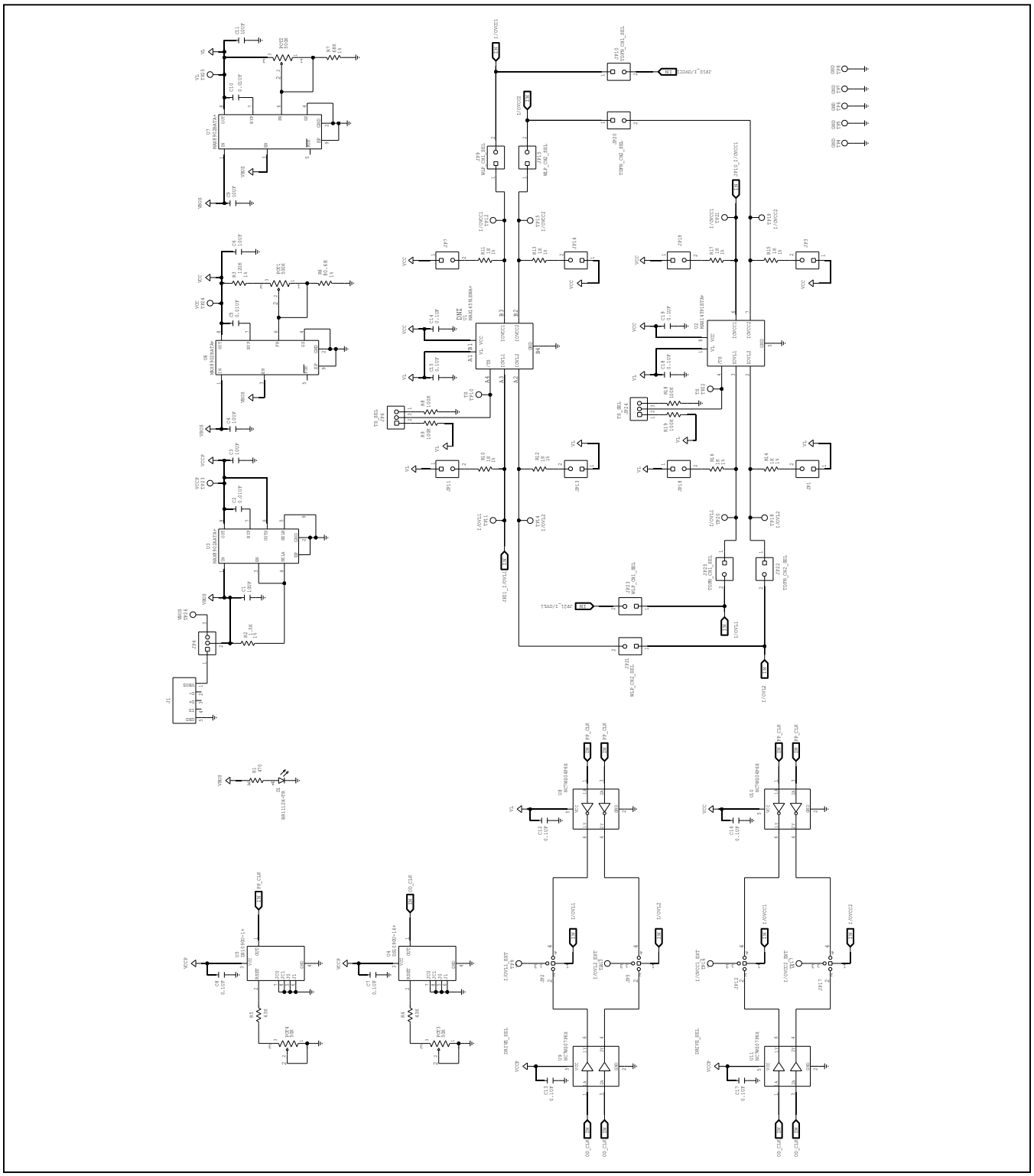
MAX14591 EV Kit Bill of Materials

ITEM	REF_DES	DNI/DNP	QTY	MFG PART #	MFG	VALUE	DESCRIPTION
1	C1, C3, C4, C6, C9, C11	-	6	C0805C106K9PAC; GRM21BR60J106K	KEMET;MURATA	10UF	CAPACITOR; SMT (0805); CERAMIC CHIP; 10UF; 6.3V; TOL=10%; MODEL=; TG=-55 DEGC TO +125 DEGC; TC=X5R;
2	C2, C5, C10	-	3	GRM188R71C103KA01; ECJ-1VB1C10; CL10B103KO8NNN; GCJ188R71C103KA01	MURATA;PANASONIC;SAMSUNG; MURATA	0.01UF	CAPACITOR; SMT (0603); CERAMIC CHIP; 0.01UF; 16V; TOL=10%; TG=-55 DEGC TO +125 DEG; TC=X7R
3	C7, C8, C12-C19	-	10	C0603C104K4RAC; GCM188R71C104KA37; C1608X7R1C104K; GRM188R71C104KA01; C0603X7R160-104KNE; C0603C104K4RACAUTO; VJ0603Y104KXJCW1BC; 0603YC104KAT4A; 885012206046	KEMET; MURATA; TDK; MURATA;VENKEL LTD; KEMET; VISHAY DALE; AVX; WURTH ELECTRONICS INC	0.1UF	CAPACITOR; SMT (0603); CERAMIC CHIP; 0.1UF; 16V; TOL=10%; TG=-55 DEGC TO +125 DEGC; TC=X7R;
4	D1	-	1	BR1112H-TR	STANLEY ELECTRIC CO.	BR1112H-TR	DIODE; LED; 1112H SERIES; RED; SMT(0805); PIV=4.0V; IF=0.025A
5	J1	-	1	ZX62D-B-5PA8	HIROSE ELECTRIC CO LTD.	ZX62D-B-5PA8	CONNECTOR; MALE; THROUGH HOLE; MICRO-USB CONNECTOR; RIGHT ANGLE; 5PINS
6	JP1, JP3, JP7, JP9-JP11, JP13-JP15, JP18-JP23, JP25	-	16	" 22-28-4023"	MOLEX	" 22-28-4023"	CONNECTOR; MALE; THROUGH HOLE; FLAT VERTICAL BREAKAWAY; STRAIGHT; 2PINS
7	JP2, JP5, JP12, JP17	-	4	" 22-28-4043"	MOLEX	" 22-28-4043"	CONNECTOR; MALE; THROUGH HOLE; FLAT VERTICAL BREAKAWAY; STRAIGHT; 4PINS
8	JP4, JP6, JP24	-	3	" 22-28-4033"	MOLEX	" 22-28-4033"	CONNECTOR; MALE; THROUGH HOLE; FLAT VERTICAL BREAKAWAY; STRAIGHT; 3PINS
9	POT1, POT2	-	2	PV37W504C01B00	MURATA	500K	RESISTOR; THROUGH-HOLE-RADIAL LEAD; 500K OHM; 10%; 150PPM; 0.25W; MOLDER CERAMIC OVER METAL FILM
10	POT3, POT4	-	2	PV37W503C01B00	MURATA	50K	RESISTOR; THROUGH-HOLE-RADIAL LEAD; 50K OHM; 10%; 150PPM; 0.25W; MOLDER CERAMIC OVER METAL FILM
11	R1	-	1	ERJ-6GEYJ471	PANASONIC	470	RESISTOR; 0805; 470 OHM; 5%; 200PPM; 0.125W; THICK FILM
12	R2	-	1	CRCW08051K50FK; MCR10EZPF1501	VISHAY DALE/ROHM	1.5K	RESISTOR, 0805, 1.5K OHM, 1%, 100PPM, 0.125W, THICK FILM
13	R3	-	1	CRCW0805120KFK	VISHAY DALE	120K	RESISTOR, 0805, 120K OHM, 1%, 100PPM, 0.125W, THICK FILM
14	R4, R5	-	2	ERJ-6GEYJ433	PANASONIC	43K	RESISTOR; 0805; 43K OHM; 5%; 200PPM; 0.125W; THICK FILM
15	R6	-	1	CRCW080580K6FK	VISHAY DALE	80.6K	RESISTOR; 0805; 80.6K OHM; 1%; 100PPM; 0.125W; THICK FILM
16	R7	-	1	CRCW080568K0FK	VISHAY DALE	68K	RESISTOR; 0805; 68K OHM; 1%; 100PPM; 0.125W; THICK FILM
17	R8, R9, R18, R19	-	4	ERJ-6GEYJ104	PANASONIC	100K	RESISTOR; 0805; 100K OHM; 5%; 200PPM; 0.125W; THICK FILM
18	R10-R17	-	8	CRCW08051K00FK;ERJ-6ENF1001;MCR10EZHF1001;RC0805FR-071KL	VISHAY DALE;PANASONIC;ROHM;YAGEO	1K	RESISTOR; 0805; 1K; 1%; 100PPM; 0.125W; THICK FILM
19	TP4-TP8	-	5	5011	KEYSTONE	N/A	TEST POINT; PIN DIA=0.125IN; TOTAL LENGTH=0.445IN; BOARD HOLE=0.063IN; BLACK; PHOSPHOR BRONZE WIRE SILVER PLATE FINISH;
20	TP9, TP10, TP13, TP16, TP17, TP22	-	6	5012	KEYSTONE	N/A	TEST POINT; PIN DIA=0.125IN; TOTAL LENGTH=0.445IN; BOARD HOLE=0.063IN; WHITE; PHOSPHOR BRONZE WIRE SILVER PLATE FINISH;
21	TP11, TP12, TP14, TP15, TP18-TP21	-	8	5014	KEYSTONE	N/A	TEST POINT; PIN DIA=0.125IN; TOTAL LENGTH=0.445IN; BOARD HOLE=0.063IN; YELLOW; PHOSPHOR BRONZE WIRE SILVER PLATE FINISH;

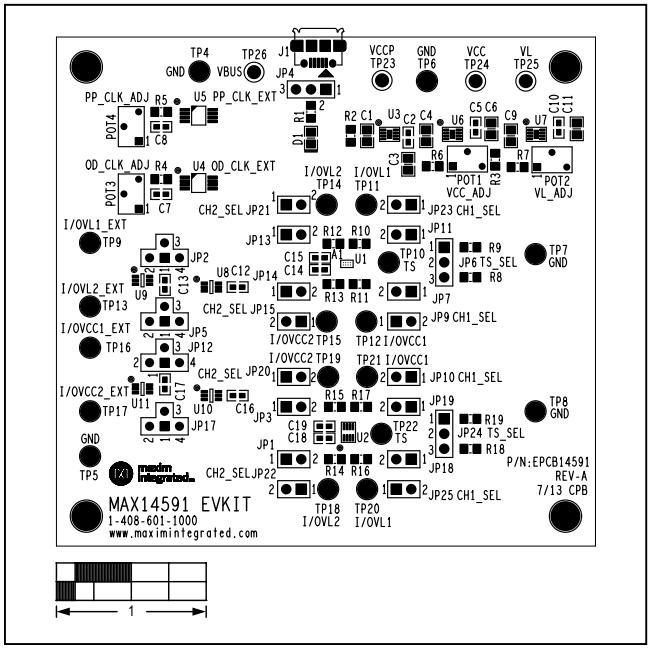
MAX14591 EV Kit Bill of Materials

ITEM	REF_DES	DNI/DNP	QTY	MFG PART #	MFG	VALUE	DESCRIPTION
22	TP23-TP26	-	4	5010	KEYSTONE	N/A	TESTPOINT WITH 1.80MM HOLE DIA, RED, MULTIPURPOSE;
23	U2	-	1	MAX14591ETA+	MAXIM	MAX14591ETA+	IC; TRANS; HIGH-SPEED; OPEN-DRAIN CAPABLE LOGIC-LEVEL TRANSLATOR; TDFN8
24	U3	-	1	MAX8902AATA+	MAXIM	MAX8902AATA+	IC; VREG; LOW-NOISE LDO REGULATOR PIN-SELECTABLE OUTPUT VOLTAGE; TDFN8 2X2
25	U4	-	1	DS1090U-16+	MAXIM	DS1090U-16+	IC; PSCLR; 250KHZ TO 500KHZ; LOW-FREQUENCY; SPREAD-SPECTRUM; ECONOSCILLATOR; USOP8
26	U5	-	1	DS1090U-1+	MAXIM	DS1090U-1+	IC; PSCLR; 4MHZ TO 8MHZ; LOW-FREQUENCY; SPREAD-SPECTRUM; ECONOSCILLATOR; USOP8
27	U6, U7	-	2	MAX8902BATA+	MAXIM	MAX8902BATA+	IC; VREG; LOW-NOISE LDO REGULATOR; TDFN8 2X2
28	U8, U10	-	2	NC7WZ04P6X	FAIRCHILD SEMI	NC7WZ04P6X	IC; INV; TINY LOGIC ULTRA-HIGH SPEED DUAL INVERTER; SC70-6
29	U9, U11	-	2	NC7WZ07P6X	FAIRCHILD SEMI	NC7WZ07P6X	IC; BUF; TINY LOGIC ULTRA-HIGH SPEED DUAL BUFFER; SC70-6
30	XJP1-XJP7, XJP9-XJP11, XJP13, XJP14, XJP18, XJP19, XJP23-XJP25	-	17	S1100-B;SX1100-B;STC02SYAN	KYCON; KYCON; SULLINS ELECTRONICS CORP.	SX1100-B	TEST POINT; JUMPER; STR; TOTAL LENGTH=0.24IN; BLACK; INSULATION=PBT;PHOSPHOR BRONZE CONTACT=GOLD PLATED
31	PCB	-	1	MAX14591	MAXIM	PCB	PCB:MAX14591
32	U1	DNP	0	MAX14591EWA+	MAXIM	MAX14591EWA+	IC; TRANS; HIGH-SPEED; OPEN-DRAIN CAPABLE LOGIC-LEVEL TRANSLATOR; WLP8
TOTAL			118				
NOTE: DNI--> DO NOT INSTALL(PACKOUT) ; DNP--> DO NOT PROCURE							

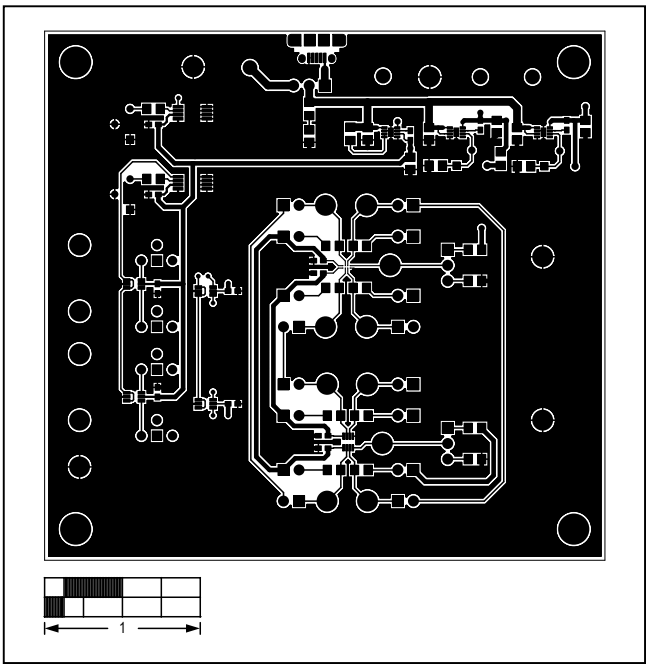
MAX14591 EV Kit Schematic



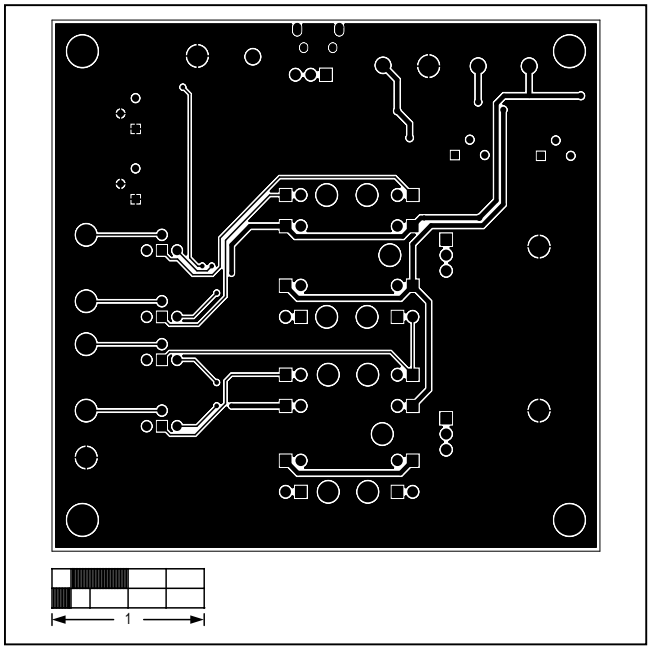
MAX14591 EV Kit PCB Layout Diagrams



MAX14591 EV Kit Component Placement Guide



MAX14591 EV Kit Layout—Component Side



MAX14591 EV Kit Layout—Solder Side

Ordering Information

PART	TYPE
MAX14591EVKIT#	EV Kit

#Denotes RoHS compliant.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/13	Initial release	—
1	3/19	Updated *General Description, Quick Start, Table 1, Bill of Materials*, and *Schematic*	1–6

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at https://www.maximintegrated.com/en/storefront/storefront.html.

Maxim Integrated cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim Integrated product. No circuit patent licenses are implied. Maxim Integrated reserves the right to change the circuitry and specifications without notice at any time.

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Interface Development Tools ***category:***

Click to view products by Maxim ***manufacturer:***

Other Similar products are found below :

ADP5585CP-EVALZ CHA2066-99F AS8650-DB MLX80104 TESTINTERFACE 416100120-3 XR18910ILEVB XR21B1421IL28-0A-EVB TW-DONGLE-USB EVAL-ADM2491EEBZ MAXREFDES23DB# MAX13235EEVKIT DFR0257 XR22404CG28EVB ZLR964122L ZLR88822L EVK-U23-01S EVK-W262U-00 DC327A PIM511 PIM536 PIM517 DEV-17512 STR-FUSB3307MPX-PPS-GEVK MAXREFDES177# EVAL-ADM2567EEBZ ZSSC3240KIT MAX9121EVKIT PIM532 ZSC31010KITV2P1 UMFT4233HPEV LVDS-18B-EVK XR20M1170G16-0B-EB XR20M1170G24-0B-EB XR20M1172G28-0A-EB XR20M1172G28-0B-EB SI871XSOIC8-KIT 1764 1833 1862 EVB-USB82514 ATA6628-EK ATA6631-EK EVAL-CN0313-SDPZ 2264 MCP23X17EV PS081-EVA-HR MODULE 237 SMA2RJ45EVK/NOPB FR12-0002 MAFR-000455-001