EVALUATION KIT AVAILABLE

MAX14808/MAX14809

Octal Three-Level/Quad Five-Level High-Voltage 2A Digital Pulsers with T/R Switch

General Description

The MAX14808/MAX14809 octal three-level/quad five-level, high-voltage (HV) pulser devices generate high-frequency HV bipolar pulses (up to ±105V) from low-voltage control logic inputs for driving piezoelectric transducers in ultrasound systems. All eight channels have embedded overvoltage-protection diodes and an integrated active return-to-zero clamp. Both devices have embedded independent (floating) power supplies (FPS) and level shifters that allow signal transmission without the need for external HV capacitors. The MAX14808 also features eight integrated transmit/receive (T/R) switches. The MAX14809 does not have the T/R switch function.

The devices feature two modes of operation: an octal three-level pulser mode (with integrated active return-to-zero clamp) or a quad five-level pulser mode. In octal three-level pulser mode, each channel is controlled by two logic inputs (DINN_/DINP_) and the active return to zero features half the current driving of the pulser 1A (typ). In quad five-level pulser mode, each channel is controlled by three logic inputs and the active return to zero has the same current driving of the pulser 2A (typ).

The devices can operate both in clocked and transparent mode. In clocked mode, data inputs can be synchronized with a clean differential or single-ended clock to reduce phase noise associated with FPGA output signals that are detrimental for Doppler analysis. In transparent mode, the synchronization feature is disabled and output reflects the data input after a 18ns delay. Both devices feature adjustable maximum current (0.5A to 2A) to reduce power consumption when full current capability is not required.

The devices feature integrated grass-clipping diodes (with low parasitic capacitance) for receive (Rx) and transmit (Tx) isolations. Both devices feature a damping circuit that can be activated as soon as the transmit burst is over. The damping circuit has a typical on-resistance of 500Ω. It fully discharges the pulser's output internal node before the grass-clipping diodes.

The devices are available in a 68-pin (10mm x 10mm) TQFN package with an exposed pad and are specified over the -40°C to +85°C extended temperature range.

Benefits and Features

- **Save Space (Optimized for High-Channel-Count Systems/Portable Systems)**
  - **High Density**
    - **8 Channels (Three-Level Operation)**
    - **4 Channels (Five-Level Operation) in One Package**
  - **Integrated Low-Power T/R Switches (MAX14808)**
  - **DirectDrive® Architecture Eliminates External High-Voltage Capacitor**
  - **No External Floating Power Supply (FPS) Required**
- **High Performance (Designed to Enhance Image Quality)**
  - **Excellent -43dBc (typ) THD for Second Harmonic at 5MHz**
  - **Sync Function Eliminates Effects of FPGA Jitter and Improves Performance in Doppler Mode**
  - **Low Propagation Delay 18ns (typ)**
  - **Strong Active Return to Zero**
- **Save Power**
  - **Low Quiescent Power Dissipation (5.7mW/Channel in Octal Mode)**
  - **Programmable Current Capability**
  - **Shutdown Mode and Disable Transmit Mode**

Applications

Ultrasound Medical Imaging

Industrial Flaw Detection

Piezoelectric Drivers

Test Equipment

***Ordering Information* and *Functional Diagram* appear at end of data sheet.**

DirectDrive is a registered trademark of Maxim Integrated Products, Inc.

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX14808.related.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-6438; Rev 2; 1/14

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{DD} Logic Supply Voltage Range .....-0.3V to +5.6V
V_{CC} Positive Driver Supply Voltage Range .....-0.3V to +5.6V
V_{EE} Negative Driver Supply Voltage Range.....-5.6V to +0.3V
V_{NNA}, V_{NNB} High Negative Supply Voltage Range.....-110V to +0.3V
V_{PPA}, V_{PPB} High Positive Supply Voltage Range.....-0.3V to +110V
OUT_ Output Voltage Range .....$V_{NN\_}$ to $V_{PP\_}$
LVOUT_ Output Voltage Range (100mA Maximum Current).....-1.2V to +1.2V
DINN_, DINP_, CC_, SYNC, $\overline{LDO\_EN}$.....-0.3V to +5.6V
CLK, $\overline{CLK}$, MODE_ Voltage Range..... -0.3V to (V_{CC} + 0.3V)
THP Logic Output Voltage Range.....-0.3V to +5.6V
V_{GPA}, V_{GPB} Output Voltage Range .....max[($V_{PP\_}$ - 5.6V), (V_{EE} + 0.6V)] to ($V_{PP\_}$ + 0.3V)
V_{GNA}, V_{GNB} Output Voltage Range .....($V_{NN\_}$ - 0.3V) to min[(V_{CC} + 0.6V), ($V_{NN\_}$ + 5.6V)]
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 50mW/°C above +70°C) 4000mW
Operating Temperature Range ..... -40°C to +85°C
Maximum Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}).....20°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....0.5°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = +3V, V_{CC} = +5V, V_{EE} = -5V, V_{PPA} = +100V, V_{NNA} = -100V, V_{PPB} = +100V, V_{NNB} = -100V, 1µF bypass capacitor between V_{GNA} and V_{NNA}, 1µF bypass capacitor between V_{GNB} and V_{NNB}, 1µF bypass capacitor between V_{GPA} and V_{PPA}, 1µF bypass capacitor between V_{GPB} and V_{PPB}, $V_{\overline{LDO\_EN}}$ = 0V, no load, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES (V_{DD}, V_{CC}, V_{EE}, $V_{PP\_}$, $V_{NN\_}$)						
Logic Supply Voltage	V_{DD}		+1.7	+3	+5.25	V
Positive Drive Supply Voltage	V_{CC}		+4.9	+5	+5.1	V
Negative Drive Supply Voltage	V_{EE}		-5.1	-5	-4.9	V
High-Side Supply Voltage	$V_{PP\_}$		0		+105	V
Low-Side Supply Voltage	$V_{NN\_}$		-105		0	V
External Low-Side LDO Voltage	$V_{GN\_}$ - $V_{NN\_}$	$\overline{LDO\_EN}$ = high	5	5.3	5.5	V
External High-Side LDO Voltage	$V_{PP\_}$ - $V_{GP\_}$	$\overline{LDO\_EN}$ = high	5	5.3	5.5	V
External Floating Power-Supply Current from $V_{GN\_}$	$I_{VGN\_}$	$\overline{LDO\_EN}$ = high (Note 3)	50			mA
External Floating Power-Supply Current from $V_{GP\_}$	$I_{VGP\_}$	$\overline{LDO\_EN}$ = high (Note 3)	85			mA
LOGIC INPUTS/OUTPUTS (DINN_, DINP_, MODE_, SYNC, CC_, $\overline{LDO\_EN}$)						
Low-Level Input Threshold	V_{IL}				0.2 x V_{DD}	V
High-Level Input Threshold	V_{IH}		0.8 x V_{DD}			V
Logic Input Capacitance	C_{IN}			4		pF

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3V, V_{CC} = +5V, V_{EE} = -5V, V_{PPA} = +100V, V_{NNA} = -100V, V_{PPB} = +100V, V_{NNB} = -100V, 1µF bypass capacitor between V_{GNA} and V_{NNA}, 1µF bypass capacitor between V_{GNB} and V_{NNB}, 1µF bypass capacitor between V_{GPA} and V_{PPA}, 1µF bypass capacitor between V_{GPB} and V_{PPB}, $V_{\overline{LDO\_EN}}$ = 0V, no load, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Logic Input Leakage (All Inputs Except $\overline{LDO\_EN}$)	I_{IN}	V_{IN} = 0V or V_{DD}		-1	0	+1	µA
$\overline{LDO\_EN}$ Pulldown Resistance	$R_{\overline{LDO\_EN}}$			7	10	14	kΩ
THP Low-Level Output Voltage	V_{OL}	Pullup resistor to V_{DD} (R_{PULLUP} = 1kΩ)				0.1 x V_{DD}	V
CLOCK INPUTS (CLK, $\overline{CLK}$)—DIFFERENTIAL MODE							
Differential Clock Input Voltage Range	V_{CLKD}			0.2		2	V_{P-P}
Common-Mode Voltage	V_{CLKCM}				V_{CC}/2		V
Common-Mode Voltage Range	V_{CL}			V_{CC}/2 - 0.45		V_{CC}/2 + 0.45	V
Input Resistance	R_{CLK}, $R_{\overline{CLK}}$	Differential			7		kΩ
		Common mode			23		kΩ
Input Capacitance	C_{CLK}, $C_{\overline{CLK}}$	Capacitance to GND (each input)			4		pF
CLOCK INPUTS (CLK, $\overline{CLK}$)—SINGLE-ENDED MODE ($V_{\overline{CLK}}$ < 0.1V)							
Low-Level Input	V_{IL}	CLK				0.2 x V_{DD}	V
High-Level Input	V_{IH}	CLK		0.8 x V_{DD}			V
Single-Ended Mode Selection Threshold Low	V_{IL}	$\overline{CLK}$				0.1	V
Single-Ended Mode Selection Threshold High	V_{IH}	$\overline{CLK}$		1			V
Input Capacitance (CLK)	C_{CLK}				4		pF
Logic Input Leakage (CLK)	I_{CLK}	V_{CLK} = 0V or V_{DD}		-1	0	+1	µA
Pullup Current ($\overline{CLK}$)	$I_{\overline{CLK}}$	$V_{\overline{CLK}}$ = 0V			120	180	µA
SUPPLY CURRENT—SHUTDOWN MODE (MODE0 = Low, MODE1 = Low)							
V_{DD} Supply Current	I_{DD}	All inputs connected to GND or V_{DD}				3	µA
V_{CC} Supply Current	I_{CC}	All inputs connected to GND or V_{DD}				22	µA
V_{EE} Supply Current	I_{EE}	All inputs connected to GND or V_{DD}				13	µA
$V_{PP\_}$ Supply Current	$I_{PP\_}$	All inputs connected to GND or V_{DD}				10	µA
$V_{NN\_}$ Supply Current	$I_{NN\_}$	All inputs connected to GND or V_{DD}				10	µA
SUPPLY CURRENT—DISABLE MODE (MODE0 = High, MODE1 = High)							
V_{DD} Supply Current	I_{DDQ}	All inputs connected to GND or V_{DD}	Transparent or single-ended clock mode		1.7	3	µA
			Differential clock mode, V_{CLKD} = 0.2V		110	190	

DC ELECTRICAL CHARACTERISTICS (continued)

((V_{DD} = +3V, V_{CC} = +5V, V_{EE} = -5V, V_{PPA} = +100V, V_{NNA} = -100V, V_{PPB} = +100V, V_{NNB} = -100V, 1µF bypass capacitor between V_{GNA} and V_{NNA}, 1µF bypass capacitor between V_{GNB} and V_{NNB}, 1µF bypass capacitor between V_{GPA} and V_{PPA}, 1µF bypass capacitor between V_{GPB} and V_{PPB}, $V_{\overline{LDO\_EN}}$ = 0V, no load, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{EE} Supply Current	I_{EEQ}	DINN_ = DINP_ = GND			0.26	0.4	mA
		DINN_ = DINP_ = V_{DD}	MAX14808		9.4	13	
			MAX14809		1.37	2	
V_{CC} Supply Current	I_{CCQ}	DINN_ = DINP_ = GND			0.49	0.75	mA
		DINN_ = DINP_ = V_{DD}	MAX14808		9.6	13.2	
			MAX14809		1.6	2.3	
V_{CC} Supply Current Increase in Clocked Mode	ΔI_{CC}	Differential clock mode			3.5	5	mA
$V_{NN\_}$ Total Supply Current (Quiescent Mode)	$I_{NNQ\_}$	All inputs connected to GND or V_{DD}			195	305	µA
$V_{PP\_}$ Total Supply Current (Quiescent Mode)	$I_{PPQ\_}$	All inputs connected to GND or V_{DD}			220	340	µA
Total Power Dissipation per Channel (Disable Mode)	P_{PDIS1}	T/R switch off, damp off (transparent mode)			5.7		mW
	P_{PDIS2}	DINN_ = DINP_ = V_{DD}	MAX14808		17		
			MAX14809		7		
SUPPLY CURRENT—OCTAL THREE-LEVEL MODE, NO LOAD (MODE0 = High, MODE1 = Low)							
V_{DD} Supply Current (Quiescent Mode)	I_{DD}	All inputs connected to GND or V_{DD}	Transparent or single-ended clock mode		1.7	3	µA
			Differential clock mode, V_{CLKD} = 0.2V		110	190	
V_{EE} Supply Current (Quiescent Mode)	I_{EEQ}	DINN_ = DINP_ = GND			0.26	0.4	mA
		DINN_ = DINP_ = V_{DD}	MAX14808		9.4	13	
			MAX14809		1.37	2	
V_{CC} Supply Current (Quiescent Mode)	I_{CCQ}	DINN_ = DINP_ = GND			0.49	0.75	mA
		DINN_ = DINP_ = V_{DD}	MAX14808		9.6	13.2	
			MAX14809		1.6	2.3	
V_{CC} Supply Current Increase in Clocked Mode	ΔI_{CC}	Differential clock mode			3.5	5	mA
$V_{NN\_}$ Total Supply Current (Quiescent Mode)	$I_{NNQ\_}$	All inputs connected to GND or V_{DD}			195	305	µA
$V_{PP\_}$ Total Supply Current (Quiescent Mode)	$I_{PPQ\_}$	All inputs connected to GND or V_{DD}			220	340	µA

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3V, V_{CC} = +5V, V_{EE} = -5V, V_{PPA} = +100V, V_{NNA} = -100V, V_{PPB} = +100V, V_{NNB} = -100V, 1µF bypass capacitor between V_{GNA} and V_{NNA}, 1µF bypass capacitor between V_{GNB} and V_{NNB}, 1µF bypass capacitor between V_{GPA} and V_{PPA}, 1µF bypass capacitor between V_{GPB} and V_{PPB}, $V_{\overline{LDO\_EN}}$ = 0V, no load, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Total Power Dissipation per Channel (Quiescent Mode)	P_{PDIS1}	T/R switch off, damp off (transparent mode)			5.7		mW
	P_{PDIS2}	DINN_ = DINP_ = V_{DD} (transparent mode)	MAX14808		17		
			MAX14809		7		
V_{DD} Supply Current	I_{DD1}	CW Doppler (Note 4), transparent or single-ended clock mode			2.2	3.2	mA
	I_{DD2}	B mode (Note 5), transparent or single-ended clock mode (Figure 1a) (MAX14808)			3.3	6	µA
		B mode (Note 5), transparent or single-ended clock mode (Figure 1a) (MAX14809)			10	20	
V_{EE} Supply Current	I_{EE1}	8 channels switching, CW Doppler (Note 4)	CC0 = high, CC1 = high		67	92	mA
	I_{EE2}	8 channels switching, B mode (Note 5) (Figure 1a), CC0 = low, CC1 = low	MAX14808		9.7	14.8	
			MAX14809		2	3	
V_{CC} Supply Current	I_{CC1}	8 channels switching, CW Doppler (Note 4)	CC0 = high, CC1 = high		45	60	mA
	I_{CC2}	8 channels switching, B mode (Note 5) (Figure 1a), CC0 = low, CC1 = low	MAX14808		10	15	
			MAX14809		2.1	3.2	
V_{DD} Supply Current Increase in Clocked Mode	ΔI_{DD}	Differential clock mode			1.8		mA
V_{CC} Supply Current Increase in Clocked Mode	ΔI_{CC}	Differential clock mode			3.8		mA
$V_{NN\_}$ Supply Current	I_{NN1}	8 channels switching, CW Doppler, CC0 = high, CC1 = high, R_L = 1kΩ, C_L = 240pF (Note 4)			157	200	mA
	I_{NN2}	8 channels switching, B mode (Figure 1a), CC0 = low, CC1 = low, R_L = 1kΩ, C_L = 240pF (Note 5)			2	2.8	

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3V, V_{CC} = +5V, V_{EE} = -5V, V_{PPA} = +100V, V_{NNA} = -100V, V_{PPB} = +100V, V_{NNB} = -100V, 1µF bypass capacitor between V_{GNA} and V_{NNA}, 1µF bypass capacitor between V_{GNB} and V_{NNB}, 1µF bypass capacitor between V_{GPA} and V_{PPA}, 1µF bypass capacitor between V_{GPB} and V_{PPB}, $V_{\overline{LDO\_EN}}$ = 0V, no load, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{PP\_}$ Supply Current	I_{PP1}	8 channels switching, CW Doppler, CC0 = high, CC1 = high, R_L = 1kΩ, C_L = 240pF (Note 4)			186	230	mA
	I_{PP2}	8 channels switching, B mode (Figure 1a), CC0 = low, CC1 = low, R_L = 1kΩ, C_L = 240pF (Note 5)			3.1	4.5	
Power Dissipation per Channel (Octal Three-Level Mode)	PD_{CW}	1 channel switching, CW Doppler (Note 4)			286		mW
	PD_{PW}	1 channel switching, B mode (Note 5) (Figure 1a), CC0 = low, CC1 = low, R_L = 1kΩ, C_L = 240pF	MAX14808		73		
			MAX14809		69.5		
SUPPLY CURRENT—QUAD FIVE-LEVEL DUAL MODE, NO LOAD (MODE0 = Low, MODE1 = High)							
V_{DD} Supply Current (Quiescent Mode)	I_{DDQ}	All inputs connected to GND or V_{DD}	Transparent or single-ended clock mode		1.7	3	µA
			Differential clock mode, V_{CLKD} = 0.2V		110	190	
V_{EE} Supply Current (Quiescent Mode)	I_{EEQ}	DINN_ = DINP_ = GND			0.26	0.4	mA
		DINN_ = DINP_ = V_{DD}	MAX14808		5.4	7.7	
			MAX14809		1.35	2	
V_{CC} Supply Current (Quiescent Mode)	I_{CCQ}	DINN_ = DINP_ = GND			0.49	0.75	mA
		DINN_ = DINP_ = V_{DD}	MAX14808		5.6	7.8	
			MAX14809		1.6	2.3	
V_{CC} Supply Current Increase	ΔI_{CC}	Differential clock mode			3.5	5	mA
$V_{NN\_}$ Supply Current (Quiescent Mode)	$I_{NNQ\_}$	All inputs connected to GND or V_{DD}			195	305	µA
$V_{PP\_}$ Supply Current (Quiescent Mode)	$I_{PPQ\_}$	All inputs connected to GND or V_{DD}			220	340	µA
Power Dissipation per Channel (Quiescent Mode)	P_{PDIS1}	T/R switch off, DAMP off (transparent mode)			11.3		mW
	P_{PDIS2}	DINN_ = DINP_ = V_{DD} (transparent mode)	MAX14808		24.1		
			MAX14809		14.1		

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3V, V_{CC} = +5V, V_{EE} = -5V, V_{PPA} = +100V, V_{NNA} = -100V, V_{PPB} = +100V, V_{NNB} = -100V, 1µF bypass capacitor between V_{GNA} and V_{NNA}, 1µF bypass capacitor between V_{GNB} and V_{NNB}, 1µF bypass capacitor between V_{GPA} and V_{PPA}, 1µF bypass capacitor between V_{GPB} and V_{PPB}, $V_{\overline{LDO\_EN}}$ = 0V, no load, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} Supply Current	I_{DD1}	4 channels switching, CW Doppler (Note 4)			1.4		mA
	I_{DD2}	4 channels switching, B mode (Note 5) (Figure 1a)			4.3		µA
V_{EE} Supply Current	I_{EE1}	4 channels switching, CW Doppler (Note 4)	CC0 = high, CC1 = high		33		mA
	I_{EE2}	4 channels switching, B mode (Note 5) (Figure 1a), CC0 = low, CC1 = low	MAX14808		5.9		
			MAX14809		1.9		
V_{CC} Supply Current	I_{CC1}	4 channels switching, CW Doppler (Note 4)	CC0 = high, CC1 = high		22		mA
	I_{CC2}	4 channels switching, B mode (Note 5) (Figure 1a), CC0 = low, CC1 = low	MAX14808		6		
			MAX14809		2		
V_{DD} Supply Current Increase	ΔI_{DD}	Differential clock mode			1.8		mA
V_{CC} Supply Current Increase	ΔI_{CC}	Differential clock mode			3.8		mA
$V_{NN\_}$ Supply Current	I_{NN1}	4 channels switching, CW Doppler (Note 4)	CC0 = high, CC1 = high, R_L = 1kΩ, C_L = 240pF		90		mA
	I_{NN2}	4 channels switching, B mode (Note 5) (Figure 1a), CC0 = low, CC1 = low			1.3		
$V_{PP\_}$ Supply Current	I_{PP1}	4 channels switching, CW Doppler (Note 4)	CC0 = high, CC1 = high, R_L = 1kΩ, C_L = 240pF		103		mA
	I_{PP2}	4 channels switching, B mode (Note 5) (Figure 1a), CC0 = low, CC1 = low			2.2		

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3V, V_{CC} = +5V, V_{EE} = -5V, V_{PPA} = +100V, V_{NNA} = -100V, V_{PPB} = +100V, V_{NNB} = -100V, 1µF bypass capacitor between V_{GNA} and V_{NNA}, 1µF bypass capacitor between V_{GNB} and V_{NNB}, 1µF bypass capacitor between V_{GPA} and V_{PPA}, 1µF bypass capacitor between V_{GPB} and V_{PPB}, $V_{\overline{LDO\_EN}}$ = 0V, no load, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Total Power Dissipation per Channel (Quad Five-Level Dual Mode)	PD_{CW}	1 channel switching, CW Doppler (Note 4), R_L = 1kΩ, C_L = 240pF			311		mW
	PD_{PW}	1 channel switching, B mode (Note 5) (Figure 1a), CC0 = low, CC1 = low, R_L = 1kΩ, C_L = 240pF	MAX14808		102		
			MAX14809		94.5		
SUPPLY CURRENT—OCTAL THREE-LEVEL, NO LOAD (MODE0 = High, MODE1 = Low, $\overline{LDO\_EN}$ = High, $V_{PP\_}$ - $V_{GP\_}$ = +5V, $V_{GN\_}$ - $V_{NN\_}$ = +5V)							
V_{EE} Supply Current (Quiescent Mode)	$I_{EEQ\_}$	All inputs connected to GND			25	46	µA
V_{CC} Supply Current (Quiescent Mode)	$I_{CCQ\_}$	All inputs connected to GND			280	420	µA
$V_{NN\_}$ Supply Current (Quiescent Mode)	$I_{NNQ\_}$	All inputs connected to GND			40	62	µA
$V_{PP\_}$ Supply Current (Quiescent Mode)	$I_{PPQ\_}$	All inputs connected to GND			40	62	µA
OUTPUT STAGE							
V_{NNA}, V_{NNB} Connected Low-Side Output Impedance	R_{OLS}	$I_{OUT\_}$ = -50mA	CC0 = low, CC1 = low		8.5		Ω
			CC0 = high, CC1 = low		10		
			CC0 = low, CC1 = high		13.5		
			CC0 = high, CC1 = high		26	48	
V_{PPA}, V_{PPB} Connected High-Side Output Impedance	R_{OHS}	$I_{OUT\_}$ = +50mA	CC0 = low, CC1 = low		9		Ω
			CC0 = high, CC1 = low		10.5		
			CC0 = low, CC1 = high		14.5		
			CC0 = high, CC1 = high		27	53	
Clamp nFET Output Impedance	R_{ONG}	$I_{OUT\_}$ = -50mA,			13.5		Ω
Clamp pFET Output Impedance	R_{OPG}	$I_{OUT\_}$ = +50mA			13.5		Ω
Active Damp Output Impedance	R_{DAMP}	Before grass-clipping diode			500		Ω

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3V, V_{CC} = +5V, V_{EE} = -5V, V_{PPA} = +100V, V_{NNA} = -100V, V_{PPB} = +100V, V_{NNB} = -100V, 1µF bypass capacitor between V_{GNA} and V_{NNA}, 1µF bypass capacitor between V_{GNB} and V_{NNB}, 1µF bypass capacitor between V_{GPA} and V_{PPA}, 1µF bypass capacitor between V_{GPB} and V_{PPB}, $V_{\overline{LDO\_EN}}$ = 0V, no load, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{NNA}, V_{NNB} Connected Low-Side Output Current	I_{OLS}	V_{DS} = +100V	CC0 = low, CC1 = low		2.0		A
			CC0 = high, CC1 = low		1.5		
			CC0 = low, CC1 = high		1.0		
			CC0 = high, CC1 = high		0.5		
V_{PPA}, V_{PPB} Connected High-Side Output Current	I_{OHS}	V_{DS} = +100V	CC0 = low, CC1 = low		2.0		A
			CC0 = high, CC1 = low		1.5		
			CC0 = low, CC1 = high		1.0		
			CC0 = high, CC1 = high		0.5		
GND-Connected nFET Output Current	I_{ONG}	V_{DS} = +100V			1		A
GND-Connected pFET Output Current	I_{OPG}	V_{DS} = +100V			1		A
Diode Voltage Drop (Blocking Diode and Grass-Clipping Diode)	V_{DROP}	$I_{OUT\_}$ = ±50mA			1.7		V
LVOUT_Diode Clamping Voltage	LV_{CLAMP}	I_{LOAD} = 1mA (MAX14808 only)		-0.9		+1	V
Grass-Clipping Diode Reverse Capacitance	C_{REV}				2.5		pF
OUT_ Equivalent Large-Signal Shunt Capacitance	C_{HS}	200V_{P-P} signal			80		pF
T/R Switch On Impedance	R_{ON}	MAX14808 only			11.5		Ω
T/R Switch Off Impedance	R_{OFF}	MAX14808 only		1			MΩ
LVOUT_ Output Offset	LV_{OFF}	LVOUT_, OUT_ unconnected, V_{CC} = +5V, V_{EE} = -5V		-40	0	+40	mV
THERMAL SHUTDOWN							
Thermal-Shutdown Threshold	t_{SDN}	Temperature rising			+145		°C
Thermal-Shutdown Hysteresis	t_{HYS}				20		°C

AC ELECTRICAL CHARACTERISTICS

(V_{DD} = +3V, V_{CC} = +5V, V_{EE} = -5V, V_{PPA} = +100V, V_{NNA} = -100V, V_{PPB} = +100V, V_{NNB} = -100V, V_{GNA} connected to V_{NNA} with 1µF capacitor, V_{GNB} connected to V_{NNB} with 1µF capacitor, V_{GPA} connected to V_{PPA} with 1µF capacitor, V_{GPB} connected to V_{PPB} with 1µF capacitor, $V_{\overline{LDO\_EN}}$ = 0V, V_{CC0} = 0V, V_{CC1} = 0V, R_L = 1kΩ, C_L = 240pF, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Logic Input to Output Rise Propagation Delay	t_{PLH}	From 50% DINP_/DINN_ (transparent mode) to 10% OUT_ transition swing (Figure 2a)			18		ns
Logic Input to Output Fall Propagation Delay	t_{PHL}	From 50% DINP_/DINN_ (transparent mode) to 10% OUT_ transition swing (Figure 2a)			18		ns
Logic Input to Output Rise to GND Propagation Delay	t_{PL0}	From 50% DINP_/DINN_ (transparent mode) to 10% OUT_ transition swing (Figure 2a)			18		ns
Logic Input to Output Fall to GND Propagation Delay	t_{PH0}	From 50% DINP_/DINN_ (transparent mode) to 10% OUT_ transition swing (Figure 2a)			18		ns
OUT_ Fall Time (V_{PPA} to V_{NNA}, V_{PPB} to V_{NNB})	t_{FPN}	Figure 2b			30	48	ns
OUT_ Rise Time (V_{NNA} to V_{PPA}, V_{NNB} to V_{PPB})	t_{RNP}	Figure 2b			30	48	ns
OUT_ Rise Time (GND to V_{PPA}, GND to V_{PPB})	t_{R0P}	Figure 2b			15	22.5	ns
OUT_ Fall Time (GND to V_{NNA}, GND to V_{NNB})	t_{F0N}	Figure 2b			15	22.5	ns
OUT_ Rise Time (V_{NNA} to GND, V_{NNB} to GND)	t_{RN0}	20% to 80% transition (Figure 2b)	Three-level mode		21		ns
			Five-level dual mode		13		
OUT_ Fall Time (V_{PPA} to GND, V_{PPB} to GND)	t_{FP0}	20% to 80% transition (Figure 2b)	Three-level mode		21		ns
			Five-level dual mode		13		
T/R Switch Turn-On Time	t_{ONTRSW}	(MAX14808 only) Figure 3			0.65	1.2	µs
T/R Switch Turn-Off Time	$t_{OFFTRSW}$	(MAX14808 only) Figure 3 (Note 6)			0.02	0.1	µs
Output Enable Time (Shutdown Mode to Normal Operation)	t_{EN1}					100	µs
Output Disable Time (Normal Operation to Shutdown Mode)	t_{DIS1}					10	µs

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3V, V_{CC} = +5V, V_{EE} = -5V, V_{PPA} = +100V, V_{NNA} = -100V, V_{PPB} = +100V, V_{NNB} = -100V, V_{GNA} connected to V_{NNA} with 1µF capacitor, V_{GNB} connected to V_{NNB} with 1µF capacitor, V_{GPA} connected to V_{PPA} with 1µF capacitor, V_{GPB} connected to V_{PPB} with 1µF capacitor, $V_{\overline{LDO\_EN}}$ = 0V, V_{CC0} = 0V, V_{CC1} = 0V, R_L = 1kΩ, C_L = 240pF, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Enable Time (Transmit Disable Mode to Normal Operation)	t_{EN2}				50	ns
Output Disable Time (Normal Operation to Transmit Disable Mode)	t_{DIS2}				65	ns
Output Enable Time (Normal Operation to Sync Mode)	t_{EN3}				4	µs
Output Disable Time (Sync Mode to Normal Operation)	t_{DIS3}				500	ns
CLK Frequency	f_{CLK}	V_{DD} = 2.5V			200	MHz
Input Setup Time (DINN_, DINP_)	t_{SETUP}	V_{DD} = 2.5V	2			NS
Input Hold Time (DINN_, DINP_)	t_{HOLD}	V_{DD} = 2.5V	0.5			ns
Second-Harmonic Distortion (Low Voltage)	THD2LV	$f_{OUT\_}$ = 5MHz, V_{PPA} = -V_{NNA} = +5V, V_{PPB} = -V_{NNB} = +5V, square wave (all modes)		-40		dBc
Second-Harmonic Distortion (High Voltage)	THD2HV	$f_{OUT\_}$ = 5MHz, V_{PPA} = -V_{NNA} = +100V, V_{PPB} = -V_{NNB} = +100V, square wave (all modes)		-43		dBc
Pulse Cancellation	PC1	$f_{OUT\_}$ = 5MHz, V_{PPA} = -V_{NNA} = +100V, V_{PPB} = -V_{NNB} = +100V, 2 periods, all harmonics of the summed signed with respect to the carrier		-40		dBc
	PC2	$f_{OUT\_}$ = 5MHz, V_{PPA} = -V_{NNA} = +100V, V_{PPB} = -V_{NNB} = +100V, 2 periods, $[(V_0 + V_{180})_{RMS}/(2 \times V_{0RMS})]_{dB}$		-40		
Pulser Bandwidth	BW	V_{PP} = +60V, V_{NNA} = -60V (Figure 4)		20		MHz
RMS Output Jitter	t_J	$f_{OUT\_}$ = 5MHz, V_{PPA} = -V_{NNA} = +5V, V_{PPB} = -V_{NNB} = +5V, both in clocked mode or transparent mode (Figure 5)		6.25		ps

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3V, V_{CC} = +5V, V_{EE} = -5V, V_{PPA} = +100V, V_{NNA} = -100V, V_{PPB} = +100V, V_{NNB} = -100V, V_{GNA} connected to V_{NNA} with 1µF capacitor, V_{GNB} connected to V_{NNB} with 1µF capacitor, V_{GPA} connected to V_{PPA} with 1µF capacitor, V_{GPB} connected to V_{PPB} with 1µF capacitor, $V_{\overline{LDO\_EN}}$ = 0V, V_{CC0} = 0V, V_{CC1} = 0V, R_L = 1kΩ, C_L = 240pF, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
T/R Switch Harmonic Distortion (MAX14808)	THD_{TRSW}	R_{LOAD} = 200Ω, V_{SIGNAL} = 100mV_{P-P}		-50		dB
T/R Switch Turn-On/Off Voltage Spike (MAX14808)	V_{SPIKE}	R_{LOAD} = 1kΩ at both sides of T/R switch		50		mV
Crosstalk	CT	f = 5MHz, adjacent channels, $R_{LOUT\_}$ = 200Ω		-51		dB

Note 2: All devices are 100% production tested at T_A = +85°C. Limits over the operating temperature range are guaranteed by design.
Note 3: Maximum operating current from $V_{GN\_}$ and $V_{GP\_}$ external power sources can vary depending on application requirements. The suggested minimum values assume 8 channels running in continuous transmission (CWD) at 5MHz with CC0 = CC1 = high.
Note 4: CW Doppler: continuous wave, f = 5MHz, V_{DD} = +3V, V_{CC} = -V_{EE} = +5V, $V_{PP\_}$ = -$V_{NN\_}$ = +5V.
Note 5: B mode: f = 5MHz, PRF = 5kHz, 1 period, V_{DD} = +3V, V_{CC} = -V_{EE} = +5V, $V_{PP\_}$ = -$V_{NN\_}$ = +100V.
Note 6: T/R switch turn-off time is the time required to switch off the bias current of the T/R switch. The off-isolation is not guaranteed.

Timing Diagrams

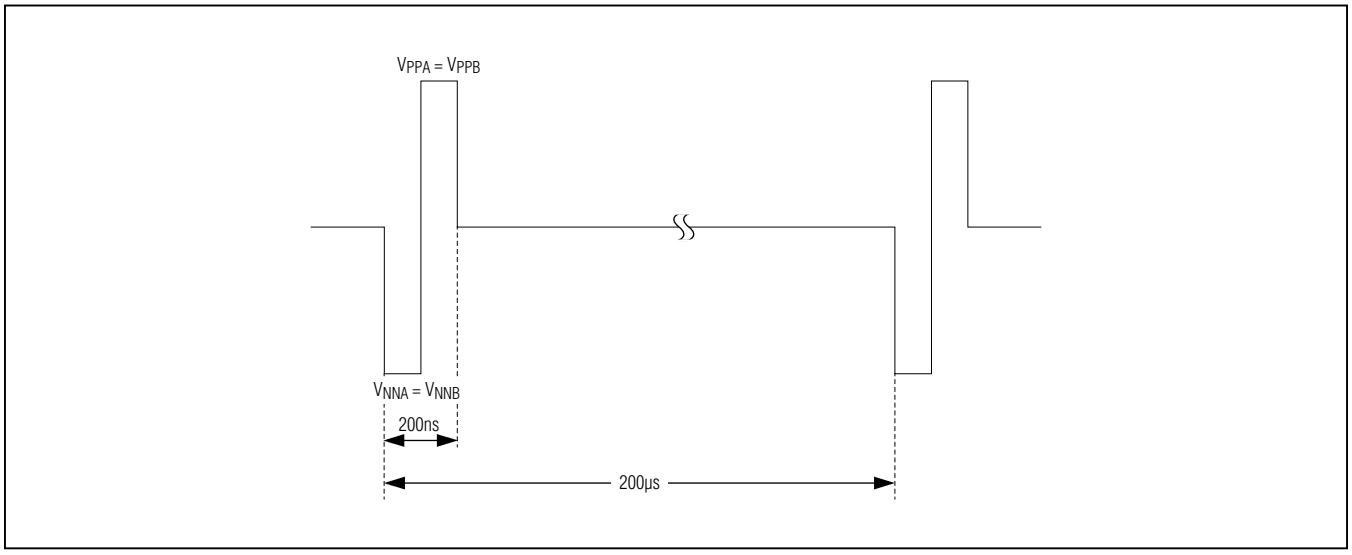


Figure 1a. High-Voltage Burst Test (Three Levels)

Timing Diagrams (continued)

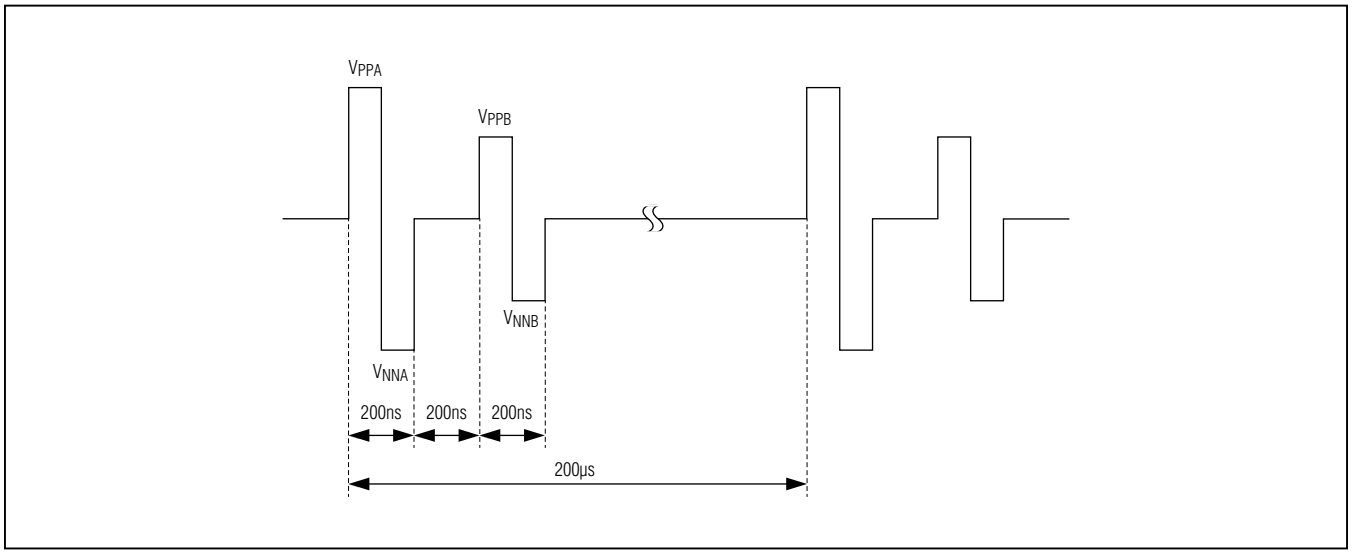


Figure 1b. High-Voltage Burst Test (Five Levels)

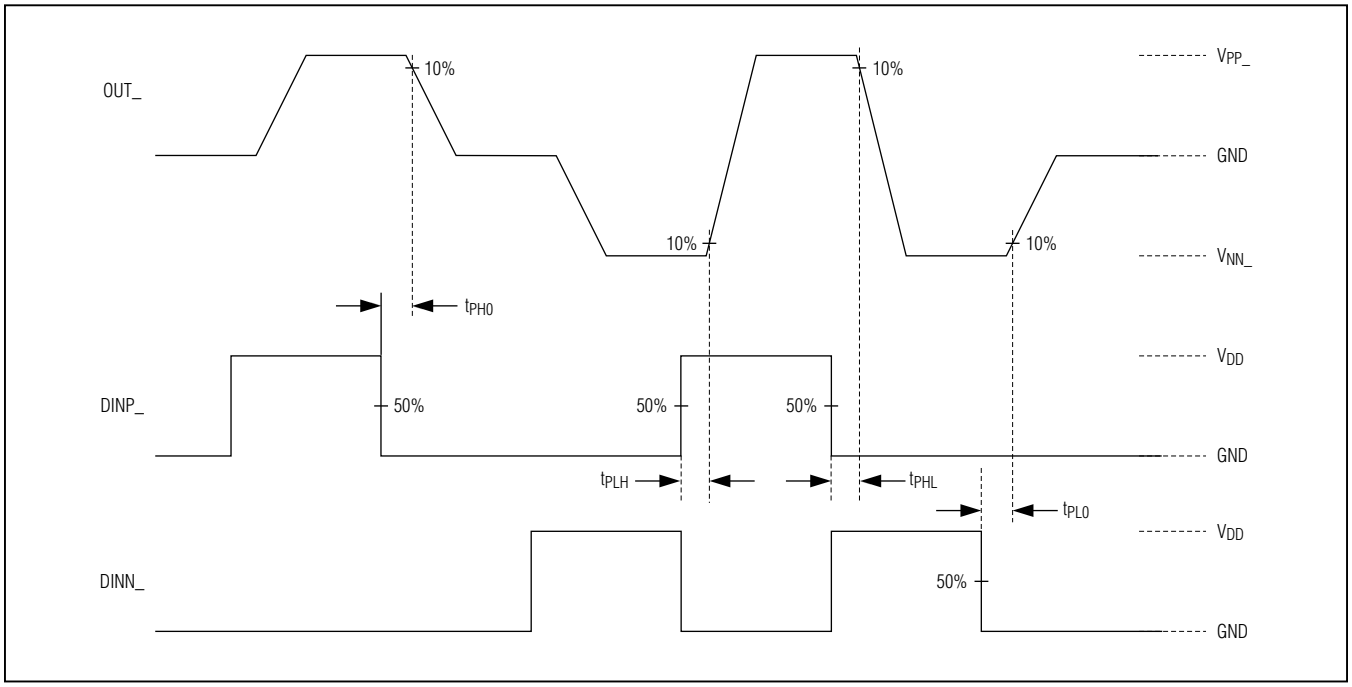


Figure 2a. Propagation Delay Timing

Timing Diagrams (continued)

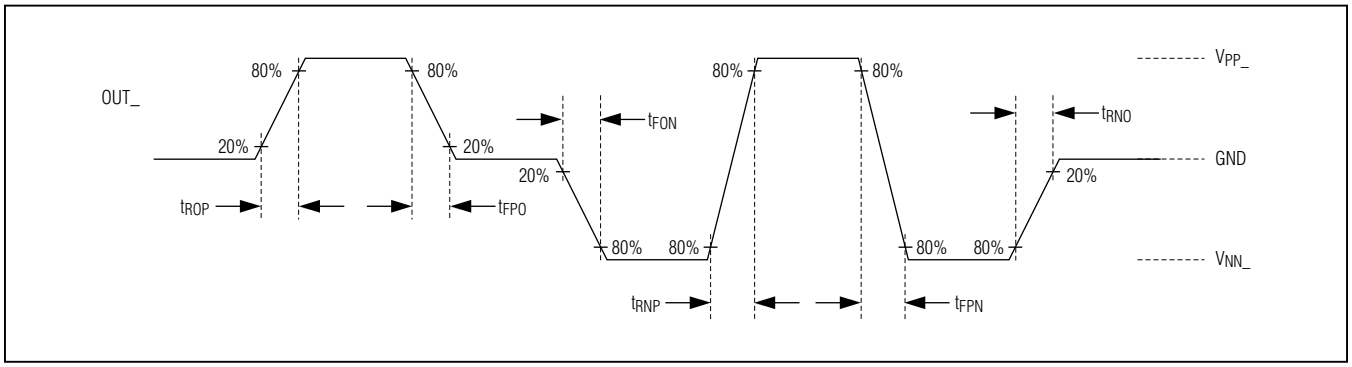


Figure 2b. Output Rise/Fall Timing

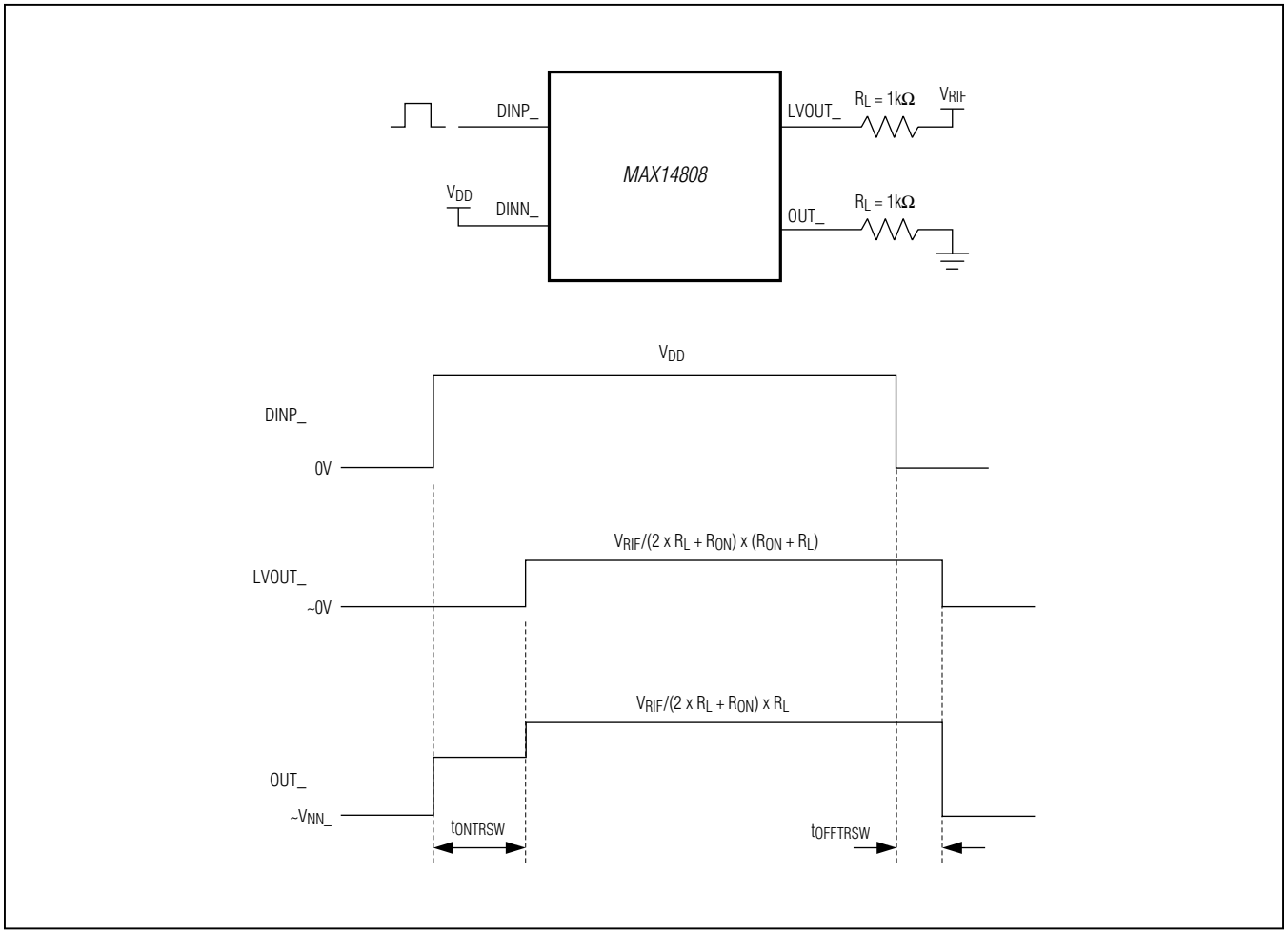


Figure 3. T/R Switch Turn-On/Off Time

Timing Diagrams (continued)

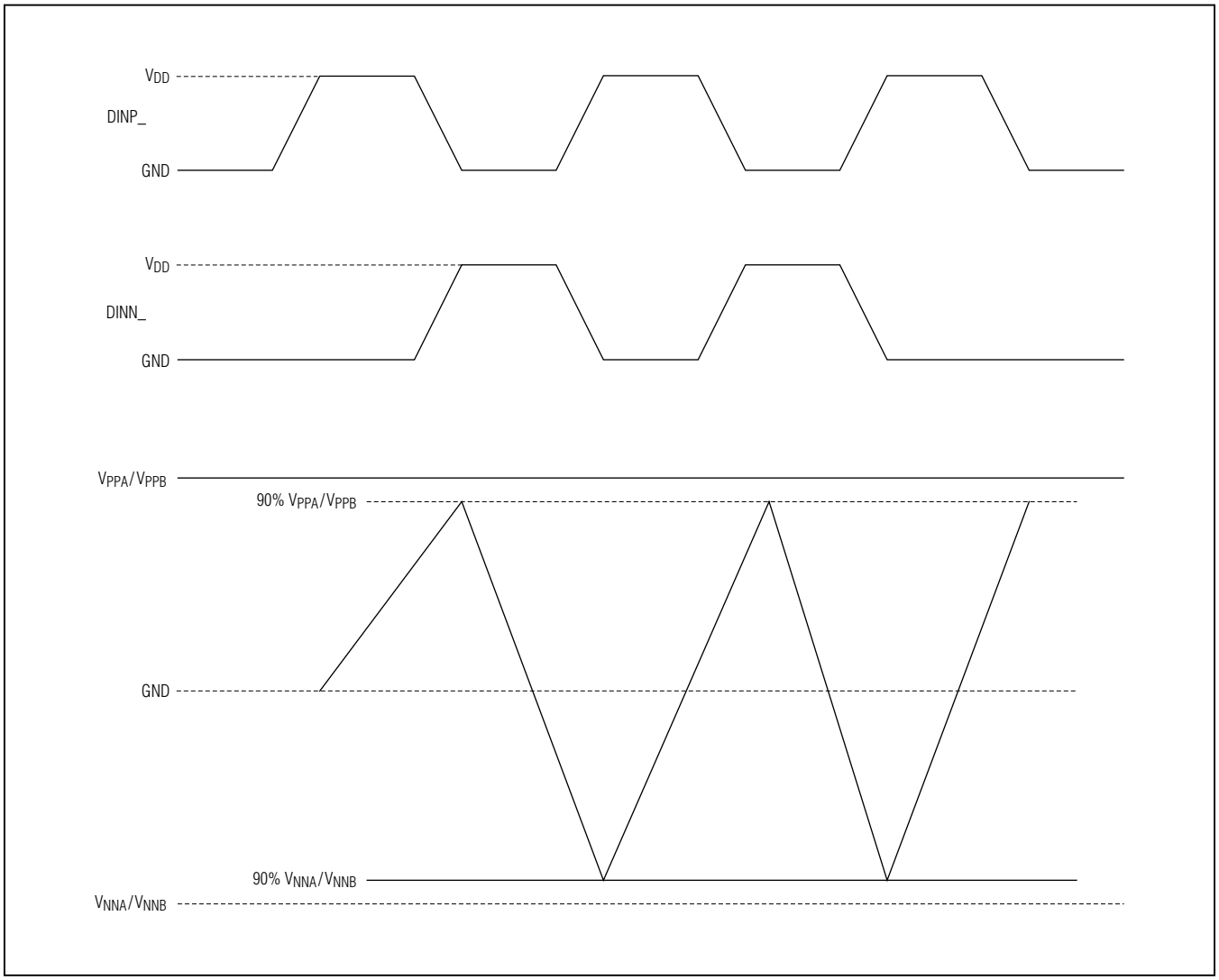


Figure 4. Bandwidth

Timing Diagrams (continued)

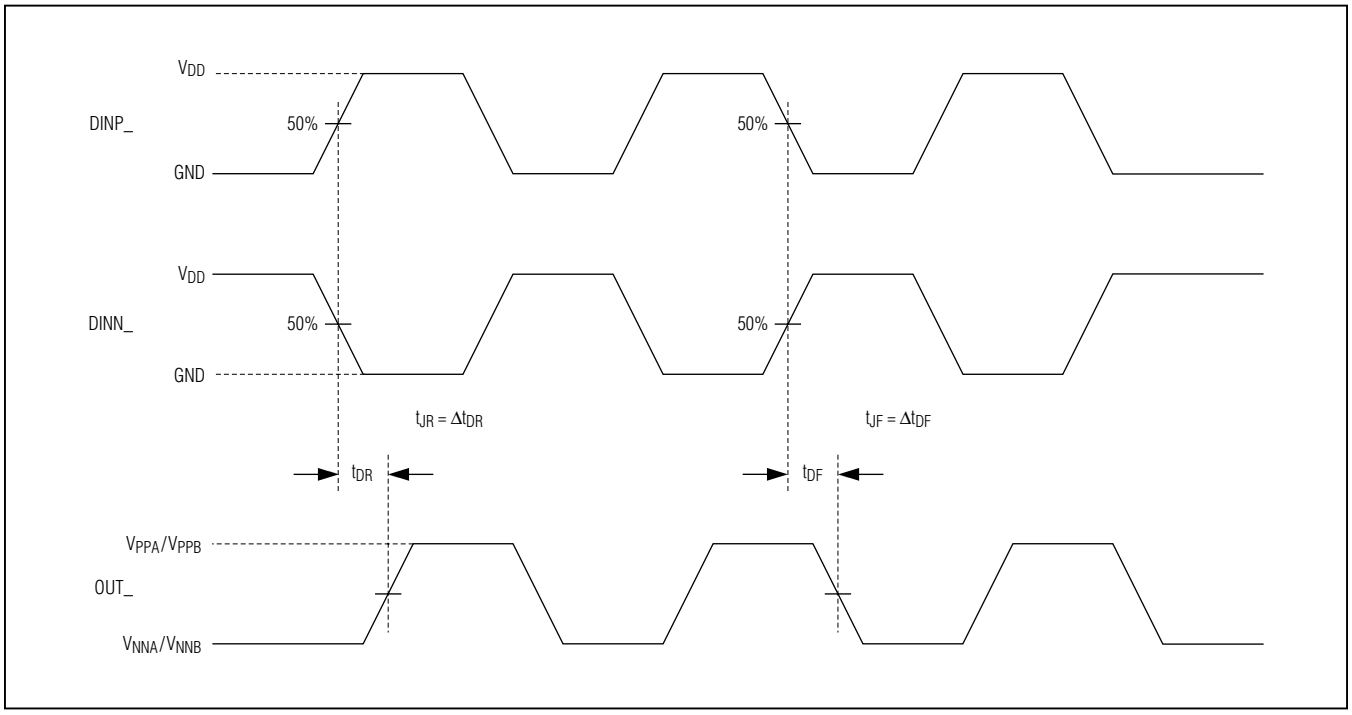
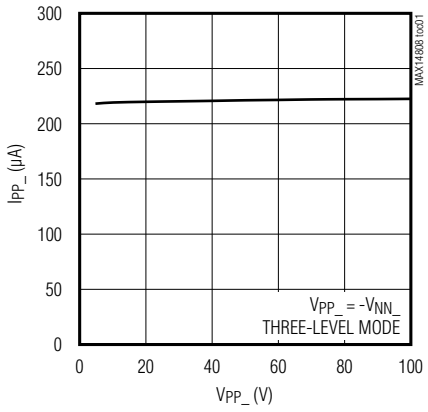


Figure 5. Jitter Timing

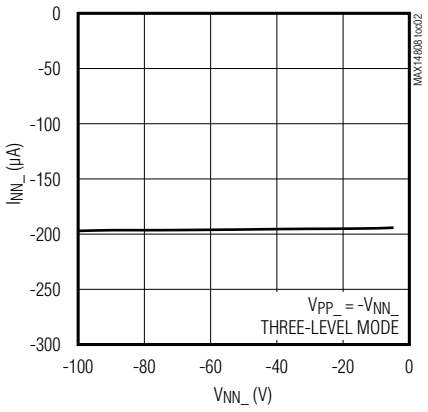
Typical Operating Characteristics

(V_{DD} = +5V, V_{CC} = +5V, V_{EE} = -5V, $V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, R_L = 1kΩ, C_L = 240pF, unless otherwise noted. Typical values are at T_A = +25°C.)

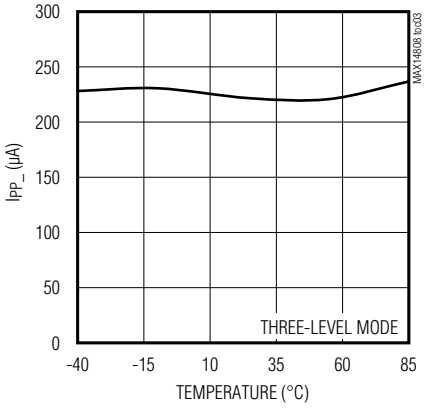
IPP_ QUIESCENT CURRENT vs. VPP_



INN_ QUIESCENT CURRENT vs. VNN_



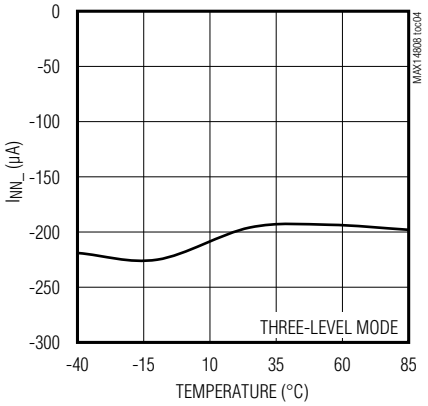
IPP_ QUIESCENT CURRENT vs. TEMPERATURE



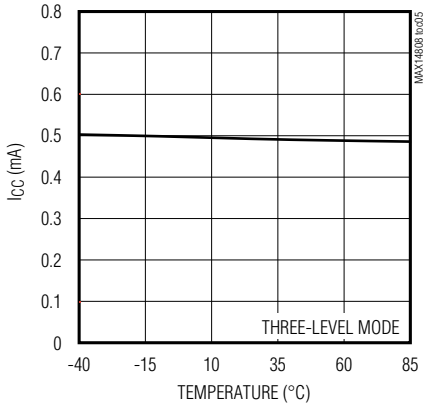
Typical Operating Characteristics (continued)

(V_{DD} = +5V, V_{CC} = +5V, V_{EE} = -5V, $V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, R_L = 1kΩ, C_L = 240pF, unless otherwise noted. Typical values are at T_A = +25°C.)

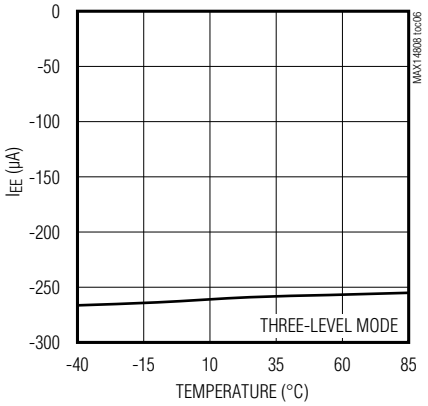
$I_{NN\_}$ QUIESCENT CURRENT vs. TEMPERATURE



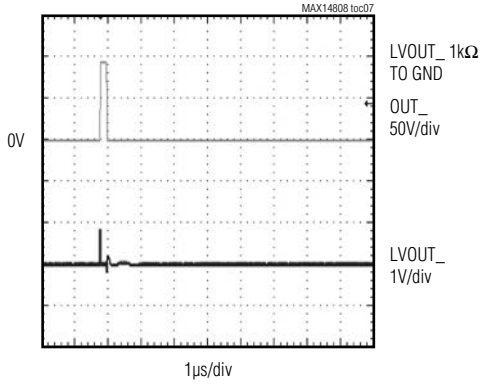
I_{CC} QUIESCENT CURRENT vs. TEMPERATURE



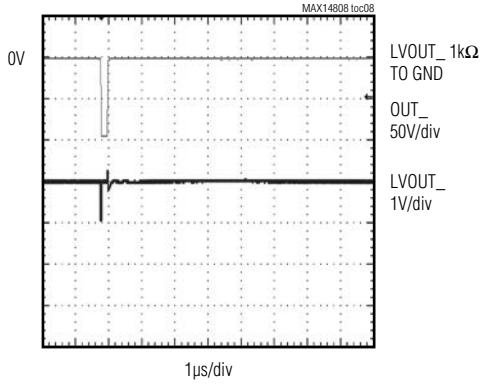
I_{EE} QUIESCENT CURRENT vs. TEMPERATURE



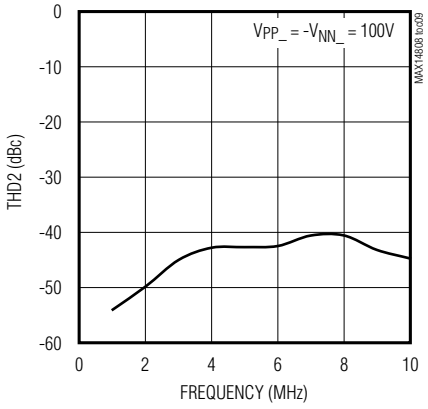
LOW TO HIGH TRANSITION VOLTAGE SPIKE



HIGH TO LOW TRANSITION SPIKE



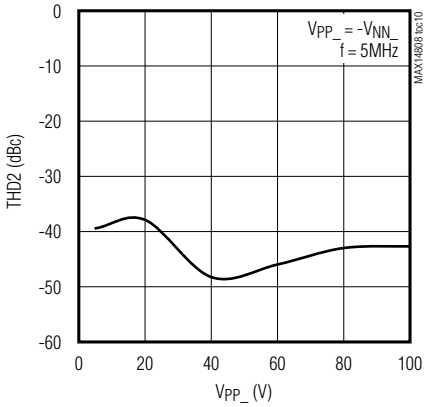
THD2 vs. FREQUENCY



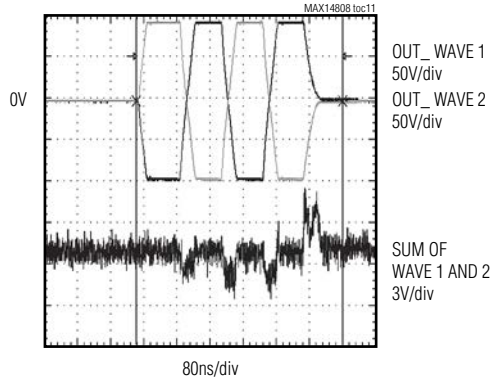
Typical Operating Characteristics (continued)

(V_{DD} = +5V, V_{CC} = +5V, V_{EE} = -5V, $V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, R_L = 1kΩ, C_L = 240pF, unless otherwise noted. Typical values are at T_A = +25°C.)

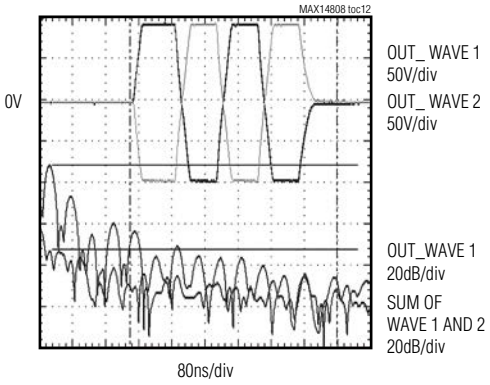
THD2 vs. $V_{PP\_}$



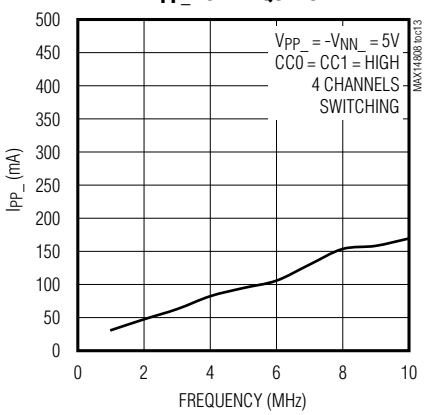
PULSE CANCELLATION



PULSE CANCELLATION FFT



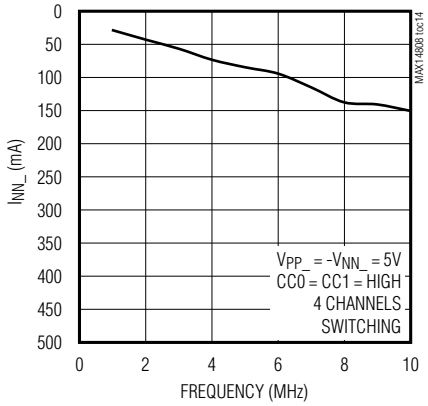
$I_{PP\_}$ vs. FREQUENCY



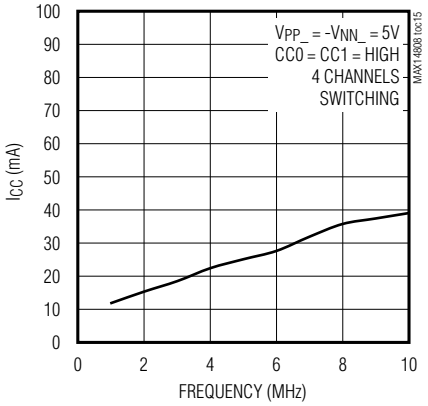
Typical Operating Characteristics (continued)

(V_{DD} = +5V, V_{CC} = +5V, V_{EE} = -5V, $V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, R_L = 1kΩ, C_L = 240pF, unless otherwise noted. Typical values are at T_A = +25°C.)

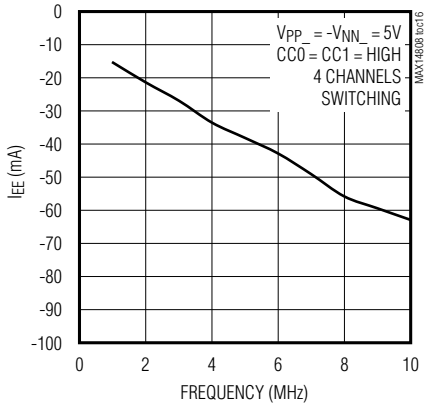
$I_{NN\_}$ vs. FREQUENCY



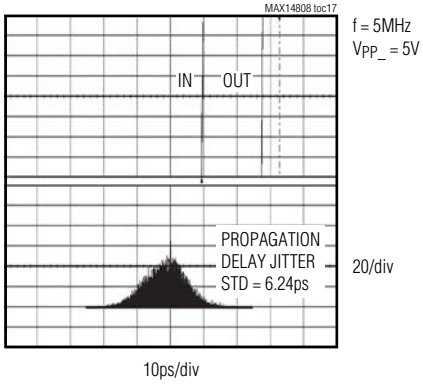
I_{CC} vs. FREQUENCY



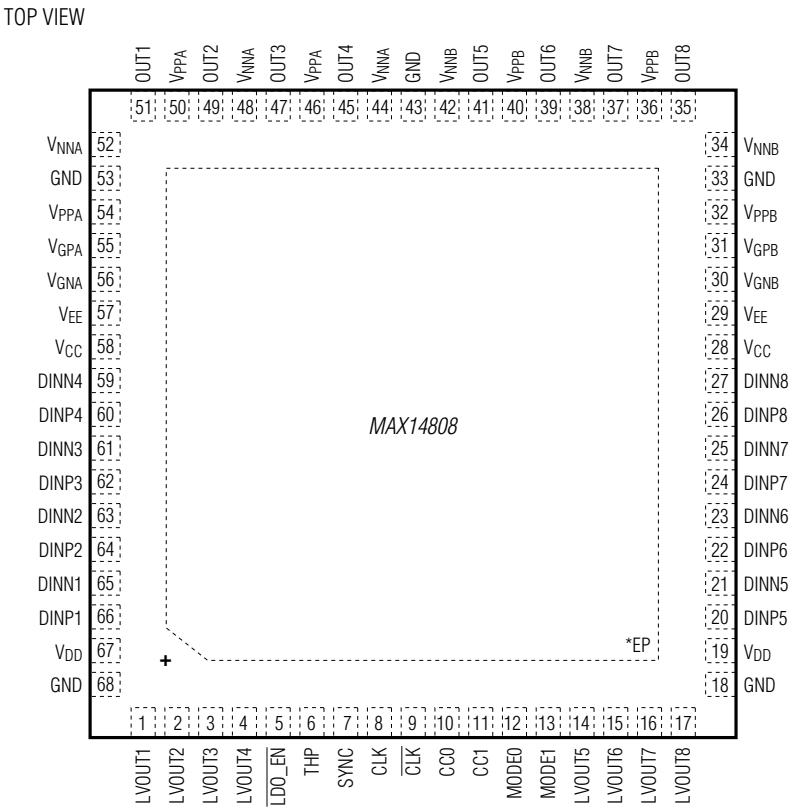
I_{EE} vs. FREQUENCY



OUTPUT JITTER



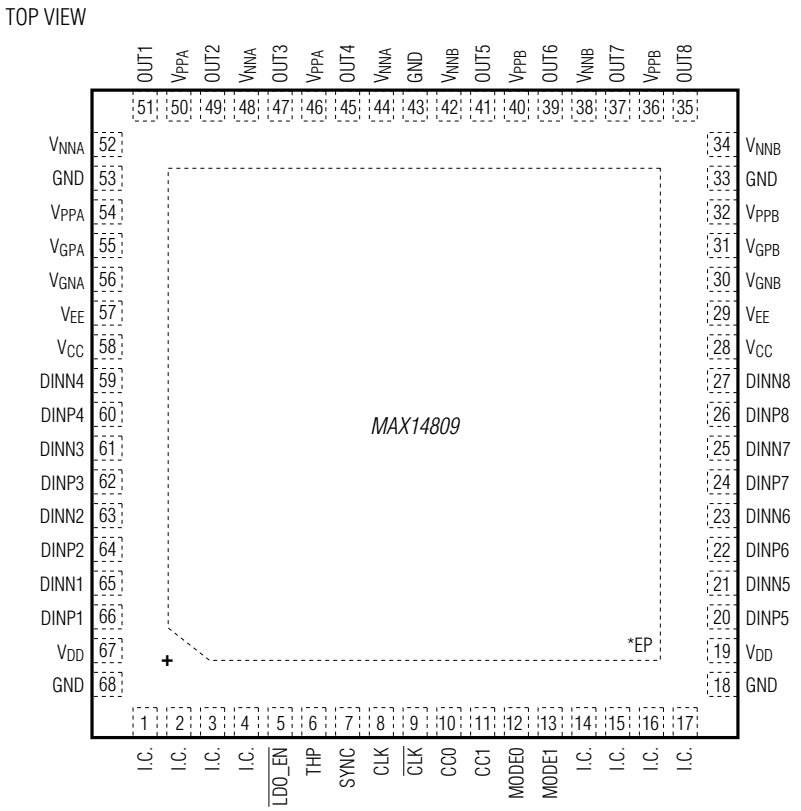
Pin Configurations



TQFN
(10mm x 10mm x 0.75mm)

*CONNECT EP TO GND

Pin Configurations (continued)



TQFN
(10mm x 10mm x 0.75mm)

*CONNECT EP TO GND

Pin Description

PIN		NAME	FUNCTION
MAX14808	MAX14809		
1	—	LVOUT1	Low-Voltage T/R Switch Output 1
2	—	LVOUT2	Low-Voltage T/R Switch Output 2
3	—	LVOUT3	Low-Voltage T/R Switch Output 3
4	—	LVOUT4	Low-Voltage T/R Switch Output 4
—	1–4, 14–17	I.C.	Internally Connected. Connect I.C. to GND externally.
5	5	$\overline{\text{LDO\_EN}}$	Internal Supply Generator Control Input. Drive $\overline{\text{LDO\_EN}}$ high to disable the internal power supply when using an external power supply on V_{GPA}, V_{GPB}, V_{GNA}, and V_{GNB}. $\overline{\text{LDO\_EN}}$ has an internal 10kΩ pulldown resistor to GND.
6	6	THP	Open-Drain Thermal-Protection Output. THP asserts and sinks a 3mA current to GND when the junction temperature exceeds +150°C.
7	7	SYNC	CMOS Control Input. Drive SYNC high to enable clocked-input mode. Drive SYNC low to operate in transparent mode (see the *Truth Tables* section).
8	8	CLK	CMOS Control Input. Clock positive phase input. Data inputs are clocked in at the rising edge of CLK and $\overline{\text{CLK}}$ in differential clocked mode or at the rising edge of CLK in single-ended clocked mode. Clock maximum frequency is 160MHz.
9	9	$\overline{\text{CLK}}$	CMOS Control Input. Clock negative phase input. Data inputs are clocked in at the edge of CLK and $\overline{\text{CLK}}$ in differential clocked mode. Clock maximum frequency is 160MHz. If $\overline{\text{CLK}}$ is connected to GND, the CLK input is a single-ended logic-level clock input. Otherwise, CLK and $\overline{\text{CLK}}$ are self-biased differential clock inputs.
10	10	CC0	Current Control Input. Control current capability (see the *Truth Tables* section).
11	11	CC1	Current Control Input. Control current capability (see the *Truth Tables* section).
12	12	MODE0	Mode Control Input. Control operation mode (see the *Truth Tables* section).
13	13	MODE1	Mode Control Input. Control operation mode (see the *Truth Tables* section).
14	—	LVOUT5	Low-Voltage T/R Switch Output 5
15	—	LVOUT6	Low-Voltage T/R Switch Output 6
16	—	LVOUT7	Low-Voltage T/R Switch Output 7
17	—	LVOUT8	Low-Voltage T/R Switch Output 8
18, 33, 43, 53, 68	18, 33, 43, 53, 68	GND	Ground
19, 67	19, 67	V_{DD}	Logic Supply Voltage. Bypass V_{DD} (both pins) to GND with a 0.1µF capacitor as close as possible to the device.
20	20	DINP5	Digital Signal Positive Input 5 (see the *Truth Tables* section)
21	21	DINN5	Digital Signal Negative Input 5 (see the *Truth Tables* section)
22	22	DINP6	Digital Signal Positive Input 6 (see the *Truth Tables* section)
23	23	DINN6	Digital Signal Negative Input 6 (see the *Truth Tables* section)
24	24	DINP7	Digital Signal Positive Input 7 (see the *Truth Tables* section)
25	25	DINN7	Digital Signal Negative Input 7 (see the *Truth Tables* section)
26	26	DINP8	Digital Signal Positive Input 8 (see the *Truth Tables* section)
27	27	DINN8	Digital Signal Negative Input 8 (see the *Truth Tables* section)

Pin Description (continued)

PIN		NAME	FUNCTION
MAX14808	MAX14809		
28, 58	28, 58	V_{CC}	V_{CC} Supply Voltage. Bypass V_{CC} (both pins) to GND with a 0.1µF capacitor as close as possible to the device.
29, 57	29, 57	V_{EE}	V_{EE} Supply Voltage. Bypass V_{EE} (both pins) to GND with a 0.1µF capacitor as close as possible to the device.
30	30	V_{GNB}	Driver Voltage Supply Output. Connect a 1µF capacitor to V_{NNB} as close as possible to the device.
31	31	V_{GPB}	Driver Voltage Supply Output. Connect a 1µF capacitor to V_{PPB} as close as possible to the device.
32, 36, 40	32, 36, 40	V_{PPB}	High-Voltage Positive Supply Input. Bypass V_{PPB} to GND with a 0.1µF capacitor as close as possible to the device.
34, 38, 42	34, 38, 42	V_{NNB}	High-Voltage Negative Supply Input. Bypass V_{NNB} to GND with a 0.1µF capacitor as close as possible to the device.
35	35	OUT8	Pulser Output 8
37	37	OUT7	Pulser Output 7
39	39	OUT6	Pulser Output 6
41	41	OUT5	Pulser Output 5
44, 48, 52	44, 48, 52	V_{NNA}	High-Voltage Negative Supply Input. Bypass V_{NNA} to GND with a 0.1µF capacitor as close as possible to the device.
45	45	OUT4	Pulser Output 4
46, 50, 54	46, 50, 54	V_{PPA}	High-Voltage Positive Supply Input. Bypass V_{PPA} to GND with a 0.1µF capacitor as close as possible to the device.
47	47	OUT3	Pulser Output 3
49	49	OUT2	Pulser Output 2
51	51	OUT1	Pulser Output 1
55	55	V_{GPA}	Driver Voltage Supply Output. Connect a 1µF capacitor to V_{PPA} as close as possible to the device.
56	56	V_{GNA}	Driver Voltage Supply Output. Connect a 1µF capacitor to V_{NNA} as close as possible to the device.
59	59	DINN4	Digital Signal Negative Input 4 (see the *Truth Tables* section)
60	60	DINP4	Digital Signal Positive Input 4 (see the *Truth Tables* section)
61	61	DINN3	Digital Signal Negative Input 3 (see the *Truth Tables* section)
62	62	DINP3	Digital Signal Positive Input 3 (see the *Truth Tables* section)
63	63	DINN2	Digital Signal Negative Input 2 (see the *Truth Tables* section)
64	64	DINP2	Digital Signal Positive Input 2 (see the *Truth Tables* section)
65	65	DINN1	Digital Signal Negative Input 1 (see the *Truth Tables* section)
66	66	DINP1	Digital Signal Positive Input 1 (see the *Truth Tables* section)
—	—	EP	Exposed Pad. Connect EP to GND. Not intended as an electrical connection point.

Detailed Description

The MAX14808/MAX14809 octal three-level/quad five-level, high-voltage (HV) pulser devices generate high-frequency, HV bipolar pulses (up to ±105V) from low-voltage control logic inputs for driving piezoelectric transducers in ultrasound systems. All 8 channels have embedded overvoltage-protection diodes and integrated active return-to-zero clamp. Both devices have embedded independent (floating) power supplies (FPSs) and level shifters that allow signal transmission without the need for external HV capacitors. The MAX14808 also features eight integrated transmit receive (T/R) switches. The MAX14809 does not have the T/R switch function.

The devices feature two modes of operation, an octal three-level pulser mode (with integrated active return-to-zero clamp) or a quad five-level pulser mode. In octal three-level pulser mode, each channel is controlled by two logic inputs (DINN_/DINP_) and the active return to zero features half the current driving of the pulser, 1A (typ). In quad five-level pulser mode, each channel is controlled by three logic inputs and the active return to zero has the same current driving of the pulser, 2A (typ).

The devices can operate both in clocked and transparent mode. In clocked mode, data inputs can be synchronized with a clean differential or single-ended clock to reduce phase noise associated with FPGA output signals that are detrimental for Doppler analysis. In transparent mode, the synchronization feature is disabled and output reflects the data input after an 18ns delay. Both devices feature adjustable maximum current (0.5A to 2A) to reduce power consumption when full current capability is not required.

The devices feature integrated grass-clipping diodes (with low parasitic capacitance) for receive (Rx) and transmit (Tx) isolations. Both devices feature a damping circuit that can be activated as soon as the transmit burst is over. The damping circuit has a typical on-resistance of 500Ω. It fully discharges the pulser's output internal node before the grass-clipping diodes.

Operation Mode

The devices have four operation modes: shutdown, octal three-level, quad five-level dual, and transmit disable. Use the MODE0 and MODE1 inputs to select the operation mode.

Shutdown Mode

All channels are disabled, no transmission and reception is possible. This mode has the lowest power consumption. See Table 1.

Octal Three-Level Mode

The devices operate in eight independent channels. Each channel can generate a three-level pulse. The high-side and low-side FET of each channel are capable of providing 2.0A current, while the clamp is capable of 1A current. See Table 2.

Quad Five-Level Dual Mode

The devices operate in four independent channels. Each channel can generate a five-level pulse. The devices feature independent dual-voltage supplies (V_{NNA}, V_{NNB}, V_{PPA}, and V_{PPB}) and can generate pulses among GND, V_{PPA}, and V_{NNA} or among GND, V_{PPB}, and V_{NNB}. The high-side and low-side FET as well as the clamp of each channel can provide 2.0A current. See Table 3.

Transmit Disable Mode

All eight high-voltage transmit channels are disabled, no pulse transmission is possible. The T/R switch (MAX14808 only) can be turn-on (to receive low-voltage signals) or turn-off (for isolation). See Table 4.

Truth Tables

Table 1. Shutdown Mode (MODE0 = Low, MODE1 = Low)

INPUTS		OUTPUTS	
DINN_	DINP_	OUT_	LVOUT_ (MAX14808 ONLY)
X	X	High impedance	High impedance (T/R switch off)

X = Don't care

Truth Tables (continued)

Table 2. Octal Three-Level Mode (MODE0 = High, MODE1 = Low, $V_{NNA} = V_{NNB}$, $V_{PPA} = V_{PPB}$)

INPUTS		OUTPUTS	
DINN_	**DINP_**	**OUT_**	**LVOUT_ (MAX14808 ONLY)**
0	0	Clamp on (damp off)	T/R switch off (LVOUT_ = GND)
1	0	V_{NNA}/V_{NNB} (damp off)	T/R switch off (LVOUT_ = GND)
0	1	V_{PPA}/V_{PPB} (damp off)	T/R switch off (LVOUT_ = GND)
1	1	Clamp on (damp on)	T/R switch on

0 = logic-low, 1 = logic-high

Table 3. Quad Five-Level Dual Mode (MODE0 = Low, MODE1 = High)

INPUTS				OUTPUTS		
DINNx x = 1, 2, 3, 4	**DINPx x = 1, 2, 3, 4**	**DINNy y = 5, 6, 7, 8**	**DINPy y = 5, 6, 7, 8**	**OUTx = OUTy**	**LVOUTy y = 1, 2, 3, 4 (MAX14808 ONLY)**	**LVOUTy y = 5, 6, 7, 8 (MAX14808 ONLY)**
0	0	X	0	High impedance (damp off)	T/R switch off (LVOUT_ = GND)	T/R switch off (LVOUT_ = GND)
0	0	X	1	Clamp on (damp off)	T/R switch off (LVOUT_ = GND)	T/R switch off (LVOUT_ = GND)
0	1	0	X	V_{PPB} (damp off)	T/R switch off (LVOUT_ = GND)	T/R switch off (LVOUT_ = GND)
1	0	0	X	V_{NNB} (damp off)	T/R switch off (LVOUT_ = GND)	T/R switch off (LVOUT_ = GND)
0	1	1	X	V_{PPA} (damp off)	T/R switch off (LVOUT_ = GND)	T/R switch off (LVOUT_ = GND)
1	0	1	X	V_{NNA} (damp off)	T/R switch off (LVOUT_ = GND)	T/R switch off (LVOUT_ = GND)
1	1	1	X	Clamp on (damp on)	T/R switch on	T/R switch off

Note: *Only three control inputs (DINNx, DINPx, DINNy) are required for five-level, dual-mode operation. DINPy can be connected to GND or V_{DD}.*

X = Don't care, 0 = logic-low, 1 = logic-high

Table 4. Transmit Disable Mode (MODE0 = High, MODE1 = High)

INPUTS		OUTPUTS	
DINN_	**DINP_**	**OUT_**	**LVOUT_ (MAX14808 ONLY)**
0	0	High impedance (damp off)	T/R switch off (LVOUT_ = GND)
1	0	High impedance (damp off)	T/R switch off (LVOUT_ = GND)
0	1	High impedance (damp off)	T/R switch off (LVOUT_ = GND)
1	1	High impedance (damp on)	T/R switch on

0 = logic-low, 1 = logic-high

Current Capability Selection

The devices feature pulser current drive capability selection. Two control inputs (CC0, CC1) control the current drive capability (Table 5).

Sync Function

The devices provide the ability to resynchronize all the data inputs by means of a clean clock signal. In ultrasound systems, the FPGA output signals are often affected by a high jitter. The jitter induces phase noise that is detrimental in Doppler analysis. The input clock can be either a differential signal or a single-ended signal running up to 160MHz. Data are clocked in on the rising edge of the CLK input (falling edge of $\overline{CLK}$). Connect $\overline{CLK}$ to GND for single-ended operation. The sync feature can be enabled or disabled by the SYNC control input. Drive the SYNC input low to disable the synchronization function (no external clock signal). Drive the SYNC input high to enable the synchronization function (with an external clock signal). Figure 6 shows the simplified CLK and $\overline{CLK}$ inputs schematic.

T/R Switches (MAX14808 Only)

Each channel features a low-power T/R switch. The T/R switch recovery time after the transmission is less than 1.2µs. The T/R switches are controlled by the same pulser digital inputs (see the *Truth Tables* section). No dedicated input signals are required to activate/deactivate the T/R switches. The integrated T/R switches do not require any special timings and can operate synchronously with the digital pulser. To minimize the leakage current during transmission, it's recommended to switch off the T/R switches 3µs before the beginning of the transmit burst.

Table 5. Current Drive Selection

INPUTS		PULSER OUTPUT CURRENT (typ)
CC0	CC1	
0	0	2A
1	0	1.5A
0	1	1A
1	1	0.5A

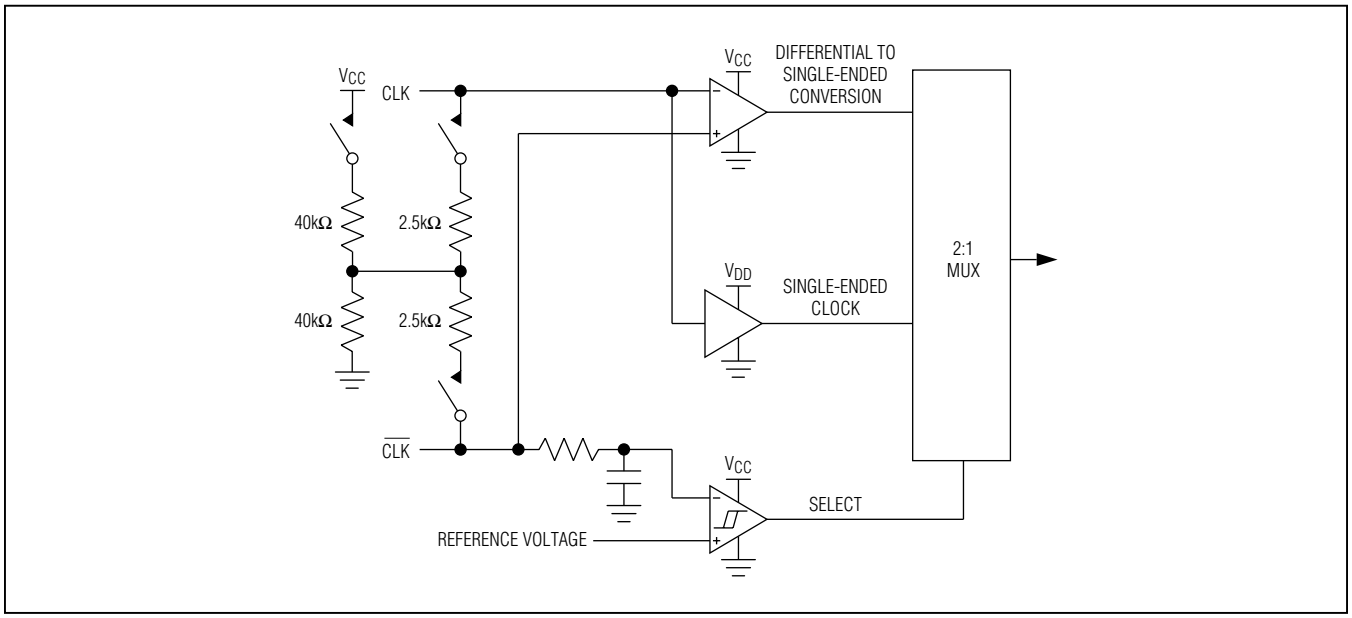


Figure 6. Simplified CLK and $\overline{CLK}$ Inputs Schematic

Grass-Clipping Diodes

A pair of diodes in antiparallel configuration (referred to as grass-clipping diodes) is presented at each pulser's output. The diodes' reverse capacitance is extremely low, allowing a perfect isolation between the receive path and the actual pulser's output stage.

Active Damp Circuit

An active damp circuit is integrated between the internal pulser output node (before grass-clipping diodes) and GND. The purpose of this circuit is to fully discharge the pulser output internal node so that the node is not left in high-impedance condition as soon as the transmit burst is over. This results in two main advantages:

1) The grass-clipping isolation is more effective.
2) Suppression of any low-frequency oscillation of a node that could be detrimental for Doppler mode performances.

Independent (Floating) Power-Supply Enable (LDO_EN)

The devices feature the $\overline{LDO\_EN}$ control input to enable/disable the internal FPSs. This allows the usage of external high-efficiency power supplies to save system power. This option must be considered only for special applications requiring extremely low power dissipation. The low power dissipation of the embedded FPSs already meets power requirements in most of the cases. Drive $\overline{LDO\_EN}$ low or leave unconnected to enable the internal FPSs; drive $\overline{LDO\_EN}$ high to disable the internal FPSs.

Thermal Warning Outputs

The devices feature an open-drain thermal-protection output (THP). When the internal junction temperature exceeds +150°C, the devices automatically enter shut-down mode and THP asserts. The devices reenter normal operation and the THP deasserts when the die temperature drops below +130°C.

Power Sequencing

When using the embedded FPSs ($\overline{LDO\_EN}$ = low), the devices do not require any power-up/power-down sequence. When external FPSs are used ($\overline{LDO\_EN}$ = high), the conditions $V_{GP\_}$ > (V_{EE} - 0.6V) and $V_{GN\_}$ < (V_{CC} + 0.6V) must be satisfied during the entire power-up/power-down transients (see the electrical characteristics tables).

Applications Information

Exposed Pad and Layout Concerns

The devices provide an exposed pad (EP) underneath the TQFN package for improved thermal performance. Connect EP to GND externally and do not run traces under the package to avoid possible short circuits. To aid heat dissipation, connect EP to a similarly sized pad on the component side of the PCB. This pad should be connected through to the solder-side copper by several plated holes to a large heat-spreading copper area to conduct heat away from the device.

The devices' high-speed pulser requires low-inductance bypass capacitors to their supply inputs. High-speed PCB trace design practices are recommended. Pay particular attention to minimize trace lengths and use sufficient trace width to reduce inductance. Use of surface-mount components is recommended.

Typical Application Circuit

Figure 7 shows the MAX14808 in an octal three-level pulsing application.

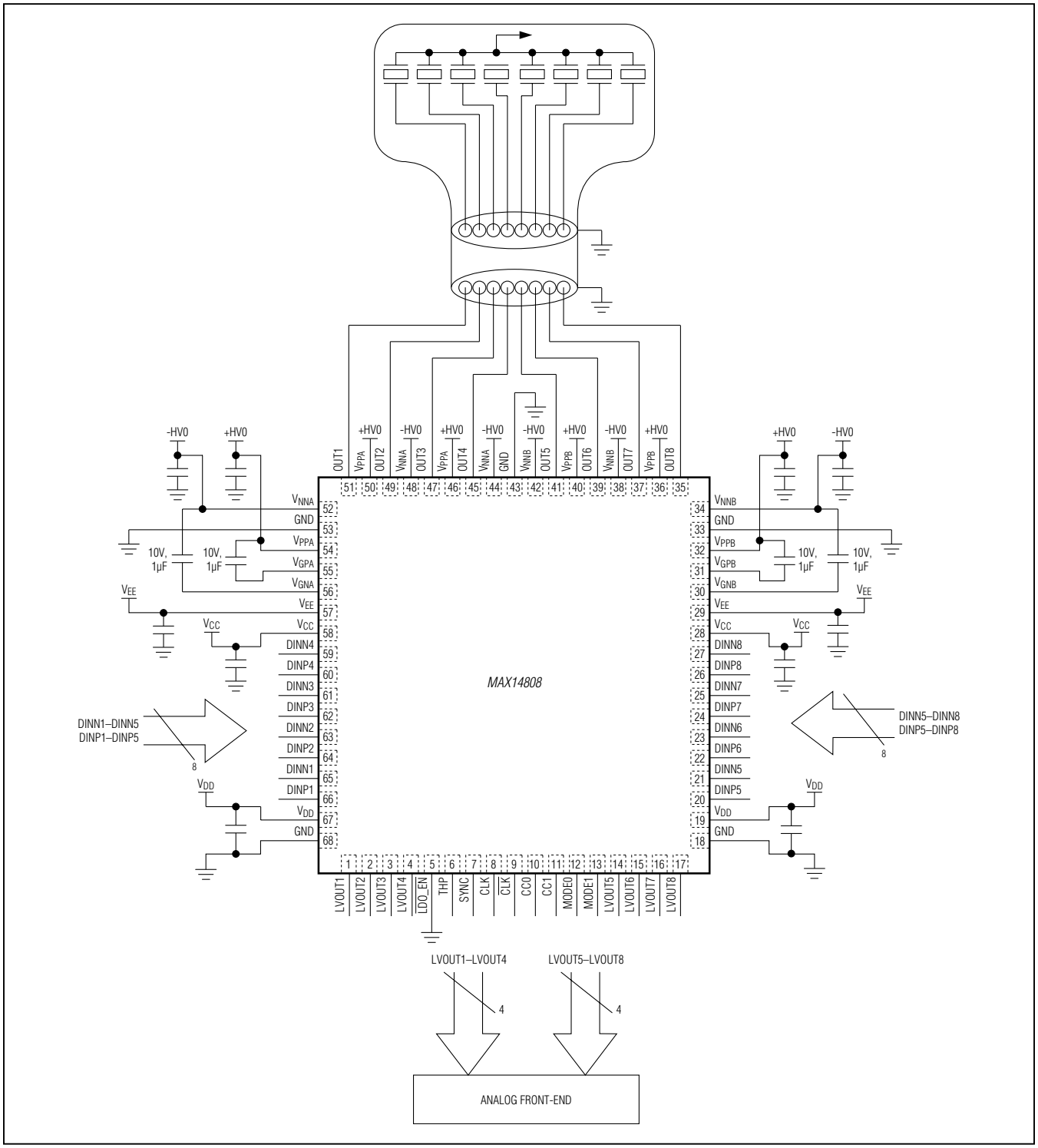
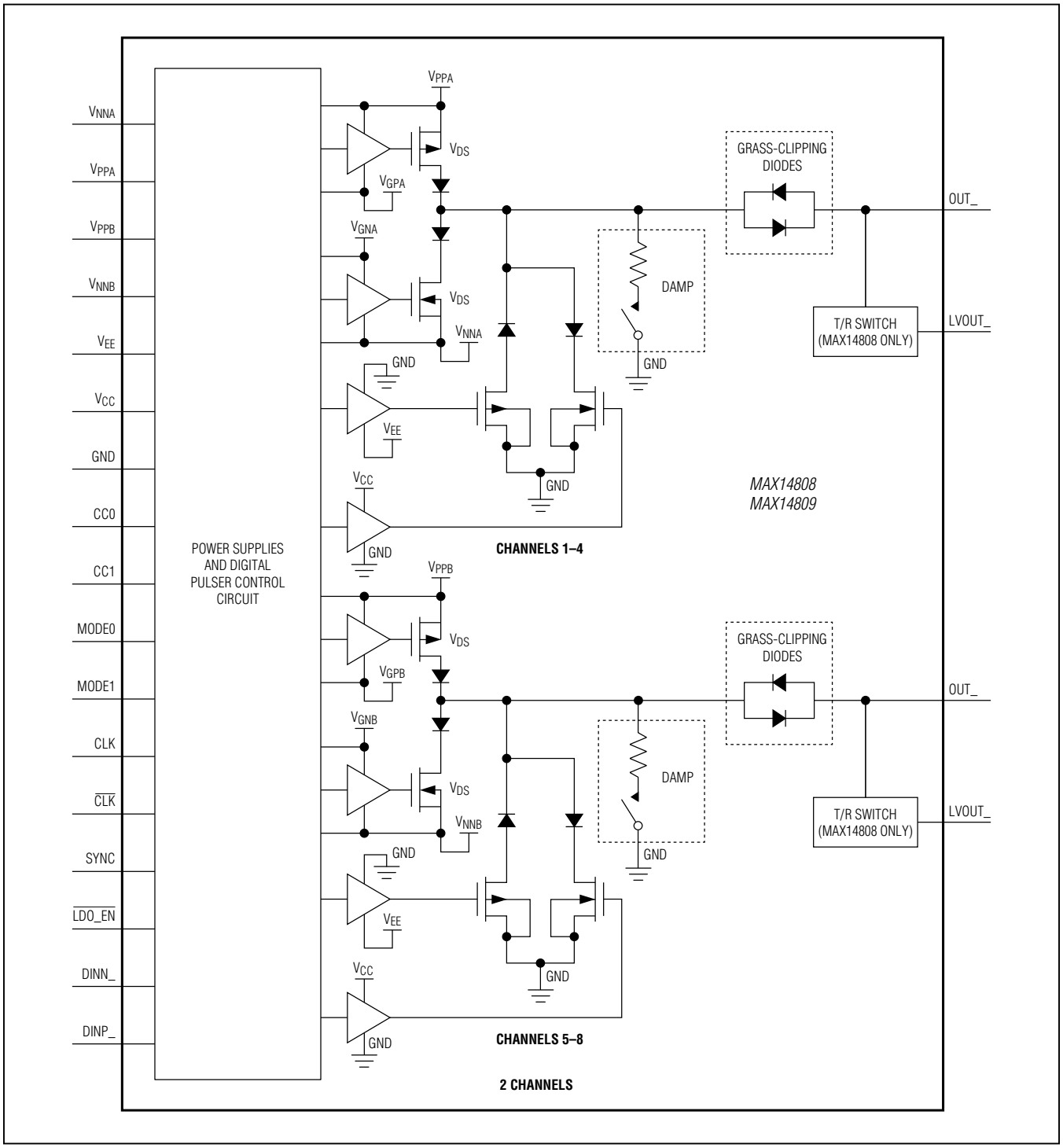


Figure 7. Octal Three-Level Pulsing (MAX14808)

Functional Diagram



Ordering Information

PART	TRANSMIT CHANNELS	T/R SWITCHES	TEMP RANGE	PIN-PACKAGE
MAX14808ETK+	Yes	Yes	-40°C to +85°C	68 TQFN-EP*
MAX14809ETK+	Yes	No	-40°C to +85°C	68 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
68 TQFN-EP	T6800+4	21-0142	90-0101

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/12	Initial release	—
1	3/13	Updated the *DC Electrical Characteristics* and *AC Electrical Characteristics* tables; updated TOC 9 in the *Typical Operating Characteristics* section; removed the future product notation from the MAX14809 in the *Ordering Information* table	5–8, 11, 17, 30
2	1/14	Updated the *DC Electrical Characteristics* and *AC Electrical Characteristics* tables	8, 9, 11

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