MAX15058 High-Efficiency, 3A, Current-Mode Synchronous, Step-Down Switching Regulator

General Description

The MAX15058 high-efficiency, current-mode, synchronous step-down switching regulator with integrated power switches delivers up to 3A of output current. The device operates from 2.7V to 5.5V and provides an output voltage from 0.6V up to 94% of the input voltage, making the device ideal for distributed power systems, portable devices, and preregulation applications.

The MAX15058 utilizes a current-mode control architecture with a high-gain transconductance error amplifier. The current-mode control architecture facilitates easy compensation design and ensures cycle-by-cycle current limit with fast response to line and load transients.

The MAX15058 offers selectable skip-mode functionality to reduce current consumption and achieve a higher efficiency at light output load. The low $R_{DS(ON)}$ integrated switches ensure high efficiency at heavy loads while minimizing critical inductances, making the layout design a much simpler task with respect to discrete solutions. Utilizing a simple layout and footprint assures first-pass success in new designs.

The MAX15058 features a 1MHz, factory-trimmed, fixed-frequency PWM mode operation. The high switching frequency, along with the PWM current-mode architecture, allows for a compact, all-ceramic capacitor design.

The MAX15058 offers a capacitor-programmable soft-start reducing inrush current, startup into PREBIAS operations, and a PGOOD open-drain output that can be used as an interrupt and for power sequencing.

The MAX15058 is available in a 9-bump (3 x 3 array), 1.5mm x 1.5mm WLP package and is specified over the -40°C to +85°C temperature range.

Applications

- Distributed Power Systems
- Preregulators for Linear Regulators
- Portable Devices
- Notebook Power
- Server Power
- IP Phones

Features

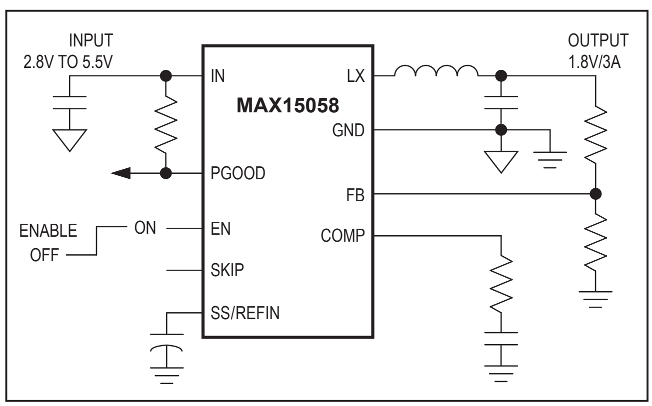
- Internal 30mΩ (typ) $R_{DS(ON)}$ High-Side and 18mΩ (typ) Low-Side MOSFETs at 5V
- Continuous 3A Output Current Over Temperature
- 95% Efficiency with 3.3V Output at 3A
- 1% Output Voltage Accuracy Over Load, Line, and Temperature
- Operates from 2.7V to 5.5V Supply
- Cycle-by-Cycle Overcurrent Protection
- Adjustable Output from 0.6V to Up to 0.94 x V_{IN}
- Programmable Soft-Start
- Factory-Trimmed, 1MHz Switching Frequency
- Stable with Low-ESR Ceramic Output Capacitors
- Safe-Startup Into Prebiased Output
- External Reference Input
- Skip-Mode Functionality
- Enable Input/Power-Good Output
- Fully Protected Against Overcurrent and Overtemperature
- Input Undervoltage Lockout

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX15058EWL+	-40°C to +85°C	9 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

Typical Operating Circuit



Absolute Maximum Ratings

IN, PGOOD to GND ....-0.3V to +6V
LX to GND ....-0.3V to (V_{IN} + 0.3V)
LX to GND .... -1V to (V_{IN} + 0.3V) for 50ns
EN, COMP, FB, SS/REFIN, SKIP to GND .-0.3V to (V_{IN} + 0.3V)
LX Current (Note 1) .... -6A to +6A
Output Short-Circuit Duration ....Continuous

Continuous Power Dissipation (T_A = +70°C)
9-Bump WLP Multilayer Board
(derate 14.1mW/°C above T_A = +70°C)...................1127mW
Operating Temperature Range.......................... -40°C to +85°C
Storage Temperature Range........................... -65°C to +150°C
Soldering Temperature (reflow).....................................+260°C

Note 1: LX has internal clamp diodes to GND and IN. Applications that forward bias these diodes should not exceed the IC's package power dissipation limits.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 9 WLP	
Package Code	W91E1Z+1
Outline Number	**21-0508**
Land Pattern Number	Refer to **Application Note 1891**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	71°C/W
Junction to Case (θ_{JC})	26°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = 5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IN Voltage Range	V_{IN}		2.7		5.5	V
IN Shutdown Supply Current		V_{EN} = 0V		0.2	2	µA
IN Supply Current	I_{IN}	V_{EN} = 5V, V_{FB} = 0.65V, no switching		1.56	2.3	mA
V_{IN} Undervoltage Lockout Threshold		LX starts switching, V_{IN} rising		2.6	2.7	V
V_{IN} Undervoltage Lockout Hysteresis		LX stops switching, V_{IN} falling		200		mV
ERROR AMPLIFIER						
Transconductance	g_{MV}			1.5		mS
Voltage Gain	A_{VEA}			90		dB
FB Set-Point Accuracy	V_{FB}	Over line, load, and temperature	594	600	606	mV
FB Input Bias Current	I_{FB}	V_{FB} = 0.6V	-500		+500	nA
COMP to Current-Sense Transconductance	g_{MC}			18		A/V
COMP Clamp Low		V_{FB} = 0.65V, V_{SS} = 0.6V		0.94		V
POWER SWITCHES						
LX On-Resistance, High-Side pMOS				30		mΩ
LX On-Resistance, Low-Side nMOS				18		mΩ
High-Side Switch Current-Limit Threshold	I_{HSCL}			5		A
Low-Side Switch Sink Current-Limit Threshold				4		A
Low-Side Switch Source Current-Limit Threshold				5		A
LX Leakage Current		V_{EN} = 0V			10	µA
RMS LX Output current			3			A
OSCILLATOR						
Switching Frequency	f_{SW}		850	1000	1150	kHz
Maximum Duty Cycle	D_{MAX}			94		%
Minimum Controllable On-Time				70		ns
Slope Compensation Ramp Valley				1.15		V
Slope Compensation Ramp Amplitude	V_{SLOPE}	Extrapolated to 100% duty cycle		320		mV

Electrical Characteristics (continued)

(V_{IN} = 5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

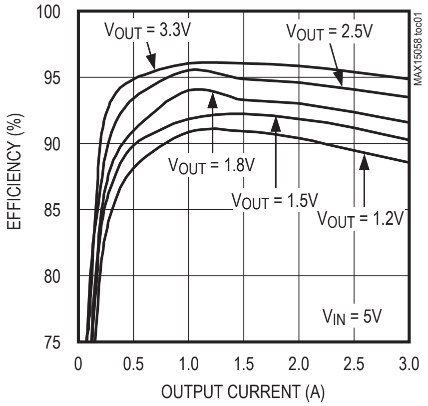
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE						
EN Input High Threshold Voltage		V_{EN} rising			1.45	V
EN Input Low Threshold Voltage		V_{EN} falling	0.4			V
EN Input Leakage Current		V_{EN} = 5V		0.025		µA
SKIP Input Leakage Current		V_{SKIP} = V_{EN} = 5V		25		µA
SOFT-START, PREBIAS, REFIN						
Soft-Start Current	I_{SS}	$V_{SS/REFIN}$ = 0.45V, sourcing		10		µA
SS/REFIN Discharge Resistance	R_{SS}	$I_{SS/REFIN}$ = 10mA, sinking		8.3		Ω
SS/REFIN Prebias Mode Stop Voltage		$V_{SS/REFIN}$ rising		0.58		V
External Reference Input Range			0		IN - 1.8	V
HICCUP						
Number of Consecutive Current-Limit Events to Hiccup				8		Events
Timeout				1024		Clock Cycles
POWER-GOOD OUTPUT						
PGOOD Threshold		V_{FB} rising	0.535	0.555	0.575	V
PGOOD Threshold Hysteresis		V_{FB} falling		28		mV
PGOOD V_{OL}		I_{PGOOD} = 5mA, V_{FB} = 0.5V		20	60	mV
PGOOD Leakage		V_{PGOOD} = 5V, V_{FB} = 0.65V		0.013		µA
THERMAL SHUTDOWN						
Thermal Shutdown Threshold				150		°C
Thermal Shutdown Hysteresis		Temperature falling		20		°C

Note 2: Specifications are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.

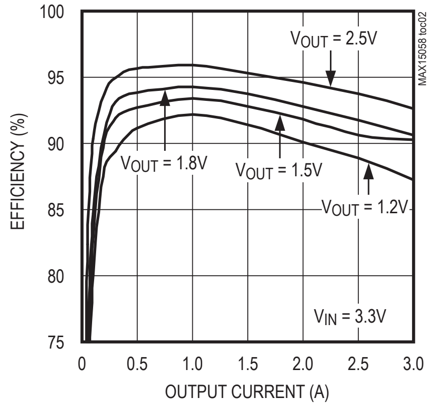
Typical Operating Characteristics

(V_{IN} = 5V, V_{OUT} = 1.8V, I_{LOAD} = 3A, Circuit of Figure 5, T_A = +25°C, unless otherwise noted.)

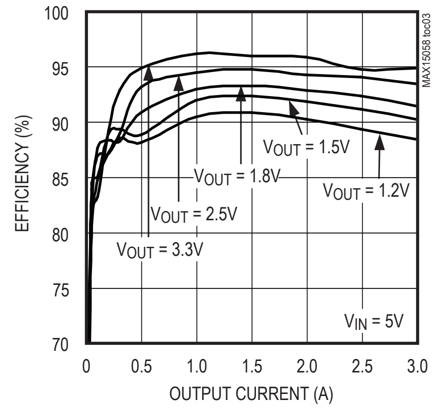
EFFICIENCY vs. LOAD CURRENT (PWM MODE)



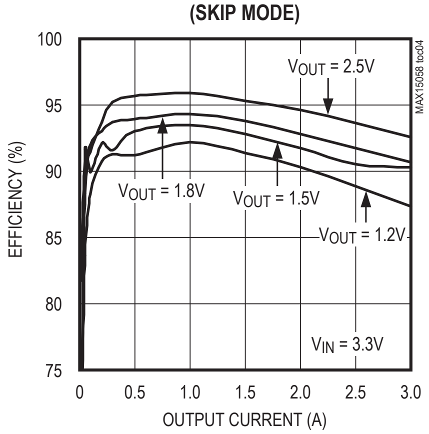
EFFICIENCY vs. OUTPUT CURRENT (FORCED PWM)



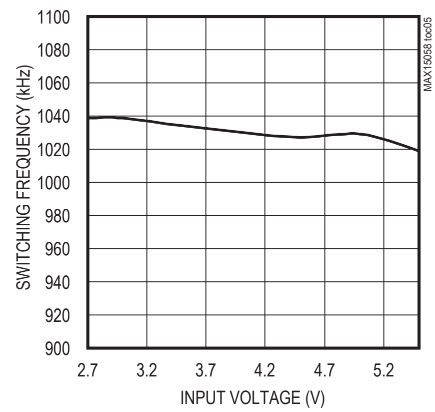
EFFICIENCY vs. LOAD CURRENT (SKIP MODE)



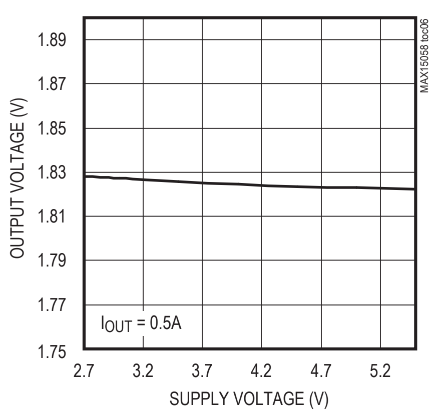
EFFICIENCY vs. OUTPUT CURRENT (SKIP MODE)



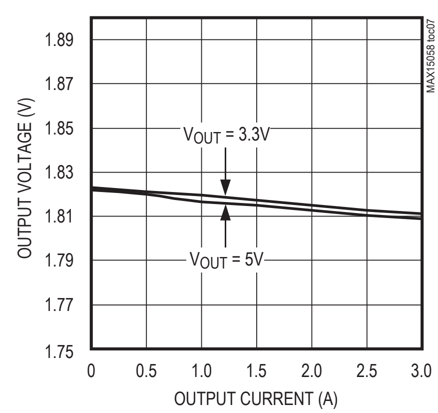
SWITCHING FREQUENCY vs. INPUT VOLTAGE



OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



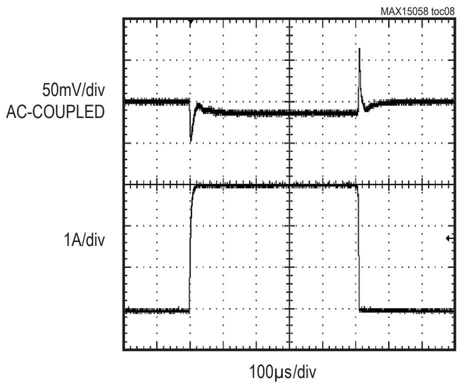
OUTPUT VOLTAGE vs. OUTPUT CURRENT



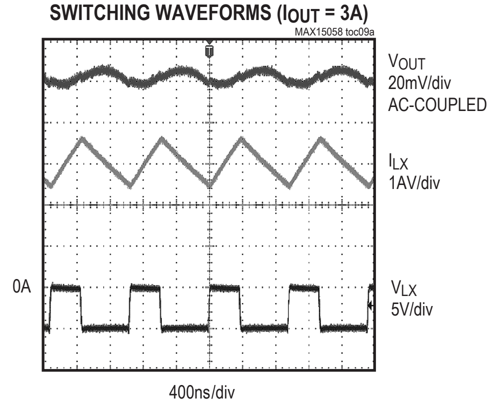
Typical Operating Characteristics (continued)

(V_{IN} = 5V, V_{OUT} = 1.8V, I_{LOAD} = 3A, Circuit of Figure 5, T_A = +25°C, unless otherwise noted.)

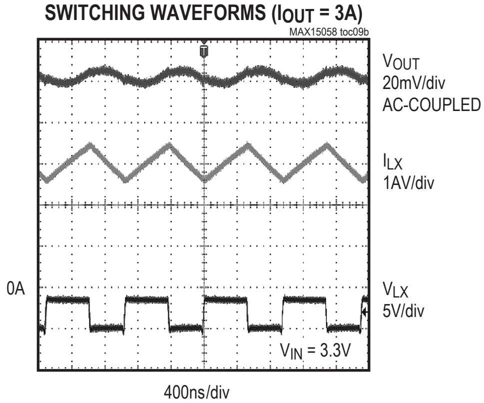
LOAD-TRANSIENT RESPONSE



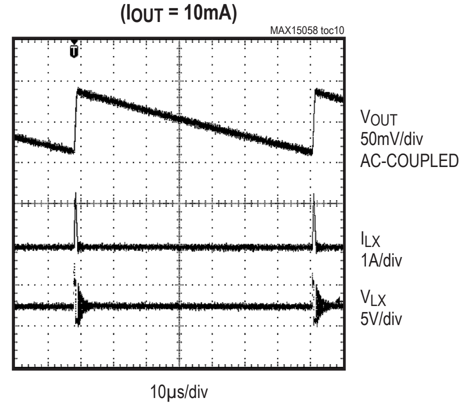
SWITCHING WAVEFORMS (I_{OUT} = 3A)



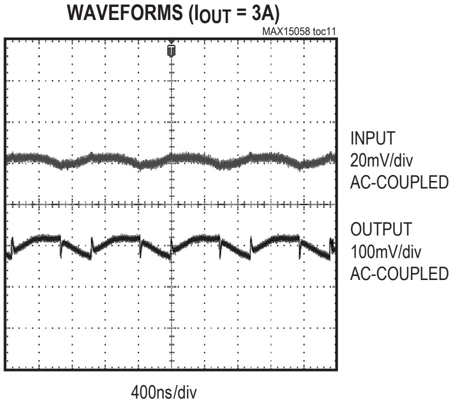
SWITCHING WAVEFORMS (I_{OUT} = 3A)



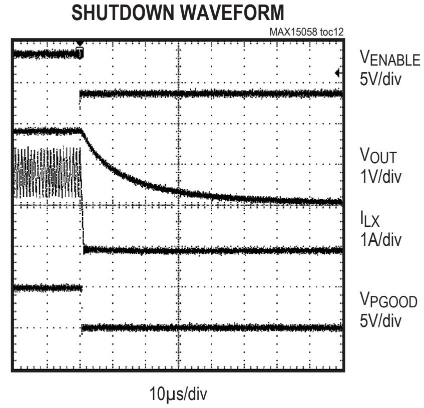
SWITCHING WAVEFORM IN SKIP MODE (I_{OUT} = 10mA)



INPUT AND OUTPUT WAVEFORMS (I_{OUT} = 3A)



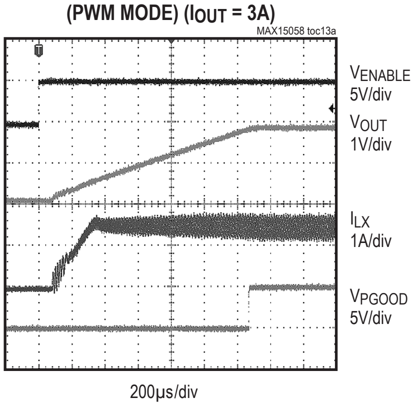
SHUTDOWN WAVEFORM



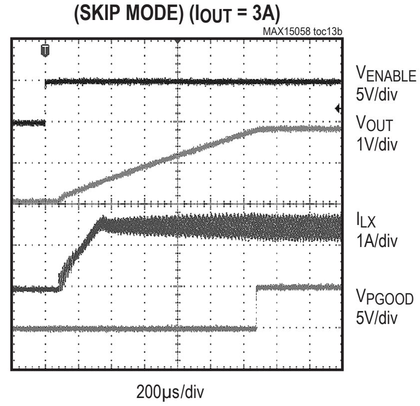
Typical Operating Characteristics (continued)

(V_{IN} = 5V, V_{OUT} = 1.8V, I_{LOAD} = 3A, Circuit of Figure 5, T_A = +25°C, unless otherwise noted.)

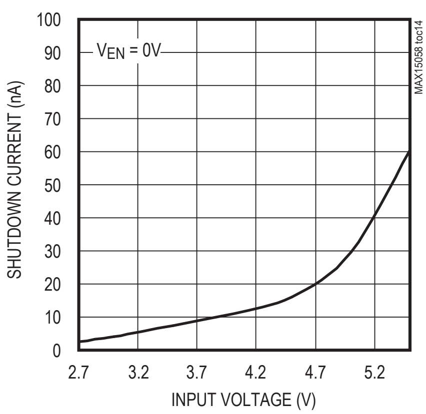
SOFT-START WAVEFORMS (PWM MODE) (I_{OUT} = 3A)



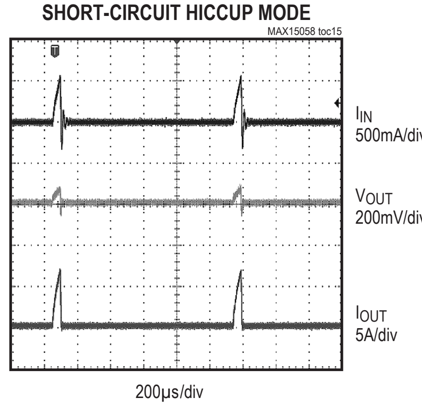
SOFT-START WAVEFORMS (SKIP MODE) (I_{OUT} = 3A)



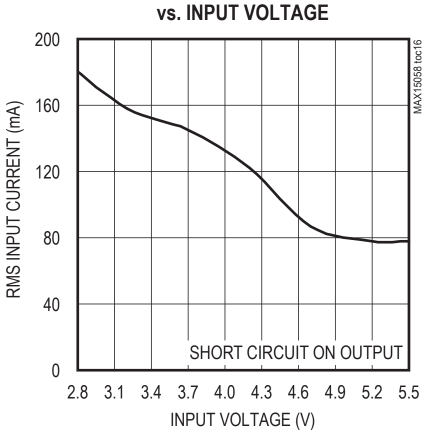
SHUTDOWN CURRENT vs. INPUT VOLTAGE



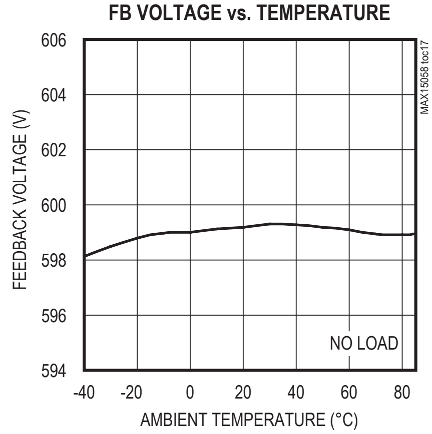
SHORT-CIRCUIT HICCUP MODE



RMS INPUT CURRENT vs. INPUT VOLTAGE



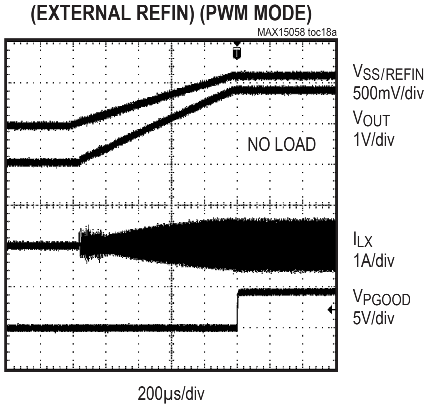
FB VOLTAGE vs. TEMPERATURE



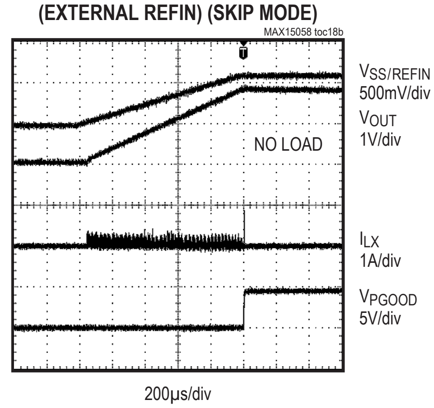
Typical Operating Characteristics (continued)

(V_{IN} = 5V, V_{OUT} = 1.8V, I_{LOAD} = 3A, Circuit of Figure 5, T_A = +25°C, unless otherwise noted.)

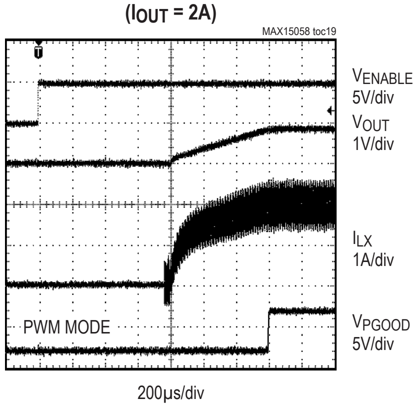
SOFT-START WAVEFORMS (EXTERNAL REFIN) (PWM MODE)



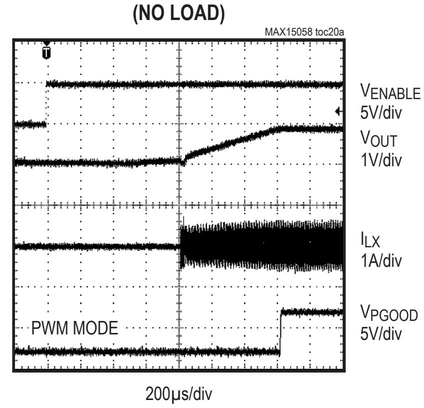
SOFT-START WAVEFORMS (EXTERNAL REFIN) (SKIP MODE)



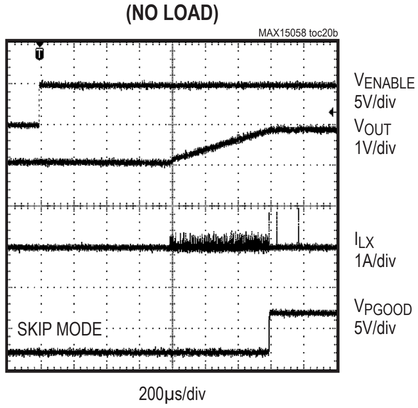
STARTING INTO A PREBIASED OUTPUT (I_{OUT} = 2A)



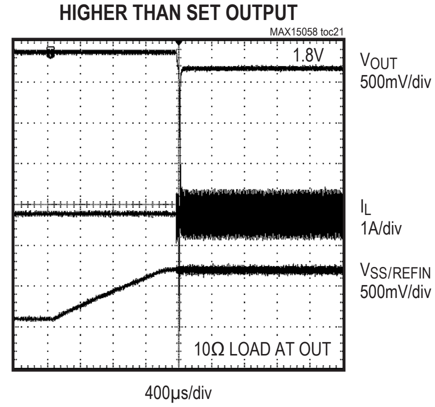
STARTING INTO A PREBIASED OUTPUT (NO LOAD)



STARTING INTO A PREBIASED OUTPUT (NO LOAD)

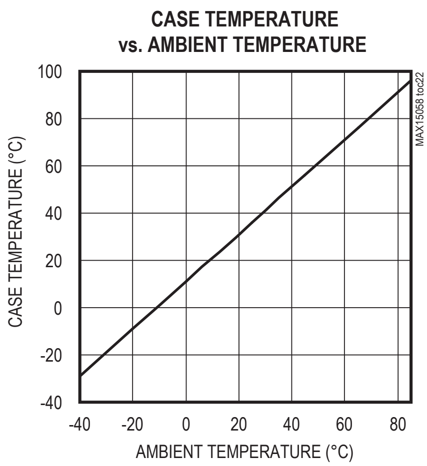


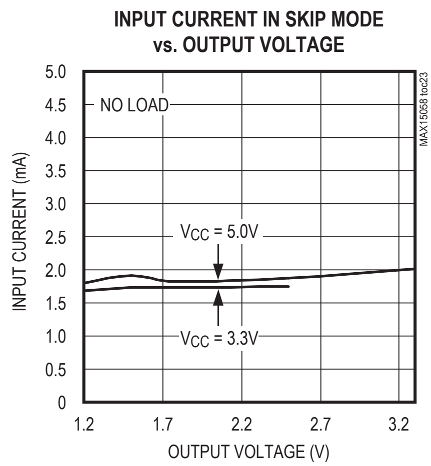
STARTING INTO A PREBIASED OUTPUT HIGHER THAN SET OUTPUT



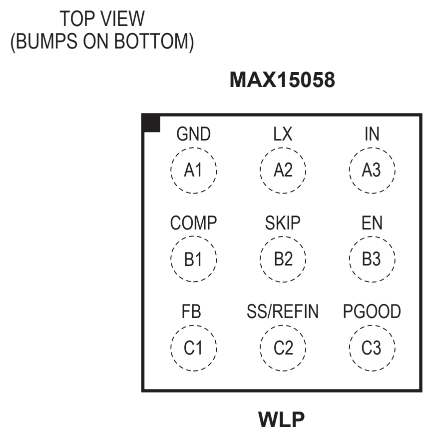
Typical Operating Characteristics (continued)

(V_{IN} = 5V, V_{OUT} = 1.8V, I_{LOAD} = 3A, Circuit of Figure 5, T_A = +25°C, unless otherwise noted.)





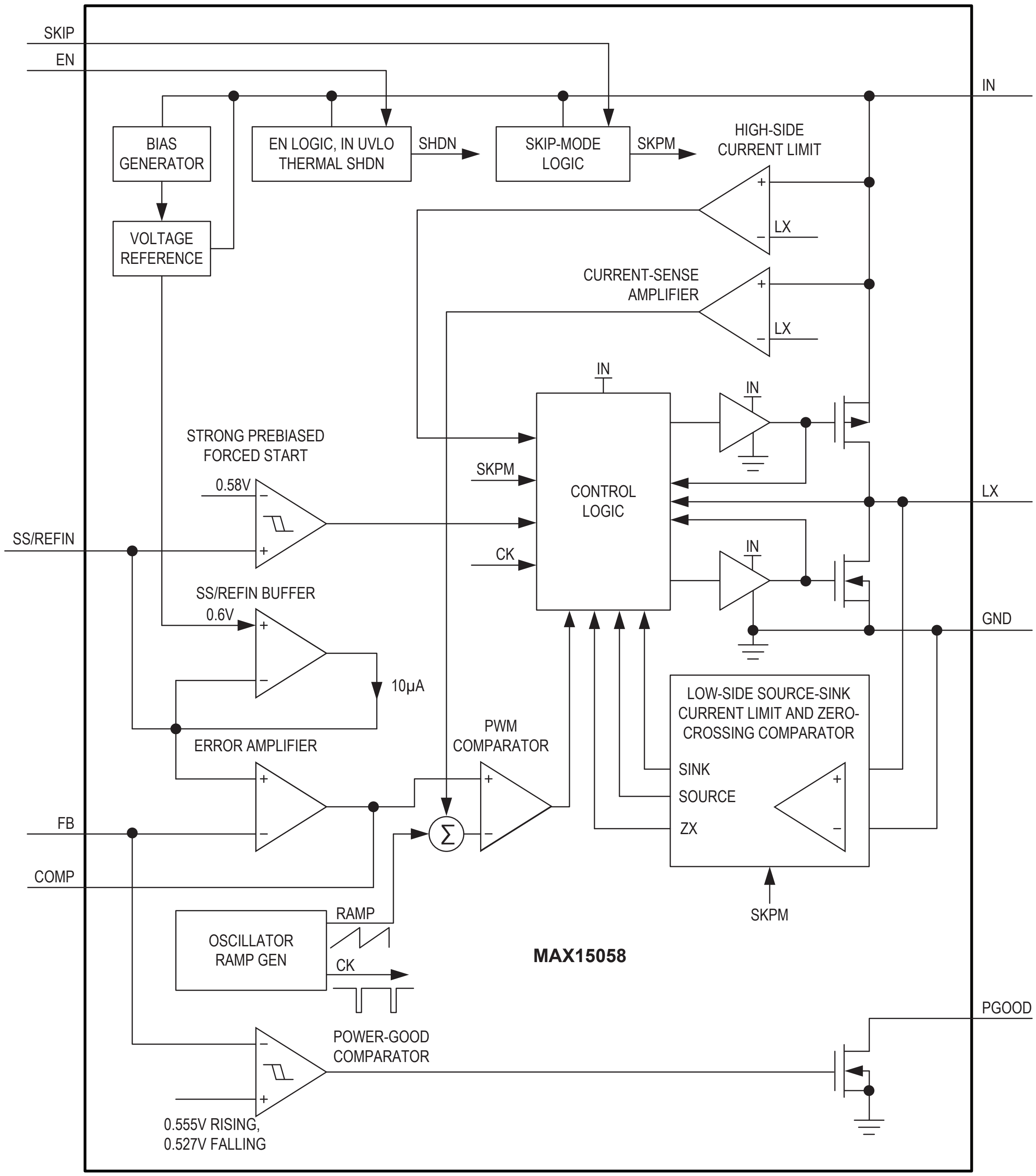
Pin Configuration



Pin Description

BUMP	NAME	FUNCTION
A1	GND	Analog Ground/Low-Side Switch Source Terminal. Connect to the PCB copper plane at one point near the input bypass capacitor return terminal.
A2	LX	Inductor Connection. Connect LX to the switched side of the inductor. LX is high impedance when the IC is in shutdown mode.
A3	IN	Input Power Supply. Input supply range is from 2.7V to 5.5V. Bypass with a minimum 10µF ceramic capacitor to GND. See Figures 5 and 6.
B1	COMP	Voltage Error-Amplifier Output. Connect the necessary compensation network from COMP to GND. See the *Closing the Loop: Designing the Compensation Circuitry* section.
B2	SKIP	Skip-Mode Input. Connect to EN to select skip mode or leave unconnected for normal operation.
B3	EN	Enable Input. EN is a digital input that turns the regulator on and off. Drive EN high to turn on the regulator. Connect to IN for always-on operation.
C1	FB	Feedback Input. Connect FB to the center tap of an external resistor-divider from the output to GND to set the output voltage from 0.6V up to 94% of V_{IN}.
C2	SS/REFIN	Soft-Start/External Voltage Reference Input. Connect a capacitor from SS/REFIN to GND to set the startup time. See the *Setting the Soft-Start Time* section for details on setting the soft-start time. Apply a voltage reference from 0V to V_{IN} - 1.5V to drive soft-start externally.
C3	PGOOD	Open-Drain Power-Good Output. PGOOD goes high when FB is above 555mV and pulls low if FB is below 527mV.

Block Diagram



Detailed Description

The MAX15058 high-efficiency, current-mode switching regulator can deliver up to 3A of output current. The MAX15058 provides output voltages from 0.6V to 0.94 x V_{IN} from 2.7V to 5.5V input supplies, making the device ideal for on-board point-of-load applications.

The MAX15058 delivers current-mode control architecture using a high-gain transconductance error amplifier. The current-mode control architecture facilitates easy compensation design and ensures cycle-by-cycle current limit with fast response to line and load transients.

The MAX15058 features a 1MHz fixed switching frequency, allowing for all-ceramic capacitor designs and fast transient responses. The high operating frequency minimizes the size of external components. The MAX15058 is available in a 1.5mm x 1.5mm (3 x 3 array) x 0.5mm pitch WLP package.

The MAX15058 offers a selectable skip-mode functionality to reduce current consumption and achieve a higher efficiency at light output loads. The low $R_{DS(ON)}$ integrated switches (30mΩ high-side and 18mΩ low-side, typ) ensure high efficiency at heavy loads while minimizing critical inductances, making the layout design a much simpler task with respect to discrete solutions. Utilizing a simple layout and footprint assures first-pass success in new designs.

The MAX15058 features 1MHz ±15%, factory-trimmed, fixed-frequency PWM mode operation. The MAX15058 also offers capacitor-programmable, soft-start reducing inrush current, startup into PREBIAS operation, and a PGOOD open-drain output for sequencing with other devices.

Controller Function—PWM Logic

The controller logic block is the central processor that determines the duty cycle of the high-side MOSFET under different line, load, and temperature conditions. Under normal operation, where the current-limit and temperature protection are not triggered, the controller logic block takes the output from the PWM comparator and generates the driver signals for both high-side and low-side MOSFETs. The control logic block controls the break-before-make logic and all the necessary timing.

The high-side MOSFET turns on at the beginning of the oscillator cycle and turns off when the COMP voltage crosses the internal current-mode ramp waveform, which is the sum of the slope compensation ramp and the current-mode ramp derived from inductor current (current-sense block). The high-side MOSFET also turns off if the maximum duty cycle is 94%, or when the current limit is reached. The low-side MOSFET turns on for the remainder of the oscillation cycle.

Starting into a Prebiased Output

The MAX15058 can soft-start into a prebiased output without discharging the output capacitor. In safe prebiased startup, both low-side and high-side MOSFETs remain off to avoid discharging the prebiased output. PWM operation starts when the voltage on SS/REFIN crosses the voltage on FB.

The MAX15058 can start into a prebiased voltage higher than the nominal set point without abruptly discharging the output. Forced PWM operation starts when the SS/REFIN voltage reaches 0.58V (typ), forcing the converter to start. In case of prebiased output, below or above the output nominal set point, if low-side sink current-limit threshold (set to the reduced value of -0.4A (typ) for the first 32 clock cycles and then set to -5A (typ)) is reached, the low-side switch turns off before the end of the clock period, and the high-side switch turns on until one of the following conditions is satisfied:

- High-side source current hits the reduced high-side current limit (0.4A, typ); in this case, the high-side switch is turned off for the remaining time of the clock period.
- The clock period ends. Reduced high-side current limit is activated to recirculate the current into the high-side power switch rather than into the internal high-side body diode, which could be damaged. Low-side sink current limit is provided to protect the low-side switch from excessive reverse current during prebiased operation.

In skip mode operation, the prebias output needs to be lower than the set point.

Enable Input

The MAX15058 features independent device enable control and power-good signal that allow for flexible power sequencing. Drive the enable input (EN) high to enable the regulator, or connect EN to IN for always-on operation. Power-good (PGOOD) is an open-drain output that asserts when V_{FB} is above 555mV (typ), and deasserts low if V_{FB} is below 527mV (typ).

Programmable Soft-Start (SS/REFIN)

The MAX15058 utilizes a soft-start feature to slowly ramp up the regulated output voltage to reduce input inrush current during startup. Connect a capacitor from SS/REFIN to GND to set the startup time (see the *Setting the Soft-Start Time* section for capacitor selection details).

Error Amplifier

A high-gain error amplifier provides accuracy for the voltage-feedback loop regulation. Connect the necessary compensation network between COMP and GND (see the *Compensation Design Guidelines* section). The error-amplifier transconductance is 1.5mS (typ). COMP clamp low is set to 0.94V (typ), just below the slope ramp compensation valley, helping COMP to rapidly return to the correct set point during load and line transients.

PWM Comparator

The PWM comparator compares COMP voltage to the current-derived ramp waveform (LX current to COMP voltage transconductance value is 18A/V typ). To avoid instability due to subharmonic oscillations when the duty cycle is around 50% or higher, a slope compensation ramp is added to the current-derived ramp waveform. Confirm the compensation ramp slope (0.3V x 1MHz = 0.3V/µs) is equivalent to half the inductor current downslope in the worst case (load 3A, current ripple 30% and maximum duty-cycle operation of 94%). The slope compensation ramp valley is set to 1.15V (typ).

Overcurrent Protection and Hiccup

When the converter output is shorted or the device is overloaded, each high-side MOSFET current-limit event (5A typ) turns off the high-side MOSFET and turns on the low-side MOSFET. On each current-limit event a 3-bit counter is incremented. The counter is reset after three consecutive high-side MOSFETs turn on without reaching current limit. If the current-limit condition persists, the counter fills up reaching eight events. The control logic then discharges SS/REFIN, stops both high-side and low-side MOSFETs, and waits for a hiccup period (1024 clock cycles typ) before attempting a new soft-start sequence. The hiccup mode is also enabled during soft-start time.

Thermal-Shutdown Protection

The MAX15058 contains an internal thermal sensor that limits the total power dissipation to protect the device in the event of an extended thermal fault condition. When the die temperature exceeds +150°C (typ), the thermal sensor shuts down the device, turning off the DC-DC converter to allow the die to cool. After the die temperature falls by 20°C (typ), the device restarts, following the soft-start sequence.

Skip Mode Operation

The MAX15058 operates in skip mode when SKIP is connected to EN. When in skip mode, LX output becomes high impedance when the inductor current falls below 200mA (typ). The inductor current does not become negative. If during a clock cycle the inductor current falls below the 200mA threshold (during off-time), the low side turns off. At the next clock cycle, if the output voltage is above set point, the PWM logic keeps both high-side and low-side MOSFETs off. If instead the output voltage is below the set point, the PWM logic drives the high-side on for a minimum fixed on-time (300ns typ). In this way the system can skip cycles, reducing frequency of operations, and switches only as needed to service load at the cost of an increase in output voltage ripple (see the *Skip Mode Frequency and Output Ripple* section). In skip mode, power dissipation is reduced and efficiency is improved at light loads because power MOSFETs do not switch at every clock cycle.

Applications Information

Setting the Output Voltage

The MAX15058 output voltage is adjustable from 0.6V up to 94% of V_{IN} by connecting FB to the center tap of a resistor-divider between the output and GND (Figure 1). Choose R1 and R2 so that the DC errors due to the FB input bias current (±500nA) do not affect the output voltage accuracy. With lower value resistors, the DC error is reduced, but the amount of power consumed in the resistor-divider increases. A typical value for R2 is 10kΩ, but values between 5kΩ and 50kΩ are acceptable. Once R2 is chosen, calculate R1 using:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right)$$

where the feedback threshold voltage, V_{FB} = 0.6V (typ). When regulating for an output of 0.6V in skip mode, short FB to OUT and keep R2 connected from FB to GND.

Inductor Selection

A high-valued inductor results in reduced inductor ripple current, leading to a reduced output ripple voltage. However, a high-valued inductor results in either a larger physical size or a high series resistance (DCR) and a lower saturation current rating. Typically, choose an inductor value to produce a current ripple equal to 30% of load current. Choose the inductor with the following formula:

$$L = \frac{V_{OUT}}{f_{SW} \times LIR \times I_{LOAD}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where f_{SW} is the internally fixed 1MHz switching frequency, and LIR is the desired inductor current ratio (typically

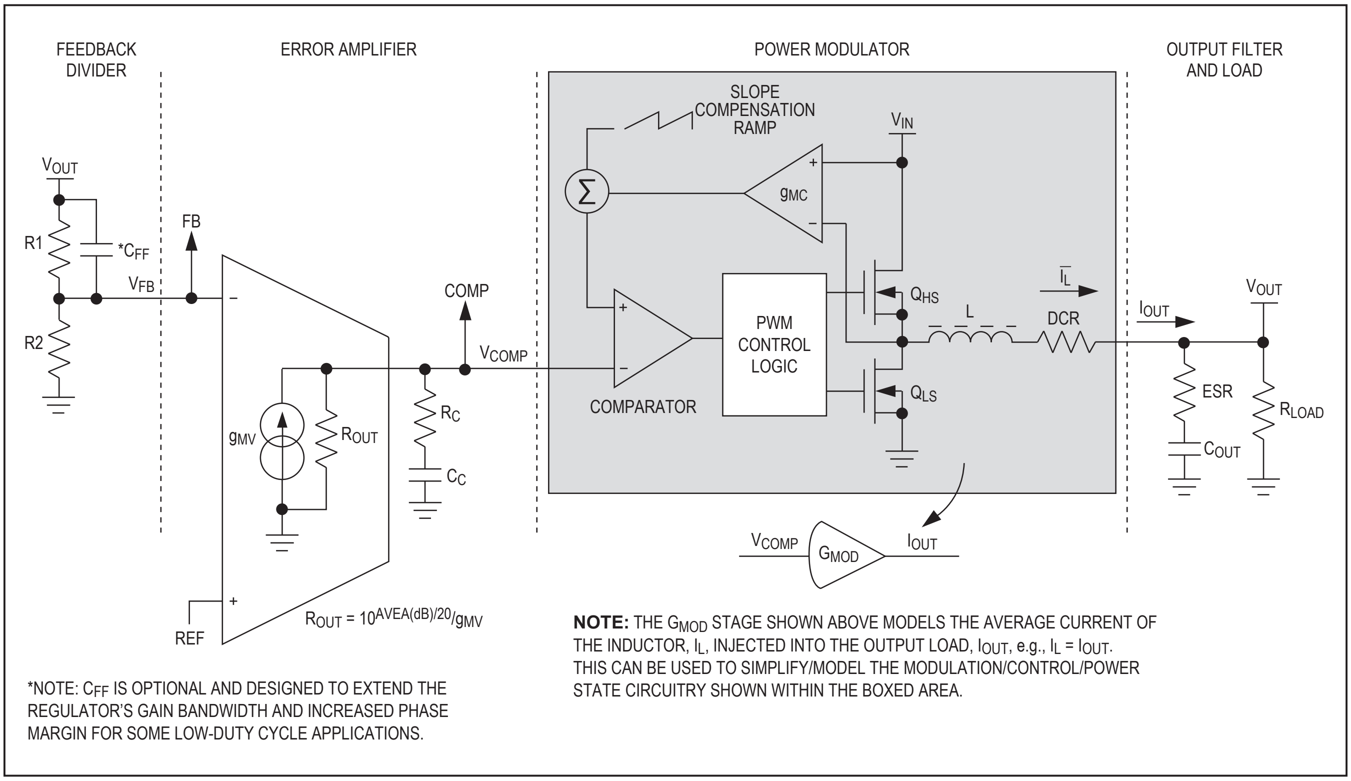


Figure 1. Peak Current-Mode Regulator Transfer Model

set to 0.3). In addition, the peak inductor current, I_{L_PK}, must always be below the minimum high-side current-limit value, I_{HSCL}, and the inductor saturation current rating, I_{L_SAT}.

Ensure that the following relationship is satisfied:

$$I_{L\_PK} = I_{LOAD} + \frac{1}{2}\Delta I_L < \min\left(I_{HSCL\_}, I_{L\_SAT}\right)$$

Input Capacitor Selection

The input capacitor reduces the peak current drawn from the input power supply and reduces switching noise in the device. The total input capacitance must be equal to or greater than the value given by the following equation to keep the input ripple voltage within the specification and minimize the high-frequency ripple current being fed back to the input source:

$$C_{IN} = \frac{I_{LOAD}}{f_{SW} \times \Delta V_{IN\_RIPPLE}} \times \frac{V_{OUT}}{V_{IN}}$$

where ΔV_{IN_RIPPLE} is the maximum-allowed input ripple voltage across the input capacitors and is recommended to be less than 2% of the minimum input voltage, f_{SW} is the switching frequency (1MHz), and I_{LOAD} is the output load. The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source, but are instead shunted through the input capacitor.

The input capacitor must meet the ripple current requirement imposed by the switching currents. The RMS input ripple current is given by:

$$I_{RIPPLE} = \left[\frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}\right] I_{LOAD}$$

where I_{RIPPLE} is the input RMS ripple current.

Output Capacitor Selection

The key selection parameters for the output capacitor are capacitance, ESR, ESL, and voltage rating. The parameters affect the overall stability, output ripple voltage, and transient response of the DC-DC converter. The output ripple occurs due to variations in the charge stored in the output capacitor, the voltage drop due to the capacitor's ESR, and the voltage drop due to the capacitor's ESL. Estimate the output-voltage ripple due to the output capacitance, ESR, and ESL as follows:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR\_COUT} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right)$$

For ceramic capacitors, ESR contribution is negligible:

$$R_{ESR\_OUT} << \frac{1}{8 \times f_{SW} \times C_{OUT}}$$

For tantalum or electrolytic capacitors, ESR contribution is dominant:

$$R_{ESR\_OUT} >> \frac{1}{8 \times f_{SW} \times C_{OUT}}$$

Use these equations for initial output-capacitor selection. Determine final values by testing a prototype or an evaluation circuit. A smaller ripple current results in less output-voltage ripple. Since the inductor ripple current is a factor of the inductor value, the output-voltage ripple decreases with larger inductance. Use ceramic capacitors for low ESR and low ESL at the switching frequency of the converter. The ripple voltage due to ESL is negligible when using ceramic capacitors.

Load-transient response also depends on the selected output capacitance. During a load transient, the output instantly changes by ESR x ΔI_{LOAD}. Before the controller can respond, the output deviates further, depending on the inductor and output capacitor values. After a short time, the controller responds by regulating the output voltage back to the predetermined value.

Use higher C_{OUT} values for applications that require light load operation or transition between heavy load and light load, triggering skip mode, causing output undershooting or overshooting. When applying the load, limit the output undershoot by sizing C_{OUT} according to the following formula:

$$C_{OUT} \cong \frac{\Delta I_{LOAD}}{3f_{CO} \times \Delta V_{OUT}}$$

where ΔI_{LOAD} is the total load change, f_{CO} is the regulator unity-gain bandwidth (or zero crossover frequency), and ΔV_{OUT} is the desired output undershooting. When removing the load and entering skip mode, the device cannot control output overshooting, since it has no sink current capability; see the *Skip Mode Frequency and Output Ripple* section to properly size C_{OUT}.

Skip Mode Frequency and Output Ripple

In skip mode, the switching frequency (f_{SKIP}) and output ripple voltage ($V_{OUT-RIPPLE}$) shown in Figure 2 are calculated as follows:

t_{ON} is a fixed time (300ns, typ); the peak inductor current reached is:

$$I_{SKIP-LIMIT} = \frac{V_{IN} - V_{OUT}}{L} \times t_{ON}$$

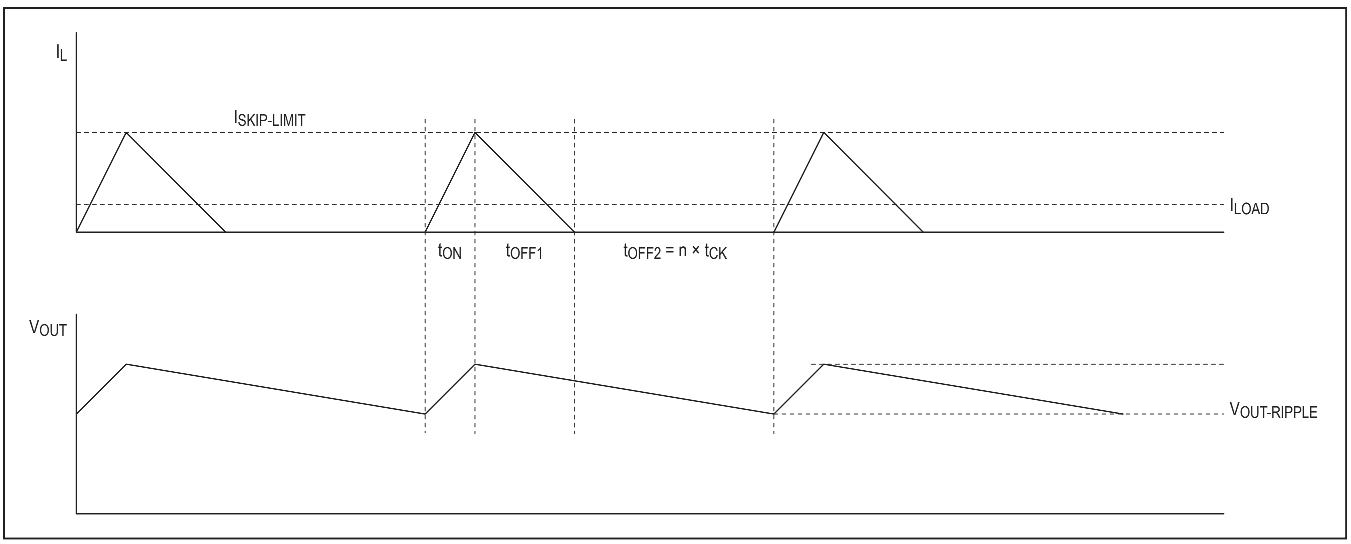


Figure 2. Skip Mode Waveform

t_{OFF1} is the time needed for inductor current to reach the zero-current crossing limit (~0A):

$$t_{OFF1} = \frac{L \times I_{SKIP-LIMIT}}{V_{OUT}}$$

During t_{ON} and t_{OFF1}, the output capacitor stores a charge equal to (see Figure 2):

$$\Delta Q_{OUT} = \frac{L \times (I_{SKIP-LIMIT} - I_{LOAD})^2 \times \left(\frac{1}{V_{IN} - V_{OUT}} + \frac{1}{V_{OUT}}\right)}{2}$$

During t_{OFF2} (= n x t_{CK}, number of clock cycles skipped), output capacitor loses this charge:

$$t_{OFF2} = \frac{\Delta Q_{OUT}}{I_{LOAD}} \Rightarrow$$

$$t_{OFF2} = \frac{L \times (I_{SKIP-LIMIT} - I_{LOAD})^2 \times \left(\frac{1}{V_{IN} - V_{OUT}} + \frac{1}{V_{OUT}}\right)}{2 \times I_{LOAD}}$$

Finally, frequency in skip mode is:

$$f_{SKIP} = \frac{1}{t_{ON} + t_{OFF1} + t_{OFF2}}$$

Output ripple in skip mode is:

$$V_{OUT-RIPPLE} = V_{COUT-RIPPLE} + V_{ESR-RIPPLE}$$
$$= \frac{(I_{SKIP-LIMIT} - I_{LOAD}) \times t_{ON}}{C_{OUT}}$$
$$+ R_{ESR,COUT} \times (I_{SKIP-LIMIT} - I_{LOAD})$$

$$V_{OUT-RIPPLE} = \left[\frac{L \times I_{SKIP-LIMIT}}{C_{OUT} \times (V_{IN} - V_{OUT})} + R_{ESR,COUT}\right] \times (I_{SKIP-LIMIT} - I_{LOAD})$$

To limit output ripple in skip mode, size C_{OUT} based on the above formula. All the above calculations are applicable only in skip mode.

Compensation Design Guidelines

The MAX15058 uses a fixed-frequency, peak-current-mode control scheme to provide easy compensation and fast transient response. The inductor peak current is monitored on a cycle-by-cycle basis and compared to the COMP voltage (output of the voltage error amplifier). The regulator's duty cycle is modulated based on the inductor's peak current value. This cycle-by-cycle control of the inductor current emulates a controlled current source. As a result, the inductor's pole frequency is shifted beyond the gain bandwidth of the regulator. System stability is provided with the addition of a simple series capacitor-resistor from COMP to GND. This pole-zero combination serves to tailor the desired response of the closed-loop system. The basic regulator loop consists of a power modulator (comprising the regulator's pulse-width modulator, current sense and slope compensation ramps, control circuitry, MOSFETs, and inductor), the capacitive output filter and load, an output feedback divider, and a voltage-loop error amplifier with its associated compensation circuitry. See Figure 1.

The average current through the inductor is expressed as:

$$\overline{I_L} = G_{MOD} \times \overline{V_{COMP}}$$

where $\overline{I_L}$ is the average inductor current and G_{MOD} is the power modulator's transconductance.

For a buck converter:

$$\overline{V_{OUT}} = R_{LOAD} \times \overline{I_L}$$

where R_{LOAD} is the equivalent load resistor value.

Combining the above two relationships, the power modulator's transfer function in terms of $\overline{V_{OUT}}$ with respect to $\overline{V_{COMP}}$ is:

$$\frac{\overline{V_{OUT}}}{\overline{V_{COMP}}} = \frac{R_{LOAD} \times \overline{I_L}}{\frac{\overline{I_L}}{G_{MOD}}} = R_{LOAD} \times G_{MOD}$$

The peak current-mode controller's modulator gain is attenuated by the equivalent divider ratio of the load resistance and the current-loop gain's impedance. G_{MOD} becomes

$$G_{MOD}(DC) = g_{MC} \times \frac{1}{\left\{1 + \frac{R_{LOAD}}{f_{SW} \times L} \times \left[K_S \times (1 - D) - 0.5\right]\right\}}$$

where R_{LOAD} = $V_{OUT/IOUT(MAX)}$, f_{SW} is the switching frequency, L is the output inductance, D is the duty cycle (V_{OUT}/V_{IN}), and K_S is a slope compensation factor calculated from the following equation:

$$K_S = 1 + \frac{S_{SLOPE}}{S_N} = 1 + \frac{V_{SLOPE} \times f_{SW} \times L \times g_{MC}}{(V_{IN} - V_{OUT})}$$

where:

$$S_{SLOPE} = \frac{V_{SLOPE}}{t_{SW}} = V_{SLOPE} \times f_{SW}$$

$$S_N = \frac{(V_{IN} - V_{OUT})}{L \times g_{MC}}$$

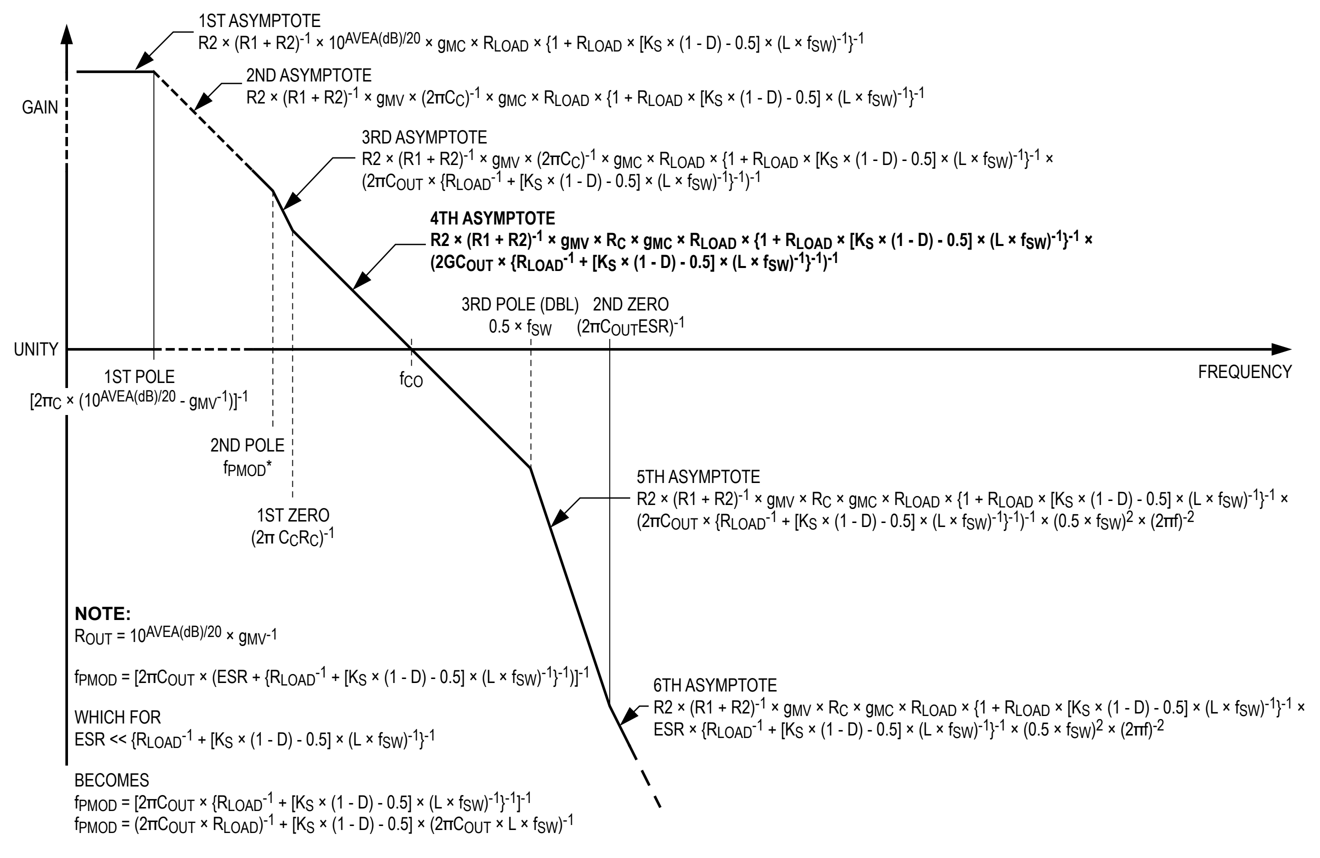


Figure 3. Asymptotic Loop Response of Current-Mode Regulator

As previously mentioned, the power modulator's dominant pole is a function of the parallel effects of the load resistance and the current-loop gain's equivalent impedance:

$$f_{PMOD} = \frac{1}{2\pi \times C_{OUT} \times \left[ESR + \left(\frac{1}{R_{LOAD}} + \frac{[K_S \times (1-D) - 0.5]}{f_{SW} \times L}\right)^{-1}\right]}$$

And knowing that the ESR is typically much smaller than the parallel combination of the load and the current loop:

$$ESR << \left(\frac{1}{R_{LOAD}} + \frac{[K_S \times (1-D) - 0.5]}{f_{SW} \times L}\right)^{-1}$$

$$f_{PMOD} \approx \frac{1}{2\pi \times C_{OUT} \times \left(\frac{1}{R_{LOAD}} + \frac{[K_S \times (1-D) - 0.5]}{f_{SW} \times L}\right)^{-1}}$$

which can be expressed as:

$$f_{PMOD} \approx \frac{1}{2\pi \times C_{OUT} \times R_{LOAD}} + \frac{[K_S \times (1-D) - 0.5]}{2\pi \times f_{SW} \times L \times C_{OUT}}$$

Note: Depending on the application's specifics, the amplitude of the slope compensation ramp could have a significant impact on the modulator's dominate pole. For low duty-cycle applications, it provides additional damping (phase lag) at/near the crossover frequency (see the *Closing the Loop: Designing the Compensation Circuitry* section). There is no equivalent effect on the power modulator zero, f_{ZMOD}.

$$f_{ZMOD} = f_{ZESR} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$

The effect of the inner current loop at higher frequencies is modeled as a double-pole (complex conjugate) frequency term, $G_{SAMPLING}(s)$, as shown:

$$G_{SAMPLING}(s) = \frac{1}{\frac{s^2}{(\pi \times f_{SW})^2} + \frac{s}{\pi \times f_{SW} \times Q_C} + 1}$$

where the sampling effect quality factor, Q_C, is:

$$Q_C = \frac{1}{\pi \times [K_S \times (1 - D) - 0.5]}$$

And the resonant frequency is:

$$\omega SAMPLING(s) = \pi \times f_{SW}$$

or:

$$f_{SAMPLING} = \frac{f_{SW}}{2}$$

Having defined the power modulator's transfer function, the total system transfer can be written as follows (see Figure 3):

$$Gain(s) = G_{FF}(s) \times G_{EA}(s) \times G_{MOD}(DC) \times G_{FILTER}(s) \times G_{SAMPLING}(s)$$

where:

$$G_{FF}(s) = \frac{R2}{R1 + R2} \times \frac{(sC_{FF}R1 + 1)}{[sC_{FF}(R1 \| R2) + 1]}$$

Leaving C_{FF} empty, $G_{FF}(s)$ becomes:

$$G_{FF}(s) = \frac{R2}{R1 + R2}$$

Also:

$$G_{EA}(s) = 10^{AVEA(dB)/20} \times \frac{(sC_C R_C + 1)}{\left[sC_C\left(R_C + \frac{10^{AVEA(dB)/20}}{g_{MV}}\right) + 1\right]}$$

which simplifies to:

$$G_{EA}(s) = 10^{AVEA(dB)/20} \times \frac{(sC_C R_C + 1)}{\left[sC_C\left(\frac{10^{AVEA(dB)/20}}{g_{MV}}\right) + 1\right]}$$

when $R_C << \frac{10^{AVEA(dB)/20}}{g_{MV}}$

$$G_{FILTER}(s) = R_{LOAD} \times \frac{(sC_{OUT}ESR + 1)}{\left(sC_{OUT}\left\{\frac{1}{R_{LOAD}} + \frac{[K_S \times (1 - D) - 0.5]}{f_{SW} \times L}\right\}^{-1} + 1\right)}$$

The dominant poles and zeros of the transfer loop gain are shown below:

$$f_{P1} = \frac{g_{MV}}{2\pi \times 10^{AVEA(dB)/20} \times C_C}$$

$$f_{P2} = \frac{1}{2\pi \times C_{OUT}\left\{\frac{1}{R_{LOAD}} + \frac{[K_S \times (1-D) - 0.5]}{f_{SW} \times L}\right\}^{-1}}$$

$$f_{P3} = \frac{1}{2}(f_{SW})$$

$$f_{Z1} = \frac{1}{2\pi \times C_C R_C}$$

$$f_{Z2} = \frac{1}{2\pi \times C_{OUT}ESR}$$

The order of pole-zero occurrence is:

$$f_{P1} < f_{P2} \le f_{Z1} < f_{CO} \le f_{P3} < f_{Z2}$$

Under heavy load, f_{P2}, approaches f_{Z1}. Figure 3 shows a graphical representation of the asymptotic system closed-loop response, including dominant pole and zero locations.

The loop response's fourth asymptote (in bold, Figure 3) is the one of interest in establishing the desired crossover frequency (and determining the compensation component values). A lower crossover frequency provides for stable closed-loop operation at the expense of a slower load- and line-transient response. Increasing the crossover frequency improves the transient response at the (potential) cost of system instability. A standard rule of thumb sets the crossover frequency between 1/10 and 1/5 of the switching frequency. First, select the passive power and decoupling components that meet the application's requirements. Then, choose the small-signal compensation components to achieve the desired closed-loop frequency response and phase margin as outlined in the *Closing the Loop: Designing the Compensation Circuitry* section.

Closing the Loop: Designing the Compensation Circuitry

1) Select the desired crossover frequency. Choose f_{CO} approximately 1/10 to 1/5 of the switching frequency (f_{SW}).
2) Determine R_C by setting the system transfer's fourth asymptote gain equal to unity (assuming $f_{CO} > f_{Z1}$, f_{P2}, and f_{P1}) where:

$$R_C = \frac{R1+R2}{R2} \times \frac{\left(1+\frac{R_{LOAD}K_S[(1-D)-0.5]}{L \times f_{SW}}\right)}{g_{MV} \times g_{MC} \times R_{LOAD}} \times 2\pi f_{CO} C_{OUT} \times \left[ESR + \frac{1}{\left(\frac{1}{R_{LOAD}} + \frac{K_S[(1-D)-0.5]}{L \times f_{SW}}\right)}\right]$$

and where the ESR is much smaller than the parallel combination of the equivalent load resistance and the current loop impedance, e.g.,:

$$ESR << \frac{1}{\left(\frac{1}{R_{LOAD}} + \frac{K_S[(1-D)-0.5]}{L \times f_{SW}}\right)}$$

R_C becomes:

$$R_C = \frac{R1+R2}{R2} \times \frac{2\pi f_{CO} \times C_{OUT}}{g_{MV} \times g_{MC}}$$

3) Determine C_C by selecting the desired first system zero, f_{Z1}, based on the desired phase margin. Typically, setting f_{Z1} below 1/5 of f_{CO} provides sufficient phase margin.

$$f_{Z1} = \frac{1}{2\pi \times C_C R_C} \le \frac{f_{CO}}{5}$$

therefore:

$$C_C \ge \frac{5}{2\pi \times f_{CO} \times R_C}$$

4) For low duty-cycle applications, the addition of a phase-leading capacitor (C_{FF} in Figure 1) helps mitigate the phase lag of the damped half-frequency double pole. Adding a second zero near to but below the desired crossover frequency increases both the closed-loop phase margin and the regulator's unity-gain bandwidth (crossover frequency). Select the capacitor as follows:

$$C_{FF} = \frac{1}{2\pi \times f_{CO} \times (R1 || R2)}$$

This guarantees the additional phase-leading zero occurs at a frequency lower than f_{CO} from:

$$f_{PHASE\_LEAD} = \frac{1}{2\pi \times C_{FF} \times R1}$$

Using C_{FF} the zero-pole order is adjusted as follows:

$$f_{P1} < f_{P2} \le f_{Z1} < \frac{1}{2\pi C_{FF} R1} < \frac{1}{2\pi C_{FF}(R1 || R2)} \approx f_{CO} < f_{P3} < f_{Z2}$$

Confirm the desired operation of C_{FF} empirically. The phase lead of C_{FF} diminishes as the output voltage is a smaller multiple of the reference voltage, e.g., below about 1V. Do not use C_{FF} when $V_{OUT} = V_{FB}$.

Setting the Soft-Start Time

The soft-start feature ramps up the output voltage slowly, reducing input inrush current during startup. Size the C_{SS} capacitor to achieve the desired soft-start time, t_{SS}, using:

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{FB}}$$

I_{SS}, the soft-start current, is 10µA (typ) and V_{FB}, the output feedback voltage threshold, is 0.6V (typ). When using large C_{OUT} capacitance values, the high-side current limit can trigger during the soft-start period. To ensure the correct soft-start time, t_{SS}, choose C_{SS} large enough to satisfy:

$$C_{SS} >> C_{OUT} \times \frac{V_{OUT} \times I_{SS}}{(I_{HSCL\_} - I_{OUT}) \times V_{FB}}$$

$I_{HSCL\_}$ is the typical high-side MOSFET current-limit value.

An external tracking reference with steady-state value between 0V and V_{IN} - 1.8V can be applied to SS/REFIN. In this case, connect an RC network from external tracking reference and SS/REFIN, as shown in Figure 4. The recommended value for R_{SS} is approximately 1kΩ. R_{SS} is needed to ensure that, during hiccup period, SS/REFIN can be internally pulled down.

When an external reference is connected to SS/REFIN, the soft-start must be provided externally.

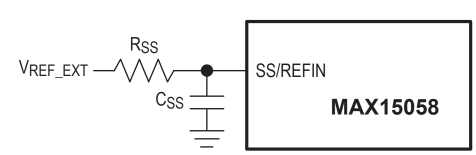


Figure 4. RC Network for External Reference at SS/REFIN

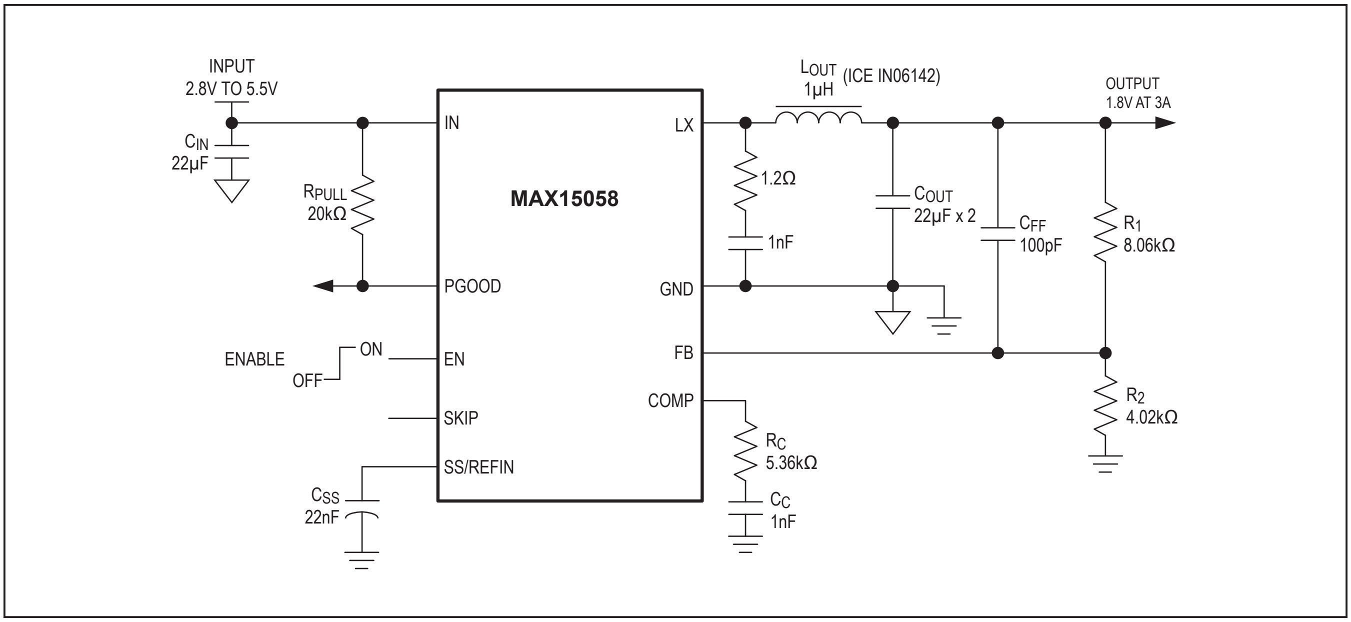


Figure 5. Application Circuit for PWM Mode Operation

Power Dissipation

The MAX15058 is available in a 9-bump WLP package and can dissipate up to 1127mW at T_A = +70°C. When the die temperature exceeds +150°C, the thermal-shutdown protection is activated (see the *Thermal-Shutdown Protection* section).

Layout Procedure

Careful PCB layout is critical to achieve clean and stable operation. It is highly recommended to duplicate the MAX15058 Evaluation Kit layout for optimum performance. If deviation is necessary, follow these guidelines for good PCB layout:

1) Connect the signal and ground planes at a single point immediately adjacent to the GND bump of the IC.
2) Place capacitors on IN and SS/REFIN as close as possible to the IC and the corresponding pad using direct traces.
3) Keep the high-current paths as short and wide as possible. Keep the path of switching current short and minimize the loop area formed by LX, the output capacitors, and the input capacitors.
4) Connect IN, LX, and GND separately to a large copper area to help cool the IC to further improve efficiency.
5) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close as possible to the IC.
6) Route high-speed switching nodes (such as LX) away from sensitive analog areas (such as FB and COMP).

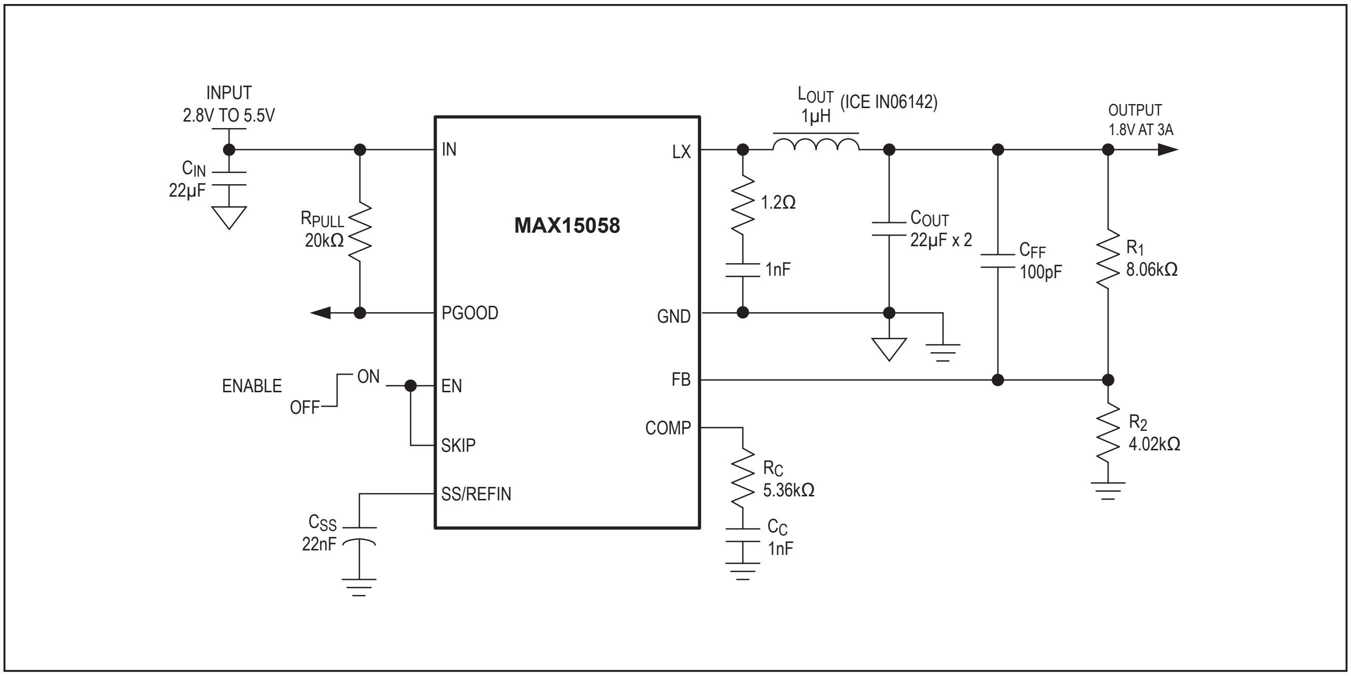


Figure 6. Application Circuit for Skip Mode Operation

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/10	Initial release	—
1	3/11	Revised *Package Information* section.	20
2	7/11	Changed the 1.65mm x 1.65mm, 9-bump package information to 1.5mm x 1.5mm, 9-bump package information. Inserted *Typical Operating Circuit* on page one.	1, 11

