MAX15492

Single-Phase Synchronous MOSFET Driver with Ultra-Low-Power Mode

General Description

The MAX15492 is a synchronous half-bridge driver with ultra-low-power mode. The device is intended to work with controller ICs such as the MAX15411, MAX15566/MAX15567, or MAX15576/MAX15577 in multiphase CPU core regulators. To provide the best light-load efficiency, the controller can place the device into an ultra-low power mode where the supply current is only 4µA.

The low-side driver is optimized to drive 3nF capacitive loads with 3ns/7ns typical fall/rise times, and the high-side driver with 7ns/14ns typical fall/rise times. Adaptive dead-time control prevents shoot-through currents and maximizes converter efficiency.

The MAX15492 is available in a small, 8-pin (2mm x 2mm) TDFN package with an exposed pad.

Applications

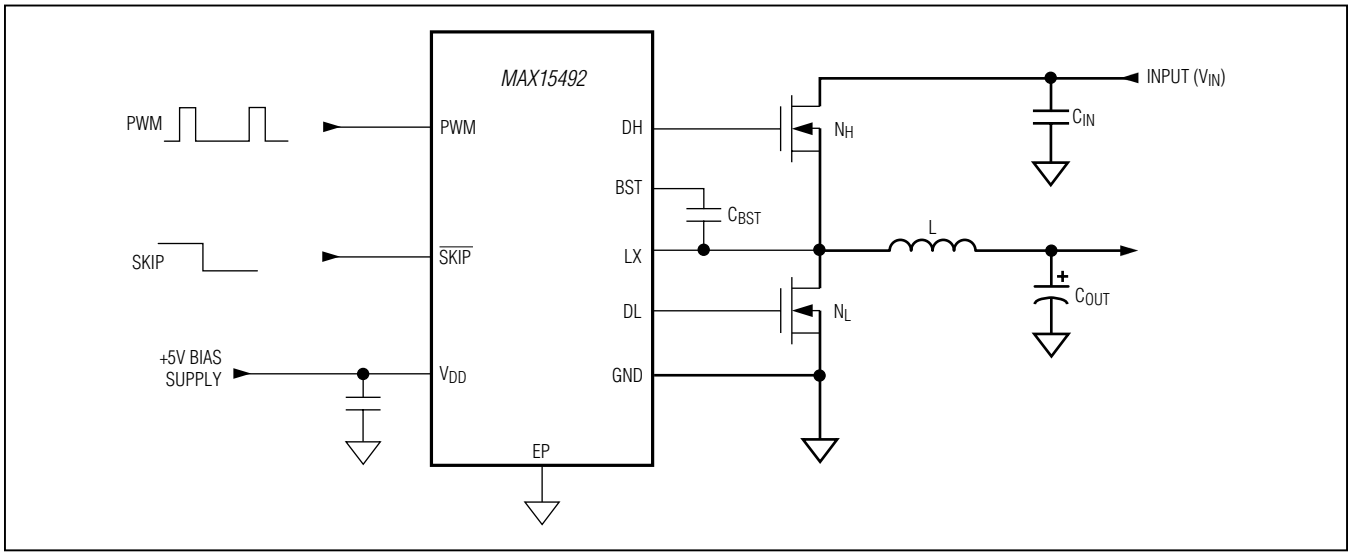
- Intel® Ultrabook™/Notebook Computers
- Tablet Computers
- Multiphase DC-DC Converters

Benefits and Features

- Extends Battery Life
  - Ultra-Low-Power Mode with 4µA Supply Current
  - 2V to 24V Input Voltage Range
  - Selectable Pulse-Skipping Mode
  - 7ns Minimum Guaranteed Dead-Time
- Allows Operation Up to 3MHz per Phase
  - 0.7Ω Low-Side On-Resistance
  - 1.5Ω High-Side On-Resistance
  - 12ns Propagation Delay
  - 4.2V to 5.5V Bias Supply Range (MAX15492)
  - 3V to 5.5V Bias Supply Range (MAX15492B)
- Integrated Boost Switch Saves Space and Cost

***Ordering Information* appears at end of data sheet.**

Typical Operating Circuit



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Absolute Maximum Ratings

V_{DD} to GND .....-0.3V to +6V
SKIP to GND .....-0.3V to (V_{DD} + 0.3V)
PWM to GND.....-0.3V to (V_{DD} + 0.3V)
DL to GND (Note 1).....-0.3V to (V_{DD} + 0.3V)
BST to GND (Note 1) .....-0.3V to +30V
DH to LX (Note 1).....-0.3V to (V_{BST} + 0.3V)
BST to V_{DD} .....-0.3V to +24V
BST to LX (Note 1).....-0.3V to +6V

Continuous Power Dissipation
8-Pin, 2mm x 2mm TDFN (T822)
(derate 11.9mW/°C above +70°C) 953mW
Operating Temperature Range..... -40°C to +105°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{DD} = $V_{\overline{SKIP}}$ = 5.0V, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} Input Voltage Range	V_{DD}	MAX15492		4.2		5.5	V
		MAX15492B		3		5.5	
V_{DD} Undervoltage-Lockout Threshold	V_{UVLO}	Rising edge, PWM disabled below this level	MAX15492		3.7	4.1	V
			MAX15492B		2.8	2.95	
		Falling edge, PWM disabled below this level	MAX15492	3.2	3.5	3.75	
			MAX15492B	2.5	2.65	2.78	
Quiescent Supply Current (V_{DD})	I_{DD}	$\overline{SKIP}$ = high-Z, after $t_{SULP-DLY}$ delay			4	10	µA
		$\overline{SKIP}$ = V_{DD}, PWM = high-Z after the shutdown hold time has expired			80	200	
		$\overline{SKIP}$ = GND, PWM = GND, LX = GND (after zero crossing)			150	300	
		$\overline{SKIP}$ = GND or V_{DD}, PWM = V_{DD}, V_{BST} = 5V			350	700	
DRIVERS							
PWM Pulse Width	$t_{ON(MIN)}$	Minimum on-time (Note 3)			30		ns
	$t_{OFF(MIN)}$	Minimum off-time. Required to allow the zero-crossing comparator time to settle to the proper state.			220		
DL Propagation Delay	t_{PWM-DL}	PWM high to DL low			12		ns
DH Propagation Delay	t_{PWM-DH}	PWM low to DH low			12		ns
DL-to-DH Dead Time	t_{DL-DH}	DL falling to DH rising	T_A = 0°C to +85°C	8	12		ns
			T_A = -40°C to +105°C	7			
DH-to-DL Dead Time	t_{DH-DL}	DH falling to DL rising	T_A = 0°C to +85°C	8	12		ns
			T_A = -40°C to +105°C	7			
DL Transition Time	t_{F-DL}	Falling, 3nF load			3		ns
		Rising, 3nF load			7		

Electrical Characteristics (continued)

(V_{DD} = $V_{\overline{SKIP}}$ = 5.0V, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DH Transition Time	t_{F-DH}	Falling, 3nF load		7		ns
		Rising, 3nF load		14		
DH Driver On-Resistance	$R_{ON(DH)}$	DH high state (pullup), BST = LX forced to 5V		1.5	3.5	Ω
		DH low state (pulldown), BST = LX forced to 5V		0.7	2.0	
DL Driver On-Resistance	$R_{ON(DL)}$	DL high state (pullup)		0.7	2.0	Ω
		DL low state (pulldown)		0.3	0.9	
DH Driver Source Current				2.2		A
DH Driver Sink Current				2.7		A
DL Driver Source Current				2.7		A
DL Driver Sink Current				8		A
Zero-Crossing Current Threshold	V_{ZX}	GND - LX, $\overline{SKIP}$ = GND		1.5		mV
Boost On-Resistance	$R_{ON(BST)}$	V_{DD} = 5V, PWM = GND, DH = LX = GND (pulldown state), I_{BST} = 10mA		6	12	Ω
LOGIC INPUTS						
PWM Input Logic Levels		High	V_{DD} - 0.4			V
		Midlevel		V_{DD}/2		
		Low			0.4	
$\overline{SKIP}$ Input Logic Levels		High	V_{DD} - 0.4			V
		Midlevel		V_{DD}/2		
		Low			0.4	
PWM Input Current	I_{PWM}	Sink (PWM is forced to V_{DD})	-400	-200	-120	µA
		Source (PWM forced to GND)	120	200	400	
$\overline{SKIP}$ Input Current	$I_{\overline{SKIP}}$	Sink ($\overline{SKIP}$ is forced to V_{DD})	-130	-70	-35	µA
		Source ($\overline{SKIP}$ is forced to GND)	15	30	60	
Midlevel Standby Hold Time	t_{MID}	After PWM = high-Z, $\overline{SKIP}$ = high or low	80	160	300	ns
Ultra-Low-Power Delay Time	$t_{SULP-DLY}$	After $\overline{SKIP}$ = high-Z			2	µs
Ultra-Low-Power Wakeup Delay Time	$t_{WULP-DLY}$	After $\overline{SKIP}$ = low and PWM = high or low		12.5	25	µs
Thermal-Shutdown Threshold	T_{SHDN}	Hysteresis = +20°C		+160		°C

Note 1: Self-protected against transient voltages exceeding these limits for ≤ 59ns under normal operation and loads up to the maximum rated output current.

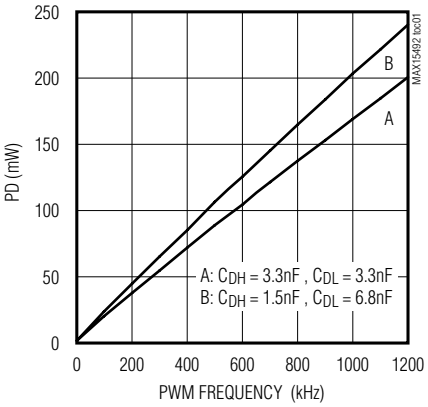
Note 2: Limits are 100% production tested at T_A = +25°C. Maximum and minimum limits over temperature are guaranteed through correlation using statistical quality control (SQC) methods.

Note 3: The minimum on-time is provided for design guidance. This determines the maximum switching the system can operate with, so this time should be as fast as possible. The primary requirement here is that short PWM pulses must NOT result in shoot-through currents.

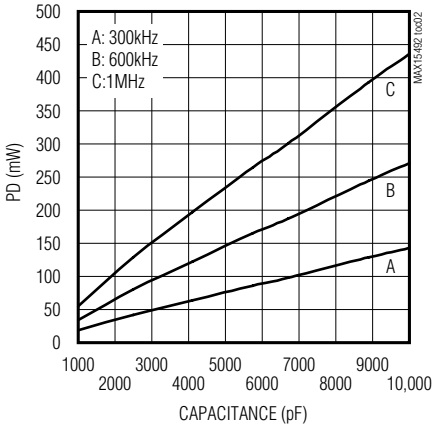
Typical Operating Characteristics

(Circuit of Figure 1, V_{DD} = 5V, C_{DH} = 3nF, C_{DL} = 3nF, T_A = +25°C, unless otherwise noted.)

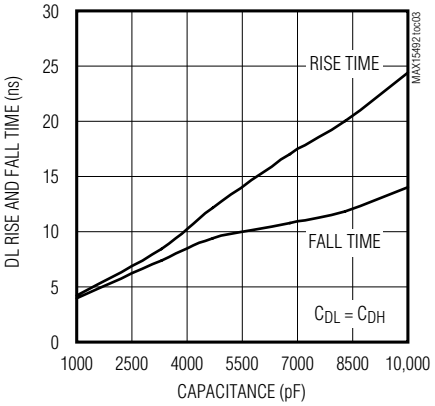
PACKAGE POWER DISSIPATION vs. PWM FREQUENCY



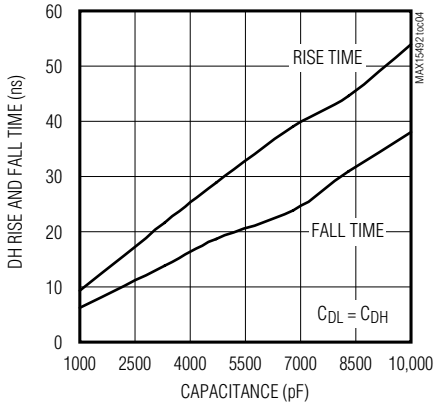
PACKAGE POWER DISSIPATION vs. CAPACITIVE LOAD ON DH AND DL



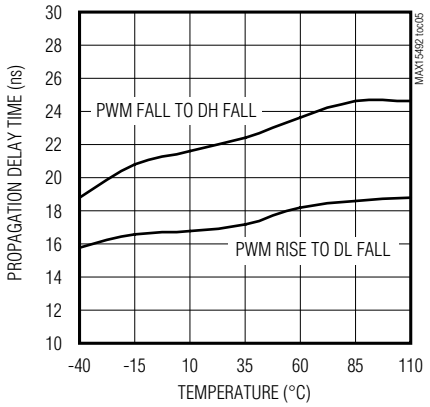
DL RISE AND FALL TIME vs. CAPACITIVE LOAD



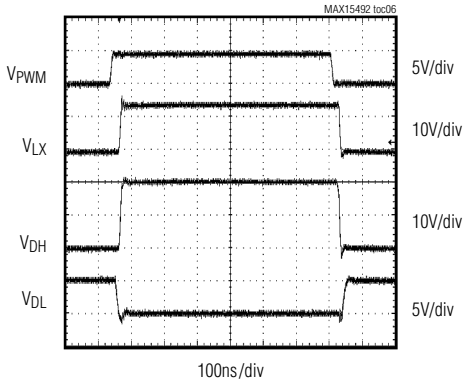
DH RISE AND FALL TIME vs. CAPACITIVE LOAD



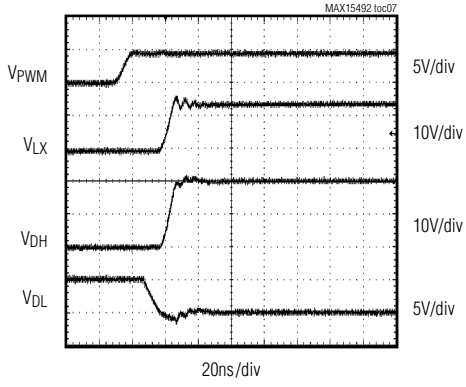
PROPAGATION DELAY TIME vs. TEMPERATURE



TYPICAL APPLICATION CIRCUIT SWITCHING WAVEFORM



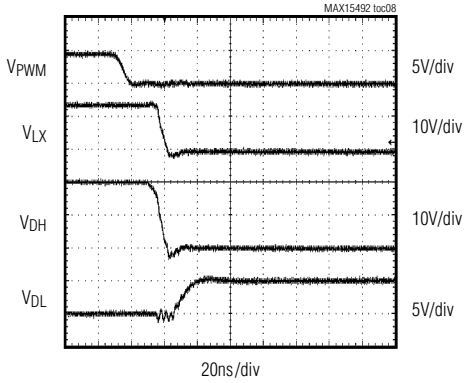
DH RISE AND DL FALL WAVEFORM



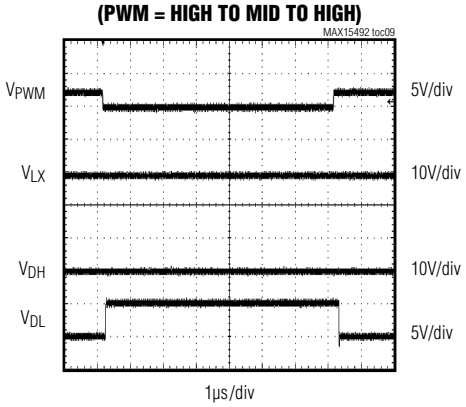
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{DD} = 5V, C_{DH} = 3nF, C_{DL} = 3nF, T_A = +25°C, unless otherwise noted.)

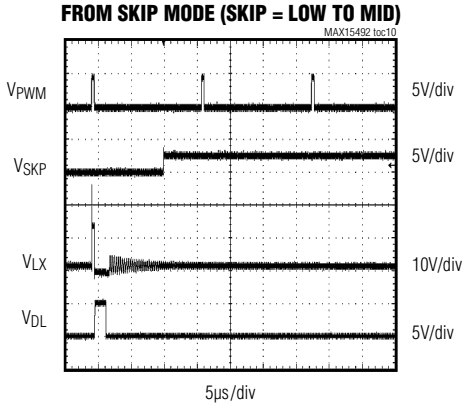
DH FALL AND DL RISE WAVEFORM



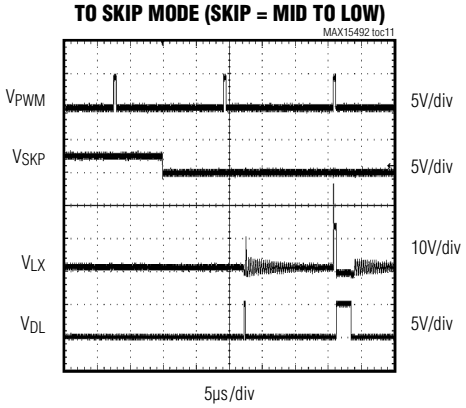
SWITCHING WAVEFORM (PWM = HIGH TO MID TO HIGH)



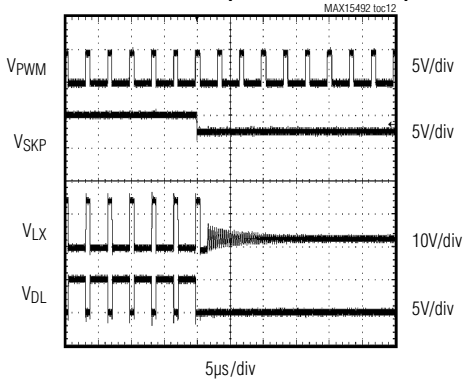
ENTERING ULTRA-LOW-POWER MODE FROM SKIP MODE (SKIP = LOW TO MID)



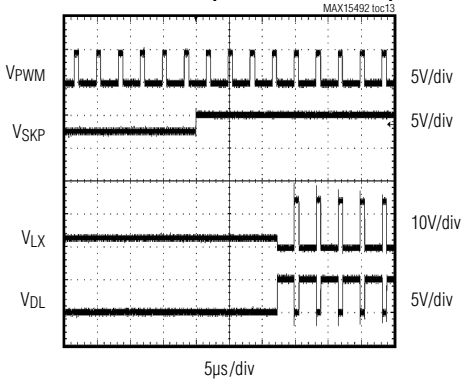
EXITING ULTRA-LOW-POWER MODE TO SKIP MODE (SKIP = MID TO LOW)



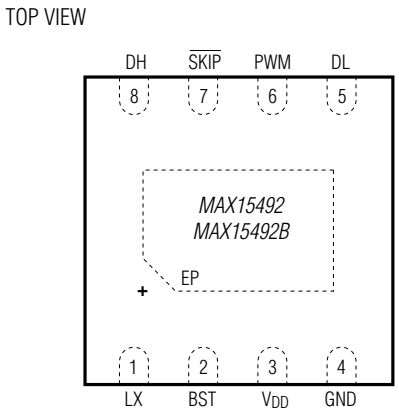
ENTERING ULTRA-LOW-POWER MODE FROM FPWM MODE (SKIP = HIGH TO MID)



EXITING ULTRA-LOW-POWER MODE TO FPWM MODE (SKIP = MID TO HIGH)



Pin Configuration



TDFN
(2mm x 2mm)

Pin Description

PIN	NAME	FUNCTION
1	LX	Switching Node and Inductor Connection. LX provides the lower supply rail for the DH high-side gate driver, and connects to the skip-mode zero-crossing comparator.
2	BST	Boost Flying-Capacitor Connection. Gate-drive power supply for the DH high-side gate driver. Connect a 0.1µF or 0.22µF capacitor between BST and LX. An optional resistor in series with BST allows the DH pullup impedance to be adjusted.
3	V_{DD}	Supply Voltage. For the MAX15492, connect to a 4.2V to 5.5V supply rail; for the MAX15492B, connect to a 3V to 5.5V supply rail. Bypass V_{DD} to power ground with a local 1µF or greater ceramic capacitor.
4	GND	Analog and Driver Ground
5	DL	Low-Side n-Channel MOSFET Gate-Driver Output. Swings between GND and V_{DD}.
6	PWM	PWM (Driver Control) Input. Noninverting driver control input from the controller IC. PWM Logic-High: DH = BST (high), DL = GND (low) PWM Midlevel: After the midlevel hold time expires, the controller enters high-impedance mode. DH = LX (low) and DL = GND (low), so LX goes high-Z. PWM Logic-Low: DH = LX (low), DL = V_{DD} (high) Internal pullup and pulldown resistors create the midlevel and prevent the controller from triggering an on-time if this input is left unconnected (not soldered properly) or driven by a high impedance.
7	$\overline{SKIP}$	Pulse Skipping/Standby Control Input. $\overline{SKIP}$ Logic-High: Forced-PWM operation (FPWM mode) $\overline{SKIP}$ Midlevel: After the ultra-low-power delay time expires, the controller enters ultra-low-power standby mode. $\overline{SKIP}$ Logic-Low: Pulse-skipping operation (skip mode) Internal pullup and pulldown resistors create the midlevel and prevent the controller from triggering an on-time if this input is left unconnected (not soldered properly) or driven by a high impedance.
8	DH	High-Side n-Channel MOSFET Gate-Driver Output. Swings between LX and BST.
—	EP	Exposed Pad. Connect to ground through multiple vias to reduce the thermal impedance.

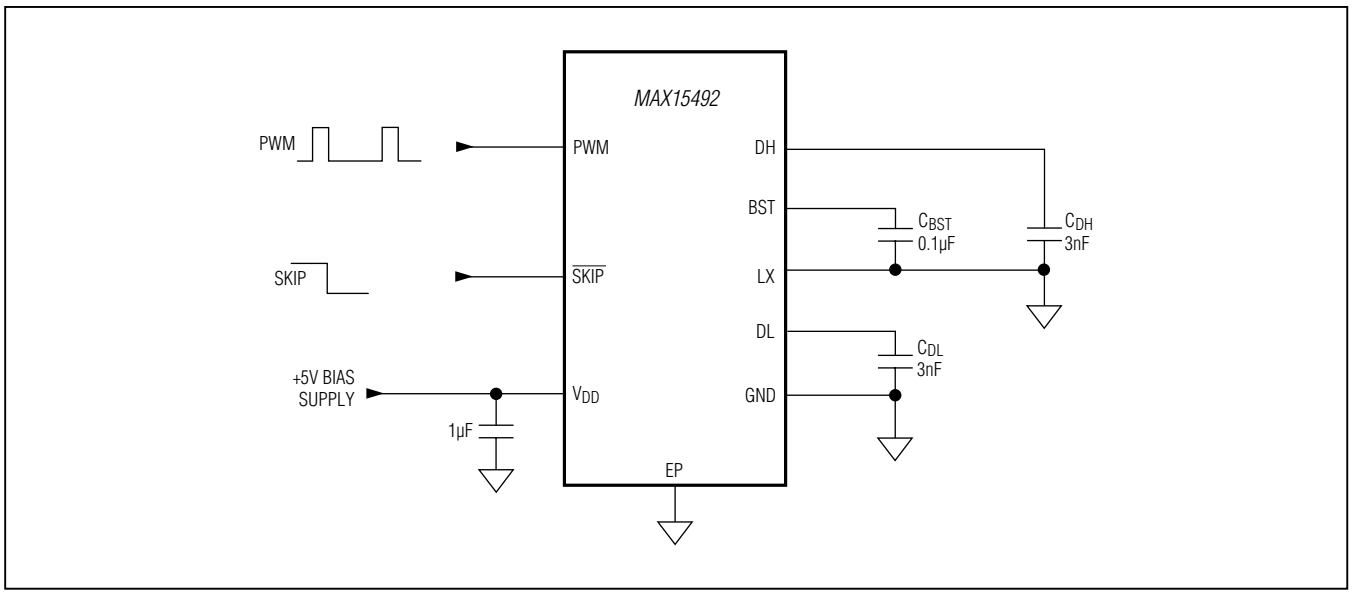


Figure 1. Test Circuit

Detailed Description

The MAX15492 is a synchronous half-bridge driver with ultra-low-power mode. The device is intended to work with controllers such as the MAX15566/MAX15567 or MAX15576/MAX15577, to provide flexible multiphase CPU core-voltage supplies. The low driver resistance allows up to 8A output peak current. Each MOSFET driver in the device can drive 3nF capacitive loads with only 12ns propagation delay and 3ns/7ns (typ) fall/rise times for the low-side driver and the high-side driver with 7ns/14ns (typ) fall/rise times, allowing operation up to 3MHz per phase. Larger capacitive loads are allowable but result in longer propagation and transition times. Adaptive dead-time control prevents shoot-through currents and maximizes converter efficiency while allowing operation with a variety of MOSFETs and PWM controllers. An input undervoltage-lockout (UVLO) circuit allows proper power-on sequencing.

PWM Input

The drivers for the device are disabled (DH and DL pulled low) if the PWM input remains in the midlevel window for at least 160ns (typ). Once the PWM signal is driven high or low, the device immediately exits the low-current shutdown state and resumes active operation. Outside the shutdown state, the drivers are enabled based on the rising and falling thresholds specified in the *Electrical Characteristics*.

Ultra-Low-Power Mode

The MAX15492 is a similar product to the MAX17491. The main difference is that the MAX17491 $\overline{SKIP}$ pin is a 2-level input. In the MAX15492, the $\overline{SKIP}$ pin is a 3-level pin, similar to the PWM pin. The high-impedance level (midlevel) on $\overline{SKIP}$ forces the part into ultra-low consumption (4µA typ) mode after a 500ns delay and produces DL and DH both low. If left unconnected, $\overline{SKIP}$ is connected to the midlevel.

MOSFET Gate Drivers (DH, DL)

The high-side driver (DH) has 1.5Ω sourcing resistance and 0.7Ω sinking resistance, resulting in 2.2A peak sourcing current and 2.7A peak sinking current with a 5V supply voltage. The low-side driver (DL) has a typical 0.7Ω sourcing resistance and 0.3Ω sinking resistance, yielding 2.7A peak sourcing current and 8A peak sinking current. This reduces switching losses, making the device ideal for both high-frequency and high-output-current applications.

Table 1. State Table

OPERATION	$\overline{SKIP}$	PWM	DH	DL	COMMENTS
V_{DD} UVLO	X	X	Low (Off)	Low (Off)	Part restarts on UVLO rising and LX goes high-Z on UVLO falling.
Thermal shutdown	X	X	Low (Off)	Low (Off)	Thermal shutdown; reset by 20°C hysteresis. When thermal is triggered, the device's LX goes high-Z.
Forced-PWM mode	H	H/L	On/Off	Off/On	Full-power operation.
Skip mode	Low	H/L	On/Off	Off/On, then ZX	Light-load operation.
Phase disabled	H/L	High-Z	Low (Off)	Low (Off)	Phase disabled.
Ultra-low-power mode	High-Z	X	Low (Off)	Low (Off)	Lowest-power operating state (system in standby).
Wake-up (exit)	High-Z to H/L	X	On/Off	Off/On	Wake-up from ultra-low power.

X= Don't care, H = high, L = low, H/L = high or low, and ZX = zero crossing.

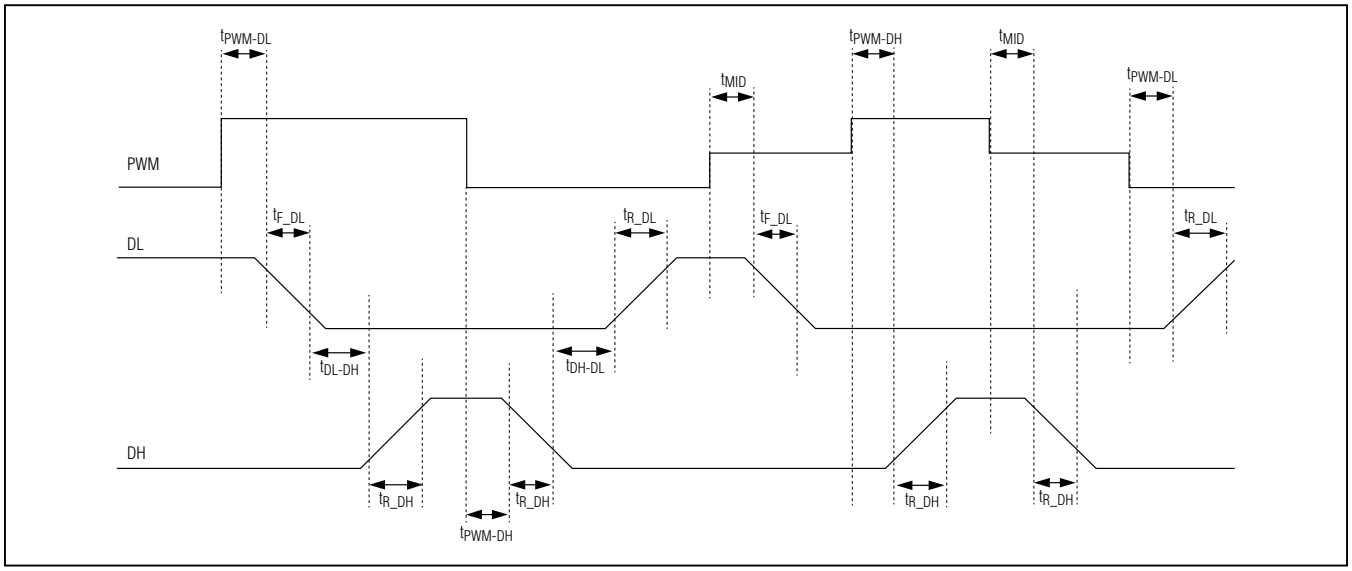


Figure 2. Timing Diagram

Table 2. Typical Components

DESIGNATION	QTY	COMPONENT SUPPLIERS
N_H	1 per phase	Siliconix Si4860DY
N_L	1 to 2 per phase	Siliconix Si4336DY
BST capacitor (C_{BST})	1 per phase	0.1µF or 0.22µF ceramic capacitor
Inductor (L)	1 per phase	0.36µH, 26A, 0.9mΩ power inductor
Output capacitors (C_{OUT})	1 to 2 per phase	330µF, 6mΩ per phase
Input capacitors (C_{IN})	1 to 2 per phase	10µF, 25V X5R ceramic capacitors

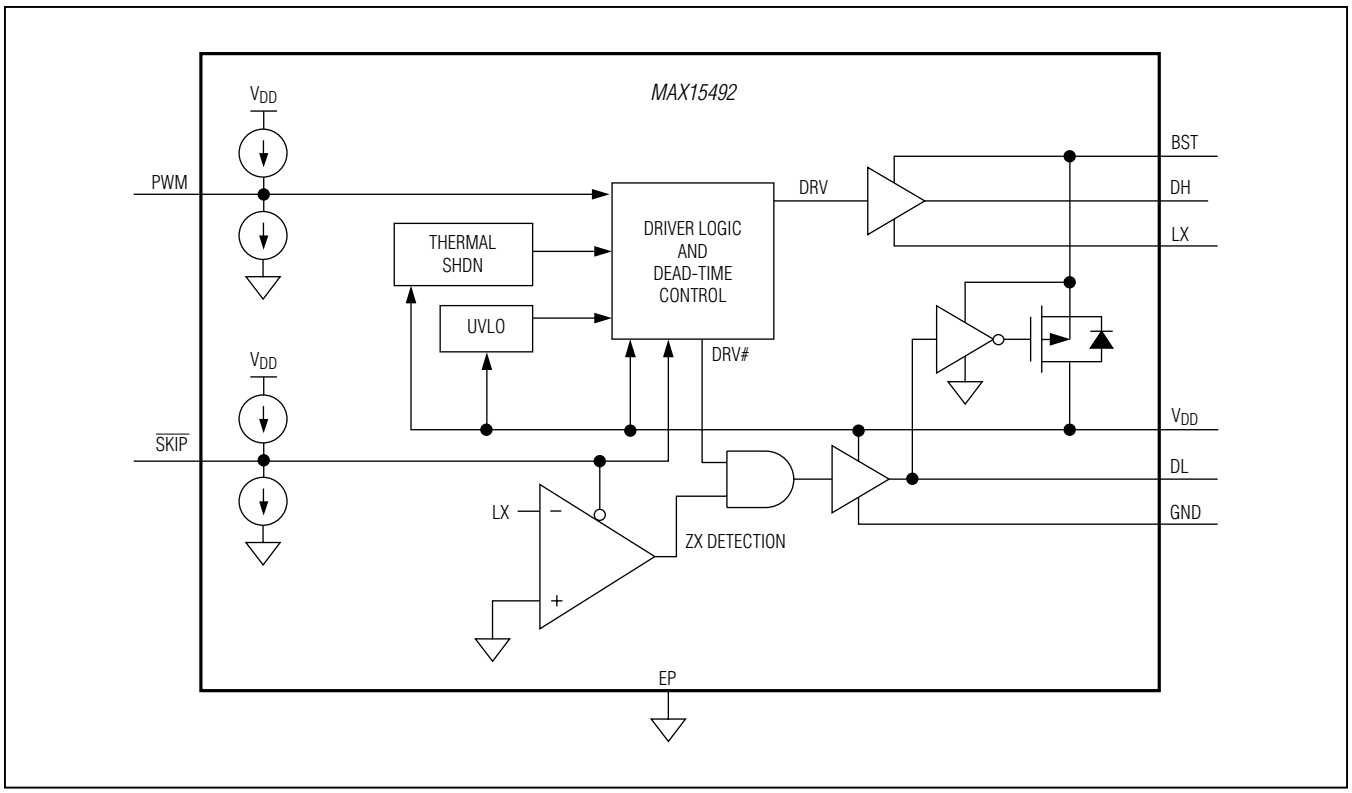


Figure 3. Overview Block Diagram

Adaptive Shoot-Through Protection

The DH and DL drivers are optimized for driving moderately sized high-side and larger low-side power MOSFETs. This is consistent with the low duty factor seen in the notebook CPU environment, where a large V_{IN} - V_{OUT} differential exists. Two adaptive dead-time circuits monitor the DH and DL outputs and prevent the opposite-side FET from turning on until the other is fully off. The device constantly monitors the low-side driver output (DL) voltage, and only allows the high-side driver to turn on when DL drops below the adaptive threshold. Similarly, the controller monitors the high-side driver output (DH) and prevents the low side from turning on until DH falls below the adaptive threshold before allowing DL to turn on.

The adaptive driver dead-time allows operation without shoot-through with a wide range of MOSFETs, minimizing delays and maintaining efficiency. There must be a low-resistance, low-inductance path from the DL and DH drivers to the MOSFET gates for the adaptive dead-time circuits to work properly; otherwise, the sense circuitry in the device interprets the MOSFET gates as off while charge actually remains on. Use very short and wide traces (e.g., 50 mils to 100 mils wide if the MOSFET is 1in from the driver).

Internal Boost Switch

The device uses a bootstrap circuit to generate the necessary drive voltage to fully enhance the high-side n-channel MOSFET. The internal p-channel MOSFET creates an ideal diode providing a low-voltage drop between V_{DD} and BST.

The selected high-side MOSFET determines the appropriate boost capacitance values (C_{BST} in the *Typical Application Circuit*, Figure 1), according to the following equation:

$$C_{BST} = Q_{GATE}/\Delta V_{BST}$$

where Q_{GATE} is the total gate charge of the high-side MOSFET and ΔV_{BST} is the voltage variation allowed on the high-side MOSFET driver. Choose ΔV_{BST} = 0.1V to 0.2V when determining C_{BST}. The boost flying capacitor should be a low-equivalent series-resistance (ESR) ceramic capacitor.

5V Bias Supply (V_{DD})

V_{DD} provides the supply voltage for the internal logic and driver circuits. Bypass V_{DD} with a 1µF or larger ceramic capacitor to GND to limit noise to the internal circuitry. Connect these bypass capacitors as close as possible to the device.

Input Undervoltage Lockout (UVLO)

When V_{DD} is below the UVLO threshold, DH and DL are held low. Once V_{DD} is above the UVLO threshold, and while PWM is low, DL is driven high and DH is driven low. This prevents the output of the converter from rising before a valid PWM signal is applied.

Low-Power Pulse Skipping

The device enters into low-power, pulse-skipping mode when $\overline{SKIP}$ is pulled low. In skip mode, an inherent automatic switchover to pulse-frequency modulation (PFM) takes place at light loads. A zero-crossing comparator truncates the low-side switch on-time at the inductor current's zero crossing. The comparator senses the voltage across LX and GND. Once V_{LX} - V_{GND} drops below the zero-crossing comparator threshold (see the *Electrical Characteristics* section), the comparator forces DL low. This mechanism causes the threshold between pulse-skipping PFM and nonskipping-PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation. The PFM/PWM crossover occurs when the load current of each phase is equal to 1/2 the peak-to-peak ripple current, which is a function of the inductor value. For a 7V to 20V battery input range, this threshold is relatively constant, with only a minor dependence on the input voltage due to the typically low duty cycles. The switching waveforms can appear noisy and asynchronous when light loading activates the pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency.

Applications Information

Power-MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability when using high-voltage (> 20V) AC adapters. Low-current applications usually require less attention. The high-side MOSFET (N_H) must be able to dissipate the resistive losses plus the switching losses at both $V_{IN(MIN)}$ and $V_{IN(MAX)}$. Calculate both these sums. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to losses at $V_{IN(MAX)}$, with lower losses in between. If the losses at $V_{IN(MIN)}$ are significantly higher than the losses at $V_{IN(MAX)}$, consider increasing the size of N_H (reducing $R_{DS(ON)}$ but increasing C_{GATE}). Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher than the losses at $V_{IN(MIN)}$, consider reducing the size of N_H (increasing $R_{DS(ON)}$ but reducing C_{GATE}). If V_{IN} does not vary over a wide range, the minimum power dissipation occurs where the resistive losses equal the switching losses. Choose a low-side MOSFET that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (e.g., one or two 8-pin SO8, DPAK, or D2PAK), and is reasonably priced. Ensure that the DL gate driver can supply sufficient source and sink current to support the gate charge and the current injected into the parasitic gate-to-drain capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems can occur.

MOSFET Power Dissipation

Worst-case conduction losses occur at the duty-factor extremes. For the high-side MOSFET (N_H), the worst-case power dissipation due to resistance occurs at the minimum input voltage:

$$PD(N_H RESISTIVE) = \left(\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{I_{LOAD}}{\eta_{TOTAL}}\right)^2 R_{DS(ON)}$$

where η_{TOTAL} is the total number of phases. Generally, a small high-side MOSFET is desired to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package-power dissipation often limits how small the MOSFETs can be. Again, the optimum occurs when the switching losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses do not usually become an issue until the input is greater than approximately 15V.

Calculating the power dissipation in high-side MOSFETs (N_H) due to switching losses is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PCB layout characteristics.

The following switching-loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on N_H:

$$PD(N_H SWITCHING) = \left(\frac{V_{IN(MAX)} I_{LOAD} f_{SW}}{\eta_{TOTAL}}\right)\left(\frac{Q_{G(SW)}}{I_{GATE}}\right) + \frac{C_{OSS} V_{IN}^2 f_{SW}}{2}$$

where C_{OSS} is the N_H MOSFET's output capacitance, $Q_{G(SW)}$ is the charge needed to turn on the high-side MOSFET, and I_{GATE} is the peak gate-drive source/sink current (2.2A/2.7A typ).

Switching losses in the high-side MOSFET can become an insidious heat problem when maximum AC adapter voltages are applied due to the squared term in the switching-loss equation above. If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low battery voltages becomes extraordinarily hot when biased from $V_{IN(MAX)}$, consider choosing another MOSFET with lower parasitic capacitance.

For the low-side MOSFET (N_L), the worst-case power dissipation always occurs at the maximum input voltage:

$$PD(N_L RESISTIVE) = \left[1 - \left(\frac{V_{OUT}}{V_{IN(MAX)}}\right)\right]\left(\frac{I_{LOAD}}{\eta_{TOTAL}}\right)^2 R_{DS(ON)}$$

The worst case for MOSFET power dissipation occurs under heavy load conditions that are greater than $I_{LOAD(MAX)}$, but are not quite high enough to exceed the current limit and cause the fault latch to trip. The MOSFETs must have a good-sized heatsink to handle the overload power dissipation. The heat sink can be a large copper field on the PCB or an externally mounted device.

An optional Schottky diode only conducts during the dead-time when both the high-side and low-side MOSFETs are off. Choose a Schottky diode with a forward voltage low enough to prevent the low-side MOSFET body diode from turning on during the dead-time, and a peak current rating higher than the peak inductor current. The Schottky diode must be rated to handle the average power dissipation per switching cycle. This diode is optional and can be removed if efficiency is not critical.

Power Dissipation and Thermal Considerations

Power dissipation in the IC package comes mainly from driving the MOSFETs. Therefore, it is a function of both switching frequency and the total gate charge of the selected MOSFETs. The total power dissipation when both drivers are switching is given by:

$$PD(IC) = I_{BIAS} \times 5V$$

where I_{BIAS} is the bias current of the 5V supply calculated in the *5V Bias Supply (V_{DD})* section. The rise in die temperature due to self-heating is given by the following formula:

$$\Delta T_J = \theta_{JA} \times PD(IC)$$

where PD(IC) is the power dissipated by the device, and θ_{JA} is the package's thermal resistance. The typical thermal resistance is θ_{JA} = 83.9°C/W for the 2mm x 2mm TDFN package.

Avoiding dV/dt Turning on the Low-Side MOSFET

At high input voltages, fast turn-on of the high-side MOSFET can momentarily turn on the low-side MOSFET due to the high dV/dt appearing at the drain of the low-side MOSFET. The high dV/dt causes a current flow through the Miller capacitance (C_{RSS}) and the input capacitance (C_{ISS}) of the low-side MOSFET. Improper selection of the low-side MOSFET that results in a high ratio of C_{RSS}/C_{ISS} makes the problem more severe. To avoid this problem, minimize the ratio of C_{RSS}/C_{ISS} when selecting the low-side MOSFET. Adding a 1Ω to 4.7Ω resistor between BST and C_{BST} can slow the high-side MOSFET turn-on. Similarly, adding a small capacitor from the gate to the source of the high-side MOSFET has the same effect. However, both methods work at the expense of increased switching losses.

Layout Guidelines

The device's MOSFET driver sources and sinks large currents to drive MOSFETs at high switching speeds. The high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following PCB layout guidelines are recommended when designing with the MAX15492:

1) Place all decoupling capacitors as close as possible to their respective IC pins.
2) Minimize the length of the high-current loop from the input capacitor, the upper switching MOSFET, and the low-side MOSFET back to the input-capacitor negative terminal.
3) Provide enough copper area at and around the switching MOSFETs and inductors to aid in thermal dissipation.
4) Connect the GND of the device as close as possible to the source of the low-side MOSFETs.
5) Keep LX away from sensitive analog components and nodes. Place the device and the analog components on the opposite side of the board from the power-switching node if possible.

A sample layout is available in the MAX15492 evaluation kit.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX15492GTA+	-40°C to +105°C	8 TDFN-EP*
MAX15492GTA/V+	-40°C to +105°C	8 TDFN-EP*
MAX15492BGTA+	-40°C to +105°C	8 TDFN-EP*
MAX15492BGTA/V+	-40°C to +105°C	8 TDFN-EP*

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

8 TDFN-EP

Package Code	**T822+1**
Outline Number	**21-0168**
Land Pattern Number	**90-0064**
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	83.9°C/W
Junction to Case (θ_{JC})	10.8°C/W

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/12	Initial release	—
1	9/14	Added /V OPN to *Ordering Information* table	13
2	2/15	Updated *Benefits and Features* section	1
3	3/15	Added note to Absolute Maximum Ratings section, placed at end of *Electrical Characteristics* table	2, 3
4	5/16	Updated *Ordering Information* table to remove future part designation	12
5	9/16	Added MAX15492B to *Benefits and Features*, *Electrical Characteristics*, *Pin Configuration*, *Pin Description*, *and Ordering Information*	1, 2, 6, 12
6	4/20	Added thermal resistance to *Package Information*	12

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