MAX15569

2-Phase/1-Phase QuickTune-PWM Controller with Serial I²C Interface

General Description

The MAX15569 step-down controller consists of one multiphase regulator. The multiphase CPU regulator uses Maxim's unique 2-phase QuickTune-PWM constant "on-time" architecture. The 2-phase CPU regulator runs 180° out-of-phase for true interleaved operation, minimizing input capacitance.

The device's VR is controlled by writing appropriate data into a function-mapped register file. Output voltages are dynamically changed through a 2-wire, fast I²C interface (clock, data), allowing the switching regulator to be programmed to different voltages. A slew-rate controller allows controlled voltage transition and controlled soft-start. The regulator runs in a unique smart, low-power pulse-skipping-state algorithm for best efficiency over the full load range and the best transient response with respect to common pulse-skipping methods.

The device includes multiple fault-protection features: Output overvoltage protection (OVP), undervoltage protection (UVP), and thermal protection. When any of these fault-protection features detect a fault condition, the controller shuts down. A multifunction $\overline{INT}$ output monitors output voltage, overcurrent (OC), overrange (VOUTMAX), and thermal faults ($\overline{VRHOT}$).

The controller has a programmable switching frequency, allowing 300kHz to 1400kHz per each phase of operation. The controller operates with a wide variety of drivers and MOSFETs, such as the MAX15492 MOSFET driver with standard MOSFETs, or with the power stage that integrates the drivers and MOSFETs together in a single device.

Applications

- ARM Core Power Supply
- Ultrabook™ and Tablet Core Supplies
- Voltage-Positioned Step-Down Converter
- Multiphase DC-DC Controllers

Benefits and Features

- Multiphase Controller Maximizes Processor Performance
  - 2-Phase QuickTune-PWM CPU Core Regulator
  - Output-Voltage Control
  - Active Load-Line Amplifier with Adjustable Gain
  - ±5mV FB Accuracy Over Line and Load
  - Programmable Slew Rate and Soft-Start
  - Accurate Current Balance and Current Limit
  - True Differential Remote Output Sense
  - 8-Bit ADC Digitizes Current Sense to Store in Current Monitor Register
- Transient Phase Overlap Reduces Output Capacitance
- Programmable Functionality Allows Optimized Design Performance
  - Programmable 300kHz to 1400kHz Switching Frequency
  - Programmable Soft-Shutdown (2kΩ Discharge Switch)
  - I²C Serial-Interface Control
- Robust Protection for Reliable Operation
  - Overcurrent, Output-Voltage Overrange, Overvoltage, Undervoltage, and Thermal-Fault Protection
  - System Status Register
  - Multifunction $\overline{INT}$ Output
  - 4.5V to 24V Battery Input Range

***Ordering Information* appears at end of data sheet.**

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19-6646; Rev 1; 2/15

maxim integrated™

Absolute Maximum Ratings

V_{TT} to AGND ..... -0.3V to (V_{BIAS} + 0.3V)
BIAS to AGND ..... -0.3V to +6V
EN, SCL, SDA to AGND ..... -0.3V to +6V
CSP1, CSN1, CSP2, CSN2 to AGND ..... -0.3V to +6V
FB, FBAC, IMON to AGND ..... -0.3V to (V_{BIAS} + 0.3V)
DRVPWM1, DRVPWM2 to PGND ..... -0.3V to (V_{BIAS} + 0.3V)
$\overline{DRVSKP}$ to PGND ..... -0.3V to (V_{BIAS} + 0.3V)
$\overline{INT}$, THERM to AGND ..... -0.3V to +6V
IC to AGND ..... -0.3V to +6V
GNDS to AGND ..... -0.3V to +0.3V
PGND to AGND ..... -0.3V to +0.3V
TON to AGND ..... -0.3V to +26V
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 27.8mW above +70°C) 2.2W
Operating Temperature Range ..... -40°C to +105°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +165°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....36°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....3°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics (0°C to +85°C)

(Circuit of Figure 1. V_{IN} = 10V, V_{BIAS} = 5V, V_{TT} = 1.8V, EN = BIAS, GNDS = AGND, V_{FBAC} = V_{FB} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1V [SETVOUT register 0x07h set to 0x33h]. T_A = 0°C to +85°C, unless otherwise noted. Typical values are at +25°C. All devices 100% tested at +25°C. Limits over temperature are guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BIAS CURRENTS							
BIAS Voltage Range	V_{BIAS}			4.75		5.25	V
I²C Interface Supply (V_{TT})	V_{TT}			1.6		4.0	V
Quiescent Supply Current (BIAS)	I_{BIAS}	Skip mode, measured at BIAS, V_{TT} = 1.8V; FB forced above the regulation point, EN = BIAS			2	5	mA
Shutdown Supply Current (BIAS)		Measured at BIAS, EN = GND, V_{TT} = 1.8V or GND, T_A = +25°C				6	µA
V_{TT} BIAS Current	I_{VTT}	V_{BIAS} = high, EN = low, T_A = +25°C				3	µA
		V_{BIAS} = high, EN = high, T_A = +25°C				50	
PWM CONTROLLER							
DC Output Voltage Accuracy (Note 2)		T_A = +25°C; measured at FB, with respect to GNDS; includes load regulation error	DAC codes from 0.50V to 1.60V	-5		+5	mV
DC Output Voltage Accuracy (Note 2)		Measured at FB, with respect to GNDS; includes load regulation error	DAC codes from 0.50V to 1.40V	-8		+8	mV
			DAC codes from 1.40V to 1.60V	-0.7		+0.7	%
Line Regulation Error		V_{BIAS} = 4.75V to 5.25V, V_{IN} = 5.5V to 20V			0.1		mV

Electrical Characteristics (0°C to +85°C) (continued)

(Circuit of Figure 1. V_{IN} = 10V, V_{BIAS} = 5V, V_{TT} = 1.8V, EN = BIAS, GNDS = AGND, V_{FBAC} = V_{FB} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1V [SETVOUT register 0x07h set to 0x33h]. T_A = 0°C to +85°C, unless otherwise noted. Typical values are at +25°C. All devices 100% tested at +25°C. Limits over temperature are guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GNDS Input Range			-200		+200	mV
GNDS Gain	A_{GNDS}		0.97	1.00	1.03	V/V
GNDS Input BIAS Current	I_{GNDS}	T_A = +25°C	-0.5		+0.5	µA
TON Shutdown Current		EN = AGND, V_{IN} = 24V, V_{BIAS} = 0V or 5V, T_A = +25°C		0.01	0.1	µA
DRVPWM_ On-Time (Note 3)	t_{ON}	Measured at DRVPWM_, R_{TON} = 136.3kΩ (1400kHz)	60	71	82	ns
		Measured at DRVPWM_, R_{TON} = 200kΩ (1000kHz)	92	104	114	
		Measured at DRVPWM_, R_{TON} = 326.7kΩ (600kHz)	141	166	192	
Minimum Off-Time (Note 3)	$t_{OFF(MIN)}$	Measured at DRVPWM_		100	133	ns
Slew-Rate Accuracy (see Table 8 for Soft-Start and Regular Slew-Rate Combinations)		Slew rate = 3.5mV/µs , 4.5mV/µs, 5.5mV/µs, 7mV/µs, 9mV/µs, 11mV/µs, 14mV/µs, 18mV/µs, 22mV/µs, 28mV/µs, 36mV/µs, 44mV/µs (nominal)	-20			%
FAULT PROTECTION						
Upper $\overline{INT}$ and Output Overvoltage-Protection Trip Threshold	V_{OVP}	Soft-start completed, measured at FB	1.78	1.83	1.88	V
Upper $\overline{INT}$ and Output Overvoltage Propagation Delay	t_{OVP}	FB forced 25mV above trip threshold		5		µs
Lower $\overline{INT}$ and Output Undervoltage-Protection Trip Threshold	V_{UVP}	Measured at FB, with respect to unloaded output voltage	-300	-250	-200	mV
Lower $\overline{INT}$ Propagation Delay		FB forced 25mV below trip threshold		5		µs
Output Undervoltage Propagation Delay	t_{UVP}	FB forced 25mV below trip threshold	100	200	350	µs
$\overline{INT}$ Output Low Voltage		I_{SINK} = 4mA			0.3	V
$\overline{INT}$ Leakage Current		High state, $\overline{INT}$ forced to 5V, T_A = +25°C			1	µA
$\overline{INT}$ Startup Delay and Transitions Blanking Time	$t_{\overline{INT}}$	Measured from the time when FB reaches the target voltage		4		µs
V_{BIAS} Undervoltage-Lockout Threshold	V_{UVLO}	Rising edge, 50mV typical hysteresis, controller disabled below this level	4.3	4.5	4.7	V

Electrical Characteristics (0°C to +85°C) (continued)

(Circuit of Figure 1. V_{IN} = 10V, V_{BIAS} = 5V, V_{TT} = 1.8V, EN = BIAS, GNDS = AGND, V_{FBAC} = V_{FB} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1V [SETVOUT register 0x07h set to 0x33h]. T_A = 0°C to +85°C, unless otherwise noted. Typical values are at +25°C. All devices 100% tested at +25°C. Limits over temperature are guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
THERMAL PROTECTION						
THERM Resistor	R_{THERM}	Internal pullup resistance	5.24	5.35	5.48	kΩ
VRHOT Trip Threshold		Measured at THERM, with respect to V_{BIAS} falling edge; specify as % error for all temp max DAC code settings; typical hysteresis = 100mV, T_A = +25°C to +100°C	49.5		50.5	%
THERM Sampling Period		5% duty cycle		0.75	1.1	ms
Internal Thermal-Fault Shutdown Threshold	T_{TSHDN}	Typical hysteresis = +15°C		160		°C
VALLEY CURRENT LIMIT AND DROOP						
Valley Current-Limit Threshold Voltage (Positive)	V_{ILIM}	$V_{CSP\_}$ - $V_{CSN\_}$	35	38	41	mV
OC_ALARM Valley Current Threshold Voltage (Positive, CSP1 Only)	V_{OC_ALARM}	$V_{CSP1 - VCSN1}$	20	23	26	mV
Current-Balance Offset Voltage			-1.8		+1.8	mV
Current-Sense Common-Mode Input Range		CSP1, CSN1, CSP2, CSN2	0.5		1.6	V
Current-Sense Input Current		CSP1, CSN1, CSP2, CSN2, T_A = +25°C	-0.12		+0.12	µA
Discharge Switch Resistance		CSN1 only		2		kΩ
FB Input Current		T_A = +25°C	-0.2		+0.2	µA
Phase 2 Disable Threshold		CSP2	3	V_{BIAS} - 1.0	V_{BIAS} - 0.4	V
Droop Amplifier (GMD) Offset		Average ($V_{CSP\_}$ - $V_{CSN\_}$) at I_{FBAC} = 0mA	-1.0		+1.0	mV
Droop Amplifier (GMD) Transconductance	$G_{m(FBAC)}$	$\Delta I_{FBAC}/\Sigma\Delta$ ($V_{CSP\_}$ - $V_{CSN\_}$), measured at FBAC	1.182	1.2	1.218	µA/mV
CURRENT MONITOR (IMON)						
Current Monitor Output Current for Typical Full-Load Conditions	I_{IMON}	Σ($V_{CSP\_}$ - $V_{CSN\_}$) = 25mV	124.2	128	131.8	µA
Current Monitor Gain	$G_{m(IMON)}$	$\Delta I_{IMON}/\Sigma\Delta$ ($V_{CSP\_}$ - $V_{CSN\_}$), measured at IMON	4.8	5.12	5.44	µA/mV
Current Monitor Clamp Voltage		IMON		3.2	3.6	V
DRIVER CONTROL						
DRVPWM_, DRVSKP# Output Logic-High Voltage	V_{OH_DRV}	I_{SOURCE} = 3mA	V_{BIAS} - 0.4			V
DRVPWM_, DRVSKP# Output Logic-Low Voltage	V_{OL_DRV}	I_{SINK} = 3mA			0.4	V
DRVPWM_ Output Midlevel Voltage			1.6		2.3	V

Electrical Characteristics (0°C to +85°C) (continued)

(Circuit of Figure 1. V_{IN} = 10V, V_{BIAS} = 5V, V_{TT} = 1.8V, EN = BIAS, GNDS = AGND, V_{FBAC} = V_{FB} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1V [SETVOUT register 0x07h set to 0x33h]. T_A = 0°C to +85°C, unless otherwise noted. Typical values are at +25°C. All devices 100% tested at +25°C. Limits over temperature are guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE LOGIC (EN)						
EN Input High Voltage	V_{IH_EN}		0.7 x V_{TT}			V
EN Input Low Voltage	V_{IL_EN}				0.33	V
EN Input Current	I_{EN}	T_A = +25°C	-1		+1	µA
Power-Up Calibration Delay	t_{CAL}			850		µs
Enable to Startup Delay	t_{STRT}	EN to first switching edge (fully discharged output)		150		µs
I²C INTERFACE (SDA, SCL)						
I²C Input Low Voltage	V_{IL}				0.4	V
I²C Input High Voltage	V_{IH}		0.7 x V_{TT}			V
I²C Output Low Level (SDA Only)	V_{OL}	Open-drain output, 3mA pullup to V_{TT}			0.4	V
I²C Logic Inputs Leakage Current		T_A = +25°C	-1		+1	µA
I²C TIMING REQUIREMENTS						
I²C Clock Frequency					3.4	MHz
Hold Time Repeated START Condition	t_{HD_STA}	(Note 4)	160			ns
SCL Low Period	t_{LOW}	(Note 4)	160			ns
SCL High Period	t_{HIGH}	(Note 4)	60			ns
Setup Time Repeated START Condition	t_{SU_STA}	(Note 4)	160			ns
SDA Hold Time	t_{HD_DAT}	(Note 4)	0		70	ns
SDA Setup Time	t_{SU_DAT}	(Note 4)	10			ns
Setup Time for STOP Condition	t_{SU_STO}	(Note 4)	160			ns

Electrical Characteristics (-40°C to +105°C)

(Circuit of Figure 1. V_{IN} = 10V, V_{BIAS} = 5V, V_{TT} = 1.8V, EN = BIAS, GNDS = AGND, V_{FBAC} = V_{FB} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1V [SETVOUT register 0x07h set to 0x33h]. T_A = -40°C to +105°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BIAS CURRENTS							
BIAS Voltage Range	V_{BIAS}			4.75		5.25	V
I²C Interface Supply (V_{TT})	V_{TT}			1.6		4.0	V
Quiescent Supply Current (BIAS)	I_{BIAS}	Skip mode, measured at BIAS, V_{TT} = 1.8V; FB forced above the regulation point; EN = BIAS				5	mA
PWM CONTROLLER							
DC Output Voltage Accuracy (Note 2)		Measured at FB, with respect to GNDS; includes load regulation error	DAC codes from 0.50V to 1V	-10		+10	mV
			DAC codes from 1V to 1.60V	-1.0		+1.0	%
GNDS Gain	A_{GNDS}			0.97		1.03	V/V
DRVPWM_ On-Time (Note 3)	t_{ON}	Measured at DRVPWM_, R_{TON} = 136.3kΩ, (1400kHz)		60		82	ns
		Measured at DRVPWM_, R_{TON} = 200kΩ, (1000kHz)		92		114	
		Measured at DRVPWM_, R_{TON} = 326.7kΩ, (600kHz)		141		192	
Minimum Off-Time (Note 3)	$t_{OFF(MIN)}$	Measured at DRVPWM_				133	ns
Slew-Rate Accuracy (see Table 8 for Soft-Start and Regular Slew-Rate Combinations)		Slew rate = 3.5mV/µs , 4.5mV/µs, 5.5mV/µs, 7mV/µs, 9mV/µs, 11mV/µs, 14mV/µs, 18mV/µs, 22mV/µs, 28mV/µs, 36mV/µs, 44mV/µs (nominal)		-20			%
FAULT PROTECTION							
Upper $\overline{INT}$ and Output Overvoltage-Protection Trip Threshold	V_{OVP}	Soft-start completed; measured at FB		1.78		1.88	V
Lower $\overline{INT}$ and Output Undervoltage-Protection Trip Threshold	V_{UVP}	Measured at FB, with respect to unloaded output voltage		-300		-200	mV
Output Undervoltage Propagation Delay	t_{UVP}	FB forced 25mV below trip threshold		100		350	µs
$\overline{INT}$ Output Low Voltage		I_{SINK} = 4mA				0.3	V
V_{BIAS} Undervoltage-Lockout Threshold	V_{UVLO}	Rising edge, 50mV typical hysteresis; controller disabled below this level		4.3		4.7	V

Electrical Characteristics (-40°C to +105°C) (continued)

(Circuit of Figure 1. V_{IN} = 10V, V_{BIAS} = 5V, V_{TT} = 1.8V, EN = BIAS, GNDS = AGND, V_{FBAC} = V_{FB} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1V [SETVOUT register 0x07h set to 0x33h]. T_A = -40°C to +105°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
THERMAL PROTECTION						
THERM Resistor	R_{THERM}	Internal pullup resistance	5.24		5.48	kΩ
VRHOT Trip Threshold		Measured at THERM, with respect to V_{BIAS} falling edge; specify as % error for all temp max DAC code settings; typical hysteresis = 100mV; T_A = +25°C to +105°C	49.5		50.5	%
VALLEY CURRENT LIMIT AND DROOP						
Valley Current-Limit Threshold Voltage (Positive)	V_{ILIM}	$V_{CSP\_}$ - $V_{CSN\_}$	35		41	mV
OC_ALARM Valley Current Threshold Voltage (Positive, CSP1 Only)	V_{OC_ALARM}	V_{CSP1} - V_{CSN1}	20		26	mV
Current-Balance Offset Voltage			-2.5		+2.5	mV
Current-Sense Common-Mode Input Range		CSP1, CSN1, CSP2, CSN2	0.5		1.6	V
Phase 2 Disable Threshold		CSP2	3		V_{BIAS} - 0.4	V
Droop Amplifier (GMD) Offset		Average ($V_{CSP\_}$ - $V_{CSN\_}$) at I_{FBAC} = 0mA	-1.0		+1.0	mV
Droop Amplifier (GMD) Transconductance	$G_{m(FBAC)}$	$\Delta I_{FBAC}/\sum\Delta$ ($V_{CSP\_}$ - $V_{CSN\_}$), measured at FBAC	1.176		1.224	µA/mV
CURRENT MONITOR (IMON)						
Current Monitor Output Current for Typical Full-Load Conditions	I_{IMON}	$\sum$($V_{CSP\_}$ - $V_{CSN\_}$) = 25mV	122.2		133.8	µA
Current Monitor Gain	$G_{m(IMON)}$	$\Delta I_{IMON}/\sum\Delta$ ($V_{CSP\_}$ - $V_{CSN\_}$), measured at IMON	4.8		5.44	µA/mV
DRIVER CONTROL						
DRVPWM_, $\overline{DRVSKP}$ Output Logic-High Voltage	V_{OH_DRV}	I_{SOURCE} = 3mA	V_{BIAS} - 0.4			V
DRVPWM_, $\overline{DRVSKP}$ Output Logic-Low Voltage	V_{OL_DRV}	I_{SINK} = 3mA			0.4	V
DRVPWM_ Output Midlevel Voltage			1.6		2.3	V
ENABLE LOGIC (EN)						
EN Input High Voltage	V_{IH_EN}		0.7 x V_{TT}			V
EN Input Low Voltage	V_{IL_EN}				0.33	V

Electrical Characteristics (-40°C to +105°C) (continued)

(Circuit of Figure 1. V_{IN} = 10V, V_{BIAS} = 5V, V_{TT} = 1.8V, EN = BIAS, GNDS = AGND, V_{FBAC} = V_{FB} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1V [SETVOUT register 0x07h set to 0x33h]. T_A = -40°C to +105°C, unless otherwise noted.)

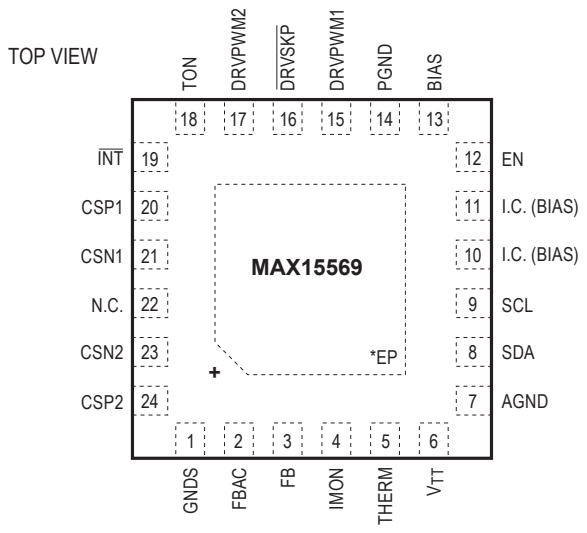
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C TIMING REQUIREMENTS						
I²C Clock Frequency					3.4	MHz
Hold Time Repeated START Condition	t_{HD_STA}	(Note 4)	160			ns
SCL Low Period	t_{LOW}	(Note 4)	160			ns
SCL High Period	t_{HIGH}	(Note 4)	60			ns
Setup Time Repeated START Condition	t_{SU_STA}	(Note 4)	160			ns
SDA Hold Time	t_{HD_DAT}	(Note 4)	0		70	ns
SDA Setup Time	t_{SU_DAT}	(Note 4)	10			ns
Setup Time for STOP Condition	t_{SU_STO}	(Note 4)	160			ns

Note 2: The equation for the target voltage V_{TARGET} is: V_{TARGET} = the output of slew control DAC, where V_{DAC} = 0V for shutdown, V_{DAC} = V_{BOOT} during startup; otherwise V_{DAC} = SETVOUT. The output voltages for all possible codes are given in Table 3.

Note 3: On-time and minimum off-time specifications are measured from 50% rise to 50% fall at the DRVPWM_ pin. Actual in-circuit times can be different due to MOSFET driver characteristics.

Note 4: Guaranteed by design. Not production tested.

Pin Configuration



TQFN
(4mm x 4mm)

*EP = EXPOSED PAD. CONNECT TO GROUND.

Pin Description

PIN	NAME	FUNCTION
1	GNDS	Ground Remote-Sense Input. Connect GNDS to the ground-sense pin of the CPU located directly at the point of load. GNDS internally connects to an internal transconductance amplifier that adjusts the feedback voltage to compensate for voltage drops between the local controller ground and the remote load ground.
2	FBAC	Output of the AC Voltage Positioning Transconductance Amplifier. The effective impedance (Z_{FBAC}) between this pin and the positive side of the remote-sensed output voltage sets the transient AC droop. See the *Load-Line Amplifier (Steady State and AC Droop)* section. FBAC is high impedance in shutdown.
3	FB	Feedback-Sense Input. An integrator on FB corrects for output ripple and ground-sense offset. Connect a resistor (R_{FB}) between FB and the positive output of the remote sense (output) to set the DC steady-state droop. The impedance from FBAC to FB sets the current-loop gain over frequency, which dominates stability. See the *Load-Line Amplifier (Steady State and AC Droop)* section.
4	IMON	Current Monitor Output. The output current at IMON is: $I_{IMON} = G_{M(IMON)} \times \sum (CSP\_ - CSN\_)$ where $G_{M(IMON)}$ = 5.12mS (typ). An external resistor (R_{IMON}) between IMON and GNDS sets the current monitor output voltage: $V_{IMON} = I_{LOAD} \times RSENSE \times G_{M(IMON)} \times R_{IMON}$ where R_{SENSE} is the value of the effective current-sense resistance. Choose R_{IMON} so that V_{IMON} is 2.56V at the desired full current. IMON is high impedance when in shutdown.
5	THERM	Thermal-Sense Input. Connect a 100kΩ NTC with β = 4250K from THERM to AGND. The NTC at THERM is used to determine the temperature of the power stages. Place near the hottest region of the regulator (typically the MOSFETs and inductor of phase 1). The VRHOT status bit (D5) activates when the NTC resistance drops to 5.68kΩ (100°C when using a 100kΩ NTC with β = 4250K).
6	V_{TT}	Interface Logic Supply. Power V_{TT} from a 1.8V to 3.3V ±10% source with a compliance of at least 1mA. Decouple V_{TT} with at least 1µF of ceramic capacitance.
7	AGND	Analog Ground
8	SDA	I²C Serial-Data Input/Output. Open-Drain I/O pin. Connect an external pullup resistor between SDA and the supply used to power the I²C interface (V_{TT}).
9	SCL	I²C Serial-Data Clock Input
10, 11	I.C.	Internally Connected. Connect to BIAS.
12	EN	Controller Enable Input. Drive EN high or connect EN to BIAS for normal operation. Pull to ground to put the controller into its 7µA (max) standby state (I²C interface active, regulator not switching). During soft-start, the controller slowly ramps the output voltage up to the boot voltage with the selected slew rate (register 0x06, default is 4.5mV/µs for start-up and 9mV/µs for normal operation). During the transition from normal operation to standby, the output is discharged through a 2kΩ internal discharge MOSFET on CSN1. Toggling EN does **NOT** reset the fault latches. Cycle power (V_{TT} or BIAS) to trigger the power-on reset (POR) to clear the fault conditions. The EN input is rated for up to 5.5V.

Pin Description (continued)

PIN	NAME	FUNCTION
13	BIAS	Analog and Driver Supply Voltage Input. BIAS provides the supply voltage for the driver's PWM and skip control outputs. Connect BIAS to the same supply used by the external drivers (typically the 4.5V to 5.5V system supply voltage). Bypass BIAS to power ground with a local 1µF or greater ceramic capacitor.
14	PGND	Power Ground
15	DRVPWM1	Direct-Drive PWM Output for Controlling the External First-Phase Driver. The DRVPWM1 push-pull output drives the signal between BIAS and PGND. DRVPWM1 is high impedance in shutdown and after fault conditions (output overvoltage/undervoltage or thermal fault).
16	$\overline{\text{DRVSKP}}$	External Driver Skip-Mode Control Output. The $\overline{\text{DRVSKP}}$ output is low in standby. $\overline{\text{DRVSKP}}$ goes high when the controller detects an output overvoltage fault condition, or during dynamic output-voltage transitions. For applications operating with forced-PWM operation, disable the driver zero-crossing detection and leave $\overline{\text{DRVSKP}}$ unconnected.
17	DRVPWM2	Direct-Drive PWM Output for Controlling the External Second-Phase Driver. The DRVPWM2 push-pull output drives the signal between BIAS and PGND. DRVPWM2 is high impedance in shutdown and after fault conditions (output overvoltage, output undervoltage, or thermal fault).
18	TON	Switching Frequency Adjustment Input. An external resistor between the input power source and TON sets the switching period (per phase) according to the following equation: $f_{SW} = (R_{TON} + 6.5k\Omega) \times 5pF$ where $f_{SW} = 1/f_{SW}$ is the nominal switching frequency. A 200kΩ resistor provides a typical operating frequency of 1MHz. TON is high impedance in shutdown.
19	$\overline{\text{INT}}$	Open-Drain Interrupt Output. $\overline{\text{INT}}$ is triggered by latched faults (output undervoltage, output overvoltage, thermal shutdown), sticky alarms (internal overcurrent (OC), non-sticky alarms (voltage regulator hot (VRHOT), and VID code violations (VOUTMAX)). The fault conditions and alarms can be masked through register 0x05h. Masking these signals only prevents $\overline{\text{INT}}$ from being asserted; the STATUS register still asserts when any of these conditions occur. $\overline{\text{INT}}$ remains high in standby mode (EN pulled low) to reduce power through the pullup resistor. $\overline{\text{INT}}$ is pulled low during soft-start. After completing the soft-start sequence, $\overline{\text{INT}}$ becomes high impedance as long as FB remains in regulation and there are no active alarms. To obtain a logic signal, pull up $\overline{\text{INT}}$ with an external resistor connected to a logic supply.
20	CSP1	Positive Current-Sense Input for the First Phase. 1) Connect CSP1 to the positive side of the current-sense resistor or the DCR sense filter capacitor of phase 1, as shown in Figure 4. 2) Connect CSP1 to the IOUT pin of the smart power stage (MAX15515). A resistor across CSP1 and CSN1 sets the current-sense gain, as shown in Figure 3. See the *Current Sense* section.
21	CSN1	Negative Current-Sense Input for the First Phase. Connect CSN1 to the negative side of the current-sense element, as shown in Figure 4. An internal 2kΩ discharge MOSFET between CSN1 and ground is enabled under an input UVLO or shutdown condition.
22	N.C.	No Connection Internally

Pin Description (continued)

PIN	NAME	FUNCTION
23	CSN2	Negative Current-Sense Input for the Second Phase. Connect CSN2 to the negative side of the current-sense element, as shown in Figure 4.
24	CSP2	Positive Current-Sense Input for the Second Phase. 1) Connect CSP2 to the positive side of the current-sense resistor or the DCR sense filter capacitor of phase 2, as shown in Figure 4. 2) Connect CSP2 to the IOUT pin of the smart power stage (MAX15515). A resistor across CSP2 and CSN2 sets the current-sense gain, as shown in Figure 3. See the *Current Sense* section. To disable phase 2, short CSP2 to BIAS.
—	EP	Exposed Pad. The substrate of the controller is internally connected to the exposed pad. Connect EP to the ground plane through multiple vias to maintain low thermal impedance.

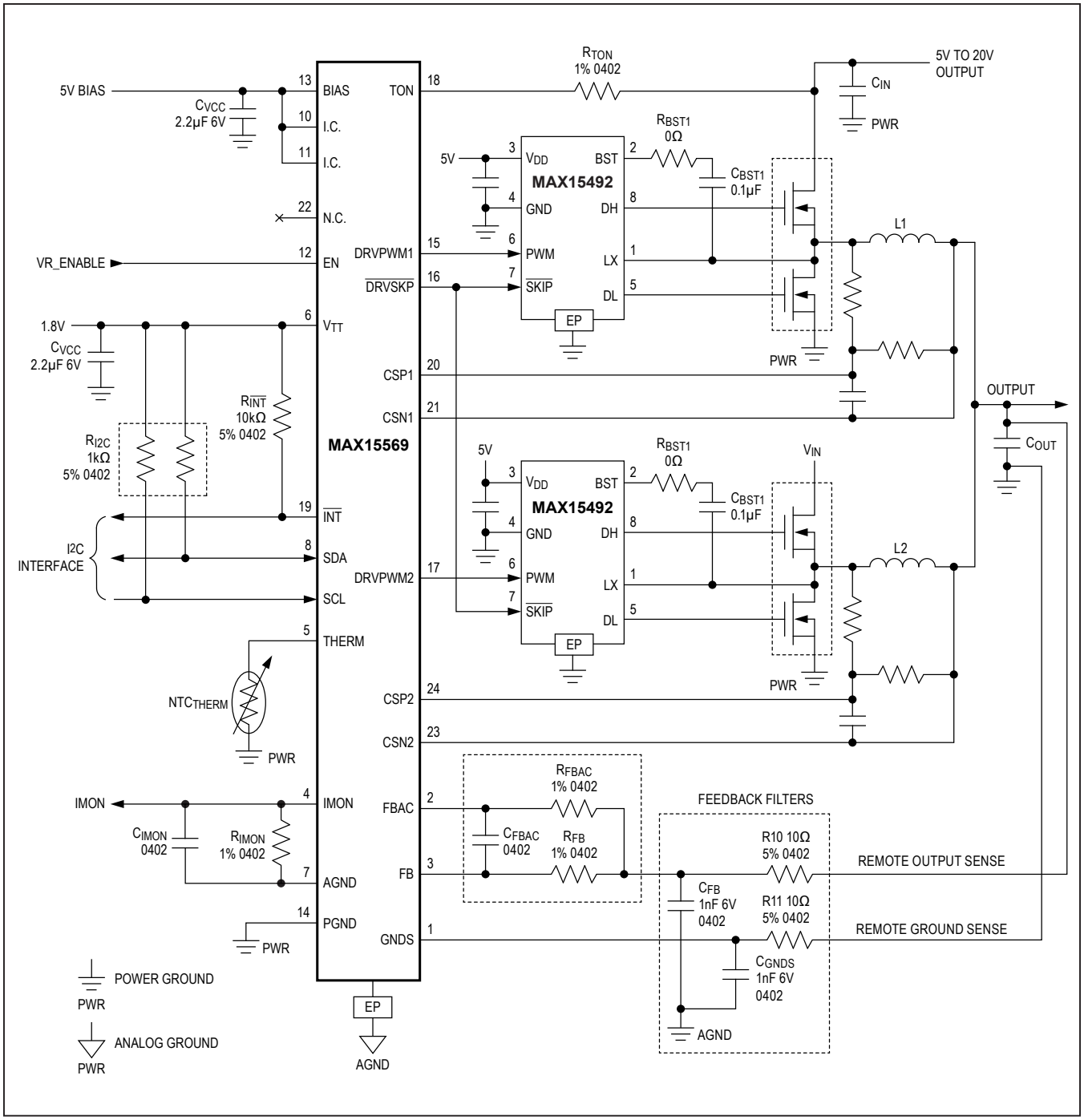


Figure 1. MAX15569 Typical Application Circuit (with MAX15492 Driver and MOSFET)

Table 1. Components for Typical Application Circuit

TYPE	REF	2-PHASE DESIGN EXAMPLE (1MHz OPERATION)
OPERATING CONDITIONS		
Input Voltage	V_{IN}	5V to 20V
Output Voltage	V_{OUT}	1V
Output Current	I_{OUT}	20A (max), 14A RMS
Load Transient	ΔI_{OUT}	25A
Current Limit	I_{OCP}	40A
Switching Frequency	f_{SW}	1MHz
Number of Phases	N_{PH}	2
COMPONENTS		
TON	R_{TON}	200kΩ 1%
Inductor	L	0.2µH/9.5mΩ/9.5A inductor (4.06mm x 4.55mm x 1.2mm) Vishay IHLP-1616AB-1A
MOSFET Driver	DRV	MAX15492
High-Side MOSFET	N_H	—
Low-Side MOSFET	N_L	
Current Sense	R_{CS}	—
Bulk Output Capacitors (Mid Frequency)	C_{OUT}	—
Ceramic Output Capacitors (High Frequency)	C_{OUT}	20 x 22µF ceramic capacitors
Input Capacitors	C_{IN}	2 x 10µF, 16V X5R ceramic capacitors
FB Droop Setting	—	$R_{FBAC} = R_{FB}$ = 1kΩ 1% C_{FBAC} = 4.7nF AC droop = -1.5mV/A DC droop = 0mV/A
IMON	R_{IMON}, C_{IMON}	R_{IMON} = 5.62kΩ 1% C_{IMON} = 47nF (260µs time constant)
THERM NTC	R_{THERM}	100kΩ, 5% NTC thermistor β = 4250K (0603) Murata NCP18WF104J03RB TDK NTCG163JF104J (0402) or Panasonic ERT-J1VR104J

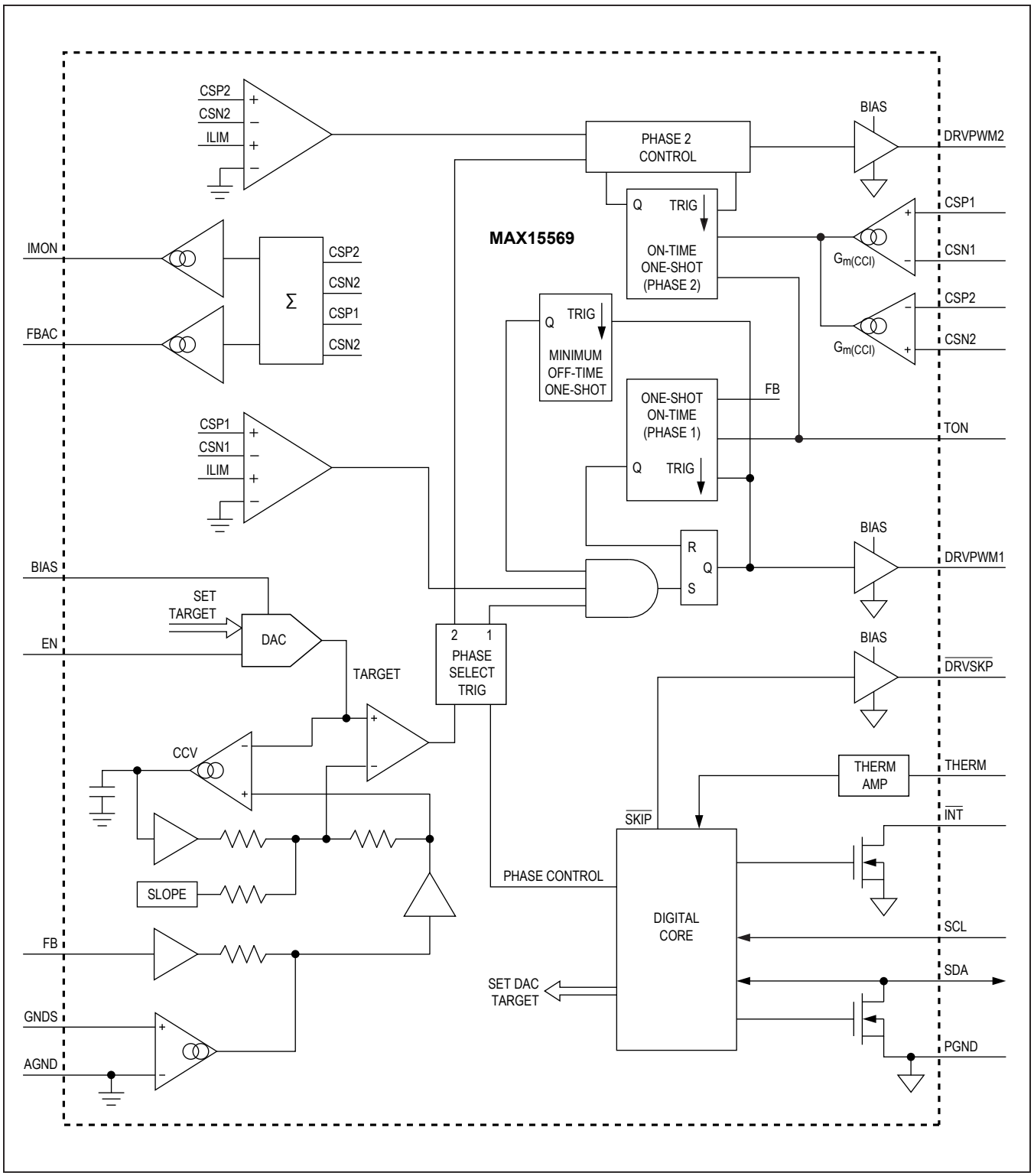


Figure 2. Functional Block Diagram

Detailed Description

For system power management, the MAX15569 controller includes a current gauge and thermal status (VRHOT) that can be monitored over the I²C interface. In addition, the device's multiple fault-protection features include: Output overvoltage protection (OVP), undervoltage protection (UVP), and thermal protection. When any of these fault-protection features detect a fault condition, the controller shuts down.

Free-Running Constant On-Time Controller with Input Feed-Forward

The QuickTune-PWM control architecture consists of a pseudo-fixed frequency, constant on-time, and current-mode regulator with voltage feed-forward (Figure 2). The control algorithm is simple; the high-side switch on-time is determined solely by a one-shot, whose period is inversely proportional to input voltage and directly proportional to the feedback voltage or the difference between the main and secondary inductor currents (see the *On-Time One-Shot* section). Another one-shot sets a minimum off-time.

The on-time one-shot triggers when the inverting input to the error comparator falls below the target voltage, the inductor current of the selected phase is below the valley current-limit threshold, and the minimum off-time one-shot times out. The regulator maintains 180° out-of-phase operation by alternately triggering the two phases after the error comparator drops below the output-voltage set point.

Switching Frequency

Connect a resistor (R_{TON}) between TON and the input supply (V_{IN}) to set the switching period (t_{SW} = 1/f_{SW}) per phase using the following equation:

$$t_{SW} (R_{TON} + 6.5k\Omega) \times 5pF$$

High-frequency (600kHz to 1.4MHz) operation optimizes the application for the smallest component size. A 200kΩ resistor sets a typical operating frequency of 1MHz.

On-Time One-Shot

The device contains fast, low-jitter, adjustable one-shots that set the respective high-side MOSFET on-times through the DRVPWM_ outputs. The one-shot for the main phase varies the on-time in response to the input and feedback voltage (V_{FB}). V_{FB} equals the SETVOUT voltage in steady-state. The main high-side switch on-time is inversely proportional to the input voltage as measured at V_{IN}, and proportional to V_{FB}:

$$t_{ON} = \frac{t_{SW}(V_{FB} + 0.075V)}{V_{IN}} \text{ (Ignoring propagation delays)}$$

For SETVOUT voltages below 0.9V, the device uses a fixed 0.9V instead to determine the on-time. Switching frequency is reduced, improving low-voltage efficiency.

$$t_{ON} = \frac{t_{SW}(0.9V + 0.075V)}{V_{IN}}$$

The one-shot for the second phase varies the on-time in response to the input voltage and the difference between the main and the second inductor currents. Two identical transconductance amplifiers integrate the difference between the first and second current-sense signals. The respective error signals are used to correct the on-time of the high-side MOSFETs for the second phase and to maintain current balanced between the two phases.

On-times translate only roughly to switching frequencies. The on-times guaranteed in the *Electrical Characteristics* section are influenced by parasitics in the conduction paths and propagation delays. The following equation shows the effect of the propagation delays on t_{ON}:

$$t_{ON} = \frac{t_{SW}(V_{FB} + 0.075V)}{V_{IN}} + t_{D(OFF)} - t_{D(ON)}$$

where $t_{D(OFF)}$ is the delay from the falling edge of the PWM signal to the to the time that the high-side MOSFET turns off. $t_{D(ON)}$ is the delay from the rising edge of the PWM signal to the time that the high-side MOSFET turns on.

For loads above the critical conduction point, where the dead-time effect (LX flying high and conducting through the high-side FET body diode) is no longer a factor, the actual switching frequency (per phase) is:

$$f_{SW} = \frac{(V_{OUT} + V_{DIS})}{t_{ON}(V_{IN} + V_{DIS} + V_{CHG})}$$

where V_{DIS} is the sum of the parasitic voltage drops in the inductor discharge and charge paths, including MOSFET, inductor, and PCB resistances; V_{CHG} is the sum of the parasitic voltage drops in the inductor charge path, including high-side switch, inductor, and PCB resistances; and t_{ON} is the on-time as determined in the prior equation.

180° Out-of-Phase Operation

The two phases in the device operate 180° out-of-phase to minimize input and output filtering requirements, reduce EMI, and improve efficiency. This effectively lowers component count—reducing cost, board space, and component power requirements—making this device ideal for high-power applications. The device shares the current between two phases that operate 180° out-of-phase under steady-state conditions.

The instantaneous input current of each phase is effectively reduced, resulting in reduced input-voltage ripple, ESR power loss, and RMS ripple current (see the *Input Capacitor Selection* section). Therefore, the same performance can be achieved with fewer or less-expensive input capacitors.

5V Bias Supply

The QuickTune-PWM controller requires an external 5V bias supply in addition to the system supply. Typically, the system has a regulated 5V bias for interface (USB) or hard-drive support that can be used. The maximum current drawn from the 5V bias supply is provided in the *Electrical Characteristics* section. If the 5V bias supply is powered up prior to the system supply, the enable signal (EN going from low to high) should be delayed until the system voltage is present to ensure startup.

Current Sense

The device senses the inductor current of each phase, allowing the use of current-sense resistors, inductor DCR, or the current-sense signal provided by the external power stage (MAX15515). Low-offset amplifiers are used for current balance, load-line gain, current monitor, and current limit.

Power Stage Current-Sense Support (MAX15515 Only)

The MAX15515 features a transconductance current-sense amplifier with a current monitor output (I_{OUT}) with an output current of:

$$I_{OUT} = A \times I_{LX}$$

where A is 10^{-5} (typ) and I_{LX} is the inductor current. I_{OUT} is internally temperature compensated and therefore, external temperature compensation is not required. Refer to the MAX15515 data sheet for more information.

A resistor between CSP_ and CSN_ (see Figure 3) sets the gain of the current-sense signal to the controller.

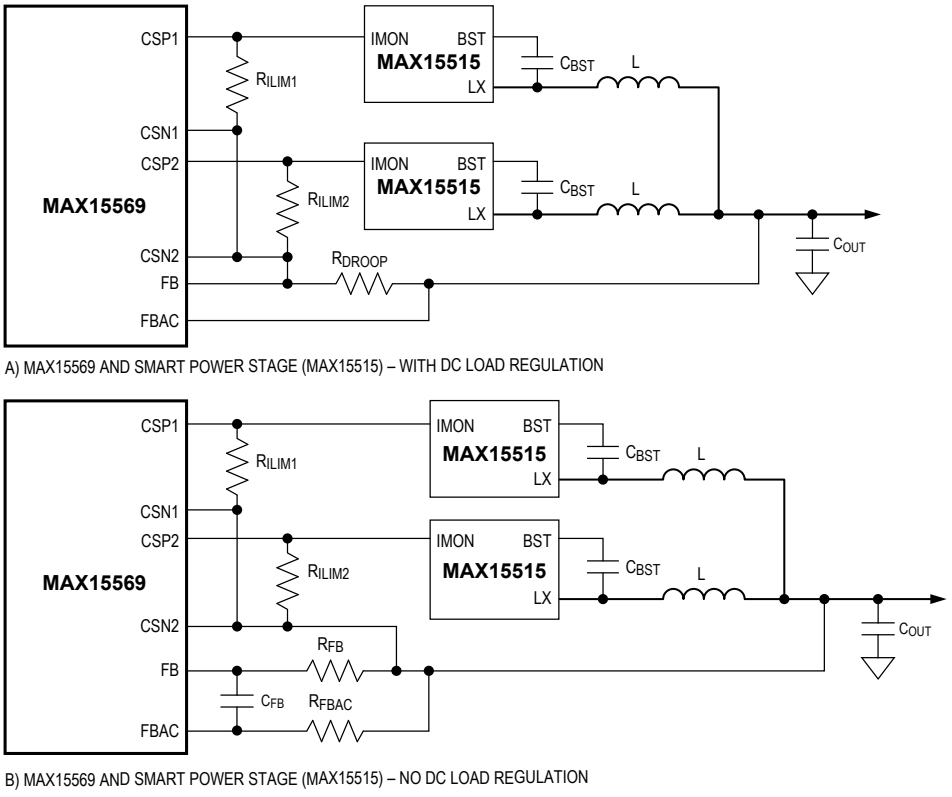


Figure 3. The MAX15569 Using the MAX15515 Internal Current-Sense Method

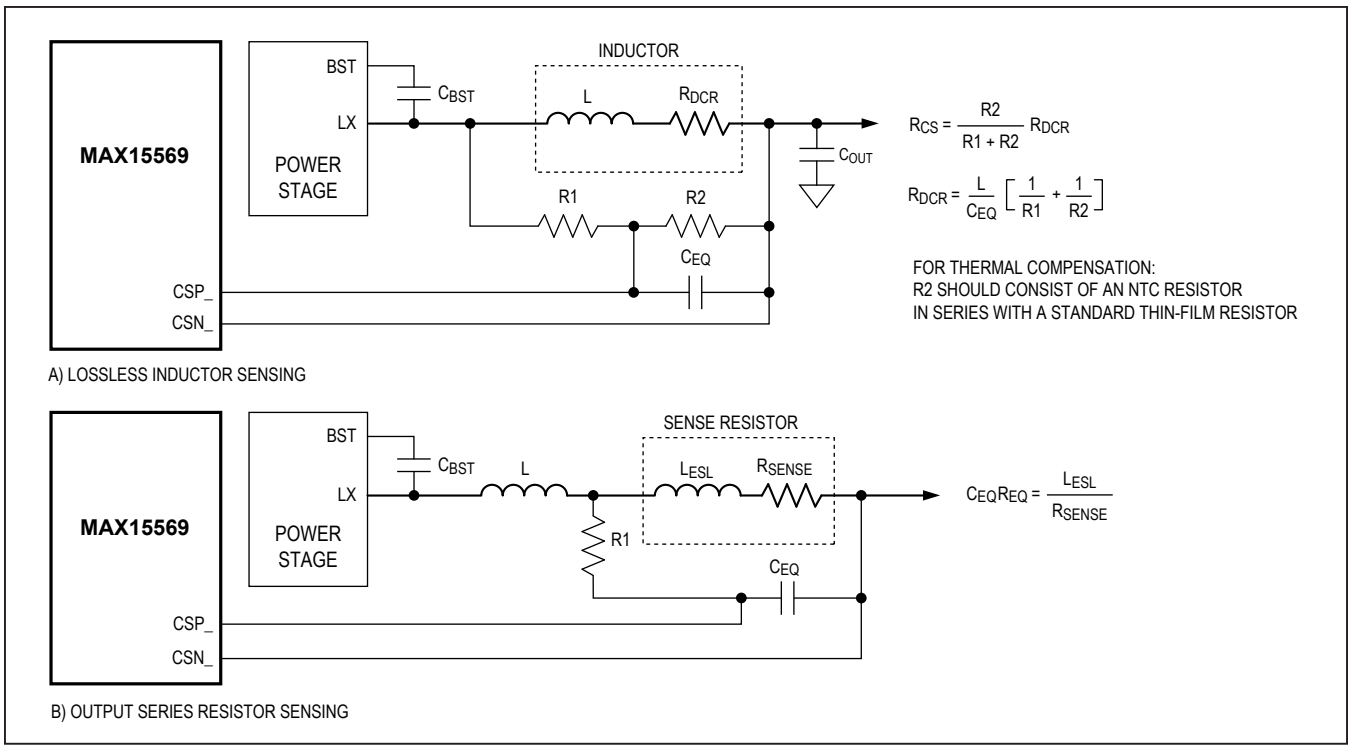


Figure 4. Sense Resistor and DCR Current-Sense Methods

Inductor DCR and Sense Resistor Current Sense

Using the DC resistance (R_{DCR}) of the output inductor allows higher efficiency compared to using a current-sense resistor. The initial tolerance and temperature coefficient of the inductor's DCR must be accounted for in the output-voltage droop-error budget and current monitor. This current-sense method uses an RC filter network to extract the current information from the output inductor (see Figure 4).

The RC network should match the time constant of the inductor (L/R_{DCR}):

$$R_{CS} = \left(\frac{R2}{R1+R2}\right)R_{DCR}$$

and:

$$R_{DCR} = \frac{L}{C_{EQ}}\left[\frac{1}{R1}+\frac{1}{R2}\right]$$

where R_{CS} is the required current-sense resistance and R_{DCR} is the inductor's series DC resistance. Use the typical inductance and R_{DCR} values provided by the inductor manufacturer. To minimize the current-sense error, due to the leakage current of the current-sense inputs ($I_{CSP\_}$ and $I_{CSN\_}$), choose R1||R2 to be less than 2kΩ and use the previous equation to determine the sense capacitance (C_{EQ}). Choose capacitors with 5% tolerance and resistors with 1% tolerance specifications. Temperature compensation is recommended for this current-sense method. See the *Load-Line Amplifier (Steady State and AC Droop)* section for detailed information.

When using a current-sense resistor for accurate output load-line control, the circuit requires a differential RC filter to eliminate the AC voltage step caused by the equivalent series inductance (L_{ESL}) of the current-sense resistor (see Figure 4). The ESL-induced voltage step might affect the average current-sense voltage. The time constant of the RC filter should match the L_{ESL}/R_{SENSE} time constant formed by the parasitic inductance of the current-sense resistor:

$$\frac{L_{ESL}}{R_{SENSE}} = C_{EQ}R_{EQ}$$

where L_{ESL} is the equivalent series inductance of the current-sense resistor, R_{SENSE} is the current-sense resistance value, and C_{EQ} and R_{EQ} are the time-constant matching components.

Current Balance

The device integrates the difference between the current-sense voltages and adjusts the on-time of the second phase to maintain current balance. The current balance relies on the accuracy of the current-sense signals across the current-sense resistor, inductor DCR, or provided by the power stage (MAX15515). With active current balancing, the current mismatch is determined by the current-sense element values and the offset voltage of the transconductance amplifiers:

$$I_{OS(IBAL)} = I_{LMAIN} - I_{LSEC} = \frac{V_{OS(IBAL)}}{R_{SENSE}}$$

where R_{SENSE} is the equivalent sense resistance across CSP_, CSN_, and $V_{OS(IBAL)}$ is the current-balance offset specification in the *Electrical Characteristics* section. The worst-case current mismatch occurs immediately after a load transient due to inductor value mismatches, resulting in different dI/dt for the two phases. The time it takes for the current-balance loop to correct the transient imbalance depends on the mismatch between the inductor values and switching frequency.

Current Limit

The current-limit circuit employs a "valley" current-sensing algorithm that senses the voltage across the current-sense inputs (CSP_ and CSN_). If the current-sense signal (V_{CSP2}, V_{CSN2} or V_{CSP1}, V_{CSN1}) of the selected phase is above the current-limit threshold (V_{ILIM}), the PWM controller does not initiate a new cycle for that phase until its inductor current drops below the valley current-limit threshold. Since only the valley current is actively limited, the actual peak current is greater than the current-limit threshold by an amount equal to 1/2 the inductor ripple current:

$$I_{LX(PEAK)} = I_{LOAD} + \frac{\Delta I}{2}$$

$$I_{LX(VALLEY)} = I_{LOAD} - \frac{\Delta I}{2}$$

where :

$$\Delta I = \frac{t_{ON}(V_{IN} - V_{OUT})}{L}$$

where L is the inductance value, t_{ON} is the on-time of the high-side MOSFET, V_{OUT} is the output voltage, and V_{IN} is the input voltage. Therefore, the exact current-limit characteristic and maximum load capability are functions of the current-sense resistance, inductor value, and battery voltage.

The positive valley current-limit threshold is preset for the MAX15569. See the *Electrical Characteristics* section.

Current Limit Using Inductor DCR or Sense Resistors

When using sense resistors or inductor DCR as current-sensing elements, calculate the required sense resistance (R_{SENSE}) with the following equation:

$$R_{SENSE} = \frac{V_{LIM(MIN)}}{I_{LX(VALLEY)}}$$

where $I_{LX(VALLEY)}$ is the inductor valley current at OCP, and $V_{ILIM(MIN)}$ is 38mV ±3mV.

Carefully observe the PCB layout guidelines to ensure that noise and trace errors do not corrupt the current-sense signals seen by the current-sense inputs (CSP_, CSN_).

Current Limit with the MAX15515 Current Sense

When using the current-sensing method of the MAX15515, calculate the CSP_ - CSN_ resistor ($R_{CSP\_}$) using the following equation:

$$R_{CSP\_} = \frac{V_{LIM(MIN)}}{A \times I_{LX(VALLEY)}}$$

where A is 10^{-5}, $I_{LX(VALLEY)}$ is the inductor valley current at OCP, and $V_{ILIM(MIN)}$ is 38mV ±3mV.

Current Monitoring (IMON)

The device includes a current monitoring function. A simplified data-acquisition system is employed to convert the analog signals from the current-sense inputs to 8-bit values in the IMON register (see Figure 5). The ADC converter filters the current-sense signal by averaging over eight samples. The acquisition rate is 100µs. The content of the IMON register is updated every 400µs.

The device includes a unidirectional transconductance amplifier that sources current proportional to the positive current-sense voltage. The IMON output current is defined by:

$$I_{IMON} = G_{m(IMON)} \times \Sigma(V_{CSP\_} - V_{CSN\_})$$
$$= G_{m(IMON)} \times I_{LOAD} \times R_{SENSE}$$

where $G_{m(IMON)}$ is the transconductance-amplifier gain, as defined in the *Electrical Characteristics* section (5.12µA/mV typ).

An external resistor (R_{IMON}) between IMON and AGND sets the current monitor output voltage:

$$V_{IMON} = I_{IMON} \times R_{IMON}$$

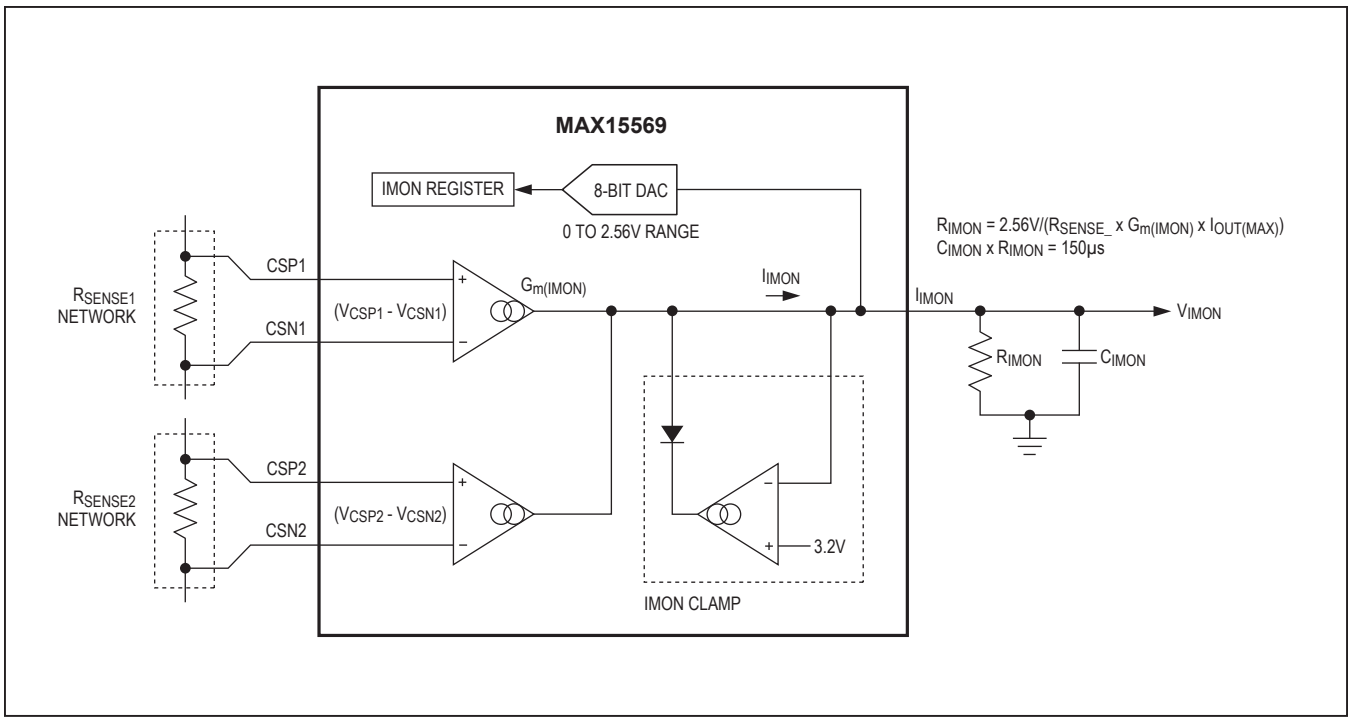


Figure 5. IMON Network

where R_{SENSE} is the value of the effective current-sense resistance. Choose R_{IMON} so that V_{IMON} is 2.56V at the full load current.

C_{IMON} is the IMON averaging capacitor. IMON is sampled every 400µs. Choose C_{IMON} such that R_{IMON} x C_{IMON} gives a time constant of approximately 150µs (see Figure 5).

The IMON voltage is internally clamped to a maximum 3.2V (typ), preventing the IMON output from exceeding the IMON voltage rating even under overload or short-circuit conditions. IMON is high impedance when in shutdown.

Feedback Adjustment Amplifier

Load-Line Amplifier (Steady State and AC Droop)

The device includes a transconductance amplifier for controlling the load-line regardless of the sense impedance value. The input signal of the amplifier is the sum of the current-sense voltages (V_{CSP1}, V_{CSN1}, and V_{CSP2}, V_{CSN2}), which differentially sense the current-sense voltage. See Figure 6.

The AC-droop amplifier output (FBAC) connects to the remote-sense point of the output through a resistor network (R_{DROOP}) that sets the DC and AC current-loop gain:

$$V_{OUT} = V_{TARGET} - (R_{DROOP} \times I_{FBAC})$$

where the target voltage (V_{TARGET}) is defined in the *Nominal Output-Voltage Selection* section, and FBAC amplifier's output current (I_{FBAC}) is determined by the current-sense voltage:

$$I_{FBAC} = G_{m(FBAC)} \times \Sigma(V_{CSP\_} - V_{CSN\_})$$

where $G_{m(FBAC)}$ = 1.2µA/mV (typ), as defined in the *Electrical Characteristics* section. Since the feedback voltage (V_{FB}) is regulated to the SETVOUT voltage, the output voltage changes in response to the FBAC current (I_{FBAC}) to create a load-line with accuracy defined by the characteristics of the R_{DROOP} network and $G_{m(FBAC)}$.

The device supports flexible combinations of AC and DC load-lines: An AC load-line > DC load-line, an AC load-line = DC load-line, and an AC load-line < DC load-line.

- The effective impedance (Z_{FBAC}) between the output of the load-line transconductance amplifier (FBAC) and the positive side of the remote-sensed output voltage sets the transient AC droop.
- The effective impedance (Z_{FB}) between the feedback-sense input (FB) and the positive side of the feedback remote sense sets the static (DC) droop.

- A capacitor from FBAC to FB (C_{FBAC}) couples the AC ripple from the output of the load-line transconductance amplifier to the feedback sense input.
- An integrator on FB corrects for output ripple and ground-sense offset (see Figure 6).

When the device is used with differential current sensing:

$$R_{LL} \approx R_{DROOP} \times R_{SENSE} \times G_{m(FBAC)}$$

where R_{LL} is the load-line, R_{SENSE} is the effective current-sense resistance across CSP_ and CSN_. R_{DROOP} is the effective resistance between the FBAC output (for AC droop) or the FB input (for DC droop) and the positive side of the remote-sensed output voltage. See Table 2 for AC- and DC-droop settings circuit configuration.

When the inductor's DCR is used as the current-sense element, the current-sense inputs should include an NTC thermistor to minimize the temperature dependence of the load-line variation due to the DCR temperature coefficient. FBAC and FB are high impedance in shutdown.

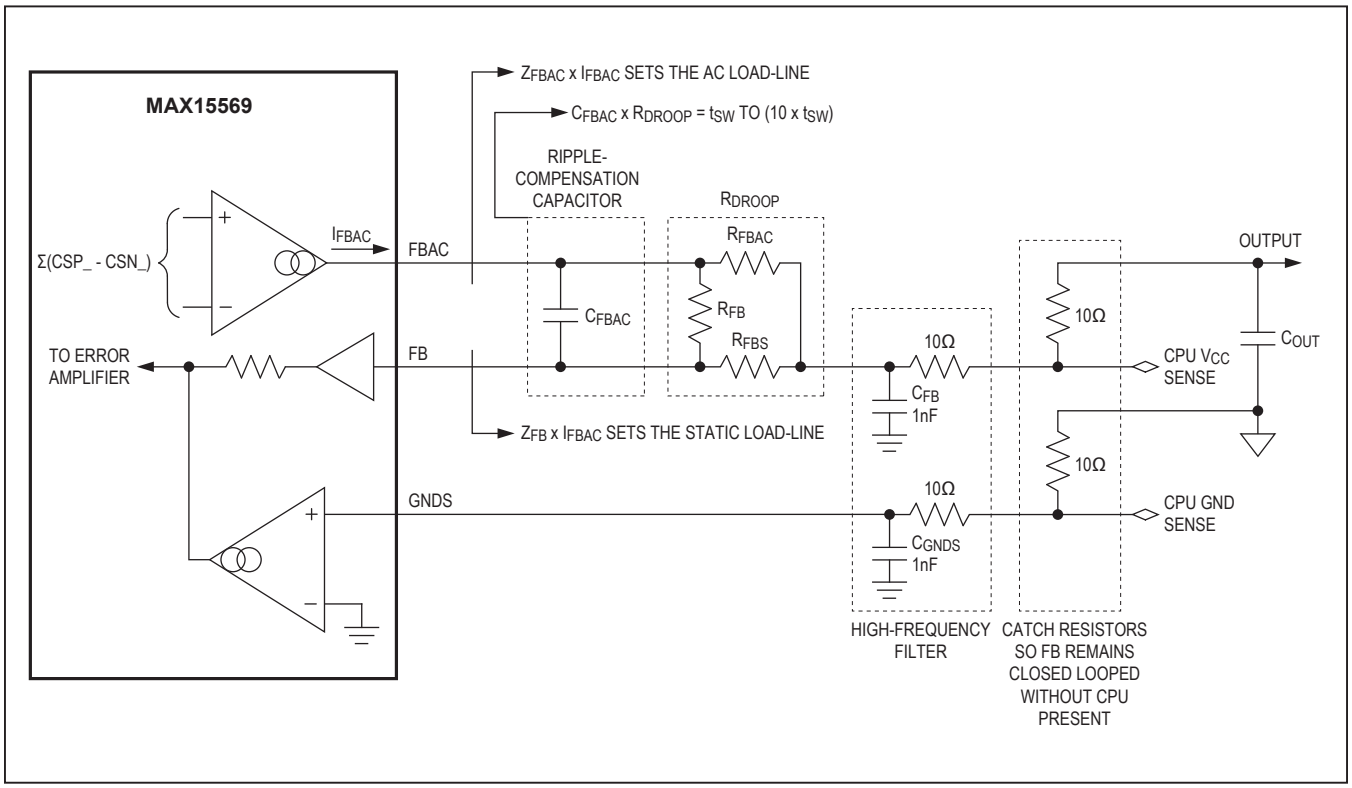


Figure 6. FB Network (Load-Line Control and Remote Sensing)

Table 2. AC-Droop and DC-Droop Settings

DC LOAD-LINE (mV/A)	AC LOAD-LINE (mV/A)	R_{DROOP_AC}	R_{DROOP_DC}	R_{FB}	C_{FBAC}	NOTE
0	R_{LL_AC}	$R_{FBAC} \| R_{FBS}$*	0Ω	Open	C_{FBAC}	$R_{FBAC} = R_{FBS}$*
R_{LL_DC}	R_{LL_AC}	R_{FBS}* + R_{FB} (R_{FBAC} = open)	R_{FBS}* (R_{FBAC} = open)	R_{FB}	C_{FBAC}	DC load-line < AC load-line
R_{LL}	R_{LL}	Open	R_{FBS}*	0Ω	Open	DC load-line = AC load-line

**See Figure 6.*

Differential Output-Voltage Remote Sense

The device includes differential, remote-sense inputs to eliminate the effects of voltage drops along the PCB traces and through the power pins of the processor. The feedback-sense node connects to the load-line resistor/capacitor network (R_{DROOP}/C_{FBAC}). The ground-sense (GNDS) input connects to an amplifier that adjusts the feedback voltage to counteract the voltage drop in the ground plane. Connect the load-line resistor (R_{DROOP}) and ground-sense (GNDS) input directly to the remote-sense outputs of the processor, as shown in Figure 6. The correction range is bounded to less than ±200mV. The remote-sense lines draw less than ±0.5µA to minimize the offset errors.

Steady-State Integrator Amplifier

The device utilizes internal integrator amplifiers that force the DC average of the FB voltage to equal the target voltage, allowing accurate DC output-voltage regulation regardless of the output voltage. The integrator is designed to correct for the steady-state offsets/errors.

Nominal Output-Voltage Selection

The nominal no-load output voltage (V_{TARGET}) is defined by the selected voltage reference, plus the remote ground-sense adjustment (V_{GNDS}), as defined in the following equation:

$$V_{TARGET} = V_{FB} - V_{DAC} + V_{GNDS}$$

where V_{DAC} is the selected output voltage.

On startup, the device slews the target voltage from ground to the default 1V boot voltage unless a different voltage code is selected before EN is pulled high.

Dynamic Output-Voltage Transitions

The device's transition time depends on the slew-rate setting, the selected SETVOUT voltage difference, and the accuracy of the slew-rate controller (see the slew rate section in the *Electrical Characteristics* section). The slew rate is not dependent on the total output capacitance, as long as the required transition current plus existing load current remains below the current limit. For dynamic VID transitions, the transition time (t_{TRAN}) is given by:

$$t_{TRAN} = \frac{|V_{NEW} - V_{OLD}|}{\left(\frac{dV_{TARGET}}{dt}\right)}$$

where dV_{TARGET}/dt is the slew rate (register 0x06h), V_{OLD} is the original output voltage, and V_{NEW} is the new target voltage (see Table 3).

Table 3. Output-Voltage Selection

LINE	BIT 7*	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	HEX	VOLTAGE
0	X	0	0	0	0	0	0	0	00h	0.000
1	X	0	0	0	0	0	0	1	01h	0.500
2	X	0	0	0	0	0	1	0	02h	0.510
3	X	0	0	0	0	0	1	1	03h	0.520
4	X	0	0	0	0	1	0	0	04h	0.530
5	X	0	0	0	0	1	0	1	05h	0.540
6	X	0	0	0	0	1	1	0	06h	0.550
7	X	0	0	0	0	1	1	1	07h	0.560
8	X	0	0	0	1	0	0	0	08h	0.570
9	X	0	0	0	1	0	0	1	09h	0.580
10	X	0	0	0	1	0	1	0	0Ah	0.590
11	X	0	0	0	1	0	1	1	0Bh	0.600
12	X	0	0	0	1	1	0	0	0Ch	0.610
13	X	0	0	0	1	1	0	1	0Dh	0.620
14	X	0	0	0	1	1	1	0	0Eh	0.630
15	X	0	0	0	1	1	1	1	0Fh	0.640
16	X	0	0	1	0	0	0	0	10h	0.650
17	X	0	0	1	0	0	0	1	11h	0.660

Table 3. Output-Voltage Selection (continued)

LINE	BIT 7*	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	HEX	VOLTAGE
18	X	0	0	1	0	0	1	0	12h	0.670
19	X	0	0	1	0	0	1	1	13h	0.680
20	X	0	0	1	0	1	0	0	14h	0.690
21	X	0	0	1	0	1	0	1	15h	0.700
22	X	0	0	1	0	1	1	0	16h	0.710
23	X	0	0	1	0	1	1	1	17h	0.720
24	X	0	0	1	1	0	0	0	18h	0.730
25	X	0	0	1	1	0	0	1	19h	0.740
26	X	0	0	1	1	0	1	0	1Ah	0.750
27	X	0	0	1	1	0	1	1	1Bh	0.760
28	X	0	0	1	1	1	0	0	1Ch	0.770
29	X	0	0	1	1	1	0	1	1Dh	0.780
30	X	0	0	1	1	1	1	0	1Eh	0.790
31	X	0	0	1	1	1	1	1	1Fh	0.800
32	X	0	1	0	0	0	0	0	20h	0.810
33	X	0	1	0	0	0	0	1	21h	0.820
34	X	0	1	0	0	0	1	0	22h	0.830
35	X	0	1	0	0	0	1	1	23h	0.840
36	X	0	1	0	0	1	0	0	24h	0.850
37	X	0	1	0	0	1	0	1	25h	0.860
38	X	0	1	0	0	1	1	0	26h	0.870
39	X	0	1	0	0	1	1	1	27h	0.880
40	X	0	1	0	1	0	0	0	28h	0.890
41	X	0	1	0	1	0	0	1	29h	0.900
42	X	0	1	0	1	0	1	0	2Ah	0.910
43	X	0	1	0	1	0	1	1	2Bh	0.920
44	X	0	1	0	1	1	0	0	2Ch	0.930
45	X	0	1	0	1	1	0	1	2Dh	0.940
46	X	0	1	0	1	1	1	0	2Eh	0.950
47	X	0	1	0	1	1	1	1	2Fh	0.960
48	X	0	1	1	0	0	0	0	30h	0.970
49	X	0	1	1	0	0	0	1	31h	0.980
50	X	0	1	1	0	0	1	0	32h	0.990
51	X	0	1	1	0	0	1	1	33h	1.000
52	X	0	1	1	0	1	0	0	34h	1.010
53	X	0	1	1	0	1	0	1	35h	1.020
54	X	0	1	1	0	1	1	0	36h	1.030
55	X	0	1	1	0	1	1	1	37h	1.040

Table 3. Output-Voltage Selection (continued)

LINE	BIT 7*	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	HEX	VOLTAGE
56	X	0	1	1	1	0	0	0	38h	1.050
57	X	0	1	1	1	0	0	1	39h	1.060
58	X	0	1	1	1	0	1	0	3Ah	1.070
59	X	0	1	1	1	0	1	1	3Bh	1.080
60	X	0	1	1	1	1	0	0	3Ch	1.090
61	X	0	1	1	1	1	0	1	3Dh	1.100
62	X	0	1	1	1	1	1	0	3Eh	1.110
63	X	0	1	1	1	1	1	1	3Fh	1.120
64	X	1	0	0	0	0	0	0	40h	1.130
65	X	1	0	0	0	0	0	1	41h	1.140
66	X	1	0	0	0	0	1	0	42h	1.150
67	X	1	0	0	0	0	1	1	43h	1.160
68	X	1	0	0	0	1	0	0	44h	1.170
69	X	1	0	0	0	1	0	1	45h	1.180
70	X	1	0	0	0	1	1	0	46h	1.190
71	X	1	0	0	0	1	1	1	47h	1.200
72	X	1	0	0	1	0	0	0	48h	1.210
73	X	1	0	0	1	0	0	1	49h	1.220
74	X	1	0	0	1	0	1	0	4Ah	1.230
75	X	1	0	0	1	0	1	1	4Bh	1.240
76	X	1	0	0	1	1	0	0	4Ch	1.250
77	X	1	0	0	1	1	0	1	4Dh	1.260
78	X	1	0	0	1	1	1	0	4Eh	1.270
79	X	1	0	0	1	1	1	1	4Fh	1.280
80	X	1	0	1	0	0	0	0	50h	1.290
81	X	1	0	1	0	0	0	1	51h	1.300
82	X	1	0	1	0	0	1	0	52h	1.310
83	X	1	0	1	0	0	1	1	53h	1.320
84	X	1	0	1	0	1	0	0	54h	1.330
85	X	1	0	1	0	1	0	1	55h	1.340
86	X	1	0	1	0	1	1	0	56h	1.350
87	X	1	0	1	0	1	1	1	57h	1.360
88	X	1	0	1	1	0	0	0	58h	1.370
89	X	1	0	1	1	0	0	1	59h	1.380
90	X	1	0	1	1	0	1	0	5Ah	1.390
91	X	1	0	1	1	0	1	1	5Bh	1.400
92	X	1	0	1	1	1	0	0	5Ch	1.410
93	X	1	0	1	1	1	0	1	5Dh	1.420

Table 3. Output-Voltage Selection (continued)

LINE	BIT 7*	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	HEX	VOLTAGE
94	X	1	0	1	1	1	1	0	5Eh	1.430
95	X	1	0	1	1	1	1	1	5Fh	1.440
96	X	1	1	0	0	0	0	0	60h	1.450
97	X	1	1	0	0	0	0	1	61h	1.460
98	X	1	1	0	0	0	1	0	62h	1.470
99	X	1	1	0	0	0	1	1	63h	1.480
100	X	1	1	0	0	1	0	0	64h	1.490
101	X	1	1	0	0	1	0	1	65h	1.500
102	X	1	1	0	0	1	1	0	66h	1.510
103	X	1	1	0	0	1	1	1	67h	1.520
104	X	1	1	0	1	0	0	0	68h	1.530
105	X	1	1	0	1	0	0	1	69h	1.540
106	X	1	1	0	1	0	1	0	6Ah	1.550
107	X	1	1	0	1	0	1	1	6Bh	1.560
108	X	1	1	0	1	1	0	0	6Ch	1.570
109	X	1	1	0	1	1	0	1	6Dh	1.580
110	X	1	1	0	1	1	1	0	6Eh	1.590
111	X	1	1	0	1	1	1	1	6Fh	1.600
112	X	1	1	1	0	0	0	0	70h	1.610
113	X	1	1	1	0	0	0	1	71h	1.620
114	X	1	1	1	0	0	1	0	72h	1.630
115	X	1	1	1	0	0	1	1	73h	1.640
116	X	1	1	1	0	1	0	0	74h	1.650
117	X	1	1	1	0	1	0	1	75h	1.660
118	X	1	1	1	0	1	1	0	76h	1.670
119	X	1	1	1	0	1	1	1	77h	1.680
120	X	1	1	1	1	0	0	0	78h	1.690
121	X	1	1	1	1	0	0	1	79h	1.700
122	X	1	1	1	1	0	1	0	7Ah	1.710
123	X	1	1	1	1	0	1	1	7Bh	1.720
124	X	1	1	1	1	1	0	0	7Ch	1.730
125	X	1	1	1	1	1	0	1	7Dh	1.740
126	X	1	1	1	1	1	1	0	7Eh	1.750
127	X	1	1	1	1	1	1	1	7Fh	1.760

**Bit 7 is ignored (don't care), but listed here to match the VOUTMAX register.*
X = Don't care.
***Note:** DAC codes above 1.6V are not advised due to proximity to the overvoltage threshold.*

Soft-start uses the slow slew rate, as set by the default setting in the SRREG register, which is a fraction of the fast slew rate. See the slew-rate accuracy specification in the *Electrical Characteristics* section. The average inductor current per phase that is required to make an output-voltage transition is given by:

$$I_L = \frac{C_{OUT}}{N_{PH}} \times \frac{dV_{TARGET}}{dt}$$

where dV_{TARGET}/dt is the required slew rate, C_{OUT} is the total output capacitance, and N_{PH} is the number of active phases.

At the beginning of an output-voltage transition, the device blanks the $\overline{INT}$, so the open-drain output enters a high-impedance state during output-voltage transitions. The controller releases the $\overline{INT}$ output approximately 4µs (typ) after the slew-rate controller reaches the target output voltage.

Automatic Pulse-Skipping Operation

The device automatically operates with a 2-phase pulse-skipping control scheme. A logic-low level on $\overline{DRVSKP}$ enables the zero-crossing comparator of the driver (MAX17492) or power stage (MAX15515). Therefore, these devices disable their low-side MOSFETs when they detect “zero” inductor current. This keeps the inductor from discharging the output capacitors and forces the controller to skip pulses under light-load conditions to avoid overcharging the output.

If the system changes the VID code to a lower voltage, the device drives $\overline{DRVSKP}$ high to disable the pulse-skipping mode. This allows the regulator to actively discharge the output at the programmed slew rate.

To disable pulse-skipping mode so the regulator continually operates in forced-PWM operation, leave $\overline{DRVSKP}$ unconnected and connect the pulse-skipping control input on the driver or power stage to ground.

Automatic Pulse-Skipping Switchover

In pulse-skipping mode, an inherent automatic switchover to PFM takes place at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current’s zero crossing. The zero-crossing detection is designed into the MAX17492 driver and the MAX15515 power stage. They sense the inductor current across the low-side MOSFET. Once the LX voltage crosses the zero-crossing comparator threshold, the low-side MOSFET turns off. This mechanism causes the threshold between pulse-skipping PFM and non-skipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation. The PFM/PWM crossover occurs when the load current of each phase is equal to 1/2 the peak-to-peak ripple current that is a function of the inductor value. Even for wide 4.5V to 14V input voltage ranges, this crossover is relatively constant, with only a minor dependence on the input voltage due to the typically low duty cycles. The total load current at the PFM/PWM crossover threshold ($I_{LOAD(SKIP)}$) is approximately:

$$I_{LOAD(SKIP)} = \frac{(V_{IN}-V_{OUT})\,t_{ON}}{2L}$$

Power-Up Sequence (POR, UVLO)

Power-on reset (POR) occurs when V_{BIAS} and V_{TT} rise above approximately 2V. POR resets the fault latch and loads the default register settings. The V_{BIAS} UVLO circuitry inhibits switching until V_{BIAS} rises above 4.5V. The controller powers up the reference once the system enables the controller, V_{BIAS} is above 4.5V, and EN is driven high (see Figure 2). With the reference in regulation, the controller ramps up to the selected output voltage (register 0x07h) at the selected slow slew rate (register 0x06h)

After this initialization, the PWM controller begins switching:

$$t_{TRAN(START)} = \frac{V_{BOOT}}{(dV_{TARGET}/dt)}$$

where dV_{TARGET}/dt is the slew rate. The soft-start slew rate is the slow slew rate set by the default setting in the SRREG register. The soft-start circuitry does not use a variable current limit, so full output current is available immediately.

Interrupt ($\overline{INT}$)

The device provides an active-low interrupt output ($\overline{INT}$) to indicate that the startup sequence is complete and the output voltage has moved to the programmed VID value. This signal is intended for system monitoring of the device. $\overline{INT}$ remains high impedance during normal DC-DC operation. The controller asserts $\overline{INT}$ to alert the system of an alarm event or if a fault condition occurs. See the *Alarms* and *Fault Protection (Latched)* sections for details (and Figure 7).

Use an external pullup resistor between $\overline{INT}$ and 3.3V to deliver a valid logic-level output.

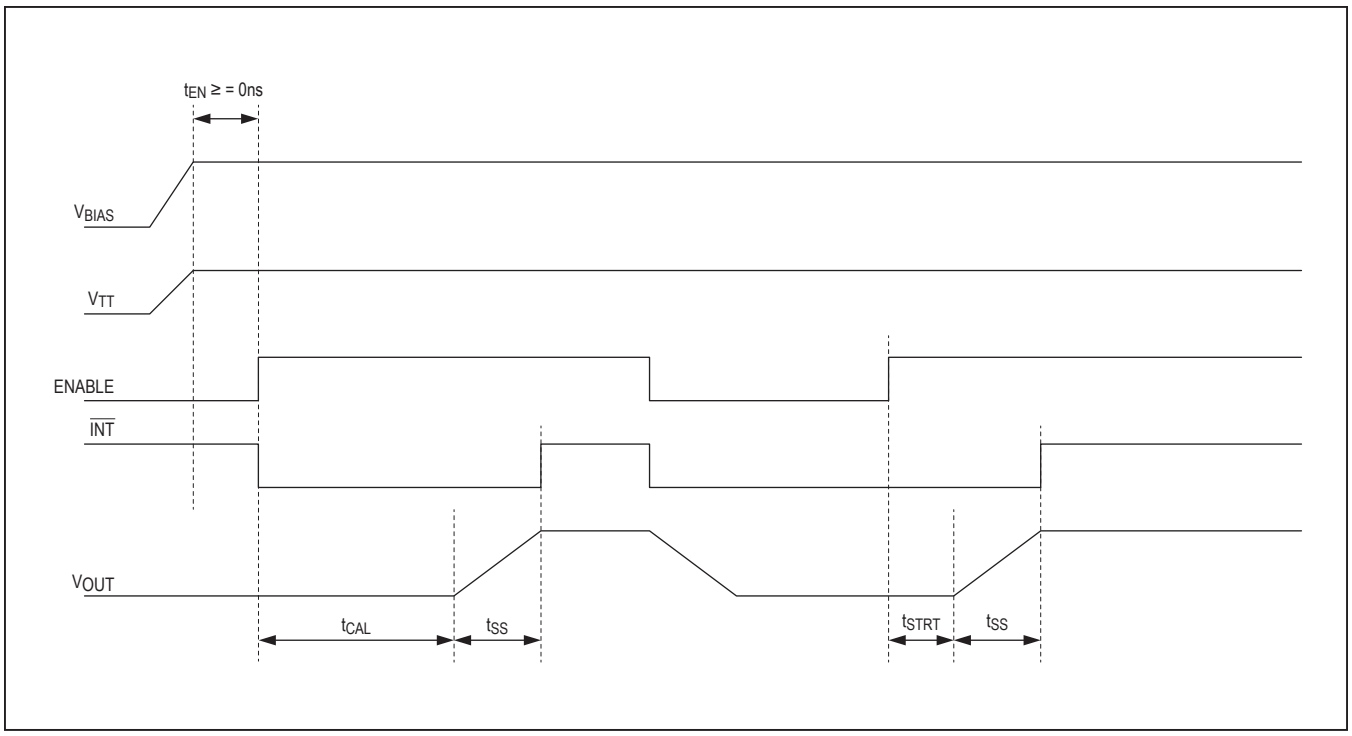


Figure 7. Startup Sequence

Alarms

Temperature Comparator (VRHOT)

The device features an independent comparator with input at THERM. This comparator has an accurate threshold of 0.5 x V_{BIAS}. Use a 100kΩ NTC with a β of 4250K. The NTC resistance drops to 5.68kΩ when the temperature reaches +100°C. The NTC forms a divider with the internal 5.35kΩ pullup resistance, so the voltage drops below the 0.5 x V_{BIAS} threshold. VRHOT is then asserted.

The internal 5.35kΩ resistor is disconnected in shutdown, saving power.

Overcurrent Warning (OC)

The device includes an overcurrent-warning threshold that samples the phase 1 current-sense signal before each phase 1 on-time. When the CSP1 - CSN1 voltage exceeds the 23mV (typ) threshold, the status bit (D2) in register 0x04h) is asserted. If the warning is not masked, the controller asserts the $\overline{INT}$ output to alert the system to the overcurrent condition.

The fixed 23mV OC_ALARM threshold is 15mV lower than the valley current-limit threshold to provide sufficient design margin before the regulator limits the output current. Additionally, the controller includes a IMON register that can be monitored by the system.

Output-Code Violation (VOUTMAX)

The controller includes a maximum output register (VOUTMAX register 0x02h) to protect against target output voltage codes that could violate the absolute maximum rating of the load. The value of this configuration register limits the output range. If a target output voltage is loaded into register 0x07h, the regulator sets the appropriate status bit. If the warning is not masked, the controller asserts the $\overline{INT}$ output to alert the system to the overcurrent condition. The output voltage attempts to ramp to the new target, but the regulator effectively clamps the output to the VOUTMAX voltage to avoid an overvoltage condition. See the *I²C Commands and Registers* section for additional details.

Fault Protection (Latched)

TON Open-Circuit Protection

The TON input includes open-circuit protection to avoid long, uncontrolled on-times that could result in an overvoltage condition on the output. The device detects an open-circuit fault if the TON current drops below 6µA (typ) for any reason (e.g., the TON resistor (R_{TON}) is unpopulated, a high-resistance value is used, the input voltage is low, etc.). Under these conditions, the device stops switching (DRVPWM_ outputs become high impedance and $\overline{DRVSKP}$ is pulled low) and immediately sets the fault latch.

Toggle EN or cycle power (BIAS) below 1V to clear the fault latch and reactivate the controller. The TON open-circuit fault is not indicated in the STATUS register.

Output Overvoltage Protection (OVP)

The OVP circuit is designed to protect the load against a shorted high-side MOSFET by drawing high current and activating the adapter or battery protection circuits. The device continuously monitors the output for an overvoltage fault. An OVP fault is detected if the output voltage exceeds the VID DAC voltage by more than 300mV (min), or the fixed 1.83V (typ) threshold during a downward VID transition in skip mode.

During pulse-skipping operation, the OVP threshold tracks the VID DAC voltage as soon as the output is in regulation; otherwise, the fixed 1.83V (typ) threshold is used. When the OVP circuit detects an overvoltage fault, the DRVPWM_ outputs become high impedance and the $\overline{DRVSKP}$ output is pulled high. OVP is disabled in the standby power state (EN pulled low).

After the fault condition occurs, the I²C interface remains active so the STATUS register can be read to determine what triggered the fault. Toggle EN or cycle power (BIAS) below 1V to clear the fault latch. With the fault latch cleared and the fault condition removed, the regulator powers back up and the fault conditions are deasserted in the STATUS register.

Output Undervoltage Protection (UVP)

If the output voltage is 200mV (min) below the target voltage and stays below this level for 200µs (typ), the controller activates the shutdown sequence. The regulator turns on a 2kΩ discharge resistor and sets the fault latch. DRVPWM_ outputs go to the high-impedance mode and $\overline{DRVSKP}$ is pulled low.

After the fault condition occurs, the I²C interface remains active so the STATUS register can be read to determine what triggered the fault. Toggle EN or cycle power (BIAS) below 1V to clear the fault latch. With the fault latch cleared and the fault condition removed, the regulator powers back up and the fault conditions are deasserted in the STATUS register.

Thermal-Fault Protection (TSHDN)

The device features an internal thermal-fault protection circuit. When the junction temperature rises above +160°C, a thermal sensor sets the fault latch and DRVPWM_ becomes high impedance.

After the fault condition occurs, the I²C interface remains active so the STATUS register can be read to determine what triggered the fault. Toggle EN or cycle power (BIAS) below 1V to clear the fault latch. With the fault latch cleared, the regulator powers back up and the fault conditions are deasserted in the STATUS register, as long as the regulator has cooled by 15°C (typ).

External Driver and Disabling Phases

The device supports an external driver (MAX15515) for both phases. The DRVPWM_ outputs provide the signals to trigger the drivers. Connecting CSP2 to BIAS of the device disables the second phase.

The device provides a pulse-skipping-mode control output ($\overline{DRVSKP}$) for the external driver control. $\overline{DRVSKP}$ goes high when the controller detects an output overvoltage-fault condition. $\overline{DRVSKP}$ is high during output-voltage transitions. The $\overline{DRVSKP}$ output is unconnected in shutdown.

I²C Interface, Commands, Registers, and Digital Control

A simplified register summery of the I²C interface for the device is shown in Table 4. The I²C interface consists of a high-speed transceiver capable of 3.4MHz data rate.

Regulator Address

The device does not feature programmable addressing. These devices are hard-coded with bus **address 70h**.

Table 4. I²C Command and Data Register Summary

COMMAND		MASTER PAYLOAD	SLAVE PAYLOAD	DESCRIPTION
HEX	NAME	WRITE	READ	
00h	—	—	—	Reserved.
01h	—	—	—	Reserved.
02h	VOUTMAX	Configures maximum output code	Returns maximum output code	The maximum allowable output voltage (0.510V to 1.76V) that can be set by user. In case the I²C interface receives a set voltage command higher than the VOUTMAX value, the regulator slews the output to VOUTMAX set voltage. Default is 51h (1.3V).
03h	—	—	—	Reserved.
04h	STATUS	—	Regulator status	Bits D[5:0] of this register consist of the VRHOT flag (bit D5), undervoltage flag (bit D4), overvoltage flag (bit D3), overcurrent flag (bit D2), VOUTMAX flag (bit D1), and $\overline{INT}$ flag (bit D0). Bits D[7:6] are not used and return 0. For a detailed description, see the *Regulator Status (0x04h)* section. The STATUS register is set regardless of the MASK register (0x05) content.
05h	MASK	Configures mask status	Current mask status	Writing to this register prevents the assertion of the $\overline{INT}$ output when the specific fault or alarm is masked. This register does not mask the STATUS register indication. Default is 00h (no masking).
06h	SLEW_RATE	Configures the output-voltage slew rate	Returns the output-voltage slew rate	Writing to this register sets the slew rate (volt/second) of the output voltage during the initial startup and dynamic output-voltage transitions. Default is 04h (4.5mV/µs for soft-start and 9mV/µs for dynamic transitions).
07h	SETVOUT	Selects the output code	Returns the output code	The 07h command sets the target output voltage. The regulator transitions up or down to the new output voltage 0.5µs after the command is acknowledged. Default is 33h (1V).
08h	IMON	—	Returns the output current value	This register returns the average output current value. IMON is updated every 400µs.

I²C Commands and Registers

The device supports the following commands and registers shown in Table 4.

VOUTMAX Control (0x02h)

This register is programmed by the bus master to the maximum output voltage the regulator is allowed to support. Any attempts to set the SETVOUT above VOUTMAX are acknowledged by setting the output voltage to the content of the VOUTMAX register. The default value is 51h (1.3V). See Table 5 for bit descriptions.

Regulator Status (0x04h)

This register consists of six flags that determine the status of the regulator in case of thermal warning, overvoltage fault, undervoltage fault, output overcurrent warning, and maximum output violation. The $\overline{INT}$ bit (D0) is asserted in case of any unmasked event. See Table 6 for bit descriptions.

1) The VRHOT bit (D5) is set when the voltage at THERM pin goes below its nominal threshold (see the *Electrical Characteristics* section).
2) The UV bit (D4) is set when the output voltage drops 200mV lower than SETVOUT value for 200µs.

Table 5. VOUTMAX (Maximum Output Voltage Allowed)

I²C COMMAND	DEFAULT	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
0x02h	0x51h		VMAX_7	VMAX_6	VMAX_5	VMAX_4	VMAX_3	VMAX_2	VMAX_1	VMAX_0
BIT	**NAME**		**DESCRIPTION**							
D7	VMAX_7	R/W	Don't care bit. Returns 0 when read.							
D6	VMAX_6	R/W	MSB of the maximum allowed output voltage code.							
D5	VMAX_5	R/W	—							
D4	VMAX_4	R/W	—							
D3	VMAX_3	R/W	—							
D2	VMAX_2	R/W	—							
D1	VMAX_1	R/W	—							
D0	VMAX_0	R/W	LSB of the maximum allowed output voltage code. 10mV resolution.							

Table 6. STATUS (Regulator Status)

I²C COMMAND	DEFAULT	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
0x04h	0x00h		X	X	VRHOT	UV	OV	OC	VMERR	INT#
BIT	**NAME**		**DESCRIPTION**							
D7	—	R	Always reads 0.							
D6	—	R	Always reads 0.							
D5	VRHOT	R	VRHOT							
D4	UV	R	UV (V_{OUT} undervoltage)							
D3	OV	R	OV (V_{OUT} overvoltage)							
D2	OC	R	OC (output current over current limit). This bit is sticky and cleared when read if the OC fault is no longer present.							
D1	VMERR	R	VOUTMAX error. Set = 1 if (VID > VOUTMAX)							
D0	$\overline{INT}$	R	NORed bits D[5:1], read-only, sets the $\overline{INT}$ output.							

X = Don't care.

3) The OV bit (D3) is set when the output voltage rises 300mV above (or 1.83V fixed) the output voltage.
4) The OC bit (D2) is set when the valley of (∑CSP1 - CSN1) current signal exceeds 23mV (OC_ALARM). The current-limit protection threshold is 15mV higher than the OC_ALARM.
5) The VMERR bit (D1) is set in case the SETVOUT exceeds the content of VOUTMAX. Changing SETVOUT to values lower than VOUTMAX clears the VMERR warning.
6) Masking of the status bit only prevents the $\overline{INT}$ bit (D0) from being set by the specific status bit. The status bit is still set if the fault occurs, regardless of the status mask setting. The OC bit (D2) is sticky, but it does not hold $\overline{INT}$ low when the OC fault goes away. This allows the system to determine what event triggered $\overline{INT}$ to go low. All other fault bits are not sticky. Reading the register after the OC event clears the flag.

Mask Status (0x05h)

Masking of the status bit only prevents the $\overline{INT}$ bit (D0) from being set by the specific status bit. The status bit is still set if the fault occurs, regardless of the Status Mask setting. See Table 7 for bit descriptions.

Table 7. MASK (Regulator Status Mask Register)

I²C COMMAND	DEFAULT	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
0x05h	0x00h		X	X	VRHMSK	UVMSK	OVMSK	OCMSK	VMERRMSK	Reserved
BIT	**NAME**		**DESCRIPTION**							
D7	—	R	Always reads 0.							
D6	—	R	Always reads 0.							
D5	VRHMSK	R/W	VRHOT masking bit.							
D4	UVMSK	R/W	Undervoltage-fault masking bit.							
D3	OVMSK	R/W	Overvoltage-fault masking bit.							
D2	OCMSK	R/W	Overcurrent-fault masking bit.							
D1	VMERRMSK	R/W	VOUTMAX error masking bit.							
D0	—	R	Always reads 0.							

X = Don't care.

Note: *In the event of UV, OC, OV, VRHOT, or VMERR, the signal is ANDed by the complement of the MASK register content.*

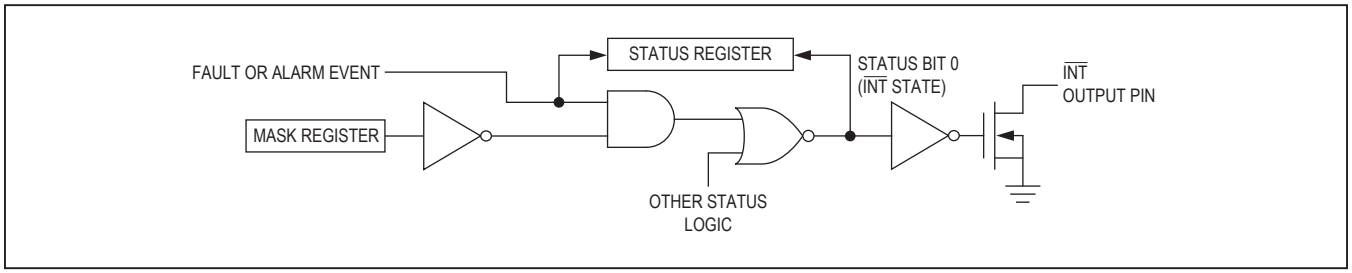


Figure 8. Status Bit Masking

Table 8. SRREG (Slew-Rate Setting Register)

I²C COMMAND	DEFAULT	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
0x06h	0x04h		X	X	SRREG_5	SRREG_4	SRREG_3	SRREG_2	SRREG_1	SRREG_0
BIT	**NAME**		**DESCRIPTION**							
D7	—	R/W	See Table 9							
D6	—	R/W	See Table 9							
D5	SRREG_5	R/W	See Table 9							
D4	SRREG_4	R/W	See Table 9							
D3	SRREG_3	R/W	See Table 9							
D2	SRREG_2	R/W	See Table 9							
D1	SRREG_1	R/W	See Table 9							
D0	SRREG_0	R/W	See Table 9							

X = Don't care.

Slew-Rate Configuration (0x06h)

The content of the SRREG register determines the slew rate at both initial startup and dynamic output-voltage transition. There are 52 possibilities of selectable slew rates (4.5mV/µs to 44mV/µs) that cover the initial startup (soft-start) and dynamic output-voltage transition with different slew rates in one setting. See Table 8 for bit descriptions and Table 9 for slew-rate selections.

Table 9. Slew-Rate Selections (Register 0x06h)

D7	D6	D5	D4	D3	D2	D1	D0	SOFT-START SLEW RATE (mV/µs)	REGULAR SLEW RATE (mV/µs)
X	X	0	0	0	0	0	0	18	18
X	X	0	0	0	0	0	1	9	18
X	X	0	0	0	0	1	0	4.5	18
X	X	0	0	0	0	1	1	9	9
X	**X**	**0**	**0**	**0**	**1**	**0**	**0**	**4.5***	**9***
X	X	0	0	0	1	0	1	36	36
X	X	0	0	0	1	1	0	18	36
X	X	0	0	0	1	1	1	9	36
X	X	0	0	1	0	0	0	4.5	36
X	X	0	0	1	0	0	1	4.5	4.5
X	X	0	0	1	0	1	X	**4.5**	**9**
X	X	0	0	1	1	0	X	**4.5**	**9**
X	X	0	0	1	1	1	0	**4.5**	**9**
X	X	0	1	0	0	0	0	22	22
X	X	0	1	0	0	0	1	11	22
X	X	0	1	0	0	1	0	5.5	22
X	X	0	1	0	0	1	1	11	11
X	X	0	1	0	1	0	0	5.5	11
X	X	0	1	0	1	0	1	44	44
X	X	0	1	0	1	1	0	22	44
X	X	0	1	0	1	1	1	11	44
X	X	0	1	1	0	0	0	5.5	44
X	X	0	1	1	0	0	1	5.5	5.5
X	X	0	1	1	0	X	X	**5.5**	**11**
X	X	0	1	1	1	1	0	**5.5**	**11**
X	X	1	0	0	0	0	0	14	14
X	X	1	0	0	0	0	1	7	14
X	X	1	0	0	0	1	0	3.5	14
X	X	1	0	0	0	1	1	7	7
X	X	1	0	0	1	0	0	3.5	7
X	X	1	0	0	1	0	1	28	28

Table 9. Slew-Rate Selections (Register 0x06h) (continued)

D7	D6	D5	D4	D3	D2	D1	D0	SOFT-START SLEW RATE (mV/µs)	REGULAR SLEW RATE (mV/µs)
X	X	1	0	0	1	1	0	14	28
X	X	1	0	0	1	1	1	7	28
X	X	1	0	1	0	0	0	3.5	28
X	X	1	0	1	0	0	1	3.5	3.5
X	X	1	0	1	0	1	0	**3.5**	**7**
X	X	1	0	1	0	1	1	**3.5**	**7**
X	X	1	0	1	1	0	0	**3.5**	**7**
X	X	1	0	1	1	0	1	**3.5**	**7**
X	X	1	0	1	1	1	0	**3.5**	**7**
X	X	1	1	0	0	0	0	18	18
X	X	1	1	0	0	0	1	9	18
X	X	1	1	0	0	1	0	4.5	18
X	X	1	1	0	0	1	1	9	9
X	X	1	1	0	1	0	0	4.5	9
X	X	1	1	0	1	0	1	36	36
X	X	1	1	0	1	1	0	18	36
X	X	1	1	0	1	1	1	9	36
X	X	1	1	1	0	0	0	4.5	36
X	X	1	1	1	0	0	1	4.5	4.5
X	X	1	1	1	0	X	X	**4.5**	**9**
X	X	1	1	1	1	1	0	**4.5**	**9**

**POR default setting.*
X = Don't care.

Output-Voltage Set Register (0x07h)

The SETVOUT register slews the output voltage 0.5µs after the SETVOUT command is acknowledged. The slew rate of the change in output voltage is equal to the value set by SRREG. The device DAC supports voltages between 0.5V and 1.6V. See Table 3 for the output-voltage codes and Table 10 for bit descriptions.

Current Monitor Register (0x08h)

The device includes a current monitoring function. An internal ADC converts the analog signals from the IMON pin output to 8-bit values in the IMON register. The ADC converter filters the current-sense signal by averaging over four samples. The acquisition rate is 100µs. The content of this register is updated every 400µs. For more information on how to set the desired value for IMON resolution, see the *Current Monitoring (IMON)* section. See Table 11 for bit descriptions.

Table 10. SETVOUT (Output-Voltage Set Register)

I²C COMMAND	DEFAULT	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
0x07	0x33		VID_7	VID_6	VID_5	VID_4	VID_3	VID_2	VID_1	VID_0
BIT	**NAME**		**DESCRIPTION**							
D7	VID_7	R	Don't care bit. Returns 0 when read.							
D6	VID_6	R	MSB of the maximum allowed output voltage code							
D5	VID_5	R	See Table 3 for the actual output-voltage code.							
D4	VID_4	R								
D3	VID_3	R								
D2	VID_2	R								
D1	VID_1	R								
D0	VID_0	R	LSB of the maximum allowed output-voltage code. 10mV resolution.							

Table 11. IMON (Current Monitor Register)

I²C COMMAND	DEFAULT	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
0x08h	0x00h		—	—	—	—	—	—	—	—
BIT	**NAME**		**DESCRIPTION**							
D7	IM_7	R	—							
D6	IM_6	R	—							
D5	IM_5	R	—							
D4	IM_4	R	—							
D3	IM_3	R	—							
D2	IM_2	R	—							
D1	IM_1	R	—							
D0	IM_0	R	—							

Multiphase QuickTune-PWM Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

1) **Input Voltage Range:** The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case high AC adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest input voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.
2) **Maximum Load Current:** There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements, and drives output-capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous-load current (I_{LOAD}) determines the thermal stresses and drives the selection of the input capacitors, MOSFETs, and other critical heat-contributing components. Modern notebook CPUs generally exhibit I_{LOAD} = 0.8 x $I_{LOAD(MAX)}$. For multiphase systems, each phase supports a fraction of the load, depending on the current balancing. When properly balanced, the load current is evenly distributed among phases:

$$I_{LOAD(PHASE)} = \frac{I_{LOAD}}{N_{PH}}$$

where N_{PH} is the total number of active phases.

3) **Switching Frequency:** This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage due to MOSFET switching losses that are proportional to frequency and V_{IN}^2. The optimum frequency is also a moving target due to rapid improvements in MOSFET technology that are making higher frequencies more practical.
4) **Inductor Operation Point:** This choice provides trade-offs between size vs. efficiency and transient responses vs. output noise. Low inductor values provide better transient response and smaller physical size, but also result in lower efficiency and higher output noise due to increased ripple current. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually between 30% and 50% ripple current. For a multiphase core regulator, select an LIR value of ~0.4.

Inductor Selection

The switching frequency and operating point (% ripple current or LIR) determine the inductor value as follows:

$$L = N_{PH}\left(\frac{V_{IN} - V_{OUT}}{f_{SW} \times I_{LOAD(MAX)} \times LIR}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)$$

where N_{PH} is the total number of phases. Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The core must not saturate at the peak-inductor current (I_{PEAK}):

$$I_{PEAK} = \left(\frac{I_{LOAD(MAX)}}{N_{PH}}\right)\left(1 + \frac{LIR}{2}\right)$$

Output Capacitor Selection

Output capacitor selection is determined by the controller stability and the transient soar and sag requirements of the application.

Output Capacitor ESR

The output filter capacitor must have low enough effective series resistance (ESR) to meet output-ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. In CPU V_{CORE} converters and other applications where the output is subject to large-load transients, the size of the output capacitor typically depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$(R_{ESR} + R_{PCB}) \le \frac{V_{STEP}}{\Delta I_{LOAD(MAX)}}$$

The output-voltage ripple of a step-down controller equals the total inductor ripple current multiplied by the output capacitor's ESR. When operating multiphase out-of-phase systems, the peak inductor currents of each phase are staggered, resulting in lower output ripple voltage by reducing the total inductor ripple current. For multiphase operation, the maximum ESR to meet ripple requirements is given in the following equation:

$$R_{ESR} \le \left[\frac{V_{IN} \times f_{SW} \times L}{(V_{IN} - (N_{PH} \times V_{OUT}))V_{OUT}}\right]V_{RIPPLE}$$

where NPH is the total number of active phases and f_{SW} is the switching frequency per phase.

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. The capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true for polymer types). When using low-capacity ceramic filter capacitors, capacitor size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the V_{SAG} and V_{SOAR} equations in the *Transient Response* section).

Output Capacitor Stability Considerations

For QuickTune-PWM controllers, stability is determined by the value of the ESR zero relative to the switching frequency. The boundary of instability is given by the following equation:

$$f_{ESR} \le \frac{f_{SW}}{\pi}$$

where:

$$f_{ESR} = \frac{1}{2\pi \times R_{EFF} \times C_{OUT}}$$

and:

$$R_{EFF} = R_{ESR} + R_{LL} + R_{PCB}$$

where C_{OUT} is the total output capacitance, R_{ESR} is the total equivalent series resistance, R_{LL} is the load-line gain, and R_{PCB} is the parasitic board resistance between the output capacitors and sense resistors. For a 1MHz application, the ESR zero frequency must be well below 300kHz, preferably below 100kHz. SANYO POSCAP and Panasonic SP capacitors are widely used and have typical ESR zero frequencies below 100kHz.

Ceramic capacitors have a high-ESR zero frequency, but applications with significant load-line (DC-coupled or AC-coupled) can take advantage of their size and low ESR. When using only ceramic output capacitors, output overshoot (V_{SOAR}) typically determines the minimum output-capacitance requirement. Their relatively low capacitance value favors high-switching-frequency operation with small inductor values to minimize the energy transferred from inductor to capacitor during load-step recovery. Unstable operation manifests itself in two related but distinctly different ways: Double pulsing and feedback-loop instability.

Double Pulsing and Feedback-Loop Instability

Double pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output-voltage signal. This “fools” the error comparator into triggering a new cycle immediately after the minimum off-time period has expired. Double pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability due to insufficient ESR. Loop instability can result in oscillations at the output after line or load steps. Such perturbations are usually damped, but can cause the output voltage to rise above or fall below the tolerance limits. The easiest method for checking stability is to apply a very fast 10% to 90% maximum load transient and carefully observe the output-voltage ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under/overshoot.

Transient Response

The inductor-ripple current impacts transient-response performance, especially at low V_{IN} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The amount of output sag is also a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time. For a multiphase controller, the worst-case output sag voltage can be determined by:

$$V_{SAG} \approx \frac{L(\Delta I_{LOAD(MAX)})^2}{2N_{PH} \times C_{OUT} \times V_{OUT}} \times \frac{t_{MIN}}{[t_{SW} - t_{MIN}]}$$

and:

$$t_{MIN} = t_{ON} + t_{OFF(MIN)}$$

where $t_{OFF(MIN)}$ is the minimum off-time (see the *Electrical Characteristics* section), t_{SW} is the programmed switching period, and N_{PH} is the total number of active phases. V_{SAG} must be less than the transient droop, $\Delta I_{LOAD(MAX)} \times R_{LL}$. The capacitive soar voltage due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{(\Delta I_{LOAD(MAX)})^2 L}{2N_{PH} \times C_{OUT} \times V_{OUT}}$$

The actual peak of the soar voltage depends on the time where the decaying ESR step and rising capacitive soar are at their maximum. This is best simulated or measured.

Input Capacitor Selection

The input capacitor must meet the ripple-current requirement (I_{RMS}) imposed by the switching currents. The multiphase QuickTune-PWM controllers operate out-of phase, reducing the RMS input. The I_{RMS} requirements can be determined by the following equation:

$$I_{RMS} = \left(\frac{I_{LOAD}}{N_{PH} \times V_{IN}}\right)\sqrt{N_{PH} \times V_{OUT}\left(V_{IN} - \left(N_{PH} \times V_{OUT}\right)\right)}$$

The worst-case RMS current requirement occurs when operating with V_{IN} = 2 (N_{PH} × V_{OUT}). Therefore, the above equation simplifies to I_{RMS} = 0.5 x ($I_{LOAD/NPH}$). Choose an input capacitor that exhibits less than 10°C temperature rise at the RMS input current for optimal circuit longevity.

Applications Information

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention. If possible, mount all the power components on the top side of the board, with their ground terminals flush against one another. The layout of the device is intimately related to the layout of the CPU. The high-current output paths from the regulator must flow cleanly into the high-current inputs on the processor. For VR12.6 processors, these inputs are orthogonal. This arrangement effectively forces the regulator to be located diagonally, with respect to the processor. Refer to the MAX15569 evaluation kit specifications for layout examples and follow these guidelines for good PCB layout:

- Keep the high-current paths short, especially at the ground terminals. This is essential for stable, jitter-free operation.
- Connect all analog grounds to a separate solid-copper plane that connects to the ground pin of the QuickTune-PWM controller. This includes the V_{BIAS} bypass capacitor, FB, and GNDS bypass capacitors.
- Keep the power traces and load connections short. This is essential for high efficiency. The use of thick copper PCB (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PCB traces is a difficult task that must be approached in terms of fractions of centimeters, where a single mΩ of excess trace resistance causes a measurable efficiency penalty.
- CSP_ and CSN_ connections for current limiting, load-line control, and current monitoring must be made using Kelvin-sense connections to guarantee the current-sense accuracy.
- When trade-offs in trace lengths must be made, it is preferable to allow the inductor charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET, or between the inductor and the output filter capacitor.
- Route high-speed switching nodes away from sensitive analog areas (i.e., FB, FBAC, CSP_, CSN_, etc.).

See Table 12 for layout procedures.

Table 12. Layout Procedures

COMPONENTS	DESCRIPTION
Capacitors	The general rule is that capacitors take priority over resistors since they provide a filtering function. The list below is in order of priority: **1) V_{BIAS} Capacitors:** Place these near the IC pins with wide traces and good connection to PGND. **2) CSP_ - CSN_ Differential Filter Capacitors:** Place the capacitors and the step resistor near the IC pins. These inputs are critical because they are used for regulation and load-line, as well as current limit and current balance. **3) Common-Mode Capacitors:** The capacitors to AGND take the next priority. **4) FB and GNDS Capacitors:** The FB capacitor can be slightly farther away from the IC since the FB resistor has priority to be closer to the IC.
FB and FBAC	The FB and FBAC resistors should be near the respective pins. Keep the trace short to reduce any inductance.
Current Sense	Use Kelvin-sense connection to the sense element (inductor or sense resistor). Route CSP_ traces near CSN_. Avoid any switching signals, especially LX when routing these current-sensing signals.
Thermistors	The NTC for THERM sensing should be placed near the power components of the first phase.
Catch Resistors	Catch resistors should be placed near the point of load so that the output-voltage trace does not need to route back to the IC. The ground catch resistor is less critical as it only requires a via to connect to the PGND plane.
Remote Sense	Route together in a quiet layer, avoiding any switching signals, especially LX.
I²C	Pullups for I²C Interface and $\overline{INT}$ do not need to be too close to the IC and can be placed farther away to make space for other more important components near the IC. Place a small 0.1µF decoupling capacitor for the V_{TT} near the pullup resistors.
AGND	Keep the AGND polygon just large enough to cover AGND components. Do not make it any larger than necessary. The AGND polygon should not run under any high-voltage switching traces since all AGND connections should be on the other side of the IC, away from the driver pins.
AGND-PGND	AGND-PGND connection should be made away from the PGND pins so as not to be in the path of the DRVPWM_ drive currents. A good location is near the BIAS pin.
Exposed Pad	Connect to AGND.
Power Components	Place the power components close to keep the current loop small. Avoid large LX nodes. Use multiple vias to keep the impedance low and to carry the high currents.

Chip Information

PROCESS: BiCMOS

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX15569GTG+	-40°C to +105°C	24 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 TQFN-EP	T2444+4	21-0139	90-0022

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/13	Initial release	—
1	2/15	Updated the *Benefits and Features* section	1

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