19-2882; Rev 1; 4/04

EVALUATION KIT AVAILABLE

Six-Channel, High-Efficiency, Digital Camera Power Supplies

General Description

The MAX1566/MAX1567 provide a complete power-supply solution for digital cameras. They improve performance, component count, and size compared to conventional multichannel controllers in 2-cell AA, 1-cell lithium-ion (Li+), and dual-battery designs. On-chip MOSFETs provide up to 95% efficiency for critical power supplies, while additional channels operate with external FETs for optimum design flexibility. This optimizes overall efficiency and cost, while also reducing board space.

The MAX1566/MAX1567 include six high-efficiency DC-to-DC conversion channels:

- Step-up DC-to-DC converter with on-chip power FETs
- Main DC-to-DC converter with on-chip FETs, configurable to step **either** up or down
- Step-down core DC-to-DC converter with on-chip FETs
- DC-to-DC controller for white LEDs or other output
- Extra DC-to-DC controller (typically for LCD); two extra controllers on the MAX1566
- Transformerless inverting DC-to-DC controller (typically for negative CCD bias) on the MAX1567

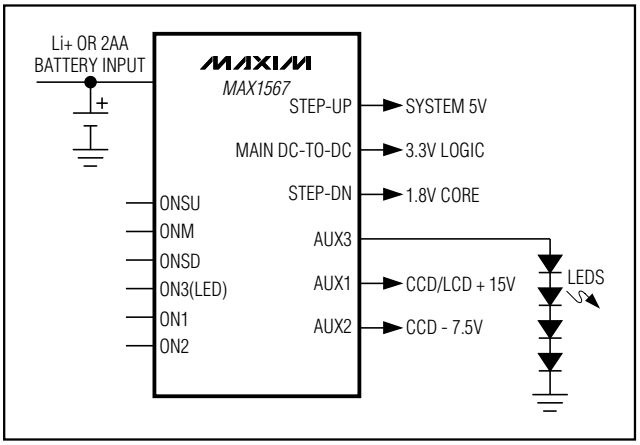
All DC-to-DC channels operate at one fixed frequency settable from 100kHz to 1MHz to optimize size, cost, and efficiency. Other features include soft-start, power-OK outputs, and overload protection. The MAX1566/MAX1567 are available in space-saving 40-pin thin QFN packages. An evaluation kit is available to expedite designs.

Applications

Digital Cameras

PDAs

Typical Operating Circuit



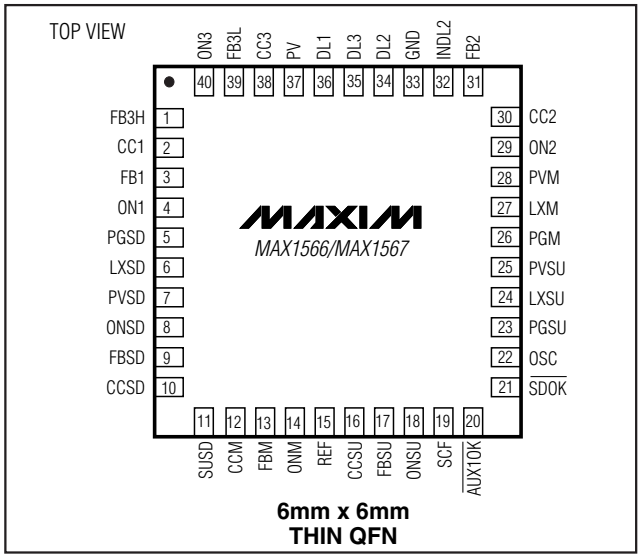
Features

- **95% Efficient Step-Up DC-to-DC Converter**
- **0.7V Minimum Input Voltage**
- **Main DC-to-DC Configurable as Either Step-Up or Step-Down**
- **Combine Step-Up and Step-Down for 90% Efficient Boost-Buck**
- **95% Efficient Step-Down for DSP Core**
- **Regulate LED Current for Four, Six, or More LEDs**
- **Open LED Overvoltage Protection**
- **Transformerless Inverting Controller (MAX1567)**
- **Three Extra PWM Controllers (Two on the MAX1567)**
- **Up to 1MHz Operating Frequency**
- **1µA Shutdown Mode**
- **Soft-Start and Overload Protection**
- **Compact 40-Pin 6mm x 6mm Thin QFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	AUX2 FUNCTION
MAX1566ETL	-40°C to +85°C	40 Thin QFN 6mm x 6mm	Step-up controller
MAX1567ETL	-40°C to +85°C	40 Thin QFN 6mm x 6mm	Inverting controller

Pin Configuration



6mm x 6mm THIN QFN

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ABSOLUTE MAXIMUM RATINGS

PV, PVSU, $\overline{SDOK}$, $\overline{AUX1OK}$, SCF, ON_, FB_, SUSD to GND ..... -0.3V to +6V
PG_ to GND .....-0.3V to +0.3V
DL1, DL3, INDL2, PVM, PVSD to GND …-0.3V to (PVSU + 0.3V)
DL2 to GND .....-0.3V to (INDL2 + 0.3V)
LXSU Current (Note 1) 3.6A
LXM Current (Note 1) 3.6A
LXSD Current (Note 1) 2.25A
REF, OSC, CC_ to GND .....-0.3V to (PVSU + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
40-Pin Thin QFN (derate 26.3mW/°C above +70°C) .2105mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: LXSU has internal clamp diodes to PVSU and PGSU, LXM has internal clamp diodes to PVM and PGM, and LXSD has internal clamp diodes to PVSD and PGSD. Applications that forward bias these diodes should take care not to exceed the devices' power dissipation limits.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{PVSU} = V_{PV} = V_{PVM} = V_{PVSD} = V_{INDL2} = 3.6V, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL					
Input Voltage Range	(Note 2)	0.7		5.5	V
Step-Up Minimum Startup Voltage (Note 2)	I_{LOAD} < 1mA, T_A = +25°C; startup voltage tempco is -2300ppm/°C (typ) (Note 3)		0.9	1.1	V
Shutdown Supply Current into PV	PV = 3.6V		0.1	10	µA
Supply Current into PV with Step-Up Enabled	ONSU = 3.6V, FBSU = 1.5V (does not include switching losses)		300	450	µA
Supply Current into PV with Step-Up and Step-Down Enabled	ONSU = ONSD = 3.6V, FBSU = 1.5V, FBSD = 1.5V (does not include switching losses)		450	700	µA
Supply Current into PV with Step-Up and Main Enabled	ONSU = ONM = 3.6V, FBSU = 1.5V, FBSD = 1.5V (does not include switching losses)		450	700	µA
Total Supply Current from PV and PVSU with Step-Up and One AUX Enabled	ONSU = ON1 = 3.6V, FBSU = 1.5V, FB2 = 1.5V (does not include switching losses)		400	650	µA
REFERENCE					
Reference Output Voltage	I_{REF} = 20µA	1.23	1.25	1.27	V
Reference Load Regulation	10µA < I_{REF} < 200µA		4.5	10	mV
Reference Line Regulation	2.7 < PVSU < 5.5V		1.3	5	mV
OSCILLATOR					
OSC Discharge Trip Level	Rising edge	1.225	1.25	1.275	V
OSC Discharge Resistance	OSC = 1.5V, I_{OSC} = 3mA		52	80	Ω
OSC Discharge Pulse Width			200		ns
OSC Frequency	R_{OSC} = 47kΩ, C_{OSC} = 100pF		500		kHz

ELECTRICAL CHARACTERISTICS (continued)

(V_{PVSU} = V_{PV} = V_{PVM} = V_{PVSD} = V_{INDL2} = 3.6V, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
STEP-UP DC-TO-DC					
Step-Up Startup-to-Normal Operating Threshold	Rising edge or falling edge (Note 4)	2.30	2.5	2.65	V
Step-Up Startup-to-Normal Operating Threshold Hysteresis			80		mV
Step-Up Voltage Adjust Range		3.0		5.5	V
Start Delay of ONSD, ONM, ON1, ON2, and ON3 after SU in Regulation			1024		OSC cycles
FBSU Regulation Voltage		1.231	1.25	1.269	V
FBSU to CCSU Transconductance	FBSU = CCSU	80	135	185	µS
FBSU Input Leakage Current	FBSU = 1.25V	-100	0.01	+100	nA
Idle Mode™ Trip Level			150		mA
Current-Sense Amplifier Transresistance			0.275		V/A
Step-Up Maximum Duty Cycle	FBSU = 1V	80	85	90	%
PVSU Leakage Current	V_{LX} = 0V, PVSU = 3.6V		0.1	5	µA
LXSU Leakage Current	V_{LX} = V_{OUT} = 3.6V		0.1	5	µA
Switch On-Resistance	N channel		95	150	mΩ
	P channel		150	250	
N-Channel Current Limit		1.8	2.1	2.4	A
P-Channel Turn-Off Current			20		mA
Startup Current Limit	PVSU = 1.8V (Note 5)		450		mA
Startup t_{OFF}	PVSU = 1.8V		700		ns
Startup Frequency	PVSU = 1.8V		200		kHz
MAIN DC-TO-DC CONVERTER					
Main Step-Up Voltage Adjust Range	SUSD = PVSU	3		5.5	V
Main Step-Down Voltage Adjust Range	SUSD = GND, PVM must be greater than output (Note 6)	2.45		5.00	V
PVM Undervoltage Lockout in Step-Down Mode	SUSD = GND (Note 6)	2.45	2.5	2.55	V
Regulation Voltage		1.231	1.25	1.269	V
FBM to CCM Transconductance	FBM = CCM	80	135	185	µS
FBM Input Leakage Current	FBM = 1.25V	-100	0.01	+100	nA
Idle Mode Trip Level	Step-up mode (SUSD = PVSU)		150		mA
	Step-down mode (SUSD = GND)		100		
Current-Sense Amplifier Transresistance	Step-up mode (SUSD = PVSU)		0.25		V/A
	Step-down mode (SUSD = GND)		0.5		

Idle Mode is a trademark of Maxim Integrated Products, Inc.

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ELECTRICAL CHARACTERISTICS (continued)

(V_{PVSU} = V_{PV} = V_{PVM} = V_{PVSD} = V_{INDL2} = 3.6V, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Duty Cycle (Note 6)	Step-up mode (SUSD = PVSU)	80	85	90	%
	Step-down mode (SUSD = GND)		95		
LXM Leakage Current	V_{LXM} = 0 to 3.6V, PVSU = 3.6V		0.1	5	µA
Switch On-Resistance	N channel		95	150	mΩ
	P channel		150	250	
Main Switch Current Limit	Step-up mode (SUSD = PVSU)	1.8	2.1	2.4	A
	Step-down mode (SUSD = GND)	0.70	0.8	0.95	
Synchronous Rectifier Turn-Off Current	Step-up mode (SUSD = PVSU)		20		mA
	Step-down mode (SUSD = GND)		20		
Soft-Start Interval			4096		OSC cycles
STEP-DOWN DC-TO-DC CONVERTER					
Step-Down Output-Voltage Adjust Range	PVSD must be greater than output (Note 7)	1.25		5.00	V
FBSD Regulation Voltage		1.231	1.25	1.269	V
FBSD to CCSD Transconductance	FBSD = CCSD	80	135	185	µS
FBSD Input Leakage Current	FBSD = 1.25V	-100	0.1	+100	nA
Idle Mode Trip Level			100		mA
Current-Sense Amplifier Transresistance			0.5		V/A
LXSD Leakage Current	V_{LXSD} = 0 to 3.6V, PVSU = 3.6V		0.1	5	µA
Switch On-Resistance	N channel		95	150	mΩ
	P channel		150	250	
P-Channel Current Limit		0.65	0.77	0.90	A
N-Channel Turn-Off Current			20		mA
Soft-Start Interval			2048		OSC cycles
$\overline{SDOK}$ Output Low Voltage	0.1mA into $\overline{SDOK}$		0.01	0.1	V
$\overline{SDOK}$ Leakage Current	ONSU = GND		0.01	1	µA
AUX1, 2, 3 DC-TO-DC CONTROLLERS					
INDL2 Undervoltage Lockout		2.45	2.5	2.55	V
Maximum Duty Cycle	FB_ = 1V	80	85	90	%
FB1, FB2 (MAX1566), FB3H Regulation Voltage		1.231	1.25	1.269	V
FB2 (MAX1567) Inverter Regulation Voltage		-0.01	0	+0.01	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{PVSU} = V_{PV} = V_{PVM} = V_{PVSD} = V_{INDL2} = 3.6V, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FB3L Regulation Voltage		0.19	0.2	0.21	V
AUX1, AUX2 FB to CC Transconductance		80	135	185	µS
AUX3 FBL or FBH to CC Transconductance		50	100	150	µS
FB_ Input Leakage Current		-100	0.1	+100	nA
DL_ Driver Resistance	Output high or low		2.5	7	Ω
DL_ Drive Current	Sourcing or sinking		0.5		A
Soft-Start Interval			4096		OSC cycles
$\overline{AUX1OK}$ Output Low Voltage	0.1mA into $\overline{AUX1OK}$		0.01	0.1	V
$\overline{AUX1OK}$ Leakage Current	ONSU = GND		0.01	1	µA
OVERLOAD PROTECTION					
Overload Protection Fault Delay			100,000		OSC cycles
SCF Leakage Current	ONSU = PVSU, FBSU = 1.5V		0.1	1	µA
SCF Output Low Voltage	0.1mA into SCF		0.01	0.1	V
THERMAL-LIMIT PROTECTION					
Thermal Shutdown			160		°C
Thermal Hysteresis			20		°C
LOGIC INPUTS (ON_, SUSD)					
ONSU Input Low Level	1.1V < PVSU < 1.8V			0.2	V
	1.8V ≤ PVSU < 2.5V			0.4	
	2.5V ≤ PVSU < 5.5V			0.5	
ONSU Input High Level	1.1V < PVSU < 1.8V	(PVSU - 0.2)			V
	1.8V < PVSU < 5.5V	1.6			
ONM, ONSD, ON1, ON2, ON3, SUSD Input Low Level	2.7V < PVSU < 5.5V (Note 8)			0.5	V
ONM, ONSD, ON1, ON2, ON3, SUSD Input High Level	2.7V < PVSU < 5.5V (Note 8)	1.6			V
SUSD Input Leakage			0.1	1	µA
ON_ Impedance to GND			330		kΩ

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ELECTRICAL CHARACTERISTICS

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PARAMETER	CONDITIONS	MIN	MAX	UNITS
GENERAL				
Input Voltage Range	(Note 2)	0.7	5.5	V
Step-Up Minimum Startup Voltage (Note 2)	I_{LOAD} < 1mA, T_A = +25°C; startup voltage tempco is -2300ppm/°C (typ) (Note 3)		1.1	V
Shutdown Supply Current into PV	PV = 3.6V		10	µA
Supply Current into PV with Step-Up Enabled	ONSU = 3.6V, FBSU = 1.5V (does not include switching losses)		400	µA
Supply Current into PV with Step-Up and Step-Down Enabled	ONSU = ONSD = 3.6V, FBSU = 1.5V, FBSD = 1.5V (does not include switching losses)		600	µA
Supply Current into PV with Step-Up and Main Enabled	ONSU = ONM = 3.6V, FBSU = 1.5V, FBSD = 1.5V (does not include switching losses)		600	µA
Total Supply Current from PV and PVSU with Step-Up and One AUX Enabled	ONSU = ON1 = 3.6V, FBSU = 1.5V, FB2 = 1.5V (does not include switching losses)		550	µA
REFERENCE				
Reference Output Voltage	I_{REF} = 20µA	1.23	1.27	V
Reference Load Regulation	10µA < I_{REF} < 200µA		10	mV
Reference Line Regulation	2.7V < PVSU < 5.5V		5	mV
OSCILLATOR				
OSC Discharge Trip Level	Rising edge	1.225	1.275	V
OSC Discharge Resistance	OSC = 1.5V, I_{OSC} = 3mA		80	Ω
STEP-UP DC-TO-DC CONVERTER				
Step-Up Startup-to-Normal Operating Threshold	Rising edge or falling edge (Note 4)	2.30	2.65	V
Step-Up Voltage Adjust Range		3.0	5.5	V
FBSU Regulation Voltage		1.231	1.269	V
FBSU to CCSU Transconductance	FBSU = CCSU	80	185	µS
FBSU Input Leakage Current	FBSU = 1.25V	-100	+100	nA
Step-Up Maximum Duty Cycle	FBSU = 1V	80	90	%
PVSU Leakage Current	V_{LX} = 0V, PVSU = 3.6V		5	µA
LXSU Leakage Current	V_{LX} = V_{OUT} = 3.6V		5	µA
Switch On-Resistance	N channel		150	mΩ
	P channel		250	
N-Channel Current Limit		1.8	2.4	A
MAIN DC-TO-DC CONVERTER				
Main Step-Up Voltage Adjust Range	SUSD = PVSU	3.0	5.5	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{PVSU} = V_{PV} = V_{PVM} = V_{PVSD} = V_{INDL2} = 3.6V, **T_A = -40°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	MAX	UNITS
Main Step-Down Voltage Adjust Range	SUSD = GND, PVM must be greater than output (Note 6)	2.45	5.00	V
PVM Undervoltage Lockout in Step-Down Mode	SUSD = GND (Note 6)	2.45	2.55	V
Regulation Voltage		1.225	1.275	V
FBM to CCM Transconductance	FBM = CCM	80	185	µS
FBM Input Leakage Current	FBM = 1.25V	-100	+100	nA
Maximum Duty Cycle	Step-up mode (SUSD = PVSU), step-down mode (SUSD = GND) (Note 6)	80	90	%
LXM Leakage Current	V_{LXM} = 0 to 3.6V, PVSU = 3.6V		5	µA
Switch On-Resistance	N channel		150	mΩ
	P channel		250	
Main Switch Current Limit	Step-up mode (SUSD = PVSU)	1.8	2.4	A
	Step-down mode (SUSD = GND)	0.70	0.95	
STEP-DOWN DC-TO-DC CONVERTER				
Step-Down Output Voltage Adjust Range	PVSD must be greater than output (Note 7)	1.25	5.00	V
FBSD Regulation Voltage		1.225	1.275	V
FBSD to CCSD Transconductance	FBSD = CCSD	80	185	µS
FBSD Input Leakage Current	FBSD = 1.25V	-100	+100	nA
LXSD Leakage Current	V_{LXSD} = 0 to 3.6V, PVSU = 3.6V		5	µA
Switch On-Resistance	N channel		150	mΩ
	P channel		250	
P-Channel Current Limit		0.65	0.90	A
$\overline{SDOK}$ Output Low Voltage	0.1mA into $\overline{SDOK}$		0.1	V
$\overline{SDOK}$ Leakage Current	ONSU = GND		1	µA
AUX1, 2, 3 DC-TO-DC CONTROLLERS				
INDL2 Undervoltage Lockout		2.45	2.55	V
Maximum Duty Cycle	FB_ = 1V	80	90	%
FB1, FB2 (MAX1566), FB3H Regulation Voltage		1.225	1.275	V
FB2 (MAX1567) Inverter Regulation Voltage		-0.01	+0.01	V
FB3L Regulation Voltage		0.19	0.21	V
AUX1, AUX2 FB to CC Transconductance		80	185	µS

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ELECTRICAL CHARACTERISTICS (continued)

(V_{PVSU} = V_{PV} = V_{PVM} = V_{PVSD} = V_{INDL2} = 3.6V, **T_A = -40°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	MAX	UNITS
AUX3 FBL or FBH to CC Transconductance		35	150	µS
FB_ Input Leakage Current		-100	+100	nA
DL_ Driver Resistance	Output high or low		7	Ω
$\overline{AUX1OK}$ Output Low	0.1mA into $\overline{AUX1OK}$		0.1	V
$\overline{AUX1OK}$ Leakage Current	ONSU = GND		1	µA
OVERLOAD PROTECTION				
SCF Leakage Current	ONSU = PVSU, FBSU = 1.5V		1	µA
SCF Output Low Voltage	0.1mA into SCF		0.1	V
LOGIC INPUTS (ON_, SUSD)				
ONSU Input Low Level	1.1V < PVSU < 1.8V		0.2	V
	1.8V ≤ PVSU < 2.5V		0.4	
	2.5V ≤ PVSU < 5.5V		0.5	
ONSU Input High Level	1.1V < PVSU < 1.8V	(PVSU - 0.2)		V
	1.8V < PVSU < 5.5V	1.6		
ONM, ONSD, ON1, ON2, ON3, SUSD Input Low Level	2.7V < PVSU < 5.5V (Note 8)		0.5	V
ONM, ONSD, ON1, ON2, ON3, SUSD Input High Level	2.7V < PVSU < 5.5V (Note 8)	1.6		V
SUSD Input Leakage			1	µA

Note 2: The MAX1566/MAX1567 are powered from the step-up output (PVSU). An internal low-voltage startup oscillator drives the step-up starting at approximately 0.9V until PVSU reaches approximately 2.5V. When PVSU reaches 2.5V, the main control circuitry takes over. Once the step-up is up and running, it can maintain operation with very low input voltages; however, output current is limited.

Note 3: Since the device is powered from PVSU, a Schottky rectifier, connected from the battery to PVSU, is required for low-voltage startup.

Note 4: The step-up regulator is in startup mode until this voltage is reached. Do not apply full load current during startup. A power-OK output can be used with an external PFET to gate the load until the step-up is in regulation. See the *$\overline{AUX1OK}$, $\overline{SDOK}$, and SCF Connections* section.

Note 5: The step-up current limit in startup refers to the LXSU switch current limit, not the output current limit.

Note 6: If the main converter is configured as a step-up (SUSD = PVSU), the P-channel synchronous rectifier is disabled until the 2.5V normal operation threshold has been exceeded. If the main converter is configured as a step-down (SUSD = GND), all step-down operation is locked out until the normal operation threshold has been exceeded. When the main is configured as a step-down, operation in dropout (100% duty cycle) can only be maintained for 100,000 OSC cycles before the output is considered faulted, triggering global shutdown.

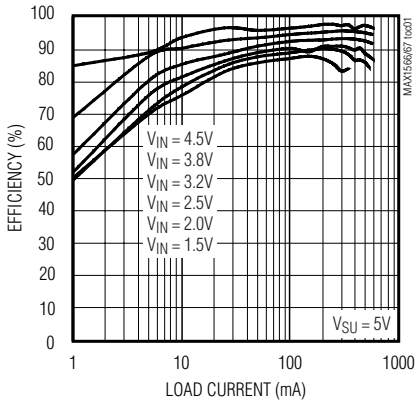
Note 7: Operation in dropout (100% duty cycle) can only be maintained for 100,000 OSC cycles before the output is considered faulted, triggering global shutdown.

Note 8: ONM, ONSD, ON1, ON2, and ON3 are disabled until 1024 OSC cycles after PVSU reaches 2.7V.

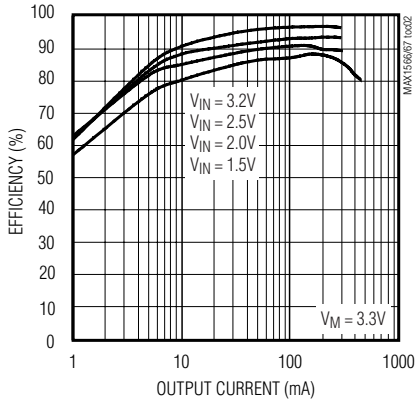
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

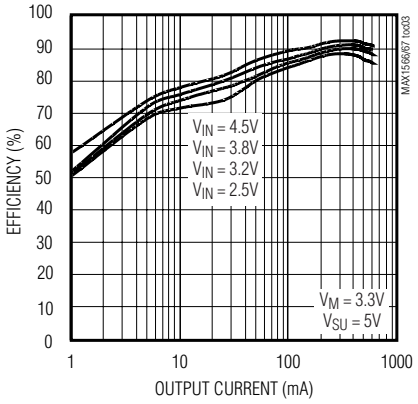
STEP-UP EFFICIENCY vs. LOAD CURRENT



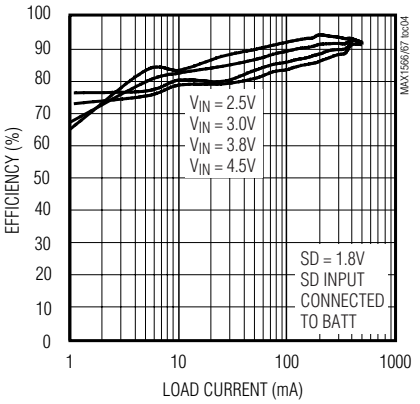
MAIN (STEP-UP) EFFICIENCY vs. LOAD CURRENT



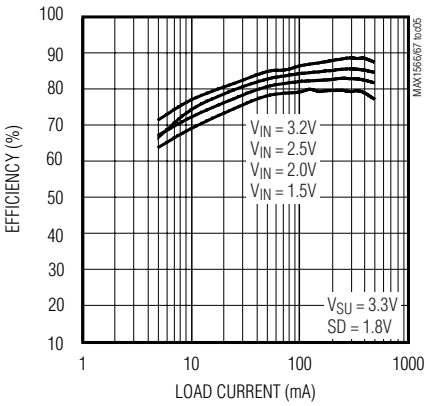
BOOST-BUCK EFFICIENCY (SU + MAIN AS STEP-DOWN) vs. LOAD CURRENT



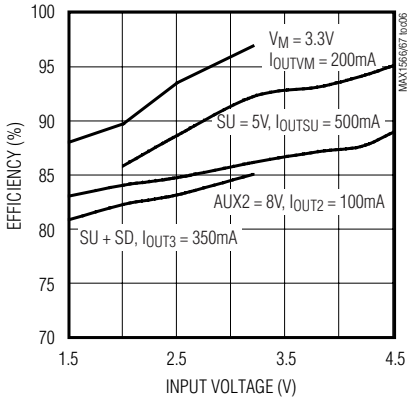
STEP-DOWN EFFICIENCY vs. LOAD CURRENT



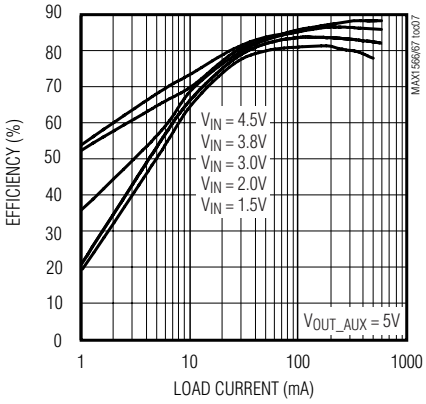
BOOST-BUCK EFFICIENCY (SU + SD) vs. LOAD CURRENT



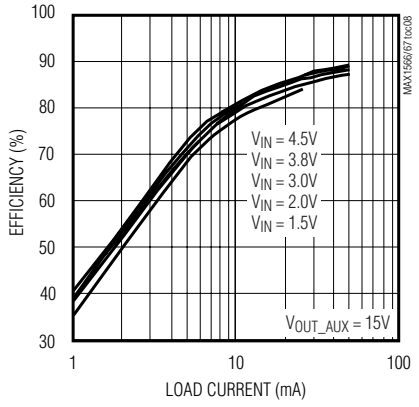
EFFICIENCY vs. INPUT VOLTAGE



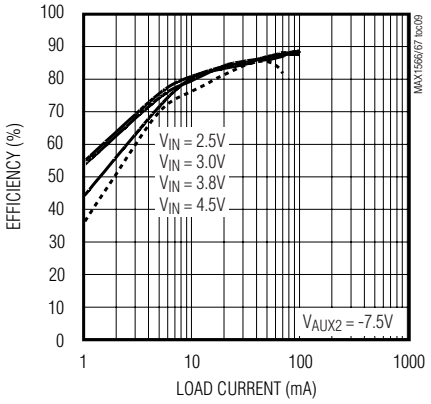
AUX EFFICIENCY vs. LOAD CURRENT



AUX EFFICIENCY vs. LOAD CURRENT



MAX1567 AUX2 EFFICIENCY vs. LOAD CURRENT



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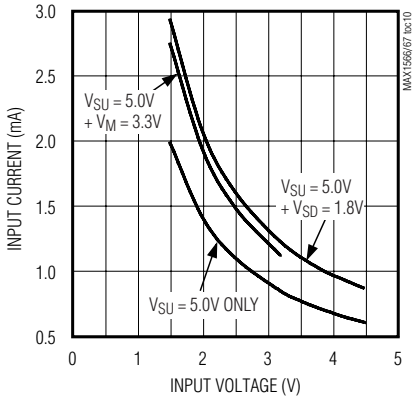
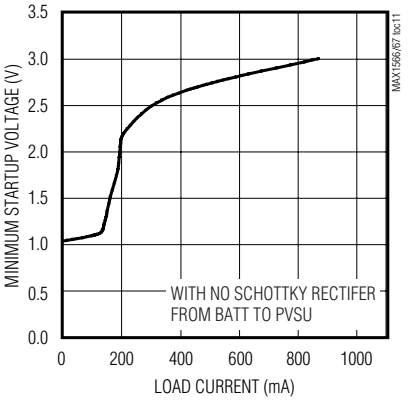
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

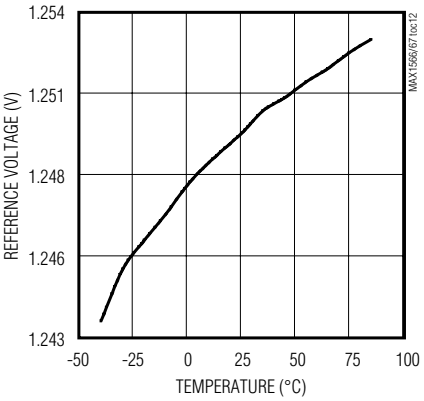
NO-LOAD INPUT CURRENT vs. INPUT VOLTAGE (SWITCHING)



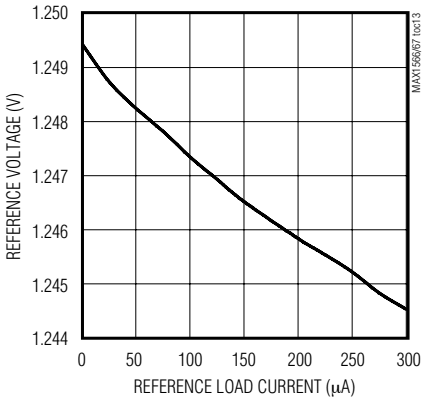
MINIMUM STARTUP VOLTAGE vs. LOAD CURRENT (OUTSU)



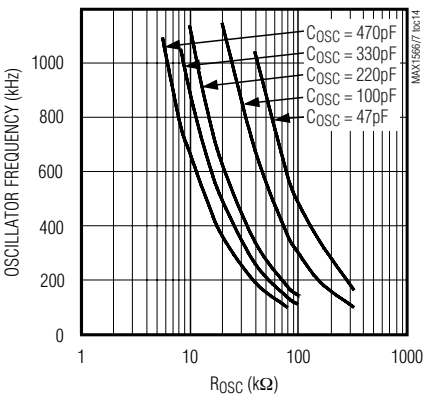
REFERENCE VOLTAGE vs. TEMPERATURE



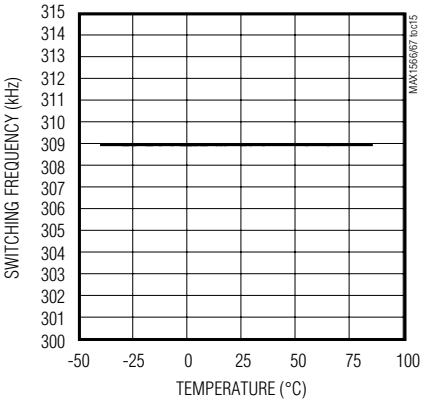
REFERENCE VOLTAGE vs. REFERENCE LOAD CURRENT



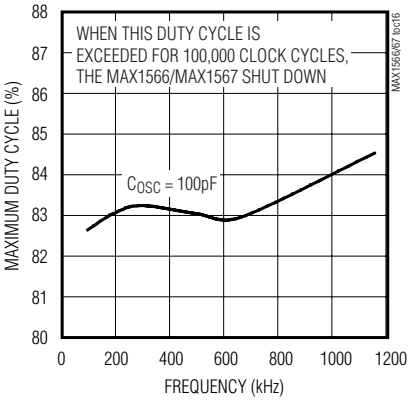
OSCILLATOR FREQUENCY vs. ROSC



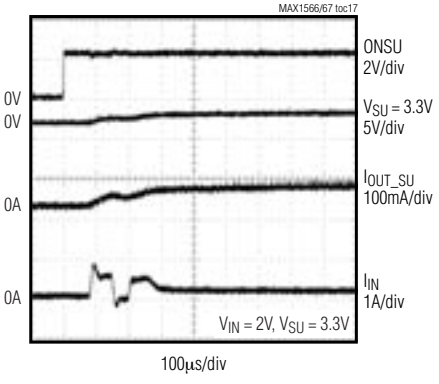
SWITCHING FREQUENCY vs. TEMPERATURE



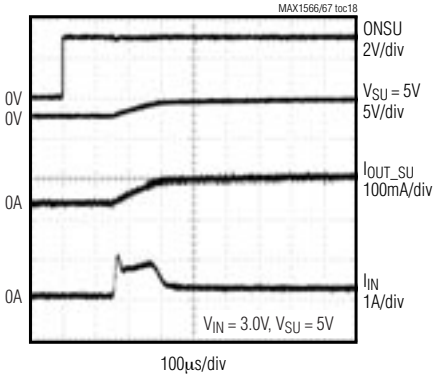
AUX_ MAXIMUM DUTY CYCLE vs. FREQUENCY



STEP-UP STARTUP WAVEFORMS



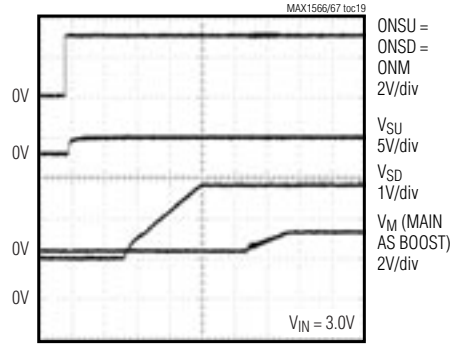
STEP-UP STARTUP WAVEFORMS



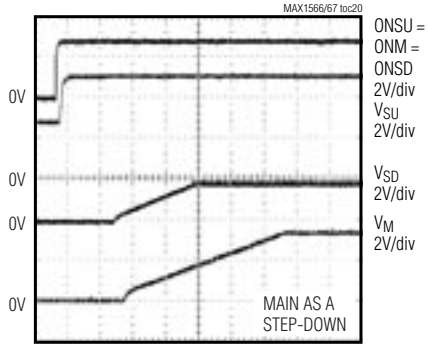
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

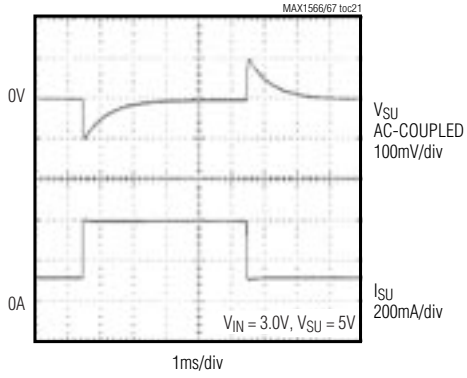
MAIN (STEP-UP MODE) AND STEP-DOWN STARTUP WAVEFORMS



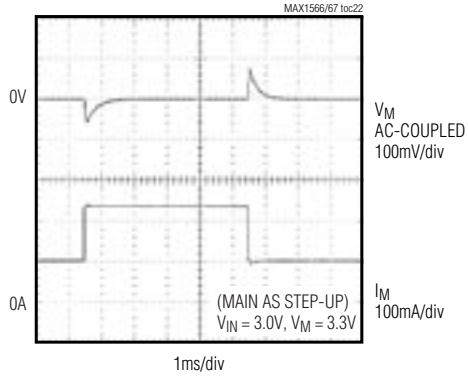
MAIN (STEP-DOWN MODE) AND STEP-DOWN STARTUP WAVEFORMS



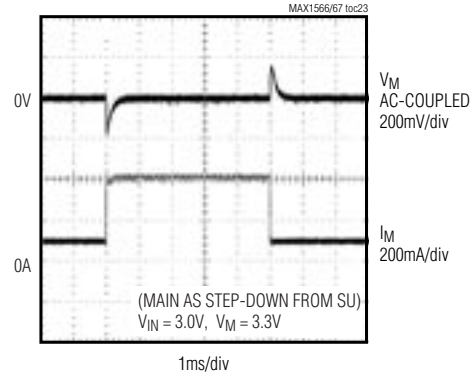
STEP-UP LOAD TRANSIENT RESPONSE



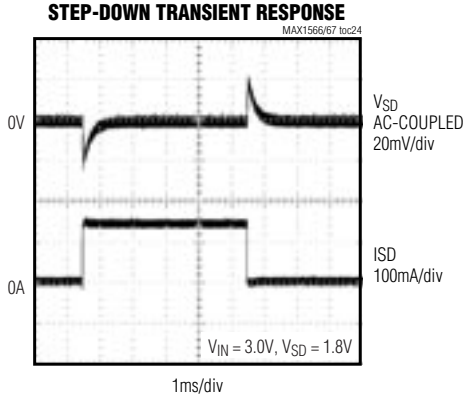
MAIN (STEP-UP MODE) LOAD TRANSIENT RESPONSE



MAIN (STEP-DOWN MODE) LOAD TRANSIENT RESPONSE



STEP-DOWN TRANSIENT RESPONSE



Six-Channel, High-Efficiency, Digital Camera Power Supplies

Pin Description

PIN	NAME	FUNCTION
1	FB3H	AUX3 Controller Voltage Feedback Input. Connect a resistive voltage-divider from the step-up converter output to FBH to set the output voltage. The feedback threshold is 1.25V. This pin is high impedance in shutdown. FB3H can provide conventional voltage feedback (with FB3L grounded) or open-LED protection in white LED drive circuits.
2	CC1	AUX1 Controller Compensation Node. Connect a series resistor-capacitor from this pin to GND to compensate the converter control loop. This pin is actively driven to GND in shutdown, overload, and thermal limit. See the *AUX Compensation* section.
3	FB1	AUX1 Controller Feedback Input. The feedback threshold is 1.25V. This pin is high impedance in shutdown.
4	ON1	AUX1 Controller On/Off Input. Logic high = on; however, turn-on is locked out until 1024 OSC cycles after the step-up has reached regulation. This pin has an internal 330kΩ pulldown resistance to GND.
5	PGSD	Power Ground. Connect all PG_ pins to GND with short wide traces as close to the IC as possible.
6	LXSD	Step-Down Converter Switching Node. Connect to the inductor of the step-down converter. LXSD is high impedance in shutdown.
7	PVSD	Step-Down Converter Input. Bypass to GND with a 1µF ceramic capacitor. The step-down efficiency is measured from this input.
8	ONSD	Step-Down Converter On/Off Control Input. Logic high = on; however, turn-on is locked out until 1024 OSC cycles after the step-up has reached regulation. This pin has an internal 330kΩ pulldown resistance to GND.
9	FBSD	Step-Down Converter Feedback Input. The feedback threshold is 1.25V. This pin is high impedance in shutdown.
10	CCSD	Step-Down Converter Compensation Node. Connect a series resistor-capacitor from this pin to GND for compensating the converter control loop. This pin is actively driven to GND in shutdown, overload, and thermal limit. See the *Step-Down Compensation* section.
11	SUSD	Configures the Main Converter as a Step-Up or a Step-Down. This function must be hardwired. On-the-fly changes are not allowed. With SUSD connected to PV, the main is configured as a step-up and PVM is the converter output. With SUSD connected to GND, the main is configured as a step-down and PVM is the power input.
12	CCM	Main Converter Compensation Node. Connect a series resistor-capacitor from this pin to GND for compensating the converter control loop. This pin is actively driven to GND in shutdown, overload, and thermal limit. See the *Step-Up Compensation* section when the main is used in step-up mode and the *Step-Down Compensation* section when the main is used in step-down mode.
13	FBM	Main Converter Feedback Input. The feedback threshold is 1.25V. This pin is high impedance in shutdown. The main output voltage must not be set higher than the step-up output.
14	ONM	On/Off Control for the Main DC-to-DC Converter. Logic high = on; however, turn-on is locked out until 1024 OSC cycles after the step-up has reached regulation. This pin has an internal 330kΩ pulldown resistance to GND. SUSD pin configures the main converter as a step-up or step-down.
15	REF	Reference Output. Bypass REF to GND with a 0.1µF or greater capacitor. The maximum-allowed REF load is 200µA. REF is actively pulled to GND when the step-up is shut down (all converters turn off).

Pin Description (continued)

PIN	NAME	FUNCTION
16	CCSU	Step-Up Converter Compensation Node. Connect a series resistor-capacitor from this pin to GND for compensating the converter control loop. This pin is actively driven to GND in shutdown, overload, and thermal limit. See the *Step-Up Compensation* section.
17	FBSU	Step-Up Converter Feedback Input. The feedback threshold is 1.25V. This pin is high impedance in shutdown.
18	ONSU	Step-Up Converter On/Off Control. Logic high = on. All other ON_ pins are locked out until 1024 OSC cycles after the step-up DC-to-DC converter output has reached its final value. This pin has an internal 330kΩ pulldown resistance to GND.
19	SCF	Open-Drain, Active-Low, Short-Circuit Flag Output. SCF goes open when overload protection occurs and during startup. SCF can drive high-side PFET switches connected to one or more outputs to completely disconnect the load when the channel turns off in response to a logic command or an overload. See the *Status Outputs ($\overline{SDOK}$, $\overline{AUX1OK}$, SCF)* section.
20	$\overline{AUX1OK}$	Open-Drain, Active-Low, Power-OK Signal for AUX1 Controller. $\overline{AUX1OK}$ goes low when the AUX1 controller has successfully completed soft-start. $\overline{AUX1OK}$ goes high impedance in shutdown, overload, and thermal limit.
21	$\overline{SDOK}$	Open-Drain, Active-Low, Power-OK Signal for Step-Down Converter. $\overline{SDOK}$ goes low when the step-down has successfully completed soft-start. $\overline{SDOK}$ goes high impedance in shutdown, overload, and thermal limit.
22	OSC	Oscillator Control. Connect a timing capacitor from OSC to GND and a timing resistor from OSC to PVSU (or other DC voltage) to set the oscillator frequency between 100kHz and 1MHz. See the *Setting the Switching Frequency* section. This pin is high impedance in shutdown.
23	PGSU	Power Ground. Connect all PG_ pins to GND with short wide traces as close to the IC as possible.
24	LXSU	Step-Up Converter Switching Node. Connect to the inductor of the step-up converter. LXSU is high impedance in shutdown.
25	PVSU	Power Output of the Step-Up DC-to-DC Converter. PVSU can also power other converter channels. Connect PVSU and PV together.
26	PGM	Power Ground. Connect all PG_ pins to GND with short wide traces as close to the IC as possible.
27	LXM	Main Converter Switching Node. Connect to the inductor of the main converter (can be configured as a step-up or step-down by SUSD). LXM is high impedance in shutdown.
28	PVM	When SUSD = PVSU, the main converter is configured as a step-up and PVM is the main output. When SUSD = GND, the main is configured as a step-down and PVM is the power input.
29	ON2	AUX2 Controller On/Off Input. Logic high = on; however, turn-on is locked out until 1024 OSC cycles after the step-up has reached regulation. This pin has an internal 330kΩ pulldown resistance to GND.
30	CC2	AUX2 Controller Compensation Node. Connect a series resistor-capacitor from this pin to GND to compensate the converter control loop. This pin is actively driven to GND in shutdown, overload, and thermal limit. See the *AUX Compensation* section.

Pin Description (continued)

PIN	NAME	FUNCTION	
31	FB2	AUX2 Controller Feedback Input. This pin is high impedance in shutdown.	MAX1566 (AUX2 is configured as a boost): FB2 feedback threshold is 1.25V.
			MAX1567 (AUX2 is configured as an inverter): FB2 feedback threshold is 0V.
32	INDL2	Voltage Input for AUX2 Gate Driver. The voltage at INDL2 sets the high gate-drive voltage.	MAX1566 (AUX2 is configured as a boost): connect INDL2 to PVSU for optimum N-channel gate drive.
			MAX1567 (AUX2 is configured as an inverter): connect INDL2 to the external P-channel MOSFET source to ensure the P channel is completely off when DL2 swings high.
33	GND	Analog Ground. Connect to all PG_ pins as close to the IC as possible.	
34	DL2	AUX2 Controller Gate-Drive Output. DL2 drives between INDL2 and GND.	The MAX1566 configures DL2 to drive an N-channel FET in a boost configuration. DL2 is driven low in shutdown, overload, and thermal limit.
			The MAX1567 configures DL2 to drive a PFET in an inverter configuration. DL2 is driven high in shutdown, overload, and thermal limit.
35	DL3	AUX3 Controller Gate-Drive Output. Connect to the gate of an N-channel MOSFET. DL3 drives between GND and PVSU and supplies up to 500mA. This pin is actively driven to GND in shutdown, overload, and thermal limit.	
36	DL1	AUX1 Controller Gate-Drive Output. Connect to the gate of an N-channel MOSFET. DL1 drives between GND and PVSU and supplies up to 500mA. This pin is actively driven to GND in shutdown, overload, and thermal limit.	
37	PV	IC Power Input. Connect PVSU and PV together.	
38	CC3	AUX3 Controller Compensation Node. Connect a series resistor-capacitor from this pin to GND for compensating the converter control loop. This pin is actively driven to GND in shutdown, overload, and thermal limit. See the *AUX Compensation* section.	
39	FB3L	AUX3 Controller Current-Feedback Input. Connect a resistor from FB3L to GND to set LED current in LED boost-drive circuits. The feedback threshold is 0.2V. Connect this pin to GND if using only the FB3H feedback. This pin is high impedance in shutdown.	
40	ON3	AUX3 Controller On/Off Input. Logic high = on; however, turn-on is locked out until 1024 OSC cycles after the step-up has reached regulation. This pin has an internal 330kΩ pulldown resistance to GND.	
Pad	EP	Exposed Metal Pad. This pad is connected to ground. Note this internal connection is a soft-connect, meaning there is no internal metal or bond wire physically connecting the exposed pad to the GND pin. The connection is through the silicon substrate of the die and then through a conductive epoxy. Connecting the exposed pad to ground does not remove the requirement for a good ground connection to the appropriate pins.	

Detailed Description

The MAX1566/MAX1567 include the following blocks to build a multiple-output digital camera power-supply system. Both devices can accept inputs from a variety of sources including 1-cell Li+ batteries, 2-cell alkaline or NiMH batteries, and even systems designed to accept both battery types. The MAX1566/MAX1567 include six DC-to-DC converter channels to generate all required voltages:

- Step-up DC-to-DC converter (_SU pins) with on-chip power FETS
- Main DC-to-DC converter (_M pins) with on-chip power FETS that can be configured as either a step-up or step-down DC-to-DC converter
- Step-down core DC-to-DC converter with on-chip MOSFETs (_SD pins)
- AUX1 DC-to-DC controller for boost and flyback converters
- AUX2 DC-to-DC controller for boost and flyback converters (MAX1566)
- AUX2 DC-to-DC controller for inverting DC-to-DC converters (MAX1567)
- AUX3 DC-to-DC controller for white LED as well as conventional boost applications; includes open LED overvoltage protection

Step-Up DC-to-DC Converter

The step-up DC-to-DC switching converter typically is used to generate a 5V output voltage from a 1.5V to 4.5V battery input, but any voltage from V_{IN} to 5V can be set. An internal NFET switch and external synchronous rectifier allow conversion efficiencies as high as 95%. Under moderate to heavy loading, the converter operates in a low-noise PWM mode with constant frequency and modulated pulse width. Switching harmonics generated by fixed-frequency operation are consistent and easily filtered. Efficiency is enhanced under light (<75mA typ) loading by an Idle Mode that switches the step-up only as needed to service the load. In this mode, the maximum inductor current is 150mA for each pulse.

Main DC-to-DC Converter (Step-Up or Step-Down)

The main converter can be configured as a step-up (Figure 2) or a step-down converter (Figure 1) with the SUSD pin. The main DC-to-DC converter is typically used to generate 3.3V, but any voltage from 2.7V to 5V can be set; however, the main output must not be set higher than the step-up output (PVSU).

An internal MOSFET switch and synchronous rectifier allow conversion efficiencies as high as 95%. Under moderate to heavy loading, the converter operates in a low-noise PWM mode with constant frequency and modulated pulse width. Switching harmonics generated by fixed-frequency operation are consistent and easily filtered. Efficiency is enhanced under light loading (<150mA typical for step-up mode, <100mA typical for step-down mode) by assuming an Idle Mode during which the converter switches only as needed to service the load.

Step-down operation can be direct from a Li+ cell if the minimum input voltage exceeds the desired output by approximately 200mV. Note that if the main DC-to-DC, operating as a step-down, operates in dropout, the overload protection circuit senses an out-of-regulation condition and turns off all channels.

Li+ to 3.3V Boost-Buck Operation

When generating 3.3V from an Li+ cell, boost-buck operation may be needed so a regulated output can be maintained for input voltages above and below 3.3V. In that case, it may be best to configure the main converter as a step-down (SUSD = GND) and to connect its input, PVM, to the step-up output (PVSU), set to a voltage at or above 4.2V (Figures 1 and 3). The compound efficiency with this connection is typically up to 90%. This connection is also suitable for designs that must operate from both 1-cell Li+ and 2 AA cells.

Note that the step-up output supplies both the step-up load and the main step-down input current when the main is powered from the step-up. The main input current reduces the available step-up output current for other loads.

2 AA to 3.3V Operation

In designs that operate only from 2 AA cells, the main DC-to-DC can be configured as a boost converter (SUSD = PVM) to maximize the 3.3V efficiency (Figure 2).

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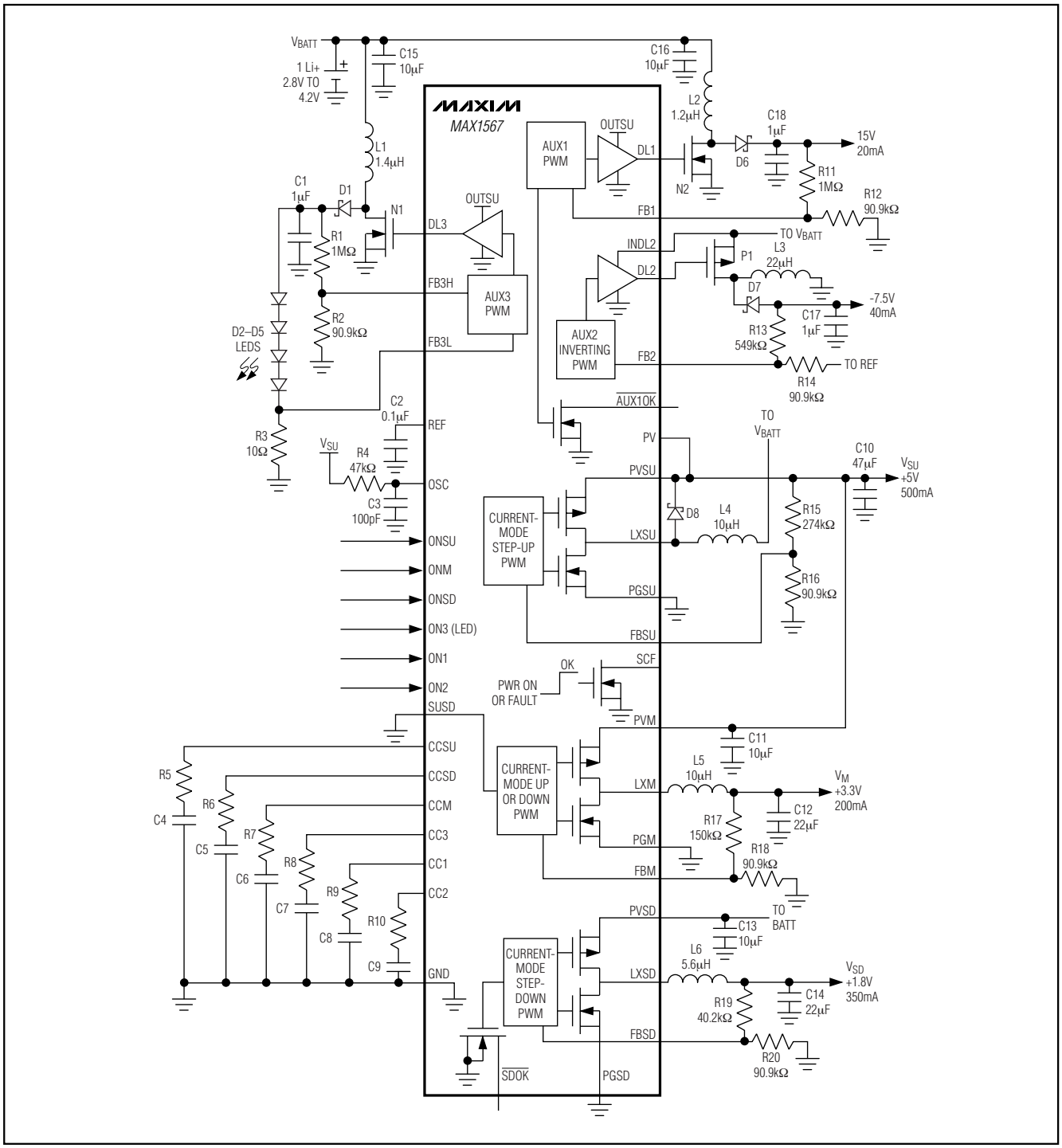

Figure 1. Typical 1-Cell Li+ Powered System (3.3V logic is stepped down from +5V, and 1.8V core is stepped down directly from the battery. Alternate connections are shown in the following figures.)

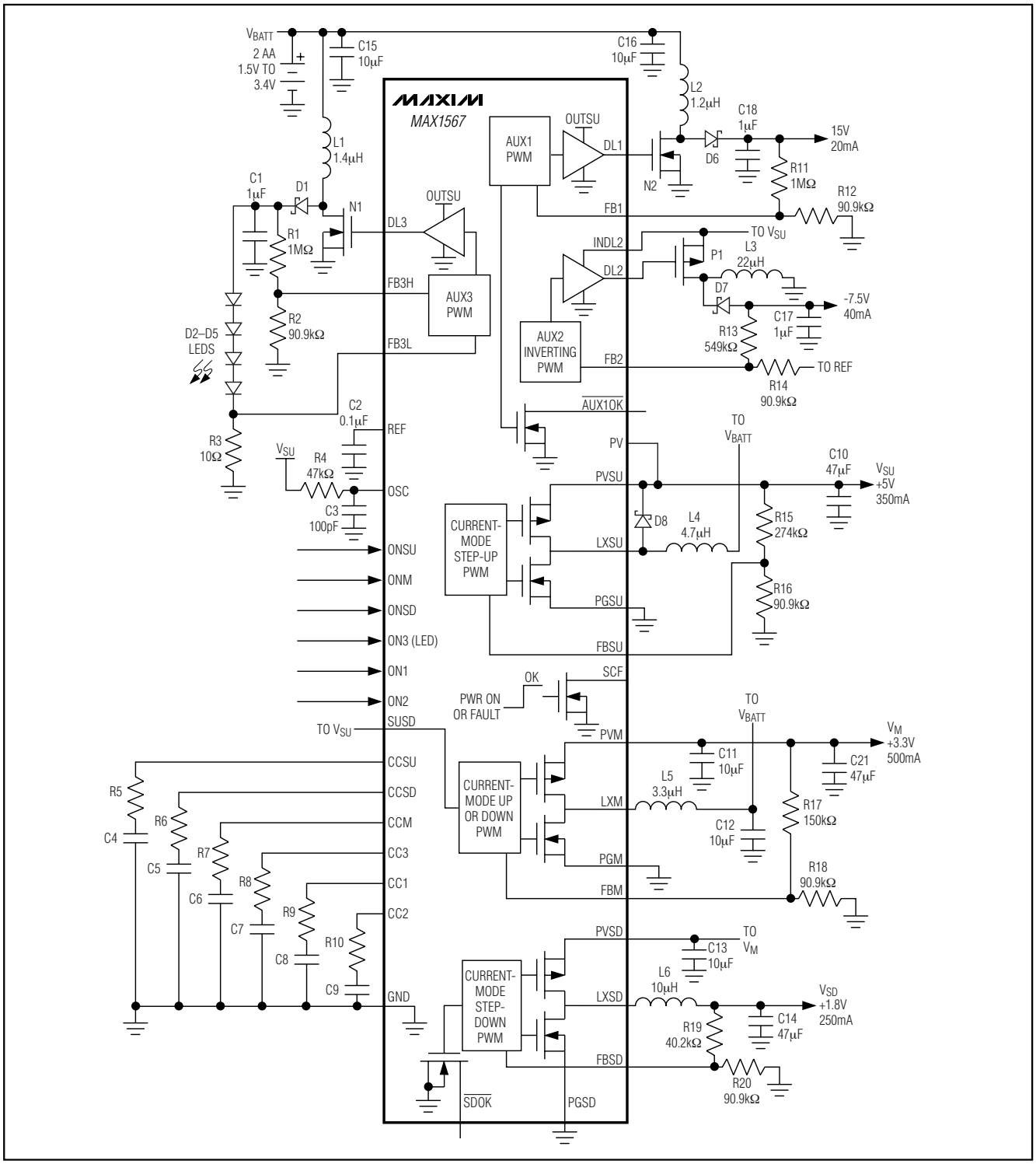

Figure 2. Typical 2-Cell AA-Powered System (3.3V is boosted from the battery and 1.8V is stepped down from V_M (3.3V).)

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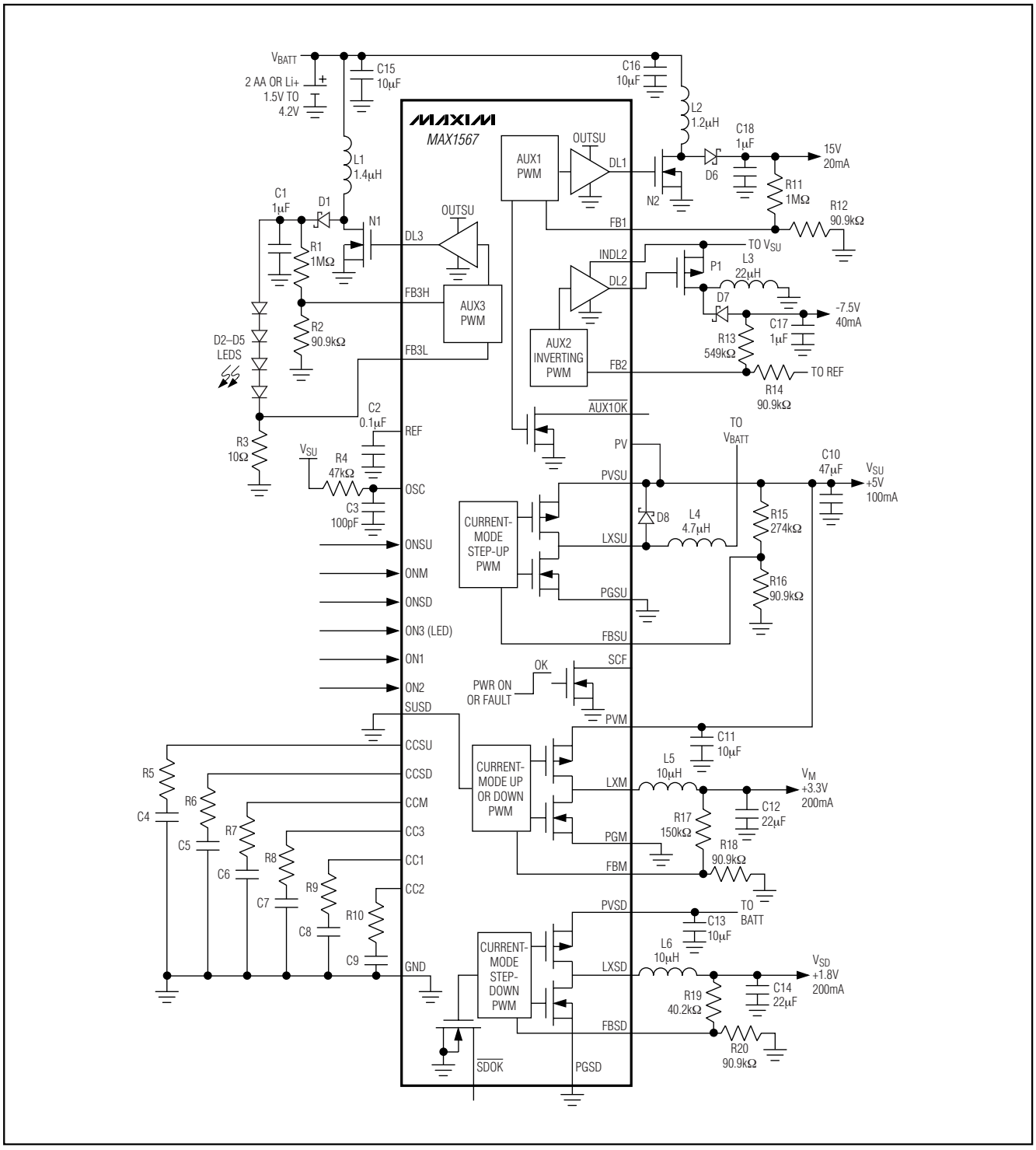


Figure 3. Li+ or Multibattery Input (This power supply accepts inputs from 1.5V to 4.2V, so it can operate from either 2 AA cells or 1 Li+ cell. The 3.3V logic supply and the 1.8V core supply are both stepped down from 5V for true boost-buck operation.)

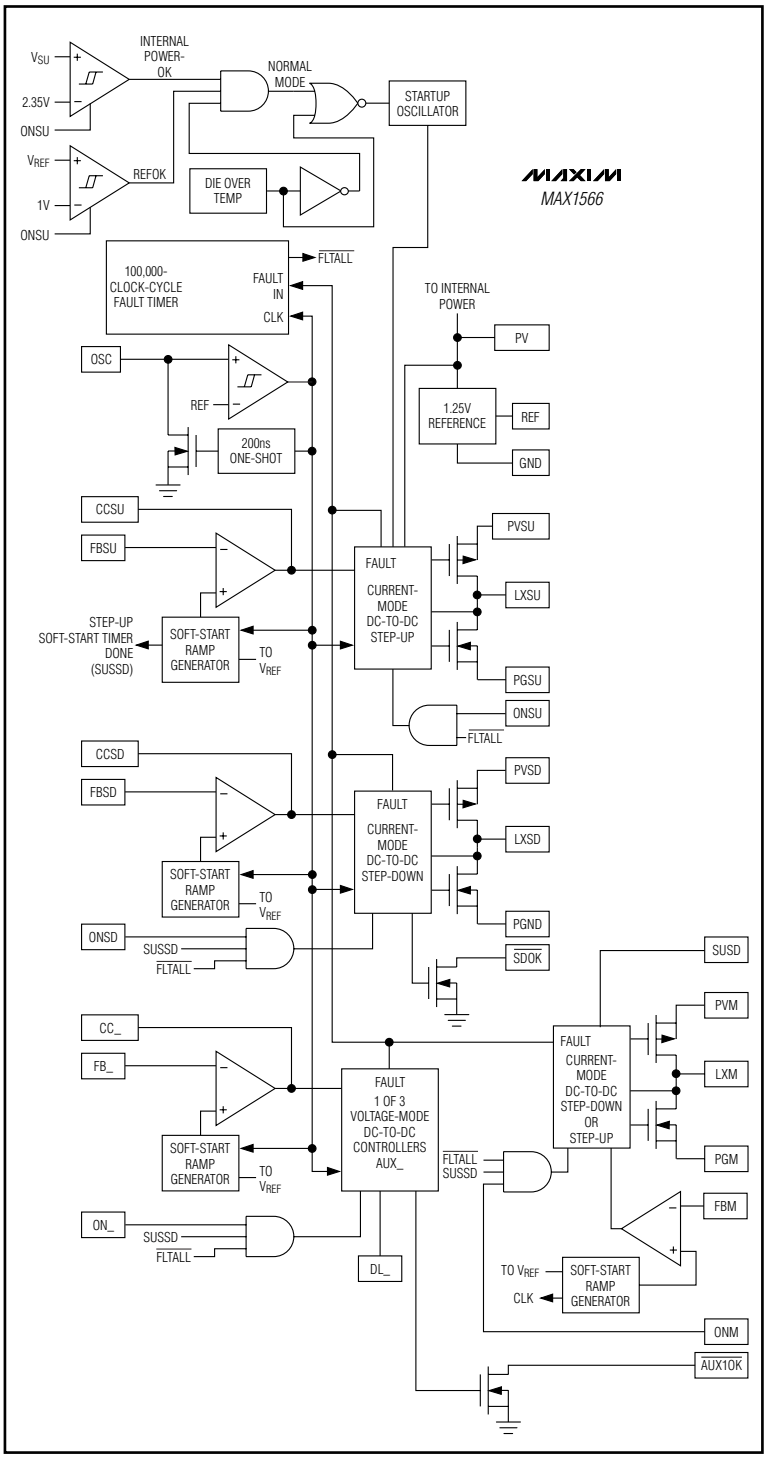


Figure 4. MAX1566 Functional Diagram

Six-Channel, High-Efficiency, Digital Camera Power Supplies

Core Step-Down DC-to-DC Converter

The step-down DC-to-DC is optimized for generating low output voltages (down to 1.25V) at high efficiency. The step-down runs from the voltage at PVSD. This pin can be connected directly to the battery if sufficient headroom exists to avoid dropout; otherwise, PVSD can be powered from the output of another converter. The step-down can also operate with the step-up, or the main converter in step-up mode, for boost-buck operation.

Under moderate to heavy loading, the converter operates in a low-noise PWM mode with constant frequency and modulated pulse width. Efficiency is enhanced under light (<75mA typ) loading by assuming an Idle Mode during which the step-down switches only as needed to service the load. In this mode, the maximum inductor current is 100mA for each pulse. The step-down DC-to-DC is inactive until the step-up DC-to-DC is in regulation.

The step-down also features an open-drain $\overline{SDOK}$ output that goes low when the step-down output is in regulation. $\overline{SDOK}$ can be used to drive an external MOSFET switch that gates 3.3V power to the processor after the core voltage is in regulation. This connection is shown in Figure 15.

AUX1, AUX2, and AUX3 DC-to-DC Controllers

The three auxiliary controllers operate as fixed-frequency voltage-mode PWM controllers. They do not have internal MOSFETs, so output power is determined by external components. The controllers regulate output voltage by modulating the pulse width of the DL_ drive signal to an external MOSFET switch.

On the MAX1566, AUX1 and AUX2 are boost/flyback PWM controllers. On the MAX1567, AUX1 is a boost/flyback PWM controller, but AUX2 is an inverting PWM controller. On both devices, AUX3 is a boost/flyback controller that can be connected to regulate output voltage and/or current (for white-LED drive).

Figure 5 shows a functional diagram of an AUX boost controller channel. A sawtooth oscillator signal at OSC governs timing. At the start of each cycle, DL_ goes high, turning on the external NFET switch. The switch then turns off when the internally level-shifted sawtooth rises above CC_ or when the maximum duty cycle is exceeded. The switch remains off until the start of the next cycle. A transconductance error amplifier forms an integrator at CC_ to maintain high DC loop gain and accuracy.

The auxiliary controllers do not start until 1024 OSC cycles after the step-up DC-to-DC output is in regulation. If the auxiliary controller remains faulted for 100,000 OSC cycles (200ms at 500kHz), then all MAX1566/MAX1567 channels latch off.

Maximum Duty Cycle

The AUX PWM controllers have a guaranteed maximum duty cycle of 80%: all controllers can achieve at least 80% and typically reach 85%. In boost designs that employ continuous current, the maximum duty cycle limits the boost ratio so:

$$1 - V_{IN} / V_{OUT} \leq 80\%$$

With discontinuous inductor current, no such limit exists for the input/output ratio since the inductor has time to fully discharge before the next cycle begins.

AUX1

AUX1 can be used for conventional DC-to-DC boost and flyback designs (Figures 8 and 9). Its output (DL1) is designed to drive an N-channel MOSFET. Its feedback (FB1) threshold is 1.25V.

AUX2

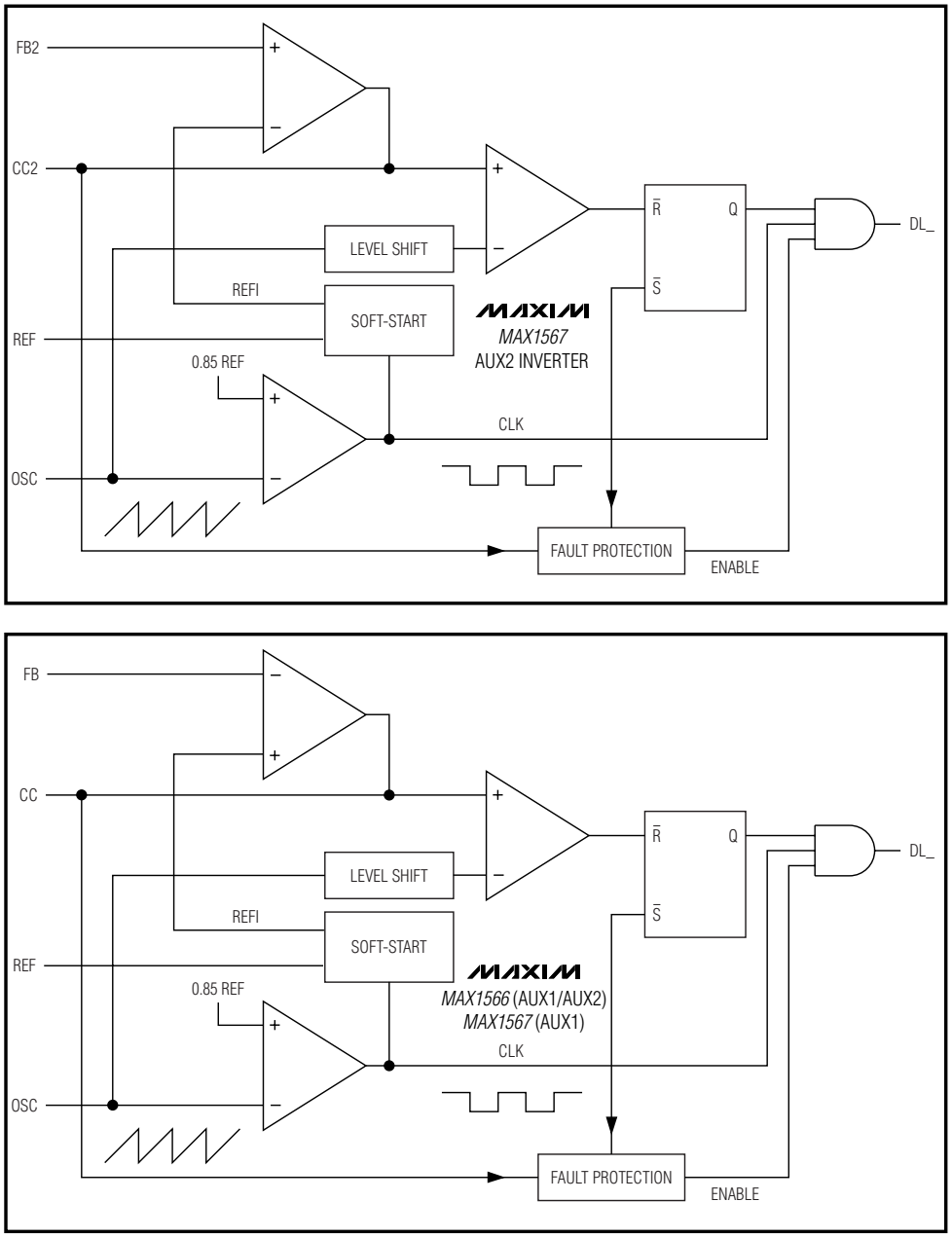
In the MAX1566, AUX2 is identical to AUX1. In the MAX1567, AUX2 is an inverting controller that generates a regulated negative output voltage, typically for CCD and LCD bias. This is useful in height-limited designs where transformers may not be desired.

The AUX2 MOSFET driver (DL2) in the MAX1567 is designed to drive P-channel MOSFETs. INDL2 biases the driver so V_{INDL2} is the high output level of DL2. INDL2 should be connected to the P-channel MOSFET source to ensure the MOSFET turns completely off when DL2 is high. See Figure 10 for a typical inverter circuit.

AUX3 DC-to-DC Controller, LED Driver

The AUX3 step-up DC-to-DC controller has two feedback inputs, FB3L and FB3H, with feedback thresholds of 0.2V (FB3L) and 1.25V (FB3H). If used as a conventional voltage-output step-up, FB3L is grounded and FB3H is used as the feedback input. In that case, AUX3 behaves exactly like AUX1.

If AUX3 is used as a switch-mode boost current source for white LEDs, FB3L provides current-sensing feedback, while FB3H provides (optional) open-LED overvoltage protection (Figure 7).



IN 1024 CLOCK CYCLES, SOFT-START RAMPS UP REFI FROM 0V TO V_{REF} IN MAX1566/MAX1567 AUX_ BOOST CONTROLLERS AND RAMPS DOWN REFI FROM V_{REF} TO 0V IN MAX1567 AUX2 INVERTER.

Figure 5. AUX Controller Functional Diagram

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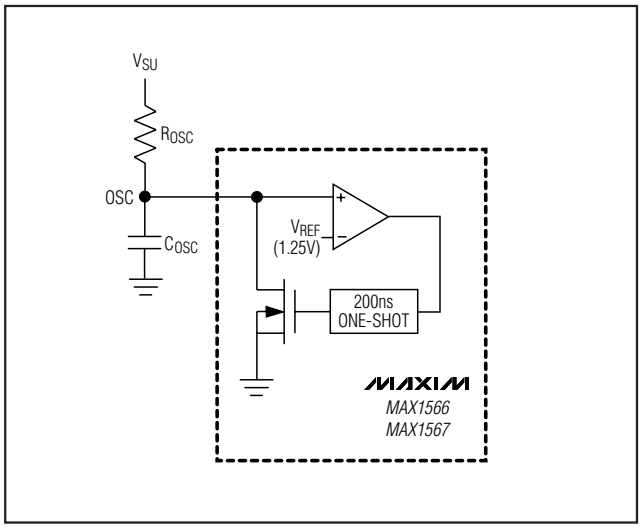

Figure 6. Oscillator Functional Diagram

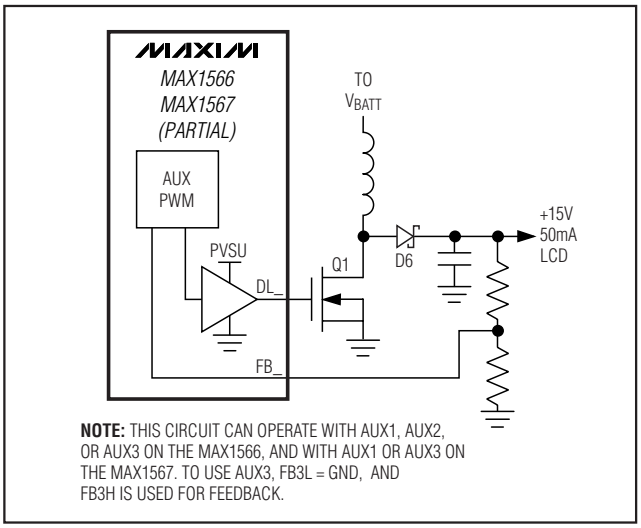

Figure 8. +15V LCD Bias with Basic Boost Topology

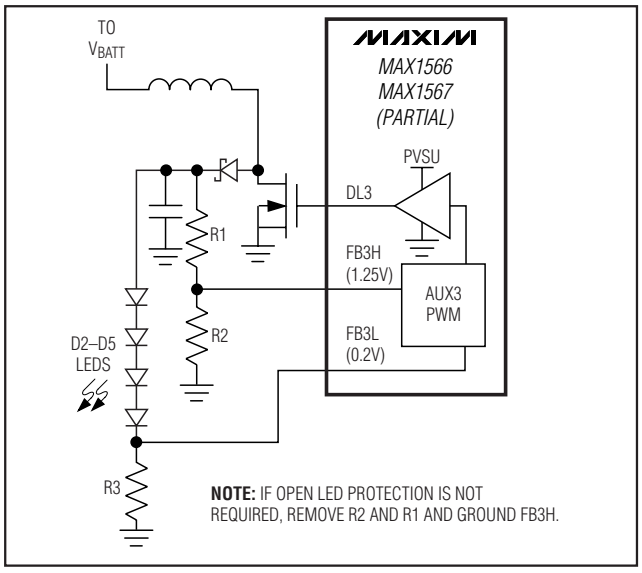

Figure 7. LED drive with open LED overvoltage protection is provided by the additional feedback input to AUX3, FB3H.

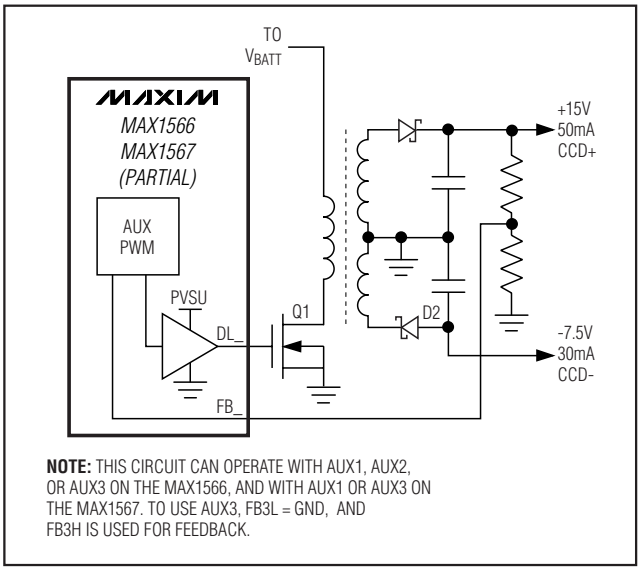

Figure 9. +15V and -7.5V CCD Bias with Transformer

Master-Slave Configurations

The MAX1566/MAX1567 support MAX1801 slave PWM controllers that obtain input power, a voltage reference, and an oscillator signal directly from the MAX1566/MAX1567 master. The master-slave configuration allows channels to be easily added and minimizes system cost by eliminating redundant circuitry. The slaves also control the harmonic content of noise because their operating frequency is synchronized to that of the MAX1566/MAX1567 master converter. A MAX1801 connection to the MAX1566/MAX1567 is shown in Figure 14.

Status Outputs ($\overline{SDOK}$, $\overline{AUX1OK}$, SCF)

The MAX1566/MAX1567 include three versatile status outputs that can provide information to the system. All are open-drain outputs and can directly drive MOSFET switches to facilitate sequencing, disconnect loads during overloads, or perform other hardware-based functions.

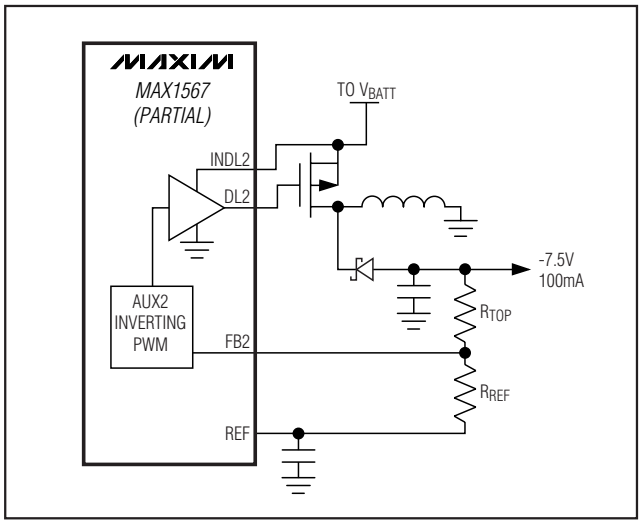

Figure 10. Regulated -7.5V Negative CCD (Bias is provided by conventional inverter (works only with the MAX1567).)

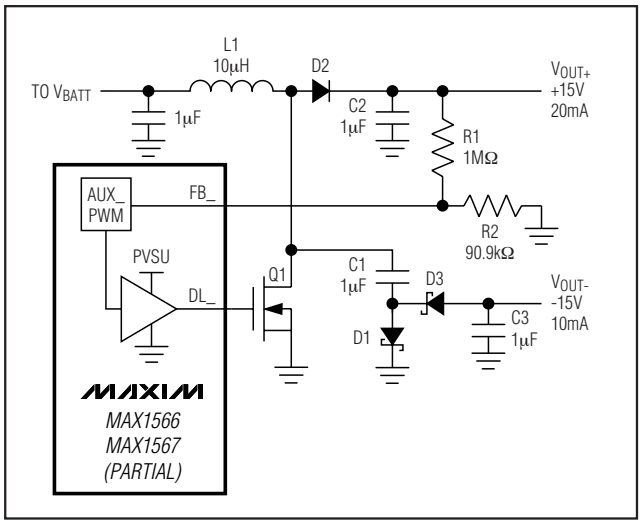

Figure 11. ±15V Output Using an AUX-Driven Boost with Charge-Pump Inversion

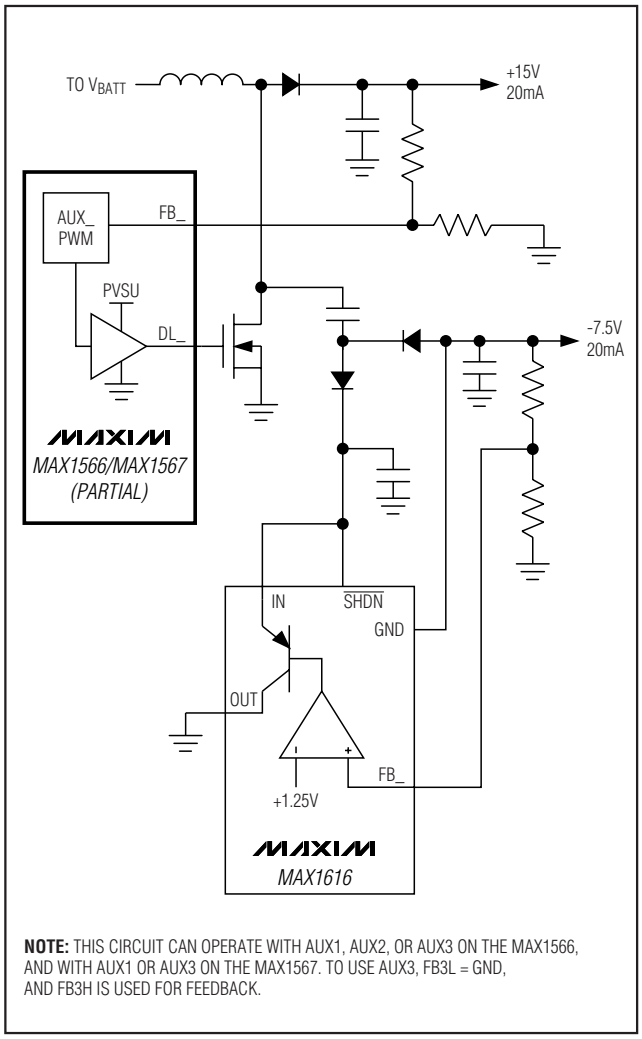

Figure 12. +15V and -7.5V CCD Bias Without Transformer Using Boost with a Diode-Capacitor Charge Pump (A positive-output linear regulator (MAX1616) can be used to regulate the negative output of the charge pump.)

$\overline{\text{SDOK}}$ pulls low when the step-down has successfully completed soft-start. $\overline{\text{SDOK}}$ goes high impedance in shutdown, overload, and thermal limit. A typical use for $\overline{\text{SDOK}}$ is to drive a P-channel MOSFET that connects 3.3V power to the CPU I/O after the CPU core is powered up (Figure 15), thus providing safe sequencing in hardware without system intervention.

$\overline{\text{AUX1OK}}$ pulls low when the AUX1 controller has successfully completed soft-start. $\overline{\text{AUX1OK}}$ goes high impedance in shutdown, overload, and thermal limit. A typical use for $\overline{\text{AUX1OK}}$ is to drive a P-channel MOSFET that connects 5V power to the CCD after the 15V CCD bias (generated by AUX1) is powered up (Figure 16).

SCF goes high (high impedance, open drain) when overload protection occurs. Under normal operation, SCF pulls low. SCF can drive a high-side P-channel MOSFET switch that can disconnect a load during power-up or when a channel turns off in response to a logic command or an overload. Several connections are possible for SCF. One is shown in Figure 17 where SCF provides load disconnect for the step-up on fault and power-up.

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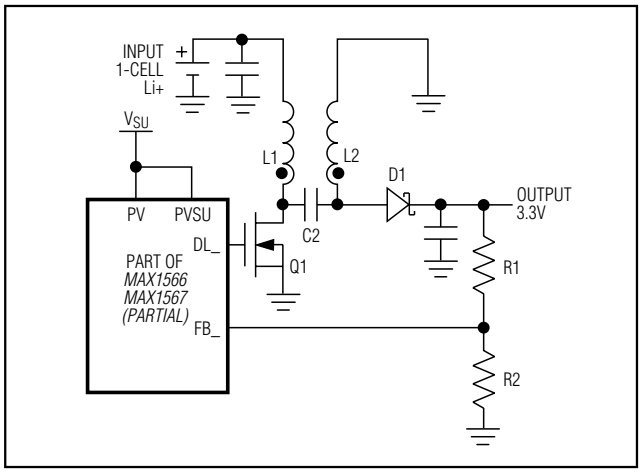

Figure 13. SEPIC Converter Additional Boost-Buck Channel

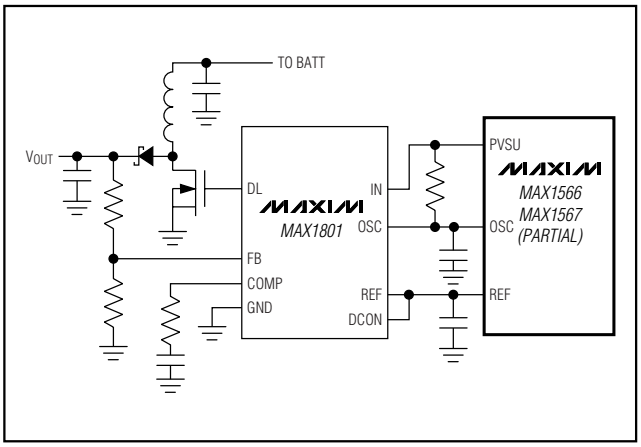

Figure 14. Adding a PWM Channel with an External MAX1801 Slave Controller

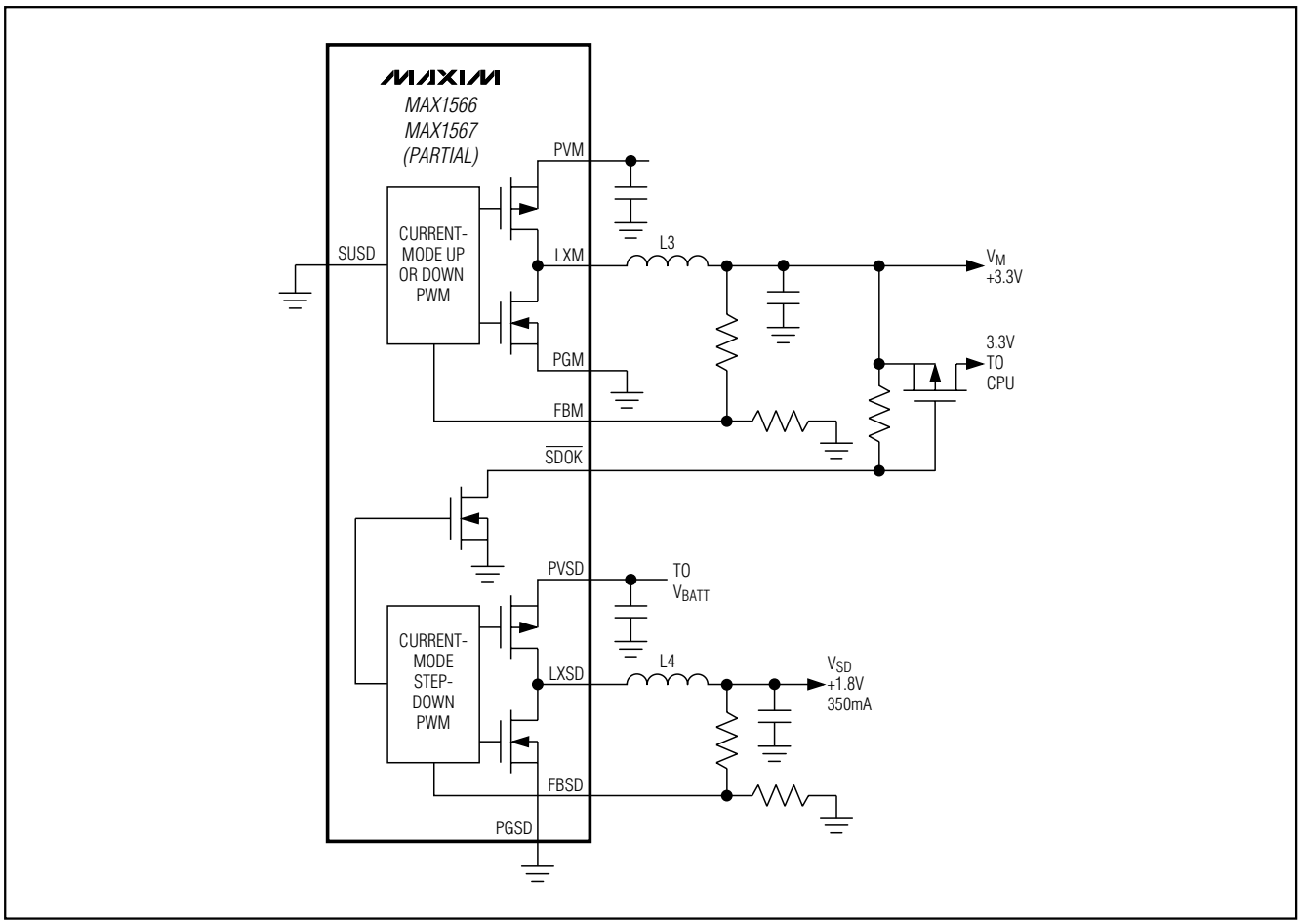

Figure 15. Using $\overline{SDOK}$ to Drive External PFET that Gates 3.3V Power to CPU After 1.8V Core Voltage Is in Regulation

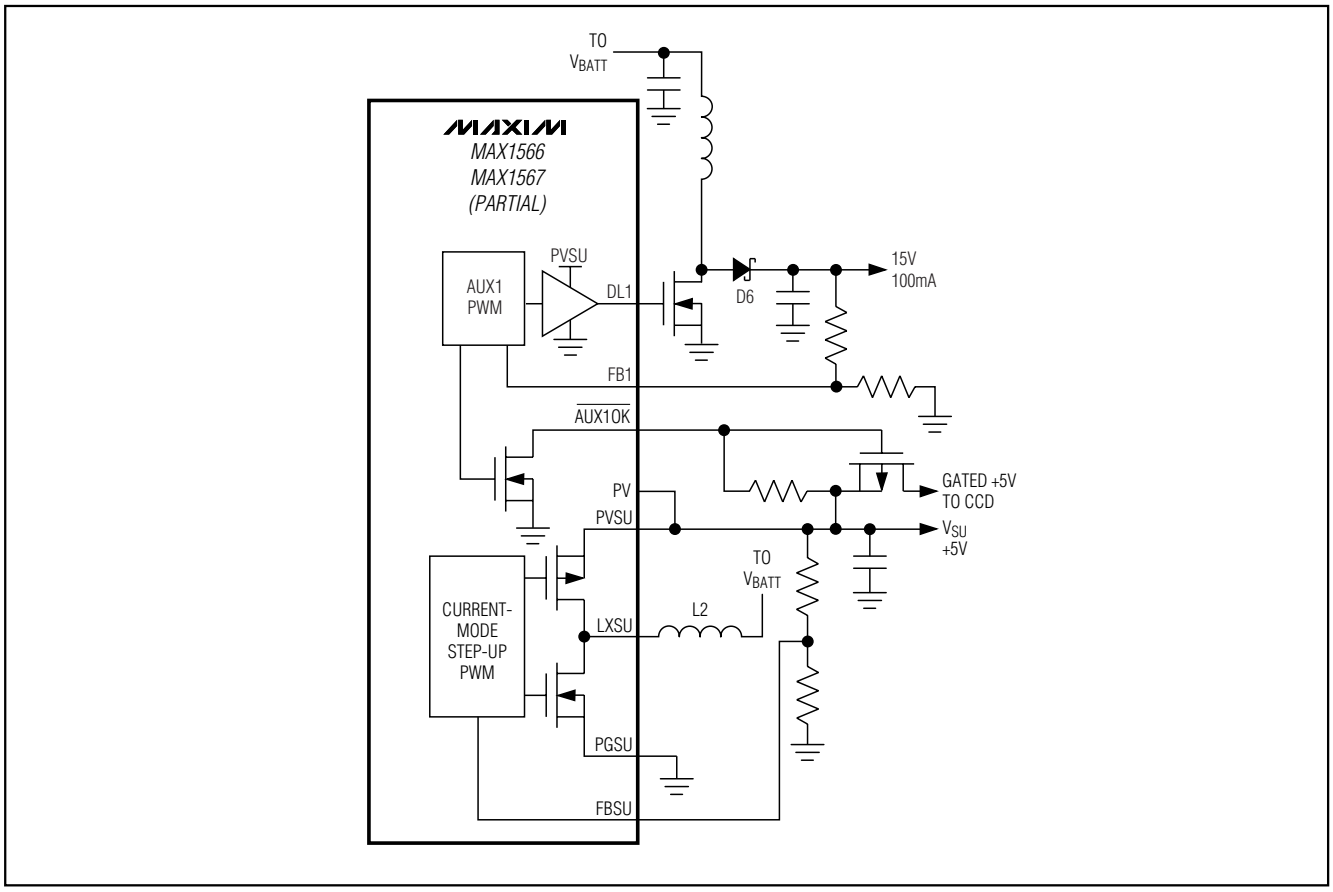

Figure 16. $\overline{AUX1OK}$ Drives an External PFET that Gates 5V Supply to the CCD After the +15V CCD Bias Supply Is Up

Soft-Start

The MAX1566/MAX1567 channels feature a soft-start function that limits inrush current and prevents excessive battery loading at startup by ramping the output voltage of each channel up to the regulation voltage. This is accomplished by ramping the internal reference inputs to each channel error amplifier from 0V to the 1.25V reference voltage over a period of 4096 oscillator cycles (16ms at 500kHz) when initial power is applied or when a channel is enabled.

The step-down soft-start ramp takes half the time (2048 clock cycles) of the other channel ramps. This allows the step-down and main outputs to track each other and rise at nearly the same dV/dt rate on power-up. Once the step-down output reaches its regulation point (1.5V or 1.8V typ), the main output (3.3V typ) continues to rise at the same ramp rate. See the *Typical Operating Characteristics* Main and Step-Down Startup Waveforms graphs.

Soft-start is not included in the step-up converter to avoid limiting startup capability with loading.

Fault Protection

The MAX1566/MAX1567 have robust fault and overload protection. After power-up, the device is set to detect an out-of-regulation state that could be caused by an overload or short. If any DC-to-DC converter channel (step-up, main, step-down, or any of the auxiliary controllers) remains faulted for 100,000 clock cycles (200ms at 500kHz), then **all** outputs latch off until the step-up DC-to-DC converter is reinitialized by the ONSU pin or by cycling the input power. The fault-detection circuitry for any channel is disabled during its initial turn-on soft-start sequence.

An exception to the standard fault behavior is that there is no 100,000 clock cycle delay in entering the fault state if the step-up output (PVSU) is dragged below its 2.5V UVLO threshold or is shorted. In this case, the

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step-up UVLO immediately triggers and shuts down all channels. The step-up then continues to attempt starting. If the step-up output short remains, these attempts cannot succeed since PVSU remains near ground.

If a soft-short or overload remains on PVSU, the startup oscillator switches the internal N-channel MOSFET, but fault is retriggered if regulation is not achieved by the end of the soft-start interval. If PVSU is dragged below the input, the overload is supplied by the body diode of the internal synchronous rectifier, or by a Schottky diode connected from the battery to PVSU. If desired, this overload current can be interrupted by a P-channel MOSFET controlled by SCF, as shown in Figure 17.

Reference

The MAX1566/MAX1567 has a precise 1.250V reference. Connect a 0.1µF ceramic bypass capacitor from REF to GND within 0.2in (5mm) of the REF pin. REF can source up to 200µA and is enabled whenever ONSU is high and PVSU is above 2.5V. The auxiliary controllers and MAX1801 slave controllers (if connected) each sink up to 30µA REF current during startup. In addition, the feedback network for the AUX2 inverter (MAX1567) also draws current from REF. If the 200µA REF load limit must be exceeded, buffer REF with an external op amp.

Oscillator

All DC-to-DC converter channels employ fixed-frequency PWM operation. The operating frequency is set by an RC network at the OSC pin. The range of usable settings is 100kHz to 1MHz. When MAX1801 slave controllers are added, they operate at the frequency set by OSC.

The oscillator uses a comparator, a 200ns one-shot, and an internal NFET switch in conjunction with an external timing resistor and capacitor (Figure 6). When the switch is open, the capacitor voltage exponentially approaches the step-up output voltage from zero with a time constant given by the product of R_{OSC} and C_{OSC}. The comparator output switches high when the capacitor voltage reaches V_{REF} (1.25V). In turn, the one-shot activates the internal MOSFET switch to discharge the capacitor for 200ns, and the cycle repeats. The oscillation frequency changes as the main output voltage ramps upward following startup. The oscillation frequency is then constant once the main output is in regulation.

Low-Voltage Startup Oscillator

The MAX1566/MAX1567 internal control and reference-voltage circuitry receive power from PVSU and do not function when PVSU is less than 2.5V. To ensure low-voltage startup, the step-up employs a low-voltage startup oscillator that activates at 0.9V if a Schottky rectifier is connected from V_{BATT} to PVSU (1.1V with no Schottky rectifier). The startup oscillator drives the internal N-channel MOSFET at LXSU until PVSU reaches 2.5V, at which point voltage control is passed to the current-mode PWM circuitry.

Once in regulation, the MAX1566/MAX1567 operate with inputs as low as 0.7V since internal power for the IC is supplied by PVSU. At low input voltages, the step-

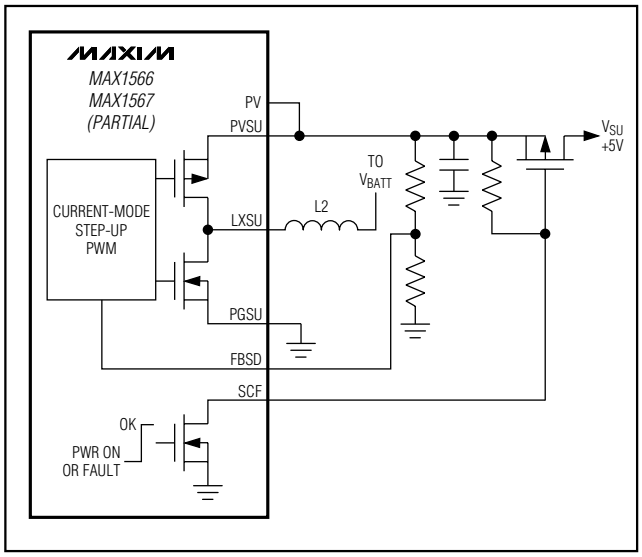

Figure 17. SCF Drives PFET Load Switch on 5V to Disconnect Load on Fault and Allow Full-Load Startup

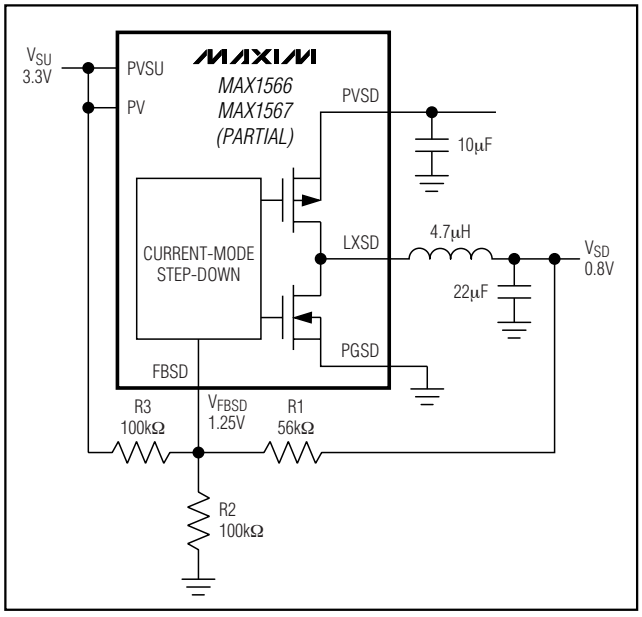

Figure 18. Setting PVSD for Outputs Below 1.25V

up may have difficulty starting into heavy loads (see the Minimum Startup Voltage vs. Load Current (OUTSU) graph in the *Typical Operating Characteristics*); however, this can be remedied by connecting an external P-channel load switch driven by SCF so the load is not connected until the PVSU is in regulation (Figure 17).

Shutdown

The step-up converter is activated with a high input at ONSU. The main converter (step-up or step-down) is activated by a high input on ONM. The step-down and auxiliary DC-to-DC converters 1, 2, and 3 activate with high inputs at ONSD, ON1, ON2, and ON3, respectively. The step-down, main, and AUX_ converters cannot be activated until PVSU is in regulation. For automatic startup, connect ON_ to PVSU or a logic level greater than 1.6V.

Design Procedure

Setting the Switching Frequency

Choose a switching frequency to optimize external component size or circuit efficiency for the particular application. Typically, switching frequencies between 400kHz and 500kHz offer a good balance between component size and circuit efficiency—higher frequencies generally allow smaller components, and lower frequencies give better conversion efficiency. The switching frequency is set with an external timing resistor (R_{OSC}) and capacitor (C_{OSC}). At the beginning of a cycle, the timing capacitor charges through the resistor until it reaches V_{REF}. The charge time, t_1, is as follows:

$$t_1 = -R_{OSC} \times (C_{OSC} + C_{par}) \times \ln (1 - 1.25 / V_{PVSU})$$

where C_{par} (15pF typ) is the parasitic capacitance at the OSC pin due to internal ESD protection structure and the die-to-package capacitance.

The internal comparator that compares the capacitor C_{OSC} voltage to the reference has a delay t_d of 50ns (typ). The capacitor voltage then decays to zero over time, t_2 = 200ns. The oscillator frequency is as follows:

$$f_{OSC} = 1 / (t_1 + t_d + t_2)$$

f_{OSC} can be set from 100kHz to 1MHz. Choose C_{OSC} between 22pF and 470pF. Determine R_{OSC}:

$$R_{OSC} = (200ns + 50ns - 1/ f_{OSC}) / ([C_{OSC} + C_{par}] \ln[1 - 1.25 / V_{PVSU}])$$

See the *Typical Operating Characteristics* for f_{OSC} vs. R_{OSC} using different values of C_{OSC}.

Setting Output Voltages

All MAX1566/MAX1567 output voltages are resistor set. The FB_ threshold is 1.25V for all channels except for FB3L (0.2V) on both devices and FB2 (inverter) on the MAX1567. When setting the voltage for any channel except the MAX1567 AUX2, connect a resistive voltage-divider from the channel output to the corresponding FB_ input and then to GND. The FB_ input bias current is less than 100nA, so choose the bottom-side (FB_-to-GND) resistor to be 100kΩ or less. Then calculate the top-side (output-to-FB_) resistor:

$$R_{TOP} = R_{BOTTOM}[(V_{OUT} / 1.25) - 1]$$

When using AUX3 to drive white LEDs (Figure 7), select the LED current-setting resistor (R3, Figure 7) using the following formula:

$$R3 = 0.2V / I_{LED}$$

The FB2 threshold on the MAX1567 is 0V. To set the AUX2 negative output voltage, connect a resistive voltage-divider from the negative output to the FB2 input, and then to REF. The FB2 input bias current is less than 100nA, so choose the REF-side (FB2-to-REF) resistor (R_{REF}) to be 100kΩ or less. Then calculate the top-side (output-to-FB2) resistor:

$$R_{TOP} = R_{REF}(-V_{OUT(AUX2)} / 1.25)$$

General Filter Capacitor Selection

The input capacitor in a DC-to-DC converter reduces current peaks drawn from the battery or other input power source and reduces switching noise in the controller. The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source.

The output capacitor keeps output ripple small and ensures control-loop stability. The output capacitor must also have low impedance at the switching frequency. Ceramic, polymer, and tantalum capacitors are suitable, with ceramic exhibiting the lowest ESR and high-frequency impedance.

Output ripple with a ceramic output capacitor is approximately as follows:

$$V_{RIPPLE} = I_{L(PEAK)}[1 / (2\pi \times f_{OSC} \times C_{OUT})]$$

If the capacitor has significant ESR, the output ripple component due to capacitor ESR is as follows:

$$V_{RIPPLE(ESR)} = I_{L(PEAK)} \times ESR$$

Output capacitor specifics are also discussed in each converter's *Compensation* section.

Step-Up Component Selection

This section describes component selection for the step-up, as well as for the main, if SUSD = PV.

The external components required for the step-up are an inductor, an input and output filter capacitor, and a compensation RC.

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The inductor is typically selected to operate with continuous current for best efficiency. An exception might be if the step-up ratio, (V_{OUT} / V_{IN}), is greater than 1 / (1 - D_{MAX}), where D_{MAX} is the maximum PWM duty factor of 80%.

When using the step-up channel to boost from a low input voltage, loaded startup is aided by connecting a Schottky diode from the battery to PVSU. See the Minimum Startup Voltage vs. Load Current graph in the *Typical Operating Characteristics*.

Step-Up Inductor

In most step-up designs, a reasonable inductor value (L_{IDEAL}) can be derived from the following equation, which sets continuous peak-to-peak inductor current at 1/2 the DC inductor current:

$$L_{IDEAL} = [2V_{IN(MAX)} \times D(1 - D)] / (I_{OUT} \times f_{OSC})$$

where D is the duty factor given by:

$$D = 1 - (V_{IN} / V_{OUT})$$

Given L_{IDEAL}, the consistent peak-to-peak inductor current is 0.5 I_{OUT} / (1 - D). The peak inductor current, $I_{IND(PK)}$ = 1.25 I_{OUT} / (1 - D).

Inductance values smaller than L_{IDEAL} can be used to reduce inductor size; however, if much smaller values are used, inductor current rises and a larger output capacitance may be required to suppress output ripple.

Step-Up Compensation

The inductor and output capacitor are usually chosen first in consideration of performance, size, and cost. The compensation resistor and capacitor are then chosen to optimize control-loop stability. In some cases, it may help to readjust the inductor or output-capacitor value to get optimum results. For typical designs, the component values in the circuit of Figure 1 yield good results.

The step-up converter employs current-mode control, thereby simplifying the control-loop compensation. When the converter operates with continuous inductor current (typically the case), a right-half-plane zero appears in the loop-gain frequency response. To ensure stability, the control-loop gain should cross over (drop below unity gain) at a frequency (f_C) much less than that of the right-half-plane zero.

The relevant characteristics for step-up channel compensation are as follows:

- Transconductance (from FB to CC), gm_{EA} (135µS)
- Current-sense amplifier transresistance, R_{CS} (0.3V/A)
- Feedback regulation voltage, V_{FB} (1.25V)
- Step-up output voltage, V_{SU}, in V
- Output load equivalent resistance, R_{LOAD}, in Ω = V_{OUT} / I_{LOAD}

The key steps for step-up compensation are as follows:

1) Place f_C sufficiently below the right-half-plane zero (RHPZ) and calculate C_C.
2) Select R_C based on the allowed load-step transient. R_C sets a voltage delta on the C_C pin that corresponds to load-current step.
3) Calculate the output-filter capacitor (C_{OUT}) required to allow the R_C and C_C selected.
4) Determine if C_P is required (if calculated to be >10pF).

For continuous conduction, the right-half-plane zero frequency (f_{RHPZ}) is given by the following:

$$f_{RHPZ} = V_{OUT}(1 - D)^2 / (2\pi \times L \times I_{LOAD})$$

where D = the duty cycle = 1 - (V_{IN} / V_{OUT}), L is the inductor value, and I_{LOAD} is the maximum output current. Typically target crossover (f_C) for 1/6 of the RHPZ. For example, if we assume f_{OSC} = 500kHz, V_{IN} = 2.5V, V_{OUT} = 5V, and I_{OUT} = 0.5A, then R_{LOAD} = 10Ω. If we select L = 4.7µH, then:

$f_{RHPZ} = 5 (2.5 / 5)^2 / (2\pi \times 4.7 \times 10^{-6} \times 0.5) = 84.65kHz$

Choose f_C = 14kHz. Calculate C_C:

$C_C = (V_{FB} / V_{OUT})(R_{LOAD} / R_{CS})(gm / 2\pi \times f_C)(1 - D)$
$= (1.25 / 5)(10 / 0.3) \times [135µS / (6.28 \times 14kHz)] (2/5)$
$= 6.4nF$

Choose 6.8nF.

Now select R_C so transient-droop requirements are met. As an example, if 4% transient droop is allowed, the input to the error amplifier moves 0.04 x 1.25V, or 50mV. The error-amp output drives 50mV x 135µS, or 6.75µA, across R_C to provide transient gain. Since the current-sense transresistance is 0.3V/A, the value of R_C that allows the required load-step swing is as follows:

$$R_C = 0.3 I_{IND(PK)} / 6.75µA$$

In a step-up DC-to-DC converter, if L_{IDEAL} is used, output current relates to inductor current by:

$$I_{IND(PK)} = 1.25 I_{OUT} / (1 - D) = 1.25 I_{OUT} \times V_{OUT} / V_{IN}$$

So, for a 500mA output load step with V_{IN} = 2.5V and V_{OUT} = 5V:

$$R_C = [1.25(0.3 \times 0.5 \times 5) / 2)] / 6.75µA = 69.4kΩ$$

Note that the inductor does not limit the response in this case since it can ramp at 2.5V / 4.7µH, or 530mA/µs.

The output filter capacitor is then chosen so the C_{OUT} R_{LOAD} pole cancels the R_C C_C zero:

$$C_{OUT} \times R_{LOAD} = R_C \times C_C$$

For the example:

$$C_{OUT} = 68k\Omega \times 6.8nF / 10\Omega = 46\mu F$$

Choose 47µF for C_{OUT}. If the available C_{OUT} is substantially different from the calculated value, insert the available C_{OUT} value into the above equation and recalculate R_C. Higher substituted C_{OUT} values allow a higher R_C, which provides higher transient gain and consequently less transient droop.

If the output filter capacitor has significant ESR, a zero occurs at the following:

$$Z_{ESR} = 1 / (2\pi \times C_{OUT} \times R_{ESR})$$

If $Z_{ESR} > f_C$, it can be ignored, as is typically the case with ceramic output capacitors. If Z_{ESR} is less than f_C, it should be cancelled with a pole set by capacitor C_P connected from CC to GND:

$$C_P = C_{OUT} \times R_{ESR} / R_C$$

If C_P is calculated to be <10pF, it can be omitted.

Step-Down Component Selection

This section describes component selection for the step-down converter, and for the main converter if used in step-down mode (SUSD = GND).

Step-Down Inductor

The external components required for the step-down are an inductor, input and output filter capacitors, and compensation RC network.

The MAX1566/MAX1567 step-down converter provides best efficiency with continuous inductor current. A reasonable inductor value (L_{IDEAL}) can be derived from the following:

$$L_{IDEAL} = [2(V_{IN}) \times D(1 - D)] / I_{OUT} \times f_{OSC}$$

This sets the peak-to-peak inductor current at 1/2 the DC inductor current. D is the duty cycle:

$$D = V_{OUT} / V_{IN}$$

Given L_{IDEAL}, the peak-to-peak inductor current is 0.5 I_{OUT}. The absolute-peak inductor current is 1.25 I_{OUT}. Inductance values smaller than L_{IDEAL} can be used to reduce inductor size; however, if much smaller values are used, inductor current rises, and a larger output capacitance may be required to suppress output ripple. Larger values than L_{IDEAL} can be used to obtain higher output current, but typically with larger inductor size.

Step-Down Compensation

The relevant characteristics for step-down compensation are as follows:

- Transconductance (from FB to C_C), gm_{EA} (135µS)
- Step-down slope-compensation pole, $P_{SLOPE} = V_{IN} / (\pi L)$
- Current-sense amplifier transresistance, R_{CS} (0.6V/A)
- Feedback-regulation voltage, V_{FB} (1.25V)
- Step-down output voltage, V_{SD}, in V
- Output-load equivalent resistance, R_{LOAD}, in $\Omega = V_{OUT} / I_{LOAD}$

The key steps for step-down compensation are as follows:

1) Set the compensation RC to zero to cancel the R_{LOAD} C_{OUT} pole.
2) Set the loop crossover below the lower of 1/5 the slope compensation pole or 1/5 the switching frequency.

If we assume V_{IN} = 2.5V, V_{OUT} = 1.8V, and I_{OUT} = 350mA, then $R_{LOAD} = 5.14\Omega$.

If we select f_{OSC} = 500kHz and L = 5.6µH.

$P_{SLOPE} = V_{IN} / (\pi L)$ = 142kHz, so choose f_C = 24kHz and calculate C_C:

$$C_C = (V_{FB} / V_{OUT})(R_{LOAD} / R_{CS})(gm / 2\pi \times f_C)$$
$$= (1.25 / 1.8)(5.14 / 0.6) \times [135\mu S / (6.28 \times 24kHz)]$$
$$= 6.4nF$$

Choose 6.8nF.

Now select R_C so transient-droop requirements are met. As an example, if 4% transient droop is allowed, the input to the error amplifier moves 0.04 x 1.25V, or 50mV. The error-amp output drives 50mV x 135µS, or 6.75µA across R_C to provide transient gain. Since the current-sense transresistance is 0.6V/A, the value of R_C that allows the required load-step swing is as follows:

$$R_C = 0.6\ I_{IND(PK)} / 6.75\mu A$$

In a step-down DC-to-DC converter, if L_{IDEAL} is used, output current relates to inductor current by the following:

$$I_{IND(PK)} = 1.25\ I_{OUT}$$

So for a 250mA output load step with V_{IN} = 2.5V and V_{OUT} = 1.8V:

$$R_C = (1.25 \times 0.6 \times 0.25) / 6.75\mu A = 27.8k\Omega$$

Choose 27kΩ.

Note that the inductor does somewhat limit the response in this case since it ramps at (V_{IN} - V_{OUT}) / 5.6µH, or (2.5 - 1.8) / 5.6µH = 125mA/µs.

The output filter capacitor is then chosen so the C_{OUT} R_{LOAD} pole cancels the R_C C_C zero:

$$C_{OUT} \times R_{LOAD} = R_C \times C_C$$

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For the example:

$$C_{OUT} = 27k\Omega \times 6.8nF / 5.14\Omega = 35.7\mu F$$

Since ceramic capacitors are common in either 22µF or 47µF values, 22µF is within a factor of two of the ideal value and still provides adequate phase margin for stability. If the output filter capacitor has significant ESR, a zero occurs at the following:

$$Z_{ESR} = 1 / (2\pi \times C_{OUT} \times R_{ESR})$$

If $Z_{ESR} > f_C$, it can be ignored, as is typically the case with ceramic output capacitors. If $Z_{ESR} < f_C$, it should be cancelled with a pole set by capacitor C_P connected from C_C to GND:

$$C_P = C_{OUT} \times R_{ESR} / R_C$$

If C_P is calculated to be <10pF, it can be omitted.

AUX Controller Component Selection

External MOSFET

All MAX1566/MAX1567 AUX controllers drive external logic-level MOSFETs. Significant MOSFET selection parameters are as follows:

- On-resistance ($R_{DS(ON)}$)
- Maximum drain-to-source voltage ($V_{DS(MAX)}$)
- Total gate charge (Q_G)
- Reverse transfer capacitance (C_{RSS})

On the MAX1566, all AUX drivers are designed for N-channel MOSFETs. On the MAX1567, AUX2 is a DC-to-DC inverter, so DL2 is designed to drive a P-channel MOSFET. In both devices, the driver outputs DL1 and DL3 swing between PVSU and GND. MOSFET driver DL2 swings between INDL2 and GND.

Use a MOSFET with on-resistance specified with gate drive at or below the main output voltage. The gate charge, Q_G, includes all capacitance associated with charging the gate and helps to predict MOSFET transition time between on and off states. MOSFET power dissipation is a combination of on-resistance and transition losses. The on-resistance loss is as follows:

$$P_{RDSON} = D \times I_L^2 \times R_{DS(ON)}$$

where D is the duty cycle, I_L is the average inductor current, and $R_{DS(ON)}$ is MOSFET on-resistance. The transition loss is approximately as follows:

$$P_{TRANS} = (V_{OUT} \times I_L \times f_{OSC} \times t_T) / 3$$

where V_{OUT} is the output voltage, I_L is the average inductor current, f_{OSC} is the switching frequency, and t_T is the transition time. The transition time is approximately Q_G / I_G, where Q_G is the total gate charge, and I_G is the gate-drive current (0.5A typ).

The total power dissipation in the MOSFET is as follows:

$$P_{MOSFET} = P_{RDSON} + P_{TRANS}$$

Diode

For most AUX applications, a Schottky diode rectifies the output voltage. Schottky low forward voltage and fast recovery time provide the best performance in most applications. Silicon signal diodes (such as 1N4148) are sometimes adequate in low-current (<10mA), high-voltage (>10V) output circuits where the output voltage is large compared to the diode forward voltage.

AUX Compensation

The auxiliary controllers employ voltage-mode control to regulate their output voltage. Optimum compensation depends on whether the design uses continuous or discontinuous inductor current.

AUX Step-Up, Discontinuous Inductor Current

When the inductor current falls to zero on each switching cycle, it is described as discontinuous. The inductor is not utilized as efficiently as with continuous current, but in light-load applications this often has little negative impact since the coil losses may already be low compared to other losses. A benefit of discontinuous inductor current is more flexible loop compensation, and no maximum duty-cycle restriction on boost ratio.

To ensure discontinuous operation, the inductor must have a sufficiently low inductance to fully discharge on each cycle. This occurs when:

$$L < [V_{IN}^2 (V_{OUT} - V_{IN}) / V_{OUT}^3] [R_{LOAD} / (2f_{OSC})]$$

A discontinuous current boost has a single pole at the following:

$$f_P = (2V_{OUT} - V_{IN}) / (2\pi \times R_{LOAD} \times C_{OUT} \times V_{OUT})$$

Choose the integrator cap so the unity-gain crossover, f_C, occurs at $f_{OSC} / 10$ or lower. Note that for many AUX circuits, such as those powering motors, LEDs, or other loads that do not require fast transient response, it is often acceptable to overcompensate by setting f_C at $f_{OSC} / 20$ or lower.

C_C is then determined by the following:

$$C_C = [2V_{OUT} \times V_{IN} / ((2V_{OUT} - V_{IN}) \times V_{RAMP})] [V_{OUT} / (K(V_{OUT} - V_{IN}))]^{1/2} [(V_{FB} / V_{OUT})(g_M / (2\pi \times f_C))]$$

where:

$$K = 2L \times f_{OSC} / R_{LOAD}$$

and V_{RAMP} is the internal slope-compensation voltage ramp of 1.25V.

The C_C R_C zero is then used to cancel the f_P pole, so:

$$R_C = R_{LOAD} \times C_{OUT} \times V_{OUT} / [(2V_{OUT} - V_{IN}) \times C_C]$$

AUX Step-Up, Continuous Inductor Current

Continuous inductor current can sometimes improve boost efficiency by lowering the ratio between peak inductor current and output current. It does this at the expense of a larger inductance value that requires larger size for a given current rating. With continuous inductor-current boost operation, there is a right-half-plane zero, Z_{RHP}, at the following:

$$Z_{RHP} = (1 - D)^2 \times R_{LOAD} / (2\pi \times L)$$

where $(1 - D) = V_{IN} / V_{OUT}$ (in a boost converter).

There is a complex pole pair at the following:

$$f_0 = V_{OUT} / [2\pi \times V_{IN} (L \times C_{OUT})^{1/2}]$$

If the zero due to the output capacitance and ESR is less than 1/10 the right-half-plane zero:

$$Z_{COUT} = 1 / (2\pi \times C_{OUT} \times R_{ESR}) < Z_{RHP} / 10$$

Then choose C_C so the crossover frequency f_C occurs at Z_{COUT}. The ESR zero provides a phase boost at crossover:

$$C_C = (V_{IN} / V_{RAMP}) (V_{FB} / V_{OUT}) [g_M / (2\pi \times Z_{COUT})]$$

Choose R_C to place the integrator zero, $1 / (2\pi \times R_C \times C_C)$, at f_0 to cancel one of the pole pairs:

$$R_C = V_{IN}(L \times C_{OUT})^{1/2} / (V_{OUT} \times C_C)$$

If Z_{COUT} is not less than $Z_{RHP} / 10$ (as is typical with ceramic output capacitors) and continuous conduction is required, then cross the loop over before Z_{RHP} and f_0:

$$f_C < f_0 / 10, \text{ and } f_C < Z_{RHP} / 10$$

In that case:

$$C_C = (V_{IN} / V_{RAMP}) (V_{FB} / V_{OUT}) (g_M / (2\pi \times f_C))$$

Place:

$1 / (2\pi \times R_C \times C_C) = 1 / (2\pi \times R_{LOAD} \times C_{OUT})$, so that

$$R_C = R_{LOAD} \times C_{OUT} / C_C$$

Or, reduce the inductor value for discontinuous operation.

MAX1567 AUX2 Inverter Compensation, Discontinuous Inductor Current

If the load current is very low (≤40mA), discontinuous current is preferred for simple loop compensation and freedom from duty-cycle restrictions on the inverter input-output ratio. To ensure discontinuous operation, the inductor must have a sufficiently low inductance to fully discharge on each cycle. This occurs when:

$$L < [V_{IN} / (|V_{OUT}| + V_{IN})]^2 R_{LOAD} / (2f_{OSC})$$

A discontinuous current inverter has a single pole at the following:

$$f_P = 2 / (2\pi \times R_{LOAD} \times C_{OUT})$$

Choose the integrator cap so the unity-gain crossover, f_C, occurs at $f_{OSC} / 10$ or lower. Note that for many AUX circuits that do not require fast transient response, it is often acceptable to overcompensate by setting f_C at $f_{OSC} / 20$ or lower.

C_C is then determined by the following:

$$C_C = [V_{IN} / (K^{1/2} \times V_{RAMP})] [V_{REF} / (V_{OUT} + V_{REF})] [g_M / (2\pi \times f_C)]$$

where $K = 2L \times f_{OSC} / R_{LOAD}$, and V_{RAMP} is the internal slope-compensation voltage ramp of 1.25V.

The C_C R_C zero is then used to cancel the f_P pole, so:

$$R_C = (R_{LOAD} \times C_{OUT}) / (2C_C)$$

MAX1567 AUX2 Inverter Compensation, Continuous Inductor Current

Continuous inductor current may be more suitable for larger load currents (50mA or more). It improves efficiency by lowering the ratio between peak inductor current and output current. It does this at the expense of a larger inductance value that requires larger size for a given current rating. With continuous inductor-current inverter operation, there is a right-half-plane zero, Z_{RHP}, at:

$$Z_{RHP} = [(1 - D)^2 / D] \times R_{LOAD} / (2\pi \times L)$$

where $D = |V_{OUT}| / (|V_{OUT}| + V_{IN})$ (in an inverter).

There is a complex pole pair at:

$$f_0 = (1 - D) / (2\pi (L \times C)^{1/2})$$

If the zero due to the output-capacitor capacitance and ESR is less than 1/10 the right-half-plane zero:

$$Z_{COUT} = 1 / (2\pi \times C_{OUT} \times R_{ESR}) < Z_{RHP} / 10$$

Then choose C_C such that the crossover frequency f_C occurs at Z_{COUT}. The ESR zero provides a phase boost at crossover:

$$C_C = (V_{IN} / V_{RAMP}) [V_{REF} / (V_{REF} + |V_{OUT}|)] [g_M / (2\pi \times Z_{COUT})]$$

Choose R_C to place the integrator zero, $1 / (2\pi \times R_C \times C_C)$, at f_0 to cancel one of the pole pairs:

$$R_C = (L \times C_{OUT})^{1/2} / [(1 - D) \times C_C]$$

If Z_{COUT} is not less than $Z_{RHP} / 10$ (as is typical with ceramic output capacitors) and continuous conduction is required, then cross the loop over before Z_{RHP} and f_0:

$$f_C < f_0 / 10, \text{ and } f_C < Z_{RHP} / 10$$

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In that case:

$$C_C = (V_{IN} / V_{RAMP}) [V_{REF} / (V_{REF} + |V_{OUT}|)] [g_M / (2\pi \times f_C)]$$

Place:

$$1 / (2\pi \times R_C \times C_C) = 1 / (2\pi \times R_{LOAD} \times C_{OUT}), \text{ so that}$$

$$R_C = R_{LOAD} \times C_{OUT} / C_C$$

Or, reduce the inductor value for discontinuous operation.

Applications Information

Typical Operating Circuits

Figures 1, 2, and 3 show connections for AA and Li+ battery arrangements. Figures 7–13 show various connections for the AUX1, 2, and 3 controllers. Figures 15, 16, and 17 show various connections for the $\overline{SDOK}$, $\overline{AUX1OK}$, and SCF outputs.

Figure 1. Typical Operating Circuit for One Li+ Cell

In this connection, the main converter is operated as a step-down (SUSD = GND) and is powered from PVSU. This provides boost-buck operation for the main 3.3V output so a regulated output is maintained over the Li+ 2.7V to 4.2V cell voltage range. The compound efficiency from the battery to the 3.3V output reaches 90%.

The step-down 1.8V (core) output is powered directly from V_{BATT}.

The CCD and LCD voltages are generated with a transformerless design. AUX1 generates +15V for CCD positive and LCD bias. The MAX1567 AUX2 inverter generates -7.5V for negative CCD bias. The AUX3 controller generates a regulated current for a series network of four white LEDs that backlight the LCD.

Figure 2. Typical Operating Circuit for 2 AA Cells

Figure 2 is optimized for 2-cell AA inputs (1.5V to 3.7V) by connecting the step-down input (PVSD) to the main output (PVM). The main 3.3V output operates directly from the battery as a step-up (SUSD = PVSD). The 1.8V core output now operates as a boost-buck with efficiency up to 90%. The rest of the circuit is unchanged from Figure 1.

Figure 3. Typical Operating Circuit for 2 AA Cells and 1-Cell Li+

The MAX1566/MAX1567 can also allow either 1-cell Li+ or 2 AA cells to power the same design. If the step-down and main inputs are both connected to PVSU, then both the 3.3V and 1.8V outputs operate as boost-buck converters. There is an efficiency penalty compared to stepping down VSD directly from the battery, but that is not possible with a 1.5V input.

Furthermore, the cascaded boost-buck efficiency compares favorably with other boost-buck techniques.

LED, LCD, and Other Boost Applications

Any AUX channel (except for the AUX2 inverter on the MAX1567) can be used for a wide variety of step-up applications. These include generating 5V or some other voltage for motor or actuator drive, generating 15V or a similar voltage for LCD bias, or generating a step-up current source to efficiently drive a series array of white LEDs to display backlighting. Figures 7 and 8 show examples of these applications.

Multiple-Output Flyback Circuits

Some applications require multiple voltages from a single converter channel. This is often the case when generating voltages for CCD bias or LCD power. Figure 9 shows a two-output flyback configuration with an AUX channel. The controller drives an external MOSFET that switches the transformer primary. Two transformer secondaries generate the output voltages. Only one positive output voltage can be fed back, so the other voltages are set by the turns-ratio of the transformer secondaries. The load stability of the other secondary voltages depends on transformer leakage inductance and winding resistance. Voltage regulation is best when the load on the secondary that is not fed back is small compared to the load on the one that is fed back. Regulation also improves if the load-current range is limited. Consult the transformer manufacturer for the proper design for a given application.

Transformerless Inverter for Negative CCD Bias (AUX2, MAX1567)

On the MAX1567, AUX2 is set up to drive an external P-channel MOSFET in an inverting configuration. DL2 drives low to turn on the MOSFET, and FB2 has inverted polarity and a 0V threshold. This is useful for generating negative CCD bias without a transformer, particularly with high pixel-count cameras that have a greater negative CCD load current. Figure 10 shows an example circuit.

Boost with Charge Pump for Positive and Negative Outputs

Another method of producing bipolar output voltages without a transformer is with an AUX controller and a charge-pump circuit, as shown in Figure 11. When MOSFET Q1 turns off, the voltage at its drain rises to supply current to V_{OUT+}. At the same time, C1 charges to the voltage V_{OUT+} through D1. When the MOSFET turns on, C1 discharges through D3, thereby charging C3 to V_{OUT-} minus the drop across D3 to create roughly the same voltage as V_{OUT+} at V_{OUT-}, but with inverted polarity.

If different magnitudes are required for the positive and negative voltages, a linear regulator can be used at one of the outputs to achieve the desired voltages. One such connection is shown in Figure 12. This circuit is somewhat unique in that a **positive-output** linear regulator can regulate a negative voltage output. It does this by controlling the charge current flowing to the flying capacitor rather than directly regulating at the output.

SEPIC Boost-Buck

The MAX1566/MAX1567s' internal switch step-up, main, and step-down converters can be cascaded to make a high-efficiency boost-buck converter, but it is sometimes desirable to build a second boost-buck converter with an AUX_ controller.

One type of step-up/step-down converter is the SEPIC, shown in Figure 13. Inductors L1 and L2 can be separate inductors or can be wound on a single core and coupled like a transformer. Typically, a coupled inductor improves efficiency since some power is transferred through the coupling so less power passes through the coupling capacitor (C2). Likewise, C2 should have low ESR to improve efficiency. The ripple-current rating must be greater than the larger of the input and output currents. The MOSFET (Q1) drain-source voltage rating and the rectifier (D1) reverse-voltage rating must exceed the sum of the input and output voltages. Other types of step-up/step-down circuits are a flyback converter and a step-up converter followed by a linear regulator.

Adding a MAX1801 Slave

The MAX1801 is a 6-pin, SOT-slave, DC-to-DC controller that can be connected to generate additional output voltages. It does not generate its own reference or oscillator. Instead, it uses the reference and oscillator of the MAX1566/MAX1567 (Figure 14). The MAX1801 controller operation and design are similar to that of the MAX1566/MAX1567 AUX controllers. All comments in the *AUX Controller Component Selection* section also apply to add-on MAX1801 slave controllers. For more details, refer to the MAX1801 data sheet.

Applications for Status Outputs

The MAX1566/MAX1567 have three status outputs: $\overline{SDOK}$, $\overline{AUX1OK}$, and SCF. These monitor the output of the step-down channel, the AUX1 channel, and the status of the overload-short-circuit protection. Each output is open drain to allow the greatest flexibility. Figures 15, 16, and 17 show some possible connections for these outputs.

Using $\overline{SDOK}$ and $\overline{AUX1OK}$ for Power Sequencing

$\overline{SDOK}$ goes low when the step-down reaches regulation. Some microcontrollers with low-voltage cores require that the high-voltage (3.3V) I/O rail not be powered up until the core has a valid supply. The circuit in Figure 15 accomplishes this by driving the gate of a PFET connected between the 3.3V output and the processor I/O supply.

Figure 16 shows a similar application where $\overline{AUX1OK}$ gates 5V power to the CCD only after the +15V output is in regulation.

Alternately, power sequencing can also be implemented by connecting RC networks to delay the appropriate converter ON_ inputs.

Using SCF for Full-Load Startup

The SCF output goes low only after the step-up reaches regulation. It can be used to drive a P-channel MOSFET switch that turns off the load of a selected supply in the event of an overload. Or, it can remove the load until the supply reaches regulation, effectively allowing full-load startup. Figure 17 shows such a connection for the step-up output.

Setting V_{SD} Below 1.25V

The step-down feedback voltage is 1.25V. With a standard two-resistor feedback network, the output voltage can be set to values between 1.25V and the input voltage. If a step-down output voltage **less** than 1.25V is desired, it can be set by adding a third feedback resistor from FBSD to a voltage higher than 1.25V. The step-up or main outputs are convenient for this, as shown in Figure 18.

The equation governing output voltage in Figure 18's circuit is as follows:

$$0 = [(V_{SD} - V_{FBSD}) / R1] + [(0 - V_{FBSD}) / R2] + [(V_{SU} - V_{FBSD}) / R3]$$

where V_{SD} is the output voltage, V_{FBSD} is 1.25V, and V_{SU} is the step-up output voltage. Any available voltage that is higher than 1.25V can be used as the connection point for R3 in Figure 18, and for the V_{SD} term in the equation. Since there are multiple solutions for R1, R2, and R3, the above equation cannot be written in terms of one resistor. The best method for determining resistor values is to enter the above equation into a spreadsheet and test estimated resistor values. A good starting point is with 100kΩ at R2 and R3.

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Designing a PC Board

Good PC board layout is important to achieve optimal performance from the MAX1566/MAX1567. Poor design can cause excessive conducted and/or radiated noise. Conductors carrying discontinuous currents and any high-current path should be made as short and wide as possible. A separate low-noise ground plane containing the reference and signal grounds should connect to the power-ground plane at only one point to minimize the effects of power-ground currents. Typically, the ground planes are best joined right at the IC.

Keep the voltage-feedback network very close to the IC, preferably within 0.2in (5mm) of the FB_ pin. Nodes with high dV/dt (switching nodes) should be kept as small as possible and should be routed away from high-impedance nodes such as FB_. Refer to the MAX1566/MAX1567 EV kit data sheet for a full PC board example.

Chip Information

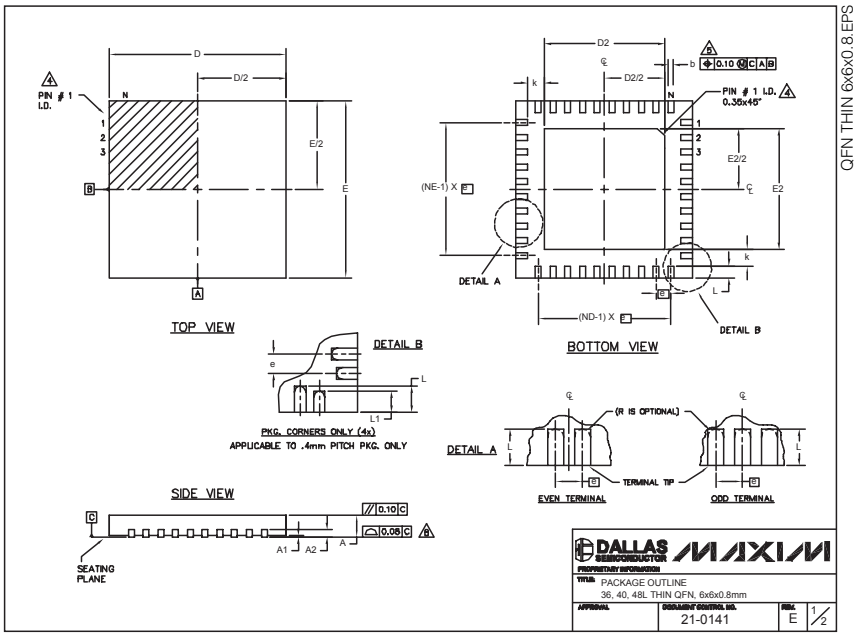
TRANSISTOR COUNT: 9420

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QFN THIN 6x6x0.8.EPS



COMMON DIMENSIONS									
PKG.	36L 6x6			40L 6x6			48L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
e	0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	0.35	0.45
L	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	–	–	–	–	–	–	0.30	0.40	0.50
N	36			40			48		
ND	9			10			12		
NE	9			10			12		
JEDEC	WJJD-1			WJJD-2			–		

EXPOSED PAD VARIATIONS							DOWN BONDS ALLOWED
PKG. CODES	D2			E2			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T3666-1	3.60	3.70	3.80	3.60	3.70	3.80	NO
T3666-2	3.60	3.70	3.80	3.60	3.70	3.80	YES
T3666-3	3.60	3.70	3.80	3.60	3.70	3.80	NO
T4066-1	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20	YES
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20	YES
T4066-4	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4866-1	4.20	4.30	4.40	4.20	4.30	4.40	YES

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH PACKAGE T4866-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE
36, 40, 48L THIN QFN, 6x6x0.8mm
APPROVAL
DOCUMENT CONTROL NO. 21-0141
REV. E
2/2

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