MAX16904

2.1MHz, High-Voltage, 600mA Mini-Buck Converter

General Description

The MAX16904 is a small, synchronous buck converter with integrated high-side and low-side switches. The device is designed to deliver 600mA with input voltages from +3.5V to +28V while using only 25µA quiescent current at no load. Voltage quality can be monitored by observing the PGOOD signal. The MAX16904 can operate in dropout by running at 97% duty cycle, making it ideal for automotive and industrial applications.

The MAX16904 operates at a 2.1MHz frequency, allowing for small external components and reduced output ripple. It guarantees no AM band interference. SYNC input programmability enables three frequency modes for optimized performance: forced fixed-frequency operation, SKIP mode (ultra-low quiescent current of 25µA), and synchronization to an external clock. The MAX16904 can be ordered with spread-spectrum frequency modulation, designed to minimize EMI-radiated emissions due to the modulation frequency.

The MAX16904 is available in a thermally enhanced, 3mm x 3mm, 10-pin TDFN package or a 16-pin TSSOP package. The MAX16904 operates over the -40°C to +125°C automotive temperature range.

Applications

- Automotive
- Industrial
- Military
- High-Voltage Input-Power DC-DC Applications

***Selector Guide* appears at end of data sheet.**

Features

- Wide +3.5V to +28V Input Voltage Range
- Tolerates Input Voltage Transients to +42V
- 600mA Minimum Output Current with Overcurrent Protection
- Fixed Output Voltages (See the Selector Guide and Contact Factory for All Available Trimmed Output Voltage Options)
- 2.1MHz Switching Frequency with Three Modes of Operation
  - 25µA Ultra-Low Quiescent Current SKIP Mode
  - Forced Fixed-Frequency Operation
  - External Frequency Synchronization
- Optional Spread-Spectrum Frequency Modulation
- Power-Good Output
- Enable-Pin Compatible from +3.3V Logic Level to +42V
- Thermal Shutdown Protection
- -40°C to +125°C Automotive Temperature Range
- 10-Pin TDFN-EP or 16-Pin TSSOP-EP Packages
- AEC-Q100 Qualified

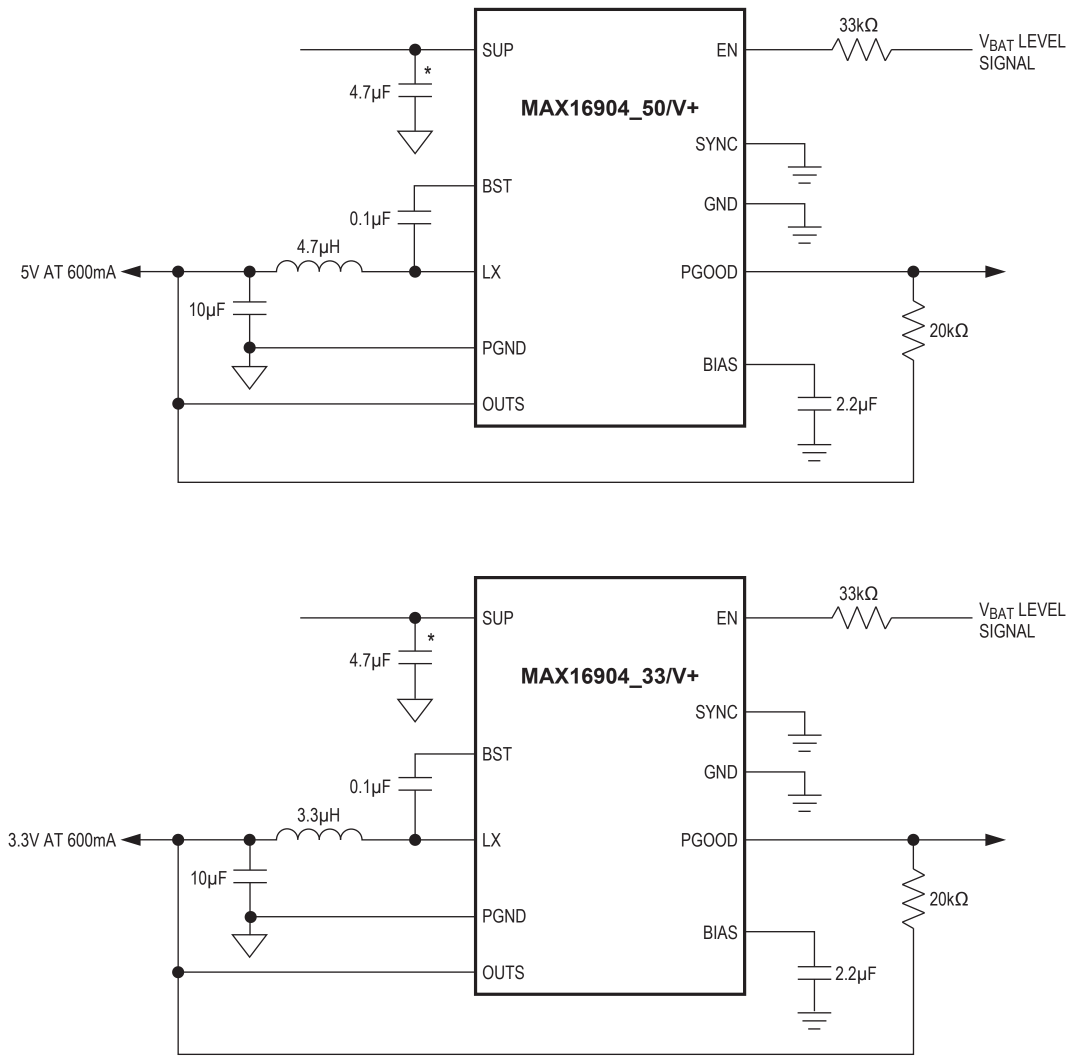
Ordering Information

PART	SPREAD SPECTRUM	TEMP RANGE	PIN-PACKAGE
MAX16904RATB__/V+	Disabled	-40°C to +125°C	10 TDFN-EP*
MAX16904RAUE__/V+	Disabled	-40°C to +125°C	16 TSSOP-EP*
MAX16904SATB__/V+	Enabled	-40°C to +125°C	10 TDFN-EP*
MAX16904SAUE__/V+	Enabled	-40°C to +125°C	16 TSSOP-EP*

Note: *Insert the desired suffix letters (from Selector Guide) into the blanks to indicate the output voltage.*
Alternative output voltages available upon request.

+Denotes a lead(Pb)-free/RoHS-compliant package.
/V Denotes an automotive qualified part.
**EP = Exposed pad.*

Typical Operating Circuits



*PLACE INPUT SUPPLY CAPACITORS AS CLOSE AS POSSIBLE TO THE SUP PIN. SEE THE *APPLICATIONS INFORMATION* SECTION FOR MORE DETAILS.

Absolute Maximum Ratings

(Voltages referenced to GND.)
SUP, EN...-0.3V to +42V
BST to LX (Note 1)...-0.3V to +6V
LX (Note 1)..-0.3V to (V_{SUP} + 0.3V)
BST...-0.3V to +47V
OUTS...-0.3V to +12V
SYNC, PGOOD, BIAS...-0.3V to +6.0V
PGND to GND ....-0.3V to +0.3V
LX Continuous RMS Current..1.0A
OUTS Short-Circuit Duration ....Continuous

ESD Protection
Human Body Model ....±2kV
Machine Model ....±200V
Continuous Power Dissipation (T_A = +70°C)
TDFN (derate 24.4 mW/°C above +70°C)..................1951mW
TSSOP (derate 26.1 mW/°C above+70°C)................2089mW
Operating Temperature Range...........................-40°C to +125°C
Junction Temperature..+150°C
Storage Temperature Range..............................-65°C to +150°C
Lead Temperature (soldering, 10s)..................................+300°C
Soldering Temperature (reflow).......................................+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Self protected against transient voltages exceeding these limits for ≤ 50ns under normal operation and loads up to the maximum rated output current.

Package Information

PACKAGE TYPE: 10 TDFN	
Package Code	T1033+1
Outline Number	**21-0137**
Land Pattern Number	**90-0003**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	41°C/W
Junction to Case (θ_{JC})	9°C/W
PACKAGE TYPE: 16 TSSOP	
Package Code	U16E+3
Outline Number	**21-0108**
Land Pattern Number	**90-0120**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	38.3°C/W
Junction to Case (θ_{JC})	3°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{SUP} = +14V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{SUP}	(Note 2)	3.5		28	V
		t < 1s			42	
Supply Current	I_{SUP}	EN = low		4	8	µA
		EN = high, no load, 3V < V_{OUT} < 5.5V		25	35	
		EN = high, continuous, no switching		1		mA
UV Lockout	V_{UVLO}	Bias rising	2.8	3	3.2	V
	$V_{UVLO,HYS}$	Hysteresis		0.4		
Bias Voltage	V_{BIAS}	+5.5V ≤ V_{SUP} ≤ +42V		5		V
Bias Current Limit	I_{BIAS}		10			mA
BUCK CONVERTER						
Voltage Accuracy	V_{OUT}	V_{OUT} = 5V, fixed frequency; 6V ≤ V_{SUP} ≤ 18V, I_{LOAD} = 0 to 600mA, T_A = -40°C to +125°C	-2.0%		+2.5%	V
		V_{OUT} = 5V, SKIP mode (Note 3)	-2.0%		+4.0%	
	$V_{OUT,3.3V}$	V_{OUT} = 3.3V, fixed frequency	-2.0%	3.3	+2.5%	
		V_{OUT} = 3.3V, SKIP mode (Note 3)	-2.0%	3.3	+4.0%	
	$V_{OUT,5V}$	V_{OUT} = 5V, fixed frequency	-2.0%	5	+2.5%	
		V_{OUT} = 5V, SKIP mode (Note 3)	-2.0%	5	+4.0%	
	$V_{OUT,5.1V}$	V_{OUT} = 5.1V, fixed frequency	-2.0%	5.1	+2.5%	
		V_{OUT} = 5.1V, SKIP mode (Note 3)	-2.0%	5.1	+4.0%	
	$V_{OUT,5.5V}$	V_{OUT} = 5.5V, fixed frequency	-2.0%	5.5	+2.5%	
		V_{OUT} = 5.5V, SKIP mode (Note 3)	-2.0%	5.5	+4.0%	
	$V_{OUT,6.0V}$	V_{OUT} = 6.0V, fixed frequency	-2.0%	6.0	+2.5%	
		V_{OUT} = 6.0V, SKIP mode (Note 3)	-2.0%	6.0	+4.0%	
	$V_{OUT,8.0V}$	V_{OUT} = 8.0V, fixed frequency	-2.0%	8.0	+2.5%	
		V_{OUT} = 8.0V, SKIP mode (Note 3)	-2.0%	8.0	+4.0%	
SKIP-Mode Peak Current	I_{SKIP}			350		mA
High-Side DMOS $R_{DS(ON)}$	$R_{ON,HS}$	V_{BIAS} = 5V		400	800	mΩ
Low-Side DMOS $R_{DS(ON)}$	$R_{ON,LS}$			250	450	mΩ
DMOS Peak Current-Limit Threshold	I_{MAX}		0.85	1.05	1.22	A
Soft-Start Ramp Time	t_{SS}		7	8	9	ms
LX Rise Time	$t_{RISE,LX}$			5		ns
Minimum On-Time	t_{ON}			80		ns
PWM Switching Frequency	f_{SW}	Internally generated	1.925	2.1	2.275	MHz
SYNC Input Frequency Range	f_{SYNC}		1.8		2.6	MHz
Spread-Spectrum Range	SS	Spread-spectrum option only		+6		%

Electrical Characteristics (continued)

(V_{SUP} = +14V, $T_A = T_J$ = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.)

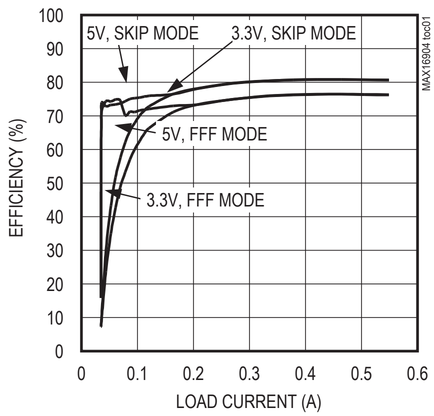
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PGOOD						
PGOOD Threshold	$V_{THR,PGD}$	V_{OUT} rising	88	93	98	%
	$V_{THF,PGD}$	V_{OUT} falling	88	91	94	
PGOOD Debounce	t_{DEB}			10		µs
PGOOD High Leakage Current	$I_{LEAK,PGD}$	T_A = +25°C, $V_{PGD} \le V_{OUT}$			1	µA
PGOOD Output Low Level	$V_{OUT,PGD}$	Sinking 1mA			0.4	V
LOGIC LEVELS						
EN Level	$V_{IH,EN}$		2.4			V
	$V_{IL,EN}$				0.6	
EN Input Current	$I_{IN,EN}$	$V_{EN} = V_{SUP}$ = +42V, T_A = +25°C			1	µA
SYNC Switching Threshold	$V_{IH,SYNC}$		1.4			V
	$V_{IL,SYNC}$				0.4	
SYNC Internal Pulldown	$R_{PD,SYNC}$			200		kΩ
THERMAL PROTECTION						
Thermal Shutdown	T_{SHDN}			175		°C
Thermal Shutdown Hysteresis	$T_{SHDN,HYS}$			15		°C

Note 2: When the typical minimum on-time of 80ns is violated, the device skips pulses.
Note 3: Guaranteed by design; not production tested.

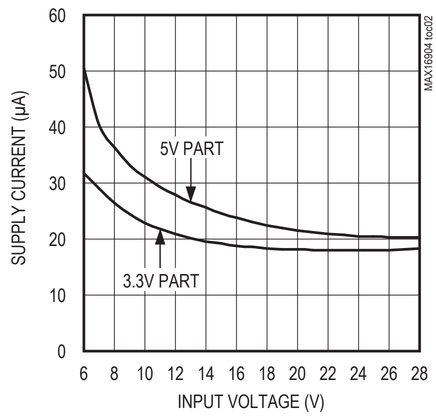
Typical Operating Characteristics

(V_{SUP} = +14V, T_A = +25°C, unless otherwise noted.)

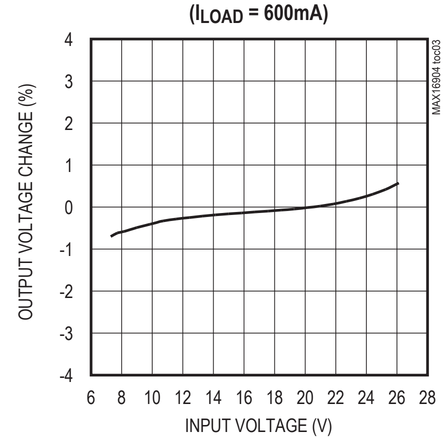
EFFICIENCY vs. LOAD CURRENT



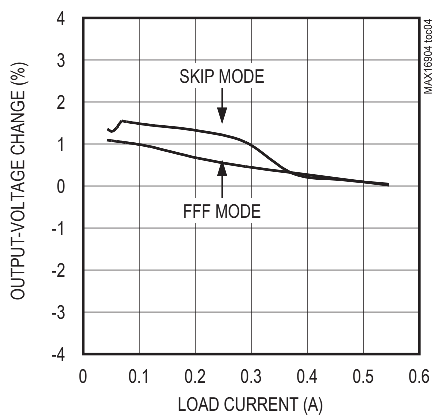
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (SKIP MODE)



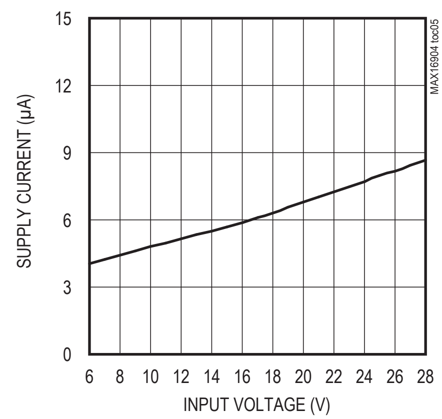
LINE REGULATION (I_{LOAD} = 600mA)



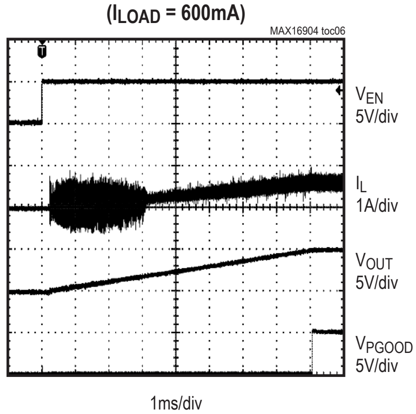
LOAD REGULATION



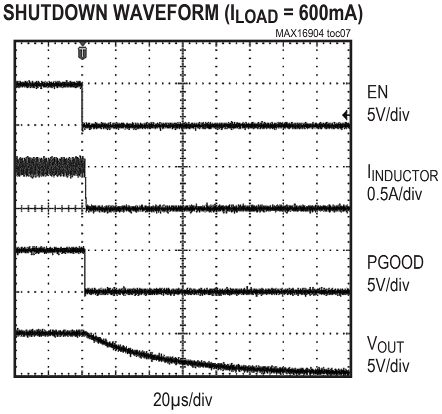
SHUTDOWN SUPPLY CURRENT vs. INPUT VOLTAGE



STARTUP RESPONSE (I_{LOAD} = 600mA)



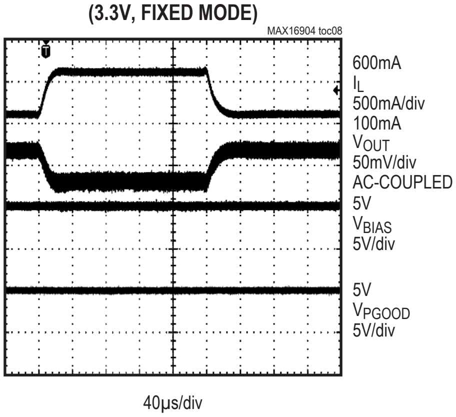
SHUTDOWN WAVEFORM (I_{LOAD} = 600mA)



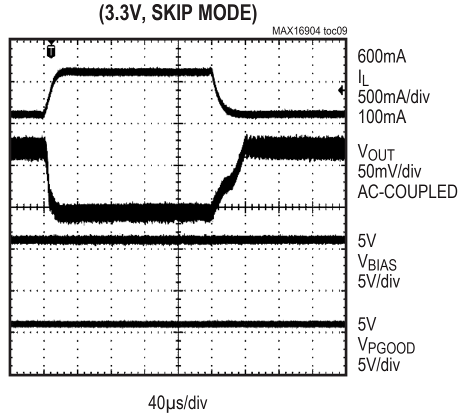
Typical Operating Characteristics (continued)

(V_{SUP} = +14V, T_A = +25°C, unless otherwise noted.)

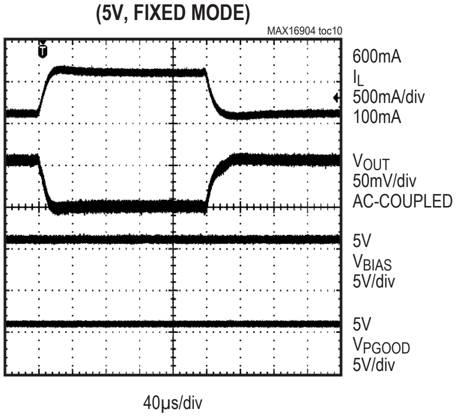
LOAD TRANSIENT RESPONSE
(3.3V, FIXED MODE)



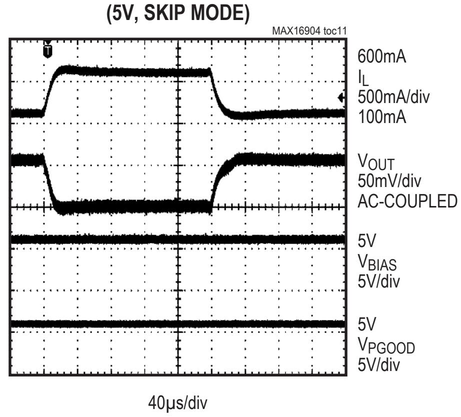
LOAD TRANSIENT RESPONSE
(3.3V, SKIP MODE)



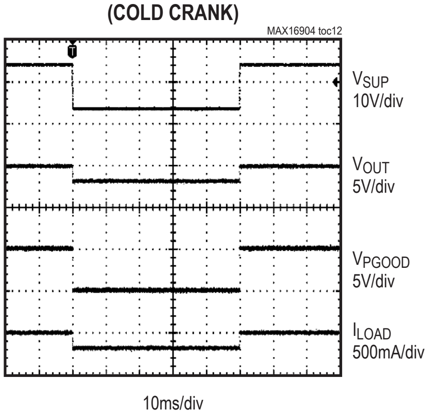
LOAD TRANSIENT RESPONSE
(5V, FIXED MODE)



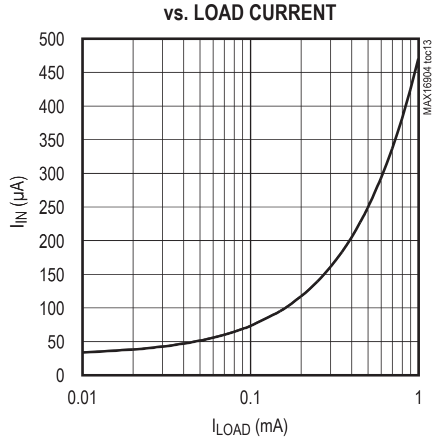
LOAD TRANSIENT RESPONSE
(5V, SKIP MODE)



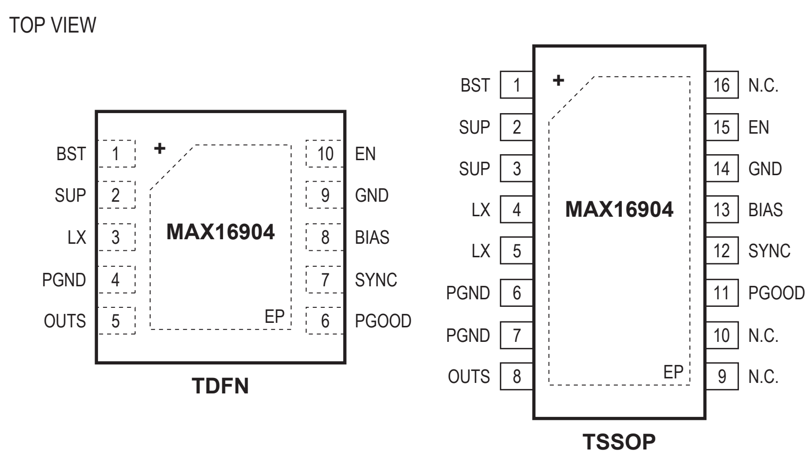
UNDERVOLTAGE PULSE
(COLD CRANK)



STANDBY CURRENT
vs. LOAD CURRENT



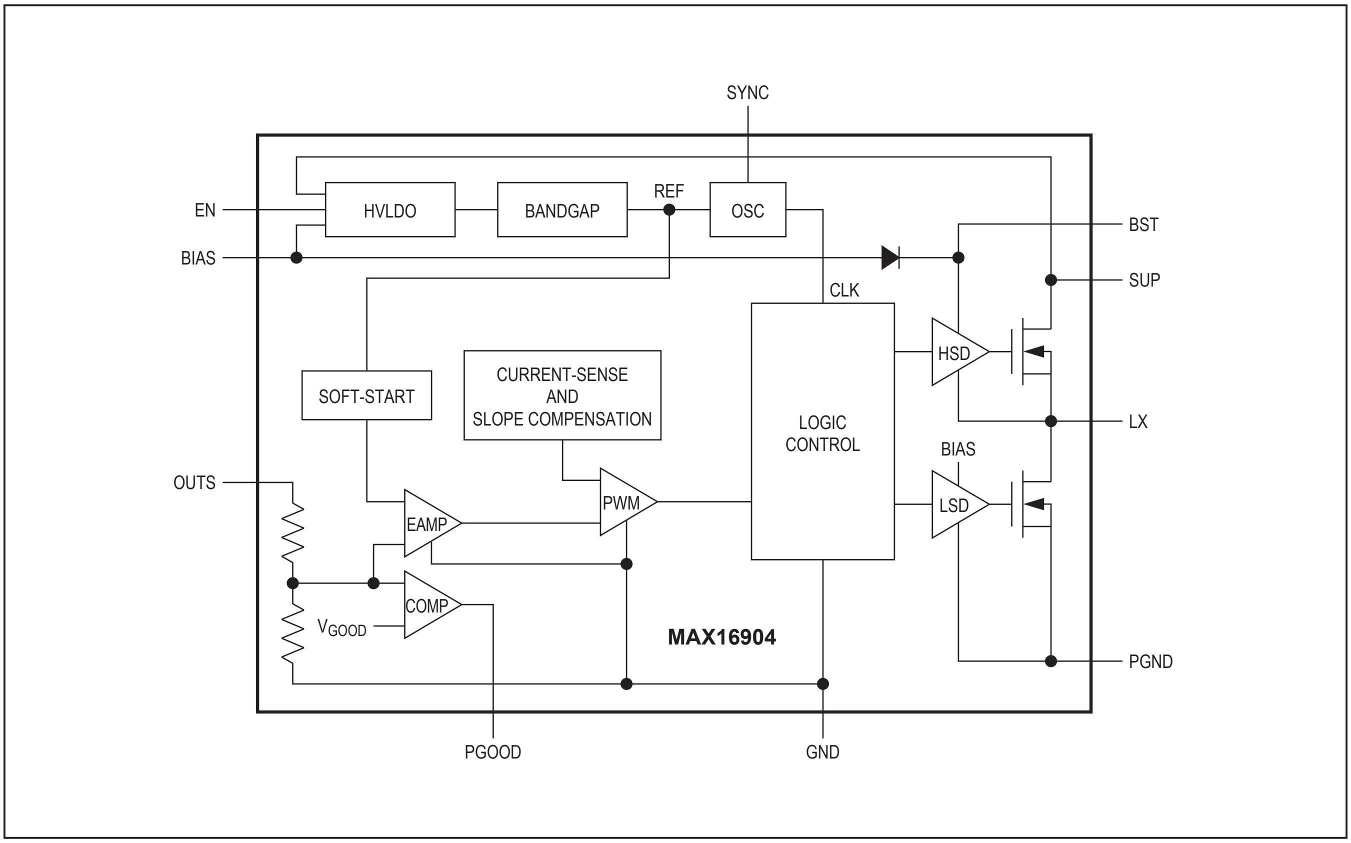
Pin Configurations



Pin Description

PIN		NAME	FUNCTION
TDFN-EP	TSSOP-EP		
1	1	BST	Bootstrap Capacitor for High-Side Driver (0.1µF)
2	2, 3	SUP	Voltage Supply Input. Connect a 4.7µF ceramic capacitor from SUP to PGND. Place the capacitor very close to the SUP pin. For the TSSOP-EP package, connect both SUP pins together for proper operation.
3	4, 5	LX	Buck Switching Node. LX is high impedance when the device is off. For the TSSOP package, connect both LX pins together for proper operation.
4	6, 7	PGND	Power Ground. For the TSSOP-EP package, connect both PGND pins together for proper operation.
5	8	OUTS	Buck Regulator Voltage-Sense Input. Bypass OUTS to PGND with a 10µF or larger X7R ceramic capacitor.
6	11	PGOOD	Open-Drain Power-Good Output.
7	12	SYNC	Sync Input. SYNC allows the device to synchronize to other supplies. When connected to GND or unconnected, SKIP mode is enabled under light loads. When connected to a clock source or BIAS, forced PWM mode is enabled.
8	13	BIAS	+5V Internal Logic Supply. Connect a 2.2µF ceramic capacitor from BIAS to GND.
9	14	GND	Analog Ground
10	15	EN	Enable Input. EN is high-voltage compatible. Drive EN HIGH for normal operation.
—	9, 10, 16	N.C.	No Connection. Not internally connected.
—	—	EP	Exposed Pad. Connect EP to PGND. Do not use EP as the only ground connection.

Functional Diagram



Detailed Description

The MAX16904 is a small, current-mode buck converter that features synchronous rectification and requires no external compensation network. The device is designed for 600mA output current, and can stay in dropout by running at 97% duty cycle. It provides an accurate output voltage within the +6.5V to +18V input range. Voltage quality can be monitored by observing the PGOOD signal. The device operates at 2.1MHz (typ) frequency, which allows for small external components, reduced output ripple, and guarantees no AM band interference.

The device features an ultra-low 25µA (typ) quiescent supply current in standby mode. Standby mode is entered when load currents are below 5mA and when SYNC is low. The device operates from a +3.5V to +28V supply voltage and tolerates transients up to +42V, making it ideal for automotive applications. The device is available in factory-trimmed output voltages from 1.8V to 10.7V in 100mV steps. Contact the factory for availability of voltage options.

Enable (EN)

The device is activated by driving EN high. EN is compatible from a +3.3V logic level to automotive battery levels. EN can be controlled by microcontrollers and automotive KEY or CAN inhibit signals. The EN input has no internal pullup/pulldown current to minimize overall quiescent supply current. To realize a programmable undervoltage lockout level, use a resistor-divider from SUP to EN to GND.

BIAS/UVLO

The device features undervoltage lockout. When the device is enabled, an internal bias generator turns on. LX begins switching after V_{BIAS} has exceeded the internal undervoltage lockout level V_{UVLO} = 3V (typ).

Soft-Start

The device features an internal soft-start timer. The output voltage soft-start ramp time is 8ms (typ). If a short circuit or undervoltage is encountered, after the soft-start timer has expired, the device is disabled for 30ms (typ) and it reattempts soft-start again. This pattern repeats until the short circuit has been removed.

Oscillator/Synchronization and Efficiency (SYNC)

The device has an on-chip oscillator that provides a switching frequency of 2.1MHz (typ). Depending on the condition of SYNC, two operation modes exist. If SYNC is unconnected or at GND, the device must operate in highly efficient pulse-skipping mode if the load current is below the SKIP mode current threshold. If SYNC is at BIAS or has a frequency applied to it, the device is in forced PWM mode. The device offers the best of both worlds. The device can be switched during operation between forced PWM mode and SKIP mode by switching SYNC.

SKIP Mode Operation

SKIP mode is entered when the SYNC pin is connected to ground or is unconnected and the peak load current is < 350mA (typ). In this mode, the high-side FET is turned on until the current in the inductor is ramped up to 350mA (typ) peak value and the internal feedback voltage is above the regulation voltage (1.2V typ). At this point, both the high-side and low-side FETs are turned off. Depending on the choice of the output capacitor and the load current the high-side FET turns on when OUTS (valley) drops below the 1.2V (typ) feedback voltage.

Achieving High Efficiency at Light Loads

The device operates with very low quiescent current at light loads to enhance efficiency and conserve battery life. When the device enters SKIP mode the output current is monitored to adjust the quiescent current.

When the output current is < 5mA, the device operates in the lowest quiescent current mode also called the standby mode. In this mode, the majority of the internal circuitry (excluding that necessary to maintain regulation) in the device, including the internal high-voltage LDO, is turned off to save current. Under no load and with SKIP mode enabled, the device draws only 25µA (typ) current. For load currents > 5mA, the device enters normal SKIP mode while still maintaining very high efficiency.

Controlled EMI with Forced-Fixed Frequency

In forced PWM mode, the device attempts to operate at a constant switching frequency for all load currents. For tightest frequency control, apply the operating frequency to SYNC. The advantage of this mode is a constant switching frequency, which improves EMI performance; the disadvantage is that considerable current can be thrown away. If the load current during a switching cycle is less than the current flowing through the inductor, the excess current is diverted to GND. With no external load present, the operating current is in the 10mA range.

Extended Input Voltage Range

In some cases, the device is forced to deviate from its operating frequency independent of the state of SYNC. For input voltages above 18V, the required duty cycle to regulate its output may be smaller than the minimum on-time (80ns, typ). In this event, the device is forced to lower its switching frequency by skipping pulses.

If the input voltage is reduced and the device approaches dropout, it tries to turn on the high-side FET continuously. To maintain gate charge on the high-side FET, the BST capacitor must be periodically recharged. To ensure proper charge on the BST capacitor when in dropout, the high-side FET is turned off every 6.5µs and the low-side FET is turned on for about 150ns. This gives an effective duty cycle of > 97% and a switching frequency of 150kHz when in dropout.

Spread-Spectrum Option

The device has an optional spread-spectrum version. If this option is selected, then the internal operating frequency varies by +6% relative to the internally generated operating frequency of 2.1MHz (typ). Spread spectrum is offered to improve EMI performance of the device. By varying the frequency 6% only in the positive direction, the device still guarantees that the 2.1MHz frequency does not drop into the AM band limit of 1.8MHz. Additionally, with the low minimum on-time of 80ns (typ) no pulse skipping is observed for a 5V output with 18V input maximum battery voltage in steady state.

The internal spread spectrum does not interfere with the external clock applied on the SYNC pin. It is active only when the device is running with internally generated switching frequency.

Power-Good (PGOOD)

The device features an open-drain power-good output. PGOOD is an active-high output that pulls low when the output voltage is below 91% of its nominal value. PGOOD is high impedance when the output voltage is above 93% of its nominal value. Connect a 20kΩ (typ) pullup resistor to an external supply or the on-chip BIAS output.

Overcurrent Protection

The device limits the peak output current to 1.05A (typ). To protect against short-circuit events, the device shuts off when OUTS is below 1.5V (typ) and one overcurrent event is detected. The device attempts a soft-start restart every 30ms and stays off if the short circuit has not been removed. When the current limit is no longer present, it reaches the output voltage by following the normal soft-start sequence. If the device die reaches the thermal limit of +175°C (typ) during the current-limit event, it immediately shuts off.

Thermal-Overload Protection

The device features thermal-overload protection. The device turns off when the junction temperature exceeds +175°C (typ). Once the device cools by 15°C (typ), it turns back on with a soft-start sequence.

Applications Information

Inductor Selection

The nominal inductor value can be calculated using Table based on the nominal output voltage of the device. Select the nearest standard inductance value to the calculated nominal value. The nominal standard value selected should be within ±25% of L_{NOM} for best performance.

Table 1. Inductor Selection

V_{OUT} (V)	L_{NOM} (µH)
1.8 to 3.1	V_{OUT}/0.55
3.2 to 6.5	V_{OUT}/0.96
6.6 to 8.1	V_{OUT}/1.40
8.2 to 10	V_{OUT}/1.75

Table 2. Examples for Standard Output Voltages

V_{OUT} (V)	CALCULATED L_{NOM} (µH)	STANDARD VALUE (µH)
1.8	3.3	3.3
3.3	3.4	3.3
5.0	5.2	4.7
8.0	5.7	5.6

Input Capacitor

A low-ESR ceramic input capacitor of 1µF or larger is needed for proper device operation. This value may need to be larger based on application input ripple requirements.

The discontinuous input current of the buck converter causes large input ripple current. The switching frequency, peak inductor current, and the allowable peak-to-peak input-voltage ripple dictate the input capacitance requirement. Increasing the switching frequency or the inductor value lowers the peak-to-average current ratio yielding a lower input capacitance requirement.

The input ripple comprises mainly of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the input capacitor). The total voltage ripple is the sum of ΔV_Q and ΔV_{ESR}. Assume the input-voltage ripple from the ESR and the capacitor discharge is equal to 50% each. The following equations show the ESR and capacitor requirement for a target voltage ripple at the input:

$$ESR = \frac{\Delta V_{ESR}}{\left(I_{OUT} + \frac{\Delta I_{P-P}}{2}\right)}$$

$$C_{IN} = \frac{I_{OUT} \times D(1-D)}{\Delta V_Q \times f_{SW}}$$

where:

$$\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

and:

$$D = \frac{V_{OUT}}{V_{IN}}$$

where I_{OUT} is the output current, D is the duty cycle, and f_{SW} is the switching frequency. Use additional input capacitance at lower input voltages to avoid possible undershoot below the UVLO threshold during transient loading.

Output Capacitor

To maintain acceptable phase margin, a minimum ceramic output capacitor value of 10µF is needed with a voltage rating of 2 times the V_{OUT} voltage. Additional output capacitance may be needed based on application-specific output voltage ripple requirements.

The allowable output-voltage ripple and the maximum deviation of the output voltage during step load currents determine the output capacitance and its ESR. The output ripple comprises of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the output capacitor). Use low-ESR ceramic or aluminum electrolytic capacitors at the output. For aluminum electrolytic capacitors, the entire output ripple is contributed by ΔV_{ESR}. Use the ESR_{OUT} equation to calculate the ESR requirement and choose the capacitor accordingly. If using ceramic capacitors, assume the contribution to the output ripple voltage from the ESR and the capacitor discharge to be equal. The following equations show the output capacitance and ESR requirement for a specified output-voltage ripple.

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_{P-P}}$$

$$C_{OUT} = \frac{\Delta I_{P-P}}{8 \times \Delta V_Q \times f_{SW}}$$

where:

$$\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

$$V_{OUT\_RIPPLE} \cong \Delta V_{ESR} + \Delta V_Q$$

ΔI_{P-P} is the peak-to-peak inductor current as calculated above and f_{SW} is the converter's switching frequency. The allowable deviation of the output voltage during fast transient loads also determines the output capacitance and its ESR. The output capacitor supplies the step load current until the converter responds with a greater duty cycle. The response time ($t_{RESPONSE}$) depends on the closed-loop bandwidth of the converter. The device's high switching frequency allows for a higher closed-loop bandwidth, thus reducing $t_{RESPONSE}$ and the output capacitance requirement. The resistive drop across the output capacitor's ESR and the capacitor discharge causes a voltage droop during a step load. Use a combination of low-ESR tantalum and ceramic capacitors for better transient load and ripple/noise performance. Keep the maximum output-voltage deviations below the tolerable limits of the electronics being powered. When using a ceramic capacitor, assume an 80% and 20% contribution from the output capacitance discharge and the ESR drop, respectively. Use the following equations to calculate the required ESR and capacitance value:

$$ESR_{OUT} = \frac{\Delta V_{ESR}}{I_{STEP}}$$

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_Q}$$

where I_{STEP} is the load step and $t_{RESPONSE}$ is the response time of the converter. The converter response time depends on the control-loop bandwidth.

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching power losses and clean stable operation. Use a multilayer board wherever possible for better noise immunity. Refer to the MAX16904 Evaluation Kit for recommended PCB layout. Follow these guidelines for a good PCB layout:

1) The input capacitor (4.7µF, see the applications schematic in the *Typical Operating Circuits*) should be placed right next to the SUP pins (pins 2 and 3 on the TSSOP-EP package). Because the device operates at 2.1MHz switching frequency, this placement is critical for effective decoupling of high-frequency noise from the SUP pins.

2) Solder the exposed pad to a large copper plane area under the device. To effectively use this copper area as heat exchanger between the PCB and ambient, expose the copper area on the top and bottom side. Add a few small vias or one large via on the copper pad for efficient heat transfer. Connect the exposed pad to PGND ideally at the return terminal of the output capacitor.
3) Isolate the power components and high current paths from sensitive analog circuitry.
4) Keep the high current paths short, especially at the ground terminals. The practice is essential for stable jitter-free operation.
5) Connect the PGND and GND together preferably at the return terminal of the output capacitor. Do not connect them anywhere else.
6) Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PCB to enhance full load efficiency and power dissipation capability.
7) Route high-speed switching nodes away from sensitive analog areas. Use internal PCB layers as PGND to act as EMI shields to keep radiated noise away from the device and analog bypass capacitor.

ESD Protection

The device's ESD tolerance is rated for Human Body Model and Machine Model. The Human Body Model discharge components are C_S = 100pF and R_D = 1.5kΩ (Figure 1). The Machine Model discharge components are C_S = 200pF and R_D = 0Ω (Figure 2).

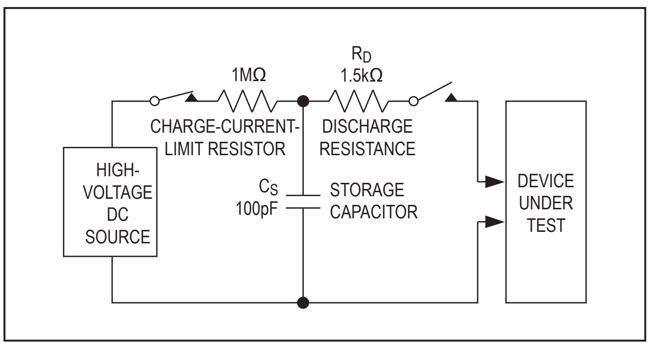


Figure 1. Human Body ESD Test Circuit

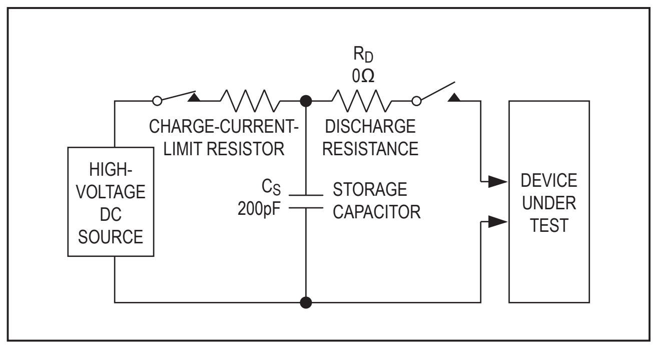


Figure 2. Machine Model ESD Test Circuit

Selector Guide

PART	OUTPUT VOLTAGE (V)	PIN-PACKAGE	SPREAD-SPECTRUM SWITCHING FREQUENCY	TOP MARK
MAX16904RATB50/V+	5.0	10 TDFN-EP* (3mm x 3mm x 0.75mm)	—	AVY
MAX16904RAUE50/V+	5.0	16 TSSOP-EP* (5mm x 4.4mm)	—	—
MAX16904SATB50/V+	5.0	10 TDFN-EP* (3mm x 3mm x 0.75mm)	Yes	AWA
MAX16904SATB51/V+	5.1	10 TDFN-EP* (3mm x 3mm x 0.75mm)	Yes	AYX
MAX16904SATB52/V+	5.2	10 TDFN-EP* (3mm x 3mm x 0.75mm)	Yes	AYY
MAX16904SAUE50/V+	5.0	16 TSSOP-EP* (5mm x 4.4mm)	Yes	—
MAX16904RATB28/V+	2.8	10 TDFN-EP* (3mm x 3mm x 0.75mm)	—	BPP
MAX16904RATB33/V+	3.3	10 TDFN-EP* (3mm x 3mm x 0.75mm)	—	AVX
MAX16904RAUE33/V+	3.3	16 TSSOP-EP* (5mm x 4.4mm)	—	—
MAX16904SATB33/V+	3.3	10 TDFN-EP* (3mm x 3mm x 0.75mm)	Yes	AVZ
MAX16904SAUE33/V+	3.3	16 TSSOP-EP* (5mm x 4.4mm)	Yes	—
MAX16904RAUE18/V+**	1.8	16 TSSOP-EP* (5mm x 4.4mm)	—	—
MAX16904SATB60/V+	6.0	10 TDFN-EP* (3mm x 3mm x 0.75mm)	Yes	AYO
MAX16904SATB80/V+	8.0	10 TDFN-EP* (3mm x 3mm x 0.75mm)	Yes	AYN
MAX16904RATB33+	3.3	10 TDFN-EP* (3mm x 3mm x 0.75mm)	—	AZR
MAX16904RATB50+	5.0	10 TDFN-EP* (3mm x 3mm x 0.75mm)	—	AYG
MAX16904RATB55/V+**	5.5	10 TDFN-EP* (3mm x 3mm x 0.75mm)	—	AYL
MAX16904RAUE33+	3.3	16 TSSOP-EP* (5mm x 4.4mm)	—	—
MAX16904RAUE50+	5.0	16 TSSOP-EP* (5mm x 4.4mm)	—	—
MAX16904SATB33+	3.3	10 TDFN-EP* (3mm x 3mm x 0.75mm)	Yes	AZS
MAX16904SATB41/V+**	4.1	10 TDFN-EP* (3mm x 3mm x 0.75mm)	Yes	BAC
MAX16904SATB50+	5.0	10 TDFN-EP* (3mm x 3mm x 0.75mm)	Yes	AZT
MAX16904SATB55/V+	5.5	10 TDFN-EP* (3mm x 3mm x 0.75mm)	Yes	BAG
MAX16904SAUE33+	3.3	16 TSSOP-EP* (5mm x 4.4mm)	Yes	—
MAX16904SAUE50+	5.0	16 TSSOP-EP* (5mm x 4.4mm)	Yes	—

Note: *All devices operate over the -40°C to +125°C automotive temperature range.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
/V denotes an automotive qualified part.
**EP = Exposed pad.*
***Future product—contact factory for availability.*

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/10	Initial release	—
1	11/10	Added new output voltage trim to *Selector Guide*	12
2	3/11	Updated the Voltage Accuracy and the DMOS Peak Current-Limit Threshold parameters in the *Electrical Characteristics*, updated TOCs 1, 6, and 8–13	3, 4, 5, 6
3	7/11	Added the MAX16904RATB50+ part number to the *Selector Guide*	13
4	3/12	Added new future part numbers to the *Selector Guide*	13
5	6/12	Updated *Selector Guide* to include MAX16904SATB51/V+ and the MAX16904SATB52/V+	13
6	4/13	Updated *Pin Description*, *Inductor Selection*, *Input Capacitor*, *Output Capacitor*, and *Selector Guide* sections	1, 7, 10, 11, 13
7	8/13	Added limits for 5.1V, 6V, and 8V options in *Electrical Characteristics* and update *Selector Guide*	3, 13, 14
8	12/13	Added condition for Supply Current and Voltage Accuracy in *Electrical Characteristics* and removed future product indicator from MAX16904SATB52/V+	2, 13
9	9/14	Updated *Typical Operating Circuit* and PGOOD high leakage current conditions in *Electrical Characteristics*	2, 4
10	3/15	Added new Note 1 in *Absolute Maximum Ratings* section and renumbered remaining notes in *Package Thermal Characteristics* and *Electrical Characteristics* sections	3, 4
11	9/15	Added V_{OUT} 5.5V parts to *Electrical Characteristics* and *Selector Guide* tables; updated PGOOD Threshold min/max values in *Electrical Characteristics* table	3, 4, 13, 14
12	11/15	Removed future product status to MAX16904SATB55/V+ in *Selector Guide*	15
13	4/16	Added MAX16904RATB28/V+ in *Selector Guide*	14
14	8/18	Updated the *Package Information* table	3
15	12/18	Updated Output Voltage value for MAX16904RATB28/V+ in the *Selector Guide*	14