MAX16914/MAX16915

Ideal Diode, Reverse-Battery, and Overvoltage Protection Switch/Limiter Controllers with External MOSFETs

General Description

The MAX16914/MAX16915 low-quiescent-current overvoltage and reverse-battery protection controllers are designed for automotive and industrial systems that must tolerate high-voltage transient and fault conditions. These conditions include load dumps, voltage dips, and reversed input voltages. The controllers monitor the input voltage on the supply line and control two external pFETs to isolate the load from the fault condition. The external pFETs are turned on when the input supply exceeds 4.5V and stay on up to the programmed overvoltage threshold. During high-voltage fault conditions, the controllers regulate the output voltage to the set upper threshold voltage (MAX16915), or switch to high resistance (MAX16914) for the duration of the overvoltage transient to prevent damage to the downstream circuitry. The overvoltage event is indicated through an active-low, open-drain output, $\overline{OV}$.

The reverse-battery pFET behaves as an ideal diode, minimizing the voltage drop when forward biased. Under reverse bias conditions, the pFET is turned off, preventing a downstream tank capacitor from being discharged into the source.

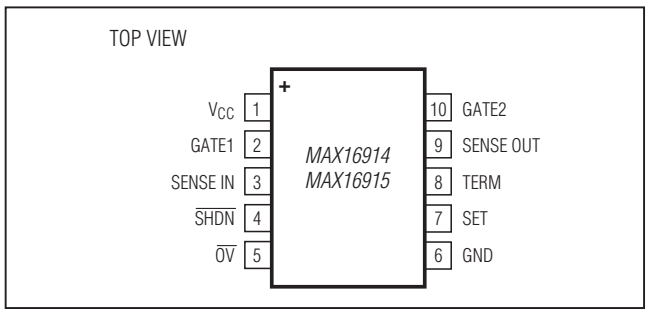
Shutdown control turns off the IC completely, disconnecting the input from the output and disconnecting TERM from its external resistor-divider to reduce the quiescent current to a minimum.

Both devices are available in a 10-pin µMAX® package and operate over the automotive -40°C to +125°C temperature range.

Applications

Industrial

Pin Configuration



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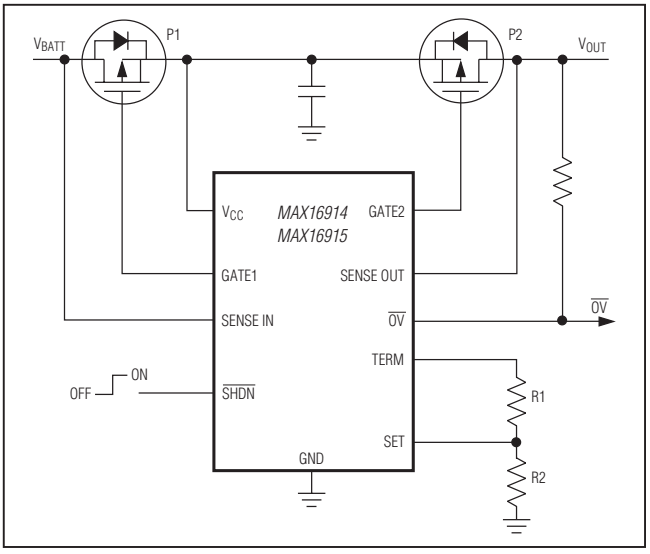
Benefits and Features

- Architecture Replaces Protection Diodes Reducing the Forward Voltage, Allowing Operation During Cold-Crank Conditions
  - Transient Voltage Protection Up to +44V and -75V
  - Low-Voltage Drop when Used with Properly Sized External pFETs
  - 4.5V to 19V Input-Voltage Operation
- Ideal Diode Reverse-Battery Protection Supports Down to -75V to Protect System During Negative-Voltage Transients
  - Back-Charge Prevention Avoids Discharging Downstream Tank Capacitance
- Overvoltage Protection Enables System to Survive Up to a +44V Load Dump
  - Overvoltage Indicator
  - Thermal-Overload Protection
- Low Operating Current Meets Stringent Module Specifications While Maintaining System Protection
  - 29µA Low Operating Current
  - 6µA Low Shutdown Current

Ordering Information appears at end of data sheet.

Typical Operating Circuit



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Absolute Maximum Ratings

V_{CC}, SENSE OUT, TERM, $\overline{SHDN}$, $\overline{OV}$ to GND for ≤ 400ms ..... -0.3V to +44V
V_{CC}, SENSE OUT, TERM, $\overline{SHDN}$, $\overline{OV}$ to GND for ≤ 90s ..... -0.3V to +28V
V_{CC}, SENSE OUT, TERM, $\overline{SHDN}$, $\overline{OV}$ to GND ..... -0.3V to +20V
SENSE IN to GND for ≤ 2ms ..... -75V to +44V
SENSE IN to GND for ≤ 90s ..... -18V to +44V
SENSE IN to GND ..... -0.3V to +20V
GATE1, GATE2 to V_{CC} ..... -16V to +0.3V
GATE1, GATE2 to GND ..... -0.3V to (V_{CC} + 0.3V)
SET to GND ..... -0.3V to +8V
Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 8.8mW/°C above T_A = +70°C) (Note 1) 707mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = 14V, C_{GATE1} = 32nF, C_{GATE2} = 32nF, $\overline{SHDN}$ = high, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	(Note 3)		4.5		19	V
Shutdown Supply Current ($I_{SENSE\ IN}$ + $I_{SENSE\ OUT}$ + $I_{\overline{OV}}$ + $I_{\overline{SHDN}}$ + I_{VCC})	$I_{\overline{SHDN}}$	$\overline{SHDN}$ = low, $V_{SENSE\ OUT}$ = 0V, V_{TERM} = 0V	T_A = +25°C		6.0	12	µA
			T_A = +85°C (Note 3)		6.1	12	
			T_A = +125°C (Note 3)		6.2	12	
Quiescent Supply Current ($I_{SENSE\ IN}$ + $I_{SENSE\ OUT}$ + $I_{\overline{OV}}$ + $I_{\overline{SHDN}}$ + I_{VCC})	I_Q	$\overline{SHDN}$ = high	T_A = +25°C		29	53	µA
			T_A = +85°C (Note 3)		30	55	
			T_A = +125°C (Note 3)		31	57	
V_{CC} Undervoltage Lockout	V_{UVLO}	V_{CC} rising, V_{SET} = 1V , $\overline{SHDN}$ = high			4.06	4.35	V
V_{CC} Undervoltage-Lockout Hysteresis					8		%
SET Threshold Voltage	V_{SETTH}	V_{SET} rising		-3%	+1.20	+3%	V
SET Threshold Voltage Hysteresis	V_{SETHY}				4		%
SET Input Current	I_{SET}	V_{SET} = 1V			0.02	0.2	µA
$\overline{SHDN}$ Low Threshold	V_{SHDNL}					0.4	V
$\overline{SHDN}$ High Threshold	V_{SHDNH}			1.4			V
$\overline{SHDN}$ Pulldown Current	I_{SHDN}	$V_{\overline{SHDN}}$ = 14V, internally pulled to GND			0.5	1.0	µA
V_{CC} to GATE Output Low Voltage	V_{GVCC1}	V_{CC} = 14V		6.25	7.5	8.5	V
V_{CC} to GATE Clamp Voltage	V_{GVCC2}	V_{CC} = 42V				14	V

Electrical Characteristics (continued)

(V_{CC} = 14V, C_{GATE1} = 32nF, C_{GATE2} = 32nF, $\overline{SHDN}$ = high, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TERM On-Resistance	R_{TERM}	$\overline{SHDN}$ = high		150	500	Ω
TERM Output Current	I_{TERM}	$\overline{SHDN}$ = low, V_{TERM} = 0V			1.0	µA
Back-Charge Voltage Fault Threshold	V_{BCTH}	$V_{SENSE\ OUT}$ = 14V (Note 4)	18	25	32	mV
Back-Charge Voltage Threshold Hysteresis	V_{BCHY}	$V_{SENSE\ OUT}$ = 14V		50		mV
Back-Charge Turn-Off Time (GATE1)	t_{BC}	V_{CC} = 9.5V, $V_{SENSE\ IN}$ = 9V, $V_{SENSE\ OUT}$ stepped from 4.9V to 9.5V (Note 5)		6	10	µs
Back-Charge Recovery Time (GATE1)	t_{BCREC}	V_{CC} = 9.5V, $V_{SENSE\ IN}$ = 9V, $V_{SENSE\ OUT}$ stepped from 9.5V to 4.9V (Note 6)		18	30	µs
GATE2 Turn-Off Time		V_{CC} = 9.5V, V_{SET} rising from 1V to 1.5V (Note 7)		3		µs
GATE2 Turn-On Time		V_{CC} = 9.5V, V_{SET} falling from 1.5V to 1V (Note 8)		20		µs
Startup Response Time ($V_{\overline{SHDN}}$ Rising)	t_{START1}	V_{CC} = 9.5V, from $V_{\overline{SHDN}}$ rising to $V_{GATE\_}$ falling (Note 9)		100		µs
Startup Response Time (V_{CC} Rising)	t_{START2}	V_{CC} rising from 2V to 4.5V, $\overline{SHDN}$ = high (Note 10)		0.150		ms
Reverse-Battery Voltage Turn-Off Time/UVLO Turn-Off Time	$t_{REVERSE}$	V_{CC} and $V_{SENSE\ IN}$ falling from 4.25V to 3.25V, $V_{SENSE\ OUT}$ = 4.25V (Note 11)			30	µs
Thermal-Shutdown Temperature				+170		°C
Thermal-Shutdown Hysteresis				20		°C
$\overline{OV}$ Output Low Voltage	V_{OVBL}	I_{SINK} = 600µA			0.4	V
$\overline{OV}$ Open-Drain Leakage Current	I_{OVB}	V_{SET} = 1.0V			1.0	µA
SENSE IN Input Current	$I_{SENSE\ IN}$	$V_{\overline{SHDN}}$ = 0/14V		1	5	µA
SENSE OUT Input Current	$I_{SENSE\ OUT}$	$V_{\overline{SHDN}}$ = 0/14V		2	5	µA
SET to $\overline{OV}$ Output Low Propagation Delay	t_{OVBPD}	V_{CC} = 9.5V, V_{SET} rising from 1V to 1.5V to $V_{\overline{OV}}$ falling		3		µs

Note 2: All parameters are production tested at T_A = +25NC. Limits over the operating temperature range are guaranteed by design and characterization.

Note 3: Guaranteed by design and characterization.

Note 4: The back-charge voltage, V_{BC}, is defined as the voltage at SENSE OUT minus the voltage at SENSE IN.

Note 5: Defined as the time from when V_{BC} exceeds V_{BCTH} (25mV typ) to when V_{GATE1} exceeds V_{CC} - 3.5V.

Note 6: Defined as the time from when V_{BC} falls below V_{BCTH} - 50mV to when V_{GATE1} falls below V_{CC} - 3.5V.

Note 7: Defined as the time from when V_{SET} exceeds V_{SETTH} (1.20V typ) to when V_{GATE2} exceeds V_{CC} - 3.5V.

Note 8: Defined as the time from when V_{SET} falls below V_{SETTH} - 5% (1.14V typ) to when V_{GATE2} falls below V_{CC} - 3.5V.

Note 9: The external pFETs can turn on t_{START} after the IC is powered up and all input conditions are valid.

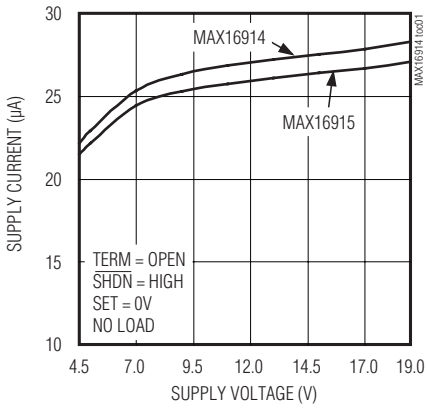
Note 10: Defined as the time from when V_{CC} exceeds the undervoltage-lockout threshold (4.3V max) to when V_{GATE1} and V_{GATE2} fall below 1V.

Note 11: Defined as the time from when V_{CC} falls below $V_{SENSE\ OUT}$ - 25mV to when V_{GATE1} reaches V_{CC} - 1.75V.

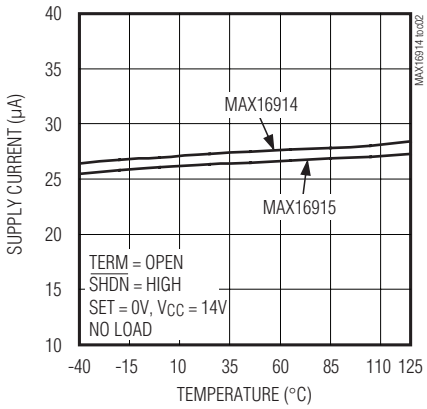
Typical Operating Characteristics

(V_{CC} = 14V, $V_{\overline{SHDN}}$ = 14V, MAX16914/MAX16915 Evaluation Kit, T_A = +25°C, unless otherwise noted.)

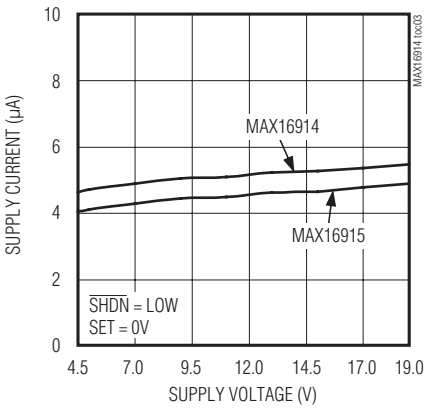
SUPPLY CURRENT vs. SUPPLY VOLTAGE



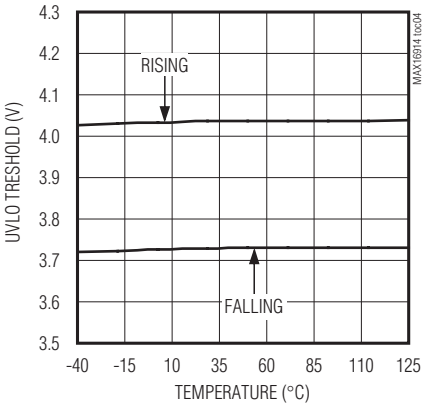
SUPPLY CURRENT vs. TEMPERATURE



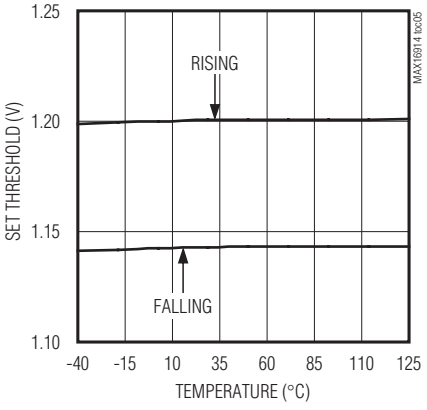
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



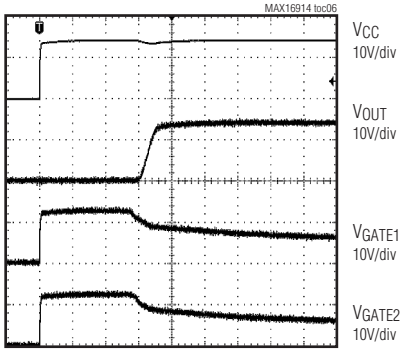
UVLO THRESHOLD vs. TEMPERATURE



SET THRESHOLD vs. TEMPERATURE

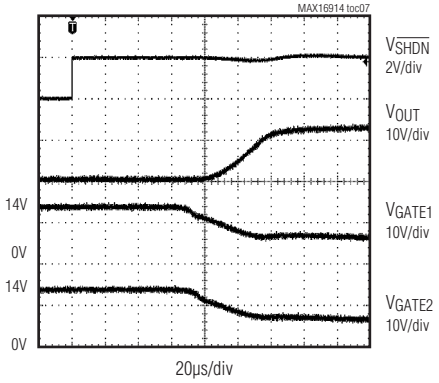


POWER-UP RESPONSE



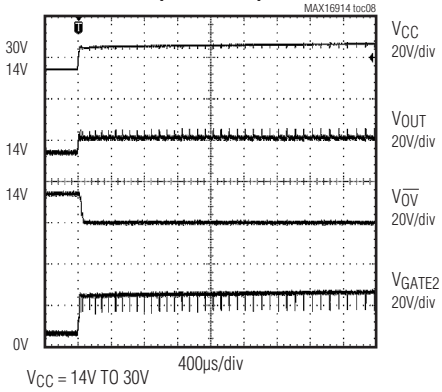
22µF INPUT AND OUTPUT CAPACITOR, R_{OUT} = 100Ω, $\overline{SHDN}$ = HIGH

STARTUP FROM SHUTDOWN RESPONSE



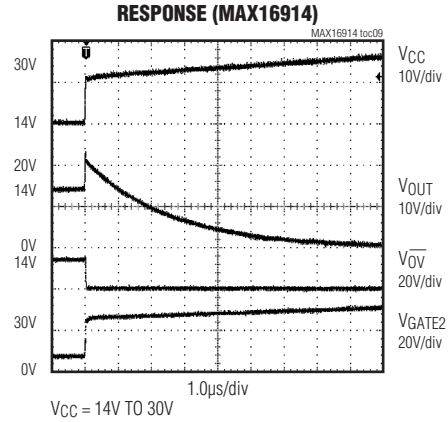
100µF INPUT CAPACITOR, 122µF OUTPUT CAPACITOR, R_{OUT} = 100Ω

OVERVOLTAGE LIMITER RESPONSE (MAX16915)



V_{CC} = 14V TO 30V
TRIP THRESHOLD = 22V
100µF INPUT CAPACITOR, 22µF
OUTPUT CAPACITOR, R_{OUT} = 100Ω
$C_{\overline{OV}}$ = 10nF

OVERVOLTAGE SWITCH-OFF RESPONSE (MAX16914)

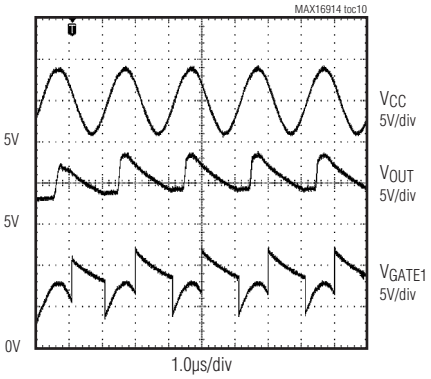


V_{CC} = 14V TO 30V
TRIP THRESHOLD = 22V
100µF INPUT CAPACITOR, 22µF
OUTPUT CAPACITOR, R_{OUT} = 100Ω

Typical Operating Characteristics (continued)

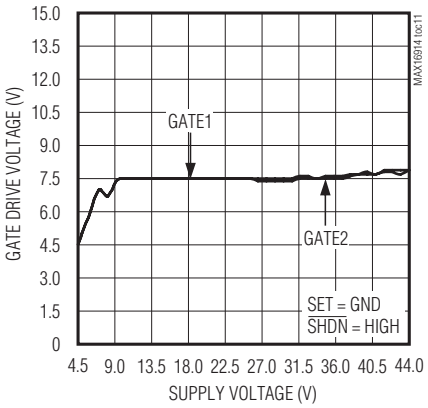
(V_{CC} = 14V, $V_{\overline{SHDN}}$ = 14V, MAX16914/MAX16915 Evaluation Kit, T_A = +25°C, unless otherwise noted.)

BACK-CHARGE RESPONSE

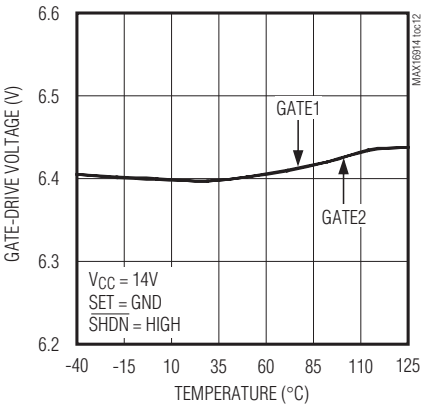


2.2µF INPUT CAPACITOR, 400Ω
INPUT RESISTOR, 22µF OUTPUT CAPACITOR

V_{CC} - $V_{GATE\_}$ vs. INPUT VOLTAGE



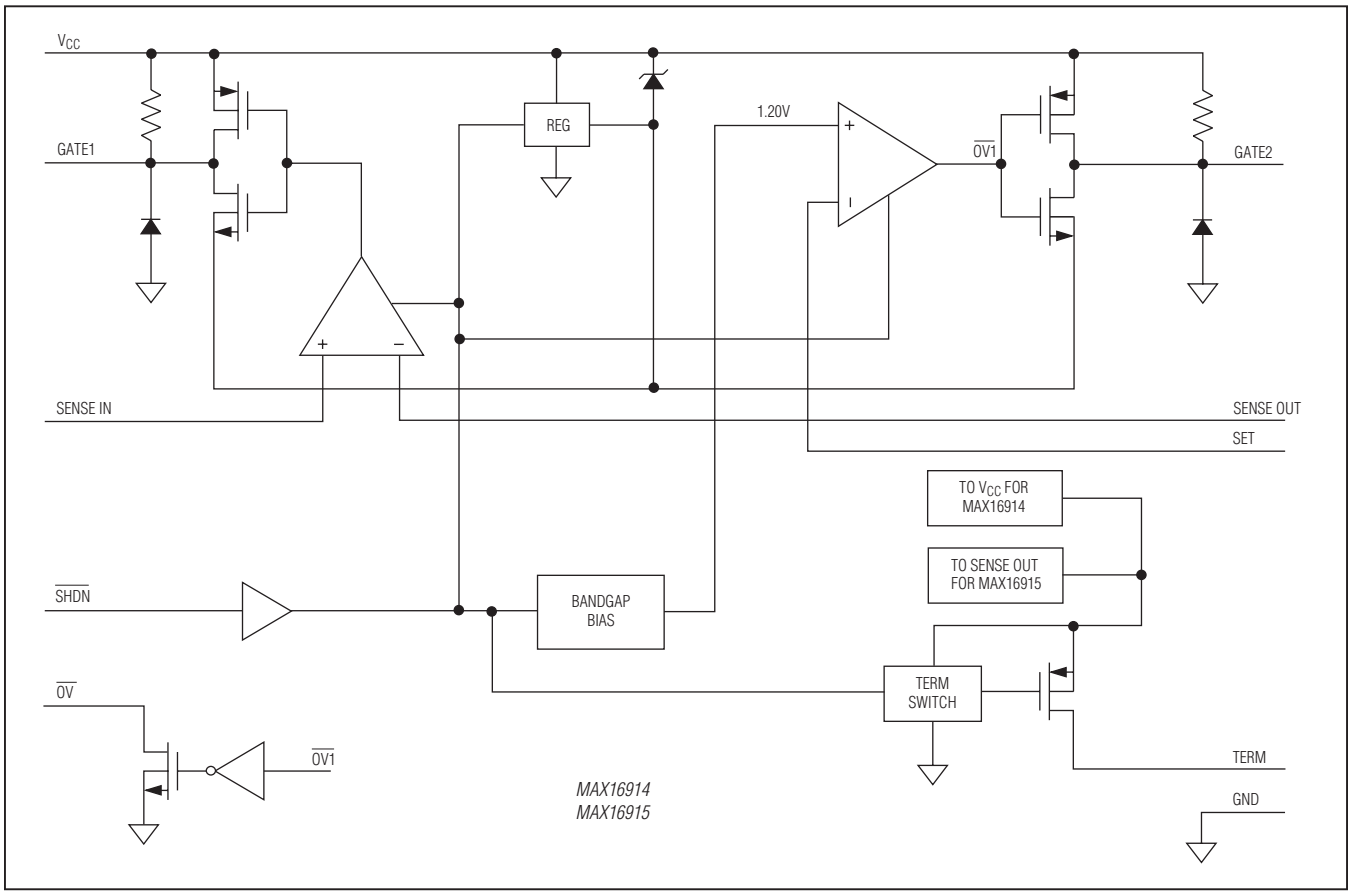
GATE-DRIVE VOLTAGE vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	V_{CC}	Positive Supply Input Voltage. Bypass V_{CC} to GND with a 0.1µF or greater ceramic capacitor.
2	GATE1	Gate-Driver Output. Connect GATE1 to the gate of an external p-channel FET pass switch to provide low drain-to-source voltage drop, reverse voltage protection, and back-charge prevention.
3	SENSE IN	Differential Voltage Sense Input (Input Side of IC). Used with SENSE OUT to provide back-charge prevention when the SENSE IN voltage falls below the SENSE OUT voltage by 25mV.
4	$\overline{SHDN}$	Active-Low Shutdown/Wake Input. Drive $\overline{SHDN}$ high to turn on the voltage detectors. GATE2 is shorted to V_{CC} when $\overline{SHDN}$ is low. $\overline{SHDN}$ is internally pulled to GND through a 0.5µA current sink. Connect $\overline{SHDN}$ to V_{CC} for always-on operation.
5	$\overline{OV}$	Open-Drain Overvoltage Indicator Output. Connect a pullup resistor from $\overline{OV}$ to a positive supply such as V_{CC}. $\overline{OV}$ is pulled low when the voltage at SET exceeds the internal threshold.
6	GND	Ground
7	SET	Controller Overvoltage Threshold Programming Input. Connect SET to the center of an external resistive divider network between TERM and GND to adjust the desired overvoltage switch-off or limiter threshold.
8	TERM	Voltage-Divider Termination Output. TERM is internally connected to SENSE OUT in the MAX16915 and to V_{CC} in the MAX16914. TERM is high impedance when $\overline{SHDN}$ is low, forcing the current to zero in the resistor-divider connected to TERM.
9	SENSE OUT	Differential Voltage Sense Input (Output Side Of IC). Used with SENSE IN to provide back-charge prevention when the SENSE IN voltage falls below the SENSE OUT voltage by 25mV.
10	GATE2	Gate-Driver Output. Connect GATE2 to the gate of an external p-channel FET pass switch. GATE2 is driven low during normal operation and quickly regulated or shorted to V_{CC} during an overvoltage condition. GATE2 is shorted to V_{CC} when $\overline{SHDN}$ is low.

Functional Diagram



Detailed Description

The MAX16914/MAX16915 are ultra-small, low-quiescent, high load-current, overvoltage-protection circuits for automotive or industrial applications. These devices monitor the input and output voltages and control two p-channel MOSFETs to protect downstream loads from reverse-battery, overvoltage, and high-voltage transient conditions and prevent downstream tank capacitors from discharging into the source (back-charging).

One MOSFET (P1) eliminates the need for external diodes, thus minimizing the input voltage drop and provides back-charge and reverse-battery protection. The second MOSFET (P2) isolates the load or regulates the output voltage during an overvoltage condition. These ICs allow system designers to size the external p-channel MOSFET to their load current, voltage drop, and board size.

Overvoltage Switch-Off Controller (MAX16914)

In the MAX16914, the input voltage is monitored (TERM is internally shorted to V_{CC}—see the *Functional Diagram*) making the device an overvoltage switch-off controller. As the V_{CC} voltage rises, and the programmed overvoltage threshold is tripped, the internal fast comparator turns off the external p-channel MOSFET (P2), pulling GATE2 to V_{CC} to disconnect the power source from the load. When the monitored voltage goes below the adjusted overvoltage threshold, the MAX16914 enhances GATE2, reconnecting the load to the power source.

Overvoltage Limiter Controller (MAX16915)

In the MAX16915, TERM is internally connected to SENSE OUT (see the *Functional Diagram*) allowing the IC to operate in voltage-limiter mode.

During normal operation, GATE2 is pulled low to fully enhance the MOSFET. The external MOSFET's drain voltage is monitored through a resistor-divider between TERM, SET, and GND. When the output voltage rises above the adjusted overvoltage threshold, an internal comparator pulls GATE2 to V_{CC} turning off P2. When the monitored voltage goes below the overvoltage threshold (-4% hysteresis), the p-channel MOSFET (P2) is turned on again. During a continuous overvoltage condition, MOSFET (P2) cycles on and off (between the overvoltage threshold and the hysteresis), generating a sawtooth waveform with a frequency dependent on the load capacitance and load current. This process continues to keep the voltage at the output regulated to within approximately a 4% window. The output voltage is regulated during the overvoltage transients and MOSFET (P2) continues to conduct during the overvoltage event, operating in switched-linear mode.

Caution must be exercised when operating the MAX16915 in voltage-limiting mode for long durations due to the MOSFET's power-dissipation consideration (see the *MOSFET Selection* section).

Shutdown

The MAX16914/MAX16915 feature an active-low shutdown input ($\overline{SHDN}$). Drive $\overline{SHDN}$ low to switch off FET (P2), disconnecting the input from the output, thus placing the IC in low-quiescent-current mode. Reverse-battery protection is still maintained.

Reverse-Battery Protection

The MAX16914/MAX16915 feature reverse-battery protection to prevent damage to the downstream circuitry caused by battery reversal or negative transients. The reverse-battery protection blocks the flow of current into the downstream load and allows the circuit designer to remove series-protection diodes.

Back-Charge Switch-Off

The MAX16914/MAX16915 monitor the input-to-output differential voltage between SENSE IN and SENSE OUT. It turns off the external FET (P1) when ($V_{SENSE\ OUT}$ - $V_{SENSE\ IN}$) > 25mV (see Figure 1) to prevent discharging of a downstream tank capacitor into the battery supply during an input voltage drop, such as a cold-crank condition or during a superimposed sinusoidal voltage on top of the supply voltage. It turns on the FET (P1) again if the back-charge voltage threshold hysteresis of 50mV is satisfied.

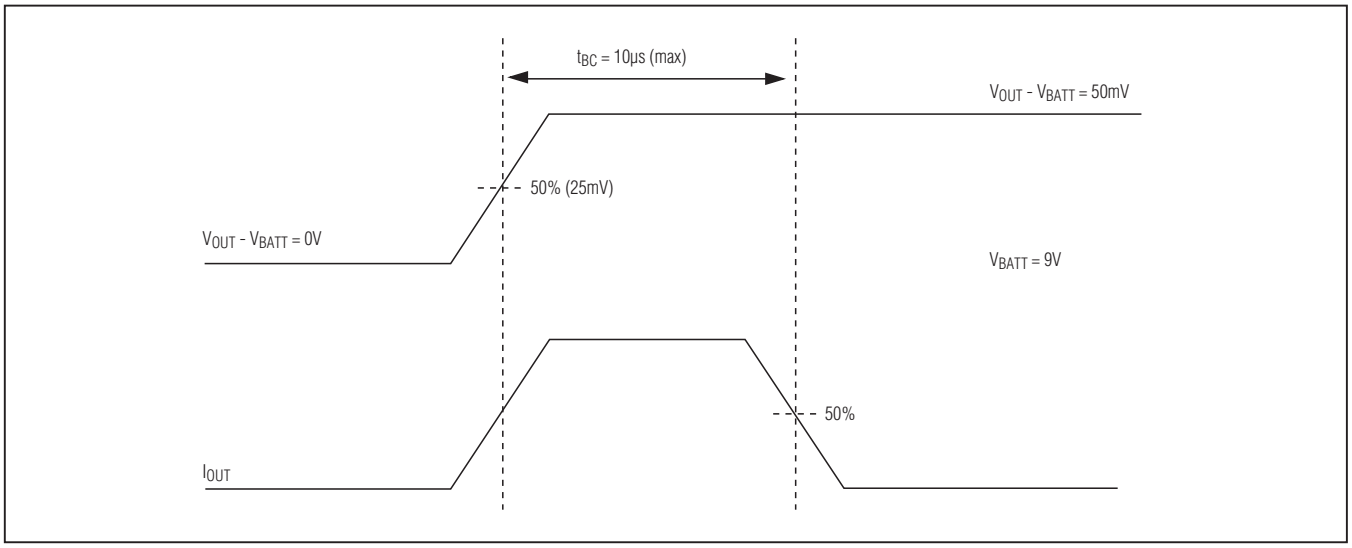


Figure 1. Back-Charge Turn-Off Time

Overvoltage Indicator Output ($\overline{OV}$)

The MAX16914/MAX16915 include an active-low, open-drain overvoltage-indicator output ($\overline{OV}$). For the MAX16914, $\overline{OV}$ asserts low when V_{CC} exceeds the programmed overvoltage threshold. $\overline{OV}$ deasserts when the overvoltage condition is over.

For the MAX16915, $\overline{OV}$ asserts if V_{OUT} exceeds the programmed overvoltage threshold. $\overline{OV}$ deasserts when V_{OUT} drops 4% (typ) below the overvoltage threshold level. If the overvoltage condition continues, $\overline{OV}$ may toggle with the same frequency as the overvoltage limiter FET (P2). If the P2 device is turned on for a very short period (less than t_{OVBPD}), the $\overline{OV}$ pin may not toggle. To obtain a logic-level output, connect a 45kΩ pullup resistor from $\overline{OV}$ to a system voltage less than 44V. A capacitor connected from $\overline{OV}$ to GND helps extend the time that the logic level remains low.

Applications Information

Load Dump

Most automotive applications run off a multicell "12V" lead-acid battery with a nominal voltage that swings between 9V and 16V (depending on load current, charging status, temperature, battery age, etc.). The battery voltage is distributed throughout the automobile and is locally regulated down to voltages required by the different system modules. Load dump occurs when the alternator is charging the battery and the battery becomes disconnected. The alternator voltage regulator is temporarily driven out of control. Power from the alternator flows into the distributed power system and elevates the voltage seen at each module. The voltage spikes have rise times typically greater than 5ms and decays within several hundred milliseconds but can extend out to 1s or more depending on the characteristics of the charging system. These transients are capable of destroying sensitive electronic equipment on the first "fault event."

Setting Overvoltage Thresholds

TERM and SET provide an accurate means to set the overvoltage level for the MAX16914/MAX16915. Use a resistive divider to set the desired overvoltage condition (see the *Typical Operating Circuit*). V_{SET} has a rising 1.20V threshold with a 4% falling hysteresis. Begin by selecting the total end-to-end resistance:

$$R_{TOTAL} = R1 + R2$$

For high accuracy, choose R_{TOTAL} to yield a total current equivalent to a minimum 100 x I_{SET} where I_{SET} is the input bias current at SET.

For example:

With an overvoltage threshold (V_{OV}) set to 20V, R_{TOTAL} < 20V/(100 x I_{SET}), where I_{SET} = 1µA (max).

$$R_{TOTAL} < 200k\Omega$$

Use the following formula to calculate R2:

$$R2 = (V_{TH} \times R_{TOTAL})/V_{OV}$$

where V_{TH} is the 1.20V SET rising threshold and V_{OV} is the desired overvoltage threshold.

Then, R2 = 12.0kΩ.

Use the nearest standard-value resistor lower than the calculated value. A lower value for total resistance dissipates more power but provides slightly better accuracy.

To determine R1:

$$R_{TOTAL} = R2 + R1$$

Then, R1 = 188kΩ.

Use the nearest standard-value resistor lower than the calculated value. A lower value for total resistance dissipates more power but provides slightly better accuracy.

MOSFET Selection

Output p-Channel MOSFET (P2)

Select the external output MOSFET according to the application current level. The MOSFET's on-resistance ($R_{DS(ON)}$) should be chosen low enough to have a minimum voltage drop at full load to limit the MOSFET power dissipation. Determine the device power rating to accommodate an overvoltage fault when operating the MAX16915 in overvoltage-limiting mode. During normal operation for either IC, the external MOSFET dissipates little power. The power dissipated in the MOSFET during normal operation is:

$$P_{NORM} = I_{LOAD}^2 \times R_{DS(ON)}$$

where P_{NORM} is the power dissipated in the MOSFET in normal operation, I_{LOAD} is the output load current, and $R_{DS(ON)}$ is the drain-to-source resistance of the MOSFET. Worst-case power dissipation in the output MOSFET occurs during a prolonged overvoltage event when operating the MAX16915 in voltage-limiting mode. The power dissipated across the MOSFET is as follows:

$$P_{OVLO} = V_{DS} \times I_{LOAD}$$

where P_{OVLO} is the power dissipated in the MOSFET in overvoltage-limiting operation, V_{DS} is the voltage across the MOSFET's drain and source, and I_{LOAD} is the load current.

Reverse-Polarity Protection MOSFET (P1)

Most battery-powered applications must include reverse-voltage protection. Many times this is implemented with a diode in series with the battery. The disadvantage in using a diode is the forward-voltage drop of the diode, which reduces the operating voltage available to downstream circuits ($V_{LOAD} = V_{BATTERY} - V_{DIODE}$).

The MAX16914/MAX16915 include high-voltage GATE1 drive circuitry allowing users to replace the high-voltage drop series diode with a low-voltage-drop MOSFET device (as shown in the *Typical Operating Circuit*). The forward-voltage drop is reduced to $I_{LOAD} \times R_{DS(ON)}$ of P1. With a suitably chosen MOSFET, the voltage drop can be reduced to millivolts.

In normal operating mode, internal GATE1 output circuitry enhances P1. The constant enhancement ensures P1 operates in a low $R_{DS(ON)}$ mode, but the gate-source junction is not overstressed during high battery-voltage applications or transients (many MOSFET devices specify a ±20V V_{GS} absolute maximum). As V_{CC} drops below 10V, GATE1 is limited to GND, reducing P1 V_{GS} to V_{CC}. In normal operation, the P1 power dissipation is very low:

$$P1 = I_{LOAD}^2 \times R_{DS(ON)}$$

During reverse-battery conditions, GATE1 is limited to GND and the P1 gate-source junction is reverse biased. P1 is turned off and neither the MAX16914/MAX16915 nor the load circuitry is exposed to the reverse-battery voltage. Care should be taken to place P1 (and its internal drain-to-source diode) in the correct orientation for proper reverse-battery operation.

Thermal Shutdown

The MAX16914/MAX16915 thermal-shutdown feature turns off both MOSFETs if the IC junction temperature exceeds the maximum allowable thermal dissipation. When the junction temperature exceeds T_J = +170°C, the thermal sensor signals the shutdown logic, turning off both GATE1 and GATE2 outputs and allowing the device to cool. The thermal sensor turns GATE1 and GATE2 on again after the IC's junction temperature cools by 20°C. For continuous operation, do not exceed the absolute maximum junction-temperature rating of T_J = +150°C.

Chip Information

PROCESS: BiCMOS

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX16914AUB+	-40°C to +125°C	10 µMAX
MAX16915AUB+	-40°C to +125°C	10 µMAX

+Denotes a lead(Pb)-free/RoHS-compliant package.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
10 µMAX	U10+2	**21-0061**	**90-0330**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/09	Initial release	—
1	4/13	Added commercial-grade OPNs to *Ordering Information*	1
2	10/14	Removed automotive reference from *Applications* and /V OPNs from *Ordering Information*	1
3	2/15	Updated the *Benefits and Features* section	1

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