MAX16936/MAX16938 36V, 220kHz to 2.2MHz Step-Down Converters with 28μA Quiescent Current

General Description

The MAX16936/MAX16938 are 2.5A current-mode step-down converters with integrated high-side and low-side MOSFETs designed to operate with an external Schottky diode for better efficiency. The low-side MOSFET enables fixed-frequency forced-PWM (FPWM) operation under light-load applications. The devices operate with input voltages from 3.5V to 36V, while using only 28μA quiescent current at no load. The switching frequency is resistor programmable from 220kHz to 2.2MHz and can be synchronized to an external clock. The devices' output voltage is available as 5V/3.3V fixed or adjustable from 1V to 10V. The wide input voltage range along with its ability to operate at 98% duty cycle during undervoltage transients make the devices ideal for automotive and industrial applications.

Under light-load applications, the FSYNC logic input allows the devices to either operate in skip mode for reduced current consumption or fixed-frequency FPWM mode to eliminate frequency variation to minimize EMI. Fixed-frequency FPWM mode is extremely useful for power supplies designed for RF transceivers where tight emission control is necessary. Protection features include cycle-by-cycle current limit and thermal shutdown with automatic recovery. Additional features include a power-good monitor to ease power-supply sequencing and a 180º out-of-phase clock output relative to the internal oscillator at SYNCOUT to create cascaded power supplies with multiple devices.

The MAX16936/MAX16938 operate over the -40ºC to +125ºC automotive temperature range and are available in 16-pin TSSOP-EP and 5mm x 5mm, 16-pin TQFN-EP packages.

Applications

- Point-of-Load Applications
- Distributed DC Power Systems
- Navigation and Radio Head Units

Benefits and Features

- Integration and High-Switching Frequency Saves Space
  - Integrated 2.5A High-Side Switch
  - Low-BOM-Count Current-Mode Control Architecture
  - Fixed Output Voltage with ±2% Accuracy (5V/3.3V) or Externally Resistor Adjustable (1V to 10V)
  - 220kHz to 2.2MHz Switching Frequency with Three Operation Modes (Skip Mode, Forced Fixed-Frequency Operation, and External Frequency Synchronization)
  - Automatic LX Slew-Rate Adjustment for Optimum Efficiency Across Operating Frequency Range
- 180° Out-of-Phase Clock Output at SYNCOUT Enables Cascaded Power Supplies for Increased Power Output
- Spread-Spectrum Frequency Modulation Reduces EMI Emissions
- Wide Input Voltage Range Supports Automotive Applications
  - 3.5V to 36V Input Voltage Range
  - Enable Input Compatible from 3.3V Logic Level to 42V
- Robust Performance Supports Wide Range of Automotive Applications
  - 42V Load-Dump Protection
  - -40°C to +125°C Automotive Temperature Range
  - Thermal-Shutdown Protection
  - AEC-Q100 Qualified
- Power-Good Output Allows Power-Supply Sequencing
- Tight Overvoltage Protection Provides Smaller Overshoot Voltages (MAX16938)

Ordering Information/Selector Guide **and** ***Typical Application Circuit*** **appear at end of data sheet.**

Absolute Maximum Ratings

SUP, SUPSW, EN to PGND ....-0.3V to +42V
LX (Note 1) ....-0.3V to +42V
SUP to SUPSW ....-0.3V to +0.3V
BIAS to AGND ....-0.3V to +6V
SYNCOUT, FOSC, COMP, FSYNC,
PGOOD, FB to AGND .... -0.3V to (V_{BIAS} + 0.3V)
OUT to PGND ....-0.3V to +12V
BST to LX (Note 1) ....-0.3V to +6V
AGND to PGND ....-0.3V to + 0.3V
LX Continuous RMS Current 3A

Output Short-Circuit Duration ....Continuous
Continuous Power Dissipation (T_A = +70°C)*
TSSOP (derate 26.1mw/°C above +70°C) 2088.8mW
TQFN (derate 28.6mw/°C above +70°C) 2285.7mW
Operating Temperature Range .... -40°C to +125°C
Junction Temperature ....+150°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

**As per JEDEC51 standard (multilayer board).*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

TSSOP

Junction-to-Ambient Thermal Resistance (θ_{JA}) ....38.3°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ....3°C/W

TQFN

Junction-to-Ambient Thermal Resistance (θ_{JA}) ....35°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ....2.7°C/W

Note 1: Self-protected against transient voltages exceeding these limits for ≤ 50ns under normal operation and loads up to the maximum rated output current.

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{SUP} = V_{SUPSW} = 14V, V_{EN} = 14V, L1 = 2.2μH, C_{IN} = 4.7μF, C_{OUT} = 22μF, C_{BIAS} = 1μF, C_{BST} = 0.1μF, R_{FOSC} = 12kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{SUP}, V_{SUPSW}		3.5		36	V
Load Dump Event Supply Voltage	V_{SUP_LD}	t_{LD} < 1s			42	V
Supply Current	$I_{SUP\_STANDBY}$	Standby mode, no load, V_{OUT} = 5V, V_{FSYNC} = 0V		28	40	μA
		Standby mode, no load, V_{OUT} = 3.3V, V_{FSYNC} = 0V		22	35	
Shutdown Supply Current	I_{SHDN}	V_{EN} = 0V		5	8	μA
BIAS Regulator Voltage	V_{BIAS}	V_{SUP} = V_{SUPSW} = 6V to 42V, I_{BIAS} = 0 to 10mA	4.7	5	5.4	V
BIAS Undervoltage Lockout	V_{UVBIAS}	V_{BIAS} rising	2.95	3.15	3.40	V
BIAS Undervoltage-Lockout Hysteresis				450	650	mV
Thermal Shutdown Threshold				+175		°C
Thermal Shutdown Threshold Hysteresis				15		°C

Electrical Characteristics (continued)

(V_{SUP} = V_{SUPSW} = 14V, V_{EN} = 14V, L1 = 2.2μH, C_{IN} = 4.7μF, C_{OUT} = 22μF, C_{BIAS} = 1μF, C_{BST} = 0.1μF, R_{FOSC} = 12kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OUTPUT VOLTAGE (OUT)							
FPWM Mode Output Voltage (Note 3)	V_{OUT_5V}	V_{FB} = V_{BIAS}, 6V < V_{SUPSW} < 36V, MAX16936/38/38____A/V+, fixed-frequency mode		4.9	5	5.1	V
	$V_{OUT\_3.3V}$	V_{FB} = V_{BIAS}, 6V < V_{SUPSW} < 36V, MAX16936/38____B/V+, fixed-frequency mode		3.234	3.3	3.366	
Skip-Mode Output Voltage (Note 4)	V_{OUT_5V}	No load, V_{FB} = V_{BIAS}, MAX16936/38____A/V+, skip mode		4.9	5	5.15	V
	$V_{OUT\_3.3V}$	V_{FB} = V_{BIAS}, 6V < V_{SUPSW} < 36V, MAX16936/38____B/V+, skip mode		3.234	3.3	3.4	
Load Regulation		V_{FB} = V_{BIAS}, 300mA < I_{LOAD} < 2.5A			0.5		%
Line Regulation		V_{FB} = V_{BIAS}, 6V < V_{SUPSW} < 36V			0.02		%/V
BST Input Current	I_{BST_ON}	High-side MOSFET on, V_{BST} - V_{LX} = 5V		1	1.5	2	mA
	I_{BST_OFF}	High-side MOSFET off, V_{BST} - V_{LX} = 5V, T_A = +25°C				5	μA
LX Current Limit	I_{LX}	Peak inductor current		3	3.75	4.5	A
LX Rise Time		R_{FOSC} = 12kΩ			4		ns
Skip-Mode Current Threshold	I_{SKIP_TH}	T_A = +25°C	MAX16936	150	300	400	mA
			MAX16938	200	400	500	
Spread Spectrum		Spread spectrum enabled			f_{OSC} ±6%		
High-Side Switch On-Resistance	R_{ON_H}	I_{LX} = 1A, V_{BIAS} = 5V			100	220	mΩ
High-Side Switch Leakage Current		High-side MOSFET off, V_{SUP} = 36V, V_{LX} = 0V, T_A = +25°C			1	3	μA
Low-Side Switch On-Resistance	R_{ON_L}	I_{LX} = 0.2A, V_{BIAS} = 5V			1.5	3	Ω
Low-Side Switch Leakage Current		V_{LX} = 36V, T_A = +25°C				1	μA
TRANSCONDUCTANCE AMPLIFIER (COMP)							
FB Input Current	I_{FB}				20	100	nA
FB Regulation Voltage	V_{FB}	FB connected to an external resistor-divider, 6V < V_{SUPSW} < 36V (Note 5)		0.99	1.0	1.015	V
FB Line Regulation	ΔV_{LINE}	6V < V_{SUPSW} < 36V			0.02		%/V
Transconductance (from FB to COMP)	g_m	V_{FB} = 1V, V_{BIAS} = 5V			700		μS
Minimum On-Time	t_{ON_MIN}	(Note 4)			80		ns
Maximum Duty Cycle	DC_{MAX}				98		%

Electrical Characteristics (continued)

(V_{SUP} = V_{SUPSW} = 14V, V_{EN} = 14V, L1 = 2.2μH, C_{IN} = 4.7μF, C_{OUT} = 22μF, C_{BIAS} = 1μF, C_{BST} = 0.1μF, R_{FOSC} = 12kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

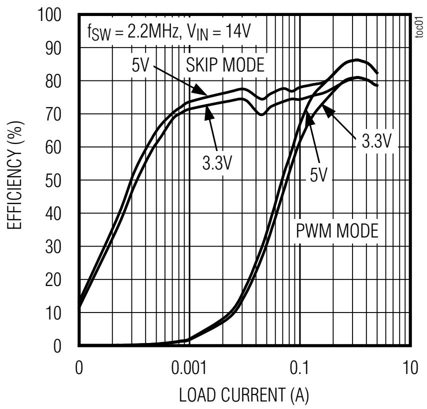
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OSCILLATOR FREQUENCY							
Oscillator Frequency		R_{FOSC} = 73.2kΩ		340	400	460	kHz
		R_{FOSC} = 12kΩ		2.0	2.2	2.4	MHz
EXTERNAL CLOCK INPUT (FSYNC)							
External Input Clock Acquisition Time	t_{FSYNC}				1		Cycles
External Input Clock Frequency		R_{FOSC} = 12kΩ (Note 6)		1.8		2.6	MHz
External Input Clock High Threshold	V_{FSYNC_HI}	V_{FSYNC} rising		1.4			V
External Input Clock Low Threshold	V_{FSYNC_LO}	V_{FSYNC} falling				0.4	V
Soft-Start Time	t_{SS}			5.6	8	12	ms
ENABLE INPUT (EN)							
Enable Input High Threshold	V_{EN_HI}			2.4			V
Enable Input Low Threshold	V_{EN_LO}					0.6	
Enable Threshold-Voltage Hysteresis	V_{EN_HYS}				0.2		V
Enable Input Current	I_{EN}	T_A = +25°C			0.1	1	μA
POWER GOOD ($\overline{PGOOD}$)							
$\overline{PGOOD}$ Switching Level	V_{TH_RISING}	V_{FB} rising, $V_{\overline{PGOOD}}$ = high		93	95	97	$\%V_{FB}$
	$V_{TH\_FALLING}$	V_{FB} falling, $V_{\overline{PGOOD}}$ = low		90	92	94	
$\overline{PGOOD}$ Debounce Time				10	25	50	μs
$\overline{PGOOD}$ Output Low Voltage		I_{SINK} = 5mA				0.4	V
$\overline{PGOOD}$ Leakage Current		V_{OUT} in regulation, T_A = +25°C				1	μA
SYNCOUT Low Voltage		I_{SINK} = 5mA				0.4	V
SYNCOUT Leakage Current		T_A = +25°C				1	μA
FSYNC Leakage Current		T_A = +25°C				1	μA
OVERVOLTAGE PROTECTION							
Overvoltage-Protection Threshold		V_{OUT} rising (monitored at FB pin)	MAX16936		107		%
			MAX16938		105		
		V_{OUT} falling (monitored at FB pin)	MAX16936		105		
			MAX16938		102		

Note 3: Device not in dropout condition.
Note 4: Guaranteed by design; not production tested.
Note 5: FB regulation voltage is 1%, 1.01V (max), for -40°C < T_A < +105°C.
Note 6: Contact the factory for SYNC frequency outside the specified range.

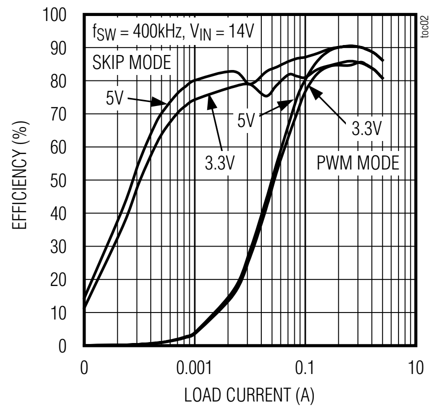
Typical Operating Characteristics

(V_{SUP} = V_{SUPSW} = 14V, V_{EN} = 14V, V_{OUT} = 5V, V_{FYSNC} = 0V, R_{FOSC} = 12kΩ, T_A = +25°C, unless otherwise noted.)

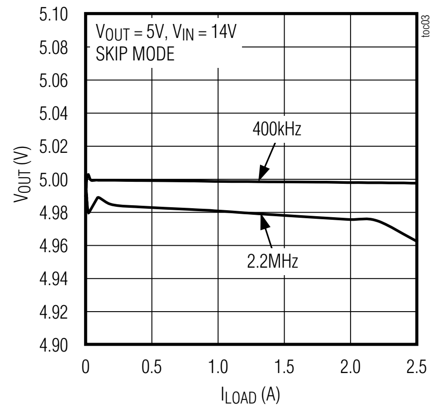
EFFICIENCY vs. LOAD CURRENT



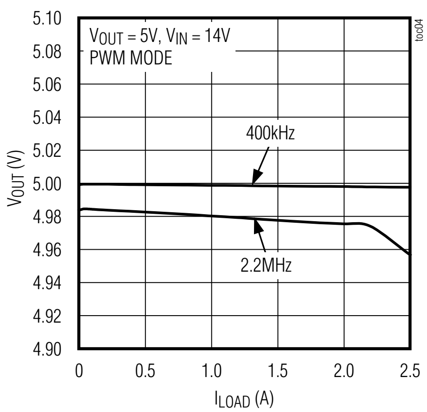
EFFICIENCY vs. LOAD CURRENT



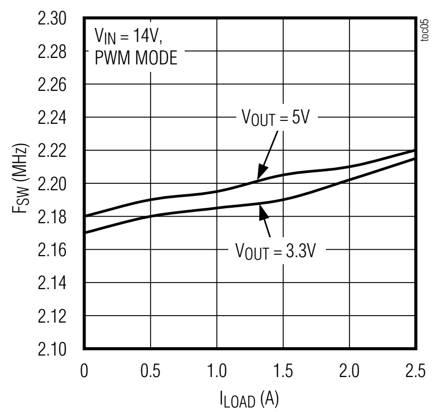
VOUT LOAD REGULATION



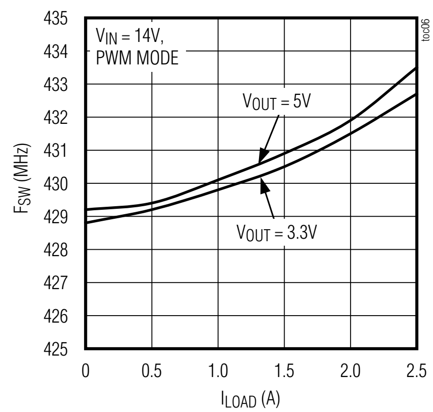
VOUT LOAD REGULATION



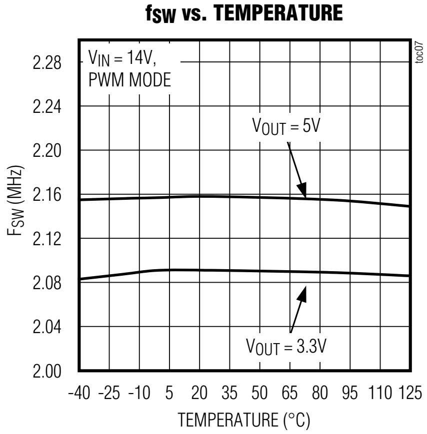
fSW vs. LOAD CURRENT



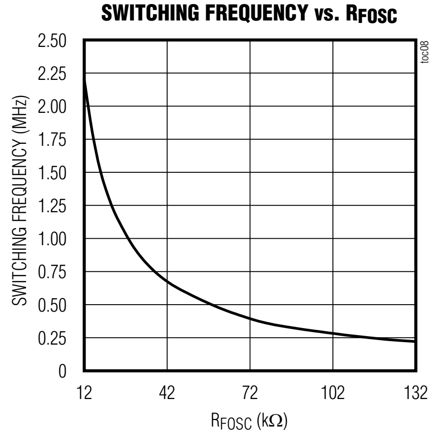
fSW vs. LOAD CURRENT



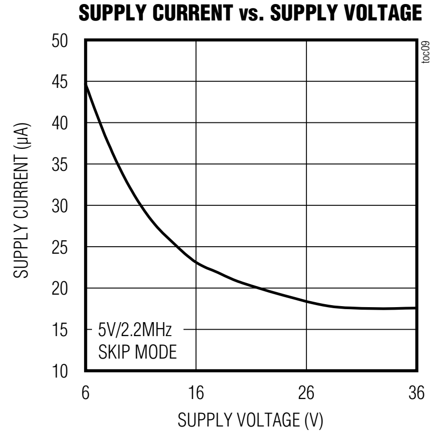
fSW vs. TEMPERATURE



SWITCHING FREQUENCY vs. RFOSC



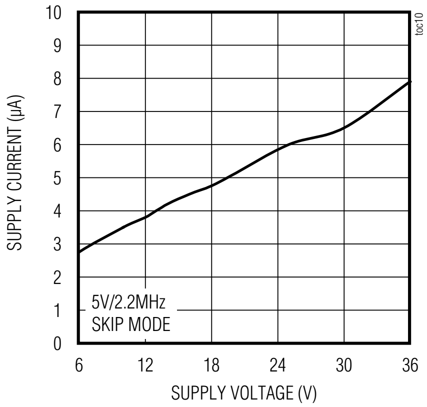
SUPPLY CURRENT vs. SUPPLY VOLTAGE



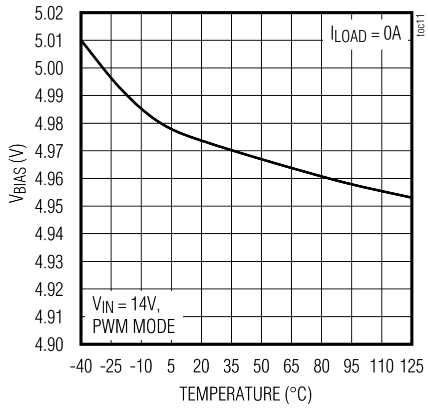
Typical Operating Characteristics (continued)

(V_{SUP} = V_{SUPSW} = 14V, V_{EN} = 14V, V_{OUT} = 5V, V_{FYSNC} = 0V, R_{FOSC} = 12kΩ, T_A = +25°C, unless otherwise noted.)

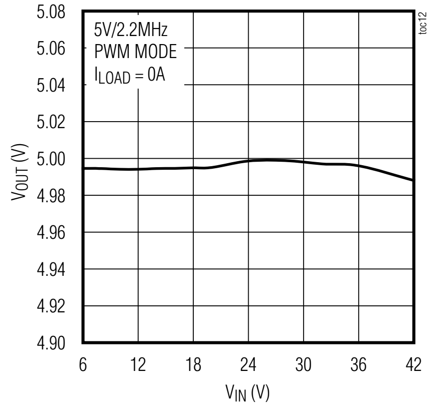
SHDN CURRENT vs. SUPPLY VOLTAGE



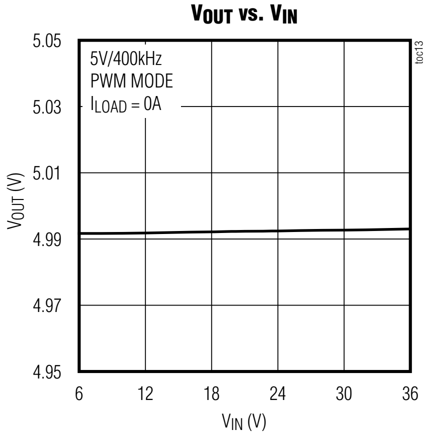
VBIAS vs. TEMPERATURE



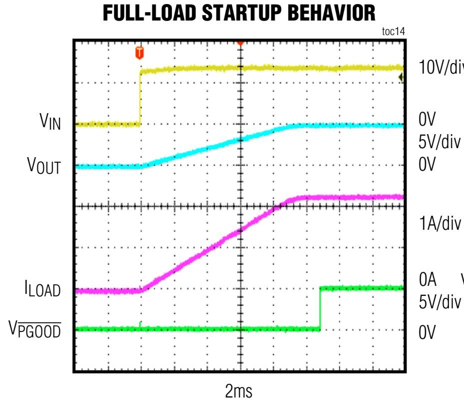
VOUT vs. VIN



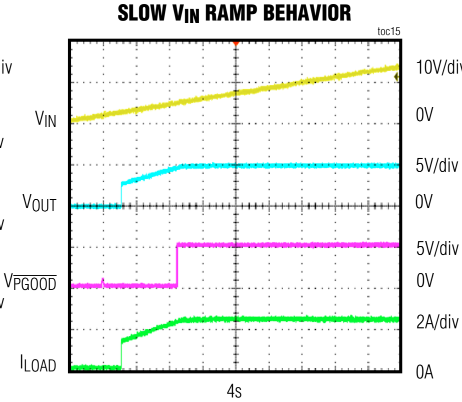
VOUT vs. VIN



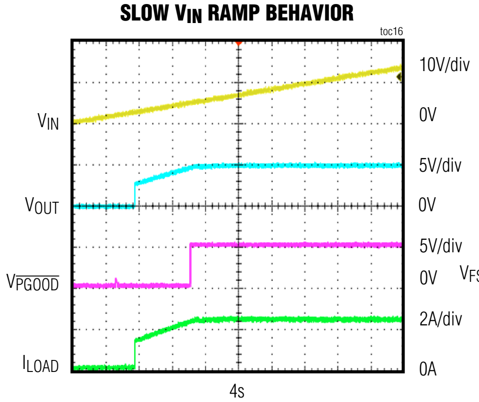
FULL-LOAD STARTUP BEHAVIOR



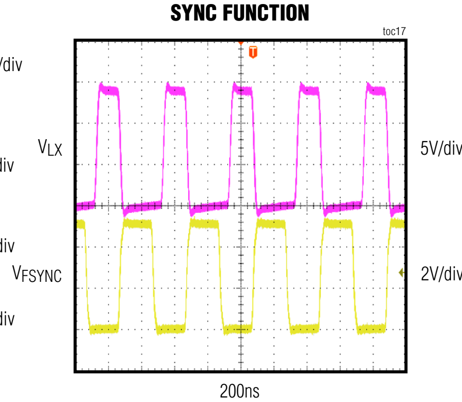
SLOW VIN RAMP BEHAVIOR



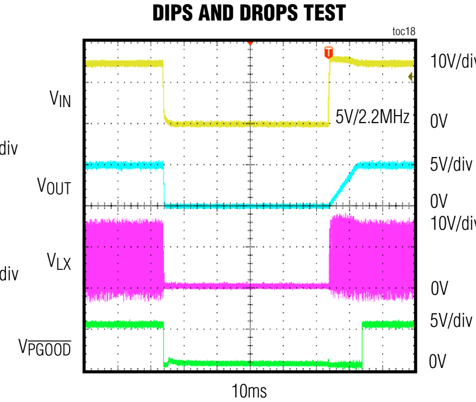
SLOW VIN RAMP BEHAVIOR



SYNC FUNCTION

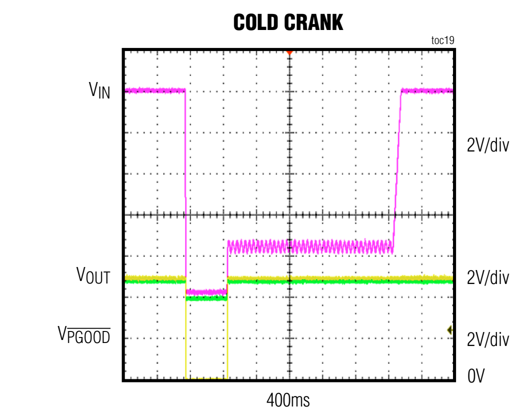


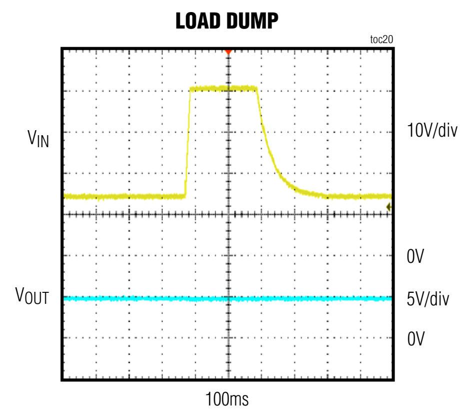
DIPS AND DROPS TEST

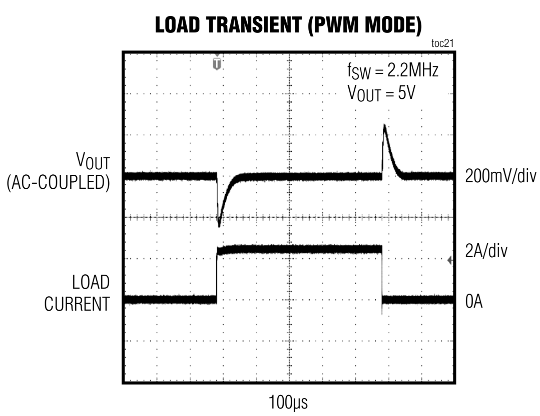


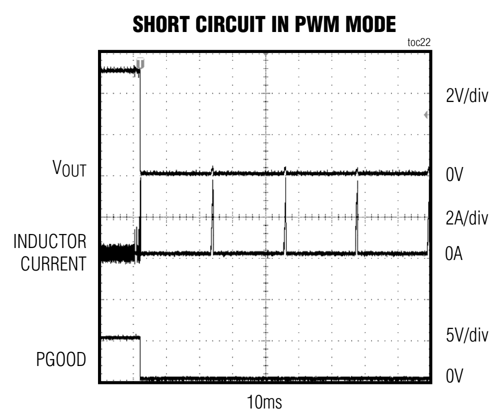
Typical Operating Characteristics (continued)

(V_{SUP} = V_{SUPSW} = 14V, V_{EN} = 14V, V_{OUT} = 5V, V_{FYSNC} = 0V, R_{FOSC} = 12kΩ, T_A = +25°C, unless otherwise noted.)

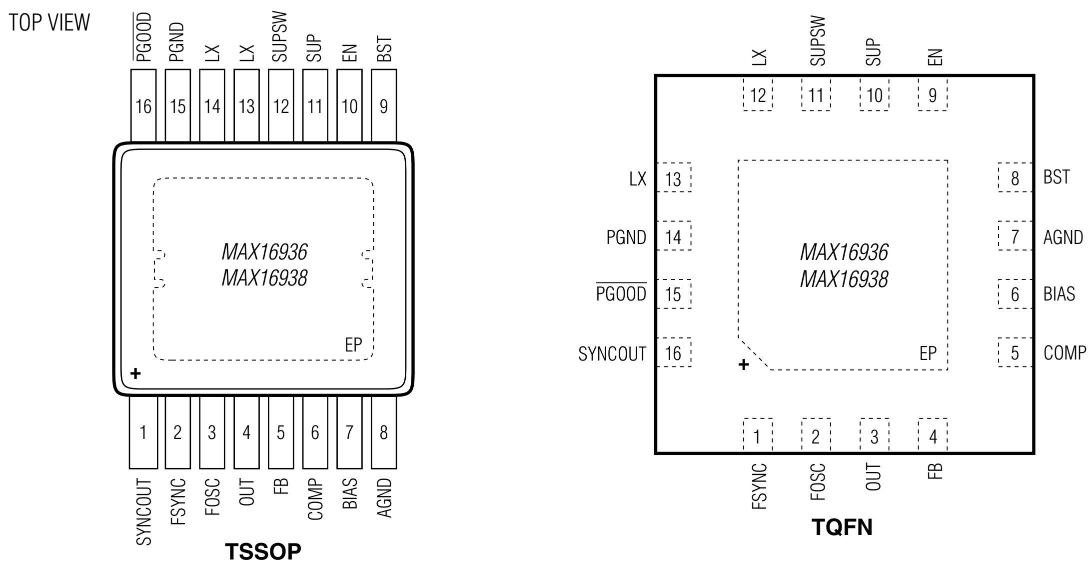








Pin Configurations



Pin Descriptions

PIN		NAME	FUNCTION
TSSOP	TQFN		
1	16	SYNCOUT	Open-Drain Clock Output. SYNCOUT outputs 180° out-of-phase signal relative to the internal oscillator. Connect to OUT with a resistor between 100Ω and 1kΩ for 2MHz operation. For low frequency operation, use a resistor between 1kΩ and 10kΩ.
2	1	FSYNC	Synchronization Input. The device synchronizes to an external signal applied to FSYNC. Connect FSYNC to AGND to enable skip mode operation. Connect to BIAS or to an external clock to enable fixed-frequency forced PWM mode operation.
3	2	FOSC	Resistor-Programmable Switching Frequency Setting Control Input. Connect a resistor from FOSC to AGND to set the switching frequency.
4	3	OUT	Switching Regulator Output. OUT also provides power to the internal circuitry when the output voltage of the converter is set between 3V to 5V during standby mode.
5	4	FB	Feedback Input. Connect an external resistive divider from OUT to FB and AGND to set the output voltage. Connect to BIAS to set the output voltage to 5V.
6	5	COMP	Error Amplifier Output. Connect an RC network from COMP to AGND for stable operation. See the *Compensation Network* section for more information.
7	6	BIAS	Linear Regulator Output. BIAS powers up the internal circuitry. Bypass with a 1μF capacitor to ground.
8	7	AGND	Analog Ground
9	8	BST	High-Side Driver Supply. Connect a 0.1μF capacitor between LX and BST for proper operation.

Pin Descriptions (continued)

PIN		NAME	FUNCTION
TSSOP	TQFN		
10	9	EN	SUP Voltage Compatible Enable Input. Drive EN low to disable the device. Drive EN high to enable the device.
11	10	SUP	Voltage Supply Input. SUP powers up the internal linear regulator. Bypass SUP to PGND with a 4.7μF ceramic capacitor. It is recommended to add a placeholder for an RC filter to reduce noise on the internal logic supply (see the *Typical Application Circuit*)
12	11	SUPSW	Internal High-Side Switch Supply Input. SUPSW provides power to the internal switch. Bypass SUPSW to PGND with 0.1μF and 4.7μF ceramic capacitors.
13, 14	12, 13	LX	Inductor Switching Node. Connect a Schottky diode between LX and PGND.
15	14	PGND	Power Ground
16	15	$\overline{\text{PGOOD}}$	Open-Drain, Active-Low Power-Good Output. $\overline{\text{PGOOD}}$ asserts when V_{OUT} is above 95% regulation point. $\overline{\text{PGOOD}}$ goes low when V_{OUT} is below 92% regulation point.
—	—	EP	Exposed Pad. Connect EP to a large-area contiguous copper ground plane for effective power dissipation. Do not use as the only IC ground connection. EP must be connected to PGND.

Detailed Description

The MAX16936/MAX16938 are 2.5A current-mode step-down converters with integrated high-side and low-side MOSFETs designed to operate with an external Schottky diode for better efficiency. The low-side MOSFET enables fixed-frequency forced-PWM (FPWM) operation under light-load applications. The devices operate with input voltages from 3.5V to 36V, while using only 28μA quiescent current at no load. The switching frequency is resistor programmable from 220kHz to 2.2MHz and can be synchronized to an external clock. The output voltage is available as 5V/3.3V fixed or adjustable from 1V to 10V. The wide input voltage range along with its ability to operate at 98% duty cycle during undervoltage transients make the devices ideal for automotive and industrial applications.

Under light-load applications, the FSYNC logic input allows the device to either operate in skip mode for reduced current consumption or fixed-frequency FPWM mode to eliminate frequency variation to minimize EMI. Fixed frequency FPWM mode is extremely useful for power supplies designed for RF transceivers where tight emission control is necessary. Protection features include cycle-by-cycle current limit, overvoltage protection, and thermal shutdown with automatic recovery. Additional features include a power-good monitor to ease power-supply sequencing and a 180° out-of-phase clock output relative to the internal oscillator at SYNCOUT to create cascaded power supplies with multiple devices.

Wide Input Voltage Range

The devices include two separate supply inputs (SUP and SUPSW) specified for a wide 3.5V to 36V input voltage range. V_{SUP} provides power to the device and V_{SUPSW} provides power to the internal switch. When the device is operating with a 3.5V input supply, conditions such as cold crank can cause the voltage at SUP and SUPSW to drop below the programmed output voltage. Under such conditions, the device operates in a high duty-cycle mode to facilitate minimum dropout from input to output.

Maximum Duty-Cycle Operation

The devices have a maximum duty cycle of 98% (typ). The IC monitors the off-time (time for which the low-side FET is on) in both PWM and skip modes every switching cycle. Once the off-time of 25ns (typ) is detected continuously for 12μs, the low-side FET is forced on for 150ns (typ) every 12μs. The input voltage at which the devices enter dropout changes depending on the input voltage, output-voltage, switching frequency, load current, and the efficiency of the design. The input voltage at which the devices enter dropout can be approximated as:

$$V_{SUP} = \frac{V_{OUT} + (I_{OUT} \times R_{ON\_H})}{0.98}$$

Note: The equation above does not take into account the efficiency and switching frequency, but is a good first-order approximation. Use the R_{ON_H} number from the max column in the *Electrical Characteristics* table.

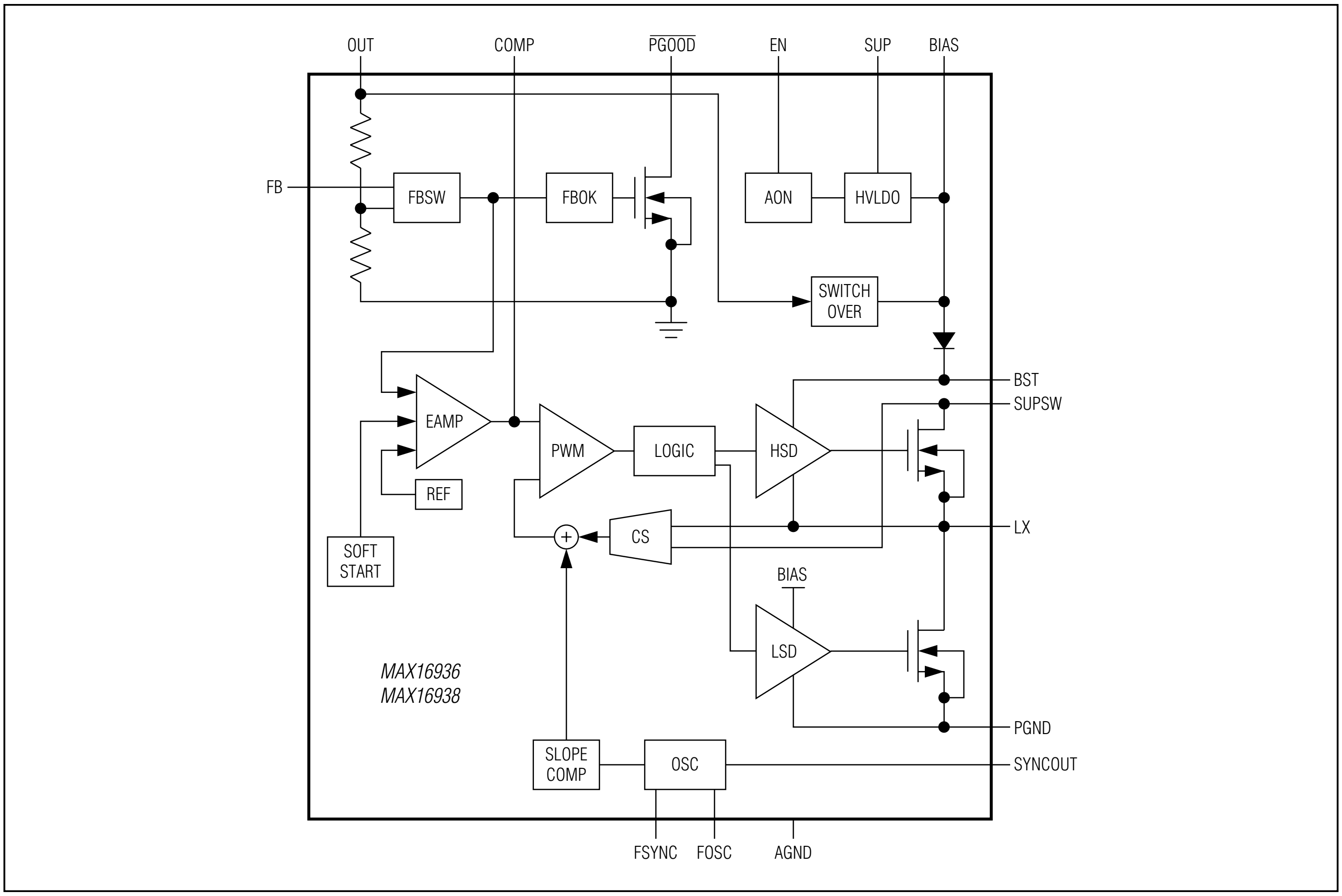


Figure 1. Internal Block Diagram

Linear Regulator Output (BIAS)

The devices include a 5V linear regulator (BIAS) that provides power to the internal circuit blocks. Connect a 1μF ceramic capacitor from BIAS to AGND. When the output voltage is set between 3V and 5.5V, the internal linear regulator only provides power until the output is in regulation. The internal linear regulator turns off once the output is in regulation and allows OUT to provide power to the device. The internal regulator turns back on once the external load on the output of the device is higher than 100mA. In addition, the linear regulator turns on anytime the output voltage is outside the 3V to 5.5V range.

Power-Good Output ($\overline{\text{PGOOD}}$)

The devices feature an open-drain power-good output, $\overline{\text{PGOOD}}$. $\overline{\text{PGOOD}}$ asserts when V_{OUT} rises above 95% of its regulation voltage. $\overline{\text{PGOOD}}$ deasserts when V_{OUT} drops below 92% of its regulation voltage. Connect $\overline{\text{PGOOD}}$ to BIAS with a 10kΩ resistor.

Overvoltage Protection (OVP)

If the output voltage reaches the OVP threshold, the high-side switch is forced off and the low-side switch is forced on until negative-current limit is reached. After negative-current limit is reached, both the high-side and low-side switches are turned off. The MAX16938 offers a lower voltage threshold for applications requiring tighter limits of protection.

Synchronization Input (FSYNC)

FSYNC is a logic-level input useful for operating mode selection and frequency control. Connecting FSYNC to BIAS or to an external clock enables fixed-frequency FPWM operation. Connecting FSYNC to AGND enables skip mode operation.

The external clock frequency at FSYNC can be higher or lower than the internal clock by 20%. Ensure the duty cycle of the external clock used has a minimum pulse width of 100ns. The device synchronizes to the external clock within one cycle. When the external clock signal at FSYNC is absent for more than two clock cycles, the device reverts back to the internal clock.

System Enable (EN)

An enable control input (EN) activates the device from its low-power shutdown mode. EN is compatible with inputs from automotive battery level down to 3.5V. The high voltage compatibility allows EN to be connected to SUP, KEY/KL30, or the inhibit pin (INH) of a CAN transceiver.

EN turns on the internal regulator. Once V_{BIAS} is above the internal lockout threshold, V_{UVL} = 3.15V (typ), the controller activates and the output voltage ramps up within 8ms.

A logic-low at EN shuts down the device. During shutdown, the internal linear regulator and gate drivers turn off. Shutdown is the lowest power state and reduces the quiescent current to 5μA (typ). Drive EN high to bring the device out of shutdown.

Spread-Spectrum Option

The devices have an internal spread-spectrum option to optimize EMI performance. This is factory set and the S-version of the device should be ordered. For spread-spectrum-enabled ICs, the operating frequency is varied ±6% centered on FOSC. The modulation signal is a triangular wave with a period of 110μs at 2.2MHz. Therefore, FOSC will ramp down 6% and back to 2.2MHz in 110μs and also ramp up 6% and back to 2.2MHz in 110μs. The cycle repeats.

For operations at FOSC values other than 2.2MHz, the modulation signal scales proportionally, e.g., at 400kHz, the 110μs modulation period increases to 110μs x 2.2MHz/400kHz = 605μs.

The internal spread spectrum is disabled if the device is synced to an external clock. However, the device does not filter the input clock and passes any modulation (including spread-spectrum) present on the driving external clock to the SYNCOUT pin.

Automatic Slew-Rate Control on LX

The devices have automatic slew-rate adjustment that optimizes the rise times on the internal HSFET gate drive to minimize EMI. The IC detects the internal clock frequency and adjusts the slew rate accordingly. When the user selects the external frequency setting resistor R_{FOSC} such that the frequency is > 1.1MHz, the HSFET is turned on in 4ns (typ). When the frequency is < 1.1MHz the HSFET is turned on in 8ns (typ). This slew-rate control optimizes the rise time on LX node externally to minimize EMI while maintaining good efficiency.

Internal Oscillator (FOSC)

The switching frequency (f_{SW}) is set by a resistor (R_{FOSC}) connected from FOSC to AGND. See Figure 3 to select the correct R_{FOSC} value for the desired switching frequency. For example, a 400kHz switching frequency is set with R_{FOSC} = 73.2kΩ. Higher frequencies allow designs with lower inductor values and less output capacitance. Consequently, peak currents and I^2R losses are lower at higher switching frequencies, but core losses, gate charge currents, and switching losses increase.

Synchronizing Output (SYNCOUT)

SYNCOUT is an open-drain output that outputs a 180° out-of-phase signal relative to the internal oscillator.

Overtemperature Protection

Thermal-overload protection limits the total power dissipation in the devices. When the junction temperature exceeds 175°C (typ), an internal thermal sensor shuts down the internal bias regulator and the step-down controller, allowing the device to cool. The thermal sensor turns on the device again after the junction temperature cools by 15°C.

Applications Information

Setting the Output Voltage

Connect FB to BIAS for a fixed +5V/+3.3 output voltage. To set the output to other voltages between 1V and 10V, connect a resistive divider from output (OUT) to FB to AGND (Figure 2). Use the following formula to determine the R_{FB2} of the resistive divider network:

$$R_{FB2} = R_{TOTAL} \times V_{FB}/V_{OUT}$$

where V_{FB} = 1V, R_{TOTAL} = selected total resistance of R_{FB1}, R_{FB2} in ω, and V_{OUT} is the desired output in volts.

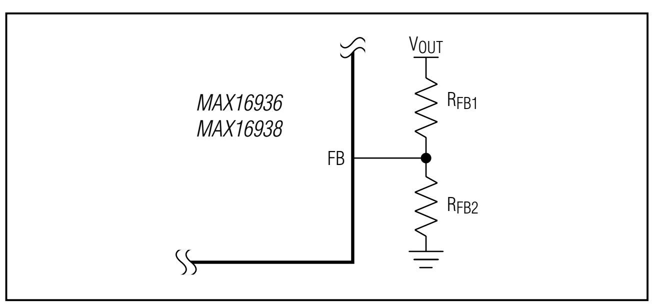


Figure 2. Adjustable Output-Voltage Setting

Calculate R_{FB1} (OUT to FB resistor) with the following equation:

$$R_{FB1} = R_{FB2}\left[\left(\frac{V_{OUT}}{V_{FB}}\right) - 1\right]$$

where V_{FB} = 1V (see the *Electrical Characteristics* table).

FPWM/Skip Modes

The MAX16936/MAX16938 offer a pin selectable skip mode or fixed-frequency PWM mode option. The IC has an internal LS MOSFET that turns on when the FSYNC pin is connected to V_{BIAS} or if there is a clock present on the FSYNC pin. This enables the fixed-frequency-forced PWM mode operation over the entire load range. This option allows the user to maintain fixed frequency over the entire load range in applications that require tight control on EMI. Even though the devices have an internal LS MOSFET for fixed-frequency operation, an external Schottky diode is still required to support the entire load range. If the FSYNC pin is connected to GND, the skip mode is enabled on the device.

In skip mode of operation, the converter's switching frequency is load dependent. At higher load current, the switching frequency does not change and the operating mode is similar to the FPWM mode. Skip mode helps improve efficiency in light-load applications by allowing the converters to turn on the high-side switch only when the output voltage falls below a set threshold. As such, the converters do not switch MOSFETs on and off as often as is the case in the FPWM mode. Consequently, the gate charge and switching losses are much lower in skip mode.

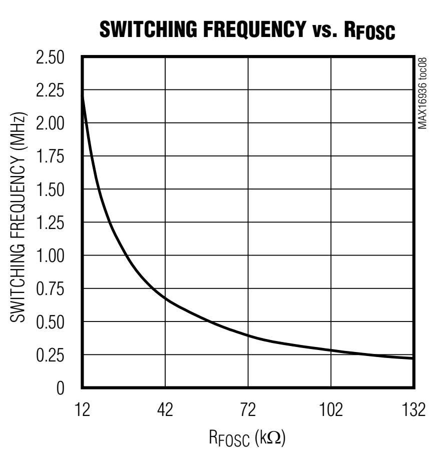


Figure 3. Switching Frequency vs. R_{FOSC}

Inductor Selection

Three key inductor parameters must be specified for operation with the devices: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). To select inductance value, the ratio of inductor peak-to-peak AC current to DC average current (LIR) must be selected first. A good compromise between size and loss is a 30% peak-to-peak ripple current to average current ratio (LIR = 0.3). The switching frequency, input voltage, output voltage, and selected LIR then determine the inductor value as follows:

$$L = \frac{V_{OUT}(V_{SUP} - V_{OUT})}{V_{SUP} f_{SW} I_{OUT} LIR}$$

where V_{SUP}, V_{OUT}, and I_{OUT} are typical values (so that efficiency is optimum for typical conditions). The switching frequency is set by R_{FOSC} (see Figure 3).

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching.

The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{LOAD(MAX)} \frac{\sqrt{V_{OUT}(V_{SUP} - V_{OUT})}}{V_{SUP}}$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage ($V_{SUP} = 2V_{OUT}$), so $I_{RMS(MAX)} = I_{LOAD(MAX)}/2$.

Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability.

The input voltage ripple is composed of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple current capability at the input. Assume the contribution from the ESR and capacitor discharge equal to 50%. Calculate the input capacitance and ESR required for a specified input voltage ripple using the following equations:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{OUT} + \frac{\Delta I_L}{2}}$$

where:

$$\Delta I_L = \frac{(V_{SUP} - V_{OUT}) \times V_{OUT}}{V_{SUP} \times f_{SW} \times L}$$

and:

$$C_{IN} = \frac{I_{OUT} \times D(1-D)}{\Delta V_Q \times f_{SW}} \text{ and } D = \frac{V_{OUT}}{V_{SUPSW}}$$

where I_{OUT} is the maximum output current and D is the duty cycle.

Output Capacitor

The output filter capacitor must have low enough ESR to meet output ripple and load transient requirements. The output capacitance must be high enough to absorb the inductor energy while transitioning from full-load to no-load conditions without tripping the overvoltage fault protection. When using high-capacitance, low-ESR capacitors, the filter capacitor's ESR dominates the output voltage ripple. So the size of the output capacitor depends on the maximum ESR required to meet the output-voltage ripple ($V_{RIPPLE(P-P)}$) specifications:

$$V_{RIPPLE(P-P)} = ESR \times I_{LOAD(MAX)} \times LIR$$

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value.

When using low-capacity filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent voltage droop and voltage rise from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem. However, low capacity filter capacitors typically have high ESR zeros that can affect the overall stability.

Rectifier Selection

The devices require an external Schottky diode rectifier as a freewheeling diode when they are is configured for skip-mode operation. Connect this rectifier close to the device using short leads and short PCB traces. In FPWM mode, the Schottky diode helps minimize efficiency losses by diverting the inductor current that would otherwise flow through the low-side MOSFET. Choose a rectifier with a voltage rating greater than the maximum expected input voltage, V_{SUPSW}. Use a low forward-voltage-drop Schottky rectifier to limit the negative voltage at LX. Avoid higher than necessary reverse-voltage Schottky rectifiers that have higher forward-voltage drops.

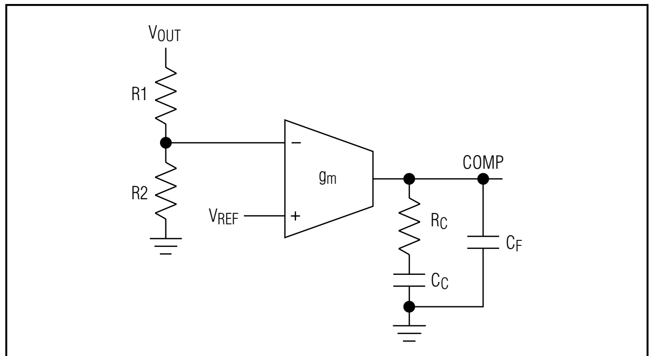


Figure 4. Compensation Network

Compensation Network

The devices use an internal transconductance error amplifier with its inverting input and its output available to the user for external frequency compensation. The output capacitor and compensation network determine the loop stability. The inductor and the output capacitor are chosen based on performance, size, and cost. Additionally, the compensation network optimizes the control-loop stability.

The controller uses a current-mode control scheme that regulates the output voltage by forcing the required current through the external inductor. The devices use the voltage drop across the high-side MOSFET to sense inductor current. Current-mode control eliminates the double pole in the feedback loop caused by the inductor and output capacitor, resulting in a smaller phase shift and requiring less elaborate error-amplifier compensation than voltage-mode control. Only a simple single-series resistor (R_C) and capacitor (C_C) are required to have a stable, high-bandwidth loop in applications where ceramic capacitors are used for output filtering (Figure 4). For other types of capacitors, due to the higher capacitance and ESR, the frequency of the zero created by the capacitance and ESR is lower than the desired closed-loop crossover frequency. To stabilize a nonceramic output capacitor loop, add another compensation capacitor (C_F) from COMP to GND to cancel this ESR zero.

The basic regulator loop is modeled as a power modulator, output feedback divider, and an error amplifier. The power modulator has a DC gain set by $g_m \times R_{LOAD}$, with a pole and zero pair set by R_{LOAD}, the output capacitor (C_{OUT}), and its ESR. The following equations allow to approximate the value for the gain of the power modulator ($GAIN_{MOD(dc)}$), neglecting the effect of the ramp stabilization. Ramp stabilization is necessary when the duty cycle is above 50% and is internally done for the device.

$$GAIN_{MOD(dc)} = g_m \times R_{LOAD}$$

where $R_{LOAD} = V_{OUT}/I_{LOUT(MAX)}$ in Ω and g_m = 3S.

In a current-mode step-down converter, the output capacitor, its ESR, and the load resistance introduce a pole at the following frequency:

$$f_{pMOD} = 1/(2\pi \times C_{OUT} \times R_{LOAD})$$

The output capacitor and its ESR also introduce a zero at:

$$f_{zMOD} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

When C_{OUT} is composed of “n” identical capacitors in parallel, the resulting C_{OUT} = n x $C_{OUT(EACH)}$, and ESR = $ESR_{(EACH)}$/n. Note that the capacitor zero for a parallel combination of alike capacitors is the same as for an individual capacitor.

The feedback voltage-divider has a gain of $GAIN_{FB} = V_{FB}/V_{OUT}$, where V_{FB} is 1V (typ). The transconductance error amplifier has a DC gain of $GAIN_{EA(dc)} = g_{m,EA} \times R_{OUT,EA}$, where $g_{m,EA}$ is the error amplifier transconductance, which is 700μS (typ), and $R_{OUT,EA}$ is the output resistance of the error amplifier 50MΩ.

A dominant pole (f_{dpEA}) is set by the compensation capacitor (C_C) and the amplifier output resistance ($R_{OUT,EA}$). A zero (f_{zEA}) is set by the compensation resistor (R_C) and the compensation capacitor (C_C). There is an optional pole (f_{pEA}) set by C_F and R_C to cancel the output capacitor ESR zero if it occurs near the cross over frequency (f_C, where the loop gain equals 1 (0dB)). Thus:

$$f_{dpEA} = \frac{1}{2\pi \times C_C \times (R_{OUT,EA} + R_C)}$$

$$f_{zEA} = \frac{1}{2\pi \times C_C \times R_C}$$

$$f_{pEA} = \frac{1}{2\pi \times C_F \times R_C}$$

The loop-gain crossover frequency (f_C) should be set below 1/5th of the switching frequency and much higher than the power-modulator pole (f_{pMOD}):

$$f_{pMOD} \ll f_C \leq \frac{f_{SW}}{5}$$

The total loop gain as the product of the modulator gain, the feedback voltage-divider gain, and the error amplifier gain at f_C should be equal to 1. So:

$$GAIN_{MOD(fC)} \times \frac{V_{FB}}{V_{OUT}} \times GAIN_{EA(fC)} = 1$$

$$GAIN_{EA(fC)} = g_{m,EA} \times R_C$$

$$GAIN_{MOD(fC)} = GAIN_{MOD(dc)} \times \frac{f_{pMOD}}{f_C}$$

Therefore:

$$GAIN_{MOD(fC)} \times \frac{V_{FB}}{V_{OUT}} \times g_{m,EA} \times R_C = 1$$

Solving for R_C:

$$R_C = \frac{V_{OUT}}{g_{m,EA} \times V_{FB} \times GAIN_{MOD(fC)}}$$

Set the error-amplifier compensation zero formed by R_C and C_C (f_{zEA}) at the f_{pMOD}. Calculate the value of C_C a follows:

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C}$$

If f_{zMOD} is less than 5 x f_C, add a second capacitor, C_F, from COMP to GND and set the compensation pole formed by R_C and C_F (f_{pEA}) at the f_{zMOD}. Calculate the value of C_F as follows:

$$C_F = \frac{1}{2\pi \times f_{zMOD} \times R_C}$$

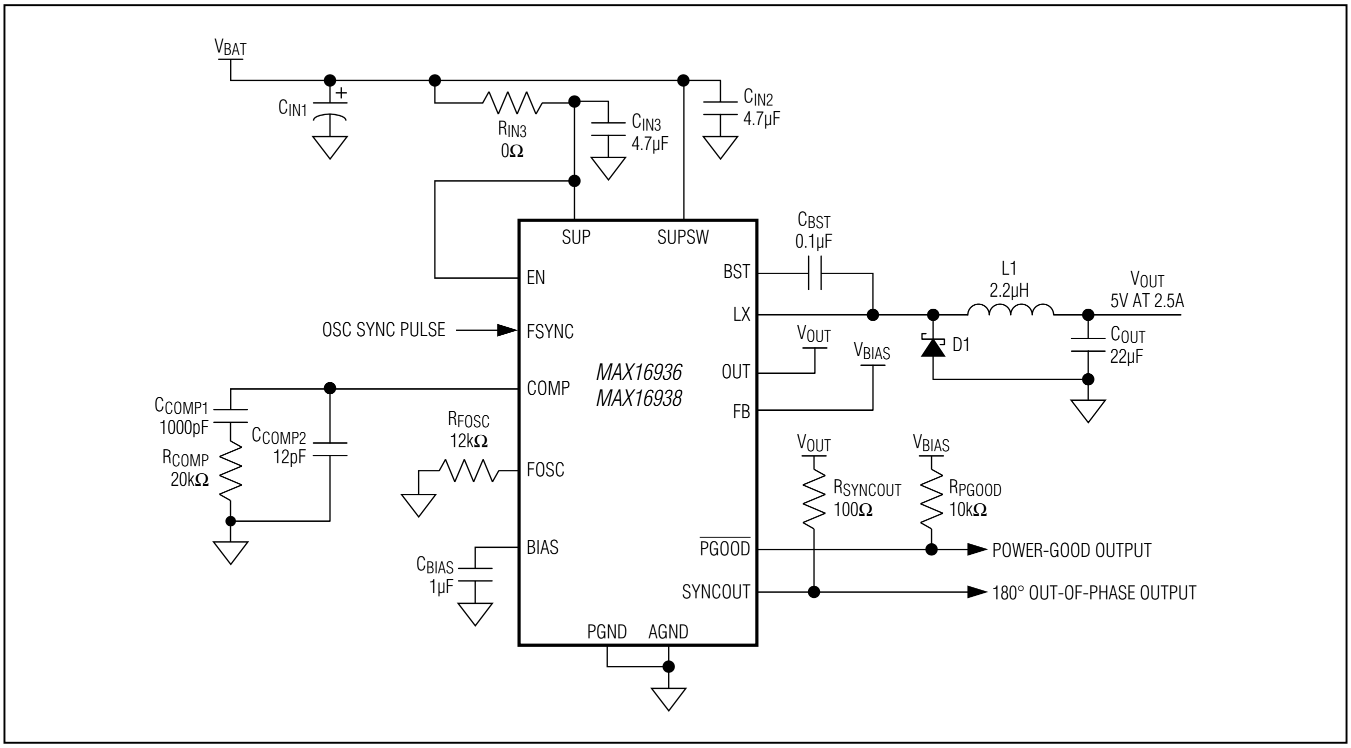
As the load current decreases, the modulator pole also decreases; however, the modulator gain increases accordingly and the crossover frequency remains the same.

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. Follow these guidelines for good PCB layout:

1) Use a large contiguous copper plane under the IC package. Ensure that all heat-dissipating components have adequate cooling. The bottom pad of the IC must be soldered down to this copper plane for effective heat dissipation and for getting the full power out of the IC. Use multiple vias or a single large via in this plane for heat dissipation.
2) Isolate the power components and high current path from the sensitive analog circuitry. Doing so is essential to prevent any noise coupling into the analog signals. Implementing an RC filter on the SUP pin decreases switching noise from entering the logic supply. Refer to the MAX16936 EV kit data sheet for details on filter configuration and PCB layout for the SUP and SUPSW input capacitors. Do not route the OUT or feedback signal next to the inductor. Make sure components used on FOSC, COMP, and BIAS are connected to analog ground.
3) Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. The high-current path composed of the input capacitor, high-side FET, inductor, and the output capacitor should be as short as possible.
4) Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PCBs (2oz vs. 1oz) to enhance full-load efficiency.
5) The analog signal lines should be routed away from the high-frequency planes. Doing so ensures integrity of sensitive signals feeding back into the IC.
6) The ground connection for the analog and power section should be close to the IC. This keeps the ground current loops to a minimum. In cases where only one ground is used, enough isolation between analog return signals and high power signals must be maintained.

Typical Application Circuit



Ordering Information/Selector Guide

PART	V_{OUT} ADJUSTABLE (FB CONNECTED TO RESISTIVE DIVIDER) (V)	V_{OUT} FIXED (FB CONNECTED TO BIAS) (V)	SPREAD SPECTRUM	TEMP RANGE	PIN-PACKAGE
MAX16936RAUEA/V+	1 to 10	5	Off	-40°C to +125°C	16 TSSOP-EP*
MAX16936RAUEB/V+	1 to 10	3.3	Off	-40°C to +125°C	16 TSSOP-EP*
MAX16936SAUEA/V+	1 to 10	5	On	-40°C to +125°C	16 TSSOP-EP*
MAX16936SAUEB/V+	1 to 10	3.3	On	-40°C to +125°C	16 TSSOP-EP*
MAX16936RATEA/V+	1 to 10	5	Off	-40°C to +125°C	16 TQFN-EP*
MAX16936RATEB/V+	1 to 10	3.3	Off	-40°C to +125°C	16 TQFN-EP*
MAX16936SATEA/V+	1 to 10	5	On	-40°C to +125°C	16 TQFN-EP*
MAX16936SATEB/V+	1 to 10	3.3	On	-40°C to +125°C	16 TQFN-EP*
MAX16938AUERA/V+**	1 to 10	5	Off	-40°C to +125°C	16 TSSOP-EP*
MAX16938AUERB/V+**	1 to 10	3.3	Off	-40°C to +125°C	16 TSSOP-EP*
MAX16938AUESA/V+**	1 to 10	5	On	-40°C to +125°C	16 TSSOP-EP*
MAX16938AUESB/V+**	1 to 10	3.3	On	-40°C to +125°C	16 TSSOP-EP*
MAX16938ATERA/V+	1 to 10	5	Off	-40°C to +125°C	16 TQFN-EP*
MAX16938ATERB/V+	1 to 10	3.3	Off	-40°C to +125°C	16 TQFN-EP*
MAX16938ATESA/V+	1 to 10	5	On	-40°C to +125°C	16 TQFN-EP*
MAX16938ATESB/V+	1 to 10	3.3	On	-40°C to +125°C	16 TQFN-EP*

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
***Future product—contact factory for availability.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TSSOP-EP	U16E+3	**21-0108**	**90-0120**
16 TQFN-EP	T1655+4	**21-0140**	**90-0121**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/13	Initial release	—
1	4/13	Added non-automotive OPNs to *Ordering Information/Selector Guide*	16
2	8/13	Updated FPWM and Skip Mode output voltages in *Electrical Characteristics*, *Internal Oscillator (FOSC)* and *Compensation Network* sections, and removed the non-automotive parts from the *Ordering Information/Selector Guide*	2, 3, 11, 13, 16
3	11/13	Removed future product references from the *Ordering Information/Selector Guide*	16
4	2/14	Changed the BST capacitor value from 0.22μF to 0.1μF in *Pin Descriptions* and *Typical Application Circuit*; updated the *Linear Regulator Output (BIAS)* section	8, 9, 15
5	3/14	Added lead-free designation to TQFN package code	16
6	1/15	Updated SUP pin in *Pin Descriptions* table, added *Maximum Duty-Cycle Operation* section, updated guideline #2 in *PCB Layout Guidelines* section, and added an RC filter in the *Typical Application Circuit*	9, 14, 15
7	2/15	Updated the *Benefits and Features* section	1
8	3/15	Added new Note 1 to *Absolute Maximum Ratings* and renumbered the remaining notes in *Package Thermal Characteristics* section and *Electrical Characteristics*	2–4
9	6/15	Added the MAX16938 to data sheet as a future product	1–17
10	6/15	Corrected MAX16938 variants in *Ordering Information/Selector Guide*	16
11	7/15	Corrected typo in *Pin Configurations* diagram; corrected exposed pad and future product designations and corrected typo in *Ordering Information/Selector Guide*	8,16
12	3/16	Updated 3rd sub-bullet under 1st main bullet in *Benefits and Features* section (changed Accuracy (5V) to (5V/3.3V)	1
13	4/16	Added new bullet in *Benefits and Features* section; removed future product references	1, 16
14	6/16	Changed part number from MAX16939 to MAX16938 in last bullet in *Benefits and Features* section	1
15	1/17	Added 3.3V option for Supply Current and changed maximum Skip-Mode Output Voltage from 3.34V to 3.4V in *Electrical Characteristics* table	2, 3
16	7/17	Added a new Note 3 in/after *Electrical Characteristics* table and renumbered the remaining four notes accordingly	2, 4
17	10/17	Deleted Note 3 in/after *Electrical Characteristics* table and renumbered the remaining four notes accordingly	2, 4
18	3/18	Changed AGND to PGND for LX pin in the *Pin Descriptions* table	9

