19-0837; Rev 0; 6/07

EVALUATION KIT AVAILABLE

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

General Description

The MAX17003A/MAX17004A are dual step-down, switch-mode, power-supply (SMPS) controllers with synchronous rectification, intended for main 5V/3.3V power generation in battery-powered systems. Fixed-frequency operation with optimal interleaving minimizes input ripple current from the lowest input voltages up to the 26V maximum input. Optimal 40/60 interleaving allows the input voltage to go down to 8.3V before duty-cycle overlap occurs, compared to 180° out-of-phase regulators where the duty-cycle overlap occurs when the input drops below 10V.

Output current sensing provides peak current-limit protection, using either an accurate sense resistor or using lossless inductor DCR current sensing. A low-noise mode maintains high light-load efficiency while keeping the switching frequency out of the audible range.

An internal, fixed 5V, 100mA linear regulator powers up the MAX17003A/MAX17004A and their gate drivers, as well as external keep-alive loads. When the main PWM regulator is in regulation, an automatic bootstrap switch bypasses the internal linear regulator, providing current up to 200mA. An additional adjustable linear-regulator driver with an external pnp transistor can be used with a secondary winding to provide a 12V supply, or powered directly from the main outputs to generate low-voltage outputs as low as 1V.

Independent enable controls and power-good signals allow flexible power sequencing. Voltage soft-start gradually ramps up the output voltage and reduces inrush current, while soft-discharge gradually decrease the output voltage, preventing negative voltage dips. The MAX17003A/MAX17004A feature output undervoltage and thermal-fault protection. The MAX17003A also includes output overvoltage-fault protection.

The MAX17003A/MAX17004A are available in a 32-pin, 5mm x 5mm thin QFN package. The exposed backside pad improves thermal characteristics for demanding linear keep-alive applications.

Applications

Main Power Supplies

2 to 4 Li+ Cell Battery-Powered Devices

Notebook and Subnotebook Computers

PDAs and Mobile Communicators

Dual Mode is a trademark of Maxim Integrated Products, Inc.

Features

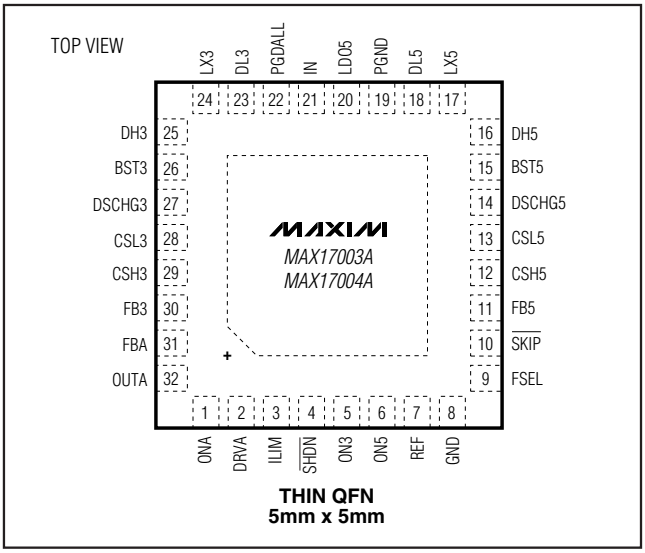
- **Fixed-Frequency, Current-Mode Control**
- **40/60 Optimal Interleaving**
- **Internal BST Switches**
- **Internal 5V, 100mA Linear Regulator**
- **Auxiliary Linear-Regulator Driver (12V or Adjustable Down to 1V)**
- **Dual Mode™ Feedback—3.3V/5V Fixed or Adjustable Output Voltages**
- **200kHz/300kHz/500kHz Switching Frequency**
- **Undervoltage and Thermal-Fault Protection**
- **Overvoltage-Fault Protection (MAX17003A Only)**
- **6V to 26V Input Range**
- **2V ±0.75% Reference Output**
- **Independent Enable Inputs and Power-Good Outputs**
- **Soft-Start and Soft-Discharge (Voltage Ramp)**
- **8µA (typ) Shutdown Current**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX17003AETJ+	-40°C to +85°C	32 Thin QFN (5mm x 5mm)	T3255-4
MAX17004AETJ+	-40°C to +85°C	32 Thin QFN (5mm x 5mm)	T3255-4

+Denotes a lead-free package.

Pin Configuration



THIN QFN 5mm x 5mm

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

ABSOLUTE MAXIMUM RATINGS

IN, $\overline{SHDN}$, DRVA, OUTA to GND .....-0.3V to +28V
LDO5, ON3, ON5, ONA to GND .....-0.3V to +6V
PGDALL, DSCHG3, DSCHG5 to GND .....-0.3V to +6V
CSL3, CSH3, CSL5, CSH5 to GND .....-0.3V to +6V
REF, FB3, FB5, FBA to GND .....-0.3V to (V_{LDO5} + 0.3V)
$\overline{SKIP}$, FSEL, ILIM to GND .....-0.3V to (V_{LDO5} + 0.3V)
DL3, DL5 to PGND .....-0.3V to (V_{LDO5} + 0.3V)
BST3, BST5 to PGND .....-0.3V to +34V
BST3 to LX3 .....-0.3V to +6V
DH3 to LX3 .....-0.3V to (V_{BST3} + 0.3V)
BST5 to LX5 .....-0.3V to +6V
DH5 to LX5 .....-0.3V to (V_{BST5} + 0.3V)
GND to PGND .....-0.3V to +0.3V
BST3, BST5 to LDO5 .....-0.3V to +0.3V
LDO Short Circuit to GND .....Momentary
REF Short Circuit to GND .....Momentary
DRVA Current (sinking) 30mA
OUTA Shunt Current 30mA
Continuous Power Dissipation (T_A = +70°C)
Multilayer PCB
32-Pin, 5mm x 5mm TQFN
(derated 34.5mW/°C above +70°C) 2459mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = 12V, both SMPS enabled, FSEL = REF, $\overline{SKIP}$ = GND, ILIM = LDO5, FBA = LDO5, I_{REF} = I_{LDO5} = I_{OUTA} = no load, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLIES (Note 1)						
V_{IN} Input Voltage Range	V_{IN}	LDO5 in regulation	5.4		26.0	V
		IN = LDO5, V_{CSL5} < 4.4V	4.5		5.5	
V_{IN} Operating Supply Current	I_{IN}	LDO5 switched over to CSL5, either SMPS on		20	36	µA
V_{IN} Standby Supply Current	$I_{IN(STBY)}$	V_{IN} = 6V to 26V, both SMPS off, includes $I_{\overline{SHDN}}$		65	120	µA
V_{IN} Shutdown Supply Current	$I_{IN(SHDN)}$	V_{IN} = 6V to 26V		8	20	µA
Quiescent Power Consumption	P_Q	Both SMPS on, FB3 = FB5 = LDO5, $\overline{SKIP}$ = GND, V_{CSL3} = 3.5V, V_{CSL5} = 5.3V, V_{OUTA} = 15V, $P_{IN} + P_{CSL3} + P_{CSL5} + P_{OUTA}$		3.5	4.5	mW
MAIN SMPS CONTROLLERS						
3.3V Output Voltage in Fixed Mode	V_{OUT3}	V_{IN} = 6V to 26V, $\overline{SKIP}$ = FB3 = LDO5, 0 < V_{CSH3} - V_{CSL3} < 50mV (Note 2)	3.265	3.315	3.365	V
5V Output Voltage in Fixed Mode	V_{OUT5}	V_{IN} = 6V to 26V, $\overline{SKIP}$ = FB5 = LDO5, 0 < V_{CSH5} - V_{CSL5} < 50mV (Note 2)	4.94	5.015	5.09	V
Feedback Voltage in Adjustable Mode (Note 2)	$V_{FB\_}$	V_{IN} = 6V to 26V, FB3 or FB5 duty factor = 20% to 80%	1.980	2.010	2.040	V
		V_{IN} = 6V to 26V, FB3 or FB5 duty factor = 50%	1.990	2.010	2.030	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, both SMPS enabled, FSEL = REF, $\overline{SKIP}$ = GND, ILIM = LDO5, FBA = LDO5, I_{REF} = I_{LDO5} = I_{OUTA} = no load, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Adjust Range		Either SMPS		2.0		5.5	V
FB3, FB5 Dual Mode Threshold				3.0	V_{LOO5} - 1.0	V_{LOO5} - 0.4	V
Feedback Input Leakage Current		V_{FB3} = V_{FB5} = 2.1V		-0.1		+0.1	µA
DC Load Regulation		Either SMPS, $\overline{SKIP}$ = LDO5, 0 < $V_{CSH\_}$ - V_{CSL} < 50mV			-0.1		%
Line Regulation Error		Either SMPS, 6V < V_{IN} < 26V			0.03		%/V
Operating Frequency (Note 1)	f_{OSC}	FSEL = GND		170	200	230	kHz
		FSEL = REF		270	300	330	
		FSEL = LDO5		425	500	575	
Maximum Duty Factor	D_{MAX}	(Note 1)		97.5	99		%
Minimum On-Time	t_{ONMIN}				100		ns
SMPS3-to-SMPS5 Phase Shift		SMPS5 starts after SMPS3			40		%
					144		Degrees
CURRENT LIMIT							
ILIM Adjustment Range				0.5		V_{REF}	V
Current-Sense Input Leakage Current		CSH3 = CSH5 = GND or LDO5		-1		+1	µA
Current-Limit Threshold (Fixed)	V_{LIMIT}	$V_{CSH\_}$ - $V_{CSL\_}$, ILIM = LDO5		45	50	55	mV
Current-Limit Threshold (Adjustable)	V_{LIMIT}	$V_{CSH\_}$ - $V_{CSL\_}$	V_{ILIM} = 2.00V	185	200	215	mV
			V_{ILIM} = 1.00V	94	100	106	
Current-Limit Threshold (Negative)	V_{NEG}	$V_{CSH\_}$ - $V_{CSL\_}$, $\overline{SKIP}$ = ILIM = LDO5		-67	-60	-53	mV
		$V_{CSH\_}$ - $V_{CSL\_}$, $\overline{SKIP}$ = LDO5, adjustable mode, percent of current limit			-120		%
Current-Limit Threshold (Zero Crossing)	V_{ZX}	$V_{CSH\_}$ - $V_{CSL\_}$, $\overline{SKIP}$ = GND, ILIM = LDO5		0	3	6	mV
Idle Mode™ Threshold	V_{IDLE}	$V_{CSH\_}$ - $V_{CSL\_}$, $\overline{SKIP}$ = GND	ILIM = LDO5	6	10	14	mV
			With respect to current-limit threshold (V_{LIMIT})		20		%
Idle Mode Threshold (Low Audible-Noise Mode)	V_{IDLE}	$V_{CSH\_}$ - $V_{CSL\_}$, $\overline{SKIP}$ = REF	ILIM = LDO5	2.5	5	7.5	mV
			With respect to current-limit threshold (V_{LIMIT})		10		%
ILIM Leakage Current		ILIM = GND or REF		-1		+1	µA
Soft-Start Ramp Time	t_{SSTART}	Measured from the rising edge of ON_ to full scale			2		ms

Idle Mode is a trademark of Maxim Integrated Products, Inc.

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, both SMPS enabled, FSEL = REF, $\overline{SKIP}$ = GND, ILIM = LDO5, FBA = LDO5, I_{REF} = I_{LDO5} = I_{OUTA} = no load, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INTERNAL FIXED LINEAR REGULATORS						
LDO5 Output Voltage	V_{LDO5}	ON5 = GND, 6V < V_{IN} < 26V, 0 < I_{LDO5} < 100mA	4.85	4.95	5.10	V
LDO5 Undervoltage-Lockout Fault		Rising edge, hysteresis = 1%	3.7	4.0	4.1	mA
Short-Circuit Current (Switched over to CSL5)		LDO5 = GND, V_{CSL5} > 4.7V	200	425		mA
AUXILIARY LINEAR REGULATOR						
DRVA Voltage Range	V_{DRVA}		0.5		26.0	V
DRVA Drive Current		V_{FBA} = 1.05V, V_{DRVA} = 5V			0.4	mA
		V_{FBA} = 0.965V, V_{DRVA} = 5V	10			
FBA Regulation Threshold	V_{FBA}	V_{DRVA} = 5V, I_{DRVA} = 1mA (sink)	0.98	1.00	1.02	V
FBA Load Regulation		V_{DRA} = 5V, I_{DRVA} = 0.5mA to 5mA		-1.2	-2.2	%
OUTA Shunt Trip Level		Rising edge	25	26	27	V
FBA Leakage Current		V_{FBA} = 1.035V	0.1		+0.1	µA
Secondary Feedback-Regulation Threshold		V_{DRVA} - V_{OUTA}		0		V
DL5 Pulse Width				1/3/f_{OSC}		µs
OUTA Leakage Current	I_{OUTA}	V_{DRVA} = V_{OUTA} = 25V			50	µA
REFERENCE (REF)						
Reference Voltage	V_{REF}	LDO5 in regulation, I_{REF} = 0	1.985	2.00	2.015	V
Reference Load-Regulation Error	ΔV_{REF}	I_{REF} = -5µA to +50µA	-10		+10	mV
REF Lockout Voltage	$V_{REF(UVLO)}$	Rising edge		1.8		V
FAULT DETECTION						
Output Overvoltage Trip Threshold (MAX17003A Only)		With respect to error-comparator threshold	8	11	14	%
Output Overvoltage Fault Propagation Delay (MAX17003A Only)	t_{OVP}	50mV overdrive		10		µs
Output Undervoltage Protection Trip Threshold		With respect to error-comparator threshold	65	70	75	%
Output Undevoltage Fault Propagation Delay	t_{UVP}	50mV overdrive		10		µs
Output Undervoltage Protection Blanking Time	t_{BLANK}	From rising edge of ON_ with respect to f_{SW}	5000	6144	7000	1/f_{OSC}

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, both SMPS enabled, FSEL = REF, $\overline{SKIP}$ = GND, ILIM = LDO5, FBA = LDO5, I_{REF} = I_{LDO5} = I_{OUTA} = no load, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PGDALL Lower Trip Threshold		With respect to either SMPS error-comparator threshold, hysteresis = 1% (typ)		-12	-10	-8	%
PGDALL Propagation Delay	t_{PGDALL}	Falling edge, 50mV overdrive			10		µs
		Rising edge, 50mV overdrive			1		
PGDALL Output Low Voltage		I_{SINK} = 1mA				0.4	V
PGDALL Leakage Current	I_{PGDALL}	High state, PGDALL forced to 5.5V				1	µA
Thermal-Shutdown Threshold	$t_{\overline{SHDN}}$	Hysteresis = 15°C			+160		°C
GATE DRIVERS							
DH_ Gate-Driver On-Resistance	R_{DH}	BST_ - LX_ forced to 5V			1.3	5	Ω
DL_ Gate-Driver On-Resistance	R_{DL}	DL_, high state			1.7	5	Ω
		DL_, low state			0.6	3	
DH_ Gate-Driver Source/Sink Current	I_{DH}	DH_ forced to 2.5V, BST_ - LX_ forced to 5V			2		A
DL_ Gate-Driver Source Current	I_{DL}	DL_ forced to 2.5V			1.7		A
DL_ Gate-Driver Sink Current	$I_{DL (SINK)}$	DL_ forced to 2.5V			3.3		A
Dead Time	t_{DEAD}	DH_ low to DL_ high		15	45		ns
		DL_ low to DH_ high		15	44		
Internal BST_ Switch On-Resistance	R_{BST}	I_{BST} = 10mA			5		Ω
BST_ Leakage Current		$V_{BST\_}$ = 26V			2	20	µA
INPUTS AND OUTPUTS							
$\overline{SHDN}$ Input Trip Level		Rising trip level		1.1	1.6	2.2	V
		Falling trip level		0.96	1	1.04	
ONA Logic Input Voltage		Hysteresis = 600mV (typ)	High	2.4			V
			Low			0.8	
ON3, ON5 Input Voltage		SMPS off level/clear fault level				0.8	V
		Delay start level		1.9		2.1	
		SMPS on level		2.4			
DSCHG_ Output Low Voltage		I_{SINK} = 1mA				0.4	V
DSCHG_ Leakage Current		High state, DSCHG_ forced to 5.5V				1	µA
Tri-Level Input Logic		$\overline{SKIP}$, FSEL	High	V_{LDO5} - 0.4			V
			REF	1.65		2.35	
			GND			0.5	
Input Leakage Current		$\overline{SKIP}$, FSEL forced to GND or LDO5		-1		+1	µA
		$\overline{SHDN}$ forced to GND or 26V		-1		+1	

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = 12V, both SMPS enabled, FSEL = REF, $\overline{SKIP}$ = GND, ILIM = LDO5, FBA = LDO5, I_{REF} = I_{LDO5} = I_{OUTA} = no load, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
INPUT SUPPLIES (Note 1)						
V_{IN} Input Voltage Range	V_{IN}	LDO5 in regulation		5.4	26.0	V
		IN = LDO5, V_{CSL5} < 4.4V		4.5	5.5	
V_{IN} Operating Supply Current	I_{IN}	LDO5 switched over to CSL5, either SMPS on			40	µA
V_{IN} Standby Supply Current	$I_{IN(STBY)}$	V_{IN} = 6V to 26V, both SMPS off, includes $I_{\overline{SHDN}}$			120	µA
V_{IN} Shutdown Supply Current	$I_{IN(SHDN)}$	V_{IN} = 6V to 26V			20	µA
Quiescent Power Consumption	P_Q	Both SMPS on, FB3 = FB5 = LDO5; $\overline{SKIP}$ = GND, V_{CSL3} = 3.5V, V_{CSL5} = 5.3V, V_{OUTA} = 15V, P_{IN} + P_{CSL3} + P_{CSL5} + P_{OUTA}			4.5	mW
MAIN SMPS CONTROLLERS						
3.3V Output Voltage in Fixed Mode	V_{OUT3}	V_{IN} = 6V to 26V, $\overline{SKIP}$ = FB3 = LDO5, 0 < V_{CSH3} - V_{CSL3} < 50mV (Note 2)		3.255	3.375	V
5V Output Voltage in Fixed Mode	V_{OUT5}	V_{IN} = 6V to 26V, $\overline{SKIP}$ = FB5 = LDO5, 0 < V_{CSH5} - V_{CSL5} < 50mV (Note 2)		4.925	5.105	V
Feedback Voltage in Adjustable Mode	$V_{FB\_}$	V_{IN} = 6V to 26V, FB3 or FB5 duty factor = 20% to 80% (Note 2)		1.974	2.046	V
Output Voltage-Adjust Range		Either SMPS		2.0	5.5	V
FB3, FB5 Dual Mode Threshold				3V	V_{LDO5} - 0.4	V
Operating Frequency (Note 1)	f_{OSC}	FSEL = GND		170	230	kHz
		FSEL = REF		270	330	
		FSEL = LDO5		425	575	
Maximum Duty Factor	D_{MAX}			97		%
CURRENT LIMIT						
ILIM Adjustment Range				0.5	V_{REF}	V
Current-Limit Threshold (Fixed)	V_{LIMIT}	$V_{CSH\_}$ - $V_{CSL\_}$, ILIM = LDO5		44	56	mV
Current-Limit Threshold (Adjustable)	V_{LIMIT}	$V_{CSH\_}$ - $V_{CSL\_}$	V_{ILIM} = 2.00V	185	215	mV
			V_{ILIM} = 1.00V	93	107	
INTERNAL FIXED LINEAR REGULATORS						
LDO5 Output Voltage	V_{LDO5}	ON5 = GND, 6V < V_{IN} < 26V, 0 < I_{LDO5} < 100mA		4.85	5.10	V
LDO5 Undervoltage-Lockout Fault Threshold		Rising edge, hysteresis = 1% (typ)		3.7	4.1	V
LDO5 Bootstrap Switch		Rising edge of CSL5, hysteresis = 1% (typ)		4.30	4.75	V
Short-Circuit Current		LDO5 = GND, ON5 = GND			450	mA
Short-Circuit Current (Switched over to CSL5)		LDO5 = GND, V_{CSL5} > 4.7V		200		mA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, both SMPS enabled, FSEL = REF, $\overline{SKIP}$ = GND, ILIM = LDO5, FBA = LDO5, I_{REF} = I_{LDO5} = I_{OUTA} = no load, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
AUXILIARY LINEAR REGULATOR						
DRVA Voltage Range	V_{DRVA}			0.5	26.0	V
DRVA Drive Current		V_{FBA} = 1.05V, V_{DRVA} = 5V			0.4	mA
		V_{FBA} = 0.965V, V_{DRVA} = 5V		10		
FBA Regulation Threshold	V_{FBA}	V_{DRVA} = 5V, I_{DRVA} = 1mA (sink)		0.98	1.02	V
OUTA Shunt Trip Level				25	27	V
REFERENCE (REF)						
Reference Voltage	V_{REF}	LDO5 in regulation, I_{REF} = 0		1.980	2.020	V
FAULT DETECTION						
Output Overvoltage Trip Threshold (MAX17003A Only)		With respect to error comparator threshold		8	14	%
Output Undervoltage Protection		With respect to error comparator threshold		65	75	%
PGDALL Lower Trip Threshold		With respect to error comparator threshold, hysteresis = 1%		-12	-8	%
PGDALL Output Low Voltage		I_{SINK} = 1mA			0.4	V
GATE DRIVERS						
DH_ Gate-Driver On-Resistance	R_{DH}	BST_ - LX_ forced to 5V			5	Ω
DL_ Gate-Driver On-Resistance	R_{DL}	DL_, high state			5	Ω
		DL_, low state			3	
INPUTS AND OUTPUTS						
$\overline{SHDN}$ Input Trip Level		Rising trip level		1.0	2.3	V
		Falling trip level		0.96	1.04	
ONA Logic Input Voltage		Hysteresis = 600mV	High	2.4		V
			Low		0.8	
ON3, ON5 Input Voltage		SMPS off level/clear fault level			0.8	V
		Delay start level		1.9	2.1	
		SMPS on level		2.4		
DSCHG_ Output Low Voltage		I_{SINK} = 1mA			0.4	V
Tri-Level Input Logic		$\overline{SKIP}$, FSEL	High	V_{LDO5} - 0.4		V
			REF	1.65	2.35	
			GND		0.5	

Note 1: The MAX17003A/MAX17004A cannot operate over all combinations of frequency, input voltage (V_{IN}), and output voltage. For large input-to-output differentials and high switching-frequency settings, the required on-time may be too short to maintain the regulation specifications. Under these conditions, a lower operating frequency must be selected. The minimum on-time must be greater than 150ns, regardless of the selected switching frequency. On-time and off-time specifications are measured from 50% point to 50% point at the DH_ pin with LX_ = GND, $V_{BST\_}$ = 5V, and a 250pF capacitor connected from DH_ to LX_. Actual in-circuit times may differ due to MOSFET switching speeds.

Note 2: When the inductor is in continuous conduction, the output voltage has a DC-regulation level lower than the error-comparator threshold by 50% of the ripple. In discontinuous conduction ($\overline{SKIP}$ = GND, light load), the output voltage has a DC regulation level higher than the trip level by approximately 1.1% due to slope compensation.

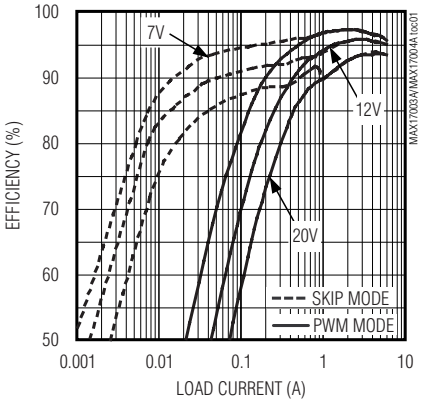
Note 3: Specifications from -40°C to +85°C are guaranteed by design, not production tested.

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

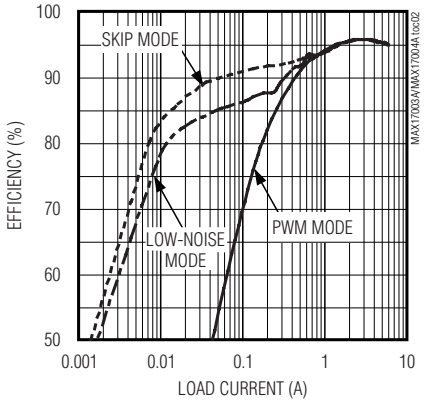
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = 12V, $\overline{SKIP}$ = GND, FSEL = REF, T_A = +25°C, unless otherwise noted.)

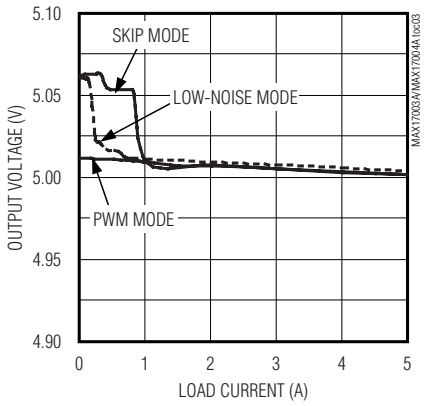
5V OUTPUT EFFICIENCY vs. LOAD CURRENT



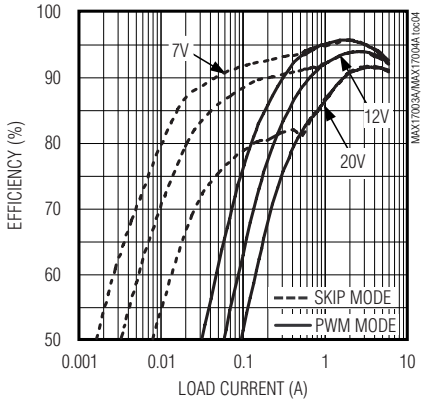
5V OUTPUT EFFICIENCY vs. LOAD CURRENT



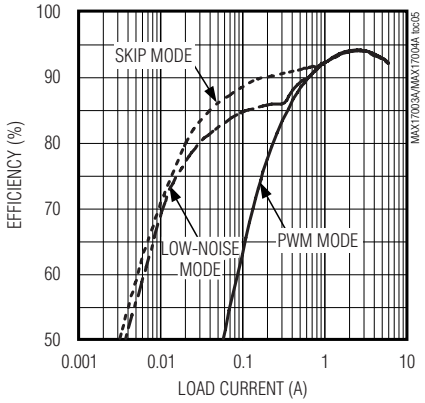
5V OUTPUT VOLTAGE vs. LOAD CURRENT



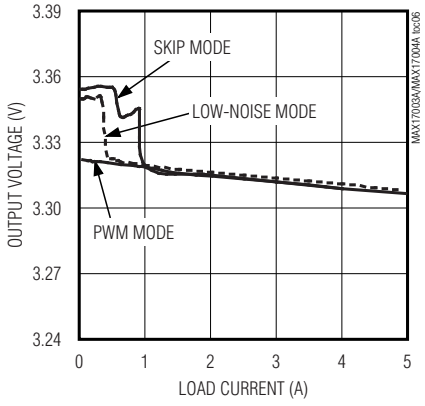
3.3V OUTPUT EFFICIENCY vs. LOAD CURRENT



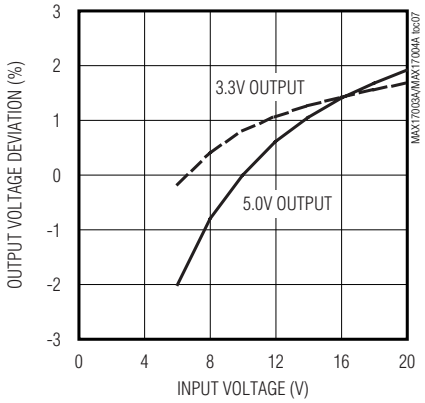
3.3V OUTPUT EFFICIENCY vs. LOAD CURRENT



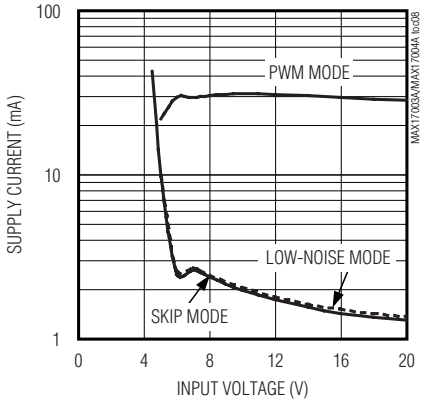
3.3V OUTPUT VOLTAGE vs. LOAD CURRENT



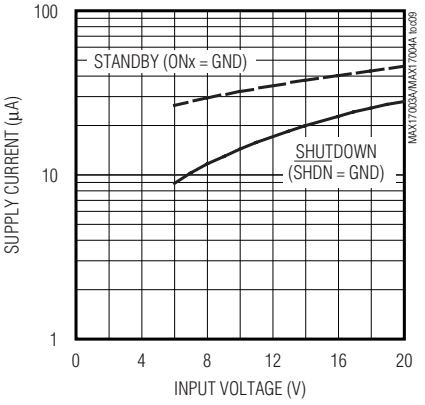
OUTPUT VOLTAGE DEVIATION vs. INPUT VOLTAGE



NO-LOAD INPUT SUPPLY CURRENT vs. INPUT VOLTAGE



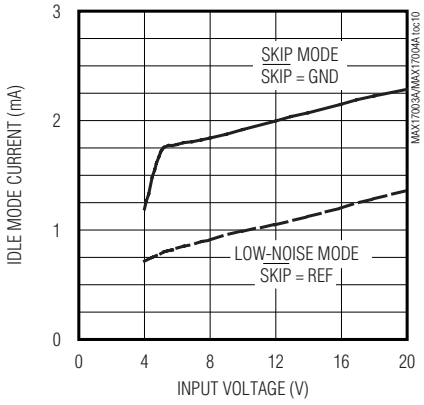
STANDBY AND SHUTDOWN INPUT CURRENT vs. INPUT VOLTAGE



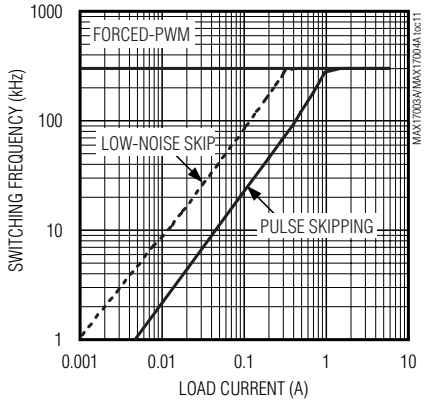
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 12V, $\overline{SKIP}$ = GND, FSEL = REF, T_A = +25°C, unless otherwise noted.)

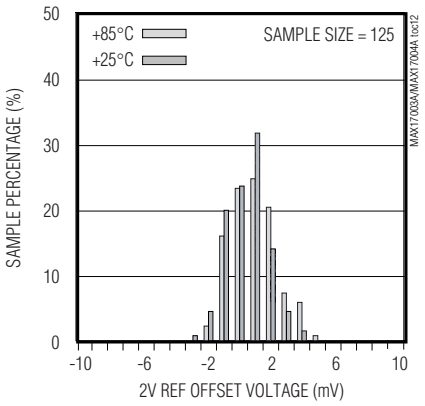
3.3V IDLE MODE CURRENT vs. INPUT VOLTAGE



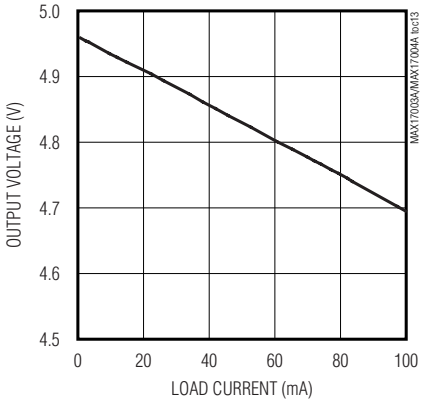
3.3V SWITCHING FREQUENCY vs. LOAD CURRENT



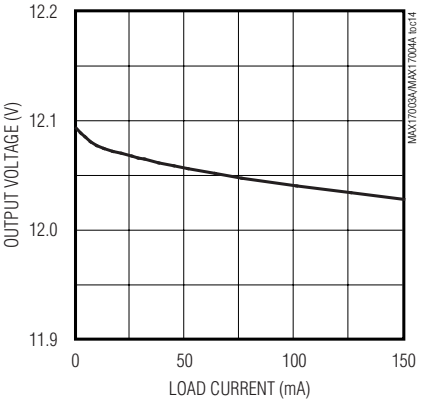
REFERENCE OFFSET VOLTAGE DISTRIBUTION



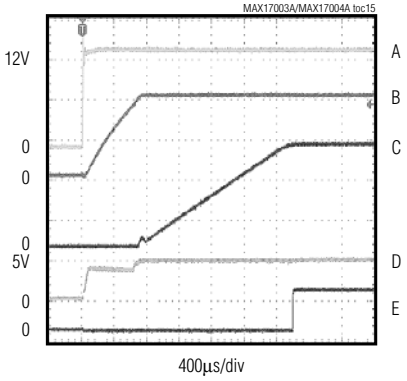
LDO5 OUTPUT VOLTAGE vs. LOAD CURRENT



OUTA OUTPUT VOLTAGE vs. LOAD CURRENT



POWER-UP SEQUENCE



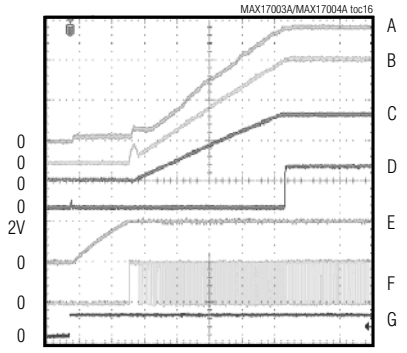
A. INPUT SUPPLY, 5V/div
B. REF, 1V/div
C. 5V OUTPUT (V_{OUT5}), 2V/div
D. LDO5, 5V/div
E. PGDALL, 5V/div

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

Typical Operating Characteristics (continued)

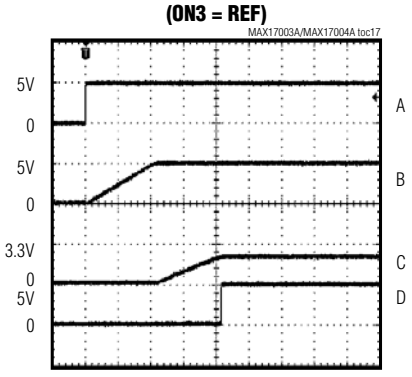
(Circuit of Figure 1, V_{IN} = 12V, $\overline{SKIP}$ = GND, FSEL = REF, T_A = +25°C, unless otherwise noted.)

SOFT-START WAVEFORM



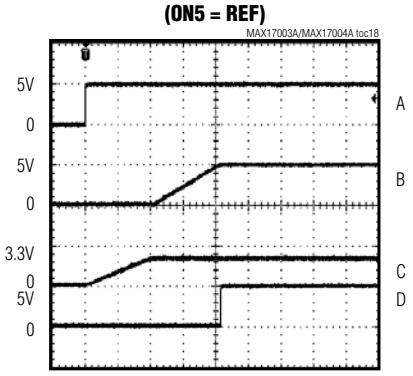
A. AUX LDO OUTPUT (V_{OUTA}), 5V/div
B. 5V OUTPUT (V_{OUT5}), 2V/div
C. 3.3V OUTPUT (V_{OUT3}), 2V/div
D. PGDALL, 5V/div
ON3 = ON5, LDO5
E. REF, 2V/div
F. DL5, 5V/div
G. $\overline{SHDN}$, 5V/div

SMPS DELAYED STARTUP SEQUENCE (ON3 = REF)



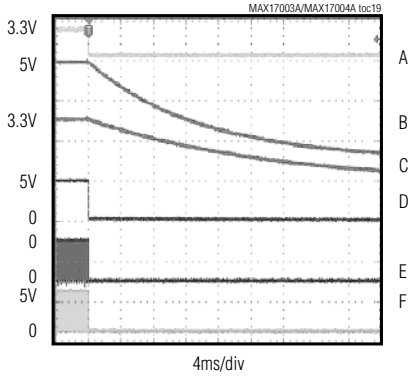
A. ON5, 5V/div
B. 5V OUTPUT (V_{OUT5}), 5V/div
C. 3.3V OUTPUT (V_{OUT3}), 5V/div
D. PGDALL, 5V/div

SMPS DELAYED STARTUP SEQUENCE (ON5 = REF)



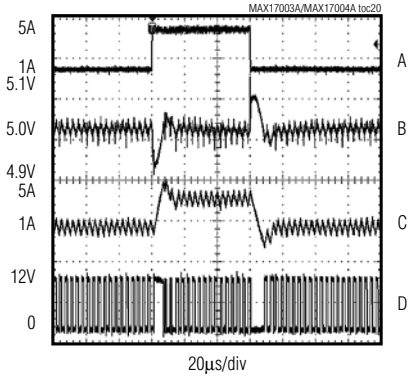
A. ON3, 5V/div
B. 5V OUTPUT (V_{OUT5}), 5V/div
C. 3.3V OUTPUT (V_{OUT3}), 5V/div
D. PGDALL, 5V/div

SMPS SHUTDOWN WAVEFORM



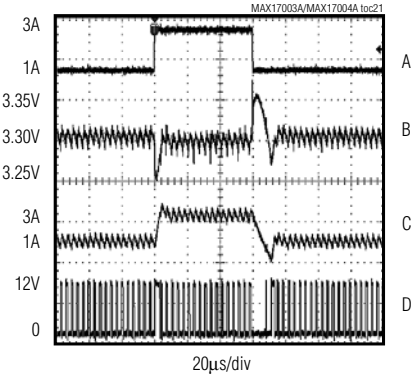
A. ON3, ON5, 5V/div
B. 5V OUTPUT (V_{OUT5}), 2V/div
C. 3.3V OUTPUT (V_{OUT3}), 2V/div
D. PGDALL, 5V/div
E. DL5, 5V/div
F. DL3, 5V/div

OUT5 LOAD TRANSIENT



A. I_{OUT5} = 1A TO 5A, 5A/div
B. V_{OUT5}, 50mV/div
C. INDUCTOR CURRENT, 5A/div
D. LX5, 10V/div

OUT3 LOAD TRANSIENT

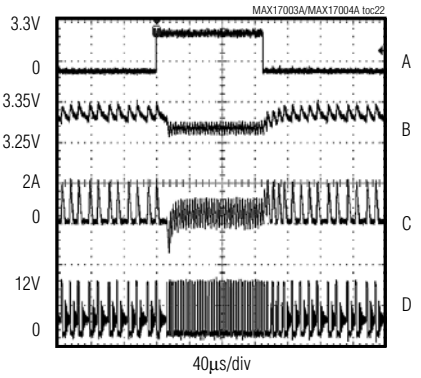


A. I_{OUT3} = 1A TO 3A, 5A/div
B. V_{OUT3}, 50mV/div
C. INDUCTOR CURRENT, 5A/div
D. LX3, 10V/div

Typical Operating Characteristics (continued)

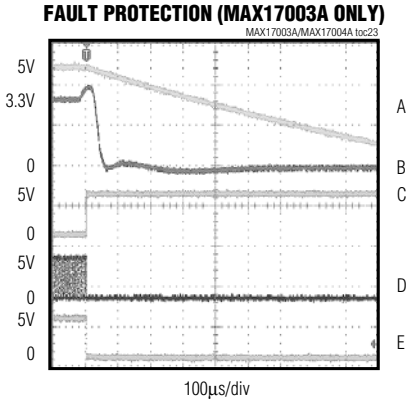
(Circuit of Figure 1, V_{IN} = 12V, $\overline{SKIP}$ = GND, FSEL = REF, T_A = +25°C, unless otherwise noted.)

$\overline{SKIP}$ TRANSITION



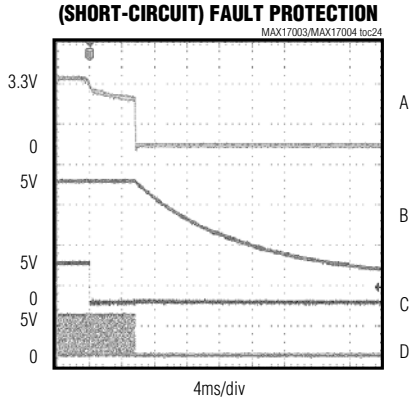
A. $\overline{SKIP}$, 5V/div
B. 3.3V OUTPUT (V_{OUT3}), 100mV/div
0.5A LOAD
C. INDUCTOR CURRENT, 2A/div
D. LX3, 10V/div

OUTPUT OVERVOLTAGE FAULT PROTECTION (MAX17003A ONLY)



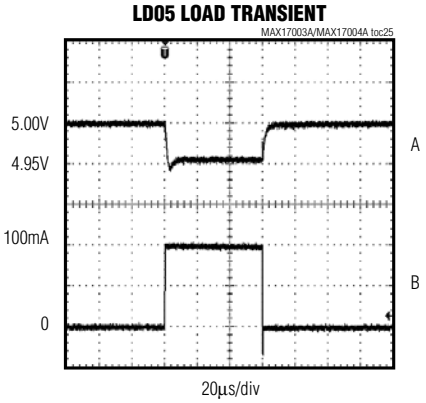
A. 5V OUTPUT (V_{OUT5}), 2V/div
B. 3.3V OUTPUT (V_{OUT3}), 2V/div
C. DL3, 5V/div
R_{LOAD5} = 5Ω
D. DL5, 5V/div
E. PGDALL, 5V/div

OUTPUT UNDERVOLTAGE (SHORT-CIRCUIT) FAULT PROTECTION



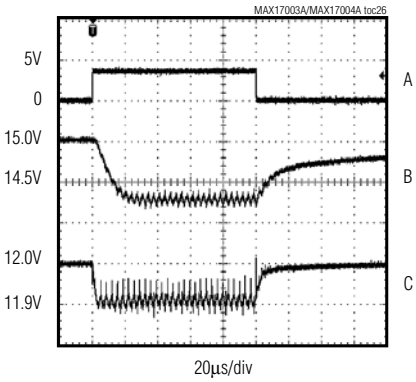
A. 3.3V OUTPUT (V_{OUT3}), 2V/div
B. 5V OUTPUT (V_{OUT5}), 2V/div
C. PGDALL, 5V/div
D. DL3, 5V/div

LDO5 LOAD TRANSIENT



A. LDO5 OUTPUT, 50mV/div
B. LOAD CURRENT, 50mA/div

LDOA LOAD TRANSIENT



A. LOAD FET GATE, 5V/div
B. AUX LDO INPUT, 0.5V/div
0 TO 150mA LOAD TRANSIENT
C. AUX LDO OUTPUT (V_{OUTA}), 0.1V/div

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

Pin Description

PIN	NAME	FUNCTION
1	ONA	Auxiliary LDO Enable Input. When ONA is pulled low, OUTA is high impedance and the secondary feedback control is disabled. When ONA is driven high, the controller enables the auxiliary LDO.
2	DRVA	Auxiliary LDO Transistor Base Driver. Connect DRVA to the base of a pnp power transistor. Add a 680Ω pullup resistor between the base and emitter.
3	ILIM	Peak Current-Limit Threshold Adjustment. The current-limit threshold defaults to 50mV if ILIM is pulled up to LDO5. In adjustable mode, the current-limit threshold across CSH_ and CSL_ is precisely 1/10 the voltage seen at ILIM over a 0.5V to 2.0V range. The logic threshold for switchover to the 50mV default value is approximately V_{LDO5} - 1V.
4	$\overline{SHDN}$	Shutdown Control Input. The device enters its 8µA supply-current shutdown mode if $V_{\overline{SHDN}}$ is less than the $\overline{SHDN}$ input falling-edge trip level and does not restart until $V_{\overline{SHDN}}$ is greater than the $\overline{SHDN}$ input rising-edge trip level. Connect $\overline{SHDN}$ to V_{IN} for automatic startup. $\overline{SHDN}$ can be connected to V_{IN} through a resistive voltage-divider to implement a programmable undervoltage lockout.
5	ON3	3.3V SMPS Enable Input. Driving ON3 high enables the 3.3V SMPS, while pulling ON3 low disables the 3.3V SMPS. If ON3 is connected to REF, the 3.3V SMPS starts after the 5V SMPS reaches regulation (delayed start). Drive ON3 below the clear fault level to reset the fault latch.
6	ON5	5V SMPS Enable Input. Driving ON5 high enables the 5V SMPS, while pulling ON5 low disables the 5V SMPS. If ON5 is connected to REF, the 5V SMPS starts after the 3.3V SMPS reaches regulation (delayed start). Drive ON5 below the clear fault level to reset the fault latch.
7	REF	2.0V Reference Voltage Output. Bypass REF to analog ground with a 0.1µF or greater ceramic capacitor. The reference sources up to 50µA for external loads. Loading REF degrades output-voltage accuracy according to the REF load-regulation error. The reference shuts down when the system pulls $\overline{SHDN}$ low.
8	GND	Analog Ground. Connect the exposed backside pad to GND.
9	FSEL	Frequency Select Input. This three-level logic input sets the controllers' switching frequency. Connect to LDO5, REF, or GND to select the following typical switching frequencies: LDO5 = 500kHz, REF = 300kHz, GND = 200kHz.
10	$\overline{SKIP}$	Pulse-Skipping Control Input. Connect to LDO5 for low-noise, forced-PWM operation. Connect to REF for automatic, low-noise, pulse-skipping operation at light loads. Connect to GND for automatic, high-efficiency, pulse-skipping operation at light loads. Startup is always in the low-noise, pulse-skipping mode (i.e., same as $\overline{SKIP}$ = REF setting), regardless of the $\overline{SKIP}$ setting. The $\overline{SKIP}$ setting takes effect once the respective SMPS is in regulation.
11	FB5	Feedback Input for the 5V SMPS. Connect to LDO5 for the preset 5V output. In adjustable mode, FB5 regulates to 2V.
12	CSH5	Positive Current-Sense Input for the 5V SMPS. Connect to the positive terminal of the current-sense element. Figure 7 describes two different current-sensing options—using accurate sense resistors or lossless inductor DCR sensing.
13	CSL5	Output-Sense and Negative Current-Sense Input for the 5V SMPS. When using the internal preset 5V feedback-divider (FB5 = LDO5), the controller uses CSL5 to sense the output voltage. Connect to the negative terminal of the current-sense element. CSL5 also serves as the bootstrap input for LDO5. For the MAX17003A, place a Schottky diode from CSL5 to GND to prevent CSL5 from going below -7V.
14	DSCHG5	Open-Drain Discharge Input for the 5V SMPS. DSCHG5 is pulled low when ON5 is low, discharging the SMPS5 output. DSCHG5 is also low under fault conditions. Connect a 47_ or larger resistor from DSCHG5 to the SMPS5 output.

Pin Description (continued)

PIN	NAME	FUNCTION
15	BST5	Boost Flying Capacitor Connection for the 5V SMPS. The MAX17003A/MAX17004A include an internal boost switch connected between LDO5 and BST5. Connect to an external capacitor as shown in Figure 1.
16	DH5	High-Side Gate-Driver Output for the 5V SMPS. DH5 swings from LX5 to BST5.
17	LX5	Inductor Connection for the 5V SMPS. Connect LX5 to the switched side of the inductor. LX5 serves as the lower supply rail for the DH5 high-side gate driver.
18	DL5	Low-Side Gate-Driver Output for the 5V SMPS. DL5 swings from PGND to LDO5.
19	PGND	Power Ground
20	LDO5	5V Internal Linear-Regulator Output. Bypass with 4.7µF minimum (1µF/25mA). Provides at least 100mA for the DL_ low-side gate drivers, the DH_ high-side drivers through the BST switches, the PWM controller, logic, reference, and external loads. If CSL5 is greater than 4.5V and soft-start is complete, the linear regulator shuts down, and LDO5 connects to CSL5 through a 1Ω switch rated for loads up to 200mA.
21	IN	Input of the Startup Circuitry and the LDO5 Internal 5V Linear Regulator. Bypass to PGND with a 0.22µF or greater ceramic capacitor close to the IC.
22	PGDALL	Open-Drain Power-Good Output for SMPS3 and SMPS5. PGDALL is pulled low if **either** SMPS3 or SMPS5 output drops more than 10% (typ) below the normal regulation point, or if **either** ON3 or ON5 is low. PGDALL becomes high impedance when **both** SMPS3 and SMPS5 are in regulation.
23	DL3	Low-Side Gate-Driver Output for the 3.3V SMPS. DL3 swings from PGND to LDO5.
24	LX3	Inductor Connection for the 3.3V SMPS. Connect LX3 to the switched side of the inductor. LX3 serves as the lower supply rail for the DH3 high-side gate driver.
25	DH3	High-Side Gate-Driver Output for the 3.3V SMPS. DH3 swings from LX3 to BST3.
26	BST3	Boost Flying Capacitor Connection for the 3.3V SMPS. The MAX17003A/MAX17004A include an internal boost switch connected between LDO5 and BST3. Connect to an external capacitor as shown in Figure 1.
27	DSCHG3	Open-Drain Discharge Output for the 3.3V SMPS. DSCHG3 is pulled low when ON3 is low, discharging the SMPS3 output. DSCHG3 is also low under fault conditions. Connect a 47Ω or larger resistor from DSCHG3 to the SMPS3 output.
28	CSL3	Output Sense and Negative Current Sense for the 3.3V SMPS. When using the internal preset 3.3V feedback divider (FB3 = LDO5), the controller uses CSL3 to sense the output voltage. Connect to the negative terminal of the current-sense element.
29	CSH3	Positive Current-Sense Input for the 3.3V SMPS. Connect to the positive terminal of the current-sense element. Figure 7 describes two different current-sensing options—using accurate sense resistors or lossless inductor DCR sensing.
30	FB3	Feedback Input for the 3.3V SMPS. Connect to LDO5 for fixed 3.3V output. In adjustable mode, FB3 regulates to 2V.

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

Pin Description (continued)

PIN	NAME	FUNCTION
31	FBA	Auxiliary LDO Feedback Input. Connect a resistive voltage-divider from OUTA to analog ground to adjust the auxiliary linear-regulator output voltage. FBA regulates at 1V.
32	OUTA	Adjustable Auxiliary Linear-Regulator Output. Bypass OUTA to GND with 1µF or greater capacitor (1µF/25mA). When DRVA < OUTA, the secondary feedback control triggers the DL5 for 1µs forcing the controller to recharge the auxiliary storage capacitor. When DRVA exceeds 25V, the MAX17003A/MAX17004A enable a 10mA shunt on OUTA, preventing the storage capacitor from rising to unsafe levels due to the transformer's leakage inductance. Pulling ONA high enables the linear-regulator driver and the secondary feedback control.
EP	EP	Exposed Pad. **Connect the exposed backside pad to analog ground.**

Table 1. Component Selection for Standard Applications

COMPONENT	300kHz 5V AT 5A 3.3V AT 5A	500kHz 5V AT 3A 3.3V AT 5A
INPUT VOLTAGE	**V_{IN} = 7V TO 24V**	**V_{IN} = 7V TO 24V**
$C_{IN\_}$, Input Capacitor	(3) 10µF, 25V Taiyo Yuden TMK432BJ106KM	(3) 10µF, 25V Taiyo Yuden TMK432BJ106KM
5V OUTPUT		
C_{OUT5}, Output Capacitor	2x 100µF, 6V, 35mΩ SANYO 6TPE100MAZB	2x 100µF, 6V, 35mΩ SANYO 6TPE100MAZB
L5/T5, Inductor/Transformer	6.8µH, 6.4A, 18mΩ (max) 1:2 Sumida 4749-T132	—
N_{H5}, High-Side MOSFET	Fairchild Semiconductor FDS6612A International Rectifier IRF7807V	Fairchild Semiconductor FDS6612A International Rectifier IRF7807V
N_{L5}, Low-Side MOSFET	Fairchild Semiconductor FDS6670S International Rectifier IRF7807VD1	Fairchild Semiconductor FDS6670S International Rectifier IRF7807VD1
3V OUTPUT		
C_{OUT3}, Output Capacitor	2x 150µF, 4V, 35mΩ SANYO 4TPE150MAZB	2x 100µF, 6V, 35mΩ SANYO 6TPE100MAZB
L3, Inductor	5.8µH, 8.6A, 16.2mΩ Sumida CORH127/LD-BR8NC	3.9µH, 6.5A, 15mΩ Sumida CDRH124-3R9NC
N_{H3}, High-Side MOSFET	Fairchild Semiconductor FDS6612A International Rectifier IRF7807V	Fairchild Semiconductor FDS6612A International Rectifier IRF7807V
N_{L3}, Low-Side MOSFET	Fairchild Semiconductor FDS6670S International Rectifier IRF7807VD1	Fairchild Semiconductor FDS6670S International Rectifier IRF7807VD1

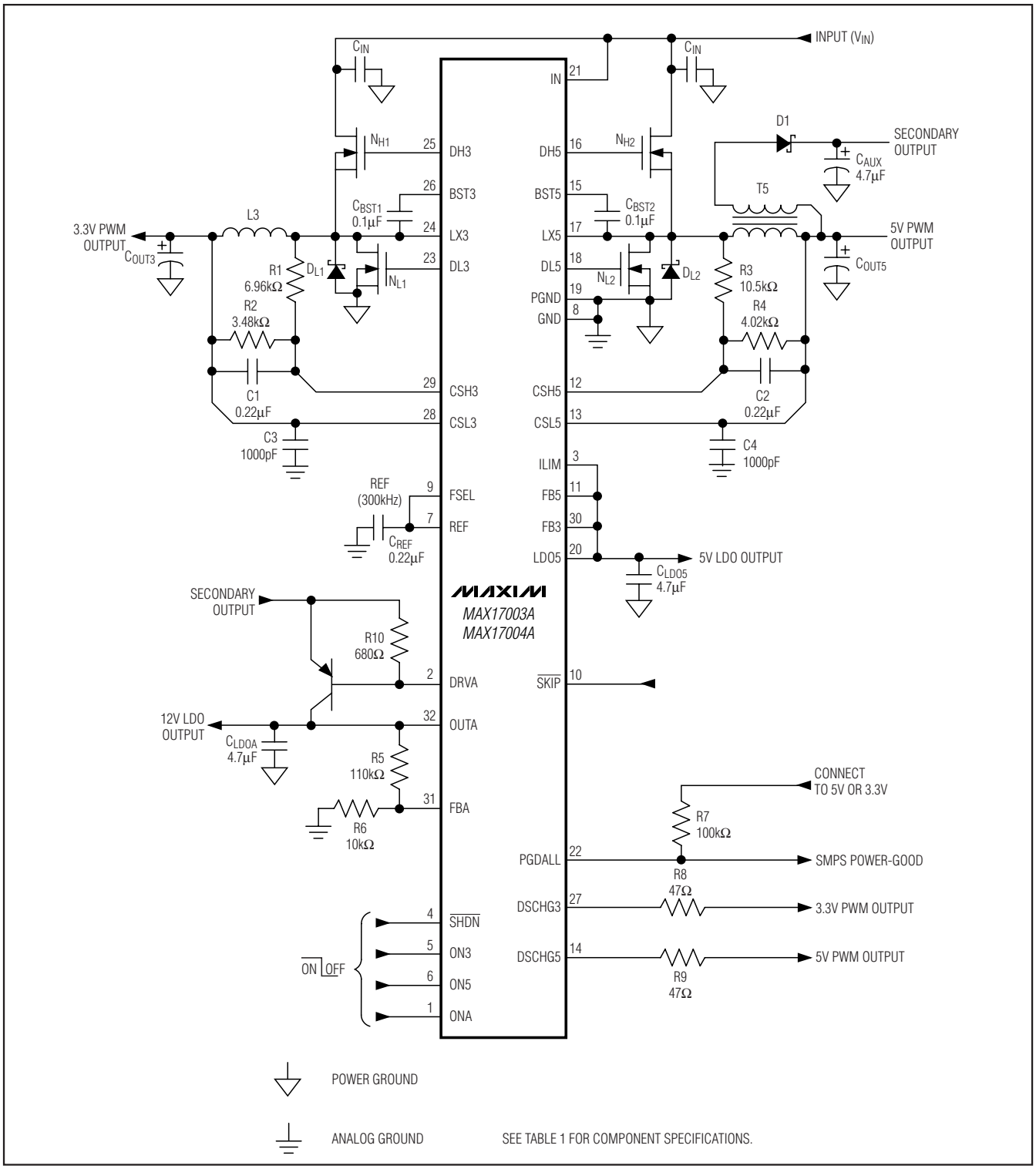


Figure 1. Standard Application Circuit

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

Table 2. Component Suppliers

SUPPLIER	WEBSITE
AVX	www.avx.com
Central Semiconductor	www.centralsemi.com
Fairchild	www.fairchildsemi.com
International Rectifier	www.irf.com
KEMET	www.kemet.com
NEC/Tokin	www.nec-tokin.com
Panasonic	www.panasonic.com/industrial
Philips	www.philips.com
Pulse	www.pulseeng.com
Renesas	www.renesas.com
SANYO	www.edc.sanyo.com
Sumida	www.sumida.com
Taiyo Yuden	www.t-yuden.com
TDK	www.component.tdk.com
TOKO	www.tokoam.com
Vishay (Dale, Siliconix)	www.vishay.com

Detailed Description

The MAX17003A/MAX17004A standard application circuit (Figure 1) generates the 5V/5A and 3.3V/5A typical of the main supplies in a notebook computer. The input supply range is 7V to 24V. See Table 1 for component selections, while Table 2 lists the component manufacturers.

The MAX17003A/MAX17004A contain two interleaved, fixed-frequency, step-down controllers designed for low-voltage power supplies. The optimal interleaved architecture guarantees out-of-phase operation, reducing the input capacitor ripple. One internal LDO generates the keep-alive 5V power. The MAX17003A/MAX17004A have an auxiliary LDO with an adjustable output for generating either the 3.3V keep-alive supply or regulating the low-power 12V system supply.

Fixed 5V Linear Regulator (LDO5)

An internal linear regulator produces a preset 5V low-current output. LDO5 powers the gate drivers for the external MOSFETs, and provides the bias supply required for the SMPS analog controller, reference, and logic blocks. LDO5 supplies at least 100mA for external and internal loads, including the MOSFET gate drive, which typically varies from 5mA to 50mA, depending on the switching frequency and external MOSFETs selected. Bypass LDO5 with a 4.7µF or greater ceramic capacitor (1µF per 25mA of load) to guarantee stability under the full-load conditions.

The MAX17003A/MAX17004A SMPS require a 5V bias supply in addition to the high-power input supply (battery or AC adapter). This 5V bias supply is generated by the controller's internal 5V linear regulator (LDO5). This bootstrapped LDO allows the controller to power up independently. The gate-driver input supply is connected to the fixed 5V linear-regulator output (LDO5). Therefore, the 5V LDO supply must provide LDO5 (PWM controller) and the gate-drive power, so the maximum supply current required is:

$$I_{BIAS} = I_{CC} + f_{SW} (Q_{G(LOW)} + Q_{G(HIGH)})$$
$$= 5mA \text{ to } 50mA \text{ (typ)}$$

where I_{CC} is 0.7mA (typ), f_{SW} is the switching frequency, and $Q_{G(LOW)}$ and $Q_{G(HIGH)}$ are the MOSFET data sheet's total gate-charge specification limits at V_{GS} = 5V.

SMPS-to-LDO Bootstrap Switchover

When the 5V main output voltage is above the LDO5 bootstrap-switchover threshold and has completed soft-start, an internal 1Ω (typ) p-channel MOSFET shorts CSL5 to LDO5, while simultaneously shutting down the LDO5 linear regulator. This bootstraps the device, powering the internal circuitry and external loads from the 5V SMPS output (CSL5), rather than through the linear regulator from the battery. Bootstrapping reduces power dissipation due to gate charge and quiescent losses by providing power from a 90%-efficient switch-mode source, rather than from a much-less-efficient linear regulator. The current capability increases from 100mA to 200mA when the LDO5 output is switched over to CSL5. When ON5 is pulled low, the controller immediately disables the bootstrap switch and reenables the 5V LDO.

Reference (REF)

The 2V reference is accurate to ±1% over temperature and load, making REF useful as a precision system reference. Bypass REF to GND with a 0.1µF or greater ceramic capacitor. The reference sources up to 50µA and sinks 5µA to support external loads. If highly accurate specifications are required for the main SMPS output voltages, the reference should not be loaded. Loading the reference reduces the LDO5, CSL5 (OUT5), CSL3 (OUT3), and OUTA output voltages slightly because of the reference load-regulation error.

System Enable/Shutdown ($\overline{SHDN}$)

Drive $\overline{SHDN}$ below the precise $\overline{SHDN}$ input falling-edge trip level to place the MAX17003A/MAX17004A in its low-power shutdown state. The controller consumes only 8µA of quiescent current while in shutdown mode. When shutdown mode activates, the reference turns off after the controller completes the shutdown sequence,

Table 3. Operating Mode Truth Table

MODE	INPUTS*			OUTPUTS		
	$\overline{SHDN}$	ON5	ON3	LDO5	5V SMPS	3V SMPS
Shutdown Mode	Low	X	X	OFF	OFF	OFF
Standby Mode	High	Low	Low	ON	OFF, DSCHG5 LOW	OFF, DSCHG3 LOW
Normal Operation	High	High	High	ON	ON	ON
3.3V SMPS Active	High	Low	High	ON	OFF, DSCHG5 LOW	ON
5V SMPS Active	High	High	Low	OFF LDO5 to CSL5 bypass switch enabled	ON	OFF, DSCHG3 LOW
Normal Operation (Delayed 5V SMPS Startup)	High	Ref	High	OFF LDO5 to CSL5 bypass switch enabled	ON Power-up after 3.3V SMPS is in regulation	ON
Normal Operation (Delayed 3.3V SMPS Startup)	High	High	Ref	OFF LDO5 to CSL5 bypass switch enabled	ON	ON Power-up after 5V SMPS is in regulation

**$\overline{SHDN}$ is an accurate, low-voltage logic input with 1V falling-edge threshold voltage and 1.6V rising-edge threshold voltage. ON3 and ON5 are tri-level CMOS logic inputs, a logic-low voltage is less than 0.8V, a logic-high voltage is greater than 2.4V, and the middle-logic level is between 1.7V and 2.3V (see the* Electrical Characteristics *table).*

making the threshold to exit shutdown less accurate. To guarantee startup, drive $\overline{SHDN}$ above 2V ($\overline{SHDN}$ input rising-edge trip level). For automatic shutdown and startup, connect $\overline{SHDN}$ to V_{IN}. The accurate 1V falling-edge threshold on $\overline{SHDN}$ can be used to detect a specific input voltage level and shut the device down. Once in shutdown, the 1.6V rising-edge threshold activates, providing sufficient hysteresis for most applications (see Table 3).

SMPS POR, UVLO, and Soft-Start

Power-on reset (POR) occurs when LDO5 rises above approximately 1V, resetting the undervoltage, overvoltage, and thermal-shutdown fault latches. The POR circuit also ensures that the low-side drivers are pulled high until the SMPS controllers are activated. Figure 2 is the MAX17003A/MAX17004A block diagram.

The LDO5 input undervoltage-lockout (UVLO) circuitry inhibits switching if the 5V bias supply (LDO5) is below its 4V UVLO threshold. Once the 5V bias supply (LDO5) rises above this input UVLO threshold and the SMPS controllers are enabled (ON_ driven high), the SMPS controllers start switching, and the output voltages begin to ramp up using soft-start. If the LDO5 voltage drops below the UVLO threshold, the controller stops switching and pulls the low-side gate drivers low until the LDO5 voltage recovers or drops below the POR threshold.

The internal soft-start gradually increases the feedback voltage with a 1V/ms slew rate. Therefore, the outputs reach their nominal regulation voltage 2ms after the SMPS controllers are enabled (see the Soft-Start Waveform in the *Typical Operating Characteristics*). This gradual slew rate effectively reduces the input surge current by minimizing the current required to charge the output capacitors ($I_{OUT} = I_{LOAD} + C_{OUT} \times V_{OUT(NOM)}/t_{SLEW}$).

SMPS Enable Controls (ON3, ON5)

ON3 and ON5 control SMPS power-up sequencing. ON3 or ON5 rising above 2.4V enables the respective outputs. ON3 or ON5 falling below 1.6V disables the respective outputs. Driving ON_ below 0.8V clears the overvoltage, undervoltage, and thermal-fault latches.

SMPS Power-Up Sequencing

Connecting ON3 or ON5 to REF forces the respective outputs off while the other output is below regulation and starts after that output regulates. The second SMPS remains on until the first SMPS turns off, the device shuts down, a fault occurs, or LDO5 goes into UVLO. Both supplies begin their power-down sequence immediately when the first supply turns off.

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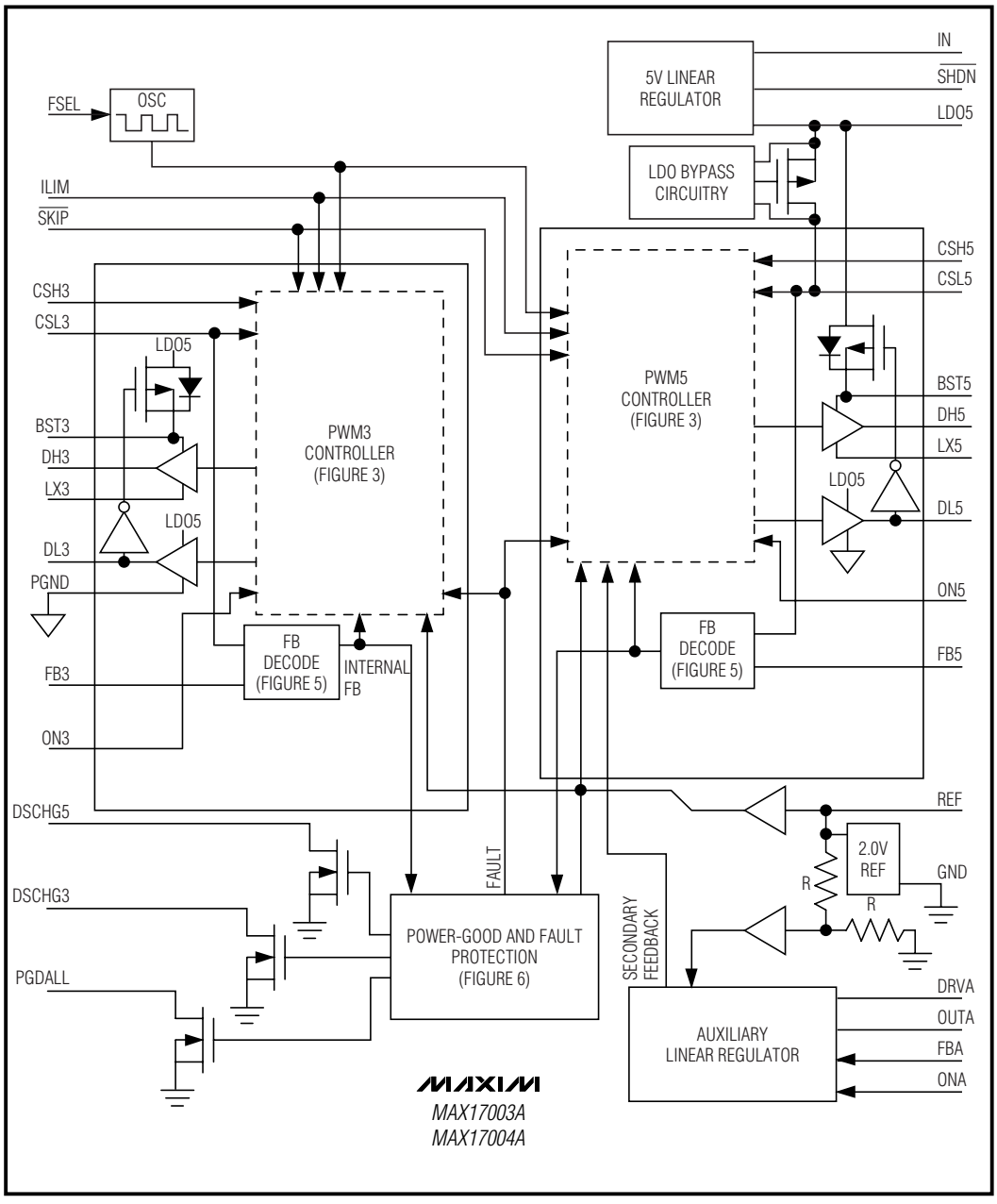

Figure 2. Functional Diagram

Output Discharge (Soft-Discharge)

When the switching regulators are disabled—when ON_ or $\overline{SHDN}$ is pulled low, or when an output undervoltage fault occurs—the internal soft-discharge gradually decreases the output voltage by pulling DSCHG_ low (see the SMPS Shutdown Waveform in the *Typical Operating Characteristics*). This slowly discharges the output capacitance, eliminating the negative output voltages caused by quickly discharging the output through the inductor and low-side MOSFET. Both SMPS controllers contain separate soft-shutdown circuits.

Fixed-Frequency, Current-Mode PWM Controller

The heart of each current-mode PWM controller is a multi-input, open-loop comparator that sums two signals: the output-voltage error signal with respect to the reference voltage and the slope-compensation ramp (Figure 3). The MAX17003A/MAX17004A use a direct-summing configuration, approaching ideal cycle-to-cycle control over the output voltage without a traditional error amplifier and the phase shift associated with it.

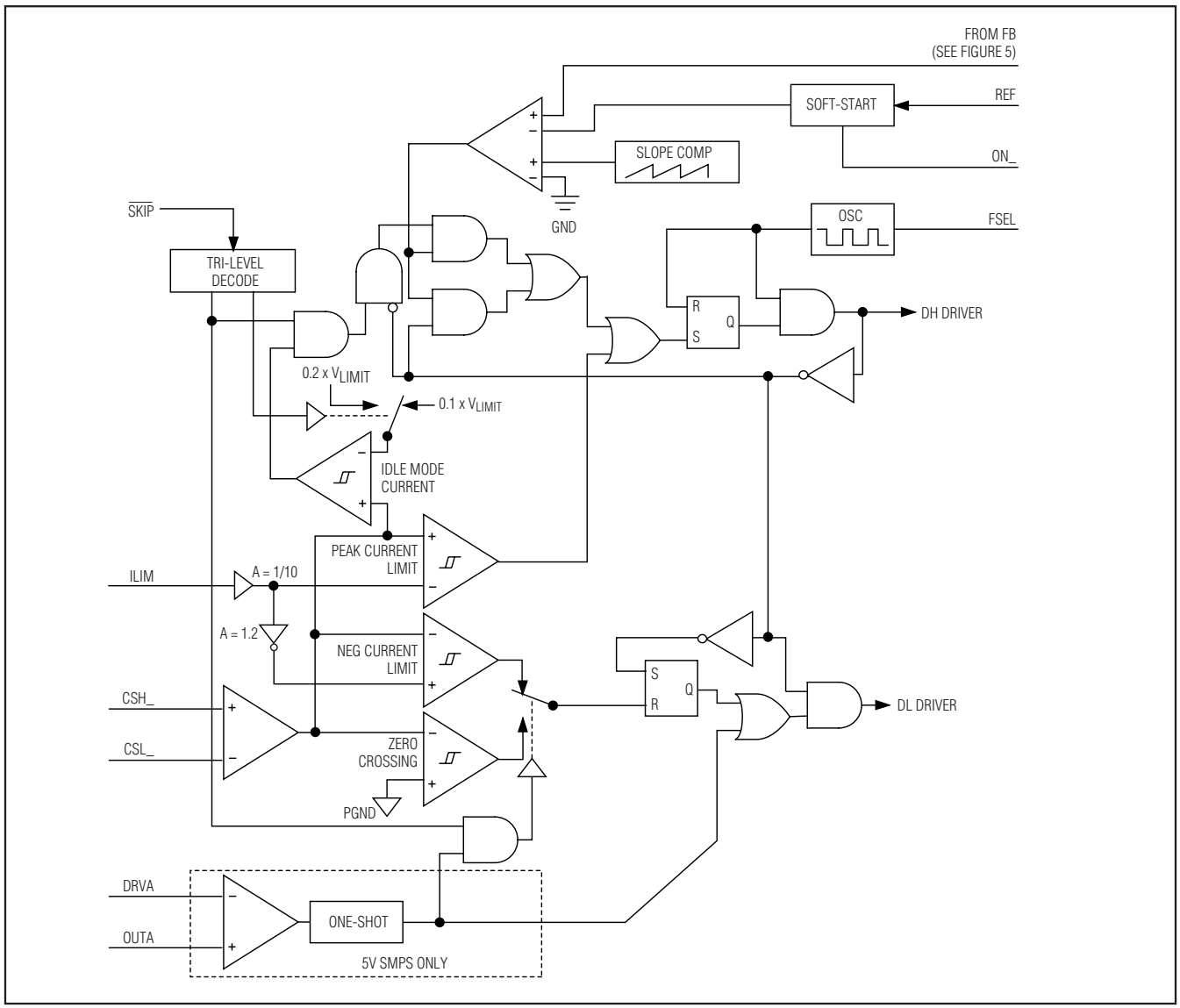

Figure 3. PWM Controller Functional Diagram

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Table 4. FSEL Configuration Table

FSEL	SWITCHING FREQUENCY (kHz)
LDO5	500
REF	300
GND	200

Frequency Selection (FSEL)

The FSEL input selects the PWM mode switching frequency. Table 4 shows the switching frequency based on FSEL connection. High-frequency (500kHz) operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. This may be acceptable in ultraportable devices where the load currents are lower. Low-frequency (200kHz) operation offers the best overall efficiency at the expense of component size and board space.

Forced-PWM Mode

The low-noise forced-PWM mode ($\overline{SKIP}$ = LDO5) disables the zero-crossing comparator, which controls the low-side switch on-time. This forces the low-side gate-drive waveform to constantly be the complement of the high-side gate-drive waveform, so the inductor current reverses at light loads while DH_ maintains a duty factor of V_{OUT}/V_{IN}. The benefit of forced-PWM mode is to keep the switching frequency fairly constant. However, forced-PWM operation comes at a cost: the no-load 5V supply current remains between 20mA and 50mA, depending on the external MOSFETs and switching frequency.

Forced-PWM mode is most useful for avoiding audio-frequency noise and improving load-transient response. Since forced-PWM operation disables the zero-crossing comparator, the inductor current reverses under light loads.

Light-Load Operation Control ($\overline{SKIP}$)

The MAX17003A/MAX17004A include a light-load operating mode control input ($\overline{SKIP}$) used to enable or disable the zero-crossing comparator for both switching regulators. When the zero-crossing comparator is enabled, the regulator forces DL_ low when the current-sense inputs detect zero inductor current. This keeps the inductor from discharging the output capacitors and forces the regulator to skip pulses under light-load conditions to avoid overcharging the output. When the zero-crossing comparator is disabled, the regulator is forced to maintain PWM operation under light load conditions (forced PWM).

Idle-Mode Current-Sense Threshold

When pulse-skipping mode is enabled, the on-time of the step-down controller terminates when the output voltage exceeds the feedback threshold and when the current-sense voltage exceeds the idle-mode current-sense threshold. Under light load conditions, the on-time duration depends solely on the idle-mode current-sense threshold, which is 20% ($\overline{SKIP}$ = GND) of the full-load current-limit threshold set by ILIM, or the low-noise current-sense threshold, which is 10% ($\overline{SKIP}$ = REF) of the full-load current-limit threshold set by ILIM. This forces the controller to source a minimum amount of power with each cycle. To avoid overcharging the output, another on-time cannot begin until the output voltage drops below the feedback threshold. Since the zero-crossing comparator prevents the switching regulator from sinking current, the controller must skip pulses. Therefore, the controller regulates the valley of the output ripple under light load conditions.

Automatic Pulse-Skipping Crossover

In skip mode, an inherent automatic switchover to PFM takes place at light loads (Figure 4). This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. The zero-crossing comparator senses the inductor current across CSH_ to CSL_. Once $V_{CSH\_} - V_{CSL\_}$ drops below the 3mV zero-crossing, current-sense threshold, the comparator forces DL_ low (Figure 3). This mechanism causes the threshold between pulse-skipping PFM and nonskipping PWM operation to coincide with the boundary between continuous and discontinuous

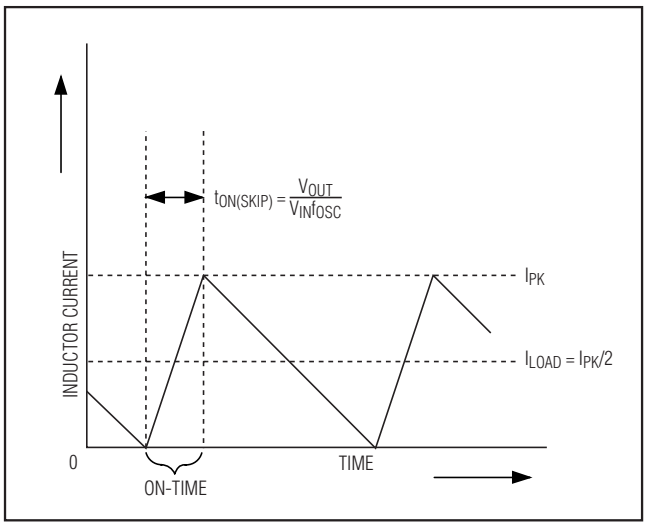

Figure 4. Pulse-Skipping/Discontinuous Crossover Point

inductor-current operation (also known as the "critical conduction" point). The load-current level at which PFM/PWM crossover occurs, $I_{LOAD(SKIP)}$, is given by:

$$I_{LOAD(SKIP)} = \frac{(V_{IN} - V_{OUT})V_{OUT}}{2V_{IN}f_{OSC}L}$$

The switching waveforms may appear noisy and asynchronous when light loading causes pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs in PFM noise vs. light-load efficiency are made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output-voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load-transient response (especially at low input-voltage levels).

Output Voltage

DC output accuracy specifications in the *Electrical Characteristics* table refer to the error comparator's threshold. When the inductor continuously conducts, the MAX17003A/MAX17004A regulate the peak of the output ripple, so the actual DC output voltage is lower than the slope-compensated trip level by 50% of the output ripple voltage. For PWM operation (continuous conduction), the output voltage is accurately defined by the following equation:

$$V_{OUT(PWM)} = V_{NOM}\left(1 - \frac{A_{SLOPE}V_{RIPPLE}}{V_{IN}}\right) - \left(\frac{V_{RIPPLE}}{2}\right)$$

where V_{NOM} is the nominal output voltage, A_{SLOPE} equals 1.1%, and V_{RIPPLE} is the output ripple voltage (V_{RIPPLE} = ESR x $\Delta I_{INDUCTOR}$, as described in the *Output Capacitor Selection* section).

In discontinuous conduction ($I_{OUT} < I_{LOAD(SKIP)}$), the MAX17003A/MAX17004A regulate the valley of the output ripple, so the output voltage has a DC regulation level higher than the error-comparator threshold. For PFM operation (discontinuous conduction), the output voltage is approximately defined by the following equation:

$$V_{OUT(PFM)} = V_{NOM} + \frac{1}{2}\left(\frac{f_{SW}}{f_{OSC}}\right)I_{IDLE}ESR$$

where V_{NOM} is the nominal output voltage, f_{OSC} is the maximum switching frequency set by the internal oscillator, f_{SW} is the actual switching frequency, and I_{IDLE} is the idle-mode inductor current when pulse skipping.

Connect FB3 and FB5 to LDO5 to enable the fixed SMPS output voltages (3.3V and 5V, respectively), set by a preset, internal resistive voltage-divider connected between the output (CSL_) and analog ground. Connect a resistive voltage-divider at FB_ between the output (CSL_) and GND to adjust the respective output voltage between 2V and 5.5V (Figure 5). Choose R_{FBLO} (resistance from FB to GND) to be approximately 10kΩ and solve for R_{FBHI} (resistance from the output to FB) using the equation:

$$R_{FBHI} = R_{FBLO}\left(\frac{V_{OUT\_}}{V_{FB\_}} - 1\right)$$

where $V_{FB\_}$ = 2V nominal.

When adjusting both output voltages, set the 3.3V SMPS lower than the 5V SMPS. LDO5 connects to the 5V output (CSL5) through an internal switch only when CSL5 is above the LDO5 bootstrap threshold (4.5V) and the soft-start sequence for the CSL5 side has completed. Bootstrapping works most effectively when the fixed output voltages are used. Once LDO5 is bootstrapped from CSL5, the internal 5V linear regulator turns off. This reduces the internal power dissipation and improves efficiency at higher input voltages.

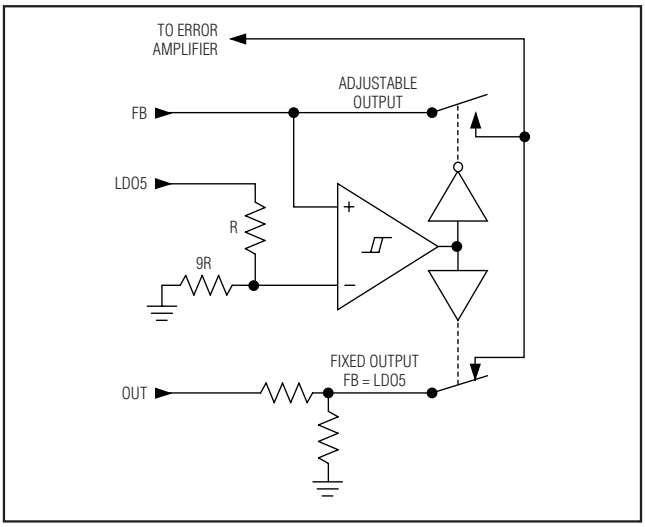

Figure 5. Dual Mode Feedback Decoder

Current-Limit Protection (ILIM)

The current-limit circuit uses differential current-sense inputs (CSH_ and CSL_) to limit the peak inductor current. If the magnitude of the current-sense signal exceeds the current-limit threshold, the PWM controller

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turns off the high-side MOSFET (Figure 3). The actual maximum load current is less than the peak current-limit threshold by an amount equal to half of the inductor ripple current. Therefore, the maximum load capability is a function of the current-sense resistance, inductor value, switching frequency, and duty cycle (V_{OUT}/V_{IN}).

In forced-PWM mode, the MAX17003A/MAX17004A also implement a negative current limit to prevent excessive reverse inductor currents when V_{OUT} is sinking current. The negative current-limit threshold is set to approximately 120% of the positive current limit and tracks the positive current limit when ILIM is adjusted.

Connect ILIM to LDO5 for the 50mV default threshold, or adjust the current-limit threshold with an external resistor-divider at ILIM. Use a 2µA to 20µA divider current for accuracy and noise immunity. The current-limit threshold adjustment range is from 50mV to 200mV. In the adjustable mode, the current-limit threshold voltage equals precisely 1/10 the voltage seen at ILIM. The logic threshold for switchover to the default value is approximately V_{LDO5} - 1V.

Carefully observe the PCB layout guidelines to ensure that noise and DC errors do not corrupt the differential current-sense signals seen by CSH_ and CSL_. Place the IC close to the sense resistor with short, direct traces, making a Kelvin-sense connection to the current-sense resistor.

MOSFET Gate Drivers (DH_, DL_)

The DH_ and DL_ drivers are optimized for driving moderate-sized high-side and larger low-side power MOSFETs. This is consistent with the low duty factor seen in notebook applications, where a large V_{IN} - V_{OUT} differential exists. The high-side gate drivers (DH_) source and sink 2A, and the low-side gate drivers (DL_) source 1.7A and sink 3.3A. This ensures robust gate drive for high-current applications. The DH_ floating high-side MOSFET drivers are powered by charge pumps at BST_ while the DL_ synchronous-rectifier drivers are powered directly by the fixed 5V linear regulator (LDO5).

Adaptive dead-time circuits monitor the DL_ and DH_ drivers and prevent either FET from turning on until the other is fully off. The adaptive driver dead time allows operation without shoot-through with a wide range of MOSFETs, minimizing delays and maintaining efficiency. There must be a low-resistance, low-inductance path from the DL_ and DH_ drivers to the MOSFET gates for the adaptive dead-time circuits to work properly; otherwise, the sense circuitry in the MAX17003A/MAX17004A interprets the MOSFET gates as "off" while charge actually remains. Use very short, wide traces (50 mils to 100 mils wide if the MOSFET is 1in from the driver).

The internal pulldown transistor that drives DL_ low is robust, with a 0.6Ω (typ) on-resistance. This helps prevent DL_ from being pulled up due to capacitive coupling from the drain to the gate of the low-side MOSFETs when the inductor node (LX_) quickly switches from ground to V_{IN}. Applications with high input voltages and long inductive driver traces may require additional gate-to-source capacitance to ensure fast-rising LX_ edges do not pull up the low-side MOSFET's gate, causing shoot-through currents. The capacitive coupling between LX_ and DL_ created by the MOSFET's gate-to-drain capacitance ($C_{GD} = C_{RSS}$), gate-to-source capacitance ($C_{GS} = C_{ISS} - C_{GD}$), and additional board parasitics should not exceed the following minimum threshold:

$$V_{GS(TH)} > V_{IN}\left(\frac{C_{RSS}}{C_{ISS}}\right)$$

Lot-to-lot variation of the threshold voltage may cause problems in marginal designs.

Power-Good Output (PGDALL)

PGDALL is the open-drain output of a comparator that continuously monitors both SMPS output voltages for undervoltage conditions. PGDALL is actively held low in shutdown ($\overline{SHDN}$ = GND), during soft-start, and soft discharge, and when either SMPS is disabled (either ON3 or ON5 low). Once the soft-start sequence terminates,

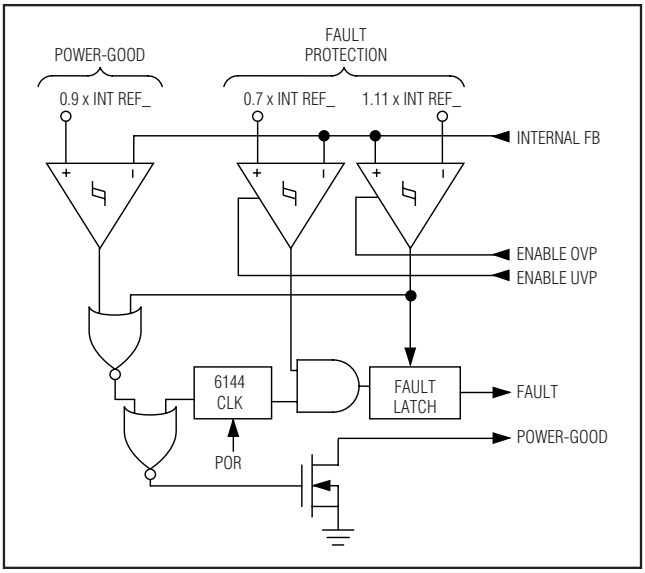

Figure 6. Power-Good and Fault Protection

Table 5. Operating Modes Truth Table

MODE	CONDITION	COMMENT
Power-Up	LDO5 < UVLO threshold	Transitions to discharge mode after V_{IN} POR and after REF becomes valid. LDO5, REF remain active. DL_ is low.
Run	$\overline{SHDN}$ = high, ON3 or ON5 enabled	Normal operation.
Output Overvoltage (OVP) Protection (MAX17003A)	Either output > 111% of nominal level	Exited by POR or cycling $\overline{SHDN}$, ON3, or ON5.
Output Undervoltage Protection (UVP)	Either output < 70% of nominal level, UVP is enabled 6144 clock cycles ($1/f_{OSC}$) after the output is enabled	Exited by POR or cycling $\overline{SHDN}$, ON3, or ON5.
Standby	ON5 and ON3 < startup threshold, $\overline{SHDN}$ = high	DL_ stays low. LDO5 active.
Shutdown	$\overline{SHDN}$ = low	All circuitry off.
Thermal Shutdown	T_J > +160°C	Exited by POR or cycling $\overline{SHDN}$, ON3, or ON5. DL3 and DL5 go low before LDO5 turns off.
Switchover Fault	Excessive current on LDO5 switchover transistors	Exited by POR or cycling $\overline{SHDN}$, ON3, or ON5.

PGDALL becomes high impedance as long as both SMPS outputs are above 90% of the nominal regulation voltage set by FB_. PGDALL goes low once either the SMPS output drops 10% below its nominal regulation point, an SMPS output overvoltage fault occurs, or ON_ or $\overline{SHDN}$ is low. For a logic-level PGDALL output voltage, connect an external pullup resistor between PGDALL and LDO5. A 100kΩ pullup resistor works well in most applications (see Table 5).

Fault Protection

Output Overvoltage Protection (OVP)—MAX17003A Only

If the output voltage of either SMPS rises above 111% of its nominal regulation voltage and the OVP protection is enabled, the controller sets the fault latch, pulls PGDALL low, shuts down the SMPS controllers that tripped the fault, and immediately pulls DH_ low and forces DL_ high. This turns on the synchronous-rectifier MOSFETs with 100% duty, rapidly discharging the output capacitors and clamping both outputs to ground. However, immediately latching DL_ high typically causes slightly negative output voltages due to the energy stored in the output LC at the instant the OVP occurs. If the load cannot tolerate a negative voltage, place a power Schottky diode across the output to act as a reverse-polarity clamp. If the condition that caused the overvoltage persists (such as a shorted high-side MOSFET), the battery blows. The other output is shut down using the soft-discharge feature with DL_ forced low. Cycle LDO5 below 1V or toggle either ON3, ON5, or $\overline{SHDN}$ to clear the fault latch and restart the SMPS controllers.

Output Undervoltage Protection (UVP)

Each SMPS controller includes an output UVP protection circuit that begins to monitor the output 6144 clock cycles ($1/f_{OSC}$) after that output is enabled (ON_ pulled high). If either SMPS output voltage drops below 70% of its nominal regulation voltage and the UVP protection is enabled, the UVP circuit sets the fault latch, pulls PGDALL low, and shuts down both controllers using the soft-discharge feature with DL_ forced low. Cycle LDO5 below 1V or toggle either ON3, ON5, or $\overline{SHDN}$ to clear the fault latch and restart the SMPS controllers.

Thermal-Fault Protection

The MAX17003A/MAX17004A feature a thermal-fault-protection circuit. When the junction temperature rises above +160°C, a thermal sensor activates the fault latch, pulls PGDALL low, and shuts down both SMPS controllers using the soft-discharge feature with DL_ forced low. Toggle either ON3, ON5, or $\overline{SHDN}$ to clear the fault latch and restart the controllers after the junction temperature cools by 15°C.

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Auxiliary LDO Detailed Description

The MAX17003A/MAX17004A include an auxiliary linear regulator (OUTA) that can be configured for 12V, ideal for PCMCIA power requirements, and for biasing the gates of load switches in a portable device. OUTA can also be configured for outputs from 1V to 23V. The auxiliary regulator has an independent ON/OFF control, allowing it to be shut down when not needed, reducing power consumption when the system is in a low-power state.

A flyback-winding control loop regulates a secondary winding output, improving cross-regulation when the primary output is lightly loaded or when there is a low input-output differential voltage. If $V_{DRVA} < V_{OUTA}$, the low-side switch is turned on for a time equal to 33% of the switching period. This reverses the inductor (primary) current, pulling current from the output filter capacitor and causing the flyback transformer to operate in forward mode. The low impedance presented by the transformer secondary in forward mode dumps current into the secondary output, charging up the secondary capacitor and bringing V_{INA} - V_{OUTA} back into regulation. The secondary feedback loop does not improve secondary output accuracy in normal flyback mode, where the main (primary) output is heavily loaded. In this condition, secondary output accuracy is determined by the secondary rectifier drop, transformer turns ratio, and accuracy of the main output voltage.

SMPS Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

- **Input Voltage Range.** The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case, high AC-adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest battery voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.
- **Maximum Load Current.** There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components.
- **Switching Frequency.** This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage, due to MOSFET switching losses that are proportional to frequency and V_{IN}^2. The optimum frequency is also a moving target, due to rapid improvements in MOSFET technology that are making higher frequencies more practical.
- **Inductor Operating Point.** This choice provides trade-offs between size vs. efficiency and transient response vs. output ripple. Low inductor values provide better transient response and smaller physical size, but also result in lower efficiency and higher output ripple due to increased ripple currents. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 20% and 50% ripple current. When pulse skipping ($\overline{SKIP}$ low and light loads), the inductor value also determines the load-current value at which PFM/PWM switchover occurs.

Inductor Selection

The switching frequency and inductor operating point determine the inductor value as follows:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} f_{OSC} I_{LOAD(MAX)} LIR}$$

For example: $I_{LOAD(MAX)}$ = 5A, V_{IN} = 12V, V_{OUT} = 5V, f_{OSC} = 300kHz, 30% ripple current or LIR = 0.3:

$$L = \frac{5V \times (12V - 5V)}{12V \times 300kHz \times 5A \times 0.3} = 6.50\mu H$$

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Most inductor manufacturers provide inductors in standard values, such as 1.0µH, 1.5µH, 2.2µH, 3.3µH, etc. Also look for nonstandard values, which can provide a better compromise in LIR across the input voltage range. If using a swinging inductor (where the no-load inductance decreases linearly with increasing current), evaluate the LIR with properly scaled inductance values. For the selected inductance value, the actual peak-to-peak inductor ripple current ($\Delta I_{INDUCTOR}$) is defined by:

$$\Delta I_{INDUCTOR} = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} f_{OSC} L}$$

Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{\Delta I_{INDUCTOR}}{2}$$

Transformer Design (for MAX17003A/MAX17004A Auxiliary Output)

A coupled inductor or transformer can be substituted for the inductor in the 5V SMPS to create an auxiliary output (Figure 1). The MAX17003A/MAX17004A are particularly well suited for such applications because the secondary feedback threshold automatically triggers DL5 even if the 5V output is lightly loaded.

The power requirements of the auxiliary supply must be considered in the design of the main output. The transformer must be designed to deliver the required current in both the primary and the secondary outputs with the proper turns ratio and inductance. The power ratings of the synchronous-rectifier MOSFETs and the current limit in the MAX17003A/MAX17004A must also be adjusted accordingly. Extremes of low input-output differentials, widely different output loading levels, and high turns ratios can further complicate the design due to parasitic transformer parameters such as interwinding capacitance, secondary resistance, and leakage inductance. Power from the main and secondary outputs is combined to get an equivalent current referred to the main output. Use this total current to determine the current limit (see the *Setting the Current Limit* section):

$$I_{TOTAL} = P_{TOTAL}/V_{OUT5}$$

where I_{TOTAL} is the equivalent output current referred to the main output, and P_{TOTAL} is the sum of the output power from both the main output and the secondary output:

$$N = \frac{V_{SEC} + V_{FWD}}{V_{OUT5} + V_{RECT} + V_{SENSE}}$$

where N is the transformer turns ratio, V_{SEC} is the minimum required rectified secondary voltage, V_{FWD} is the forward drop across the secondary rectifier, $V_{OUT5(MIN)}$ is the minimum value of the main output voltage, and V_{RECT} is the on-state voltage drop across the synchronous-rectifier MOSFET. The transformer secondary return is often connected to the main output voltage instead of ground to reduce the necessary turns ratio. In this case, subtract V_{OUT5} from the secondary voltage (V_{SEC} - V_{OUT5}) in the transformer turns-ratio equation above. The secondary diode in coupled-inductor applications must withstand flyback voltages greater than 60V. Common silicon rectifiers, such as the 1N4001, are also prohibited because they are too slow. Fast silicon rectifiers, such as the MURS120, are the only choice. The flyback voltage across the rectifier is related to the V_{IN} - V_{OUT5} difference, according to the transformer turns ratio:

$$V_{FLYBACK} = V_{SEC} + (V_{IN} - V_{OUT5}) \times N$$

where N is the transformer turns ratio (secondary windings/primary windings), and V_{SEC} is the maximum secondary DC output voltage. If the secondary winding is returned to V_{OUT5} instead of ground, subtract V_{OUT5} from $V_{FLYBACK}$ in the equation above. The diode's reverse breakdown voltage rating must also accommodate any ringing due to leakage inductance. The diode's current rating should be at least twice the DC load current on the secondary output.

Transient Response

The inductor ripple current also impacts transient-response performance, especially at low V_{IN} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The total output-voltage sag is the sum of the voltage sag while the inductor is ramping up, and the voltage sag before the next pulse can occur:

$$V_{SAG} = \frac{L\left(\Delta I_{LOAD(MAX)}\right)^2}{2C_{OUT}\left(V_{IN} \times D_{MAX} - V_{OUT}\right)} + \frac{\Delta I_{LOAD(MAX)}\left(t - \Delta t\right)}{C_{OUT}}$$

where D_{MAX} is the maximum duty factor (see the *Electrical Characteristics* table), t is the switching period ($1/f_{OSC}$), and Δt equals $V_{OUT}/V_{IN} \times t$ when in PWM mode, or $L \times 0.2 \times I_{MAX}/(V_{IN} - V_{OUT})$ when in skip mode. The amount of overshoot during a full-load to no-load transient due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{\left(\Delta I_{LOAD(MAX)}\right)^2 L}{2C_{OUT}V_{OUT}}$$

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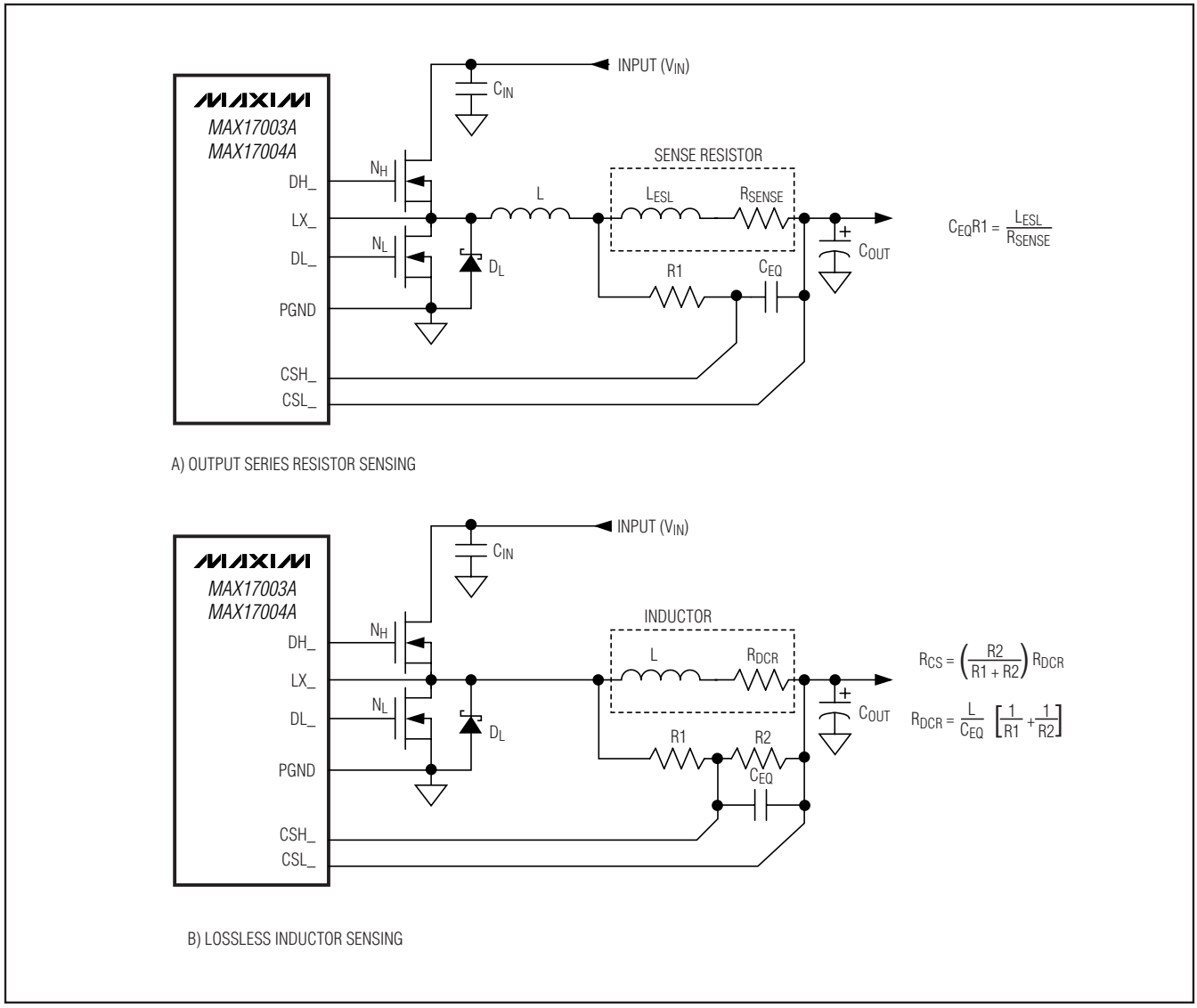

Figure 7. Current-Sense Configurations

Setting the Current Limit

The minimum current-limit threshold must be great enough to support the maximum load current when the current limit is at the minimum tolerance value. The peak inductor current occurs at $I_{LOAD(MAX)}$ plus half the ripple current; therefore:

$$I_{LIMIT} > I_{LOAD(MAX)} + \left(\frac{\Delta I_{INDUCTOR}}{2} \right)$$

where I_{LIMIT} equals the minimum current-limit threshold voltage divided by the current-sense resistance ($R_{SENSE\_}$). For the default setting, the minimum current-limit threshold is 45mV.

Connect ILIM to LDO5 for a default 50mV current-limit threshold. In adjustable mode, the current-limit threshold is precisely 1/10 the voltage seen at ILIM. For an adjustable threshold, connect a resistive divider from REF to analog ground (GND) with ILIM connected to the center tap. The external 0.5V to 2V adjustment range corresponds to a 50mV to 200mV current-limit threshold. When adjusting the current limit, use 1% tolerance resistors and a divider current of approximately 10mA to prevent significant inaccuracy in the current-limit tolerance.

The current-sense method (Figure 7) and magnitude determines the achievable current-limit accuracy and power loss. Typically, higher current-sense limits provide tighter accuracy, but also dissipate more power. Most applications employ a current-limit threshold (V_{LIMIT}) of 50mV to 100mV, so the sense resistor can be determined by:

$$R_{CS} = \frac{V_{LIMIT}}{I_{LIMIT}} = \frac{V_{ILIM}}{10 \times I_{LIMIT}}$$

For the best current-sense accuracy and overcurrent protection, use a 1% tolerance current-sense resistor between the inductor and output as shown in Figure 7A. This configuration constantly monitors the inductor current, allowing accurate current-limit protection. However, the parasitic inductance of the current-sense resistor can cause current-limit inaccuracies, especially when using low-value inductors and current-sense resistors. This parasitic inductance (L_{ESL}) can be canceled by adding an RC circuit across the sense resistor with an equivalent time constant:

$$C_{EQ}R1 = \frac{L_{ESL}}{R_{SENSE}}$$

Alternatively, high-power applications that do not require highly accurate current-limit protection may reduce the overall power dissipation by connecting a series RC circuit across the inductor (Figure 7B) with an equivalent time constant:

$$R_{CS} = \left(\frac{R2}{R1 + R2} \right) R_{DCR}$$

and:

$$R_{DCR} = \frac{L}{C_{EQ}} \left[\frac{1}{R1} + \frac{1}{R2} \right]$$

where R_{CS} is the required current-sense resistance, and R_{DCR} is the inductor's series DC resistance. Use the typical inductance and R_{DCR} values provided by the inductor manufacturer.

Output Capacitor Selection

The output filter capacitor must have low enough equivalent series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. The output capacitance must be high enough to absorb the inductor energy while transitioning from full-load to no-load conditions without tripping the overvoltage fault protection. When using high-capacitance, low-ESR capacitors (see stability requirements), the filter capacitor's ESR dominates the output voltage ripple. So the output capacitor's size depends on the maximum ESR required to meet the output voltage ripple ($V_{RIPPLE(P-P)}$) specifications:

$$V_{RIPPLE(P-P)} = R_{ESR}I_{LOAD(MAX)}LIR$$

In idle-mode, the inductor current becomes discontinuous, with peak currents set by the idle-mode current-sense threshold (V_{IDLE} = 0.2V_{LIMIT}). In idle-mode, the no-load output ripple can be determined as follows:

$$V_{RIPPLE(P-P)} = \frac{V_{IDLE}R_{ESR}}{R_{SENSE}}$$

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The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of tantalums, OS-CONs, polymers, and other electrolytics). When using low-capacity filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the V_{SAG} and V_{SOAR} equations in the *Transient Response* section). However, low-capacity filter capacitors typically have high ESR zeros that may affect the overall stability (see the *Output-Capacitor Stability Considerations* section).

Output-Capacitor Stability Considerations

Stability is determined by the value of the ESR zero relative to the switching frequency. The boundary of instability is given by the following equation:

$$f_{ESR} \le \frac{f_{OSC}}{\pi}$$

where:

$$f_{ESR} = \frac{1}{2\pi R_{ESR} C_{OUT}}$$

For a typical 300kHz application, the ESR zero frequency must be well below 95kHz, preferably below 50kHz. Tantalum and OSCON capacitors in widespread use at the time of publication have typical ESR zero frequencies of 25kHz. In the design example used for inductor selection, the ESR needed to support $25mV_{P-P}$ ripple is 25mV/1.5A = 16.7mΩ. One 220µF/4V SANYO polymer (TPE) capacitor provides 15mΩ (max) ESR. This results in a zero at 48kHz, well within the bounds of stability.

For low-input-voltage applications where the duty cycle exceeds 50% ($V_{OUT}/V_{IN} \ge 50\%$), the output ripple voltage should not be greater than twice the internal slope-compensation voltage:

$$V_{RIPPLE} \le 0.02 \times V_{OUT}$$

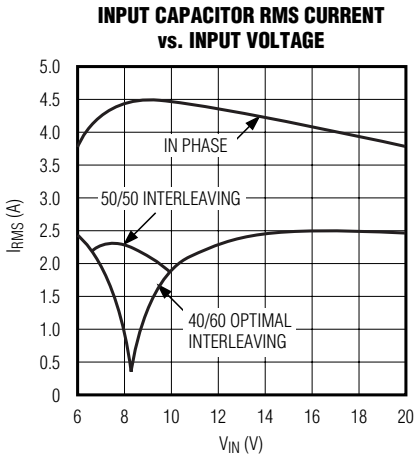
where V_{RIPPLE} equals $\Delta I_{INDUCTOR} \times R_{ESR}$. The worst-case ESR limit occurs when $V_{IN} = 2 \times V_{OUT}$, so the above equation can be simplified to provide the following boundary condition:

$$R_{ESR} \le 0.04 \times L \times f_{SW}$$

Do not put high-value ceramic capacitors directly across the feedback sense point without taking precautions to ensure stability. Large ceramic capacitors can have a high ESR zero frequency and cause erratic, unstable operation. However, it is easy to add enough series resistance by placing the capacitors a couple of inches downstream from the feedback sense point, which should be as close as possible to the inductor.

Unstable operation manifests itself in two related but distinctly different ways: short/long pulses and cycle skipping resulting in lower frequency operation. Instability occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output voltage signal. This “fools” the error comparator into triggering too early or into skipping a cycle. Cycle skipping is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability due to insufficient ESR. Loop instability can result in oscillations at the output after line or load steps. Such perturbations are usually damped, but can cause the output voltage to rise above or fall below the tolerance limits.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output-voltage-ripple envelope for overshoot and ringing. It may help to simultaneously monitor the inductor current with an AC current probe. Do not allow more than three cycles of ringing after the initial step-response under/overshoot.



INPUT RMS CURRENT FOR INTERLEAVED OPERATION:

$$I_{RMS} = \sqrt{(I_{OUT5} - I_{IN})^2 (D_{LX5} - D_{OL}) + (I_{OUT3} - I_{IN})^2 (D_{LX3} - D_{OL}) + (I_{OUT5} + I_{OUT3} - I_{IN})^2 D_{OL} + I_{IN}^2 (1 - D_{LX5} - D_{LX3} + D_{OL})}$$

$$D_{LX5} = \frac{V_{OUT5}}{V_{IN}} \qquad D_{LX3} = \frac{V_{OUT3}}{V_{IN}} \qquad D_{OL} = \text{DUTY – CYCLE OVERLAP FRACTION}$$

$$I_{IN} = \frac{V_{OUT5} I_{OUT5} + V_{OUT3} I_{OUT3}}{V_{IN}}$$

INPUT RMS CURRENT FOR SINGLE-PHASE OPERATION:

$$I_{RMS} = I_{LOAD} \left(\frac{\sqrt{V_{OUT} (V_{IN} - V_{OUT})}}{V_{IN}} \right)$$

Figure 8. Input RMS Current

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. For an out-of-phase regulator, the total RMS current in the input capacitor is a function of the load currents, the input currents, the duty cycles, and the amount of overlap as defined in Figure 8.

The 40/60 optimal interleaved architecture of the MAX17003A/MAX17004A allows the input voltage to go as low as 8.3V before the duty cycles begin to overlap. This offers improved efficiency over a regular 180° out-of-phase architecture where the duty cycles begin to overlap below 10V. Figure 8 shows the input-capacitor RMS current vs. input voltage for an application that requires 5V/5A and 3.3V/5A. This shows the improvement of the 40/60 optimal interleaving over 50/50 interleaving and in-phase operation.

For most applications, nontantalum chemistries (ceramic, aluminum, or OSCON) are preferred due to their resistance to power-up surge currents typical of systems with a mechanical switch or connector in series with the input. Choose a capacitor that has less than 10°C temperature rise at the RMS input current for optimal reliability and lifetime.

Power-MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability when using high-voltage (> 20V) AC adapters. Low-current applications usually require less attention.

The high-side MOSFET (N_H) must be able to dissipate the resistive losses plus the switching losses at both $V_{IN(MIN)}$ and $V_{IN(MAX)}$. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to the losses at $V_{IN(MAX)}$, with

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lower losses in between. If the losses at $V_{IN(MIN)}$ are significantly higher, consider increasing the size of N_H. Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher, consider reducing the size of N_H. If V_{IN} does not vary over a wide range, maximum efficiency is achieved by selecting a high-side MOSFET (N_H) that has conduction losses equal to the switching losses.

Choose a low-side MOSFET (N_L) that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., 8-pin SO, DPAK, or D^2PAK), and is reasonably priced. Ensure that the MAX17003A/MAX17004A DL_ gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic drain-to-gate capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems may occur. Switching losses are not an issue for the low-side MOSFET since it is a zero-voltage switched device when used in the step-down topology.

Power-MOSFET Dissipation

Worst-case conduction losses occur at the duty-factor extremes. For the high-side MOSFET (N_H), the worst-case power dissipation due to resistance occurs at minimum input voltage:

$$PD\left(N_H\ Resistive\right) = \left(\frac{V_{OUT}}{V_{IN}}\right)\left(I_{LOAD}\right)^2 R_{DS(ON)}$$

Generally, use a small high-side MOSFET to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power-dissipation limits often limits how small the MOSFET can be. The optimum occurs when the switching losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses do not become an issue until the input is greater than approximately 15V.

Calculating the power dissipation in high-side MOSFETs (N_H) due to switching losses is difficult, since it must allow for difficult-to-quantify factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PCB layout characteristics. The following switching-loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on N_H:

$$PD\left(N_H\ Resistive\right) = \left(\frac{I_{LOAD} Q_{G(SW)}}{I_{GATE}} + \frac{C_{OSS} V_{IN(MAX)}}{2}\right) V_{IN(MAX)} f_{SW}$$

where C_{OSS} is the output capacitance of N_H, $Q_{G(SW)}$ is the charge needed to turn on the N_H MOSFET, and I_{GATE} is the peak gate-drive source/sink current (1A, typ).

Switching losses in the high-side MOSFET can become a heat problem when maximum AC adapter voltages are applied, due to the squared term in the switching-loss equation ($C \times V_{IN}^2 \times f_{SW}$). If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low battery voltages becomes extraordinarily hot when subjected to $V_{IN(MAX)}$, consider choosing another MOSFET with lower parasitic capacitance.

For the low-side MOSFET (N_L), the worst-case power dissipation always occurs at maximum battery voltage:

$$PD\left(N_L\ Resistive\right) = \left[1 - \left(\frac{V_{OUT}}{V_{IN(MAX)}}\right)\right]\left(I_{LOAD}\right)^2 R_{DS(ON)}$$

The absolute worst case for MOSFET power dissipation occurs under heavy overload conditions that are greater than $I_{LOAD(MAX)}$ but are not high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, "overdesign" the circuit to tolerate:

$$I_{LOAD} = I_{LIMIT} - \left(\frac{\Delta I_{INDUCTOR}}{2}\right)$$

where I_{LIMIT} is the peak current allowed by the current-limit circuit, including threshold tolerance and sense-resistance variation. The MOSFETs must have a relatively large heatsink to handle the overload power dissipation.

Choose a Schottky diode (D_L) with a forward-voltage drop low enough to prevent the low-side MOSFET's body diode from turning on during the dead time. As a general rule, select a diode with a DC current rating equal to 1/3 the load current. This diode is optional and can be removed if efficiency is not critical.

Boost Capacitors

The boost capacitors (C_{BST}) must be selected large enough to handle the gate-charging requirements of the high-side MOSFETs. Typically, 0.1µF ceramic capacitors work well for low-power applications driving medium-sized MOSFETs. However, high-current applications driving large, high-side MOSFETs require boost capacitors larger than 0.1µF. For these applications, select the boost capacitors to avoid discharging the capacitor more than 200mV while charging the high-side MOSFETs' gates:

$$C_{BST} = \frac{Q_{GATE}}{200mV}$$

where Q_{GATE} is the total gate charge specified in the high-side MOSFET's data sheet. For example, assume the FDS6612A n-channel MOSFET is used on the high side. According to the manufacturer's data sheet, a single FDS6612A has a maximum gate charge of 13nC (V_{GS} = 5V). Using the above equation, the required boost capacitance would be:

$$C_{BST} = \frac{13nC}{200mV} = 0.065\mu F$$

Selecting the closest standard value, this example requires a 0.1µF ceramic capacitor.

LDOA Design Procedure

Output Voltage Selection

Adjust the auxiliary linear regulator's output voltage by connecting a resistive divider between OUTA and analog ground with the center tap connected to FBA (Figure 1). Select R6 in the 10kΩ to 30kΩ range, and calculate R5 with the following equation:

$$R5 = R6\left(\frac{V_{OUTA}}{V_{FBA}} - 1\right)$$

where V_{FBA} = 1.0V.

Transistor Selection

The pass transistor must meet specifications for current gain (β), input capacitance, collector-emitter saturation voltage, and power dissipation. The transistor's current gain limits the guaranteed maximum output current to:

$$I_{LOAD(MAX)} = \left(I_{DRV} - \frac{V_{BE}}{R_{BE}}\right)\beta_{MIN}$$

where I_{DRV} is the minimum guaranteed base drive current, V_{BE} is the base-to-emitter voltage of the transistor, and R_{BE} is the pullup resistor connected between the transistor's base and emitter. Furthermore, the transistor's current gain increases the linear regulator's DC loop gain (see the *LDOA Stability Requirements* section), so excessive gain destabilizes the output. Therefore, transistors with current gain over 100 at the maximum output current can be difficult to stabilize and are not recommended. The transistor's input capacitance and input resistance also create a second pole, which could be low enough to make the output unstable when heavily loaded.

The transistor's saturation voltage at the maximum output current determines the minimum input-to-output voltage differential that the linear regulator supports. Alternatively, the package's power dissipation could limit the usable maximum input-to-output voltage differential. The maximum power dissipation capability of the transistor's package and mounting must exceed the actual power dissipation in the device. The power dissipation equals the maximum load current times the maximum input-to-output differential:

$$PWR = I_{LOAD(MAX)} (V_{INA} - V_{OUTA})$$

$$PWR = I_{LOAD(MAX)} V_{CE}$$

LDOA Stability Requirements

The MAX17003A/MAX17004A linear-regulator controller uses an internal transconductance amplifier to drive an external pnp pass transistor. The transconductance amplifier, the pass transistor, the base-to-emitter resistor, and the output capacitor determine the loop stability.

The transconductance amplifier regulates the output voltage by controlling the pass transistor's base current. The total DC loop gain is approximately:

$$A_{V(LDO)} = \left(\frac{5.5V}{V_T}\right)\left(1 + \frac{I_{BIAS}h_{FE}}{I_{LOAD}}\right)$$

where V_T is 26mV at room temperature, h_{FE} is the pass transistor's DC gain, and I_{BIAS} is the current through the base-to-emitter resistor (R_{BE}). The 680Ω base-to-emitter resistor used in Figure 1 was chosen to provide a 1mA bias current (I_{BIAS}).

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The output capacitor and the load resistance create the dominant pole in the system. However, the internal amplifier delay, the pass transistor's input capacitance, and the stray capacitance at the feedback node create additional poles in the system, and the output capacitor's ESR generates a zero. For proper operation, use the following steps to ensure the linear-regulator stability:

1) First, calculate the dominant pole set by the linear regulator's output capacitor and the load resistor:

$$f_{POLE(LDO)} = \frac{1}{2\pi C_{OUTA} R_{LOAD}}$$

where C_{OUTA} is the output capacitance of the auxiliary LDO and R_{LOAD} is the load resistance corresponding to the maximum load current. The unity-gain crossover of the linear regulator is:

$$f_{CROSSOVER} = A_{V(LDO)} f_{POLE(LDO)}$$

2) The pole caused by the internal amplifier delay is at approximately 1MHz:

$$f_{POLE(AMP)} \approx 1MHz$$

3) Next, calculate the pole set by the transistor's input capacitance, the transistor's input resistance, and the base-to-emitter pullup resistor. Since the transistor's input resistance (h_{FE}/g_m) is typically much greater than the base-to-emitter pullup resistance, the pole can be determined from the simplified equation:

$$f_{POLE(CIN)} \approx \frac{1}{2\pi C_{IN} R_{IN}}$$

$$C_{IN} = \frac{g_m}{2\pi f_T}$$

where g_m is the transconductance of the pass transistor, and f_T is the transition frequency. Both parameters can be found in the transistor's data sheet. Therefore, the equation can be further reduced to:

$$f_{POLE(CIN)} \approx \frac{f_T}{h_{FE}}$$

4) Next, calculate the pole set by the linear regulator's feedback resistance and the capacitance between FBA and ground (approximately 5pF including stray capacitance):

$$f_{POLE(FBA)} = \frac{1}{2\pi C_{FBA}(R5 \parallel R6)}$$

5) Next, calculate the zero caused by the output capacitor's ESR:

$$f_{ZERO(ESR)} = \frac{1}{2\pi C_{OUTA} R_{ESR}}$$

where R_{ESR} is the equivalent series resistance of C_{OUTA}.

6) To ensure stability, choose C_{OUTA} large enough so that the crossover occurs well before the poles and zero calculated in steps 2 through 5. The poles in steps 3 and 4 generally occur at several MHz, and using ceramic output capacitors ensures the ESR zero occurs at several MHz as well. Placing the crossover frequency below 500kHz is typically sufficient to avoid the amplifier delay pole and generally works well, unless unusual component selection or extra capacitance moves the other poles or zero below 1MHz.

A capacitor connected between the linear regulator's output and the feedback node can improve the transient response and reduce the noise coupled into the feedback loop.

If a low-dropout solution is required, an external p-channel MOSFET pass transistor could be used. However, a pMOS-based linear regulator requires higher output capacitance to stabilize the loop. The high gate capacitance of the p-channel MOSFET lowers the $f_{POLE(CIN)}$ and can cause instability. A large output capacitance must be used to reduce the unity-gain bandwidth and ensure that the pole is well above the unity-gain crossover frequency.

Applications Information

Duty-Cycle Limits

Minimum Input Voltage

The minimum input operating voltage (dropout voltage) is restricted by the maximum duty-cycle specification (see the *Electrical Characteristics* table). Keep in mind that the transient performance gets worse as the step-down regulators approach the dropout voltage, so bulk output capacitance must be added (see the voltage sag and soar equations in the *Transient Response* section of the *SMPS Design Procedure* section). The absolute point of dropout occurs when the inductor current ramps down during the off-time (ΔI_{DOWN}) as much as it ramps up during the on-time (ΔI_{UP}). This results in a minimum operating voltage defined by the following equation:

$$V_{IN(MIN)} = V_{OUT} + V_{CHG} + h\left(\frac{1}{D_{MAX}} - 1\right)(V_{OUT} + V_{DIS})$$

where V_{CHG} and V_{DIS} are the parasitic voltage drops in the charge and discharge paths, respectively. A reasonable minimum value for h is 1.5, while the absolute minimum input voltage is calculated with h = 1.

Maximum Input Voltage

The MAX17003A/MAX17004A controllers include a minimum on-time specification, which determines the maximum input operating voltage that maintains the selected switching frequency (see the *Electrical Characteristics* table). Operation above this maximum input voltage results in pulse-skipping operation, regardless of the operating mode selected by $\overline{SKIP}$. At the beginning of each cycle, if the output voltage is still above the feedback threshold voltage, the controller does not trigger an on-time pulse, effectively skipping a cycle. This allows the controller to maintain regulation above the maximum input voltage, but forces the controller to effectively operate with a lower switching frequency. This results in an input threshold voltage at which the controller begins to skip pulses ($V_{IN(SKIP)}$):

$$V_{IN(SKIP)} = V_{OUT}\left(\frac{1}{f_{OSC}t_{ON(MIN)}}\right)$$

where f_{OSC} is the switching frequency selected by FSEL.

PCB Layout Guidelines

Careful PCB layout is critical to achieving low switching losses and clean, stable operation. The switching power stage requires particular attention (Figure 9). If possible, mount all the power components on the top side of the board, with their ground terminals flush against one another. Follow these guidelines for good PCB layout:

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Using thick copper PCB (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PCB traces is a difficult task that must be approached in terms of fractions of centimeters, where a single milliohm of excess trace resistance causes a measurable efficiency penalty.
- Minimize current-sensing errors by connecting CSH_ and CSL_ directly across the current-sense resistor ($R_{SENSE\_}$).
- When trade-offs in trace lengths must be made, it is preferable to allow the inductor charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
- Route high-speed switching nodes (BST_, LX_, DH_, and DL_) away from sensitive analog areas (REF, FB_, CSH_, CSL_).

Layout Procedure

Place the power components first, with ground terminals adjacent ($N_{L\_}$ source, C_{IN}, $C_{OUT\_}$, and $D_{L\_}$ anode). If possible, make all these connections on the top layer with wide, copper-filled areas.

Mount the controller IC adjacent to the low-side MOSFET, preferably on the back side opposite $N_{L\_}$ and $N_{H\_}$ to keep LX_, GND, and the DH_ and the DL_ gate-drive lines short and wide. The DL_ and DH_ gate traces must be short and wide (50 mils to 100 mils wide if the MOSFET is 1in from the controller IC) to keep the driver impedance low and for proper adaptive dead-time sensing.

Group the gate-drive components (BST_ capacitor, LDO5 bypass capacitor) together near the controller IC.

Make the DC-DC controller ground connections as shown in Figures 1 and 9. This diagram can be viewed as having two separate ground planes: power ground, where all the high-power components go, and an analog ground plane for sensitive analog components. The analog ground plane and power ground plane must meet only at a single point directly at the IC.

Connect the output power planes directly to the output filter capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the load as is practical.

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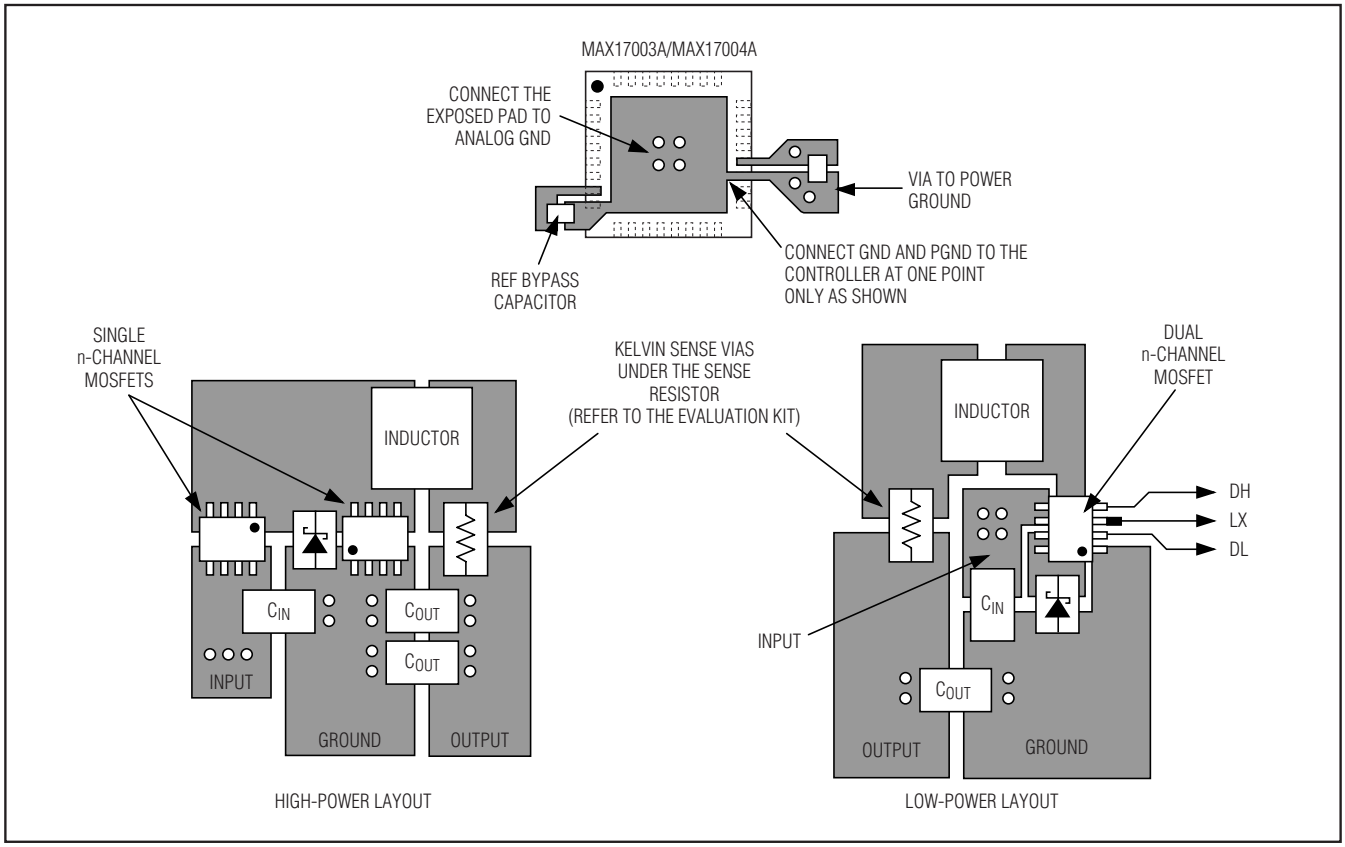


Figure 9. PCB Layout

FEATURE	MAX8744/MAX8745	MAX17003A/MAX17004A
Startup	Startup operating mode depends on the SKIP# setting. (e.g., $\overline{SKIP}$ is low, then startup occurs in skip mode).	Startup is **always** in low-noise pulse-skipping mode (i.e., same as $\overline{SKIP}$ = REF setting). This allows for startup into prebiased outputs. The $\overline{SKIP}$ setting takes effect once the SMPS is in regulation.
Shutdown	Actively discharges the output down to zero.	Soft discharge of the output using the DSCHG3 and DSCHG5 pins.
DL3 and DL5 States	DL3 and DL5 are high in shutdown. DL3 and DL5 are latched high during an OV fault of the respective output (MAX8744 only).	DL3 and DL5 are low in shutdown. DL3 and DL5 are latched high during an OV fault of the respective output (MAX17003A only).
Power-Good	PGOOD3: Power-good indicator for SMPS3.	PGDALL: Power-good indicator for SMPS3 and SMPS5.
	PGOOD5: Power-good indicator for SMPS5. PGOODA: Power-good indicator for the auxiliary LDO.	Auxiliary LDO does not have power-good indicator.

Chip Information

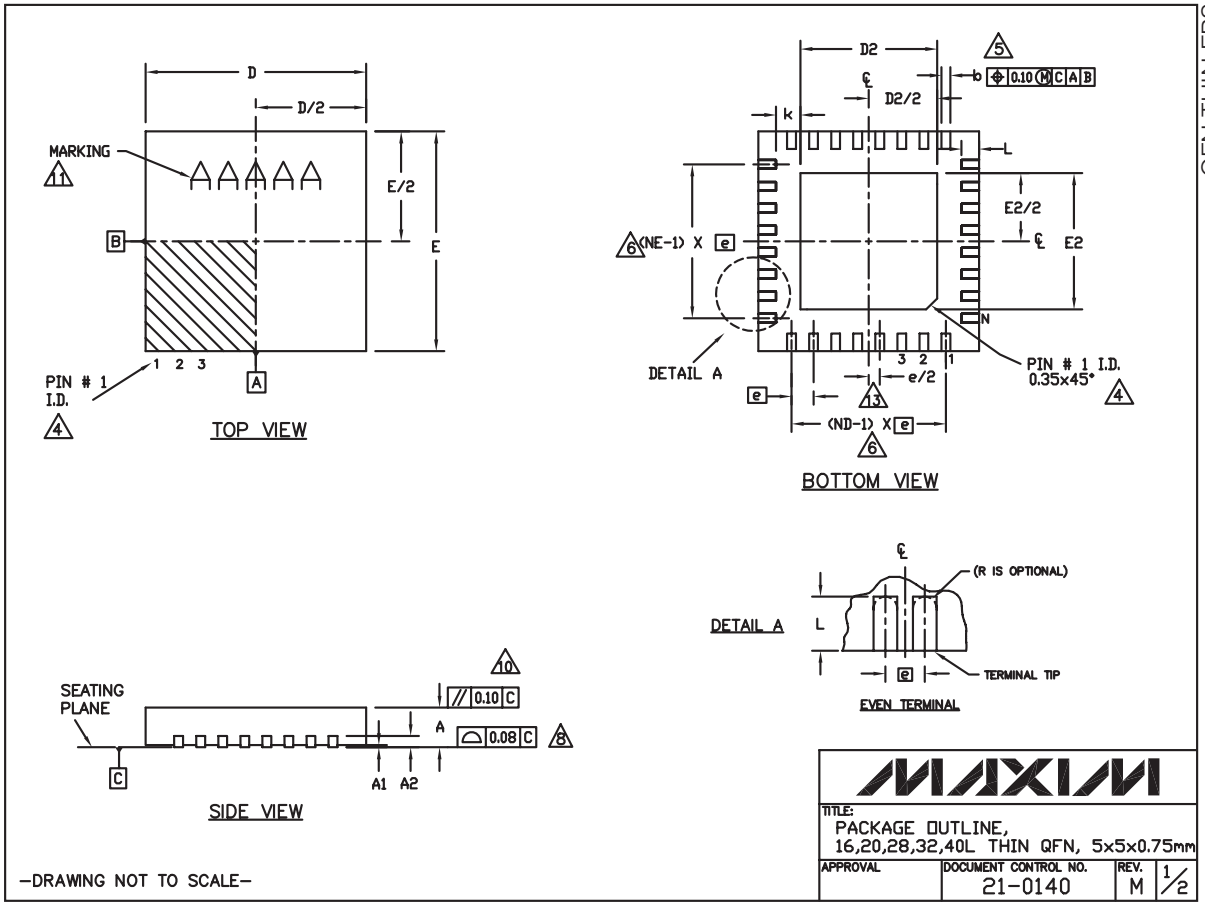
TRANSISTOR COUNT: 6897

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS																
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5			
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25	
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.			
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50	
N	16			20			28			32			40			
ND	4			5			7			8			10			
NE	4			5			7			8			10			
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----			

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655-4	2.19	2.29	2.39	2.19	2.29	2.39
T165N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055MN-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255M-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60
T4055N-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055MN-1	3.40	3.50	3.60	3.40	3.50	3.60

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

–DRAWING NOT TO SCALE–

MAXIM

TITLE: PACKAGE OUTLINE, 16,20,28,32,40L THIN QFN, 5x5x0.75mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	M	2/2

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