19-5135; Rev 2; 3/12

EVALUATION KIT AVAILABLE

Integrated Charger, Dual Main Step-Down Controllers, and Dual LDO Regulators

MAX17085B

General Description

The MAX17085B is an all-in-one notebook power solution integrating a multichemistry battery charger, dual fixed-output Quick-PWM™ step-down controllers, and dual keep-alive linear regulators:

Charger: The high-frequency (~1.4MHz) multichemistry battery charger uses a current-mode, fixed inductor current ripple architecture that significantly reduces component size and cost. Low-offset sense amplifiers allow the use of low-value sense resistors for charging and input current limit.

The charger uses n-channel switching MOSFETs. Adjustable charge current, charge voltage, and cell selection allow for flexible use with different battery packs. Charge current is set by an analog control input, or a PWM input. High-accuracy current-sense amplifiers provide fast cycle-by-cycle current-mode control to protect against short circuits to the battery and respond quickly to system load transients. Additionally, the charger provides a high-accuracy analog output that is proportional to the adapter current.

An integrated charge pump controls an n-channel adapter selector switch. The charge pump remains active even when the charger is off. When the adapter is absent, a p-channel MOSFET selects the battery.

Main SMPS: The dual Quick-PWM step-down controllers with synchronous rectification generate the 5V and 3.3V main power in a notebook. Low-side MOSFET sensing provides a simple low-cost, highly efficient valley current-limit protection. The MAX17085B also includes output undervoltage, output overvoltage, and thermal-fault protection.

Separate enable inputs for each SMPS and a combined open-drain power-good output allow flexible power sequencing. Voltage soft-start reduces inrush current, while passive shutdown discharges the output through an internal switch. Fast transient response, with an extended on-time feature reduces output capacitance requirements. Selectable pulse-skipping mode and ultrasonic mode improve light-load efficiency. Ultrasonic mode operation maintains a minimum switching frequency at light loads, minimizing audible noise effects.

Dual LDO Regulators: An internal 5V/100mA LDO5 with switchover can be used to either generate the 5V bias needed for power-up or other lower power "always-on" suspend supplies. Another 3.3V/50mA LDO3 provides "always-on" power to a system microcontroller.

Features

- **All-in-One Charger Plus Dual Main Step-Down Controllers**
- **5V/100mA and 3.3V/50mA LDO Regulators**
- **Main**
  Dual Quick-PWM with Fast Transient Response and Extended On-Time
  300kHz to 800kHz Switching Frequency
  Fixed 5V and 3.3V SMPS Outputs
  Low-Noise Ultrasonic Mode
  Autoretry Fault Protection
- **Charger**
  High Switching Frequency (1.4MHz)
  Selectable 2-, 3-, and 4-Cell Battery Voltage
  Automatic Selection of System Power Source
  Internal Charge-Pump for Adapter n-Channel MOSFETs Drive
  ±0.4% Accurate Charge Voltage
  ±2.5% Accurate Input Current Limiting
  ±3% Accurate Charge Current
- **Monitor Outputs for**
  AC Adapter Current (±2% Accuracy)
  Battery Discharge Current (±2% Accuracy)
  AC Adapter OK
- **Analog/PWM (100Hz to 500kHz) Adjustable Charge Current Setting**
- **AC Adapter Overvoltage and Overcurrent Protection**

Applications

Notebook Computers

PDAs and Mobile Communicators

5V and 3.3V Supplies

2-to-4, Li+-Cell, Battery-Powered Devices

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17085BETL+	-40°C to +85°C	40 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Pin Configuration appears at end of data sheet.

Quick-PWM is a trademark of Maxim Integrated Products, Inc.

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ABSOLUTE MAXIMUM RATINGS (Note 1)

TON, DCIN, CSSP, BATT, CSIP to GND, LX_ to GND ..... -0.3V to +28V
CSIP to CSIN, CSSP to CSSN ..... -0.3V to +0.3V
LDO3, LDO5, VCC to GND (Note 2) ..... -0.3V to +6V
ISET, VCTL, ACIN, $\overline{ACOK}$ to GND ..... -0.3V to +6V
OUT3, OUT5 to GND (Note 2) ..... -0.3V to +6V
ON3, ON5, PGOOD to GND ..... -0.3V to +6V
ILIM3, ILIM5, SKIP, REF to GND ..... -0.3V to (V_{CC} + 0.3V)
GND to EP ..... -0.3V to +0.3V
DL_ to EP ..... -0.3V to (V_{LDO5} + 0.3V)
BST_ to GND ..... -0.3V to +34V
BST_ to LDO5 ..... -0.3V to +28V
DH3 to LX3 ..... -0.3V to (V_{BST3} + 0.3V)
BST3 to LX3 ..... -0.3V to +6V
DH5 to LX5 ..... -0.3V to (V_{BST5} + 0.3V)
BST5 to LX5 ..... -0.3V to +6V
DHC to LXC ..... -0.3V to (V_{BSTC} + 0.3V)
PDSL to GND ..... -0.3V to + 36V
BSTC to LXC ..... -0.3V to +6V
CELLS, CC, IINP to GND ..... -0.3V to (V_{LDO5} + 0.3V)
LDO_ Short Circuit to GND ..... Momentary
LDO5 Current (Internal Regulator) Continuous ..... +100mA
LDO3 Current (Internal Regulator) Continuous ..... +50mA
LDO_ Current (Switched Over) Continuous ..... +200mA
Continuous Power Dissipation (T_A = +70°C)
40-Pin Thin QFN (derate 34.5mW/°C above +70°C) 2857mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Note 1: Absolute Maximum Ratings valid using 20MHz bandwidth limit.

Note 2: LDO5 has a weak leakage to V_{CC} when LDO5 is more than 0.5V above V_{CC}. OUT5 has a weak leakage to V_{CC} when OUT5 is more than 0.5V above V_{CC}.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, no load on LDO5, LDO3, OUT5, OUT3, and REF, V_{CC} = 5V, ON3 = ON5 = V_{CC}, V_{DCIN} = V_{LXC} = V_{CSSP} = V_{CSSN} = 19V, V_{BSTC} - V_{LXC} = 5V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12.6V, V_{VCTL} = V_{ISET} = 1.8V, CELLS = open, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLIES							
Adapter Present Quiescent Current		I_{DCIN} + I_{CSSP} + I_{CSSN}, ON3 = ON5 = SKIP = V_{CC}, V_{OUT3} = 3.5V, V_{OUT5} = 5.3V	Charging enabled		3	6	mA
			Charging disabled		1.5	2.5	
Adapter Absent Quiescent Current		I_{DCIN} + I_{CSSP} + I_{CSSN}, ON3 = ON5 = SKIP = V_{CC}, V_{OUT3} = 3.5V, V_{OUT5} = 5.3V	V_{ISET} = 2.4V, IINP ON		1.5	2.5	mA
			ISET = GND		1.2	2.2	
CSSN Input Current		V_{CSSP} = V_{CSSN} = 24V, T_A = +25°C			0.1	2	µA
BATT + CSIP + CSIN + LXC Input Current		V_{BATT} = 16.8V, adapter absent, T_A = +25°C				4	µA
		V_{BATT} = 2V to 19V, adapter present			200	650	
DCIN Input Current	I_{DCIN}	ON3 = ON5 = SKIP = V_{CC}, charger disabled; V_{OUT3} = 3.5V, V_{OUT5} = 5.3V			0.1	0.2	mA
DCIN Standby Supply Current		V_{DCIN} = 5V to 24V, ON3 = ON5 = GND			130	270	µA
V_{CC} Supply Current	I_{CC}	ON3 = ON5 = SKIP = V_{CC}, charger disabled; V_{OUT3} = 3.5V, V_{OUT5} = 5.3V			1.0	1.5	mA
DCIN Input Voltage Range		**Note:** LDO5 is NOT guaranteed to be in regulation until DCIN is above 6V.		4.5		24	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, no load on LDO5, LDO3, OUT5, OUT3, and REF, V_{CC} = 5V, ON3 = ON5 = V_{CC}, V_{DCIN} = V_{LXC} = V_{CSSP} = V_{CSSN} = 19V, V_{BSTC} - V_{LXC} = 5V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12.6V, V_{VCTL} = V_{ISET} = 1.8V, CELLS = open, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DCIN Undervoltage-Lockout Trip Point for Charger	$V_{DCIN(UVLO)}$	V_{DCIN} falling	7.0	7.2		V
		V_{DCIN} rising		7.7	7.9	
DCIN POR Threshold	$V_{DCIN(POR)}$	Falling edge of V_{DCIN}		2.0		V
V_{CC} Undervoltage Lockout Threshold	$V_{CC(UVLO)}$	Falling edge of V_{CC}, PWM disabled below this threshold	3.8	4.0	4.3	V
		Rising edge of V_{CC}		4.2		
V_{CC} POR Threshold		Falling edge of V_{CC}		1.5		V
LINEAR REGULATORS						
LDO_ Output-Voltage Accuracy	V_{LDO5}	V_{DCIN} = 6V to 24V, ON5 = ON3 = GND 0mA < I_{LDO5} < 100mA, ON5 = GND	4.90	5.00	5.10	V
	V_{LDO3}	V_{LDO5} = 5V, I_{LDO5} = 0A 0mA < I_{LDO3} < 50mA, ON3 = GND	3.23	3.30	3.37	
Internal LDO Voltage After Switchover	V_{LDO5}	Not production tested	4.4	4.5	4.6	V
	V_{LDO3}	Not production tested	2.7	2.8	2.9	
LDO3 Short-Circuit Current		LDO3 = GND	50		130	mA
LDO5 Short-Circuit Current		LDO5 = GND	100		260	mA
LDO5 Bootstrap Switch Resistance		LDO5 to OUT5, V_{OUT5} = 5V, I_{LDO5} = 50mA		1.0	2.5	Ω
LDO3 Bootstrap Switch Resistance		LDO3 to OUT3, V_{OUT3} = 3.3V, I_{LDO3} = 50mA		1.5	3	Ω
Thermal-Shutdown Threshold	t_{SHDN}	Hysteresis = 50°C		+160		°C
REFERENCE						
REF Output Voltage	V_{REF}	I_{REF} = 50µA	2.09	2.10	2.11	V
REF Undervoltage-Lockout Threshold	V_{REF_UVLO}	V_{REF} falling		2.0		V
MAIN SMPS						
OUT5 Output Voltage Accuracy	V_{OUT5}	V_{IN} = 6V to 28V, SKIP = REF	5.033	5.083	5.135	V
OUT3 Output Voltage Accuracy	V_{OUT3}	V_{IN} = 6V to 28V, SKIP = REF	3.267	3.300	3.333	V
Load Regulation Error		Either SMPS, V_{SKIP} = 2V, I_{LOAD} = 0 to 5A		-0.1		%
		Either SMPS, SKIP = GND, I_{LOAD} = 0 to 5A		-1.7		
		Either SMPS, SKIP = V_{CC}, I_{LOAD} = 0 to 5A		-1.5		
Line Regulation Error		Either SMPS, V_{IN} = 6V to 28V		0.005		%/V
DH5 On-Time	t_{ON5}	V_{IN} = 12V, V_{OUT5} = 5.0V (Note 3); R_{TON} = 549kΩ (300kHz + 10%)	1073	1263	1452	ns
		V_{IN} = 12V, V_{OUT5} = 5.0V (Note 3); R_{TON} = 202kΩ (800kHz + 10%)	402	473	545	

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, no load on LDO5, LDO3, OUT5, OUT3, and REF, V_{CC} = 5V, ON3 = ON5 = V_{CC}, V_{DCIN} = V_{LXC} = V_{CSSP} = V_{CSSN} = 19V, V_{BSTC} - V_{LXC} = 5V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12.6V, V_{VCTL} = V_{ISET} = 1.8V, CELLS = open, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DH3 On-Time	t_{ON3}	V_{IN} = 12V, V_{OUT3} = 3.3V (Note 3)	R_{TON} = 549kΩ (300kHz - 10%)	866	1019	1171	ns
			R_{TON} = 202kΩ (800kHz - 10%)	325	382	439	
Minimum Off-Time	$t_{OFF(MIN)}$	(Note 3)		210	270	330	ns
Extended On-Time Blanking		Duty cycle > 50%; not for production test			300	360	ns
Soft-Start Time	t_{SS}	Rising edge on ON_			2		ms
Ultrasonic Operating Frequency	$f_{SW(USONIC)}$	SKIP = GND		15	22		kHz
MAIN SMPS FAULT DETECTION							
OUT_ Overvoltage Trip Threshold (PGOOD Pulled Low Above This Level)		With respect to error comparator threshold		13	16	19	%
OUT_Overvoltage Fault Propagation Delay	t_{OVP}	$V_{FB\_}$ forced 50mV above trip threshold			10		µs
OUT_ Undervoltage Protection Trip Threshold		With respect to error comparator threshold		65	70	75	%
OUT_ Output Undervoltage Fault Propagation Delay	t_{UVP}				10		µs
PGOOD Lower Trip Threshold		With respect to error comparator threshold, falling edge, hysteresis = 15mV		-350	-250	-150	mV
PGOOD Propagation Delay	t_{PGOOD}	OUT5 or OUT3 forced 50mV beyond PGOOD trip threshold, falling edge			10		µs
PGOOD Output Low Voltage		PGOOD low impedance, ON5 = ON3 = GND, I_{SINK} = 4mA				0.3	V
PGOOD Leakage Current	I_{PGOOD}	PGOOD high impedance, SMPS in regulation, PGOOD forced to 5.5V, T_A = +25°C				1	µA
Fault Reset Timer				7	10		ms
MAIN SMPS CURRENT LIMIT							
ILIM_ Adjustment Range				0.2		2.1	V
ILIM_ Leakage Current		T_A = +25°C		-0.1		+0.1	µA
Valley Current-Limit Threshold (Adjustable)	$V_{LIM\_(VAL)}$	V_{AGND} - $V_{LX\_}$	$V_{ILIM\_}$ = 0.5V	40	50	60	mV
			$V_{ILIM\_}$ = 1.00V	87	100	113	
			$V_{ILIM\_}$ = 2.10V	184	210	236	
Ultrasonic Negative Current-Limit Threshold	$I_{NEG(US)}$				72		mV
Current-Limit Threshold (Zero Crossing)	V_{ZX}	V_{AGND} - $V_{LX\_}$, SKIP = V_{CC} or GND, V_{ILIM} = 1V			1.5		mV

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, no load on LDO5, LDO3, OUT5, OUT3, and REF, V_{CC} = 5V, ON3 = ON5 = V_{CC}, V_{DCIN} = V_{LXC} = V_{CSSP} = V_{CSSN} = 19V, V_{BSTC} - V_{LXC} = 5V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12.6V, V_{VCTL} = V_{ISET} = 1.8V, CELLS = open, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MAIN SMPS INPUTS AND OUTPUTS						
SKIP Threshold Voltage	V_{SKIP}	High = SKIP	2.3		V_{CC}	V
		Mid = PWM	1.5		1.9	
		Low = ultrasonic	0		0.8	
SKIP Leakage Current		V_{SKIP} = 0 or 5V, T_A = +25°C	-2		+2	µA
ON_ Input Logic Levels		High (SMPS on)	2.4			V
		Low (SMPS off)			0.8	
ON_ Leakage Current		V_{ON3} = V_{ON5} = 0 or 5V, T_A = +25°C	-2		+2	µA
OUT_ Discharge-Mode On-Resistance	R_{DSCHG}	ON_ = GND	7.5	20	50	Ω
SMPS GATE DRIVERS						
DH3, DH5 Gate Driver On-Resistance	R_{DH3}, R_{DH5}	BST3 - LX3 and BST5 - LX5 forced to 5V; high state		1.6	3.8	Ω
		BST3 - LX3 and BST5 - LX5 forced to 5V; low state		1.6	3.8	
DL3, DL5 Gate Driver On-Resistance	R_{DL3}, R_{DL5}	DL3, DL5; high state		1.5	3.5	Ω
		DL3, DL5; low state		0.6	1.5	
DH3, DH5 Gate Driver Source/ Sink Current	I_{DH}	DH3, DH5 forced to 2.5V, BST3 - LX3 and BST5 - LX5 forced to 5V		2		A
DL3, DL5 Gate Driver Source Current	$I_{DL(SOURCE)}$	DL3, DL5 forced to 2.5V		1.7		A
DL3, DL5 Gate Driver Sink Current	$I_{DL(SINK)}$	DL3, DL5 forced to 2.5V		3.3		A
DHC Gate Driver On-Resistance	R_{DHC}	High state, I_{DHC} = 10mA		1.5	3	Ω
		Low state, I_{DHC} = -10mA		0.8	2.1	
DLC Gate Driver On-Resistance	R_{DLC}	High state, I_{DLC} = 10mA		3	6	Ω
		Low state, I_{DLC} = -10mA		3	6	
Internal BST_ Switch On-Resistance	R_{BST}	$I_{BST\_}$ = 10mA, V_{DD} = 5V		5		Ω
BST_ Leakage Current	I_{BST}	$V_{BST\_}$ = 24V, OUT3 and OUT5 above regulation threshold, T_A = +25°C		2	20	µA
CHARGER SMPS						
DHC Off-Time K Factor		V_{DCIN} = 19V, V_{BATT} = 10V	30	35	40	ns/V
Sense Voltage for Minimum Discontinuous Mode Ripple Current		V_{CSIP} - V_{CSIN}		5		mV
Zero Crossing Comparator Threshold		V_{CSIP} - V_{CSIN}		10		mV
Cycle-by-Cycle Current- Limit Sense Voltage		V_{CSIP} - V_{CSIN}	120	125	130	mV

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, no load on LDO5, LDO3, OUT5, OUT3, and REF, V_{CC} = 5V, ON3 = ON5 = V_{CC}, V_{DCIN} = V_{LXC} = V_{CSSP} = V_{CSSN} = 19V, V_{BSTC} - V_{LXC} = 5V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12.6V, V_{VCTL} = V_{ISET} = 1.8V, CELLS = open, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CHARGE-VOLTAGE REGULATION							
Battery-Regulation Voltage Accuracy	V_{BATT}	CELLS = open, VCTL = REF, 2 cells		-0.5		+0.5	%
		CELLS = GND, VCTL = REF, 3 cells		-0.5		+0.5	
		CELLS = LDO3, VCTL = REF, 4 cells		-0.5		+0.5	
VCTL Range		CELLS = open, 2 cells		1.0		3.5	V
VCTL Input Bias Current		VCTL = GND or VCTL = REF, T_A = +25°C		-1		+1	µA
CELLS 3-Cell Threshold						0.8	V
CELLS 2-Cell Level		CELLS = open		1.9	2.1	2.3	V
CELLS 4-Cell Threshold				2.8			V
CELLS Input Bias Current		CELLS = GND or V_{CELLS} = 3.6V, T_A = +25°C		-2		+2	µA
CHARGE-CURRENT REGULATION							
ISET Range		Charging current, analog setting		0		REF	V
Full-Charge-Current Accuracy (CSIP to CSIN)	V_{CSI}	V_{BATT} = 4V to 16.8V	V_{ISET} = V_{REF}, or PWM = 100%	97	100	103	mV
			V_{ISET} = 0.6 x V_{REF}, or PWM = 60%	57.6	60.0	62.4	
Trickle Charge-Current Accuracy	V_{CSI}	V_{BATT} = 4V to 16.8V, V_{ISET} = V_{REF}/36 or PWM = 2.7%		1.25	2.70	4.30	mV
Charge-Current Gain Error				-1.5		+1.5	%
Charge-Current Offset Error		Based on V_{ISET} = V_{REF} and V_{ISET} = 0.6 x V_{REF}		-1.4		+1.4	mV
CSIP/CSIN/BATT Input-Voltage Range				0		24	V
CSIP Leakage Current		V_{CSIP} = V_{CSIN} = 24V, T_A = +25°C		-0.2		+0.2	µA
CSIN Leakage Current		V_{CSIP} = V_{CSIN} = 24V, T_A = +25°C		1		4	µA
ISET Power-Down Mode Threshold	$V_{ISET-SDN}$	ISET falling		20	26	32	mV
		ISET rising		32	38	46	
ISET Input Bias Current		V_{ISET} = V_{REF}/2 and V_{ISET} = V_{REF}, T_A = +25°C		-0.15		+0.15	µA
ISET PWM Threshold		ISET rising				2.4	V
		ISET falling		0.8			
ISET Frequency	f_{ISET}			0.128		500	kHz
ISET Effective Resolution		f_{ISET} = 100kHz			8		Bit
INPUT SOURCE-CURRENT REGULATION							
Input Source Current-Limit Threshold	V_{CSS}	V_{CSSP} - V_{CSSN}		58.5	60.0	61.5	mV
				-2.5		+2.5	%
CSSP/CSSN Input-Voltage Range				5		26	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, no load on LDO5, LDO3, OUT5, OUT3, and REF, V_{CC} = 5V, ON3 = ON5 = V_{CC}, V_{DCIN} = V_{LXC} = V_{CSSP} = V_{CSSN} = 19V, V_{BSTC} - V_{LXC} = 5V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12.6V, V_{VCTL} = V_{ISET} = 1.8V, CELLS = open, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IINP Current-Sense Amplifier Voltage Gain	G_{IINP}		59.1	60.0	60.9	V/V
IINP Output-Voltage Range			0		4	V
IINP Accuracy		V_{CSSP} - V_{CSSN} = 60mV	-2		+2	%
		V_{CSSP} - V_{CSSN} = 40mV	-3		+3	
		V_{CSSP} - V_{CSSN} = 20mV	-4		+4	
IINP Gain Error		Measured at V_{CSSP} - V_{CSSN} = 60mV and V_{CSSP} - V_{CSSN} = 20mV	-1.25		+1.25	%
IINP Offset Error		Measured at V_{CSSP} - V_{CSSN} = 60mV and V_{CSSP} - V_{CSSN} = 20mV	-0.6		+0.6	mV
ADAPTER OVERCURRENT (ACOC) DETECTION						
ACOCP Threshold	$V_{CSIN-OCP}$	With respect to V_{CSSP} _V_{CSSN}		78		mV
				130		%
ACOCP Blanking Time				16		ms
ACOCP Waiting Time		When ACOCP comparator is high and at the time the blanking time expires		0.6		s
ACIN, $\overline{ACOK}$, AND ACOV						
ACIN Rising Debounce				44		ms
ACIN Falling Delay				10		µs
ACIN Input Bias Current		T_A = +25°C	-1		+1	µA
$\overline{ACOK}$ Detect Threshold	V_{ACINOK}	Measured at ACIN rising, hysteresis = 40mV (typ)	1.47	1.50	1.53	V
			-2		+2	%
ACOV Detect Threshold	V_{ACINOV}	Measured at ACIN rising, hysteresis = 40mV (typ)	2.05	2.10	2.15	V
			-2.38		+2.38	%
$\overline{ACOK}$ Sink Current		$V_{\overline{ACOK}}$ = 0.4V, V_{ACIN} = 1.7V	1			mA
$\overline{ACOK}$ Leakage Current		$V_{\overline{ACOK}}$ = 5.5V, V_{ACIN} = 1.3V, T_A = +25°C			1	µA
ADAPTER PRESENT DETECTION						
Adapter Absence Detect Threshold		V_{DCIN} - V_{BATT}, V_{DCIN} falling	0	100	200	mV
Adapter Detect Threshold		V_{DCIN} - V_{BATT}, V_{DCIN} rising	300	440	600	mV
CHARGE-PUMP MOSFET DRIVER						
PDSL Gate-Driver Source Current	$I_{PDSL-SRC}$	V_{PDSL} - V_{DCIN} = 3V, V_{DCIN} = 19V		60		µA
PDSL Gate-Driver Output Voltage High	V_{PDSL-H}	V_{DCIN} = 19V	V_{DCIN} + 5.3	V_{DCIN} + 8		V
PDSL SWITCH CONTROL						
PDSL Turn-Off Resistance	R_{PDSL}	Measured from PDSL to GND		2.5		kΩ
BATTERY OVERVOLTAGE						
BATT Overvoltage Threshold	$V_{CELL(OV)}$	V_{BATT} rising, hysteresis = 20mV (typ)		+100		mV/cell

Integrated Charger, Dual Main Step-Down Controllers, and Dual LDO Regulators

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, no load on LDO5, LDO3, OUT5, OUT3, and REF, V_{CC} = 5V, ON3 = ON5 = V_{CC}, V_{DCIN} = V_{LXC} = V_{CSSP} = V_{CSSN} = 19V, V_{BSTC} - V_{LXC} = 5V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12.6V, V_{VCTL} = V_{ISET} = 1.8V, CELLS = open, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLIES							
Adapter Present Quiescent Current		I_{DCIN} + I_{CSSP} + I_{CSSN}, ON3 = ON5 = SKIP = V_{CC}, V_{OUT3} = 3.5V, V_{OUT5} = 5.3V	Charging enabled			6	mA
			Charging disabled			2.5	
Adapter Absent Quiescent Current		I_{DCIN} + I_{CSSP} + I_{CSSN}, ON3 = ON5 = SKIP = V_{CC}, V_{OUT3} = 3.5V, V_{OUT5} = 5.3V	V_{ISET} = 2.4V, IINP ON			2.5	mA
			ISET = GND			2.2	
CSSN Input Current		V_{CSSP} = V_{CSSN} = 24V				2	µA
BATT + CSIP + CSIN + LXC Input Current		V_{BATT} = 16.8V, adapter absent				4	µA
		V_{BATT} = 2V to 19V, adapter present				650	
DCIN Input Current	I_{DCIN}	ON3 = ON5 = SKIP = V_{CC}, charger disabled; V_{OUT3} = 3.5V, V_{OUT5} = 5.3V				0.2	mA
DCIN Standby Supply Current		V_{DCIN} = 5V to 24V, ON3 = ON5 = GND				300	µA
V_{CC} Supply Current	I_{CC}	ON3 = ON5 = SKIP = V_{CC}, charger disabled; V_{OUT3} = 3.5V, V_{OUT5} = 5.3V				1.5	mA
DCIN Input-Voltage Range		**Note:** LDO5 is NOT guaranteed to be regulation until DCIN is above 6V		4.5		24	V
DCIN Undervoltage-Lockout Trip Point for Charger	$V_{DCIN(UVLO)}$	V_{DCIN} falling		6.9			V
		V_{DCIN} rising				7.9	
V_{CC} UndervoltageLockout Threshold	$V_{CC(UVLO)}$	Falling edge of V_{CC}, PWM disabled below this threshold		3.8		4.3	V
LINEAR REGULATORS							
LDO_ Output-Voltage Accuracy	V_{LDO5}	V_{DCIN} = 6V to 24V, ON5 = ON3 = GND, 0mA < I_{LDO5} < 100mA, ON5 = GND		4.85		5.15	V
	V_{LDO3}	V_{LDO5} = 5V, I_{LDO5} = 0A, 0mA < I_{LDO3} < 50mA, ON3 = GND		3.20		3.40	
LDO3 Short-Circuit Current		LDO3 = GND				130	mA
LDO5 Short-Circuit Current		LDO5 = GND				260	mA
REFERENCE							
REF Output Voltage	V_{REF}	I_{REF} = 50µA		2.08		2.12	V
MAIN SMPS							
OUT5 Output-Voltage Accuracy	V_{OUT5}	V_{IN} = 6V to 28V, SKIP = REF		5.008		5.160	V
OUT3 Output-Voltage Accuracy	V_{OUT3}	V_{IN} = 6V to 28V, SKIP = REF		3.25		3.35	V
DH5 On-Time	t_{ON5}	V_{IN} = 12V, V_{OUT5} = 5.0V (Note 3)	R_{TON} = 549kΩ (300kHz + 10%)	1073		1452	ns
			R_{TON} = 202kΩ (800kHz + 10%)	402		545	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, no load on LDO5, LDO3, OUT5, OUT3, and REF, V_{CC} = 5V, ON3 = ON5 = V_{CC}, V_{DCIN} = V_{LXC} = V_{CSSP} = V_{CSSN} = 19V, V_{BSTC} - V_{LXC} = 5V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12.6V, V_{VCTL} = V_{ISET} = 1.8V, CELLS = open, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DH3 On-Time	t_{ON3}	V_{IN} = 12V, V_{OUT3} = 3.3V (Note 3)	R_{TON} = 549kΩ (300kHz - 10%)	866		1171	ns
			R_{TON} = 202kΩ (800kHz - 10%)	325		439	
Minimum Off-Time	$t_{OFF(MIN)}$	(Note 3)				330	ns
Extended On-Time Blanking		Duty cycle > 50%; not for production test				360	ns
Ultrasonic Operating Frequency	$f_{SW(USONIC)}$	SKIP = GND		13			kHz
MAIN SMPS FAULT DETECTION							
OUT_ Overvoltage Trip Threshold (PGOOD Pulled Low Above this Level)		With respect to error comparator threshold		12		20	%
OUT_ Undervoltage Protection Trip Threshold		With respect to error comparator threshold		63		77	%
PGOOD Lower Trip Threshold		With respect to error comparator threshold, falling edge, hysteresis = 15mV		-350		-150	mV
PGOOD Output Low Voltage		PGOOD low impedance, ON5 = ON3 = GND, I_{SINK} = 4mA				0.4	V
Fault Reset Timer		Not for production test		7			ms
MAIN SMPS CURRENT LIMIT							
ILIM_ Adjustment Range				0.2		2.1	V
Valley Current-Limit Threshold (Adjustable)	$V_{LIM\_(VAL)}$	V_{AGND} - $V_{LX\_}$	$V_{ILIM\_}$ = 0.5V	40		60	mV
			$V_{ILIM\_}$ = 1.00V	85		115	
			$V_{ILIM\_}$ = 2.10V	174		246	
MAIN SMPS INPUTS AND OUTPUTS							
SKIP Threshold Voltage	V_{SKIP}	High = SKIP		2.3		V_{CC}	V
		Mid = PWM		1.5		1.9	
		Low = ultrasonic		0		0.8	
SKIP Leakage Current		V_{SKIP} = 0 or 5V, T_A = +25°C		-2		+2	µA
ON_ Input Logic Levels		High (SMPS on)		2.4			V
		Low (SMPS off)				0.8	
SMPS GATE DRIVERS							
DH3, DH5 Gate Driver On-Resistance	R_{DH3}, R_{DH5}	BST3 - LX3 and BST5 - LX5 forced to 5V; high state				3.8	Ω
		BST3 - LX3 and BST5 - LX5 forced to 5V; low state				3.8	
DL3, DL5 Gate-Driver On-Resistance	R_{DL3}, R_{DL5}	DL3, DL5; high state				3.5	Ω
		DL3, DL5; low state				1.5	
DHC Gate-Driver On-Resistance	R_{DHC}	High state, I_{DHC} = 10mA				3	Ω
		Low state, I_{DHC} = -10mA				2.1	

Integrated Charger, Dual Main Step-Down Controllers, and Dual LDO Regulators

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, no load on LDO5, LDO3, OUT5, OUT3, and REF, V_{CC} = 5V, ON3 = ON5 = V_{CC}, V_{DCIN} = V_{LXC} = V_{CSSP} = V_{CSSN} = 19V, V_{BSTC} - V_{LXC} = 5V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12.6V, V_{VCTL} = V_{ISET} = 1.8V, CELLS = open, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DLC Gate-Driver On-Resistance	R_{DLC}	High state, I_{DLC} = 10mA			6	Ω
		Low state, I_{DLC} = -10mA			6	
CHARGER SMPS						
DHC Off-Time K Factor		V_{DCIN} = 19V, V_{BATT} = 10V	30		40	ns/V
Cycle-by-Cycle Current-Limit Sense Voltage		V_{CSIP} - V_{CSIN}	120		130	mV
CHARGE-VOLTAGE REGULATION						
Battery-Regulation Voltage Accuracy	V_{BATT}	CELLS = open, VCTL = REF, 2 cells	-0.5		+0.5	%
		CELLS = GND, VCTL = REF, 3 cells	-0.5		+0.5	
		CELLS = LDO3, VCTL = REF, 4 cells	-0.5		+0.5	
VCTL Range			0		2.4	V
CELLS 3-Cell Threshold					0.8	V
CELLS 2-Cell Level		CELLS = open	1.9		2.3	V
CELLS 4-Cell Threshold			2.8			V
CHARGE-CURRENT REGULATION						
ISET Range		Charging current, analog setting	0.0		REF	V
Full-Charge-Current Accuracy (CSIP to CSIN)	V_{CSI}	V_{BATT} = 4V to 16.8V, V_{ISET} = V_{REF}, or PWM = 100%	97		103	mV
		V_{BATT} = 4V to 16.8V, V_{ISET} = 0.6 x V_{REF}, or PWM = 60%	57.6		62.4	
Trickle Charge-Current Accuracy	V_{CSI}	V_{BATT} = 4V to 16.8V, V_{ISET} = V_{REF}/36 or PWM = 2.7%	1.2		4.3	mV
Charge-Current Gain Error			-1.5		+1.5	%
Charge-Current Offset Error		Based on V_{ISET} = V_{REF} and V_{ISET} = 0.6 x V_{REF}	-1.4		+1.4	mV
CSIP/CSIN/BATT Input Voltage Range			0		24	V
ISET Power-Down Mode Threshold	$V_{ISET-SDN}$	ISET falling	20		32	mV
		ISET rising	32		46	
ISET PWM Threshold		ISET rising			2.4	V
		ISET falling	0.8			
ISET Frequency	f_{ISET}		0.128		500	kHz

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, no load on LDO5, LDO3, OUT5, OUT3, and REF, V_{CC} = 5V, ON3 = ON5 = V_{CC}, V_{DCIN} = V_{LXC} = V_{CSSP} = V_{CSSN} = 19V, V_{BSTC} - V_{LXC} = 5V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12.6V, V_{VCTL} = V_{ISET} = 1.8V, CELLS = open, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SOURCE-CURRENT REGULATION						
Input Source-Current Limit Threshold	V_{CSS}	V_{CSSP} - V_{CSSN}	58.5		61.5	mV
			-2.5		+2.5	%
CSSP/CSSN Input-Voltage Range			5		26	V
IINP Current-Sense Amplifier Voltage Gain	G_{IINP}		59.9		60.1	V/V
IINP Output-Voltage Range			0		4	V
IINP Accuracy		V_{CSSP} - V_{CSSN} = 60mV	-2		+2	%
		V_{CSSP} - V_{CSSN} = 40mV	-3		+3	
		V_{CSSP} - V_{CSSN} = 20mV	-4		+4	
IINP Gain Error		Measured at V_{CSSP} - V_{CSSN} = 60mV and V_{CSSP} - V_{CSSN} = 20mV	-1.5		+1.5	%
IINP Offset Error		Measured at V_{CSSP} - V_{CSSN} = 60mV and V_{CSSP} - V_{CSSN} = 20mV	-0.65		+0.65	mV
ACIN, $\overline{ACOK}$, AND ACOV						
$\overline{ACOK}$ Detect Threshold	V_{ACINOK}	Measured at ACIN rising, hysteresis = 40mV (typ)	1.47		1.53	V
			-2		+2	%
ACOV Detect Threshold	V_{ACINOV}	Measured at ACIN rising, hysteresis = 40mV (typ)	2.05		2.15	V
			-2.38		+2.38	%
$\overline{ACOK}$ Sink Current		$V_{\overline{ACOK}}$ = 0.4V, V_{ACIN} = 1.7V	1			mA
ADAPTER PRESENT DETECTION						
Adapter Absence Detect Threshold		V_{DCIN} - V_{BATT}, V_{DCIN} falling	0		200	mV
Adapter Detect Threshold		V_{DCIN} - V_{BATT}, V_{DCIN} rising	300		600	mV
CHARGE-PUMP MOSFET DRIVER						
PDSL Gate-Driver Output Voltage High	V_{PDSL_H}	V_{DCIN} = 19V	V_{DCIN} + 5.3			V

Note 3: On-time and off-time specifications are measured from 50% point to 50% point at the DH pin with LX = PGND, V_{BST} = 5V, and a 500pF capacitor from DH to LX to simulate external MOSFET gate capacitance. Actual in-circuit times may be different due to MOSFET switching speeds.

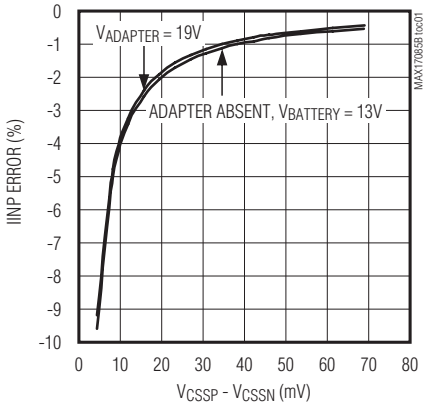
Note 4: Specifications to T_A = -40°C are guaranteed by design and not production tested.

Integrated Charger, Dual Main Step-Down Controllers, and Dual LDO Regulators

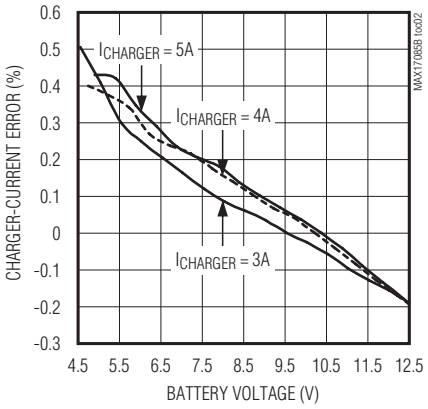
Typical Operating Characteristics

(Circuit of Figure 1, V_{ADP} = V_{SYS} = 20V, V_{BATT} = 16.8V, V_{LDO5} = V_{CC} = 5V, V_{LDO3} = 3.3V, T_A = +25°C, unless otherwise noted.)

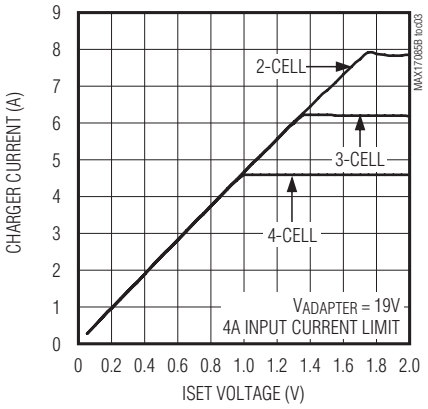
IINP ERROR vs. SYSTEM CURRENT (DC SWEEP)



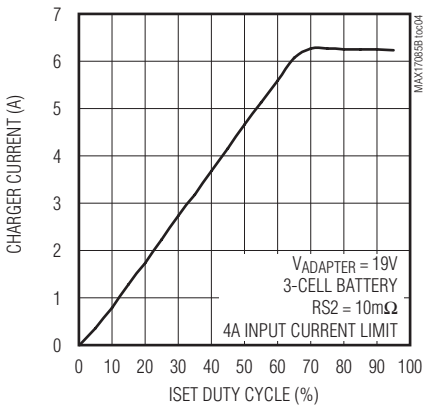
CHARGER-CURRENT ERROR vs. BATTERY VOLTAGE



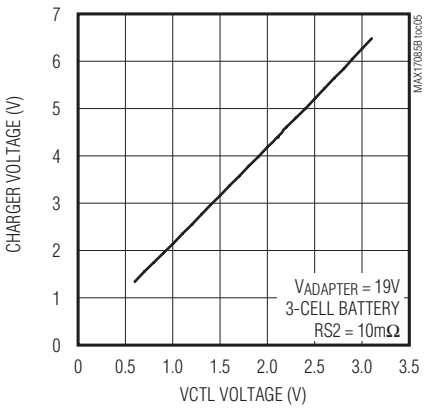
CHARGER CURRENT vs. ISET SETTING (ANALOG)



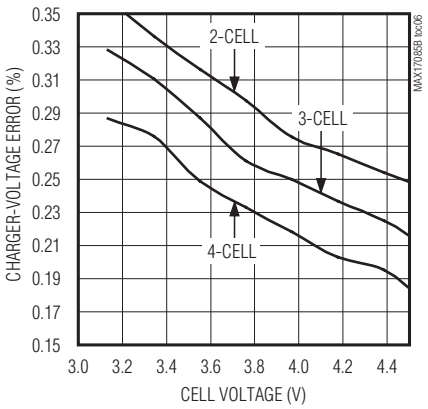
CHARGER CURRENT vs. ISET SETTING (PWM)



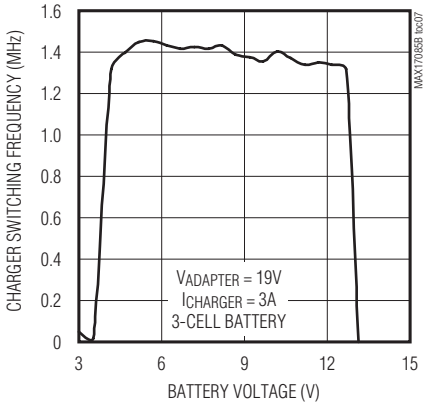
CHARGER-VOLTAGE PER CELL vs. VCTL VOLTAGE



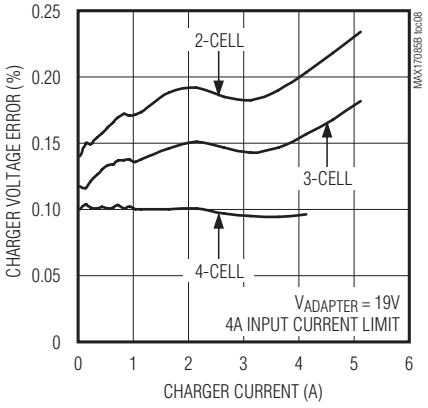
CHARGER-VOLTAGE ERROR vs. CELL VOLTAGE



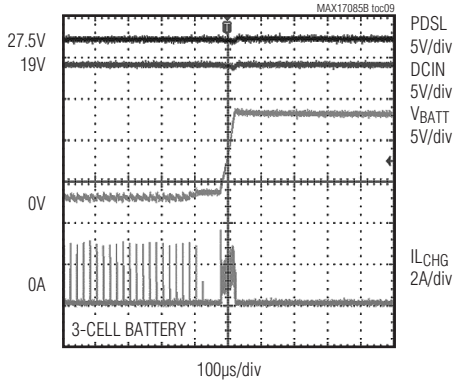
CHARGER SWITCHING FREQUENCY vs. BATTERY VOLTAGE



CHARGER VOLTAGE ERROR vs. CHARGER CURRENT



BATTERY REMOVAL (V_{BATT} = 3V)

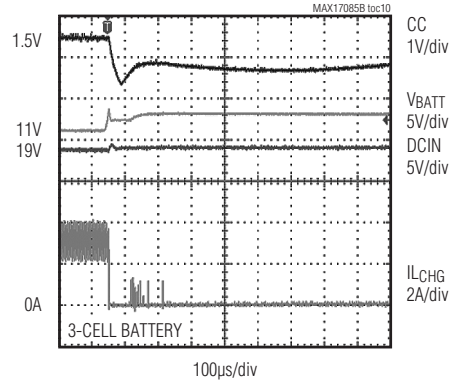


Integrated Charger, Dual Main Step-Down Controllers, and Dual LDO Regulators

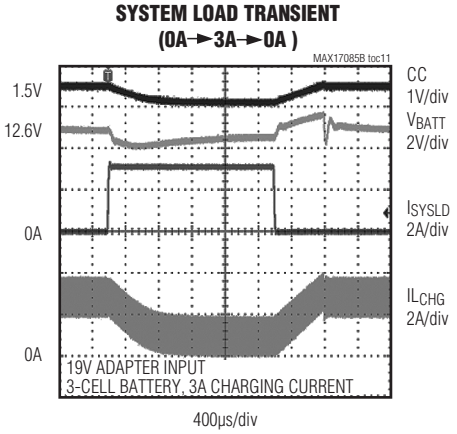
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{ADP} = V_{SYS} = 20V, V_{BATT} = 16.8V, V_{LDO5} = V_{CC} = 5V, V_{LDO3} = 3.3V, T_A = +25°C, unless otherwise noted.)

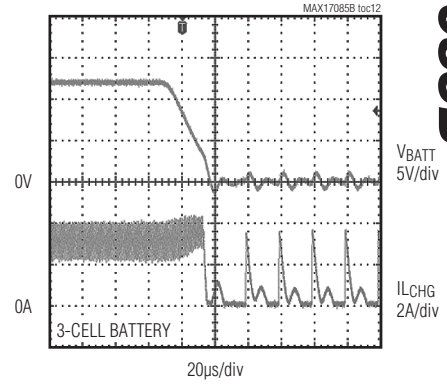
BATTERY REMOVAL (V_{BATT} = 11V)



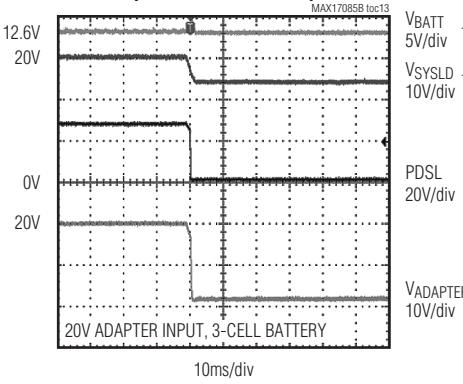
SYSTEM LOAD TRANSIENT (0A→3A→0A)



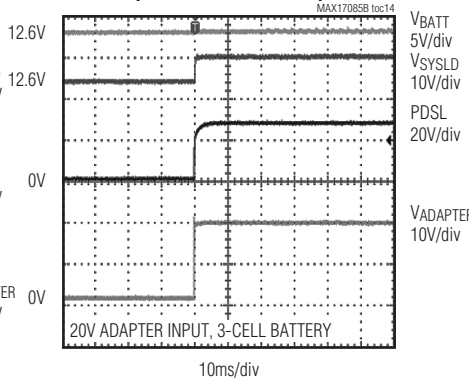
CHARGER OUTPUT SHORT CIRCUIT



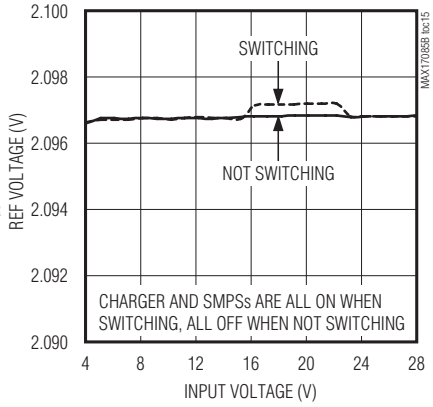
POWER-SOURCE SELECTOR SCHEME WHEN BATTERY IS PRESENT (ADAPTER REMOVAL)



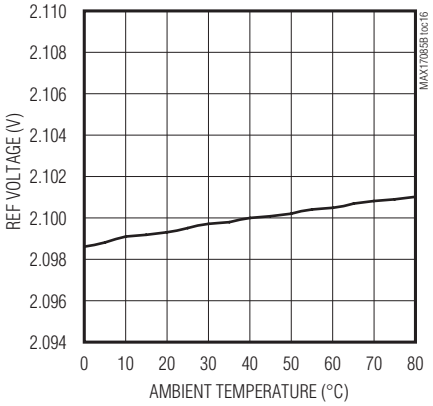
POWER-SOURCE SELECTOR SCHEME WHEN BATTERY IS PRESENT (ADAPTER INSERTION)



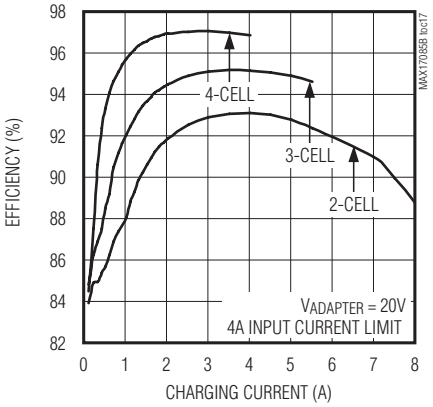
V_{REF} LINE REGULATION (SWITCHING AND NOT SWITCHING)



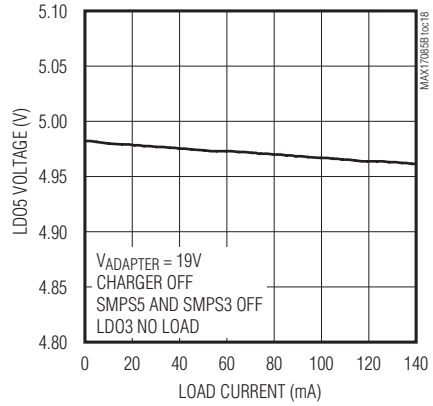
V_{REF} vs. AMBIENT TEMPERATURE



CHARGER EFFICIENCY vs. CHARGING CURRENT



LDO5 LOAD REGULATION

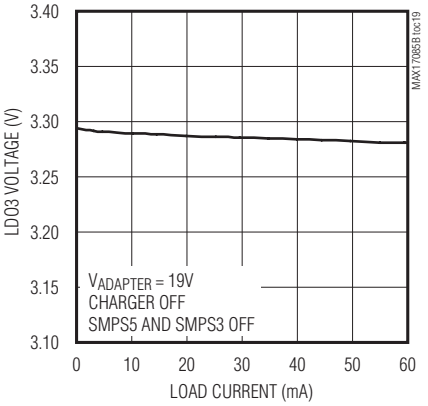


Integrated Charger, Dual Main Step-Down Controllers, and Dual LDO Regulators

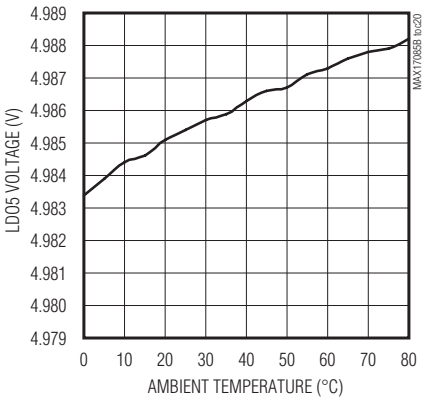
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{ADP} = V_{SYS} = 20V, V_{BATT} = 16.8V, V_{LDO5} = V_{CC} = 5V, V_{LDO3} = 3.3V, T_A = +25°C, unless otherwise noted.)

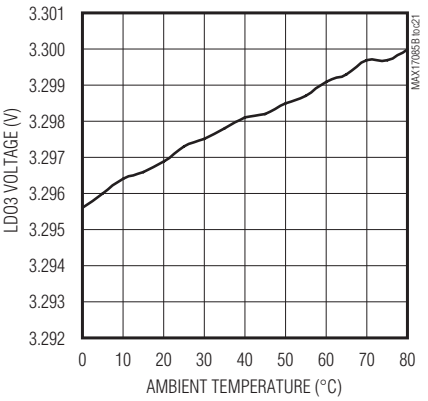
LDO3 LOAD REGULATION



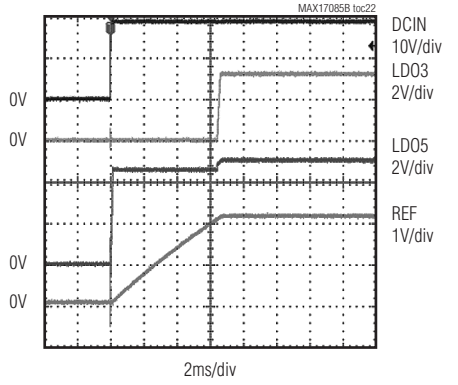
LDO5 vs. AMBIENT TEMPERATURE



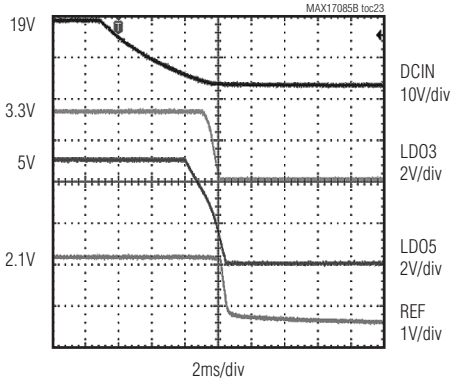
LDO3 vs. AMBIENT TEMPERATURE



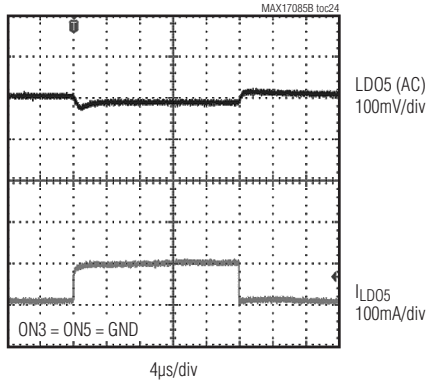
LDO AND REF POWER-UP



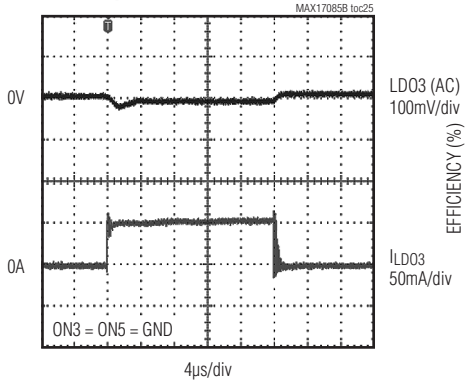
DCIN, LDO AND REF POWER REMOVAL



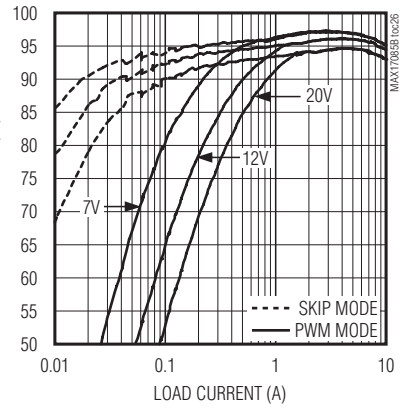
LDO5 LOAD TRANSIENT (0mA→100mA→0mA)



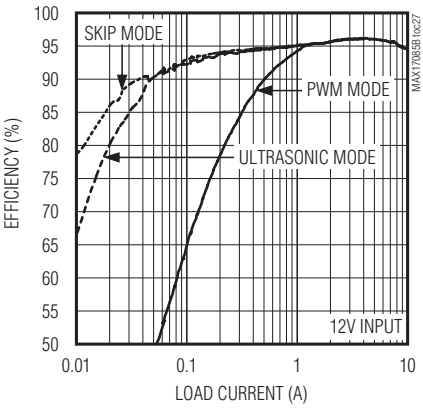
LDO3 LOAD TRANSIENT (0mA→50mA→0mA)



SMPS5 EFFICIENCY vs. LOAD CURRENT (CHARGER AND SMPS3 ARE OFF)



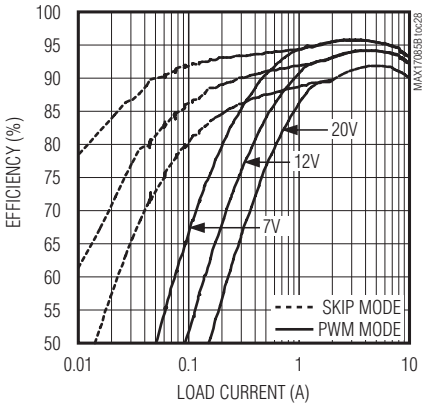
SMPS5 EFFICIENCY vs. LOAD CURRENT (CHARGER AND SMPS3 ARE OFF)



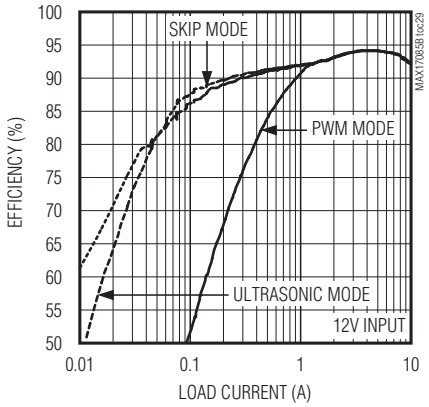
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{ADP} = V_{SYS} = 20V, V_{BATT} = 16.8V, V_{LDO5} = V_{CC} = 5V, V_{LDO3} = 3.3V, T_A = +25°C, unless otherwise noted.)

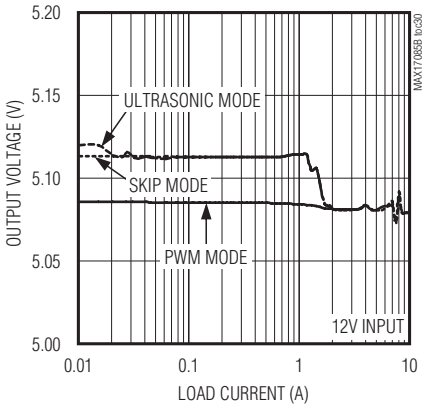
SMPS3 EFFICIENCY vs. LOAD CURRENT (CHARGER AND SMPS5 ARE OFF)



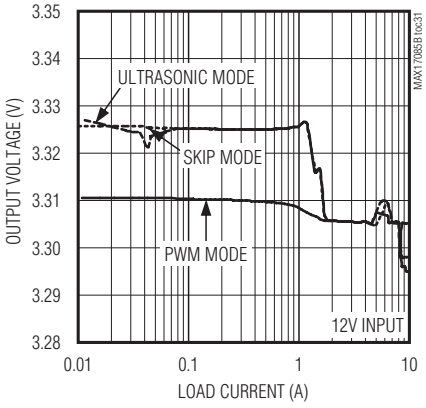
SMPS3 EFFICIENCY vs. LOAD CURRENT (CHARGER AND SMPS5 ARE OFF)



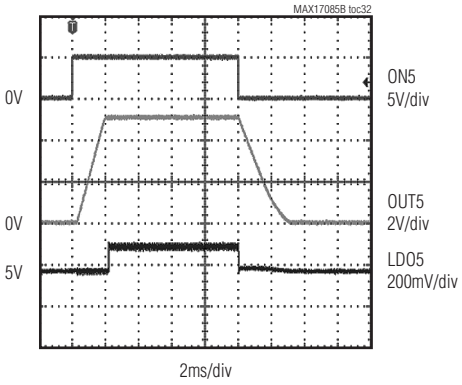
SMPS5 OUTPUT vs. LOAD CURRENT



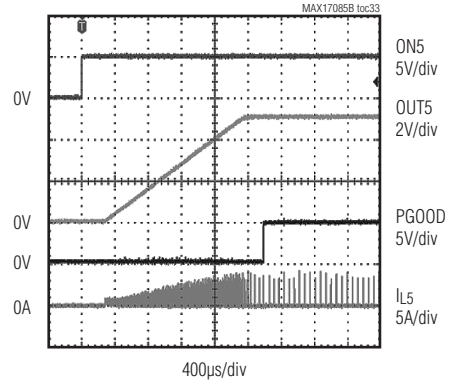
SMPS3 OUTPUT vs. LOAD CURRENT



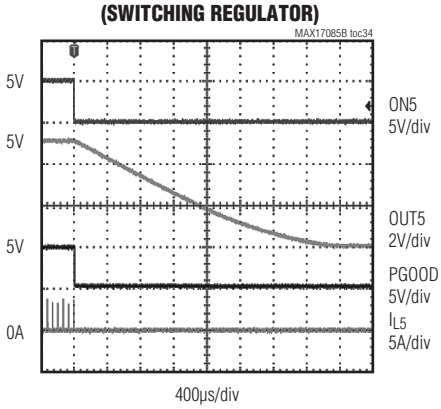
SMPS5 STARTUP AND SHUTDOWN LOAD



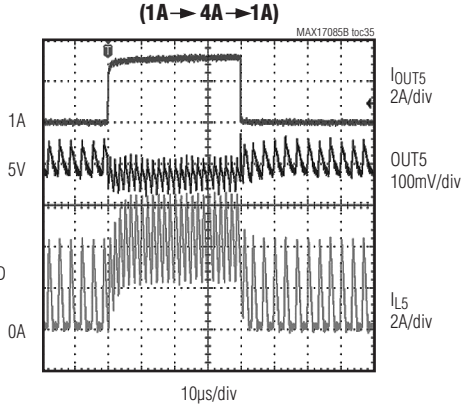
SMPS5 STARTUP WAVEFORMS (SWITCHING REGULATOR)



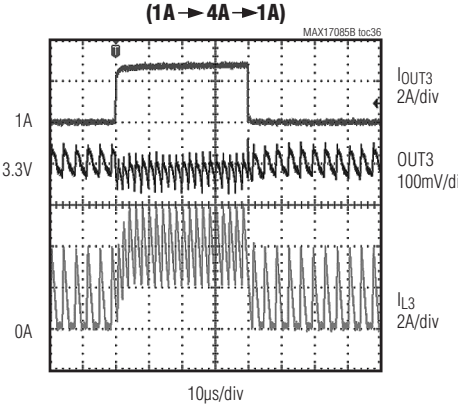
SMPS5 SHUTDOWN WAVEFORMS (SWITCHING REGULATOR)



SMPS5 LOAD TRANSIENT (1A→4A→1A)



SMPS3 LOAD TRANSIENT (1A→4A→1A)



Integrated Charger, Dual Main Step-Down Controllers, and Dual LDO Regulators

Pin Description

PIN	NAME	FUNCTION
1	LX3	Inductor Connection for SMPS3. Connect LX3 to the switched side of the inductor. LX3 is the lower supply rail for the DH3 high-side gate driver.
2	BST3	Boost Flying Capacitor Connection for SMPS3. Connect to an external capacitor as shown in Figure 1. An optional resistor in series with BST3 allows the DH3 turn-on current to be adjusted. A 4.7Ω resistor is recommended to improve crosstalk between SMPSs.
3	DL3	Low-Side Gate-Driver Output for SMPS3. DL3 swings from PGND to LDO5.
4	OUT3	Output Voltage-Sense Input for SMPS3. OUT3 is an input to the Quick-PWM on-time one-shot timer. OUT3 also serves as the feedback input for the preset 3.3V, and the discharge path when in shutdown. When OUT3 is in regulation, LDO3 is internally set to a lower level, and a bypass switch between OUT3 and LDO3 is enabled.
5	LDO3	3.3V Linear Regulator Output. LDO3 is the output of the 3.3V linear regulator supplied from LDO5. LDO3 is switched over to OUT3 when SMPS3 is in regulation plus 200µs. Bypass LDO3 to PGND with a 4.7µF or greater ceramic capacitor.
6	DCIN	LDO5 Supply Input. Bypass DCIN with a 1µF capacitor to PGND.
7	LDO5	5V Linear Regulator Output. LDO5 provides the power to the MOSFET drivers. LDO5 is the output of the 5V linear regulator supplied from DCIN. LDO5 is switched over to OUT5 when SMPS5 is in regulation plus 200µs. Bypass LDO5 to PGND with a 4.7µF or greater ceramic capacitor.
8	OUT5	Output Voltage-Sense Input for SMPS5. OUT5 is an input to the Quick-PWM on-time one-shot timer. OUT5 also serves as the feedback input for the preset 5V, and the discharge path when in shutdown. When OUT5 is in regulation, LDO5 is internally set to a lower level, and a bypass switch between OUT5 and LDO5 is enabled.
9	DL5	Low-Side Gate-Driver Output for SMPS5. DL5 swings from PGND to LDO5.
10	BST5	Boost Flying Capacitor Connection for SMPS5. Connect to an external capacitor as shown in Figure 1. An optional resistor in series with BST5 allows the DH5 turn-on current to be adjusted. A 4.7Ω resistor is recommended to improve crosstalk between SMPSs.
11	LX5	Inductor Connection for SMPS5. Connect LX5 to the switched side of the inductor. LX5 is the lower supply rail for the DH5 high-side gate driver.
12	DH5	High-Side Gate-Driver Output for SMPS5. DH5 swings from LX5 to BST5.
13	DLC	Low-Side Power MOSFET Driver Output for Charger. Connect to the low-side n-channel MOSFET gate.
14	BSTC	Boost Flying Capacitor Connection for Charger. Connect a 0.1µF capacitor from BSTC to LXC, and a Schottky diode from LDO5 to BSTC.
15	LXC	High-Side Driver Source Connection. Connect a 0.1µF capacitor from BSTC to LXC.
16	DHC	High-Side Power MOSFET Driver Output for Charger. Connect to high-side n-channel MOSFET gate.
17	PGOOD	Open-Drain Power-Good Output for SMPS3 and SMPS5. PGOOD is low when either SMPS3 or SMPS5 output voltage is more than 250mV (typ) below the nominal regulation threshold, during soft-start, in shutdown (ON3 = ON5 = GND), and after either fault latch has been tripped. After the soft-start circuit has terminated, PGOOD becomes high impedance if the output is in regulation plus 200µs. When only one SMPS is active, PGOOD monitors the active SMPS output. When the 2nd SMPS is started, PGOOD is blanked high-Z during the 2nd SMPS soft-start plus 200µs, then PGOOD monitors both SMPS outputs.

Pin Description (continued)

PIN	NAME	FUNCTION
18	$\overline{ACOK}$	AC-Detect Output. This open-drain output is low impedance when ACIN is greater than 1.5V, with a delay of 44ms. The $\overline{ACOK}$ output remains high impedance when the MAX17085B is powered down. Connect a 100kΩ pullup resistor from LDO3 or LDO5 to $\overline{ACOK}$.
19	CSIN	Output Current-Sense Negative Input
20	CSIP	Output Current-Sense Positive Input. Connect a current-sense resistor from CSIP to CSIN.
21	BATT	Battery Voltage Feedback Input
22	PDSL	Power Source Switch Driver Output. When the adapter is not present or an overvoltage and overcurrent event is detected, the PDSL output is pulled to GND. Leave PDSL unconnected when it is not used.
23	CSSN	Input Current-Sense Negative Input
24	CSSP	Input Current Sense for Positive Input. Connect a current-sense resistor from CSSP to CSSN.
25	IINP	Input Current Monitor Output. IINP sources the current proportional to the current sensed across CSSP and CSSN. The gain from (CSSP - CSSN) to IINP is 60V/V: $V_{IINP} = 60 \times (V_{CSSP} - V_{CSSN})$ IINP also monitors the battery-discharge current when the adapter is absent. To monitor the discharge current, set ISET above the PWM threshold. Pull ISET to GND to disable the IINP battery-discharge current mode.
26	CELLS	Trilevel Input for Setting Number of Cells: • CELLS = open; charge with 2 times the cell voltage programmed at VCTL. • CELLS = GND; charge with 3 times the cell voltage programmed at VCTL. • CELLS > 2.8V; charge with 4 times the cell voltage programmed at VCTL.
27	CC	Charger Loop-Compensation Point. External compensation node for the charge voltage and input current-limit loops. Connect a 4.7nF to 47nF capacitor to GND. Typically a 10nF capacitor works for most applications.
28	ACIN	AC Adapter Detect Input. ACIN is the input to an uncommitted comparator. The $\overline{ACOK}$ detect threshold is typically 1.5V. The ACOVP detect threshold is typically 2.1V. When ACIN is above the $\overline{ACOK}$ detect threshold and below the ACOVP detect threshold, PDSL is enabled.
29	VCTL	Cell Charge Voltage-Control Input. VCTL range is from GND to LDO5. For 4.375V/cell setting, connect VCTL to REF: $V_{CELL} = 2.083 \times V_{VCTL}$
30	V_{CC}	Analog Supply Voltage Input. Connect V_{CC} to the system supply voltage with a series 47Ω resistor, and bypass to analog ground using a 1µF or greater ceramic capacitor.
31	ISET	Dual-Mode Input for Setting Maximum Charge Current. In PWM mode, use input frequencies from 128Hz to 500kHz for charge-current setting. If there are no **two edges** within 20ms, ISET is directly used as an analog input. In analog mode, charge current is set as follows: $I_{CHG} = \frac{100mV}{RS2} \times \frac{V_{ISET}}{V_{REF}}$ Pull ISET to GND to shut down the charger.
32	REF	2.1V Voltage Reference and Device Power-Supply Input. Bypass REF with a 1µF capacitor to GND.
33	GND	Analog Ground
34	ILIM3	Valley Current-Limit Adjustment for SMPS3. The GND - LX3 current-limit threshold is 1/10 the voltage present on ILIM3 over a 0.2V to 2.1V range.
35	ILIM5	Valley Current-Limit Adjustment for SMPS5. The GND - LX5 current-limit threshold is 1/10 the voltage present on ILIM5 over a 0.2V to 2.1V range.

Integrated Charger, Dual Main Step-Down Controllers, and Dual LDO Regulators

Pin Description (continued)

PIN	NAME	FUNCTION
36	SKIP	Pulse-Skipping Control Input. This tri-level input determines the operating mode for the switching regulators. High (V_{CC}) = pulse-skipping mode Mid (1.8V) = forced-PWM operation GND = ultrasonic mode
37	TON	Switching Frequency Setting Input. An external resistor between the input power source and this pin sets the nominal switching frequency according to the following equation: $f_{SW(NOM)} = 1/(C_{TON} \times (R_{TON} + 6.5k\Omega))$ where C_{TON} = 6pF. SMPS5 has a switching frequency that is 10% higher than nominal, and SMPS3 has a switching frequency 10% lower than nominal. R_{TON} is high impedance when ON3 = ON5 = GND.
38	ON3	Enable Input for SMPS3. Drive ON3 high to enable SMPS3. Drive ON3 low to shut down SMPS3.
39	ON5	Enable Input for SMPS5. Drive ON5 high to enable SMPS5. Drive ON5 low to shut down SMPS5.
40	DH3	High-Side Gate-Driver Output for SMPS3. DH3 swings from LX3 to BST3.
—	EP	Exposed Pad. Internally connected to power ground (PGND). Connect the backside exposed pad to the system power ground as well.

Standard Application Circuit

The MAX17085B standard application circuit (Figure 1) features a 4A charger, 8A outputs on SMPS5 and SMPS3, and a 100mA LDO5 and 50mA LDO3 typical of most notebook CPU applications. See Table 1 for component selections. Table 2 lists the component suppliers.

Table 1. Component Selection for Standard Applications

COMPONENT	SMPS3: 3.3V, 8A, 500kHZ	SMPS5: 5V, 8A, 600kHZ	CHARGER, 16.8V, 4A, 1.2MHZ
Input Voltage	**V_{SYS} = 7V to 24V**	**V_{SYS} = 7V to 24V**	**V_{ADP} = 18V to 20V**
Input Capacitor	(2) 10µF, 25V Taiyo Yuden TMK432BJ106KM Murata GRM31CR61E106K	(2) 10µF, 25V Taiyo Yuden TMK432BJ106KM Murata GRM31CR61E106K	(2) 4.7µF, 25V Taiyo Yuden TMK432BJ475KM Murata GRM31CR71E475M
Output Capacitor	C_{OUT3} (1) 100µF, 6V, 18mΩ SANYO 6TPE100MI	C_{OUT5} (1) 100µF, 6V, 18mΩ SANYO 6TPE100MI	$C_{OUT(CHG)}$ (1) 4.7µF, 25V Taiyo Yuden TMK432BJ475KM Murata GRM31CR71E475M
Inductor	L3 1.5µH, 2.1mΩ, 11.8A Sumida CEP125S-1R5	L5 1.5µH, 2.1mΩ, 11.8A Sumida CEP125S-1R5	L_{CHG} 2µH, 19mΩ, 4.5A Sumida CDR7D28MN-2R0
High-Side MOSFET	N_{H3} 13A, 9.4mΩ/12mΩ, 30V Fairchild FDS6298	N_{H5} 13A, 9.4mΩ/12mΩ, 30V Fairchild FDS6298	N_{HC} 6.6A, 17mΩ/25mΩ, 30V International Rectifier IRF7807D1PBF
Low-Side MOSFET	N_{L3} 13A, 7.2mΩ/10mΩ, 30V Fairchild FDS6670A	N_{L5} 13A, 7.2mΩ/10mΩ, 30V Fairchild FDS6670A	N_{LC} 6.6A, 17mΩ/25mΩ, 30V International Rectifier IRF7807D1PBF
Current-Limit Setting	1.16V (1.16V limit) R_{ILIM3A} = 66.5kΩ R_{ILIM3B} = 82.5kΩ	1.16V (1.16V limit) R_{ILIM5A} = 66.5kΩ R_{ILIM5B} = 82.5kΩ	—

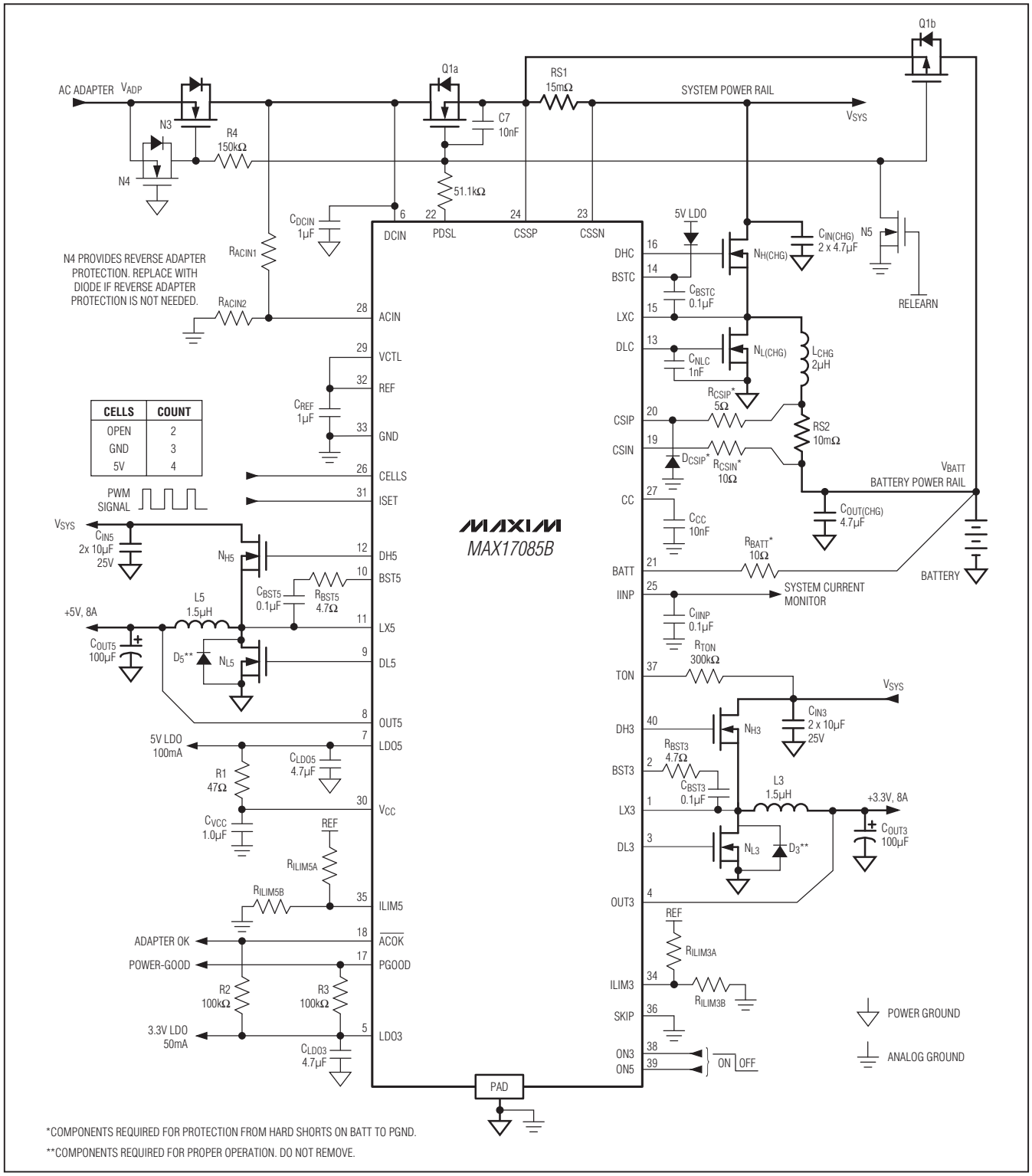


Figure 1. Standard Application Circuit

Table 2. Component Suppliers

SUPPLIER	WEBSITE
AVX Corp.	www.avxcorp.com
Central Semiconductor Corp.	www.centralsemi.com
Fairchild Semiconductor	www.fairchildsemi.com
International Rectifier	www.irf.com
KEMET Corp.	www.kemet.com
NEC/TOKIN America	www.nec-tokinamerica.com
Panasonic Corp.	www.panasonic.com/industrial
Philips/nxp Semiconductor	www.semiconductors.philips.com
Pulse Engineering	www.pulseeng.com
Renesas Technology Corp.	www.renesas.com
SANYO Electric Co., Ltd.	www.sanyodevice.com
Sumida Corp.	www.sumida.com
Taiyo Yuden	www.t-yuden.com
TDK Corp.	www.component.tdk.com
TOKO America, Inc.	www.tokoam.com
Vishay (Dale, Siliconix)	www.vishay.com
Würth Elektronik GmbH & Co. KG	www.we-online.com

Detailed Description

The MAX17085B integrated charger and main step-down controllers are ideal for notebook applications where board space and solution cost are key requirements. Together with the integrated, always-on 100mA LDO5 and 50mA LDO3, the MAX17085B provides a complete power solution for the notebook in the off-state, standby-state, and full active state. A functional diagram of the MAX17085B is shown in Figure 2.

Charger

The MAX17085B uses a new thermally optimized high-frequency architecture that reduces the output capacitance and inductance, resulting in smaller PCB area and lower cost. The MAX17085B charger includes all the necessary functions to charge Li+, NiMH, and NiCd batteries. An all n-channel synchronous-rectified step-down DC-DC converter is used to implement a precision constant-current, constant-voltage charger. The charge current and input current-limit sense amplifiers have low-input offset errors (200µV typ), allowing the use of small-valued sense resistors.

Main SMPS

The 5V and 3.3V main SMPSs in the MAX17085B use Maxim's Quick-PWM pulse-width modulator, specifically designed for handling fast load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The Quick-PWM architecture circumvents the poor load-transient timing problems of fixed-frequency current-mode PWMs while also avoiding the problems caused by widely varying switching frequencies in conventional constant-on-time and constant-off-time PWM schemes.

100mA 5V Linear Regulator (LDO5) and Bias Supply (VCC)

The MAX17085B includes a high-current (100mA), always-on fixed 5V linear regulator (LDO5). LDO5 is required to generate the 5V bias supply necessary to power up the switching regulators, and as the input supply to the 3.3V linear regulator (LDO3). Once the 5V switching regulator (SMPS5) is enabled and in regulation, LDO5 is bypassed by an internal switch from OUT5 to LDO5. After switchover, the LDO5 pin can source 200mA. LDO5 starts up as soon as DCIN has valid voltage (around 2.5V), and regulates to ~ 4.5V using an internal crude reference. REF starts at the same time, and once REF is in regulation, LDO5 switches over to use the accurate REF, and regulates up to 5V.

The MAX17085B requires a low-noise 5V bias supply (V_{CC}) for its internal circuitry. Typically, this 5V bias is supplied by LDO5 through a lowpass filter. The total supply current required for the MAX17085B is:

$$I_{BIAS(MAX)} = I_{CC(MAX)} + f_{SW5}Q_{G5} + f_{SW3}Q_{G3} + f_{SWC}Q_{GC} \approx 45mA \text{ to } 90mA \text{ (typ)}$$

50mA, 3.3V Linear Regulator (LDO3)

A lower current (50mA), always-on fixed 3.3V linear regulator, is also included in the MAX17085B. Once the 3.3V switching regulator (SMPS3) is enabled and in regulation, LDO3 is bypassed by an internal switch from OUT3 to LDO3. After switchover, the LDO3 pin can source more than 200mA. LDO3 starts up as soon as REF is in regulation. This limits the inrush current by sequencing LDO5 to start before LDO3.

Integrated Charger, Dual Main Step-Down Controllers, and Dual LDO Regulators

Thermal-Fault Protection (t_{SHDN})

The MAX17085B features a thermal fault-protection circuit. When the junction temperature rises above +160°C, a thermal sensor activates the fault latch, pulls PGOOD low, enables the 20Ω discharge circuit, and disables the controller—DH and DL pulled low. After the junction temperature cools by 50°C, the controller automatically restarts. This protects the internal LDO when a sustained overcurrent or output short circuit occurs.

POR, UVLO

When V_{CC} rises above the power-on reset (POR) threshold, the MAX17085B clears the fault latches and resets the soft-start circuit, preparing the controller for power-up. However, the V_{CC} undervoltage-lockout (UVLO) circuitry inhibits switching until V_{CC} reaches its 4.2V (typ) UVLO threshold.

When V_{CC} drops below the UVLO threshold (falling edge), the controller stops switching, pulling DH and DL low. When the 1.5V POR falling edge threshold is reached, the DL state no longer matters since there is not enough voltage to force the switching MOSFETs into a low on-resistance state, so the controller pulls DL high, allowing a soft discharge of the output capacitors (damped response). However, if the V_{CC} recovers before reaching the falling POR threshold, DL remains low until the error comparator has been properly powered up and triggers an on-time.

When DCIN is high enough for LDO5 to be in regulation and VCC to be above its UVLO, the main SMPS can begin running. Charger operation requires DCIN to be above its 7.7V UVLO threshold.

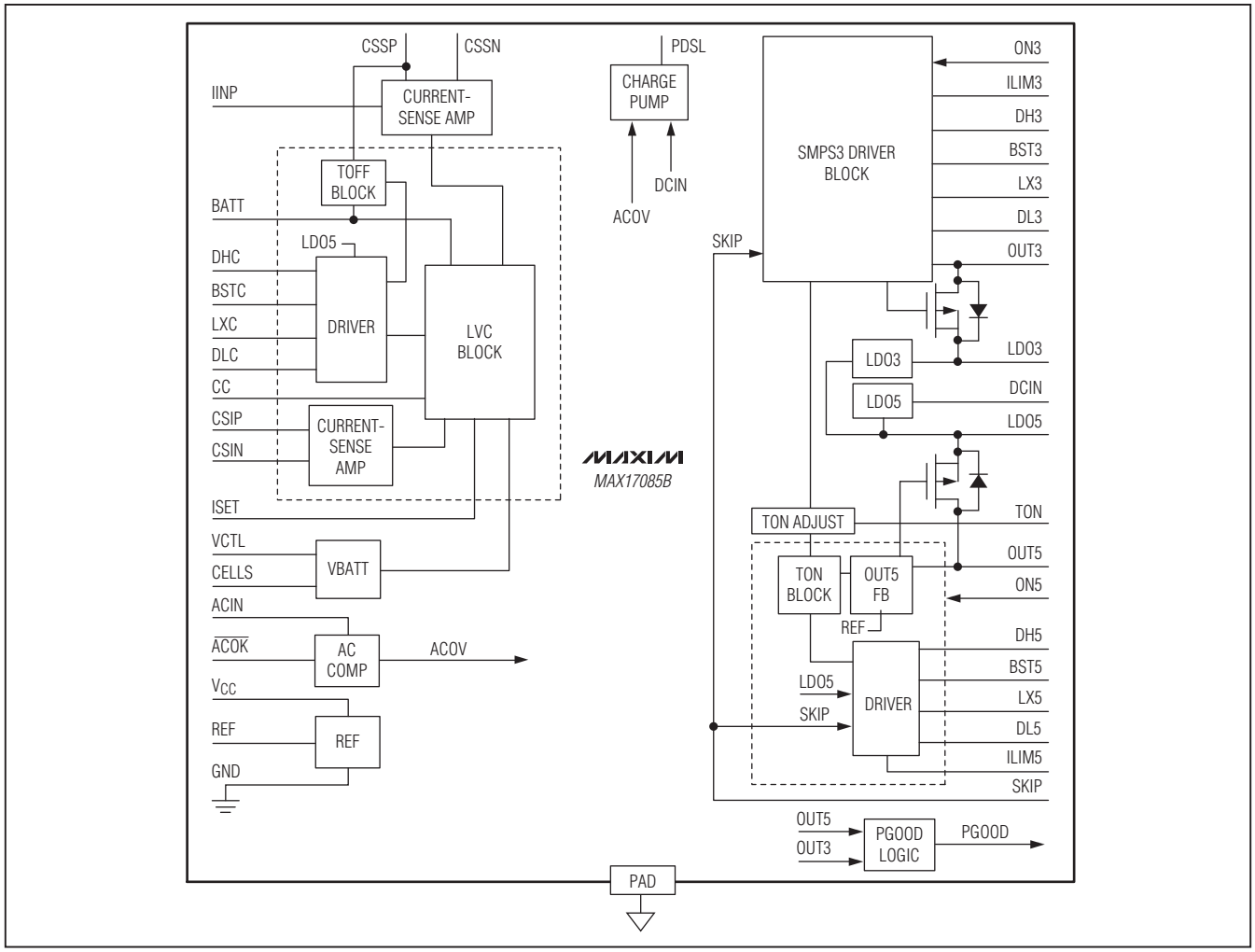


Figure 2. Functional Diagram

Integrated Charger, Dual Main Step-Down Controllers, and Dual LDO Regulators

Charger Detailed Description

The MAX17085B charger has three regulations loops: a voltage-regulation loop (CCV) and two current-regulation loops (CCI and CCS). The loops operate independently of each other. The CCV voltage-regulation loop monitors BATT to ensure that its voltage never exceeds the voltage set by VCTL and CELLS. The CCI battery charge current-regulation loop monitors current delivered to BATT to ensure that it never exceeds the current limit set by ISET. The charge current-regulation loop is in control as long as the battery voltage is below the set point. When the battery voltage reaches its set point, the voltage-regulation loop takes control and maintains the battery voltage at the set point. A third loop (CCS) takes control and reduces the charge current when the adapter current exceeds the input current limit. The CCI current loop is internally compensated while the CCS and CCV loops are externally compensated with a capacitor at the CC pin.

The new thermally optimized high-frequency architecture controls the power dissipation in the high-side MOSFET, resulting in reduced output capacitance and inductance.

Setting the Charge Voltage

The MAX17085B features separate control inputs to set the per-cell voltage and the number of cells in series. The VCTL input sets the per-cell voltage, while the CELLS input sets the total number of cells in series. Together, these two inputs set the charge voltage at the BATT input, providing a flexible way to support different cell types and different battery-pack configurations.

Setting the Per-Cell Charge Voltage (VCTL)

The MAX17085B supports charge voltages of 4.0V/cell to 4.4V/cell based on the following equation:

$$V_{BATT}/Cell = 2.083 \times V_{VCTL}$$

The dynamic range of the VCTL input is limited, so it is possible to achieve ±0.5% charge voltage accuracy using resistive voltage-dividers composed of 1% accurate resistors.

Figure 3 shows a simple method to set two different CELL voltages using a logic output from the embedded controller.

Connecting V_{VCTL} to V_{REF} = 2.10V, which gives 4.375V/cell.

Setting the Number of Cells (CELLS)

The trilevel CELLS input allows simple switching between 2, 3, and 4 cells in series.

Setting Charge Current (ISET)

The ISET input controls the voltage across current-sense resistor RS2. ISET can accept either analog or digital inputs. The full-scale differential voltage between CSIP and CSIN is 100mV (5A for RS2 = 20mΩ).

Important: Keep ISET low during the initial power-up of the MAX17085B. Wait 10ms to allow PDSL to reach its final voltage before enabling the battery charger.

Analog ISET

When the MAX17085B powers up and the charger is ready, if there are no two clock edges within 20ms, the circuit assumes ISET is an analog input, and disables the PWM filter block. For ISET analog input, set ISET according to the following equation:

$$I_{CHG} = \frac{100mV}{RS2} \times \frac{V_{ISET}}{V_{REF}}$$

The input range for ISET is from 0 to REF. To shut down the charger, pull ISET below 26mV.

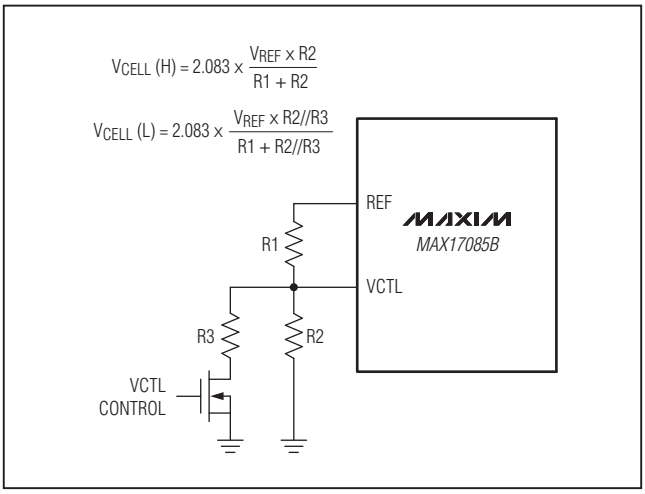


Figure 3. VCTL Setting

Table 3. CELLS Pin Setting

CELLS PIN VOLTAGE	CELLS COUNT	SETTING
OPEN	2	Charge with 2 times the cell voltage programmed at VCTL
GND	3	Charge with 3 times the cell voltage programmed at VCTL
> 2.8V	4	Charge with 4 times the cell voltage programmed at VCTL

Digital ISET

If there are two clock edges on ISET within 20ms, the PWM filter is enabled and ISET accepts digital PWM input. The PWM filter accepts the digital signal with a frequency from 128Hz to 500kHz. Zero duty cycle shuts down the MAX17085B, and the 99% duty cycle corresponds to full scale (100mV) across CSIP and CSIN. The PWM filter has a DAC with 8-bit resolution that corresponds to equivalent V_{CSIP} - V_{CSIN} steps. Each step is:

$$V_{STEP} = \frac{V_{REF}}{256 \cdot 21} = 0.391mV \text{ (7.8mA with } RS2 = 20m\Omega)$$

Choose a current-sense resistor (RS2) to have a sufficient power dissipation rating to handle the full-charge current. The current-sense voltage may be reduced to minimize the power dissipation period. However, this may degrade accuracy due to the current-sense amplifier's input offset (200µV). See the *Typical Operating Characteristics* to estimate the charge-current accuracy at various set points.

Input Source Current

Setting Input Current Limit

The total input current, from a wall adapter or other DC source, is the sum of the system supply current and the current required by the charger. When the input current exceeds the set input current limit, the controller decreases the charge current to provide priority to system load current. System current normally fluctuates as portions of the system are powered up or down. The input-current-limit circuit reduces the power requirement of the AC wall adapter, which reduces adapter cost. As the system supply rises, the available charge current drops linearly to zero. Thereafter, the total input current can increase without limit. The total input current can be estimated as follows:

$$I_{INPUT} = I_{LOAD} + \frac{I_{CHG} \times V_{BATT}}{V_{ADP} \times \eta}$$

where η is the efficiency of the DC-to-DC converter (typically 85% to 95%).

In the MAX17085B, the voltage across CSSP and CSSN is constant at 60mV. Choose the current-sense resistor, RS1, to set the input current limit. For example, for 4A input current limit choose RS1 = 15mΩ. For the input current-limit settings, which cannot be achievable with standard sense resistor values, use a resistive voltage-divider between CSSP and CSSN to tune the setting.

AC Adapter Overcurrent (ACOC)

When the input current is 1.3 times the input current-limit setting, PDSL is pulled to GND after a 16ms blanking time. This turns off the adapter switch and enables the battery selector switch. After 0.6s, PDSL is reenabled. If the fault condition persists, the cycle is repeated, until the third time when the charger is latched off. To clear the fault latch, remove the adapter and allow DCIN to fall below its UVLO threshold before reinserting the adapter.

Analog Input Current-Monitor Output

IINP monitors the system-input current, which is sensed across CSSP and CSSN. The voltage at IINP is proportional to the input current:

$$V_{IINP} = G_{IINP} \times I_{ADP} \times RS1$$
$$V_{IINP} = 60 \times (V_{CSSP} - V_{CSSN})$$

where I_{ADP} is the DC current supplied by the AC adapter, G_{IINP} is the transconductance of the sense amplifier (60V/V typ), and RS1 is the resistor connected between CSSP and CSSN.

When the adapter is absent, drive ISET above 2.1V to enable IINP during battery discharge.

AC Adapter Detection (ACIN, $\overline{ACOK}$, ACOV)

The ACIN input goes to two internal comparators, one for adapter detection ($\overline{ACOK}$) and another for adapter overvoltage detection (ACOV). When ACIN is above 1.5V, the open-drain $\overline{ACOK}$ output becomes low impedance after 44ms.

When ACIN rises above 2.1V, the MAX17085B detects an ACOV condition and immediately pulls PDSL to GND, turning off the adapter selection switch and enabling the battery selector switch. This protects the system rail from excessively high voltages that might violate the absolute maximum ratings of the downstream components. Note that $\overline{ACOK}$ remains low even when ACIN is above the ACOV threshold.

Use a resistive voltage-divider from the adapter's output to the ACIN pin to set the appropriate detection threshold. Connect a 100kΩ pullup resistor between LDO3 or LDO5 and $\overline{ACOK}$.

Automatic Power-Source Selection (PDSL)

The MAX17085B integrates a charge pump to drive the gate of n-channel adapter selector switches (N3 and Q1a) and the p-channel battery-selector switch (Q1b). When the adapter is present, PDSL is driven 8V above V_{DCIN} so that N3 and Q1a are on, and Q1b is off. See the *Operating Conditions* section for the definition of adapter present.

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Table 4. Charger Operating Mode Truth Table

DCIN	ADAPTER PRESENT (NOTE 5)	INPUT CURRENT V_{CSSP} - V_{CSSN}	ACIN	ISET	PDSL	CHARGER STATE	IINP	COMMENTS
X	No	X	X	< 1V	GND	OFF	OFF	—
X	No	X	X	> 1V	GND	OFF	ON	—
< UVLO	Yes	> OCP threshold	X	X	GND	OFF	ON	—
< UVLO	Yes	X	V_{ACIN} > V_{ACINOV}	X	GND	OFF	ON	—
< UVLO	Yes	< OCP threshold	V_{ACINOK} < V_{ACIN} and V_{ACIN} < V_{ACINOV}	X	V_{DCIN} + 8V	OFF	ON	—
> UVLO	Yes	X	V_{ACINOK} < V_{ACIN} and V_{ACIN} < V_{ACINOV}	X	GND	OFF	ON	Adapter overvoltage fault
> UVLO	Yes	> OCP threshold	X	X	GND	OFF	ON	Adapter overcurrent fault
> UVLO	Yes	< OCP threshold	V_{ACINOK} < V_{ACIN} and V_{ACIN} < V_{ACINOV}	< ISET shutdown threshold	V_{DCIN} + 8V	OFF	ON	ISET shutdown
> UVLO	Yes	< OCP threshold	< ACOV threshold	> ISET shutdown threshold	V_{DCIN} + 8V	ON (ISET control)	ON	—

Note 5: Adapter is present when V_{DCIN} - V_{CSIN} > 420mV with V_{DCIN} rising, and absent when V_{DCIN} - V_{CSIN} < 120mV with V_{DCIN} falling.

When the adapter voltage is removed and the adapter is absent, the charger is disabled and PDSL is pulled to GND. N3 and Q1a turn off, and Q1b turns on to supply power to the system from the battery.

Operating Conditions

Table 4 defines the MAX17085B charger operating conditions.

Charger SMPS

The MAX17085B employs a synchronous step-down DC-DC converter with an n-channel high-side MOSFET switch and an n-channel low-side synchronous rectifier. The charger features a controlled inductor current ripple architecture, current-mode control scheme with cycle-by-cycle current limit. The controller's off-time (t_{OFF}) is adjusted to keep the high-side MOSFET junction temperature constant. In this way, the controller switches faster when the high-side MOSFET has available thermal capacity. This allows the inductor current ripple and the output voltage ripple to decrease so that smaller and cheaper components can be used. The controller can also operate in discontinuous conduction mode for improved light-load efficiency.

The operation of the DC-to-DC controller is determined by the following five comparators as shown in the functional diagram in Figures 2 and 4:

- The **IMIN** comparator triggers a pulse in discontinuous mode when the accumulated error is too high. IMIN compares the control signal (LVC) against 5mV (typ) (referred at V_{CSIP} - V_{CSIN}). When LVC is less than 5mV, DHC and DLC are both forced low. Indirectly, IMIN sets the peak inductor current in discontinuous mode.
- The **CCMP** comparator is used for current-mode regulation in continuous conduction mode. CCMP compares LVC against the inductor current. The high-side MOSFET on-time is terminated when the CSI voltage is higher than LVC.
- The **IMAX** comparator provides a secondary cycle-by-cycle current limit. IMAX compares CSI to the current limit programmed at ISET. The high-side MOSFET on-time is terminated when the current-sense signal exceeds the programmed limit. A new

cycle cannot start until the IMAX comparator's output goes low.

- The **ZCMP** comparator provides zero-crossing detection during discontinuous conduction. ZCMP compares the current-sense feedback signal to 10mV. When the current-sense signal is lower than the 10mV threshold, the comparator output is high and DLC is turned off.
- The **OV** comparator is used to prevent overvoltage at the output due to battery removal. OV compares BATT against the VCTL and CELLS settings. When BATT is 40mV/cell above the set value, the OV comparator output goes high and the high-side MOSFET on-time is terminated. DHC and DLC remain off until the OV condition is removed.

CCV, CCI, CCS, and LVC Control Blocks

The MAX17085B controls input current (CCS control loop), charge current (CCI control loop), or charge voltage (CCV control loop), depending on the operating condition. The three control loops—CCV, CCI, and CCS—are brought together internally at the lowest voltage clamp (LVC) amplifier. The output of the LVC amplifier is the feedback control signal for the DC-DC controller. The minimum voltage at the CCV, CCI, or CCS appears at the output of the LVC amplifier and clamps the other control loops to within 0.3V above the control point. Clamping the other two control loops close to the lowest control loop ensures fast transition with minimal overshoot when switching between different control loops (see the *Compensation* section). The CCI loop is compensated internally, while the CCS and CCV loops are compensated externally using a shared capacitor on the CC pin.

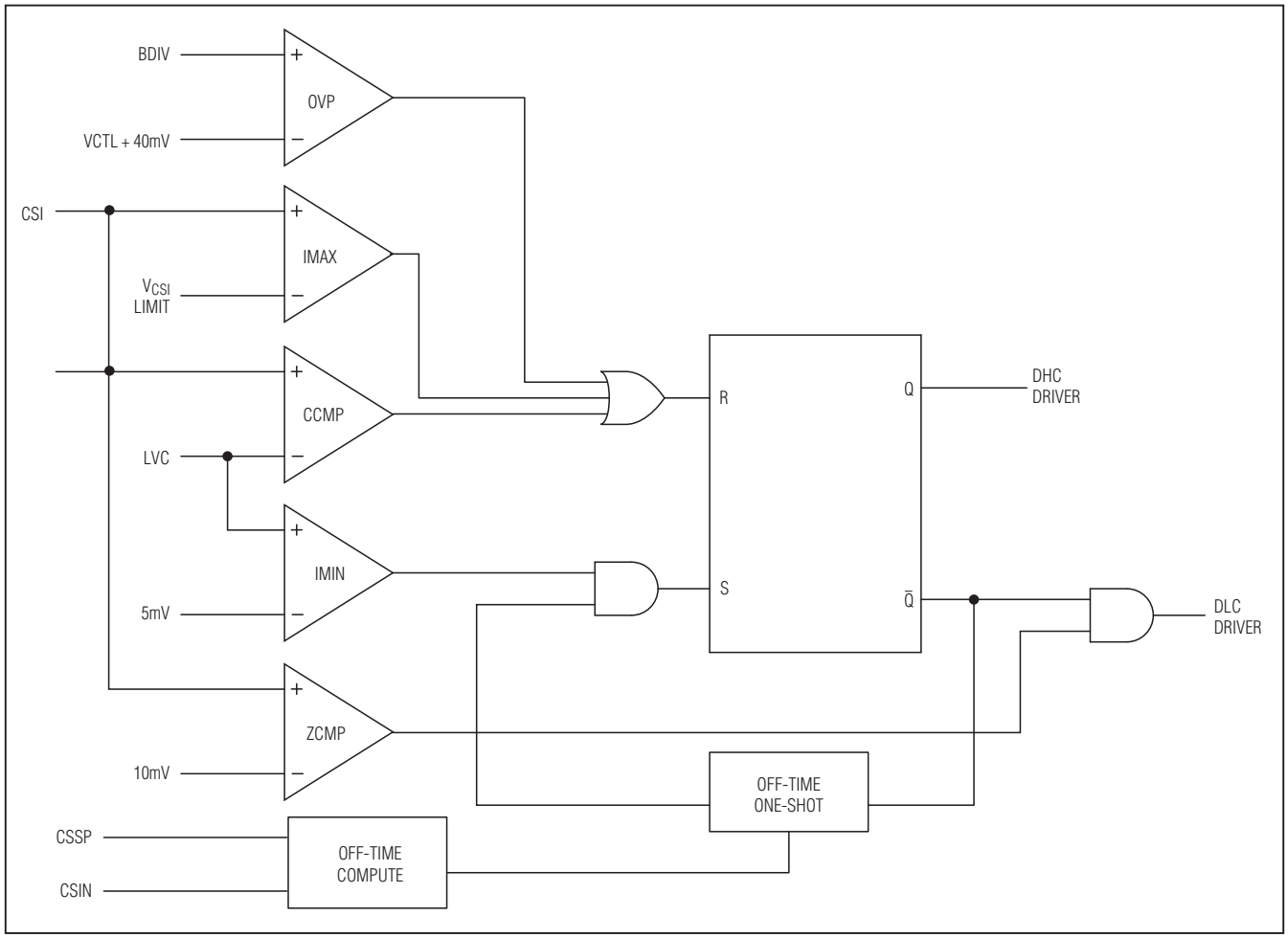

Figure 4. Charger Functional Diagram

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Continuous Conduction Mode

With sufficiently large charge current, the MAX17085B's inductor current never crosses zero, which is defined as continuous conduction mode. The controller starts a new cycle by turning on the high-side MOSFET and turning off the low-side MOSFET. When the charge-current feedback signal (CSI) is greater than the control point (LVC), the CCMP comparator output goes high and the controller initiates the off-time by turning off the high-side MOSFET and turning on the low-side MOSFET. The operating frequency is governed by the off-time and is dependent upon VCSIN and VDCIN.

The on-time can be determined using the following equation:

$$t_{ON} = \frac{L \times I_{RIPPLE}}{V_{DCIN} - V_{BATT}}$$

where:

$$I_{RIPPLE} = \frac{V_{BATT} \times t_{OFF}}{L}$$

The switching frequency can then be calculated:

$$f_{SW} = \frac{1}{t_{ON} + t_{OFF}}$$

At the end of the computed off-time, the controller initiates a new cycle if the control point (LVC) is greater than 5mV (referred at $V_{CSIP} - V_{CSIN}$), and the peak charge current is less than the cycle-by-cycle current limit. Restated another way, IMIN must be high, IMAX must be low, and OVP must be low for the controller to initiate a new cycle. If the peak inductor current exceeds IMAX comparator threshold or the output voltage exceeds the OVP threshold, then the on-time is terminated. The cycle-by-cycle current limit effectively protects against overcurrent and short-circuit faults.

If during the off-time the inductor current goes to zero, the ZCMP comparator output pulls high, turning off the low-side MOSFET. Both the high- and low-side MOSFETs are turned off until another cycle is ready to begin. ZCMP causes the MAX17085B to enter into the discontinuous conduction mode (see the *Discontinuous Conduction* section).

Discontinuous Conduction

The MAX17085B can also operate in discontinuous conduction mode to ensure that the inductor current is always positive. The MAX17085B enters discontinuous conduction mode when the output of the LVC control point falls below 5mV (referred at $V_{CSIP} - V_{CSIN}$). For RS2 = 20mΩ, this corresponds to peak inductor current to be 250mA.

In discontinuous mode, a new cycle is not started until the LVC voltage rises above 5mV. Discontinuous mode operation can occur during a conditioning charge of overdischarged battery packs, when the charge current has been reduced sufficiently by the CCS control loop, or when the charger is in constant-voltage mode with a nearly full battery pack.

Compensation

The charge voltage, charge current, and input current-limit regulation loops are compensated separately and independently. The charge-current limit loop, CCI, is compensated internally, while the input current limit and charge-voltage loops, CCS and CCV, are compensated externally using a shared capacitor at the CC pin. For most applications, it is sufficient to place a 10nF capacitor from CC to GND.

Main SMPS Detailed Description

The main SMPS of the MAX17085B consists of two independent switching regulators that generate a 3.3V and a 5V output. The regulators use the Quick-PWM control architecture for simplicity, low pin count, and fast transient response. An extended on-time feature further improves output voltage sag for high-duty-cycle applications.

Free-Running Constant-On-Time PWM Controller with Input Feed-Forward

The Quick-PWM control architecture is a pseudo-fixed-frequency, constant on-time, current-mode regulator with voltage feed-forward. This architecture relies on the output filter capacitor's ESR to act as a current-sense resistor, so the feedback ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage. Another one-shot sets a minimum off-time (270ns typ). The on-time one-shot is triggered if the error comparator is low, the low-side switch current is below the valley current-limit threshold, and the minimum off-time one-shot has timed out.

On-Time One-Shot

The heart of the PWM core is the one-shot that sets the high-side switch on-time. This fast, low-jitter, adjustable one-shot includes circuitry that varies the on-time in response to battery and output voltage. The high-side switch on-time is inversely proportional to the battery voltage as sensed by the TON input, and proportional to the output voltage:

$$t_{ON5} = V_{OUT5}/V_{SYSTEM} \times t_{SW(NOM)}/1.1$$

$$t_{ON3} = V_{OUT3}/V_{SYSTEM} \times t_{SW(NOM)}/0.9$$

$$t_{SW(NOM)} = C_{TON} \times R_{TON} + 6.5k\Omega$$

where C_{TON} = 6pF.

High-frequency (~ 600kHz nominal) operation optimizes the application for the smallest component size. Efficiency trade-off due to higher switching losses is not so significant for higher output voltage rails like 5V and 3.3V.

For continuous conduction operation, the actual switching frequency can be estimated by:

$$f_{SW} = \frac{V_{OUT} + V_{DIS}}{t_{ON}(V_{SYS} + V_{CHG})}$$

where V_{DIS} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PCB resistances; V_{CHG} is the sum of the resistances in the charging path, including the high-side switch, inductor, and PCB resistances; and t_{ON} is the on-time calculated by the MAX17085B.

Extended On-Time

During heavy load transients, the main SMPS can issue an extended on-time to increase the inductor current ramp and reduce output voltage sag, thereby reducing output capacitance requirement. The extended on-time feature is ideal for high-duty-cycle conditions where the voltage across the inductor (V_{SYS} - V_{OUT}) is less than the output voltage. The extended on-time is twice as long as the normal on-time. A minimum off-time follows after each extended on-time.

The extended on-time is allowed when the following conditions are met:

- Inductor valley current at the start of the first on pulse is less than 50% of the current-limit setting.
- Greater than 50% duty cycle.

Modes of Operation

Forced-PWM Mode (SKIP = 1.8V)

The low-noise forced-PWM mode (SKIP = 1.8V) disables the zero-crossing comparator, which controls the low-side switch on-time. This forces the low-side gate-drive waveform to constantly be the complement of the high-side gate-drive waveform, so the inductor current reverses at light loads while DH maintains a duty factor of V_{OUT}/V_{SYS}. The benefit of forced-PWM mode is to keep the switching frequency fairly constant. However, forced-PWM operation comes at a cost: the no-load 5V bias current remains between 15mA to 35mA per phase at 600kHz, depending on the MOSFET selection.

Automatic Pulse-Skipping Mode (SKIP = 3.3V or 5V)

In skip mode (SKIP = 3.3V or 5V), an inherent automatic switchover to PFM takes place at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing sensed across LX and AGND. In discontinuous conduction (SKIP = 3.3V or 5V, and $I_{OUT} < I_{LOAD(SKIP)}$), the output voltage has a DC regulation level higher than the error comparator threshold.

Ultrasonic Mode (SKIP = GND)

Forcing SKIP low (SKIP = GND) activates a unique pulse-skipping mode with a minimum switching frequency of 20kHz. This ultrasonic pulse-skipping mode eliminates audio-frequency modulation that would otherwise be present when a lightly loaded controller automatically skips pulses. In ultrasonic mode, the controller automatically transitions to fixed-frequency PWM operation when the load reaches the same critical conduction point ($I_{LOAD(SKIP)}$) that occurs when normally pulse skipping.

An ultrasonic pulse occurs (Figure 5) when the controller detects that no switching has occurred within the last 45µs. Once triggered, the ultrasonic circuitry pulls DL high, turning on the low-side MOSFET. This induces a negative inductor current. A negative current limit of 72mV protects against excessive negative currents when DL is turned on.

After the output drops below the regulation voltage, the controller turns off the low-side MOSFET (DL pulled low) and triggers a constant on-time (DH driven high). When the on-time has expired, the controller reenables the low-side MOSFET until the inductor current drops below the zero-crossing threshold. Starting with a DL pulse greatly reduces the peak output voltage when compared to starting with a DH pulse.

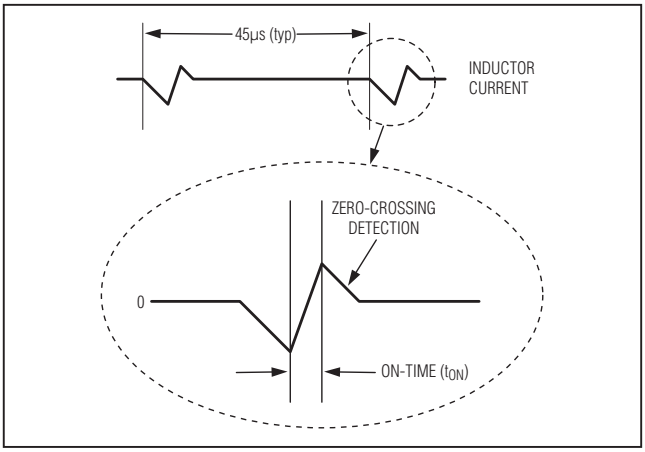

Figure 5. Ultrasonic Waveforms

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Valley Current-Limit Protection

The current-limit circuit employs a unique "valley" current-sensing algorithm that senses the inductor current through the low-side MOSFET, across LX to AGND. If the current through the low-side MOSFET exceeds the valley current-limit threshold, the PWM controller is not allowed to initiate a new cycle. The actual peak current is greater than the valley current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the inductor value and battery voltage. When combined with the UVP, this current-limit method is effective in almost every circumstance.

Soft-Start and Soft-Shutdown

The MAX17085B includes voltage soft-start and passive soft-shutdown. During startup, the slew rate control softly slews the internal target voltage over a 2ms startup period. This long startup period reduces the inrush current during startup. Startup is always in skip mode regardless of the SKIP pin setting.

When ON3 or ON5 is pulled low, or the output undervoltage fault latch is set, the regulator immediately forces DL and DH low, and enables the internal 20Ω discharge FET from the OUT pin to GND.

Output Voltage

When the inductor continuously conducts, the MAX17085B regulates the valley of the output ripple, so the actual DC output voltage is lower than the slope compensated trip level by 50% of the output ripple voltage. For PWM operation (continuous conduction), the output voltage is accurately defined by the following equation:

$$V_{OUT} = V_{NOM} + \frac{V_{RIPPLE}}{2}$$

where V_{NOM} is the nominal feedback voltage and V_{RIPPLE} is the output ripple voltage (V_{RIPPLE} = ESR x $\Delta I_{INDUCTOR}$ as described in the *Output Capacitor Selection* section).

In discontinuous conduction ($I_{OUT} < I_{LOAD(SKIP)}$), the longer off-times allow the slope compensation to increase the threshold voltage by as much as 1%, so the output voltage regulates slightly higher than it would in PWM operation.

Power-Good Output (PGOOD)

PGOOD is the open-drain output that continuously monitors the output voltage for undervoltage and overvoltage conditions. PGOOD is actively held low when either output voltage is more than 250mV (typ) below the nominal regulation threshold, during soft-start, in shutdown (ON3 = ON5 = GND), and after either fault latch has been tripped. After the soft-start circuit has terminated, PGOOD becomes high impedance if the output is in regulation plus 200µs.

When only one SMPS is active, PGOOD monitors the active SMPS output. When the 2nd SMPS is started, PGOOD is blanked high-Z during the 2nd SMPS soft-start plus 200µs, then PGOOD monitors both SMPS outputs.

For a logic-level PGOOD output voltage, connect an external pullup resistor between PGOOD and LDO3. A 100kΩ pullup resistor works well in most applications.

Fault Protection

The main SMPS features overvoltage and undervoltage fault protection that shuts down the SMPS. To prevent false trips from latching off the main SMPS, the fault latch is automatically reset after approximately 7ms. If the ON pins are still high, the respective SMPS restarts. If the fault is still present, the shutdown and restart cycle repeats. After the 4th time, the latch is permanently set and requires toggling ON3 or ON5, or pulling VCC below UVLO to start again.

The charger operation is not affected by the SMPS faults.

Overvoltage Protection (OVP)

When the output voltage rises 16% above the fixed regulation voltage, the controller immediately pulls PGOOD low, sets the overvoltage fault latch, and immediately pulls the respective DL high, clamping the output fault to GND. The nonfaulted side also enters the shutdown state.

Undervoltage Protection (UVP)

When the output voltage drops 30% below the fixed regulation voltage and the inductor current exceeds the current limit, the controller immediately pulls PGOOD low, sets the undervoltage fault latch, and discharges both SMPS outputs.

Table 5. Main SMPS Fault Protection and Shutdown Operation

MODE	CONTROLLER STATE	DRIVER STATE
Shutdown (ON_ = High to Low)	Internal error amplifier target immediately resets to GND.	DL and DH immediately pulled low; 20Ω output discharge active.
Output UVP (Latched with 4 Autorestarts)	Internal error amplifier target immediately resets to GND. After ~ 7ms timeout, the controller restarts if ON_ is still high.	DL and DH immediately pulled low; 20Ω output discharge active.
Output OVP (Latched with 4 Autorestarts)	Controller shuts down and the internal error amplifier target resets to GND. After ~ 7ms timeout, the controller restarts if ON_ is still high.	DL immediately driven high; DH pulled low; 20Ω output discharge active.
Thermal Fault (Latched with 4 Autorestarts)	SMPS controller disabled (assuming ON_ pulled high). Internal error amplifier target immediately resets to GND. After the die temperature falls by ~ 50°C, the controller restarts if ON_ is still high.	DL and DH pulled low; 20Ω output discharge active.
V_{CC} UVLO Falling Edge	SMPS controller disabled (assuming ON_ pulled high), internal error amplifier target immediately resets to GND.	DL and DH pulled low; 20Ω output discharge active.
V_{CC} UVLO Rising Edge	SMPS controller enabled (assuming ON_ pulled high), controller ramps up the output to the preset voltage.	DL and DH held low and 20Ω output discharge active until V_{CC} passes the UVLO threshold.
V_{CC} POR	SMPS inactive.	DL and DH pulled low; 20Ω output discharge active.

Charger Design Procedure

Inductor Selection

The selection criteria for the inductor trades off efficiency, transient response, size, and cost. The MAX17085B's charger combines all the inductor trade-offs in an optimum way using the high-frequency current-mode architecture. High-frequency operation permits the use of a smaller and cheaper inductor, and consequently results in smaller output ripple and better transient response.

The charge current, ripple, and operating frequency (off-time) determine the inductor characteristics. For optimum efficiency, choose the inductance according to the following equation:

$$L_{CHG} = \frac{kV_{ADP}^2}{4 \times LIR_{MAX} \times I_{CHG}}$$

where k = 35ns/V.

For optimum size and inductor current ripple, choose LIR_{MAX} = 0.4, which sets the ripple current to 40% of the charge current and results in a good balance between inductor size and efficiency. Higher inductor values decrease the ripple current. Smaller inductor values save cost but require higher saturation current capabilities and degrade efficiency.

Inductor L_{CHG} must have a saturation current rating of at least the maximum charge current plus 1/2 of the ripple current (ΔIL):

$$I_{SAT} = I_{CHG} + \frac{\Delta IL_{CHG}}{2}$$

The ripple current is determined by:

$$\Delta IL_{CHG} = \frac{kV_{ADP}^2}{4 \cdot L_{CHG}}$$

Output Capacitor Selection

The output capacitor absorbs the inductor ripple current and must tolerate the surge current delivered from the battery when it is initially plugged into the charger. As such, both capacitance and ESR are important parameters in specifying the output capacitor as a filter. Beyond the stability requirements, it is often sufficient to make sure that the output capacitor's ESR is much lower than the battery's ESR. Either tantalum or ceramic capacitors can be used on the output. Ceramic devices are preferable because of their good voltage ratings and resilience to surge currents. Choose the output capacitor based on:

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$$C_{OUT(CHG)} = \frac{I_{RIPPLE}}{f_{SW} \times 8 \times \Delta V_{BATT}} \times k_{CAP\text{-}BIAS}$$

where $k_{CAP-BIAS}$ is the derating factor for the capacitor due to DC voltage bias; $k_{CAP-BIAS}$ is typically 2 for 25V rated capacitors.

For f_{SW} = 1.2MHz, I_{RIPPLE} = 1A, ΔV_{BATT} = 70mV, 4.7µF is the closest common capacitor for $C_{OUT(CHG)}$.

If the internal resistance of the battery is close to the ESR of the output capacitor, the voltage ripple is shared with the battery, and is less than calculated.

Main SMPS Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

- **Input Voltage Range:** The maximum value ($V_{SYS(MAX)}$) must accommodate the worst-case, high AC-adapter voltage. The minimum value ($V_{SYS(MIN)}$) must account for the lowest battery voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.
- **Maximum Load Current:** There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components.
- **Switching Frequency:** This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage due to MOSFET switching losses that are proportional to frequency and V_{IN}^2. The optimum frequency is also a moving target, due to rapid improvements in MOSFET technology that are making higher frequencies more practical.
- **Inductor Operating Point:** This choice provides trade-offs between size vs. efficiency and transient response vs. output ripple. Low inductor values provide better transient response and smaller physical size, but also result in lower efficiency and higher output ripple due to increased ripple currents. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 20% and 50% ripple current. For high-duty-cycle applications, select an LIR value of ~ 0.4. When pulse skipping (SKIP high and light loads), the inductor value also determines the load-current value at which PFM/PWM switchover occurs.

Inductor Selection

The switching frequency and inductor operating point determine the inductor value as follows:

$$L = \frac{V_{OUT}(V_{SYS} - V_{OUT})}{V_{SYS} f_{SW} I_{LOAD(MAX)} LIR}$$

For example: $I_{LOAD(MAX)}$ = 8A, V_{SYS} = 12V, V_{OUT} = 5V, f_{SW} = 600kHz, 40% ripple current or LIR = 0.4:

$$L = \frac{5V \times (12V - 5V)}{12V \times 600kHz \times 8A \times 0.4} = 1.5\mu H$$

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{LOAD(MAX)}\left(1 + \frac{LIR}{2}\right)$$

Most inductor manufacturers provide inductors in standard values, such as 1.0µH, 1.5µH, 2.2µH, 3.3µH, etc. Also look for nonstandard values, which can provide a better compromise in LIR across the input voltage range. If using a swinging inductor (where the no-load inductance decreases linearly with increasing current), evaluate the LIR with properly scaled inductance values.

Output Capacitor Selection

Output capacitor selection is determined by the controller stability requirements, and the transient soar and sag requirements of the application.

Output Capacitor ESR

The output filter capacitor must have low enough equivalent series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements.

For processor core voltage converters and other applications where the output is subject to violent load transients, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$R_{ESR} \le \frac{V_{STEP}}{\Delta I_{LOAD(MAX)}}$$

In applications without large and fast load transients, the output capacitor's size often depends on how much ESR is needed to maintain an acceptable level of output voltage ripple. The output voltage ripple of a step-down controller equals the total inductor ripple current multiplied by the output capacitor's ESR. Therefore, the maximum ESR required to meet ripple specifications is:

$$R_{ESR} \le \frac{V_{RIPPLE}}{I_{LOAD(MAX)}LIR}$$

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of tantalums, OS-CONs, polymers, and other electrolytics).

When using low-capacity filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent VSAG and VSOAR from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the *Transient Response* section). However, low-capacity filter capacitors typically have high ESR zeros that may affect the overall stability (see the *Output Capacitor Stability Considerations* section).

Output Capacitor Stability Considerations

For Quick-PWM controllers, stability is determined by the value of the ESR zero relative to the switching frequency. The boundary of instability is given by the following equation:

$$f_{ESR} \le \frac{f_{SW}}{\pi}$$

where:

$$f_{ESR} = \frac{1}{2\pi R_{ESR} C_{OUT}}$$

For a typical 600kHz application, the ESR zero frequency must be well below 200kHz, preferably below 100kHz. Tantalum and OS-CON capacitors in widespread use at the time of publication have typical ESR zero frequencies of 25kHz. In the design example used for inductor selection, the ESR needed to support 25mVP-P ripple is 25mV/1.2A = 20.8mΩ. One 220µF/4V SANYO polymer (TPE) capacitor provides 15mΩ (max) ESR. This results in a zero at 48kHz, well within the bounds of stability.

Do not put high-value ceramic capacitors directly across the feedback sense point without taking precautions to ensure stability. Large ceramic capacitors can have a high ESR zero frequency and cause erratic, unstable operation. Unstable operation manifests itself in two related but distinctly different ways: double-pulsing and fast-feedback loop instability. Double-pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output voltage signal. This "fools" the error comparator into triggering a new cycle immediately after the 400ns minimum off-time period has expired. Double-pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability due to insufficient ESR. Loop instability results in oscillations at the output after line or load steps. Such perturbations are usually damped, but can cause the output voltage to rise above or fall below the tolerance limits.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output voltage ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under/overshoot.

Transient Response

The inductor ripple current also impacts transient-response performance, especially at low VSYS - VOUT differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. This favors higher switching-frequency operation.

The SMPSs include an extended on-time feature that reduces the output capacitor requirements due to heavy load transients. The capacitance required is also a function of the maximum duty factor and can be calculated from the following equation:

$$C_{OUT} \ge \frac{L\left(\Delta I_{LOAD(MAX)}\right)^2 K}{2V_{SAG}V_{OUT}}$$

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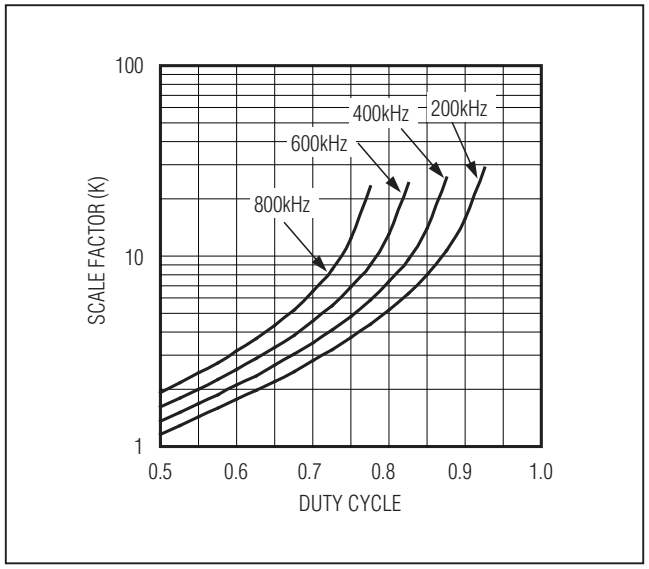

Figure 6. Scale Factor vs. Duty Cycle

where K is a function of maximum duty cycle (lowest input voltage) and switching frequency as shown in Figure 6.

The amount of overshoot during a full-load to no-load transient due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{\left(\Delta I_{LOAD(MAX)}\right)^2 L}{2 C_{OUT} V_{OUT}}$$

Setting the Current Limit

The minimum current-limit threshold must be great enough to support the maximum load current when the current limit is at the minimum tolerance value. The valley of the inductor current occurs at $I_{LOAD(MAX)}$ minus half the ripple current; therefore:

$$I_{LIM(VAL)} > I_{LOAD(MAX)} - \left(\frac{I_{LOAD(MAX)} LIR}{2}\right)$$

where $I_{LIM(VAL)}$ equals the minimum valley current-limit threshold voltage divided by the current-sense element (low-side R_{DSON}).

Connect a resistor-divider from REF to ILIM to analog ground (AGND) to set the adjustable current-limit threshold. The valley current-limit threshold is approximately 1/10 the ILIM voltage over a 0.2V to 2.1V range. The adjustment range corresponds to a 20mV to 210mV valley current-limit threshold. When adjusting the current limit, use 1% tolerance resistors to prevent significant inaccuracy in the valley current-limit tolerance.

Common Design Procedure

The input capacitor and MOSFET selection criteria share common considerations for the charger and the main SMPS. For the following sections, V_{IN} is V_{DCIN} for the charger and VSYS for the main SMPS, V_{OUT} is V_{BATT} for the charger and V_{OUT5} or V_{OUT3} for the main SMPS, and I_{OUT} is I_{CHG} for the charger and I_{LOAD} for the main SMPS.

Input Capacitor Selection

The input capacitor must meet the ripple-current requirement (IRMS) imposed by the switching currents:

$$I_{RMS} = I_{LOAD}\left(\frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}\right)$$

For most applications, nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to power-up surge currents typical of systems with a mechanical switch or connector in series with the input. In either configuration, choose a capacitor that has less than 10°C temperature rise at the RMS input current for optimal reliability and lifetime.

Power-MOSFET Selection

High-Side MOSFET Power Dissipation

The conduction loss in the high-side MOSFET (N_H) is a function of the duty factor, with the worst-case power dissipation occurring at the minimum input voltage, and maximum output voltage in the case of the charger:

$$PD_{COND}(HS) = \frac{V_{OUT}}{V_{IN}} \times I_{OUT}^2 \times RDS(ON)$$

Calculating the switching losses in high-side MOSFET (N_H) is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PCB layout characteristics. The following switching-loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on NH:

$$PD_{SW}(HS) = V_{IN} I_{OUT} f_{SW}\left(\frac{Q_{G(SW)}}{I_{GATE}}\right) + \frac{C_{OSS} V_{IN}^2 f_{SW}}{2}$$

where C_{OSS} is the NH MOSFET's output capacitance, $Q_{G(SW)}$ is the charge needed to turn on the N_H MOSFET, and I_{GATE} is the peak gate-drive source/sink current (2A typ).

The following high-side MOSFET's loss is due to the reverse-recovery charge of the low-side MOSFET's body diode:

$$PD_{QRR}(HS) = \frac{Q_{RR} \times V_{IN} \times f_{SW}}{2}$$

The total high-side MOSFET power dissipation is:

$$PD_{TOTAL}(HS) \approx PD_{COND}(HS) + PD_{SW}(HS) + PD_{QRR}(HS)$$

The optimum high-side MOSFET trades the switching losses with the conduction ($R_{DS(ON)}$) losses over the input and output voltage ranges. For the charger, the losses at $V_{OUT(MIN)}$ should be roughly equal to the losses at $V_{OUT(MAX)}$, while for the main SMPS, the losses at $V_{IN(MIN)}$ should be roughly equal to losses at $V_{IN(MAX)}$.

Low-Side MOSFET Power Dissipation

For the low-side MOSFET (N_L), the worst-case power dissipation always occurs at maximum input voltage:

$$PD_{COND}(LS) = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT}^2 \times RDS(ON)$$

The following additional loss occurs in the low-side MOSFET due to the body diode conduction losses:

$$PD_{BDY}(LS) = 0.05 I_{PEAK} \times 0.4V$$

The total power low-side MOSFET dissipation is:

$$PD_{TOTAL}(LS) \approx PD_{COND}(LS) + PD_{BDY}(LS)$$

MOSFET Gate Drivers (DH, DL)

The DH high-side MOSFET drivers are powered by internal boost switch charge pumps at BST, while the DL synchronous-rectifier drivers are powered directly by the 5V bias supply (V_{DD}). Adaptive dead-time circuits monitor the DL and DH drivers and prevent either FET from turning on until the other is fully off. The adaptive driver dead time allows operation without shoot-through with a wide range of MOSFETs, minimizing delays and maintaining efficiency.

A low-resistance, low-inductance path from the DL and DH drivers to the MOSFET gates is used for the adaptive dead-time circuits to work properly; otherwise, the sense circuitry in the MAX17085B interprets the MOSFET gates as “off” while charge actually remains. Use very short, wide traces (50 mils to 100 mils wide if the MOSFET is 1in from the driver).

Applications with high-input voltages, long inductive driver trace, and fast rising LX edges may have shoot-through currents when the low-side MOSFET gate is pulled up by the MOSFET’s gate-to-drain capacitance (C_{RSS}), gate-to-source capacitance (C_{ISS} - C_{RSS}). The following minimum threshold should not be exceeded:

$$V_{GS(TH)} > V_{IN}\left(\frac{C_{RSS}}{C_{ISS}}\right)$$

Typically, adding a 4700pF between DL and power ground (C_{NL} in Figure 7), close to the low-side MOSFETs, greatly reduces coupling. Do not exceed 22nF of total gate capacitance to prevent excessive turn-off delays.

Alternatively, shoot-through currents may be caused by a combination of fast high-side MOSFETs and slow low-side MOSFETs. If the turn-off delay time of the low-side MOSFET is too long, the high-side MOSFETs can turn on before the low-side MOSFETs have actually turned off. Adding a resistor less than 5Ω in series with B_{ST} slows down the high-side MOSFET turn-on time, eliminating the shoot-through currents without degrading the turn-off time (R_{BST} in Figure 7). Slowing down the high-side MOSFET also reduces the LX node rise time, thereby reducing EMI and high-frequency coupling responsible for switching noise.

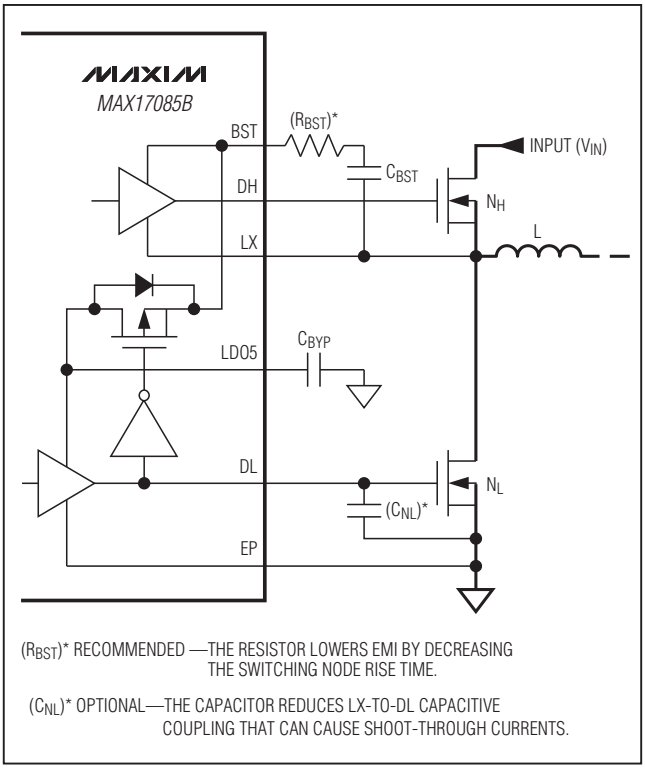

Figure 7. Gate-Drive Circuit

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Boost Capacitors

The boost capacitors (C_{BST}) selected must be large enough to handle the gate charging requirements of the high-side MOSFETs. Select the boost capacitors to avoid discharging the capacitor more than 200mV while charging the high-side MOSFETs' gates:

$$C_{BST} = \frac{N \times Q_{GATE}}{200mV}$$

where N is the number of high-side MOSFETs used for one regulator, and Q_{GATE} is the gate charge specified in the MOSFET's data sheet. For example, assume (1) FDS6298 n-channel MOSFETs are used on the high side. According to the manufacturer's data sheet, a single FDS6298 has a maximum gate charge of 19nC (V_{GS} = 5V). Using the above equation, the required boost capacitance would be:

$$C_{BST} = \frac{1 \times 10nC}{200mV} = 0.05\mu F$$

Selecting the closest standard value, this example requires a 0.1µF ceramic capacitor.

Applications Information

Setting Charger Input Current Limit

The input current limit should be set based on the current capability of the AC adapter and the tolerance of the input current limit. The upper limit of the input current threshold should never exceed the adapter's minimum available output current. For example, if the adapter's output current rating is 5A ≤ 10%, the input current limit should be selected so that its upper limit is less than 5A x 0.9 = 4.5A. Since the input current-limit accuracy of the MAX17085B is ≤ 2%, the typical value of the input current limit should be set at 4.5A divided by 1.02 ≈ 4.41A. The lower limit for input current must also be considered. For chargers at the low end of the specification, the input current limit for this example could be 4.41A x 0.95 or approximately 4.19A.

AC Adapter Detection

The minimum adapter voltage threshold is used to calculate the resistor values at ACIN:

$$V_{ADP(MIN)} \frac{R_{ACIN2}}{R_{ACIN1} + R_{ACIN2}} = V_{ACIN-ACOK}$$

where $V_{ACIN-ACOK}$ is 1.5V (typ).

To minimize power loss, choose a large value for R_{ACIN1}, and calculate R_{ACIN2}.

For example:

$$V_{ADP(MIN)} = 17V$$

$$R_{ACIN1} = 249k\Omega$$

then:

$$R_{ACIN2} = \frac{R_{ACIN1}}{\left(V_{ADP(MIN)}/V_{ACIN-ACOK} - 1\right)} = 24.1k\Omega$$

The nearest standard resistor value for R_{ACIN2} is 24.3kΩ. The ACOV threshold is then determined by:

$$V_{ADP(OV)} = V_{ACIN-ACOV}\left(1 + \frac{R_{ACIN1}}{R_{ACIN2}}\right)$$

where $V_{ACIN-ACOV}$ is 2.1V (typ).

Using the values in the example above, $V_{ADP(OV)}$ is 23.7V.

Relearn Application

The relearn function is easily implemented in the MAX17085B by configuring the system to override the PDSL gate drive to the adapter and battery selector MOSFETs as shown in Figure 1. The system initiates the relearn cycle by disabling the adapter selector MOSFET and enabling the battery selector MOSFET. The MAX17085B relies on the system to monitor the battery discharge voltage. When the battery reaches its critical discharge voltage threshold, the system reenables the adapter selector MOSFET.

Important: Keep ISET low during the relearn cycle. When the relearn cycle is completed, release PDSL first, wait 10ms, then enable charging.

Main SMPS Dropout Performance

The output voltage for continuous-conduction operation is restricted by the nonadjustable minimum off-time one-shot. For best dropout performance, use the slower (200kHz) on-time setting. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on- and off-times. Also, keep in mind that transient response performance of buck regulators operated too close to dropout is poor, and bulk output capacitance must often be added (see the *Design Procedure* section).

The absolute point of dropout is when the inductor current ramps down during the minimum off-time (ΔI_{DOWN}) as much as it ramps up during the on-time (ΔI_{UP}). The ratio $h = \Delta I_{UP}/\Delta I_{DOWN}$ indicates the controller's ability to slew the inductor current higher in response to increased load, and must always be greater than 1. As h approaches 1, the absolute minimum dropout point, the inductor current cannot increase as much during each switching cycle, and V_{SAG} greatly increases unless additional output capacitance is used.

A reasonable minimum value for h is 1.5 for most normal regulators. With the extended on-time feature, the minimum h value of 1 can be used. Adjusting this up or down allows trade-offs between VSAG, output capacitance, and minimum operating voltage. For a given value of h, the minimum operating voltage can be calculated as:

$$V_{IN(MIN)} = \frac{V_{OUT} + V_{CHG}}{1 - \left(\frac{h \times t_{OFF(MIN)}}{T_{SW}}\right)}$$

where VCHG is the parasitic voltage drop in the charge path (see the *On-Time One-Shot* section) and $t_{OFF(MIN)}$ is from the *Electrical Characteristics*.

If the calculated $V_{IN(MIN)}$ is greater than the required minimum input voltage, then operating frequency must be reduced or output capacitance added to obtain an acceptable V_{SAG}. If operation near dropout is anticipated, calculate V_{SAG} to be sure of adequate transient response.

Dropout Design Example:

V_{OUT} = 5V, f_{SW} = 600kHz, t_{SW} = 1.67µs, $t_{OFF(MIN)}$ = 250ns, V_{CHG} = 100mV, h = 1:

$$V_{IN(MIN)} = \frac{5V + 0.1V}{1 - \left(\frac{1 \times 250ns}{1.67\mu s}\right)} = 6V$$

Therefore, V_{IN} must be greater than 6V for steady-state operation. Input transient sags down to 5.5V during an output load transient are acceptable due to the extended on-time feature.

Charge Pump

The MAX17085B provides a simple way to generate and valley regulate an auxiliary charge pump to provide a low-power, high-voltage (12V to 15V) supply for load switch gate drive bias. Figure 8 shows the charge-pump application circuit. The charge pump is driven by the DL pin to boost the output to the desired bias voltage ($V_{CHG-PUMP}$):

$$V_{CHG-PUMP} \approx 3 \times (5V - V_F)$$

where V_F is the forward voltage drop of the diodes.

Connect a resistor-divider from the high-voltage output to the SKIP pin as shown in Figure 8. When the voltage at the SKIP pin drops to 2.1V, which is the typical falling-edge threshold between SKIP mode and forced-PWM mode, the MAX17085B enters forced-PWM operation, recharging the bias output. This automatic refresh operation allows the MAX17085B to remain in skip mode for best efficiency, yet keep the charge pump output above a minimum threshold. The minimum charge-pump voltage is:

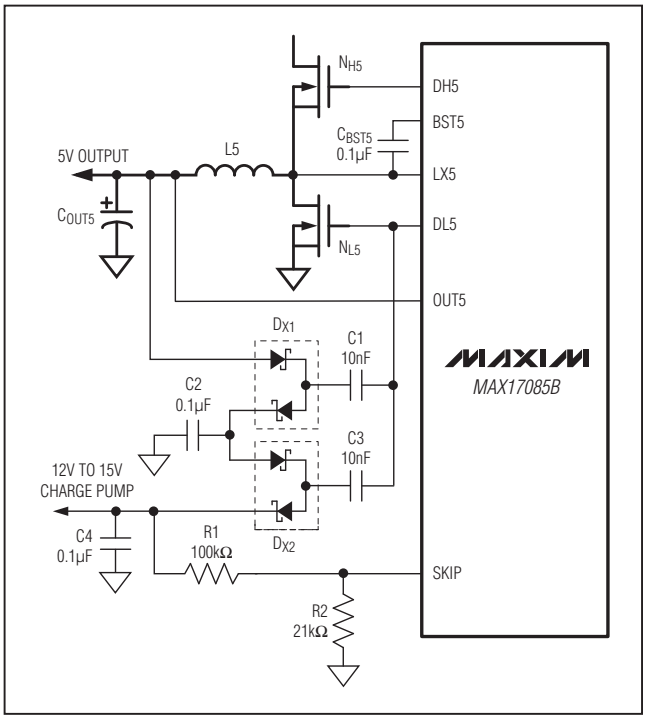

Figure 8. Charge-Pump Application

$$V_{CHG-PUMP(MIN)} = 2.1V \times \left(1 + \frac{R1}{R2}\right)$$

PCB Layout Guidelines

Careful PCB layout is critical to achieving low switching losses and clean, stable operation. The switching power stage requires particular attention. If possible, mount all the power components on the top side of the board, with their ground terminals flush against one another. Follow these guidelines for good PCB layout:

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
- Keep the power traces and load connections short and wide. This practice is essential for high efficiency. Using thick copper PCBs (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PCB traces is a difficult task that must be approached in terms of fractions of centimeters, where a single milliohm of excess trace resistance causes a measurable efficiency penalty.

Integrated Charger, Dual Main Step-Down Controllers, and Dual LDO Regulators

- Minimize the main SMPS current-sensing errors by connecting LX3 and LX5 directly to the drain of the low-side MOSFET. Minimize the charger current-sense resistor trace lengths, and ensure accurate current sensing with Kelvin connections.
- When trade-offs in trace lengths must be made, it is preferable to allow the inductor charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
- Route high-speed switching nodes (BST_, LX_, DH_, and DL_) away from sensitive analog areas (REF, VCC, and OUT).
- Refer to the MAX17085B evaluation kit for the layout example.

Layout Procedure

1) Place the power components first, with ground terminals adjacent (NL_ source, CIN, and COUT). If possible, make all these connections on the top layer with wide, copper-filled areas.
2) Mount the controller IC adjacent to the low-side MOSFET, preferably on the backside opposite NL_ and NH_ to keep LX_, GND, DH_, and the DL_ gate-drive lines short and wide. The DL_ and DH_ gate traces must be short and wide (50 mils to 100 mils wide if the MOSFET is 1in from the controller IC) to keep the driver impedance low and for proper adaptive dead-time sensing.
3) Group the gate-drive components (BST_ capacitor, LDO5 bypass capacitor) together near the controller IC.
4) Make the DC-DC controller ground connections as shown in Figure 1. This diagram can be viewed as having two separate ground planes: power ground, where all the high-power components go, and an analog ground plane for sensitive analog components. The analog ground plane and power ground plane must meet only at a single point directly at the IC.
5) Connect the output power planes directly to the output filter capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the load as is practical.
6) Use a single-point star ground placed directly below the part at the PGND pin. Connect the power ground (ground plane) and the quiet ground island at this location.

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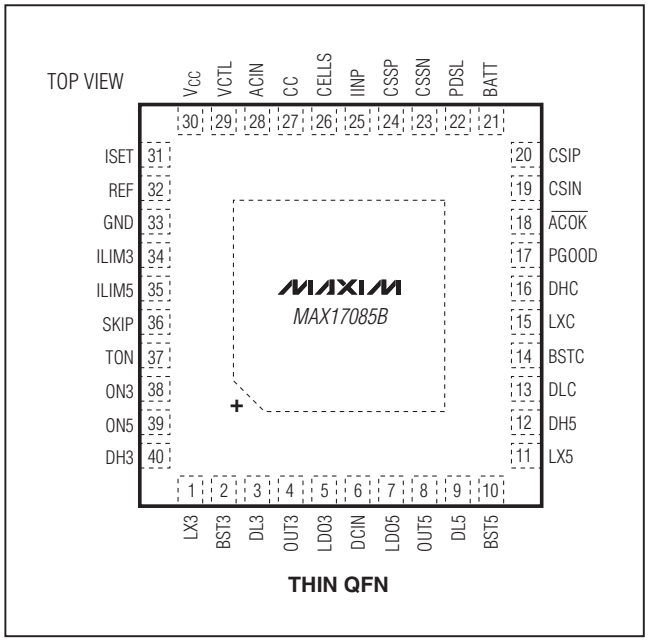
Pin Configuration



THIN QFN

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.	LAND PATTERN NO.
40 TQFN-EP	T4055+2	21-0140	90-0002

Integrated Charger, Dual Main Step-Down Controllers, and Dual LDO Regulators

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/10	Initial release	—
1	10/10	Revised the $\overline{\text{ACOK}}$ threshold to 1.5V from 1.7V in the ACIN pin description	17
2	3/12	Updated *Component Selection For Standard Applications* table	18

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