19-4936; Rev 0; 9/09

EVALUATION KIT AVAILABLE

Dual High-Voltage Scan Drivers for TFT LCD

General Description

The MAX17121 includes two high-voltage level-shifting scan drivers for TFT panel integrated gate logic. Each scan driver has two channels that switch complementarily. The scan-driver outputs swing from +40V to -30V and can swiftly drive capacitive loads. In order to save power, the scan driver's complementary outputs share the charge of their capacitive load before they change states.

The MAX17121 is available in a 24-pin, 4mm x 4mm, thin QFN package with a maximum thickness of 0.8mm for ultra-thin LCD panels.

Applications

Notebook Computer Displays

LCD Monitor and Small TV Panels

Features

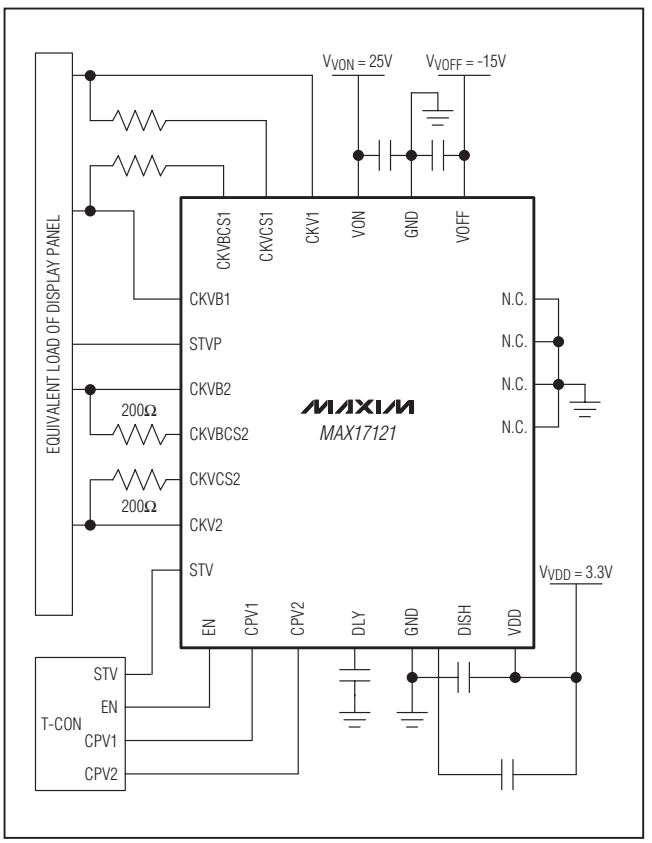
- **+40V to -30V Output Swing Range**
- **Fast Slew Rate for High Capacitive Load**
- **Load Charge Sharing for Power Saving**
- **24-Pin, 4mm x 4mm, Thin QFN Package**

Ordering Information

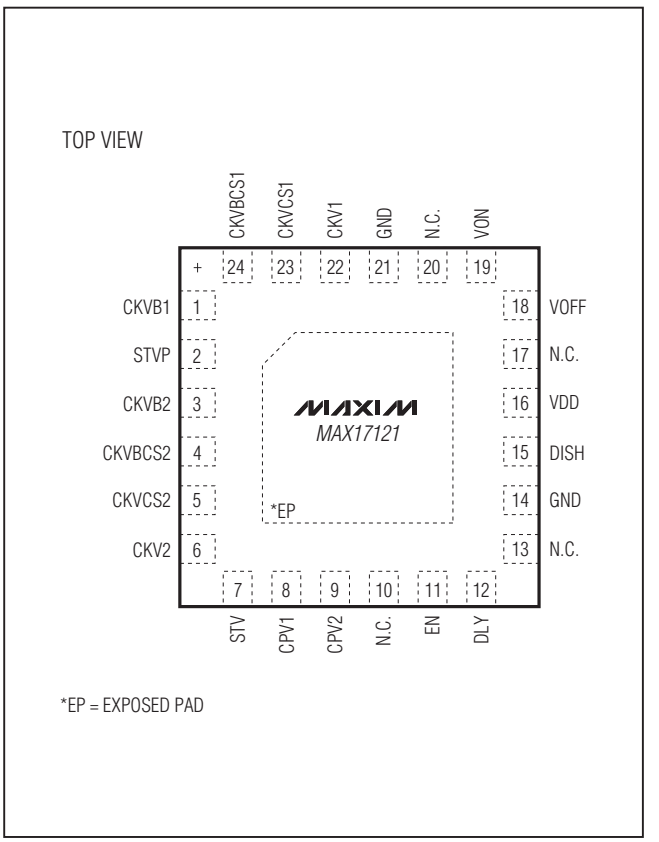
PART	TEMP RANGE	PIN-PACKAGE
MAX17121ETG+	-40°C to +85°C	24 TQFN-EP*

**EP = Exposed pad.*

Simplified Operating Circuit



Pin Configuration



Dual High-Voltage Scan Drivers for TFT LCD

ABSOLUTE MAXIMUM RATINGS

VDD to GND .....-0.3V to +4V
CPV1, CPV2, STV, EN to GND .....-0.3V to +4V
DLY to GND.....-0.3V to (V_{VDD} + 0.3V)
DISH to GND .....-6V to (V_{VDD} + 0.3V)
VON to GND.....-0.3V to +45V
VOFF to GND .....-35V to + 0.3V
VON to VOFF..... +65V
CKV1, CKV2, CKVB1, CKVB2,
to VOFF ..... -0.3V to (V_{VON} + 0.3V)
STVP to VOFF..... -0.3V to (V_{VON} + 0.3V)
CKVCS1, CKVCS2 to VOFF ..... -0.3V to (V_{VON} + 0.3V)
CKVBCS1, CKVBCS2 to VOFF ..... -0.3V to (V_{VON} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
24-Pin, 4mm x 4mm Thin QFN
(derate 27.8mW/°C above +70°C).....2222.2mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VVDD = VEN = +3.3V, VVON = 25V, VVOFF = -15V, STV = CPV1 = CPV2 = GND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VDD Input Voltage Range		2.2		3.6	V
VDD UV Lockout	Rising, hysteresis = 150mV		2	2.15	V
VDD Quiescent Current	V_{EN} = 3.3V		250	400	µA
	EN = GND		250	400	
Thermal Shutdown	Rising edge, hysteresis = 15°C		+160		°C
VON Input Voltage Range		15		40	V
VON Supply Current	V_{EN} = 3.3V		300	600	µA
	EN = GND		300	600	
VOFF Input Voltage Range		-30		-3	V
VOFF Supply Current	V_{EN} = 3.3V		200	300	µA
	EN = GND		200	300	
VON-to-VOFF Voltage Range				65	V
VON UV Lockout	VON rising		12	13	V
	VON falling	10	11		
CKV_, CKVB_ Output Low	I(CKV_) = -20mA		5	10	Ω
CKV_, CKVB_ Output High	I(CKV_) = 20mA		9	18	Ω
CPV_ Rising to CKV_ Rising	t_R, Figure 4, V_{STV} = 0V		100	150	ns
CPV_ Rising to CKV_ Falling	t_F, Figure 4, V_{STV} = 0V		100	150	ns
CPV_ Rising to CKVB_ Rising	t_R, Figure 4, V_{STV} = 0V		100	150	ns
CPV_ Rising to CKVB_ Falling	t_F, Figure 4, V_{STV} = 0V		100	150	ns
CPV_ Falling to CKVCS_ Rising	t_{CSR}, Figure 4, V_{STV} = 0V		100	150	ns
CPV_ Falling to CKVCS_ Falling	t_{CSF}, Figure 4, V_{STV} = 0V		100	150	ns
CPV_ Falling to CKVCBS_ Rising	t_{CSR}, Figure 4, V_{STV} = 0V		100	150	ns
CPV_ Falling to CKVBCS_ Falling	t_{CSF}, Figure 4, V_{STV} = 0V		100	150	ns

ELECTRICAL CHARACTERISTICS (continued)

(VVDD = VEN = +3.3V, VVON = 25V, VVOFF = -15V, STV = CPV1 = CPV2 = GND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CKV_, CKVB_ Slew Rate Rising	STV = GND, C_{LOAD} = 15nF, R_{LOAD} = 100Ω, 15% to 85% (Note 1)	100	1400		V/µs
	STV = GND, C_{LOAD} = 4.7nF, 20% to 80%	100	160		
CKV_, CKVB_ Slew Rate Falling	STV = GND, C_{LOAD} = 15nF, R_{LOAD} = 100Ω, 85% to 15% (Note 1)	100	2000		V/µs
	STV = GND, C_{LOAD} = 4.7nF, 80% to 20%	100	160		
CKV_, CKVB_ Slew Rate Rising	STV = VDD, C_{LOAD} = 15nF, R_{LOAD} = 100Ω, 15% to 85% (Note 1)	100	1400		V/µs
	STV = VDD, C_{LOAD} = 4.7nF, 20% to 80%	100	160		
CKV_, CKVB_ Slew Rate Falling	STV = VDD, C_{LOAD} = 15nF, R_{LOAD} = 100Ω, 85% to 15% (Note 1)	100	2400		V/µs
	STV = VDD, C_{LOAD} = 4.7nF, 80% to 20%	100	160		
Three-State Output Current	CKV = midsupply (Note 2)	-1		+1	µA
CKVCS_-to-CKVBCS_ Resistance	I(CKVCS_ to CKVBCS_) = 10mA		40	100	Ω
STVP Output Low	I(STVP) = -20mA		5	10	Ω
STVP Output High	I(STVP) = 20mA		18	35	Ω
STV Rising to STVP Rising			100	200	ns
STV Falling to STVP Falling			100	200	ns
STVP Slew Rate Rising	C1 = 4.7nF, R1 = 200Ω (Note 1)	50	1000		V/µs
	C1 = 4.7nF	50	100		
STVP Slew Rate Falling	C1 = 4.7nF, R1 = 200Ω (Note 1)	50	2000		V/µs
	C1 = 4.7nF	50	100		
CPV_ Input Frequency				85	kHz
Input Low Voltage	CPV_, STV, EN, 2.2V ≤ V_{VDD} ≤ 3.6V			0.8	V
Input High Voltage	CPV_, STV, EN, 2.2V ≤ V_{VDD} ≤ 3.6V	2.1			V
Input Hysteresis	CPV_, STV, EN		250		mV
Input-Bias Current	$V_{STV\_}$ = 0V or V_{VDD}; $V_{CPV\_}$ = 0V or V_{VDD} (Note 2)	-1		+1	µA
DISH Low Voltage			-0.66	-1.5	V
DISH High Voltage		-0.5	-0.65		V
DISH Hysteresis			10		mV
DISH Input Impedance	V_{DISH} = -2V		300	600	kΩ
DISH Switch Resistance	V_{DISH} = -2V		200	500	Ω
	V_{DISH} = 0V		1		MΩ
DLY Output Current	DLY = GND	3	4	5	µA
DLY Sink Current	EN = GND, V_{DLY} = 0.4V	5	8		mA
DLY Enable Threshold	Rising, hysteresis = 100mV	1.60	1.65	1.70	V
Startup Delay	C(DLY) = 0.1µF		40		ms

Dual High-Voltage Scan Drivers for TFT LCD

ELECTRICAL CHARACTERISTICS

(V_{VDD} = V_{EN} = +3.3V, V_{VON} = 25V, V_{VOFF} = -15V, STV = CPV1 = CPV2 = GND, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VDD Input Voltage Range		2.2		3.6	V
VDD UV Lockout	Rising, hysteresis = 150mV			2.15	V
VDD Quiescent Current	V_{EN} = 3.3V			400	µA
	EN = GND			400	
Thermal Shutdown	Rising edge, hysteresis = 15°C				°C
VON Input Voltage Range		15		40	V
VON Supply Current	V_{EN} = 3.3V			600	µA
	EN = GND			600	
VOFF Input Voltage Range		-30		-3	V
VOFF Supply Current	V_{EN} = 3.3V			300	µA
	EN = GND			300	
VON-to-VOFF Voltage Range				65	V
VON UV Lockout	VON rising			13	V
	VON falling	10			
CKV_, CKVB_ Output Low	I(CKV_) = -20mA			10	Ω
CKV_, CKVB_ Output High	I(CKV_) = 20mA			18	Ω
CPV_ Rising to CKV_ Rising	t_R, Figure 4, V_{STV} = 0V			150	ns
CPV_ Rising to CKV_ Falling	t_F, Figure 4, V_{STV} = 0V			150	ns
CPV_ Rising to CKVB_ Rising	t_R, Figure 4, V_{STV} = 0V			150	ns
CPV_ Rising to CKVB_ Falling	t_F, Figure 4, V_{STV} = 0V			150	ns
CPV_ Falling to CKVCS_ Rising	t_{CSR}, Figure 4, V_{STV} = 0V			150	ns
CPV_ Falling to CKVCS_ Falling	t_{CSF}, Figure 4, V_{STV} = 0V			150	ns
CPV_ Falling to CKVCBS_ Rising	t_{CSR}, Figure 4, V_{STV} = 0V			150	ns
CPV_ Falling to CKVBCS_ Falling	t_{CSF}, Figure 4, V_{STV} = 0V			150	ns
CKV_, CKVB_ Slew Rate Rising	STV = GND, C_{LOAD} = 15nF, R_{LOAD} = 100Ω, 15% to 85% (Note 2)	100			V/µs
	STV = GND, C_{LOAD} = 4.7nF, 20% to 80%	100			
CKV_, CKVB_ Slew Rate Falling	STV = GND, C_{LOAD} = 15nF, R_{LOAD} = 100Ω, 85% to 15% (Note 2)	100			V/µs
	STV = GND, C_{LOAD} = 4.7nF, 80% to 20%	100			
CKV_, CKVB_ Slew Rate Rising	STV = VDD, C_{LOAD} = 15nF, R_{LOAD} = 100Ω, 15% to 85% (Note 2)	100			V/µs
	STV = VDD, C_{LOAD} = 4.7nF, 20% to 80%	100			
CKV_, CKVB_ Slew Rate Falling	STV = VDD, C_{LOAD} = 15nF, R_{LOAD} = 100Ω, 85% to 15% (Note 2)	100			V/µs
	STV = VDD, C_{LOAD} = 4.7nF, 80% to 20%	100			

ELECTRICAL CHARACTERISTICS (continued)

(V_{VDD} = V_{EN} = +3.3V, V_{VON} = 25V, V_{VOFF} = -15V, STV = CPV1 = CPV2 = GND, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CKVCS_-to-CMVBCS Resistance	I(CKVCS_-to-CKVBCS) = 10mA			100	Ω
STVP Output Low	I(STVP) = -20mA			10	Ω
STVP Output High	I(STVP) = 20mA			35	Ω
STV Rising to STVP Rising				200	ns
STV Falling to STVP Falling				200	ns
STVP Slew Rate Rising	C_L = 4.7nF	50			V/µs
STVP Slew Rate Falling	C_L = 4.7nF	50			V/µs
CPV_ Input Frequency				85	kHz
Input Low Voltage	CPV_, STV, EN, 2.2V ≤ V_{VDD} ≤ 3.6V			0.8	V
Input High Voltage	CPV_, STV, EN, 2.2V ≤ V_{VDD} ≤ 3.6V	2.1			V
Input Hysteresis	CPV_, STV, EN				mV
DISH Low Voltage				-1.5	V
DISH High Voltage		-0.5			V
DISH Hysteresis					mV
DISH Input Impedance	V_{DISH} = -2V			600	kΩ
DISH Switch Resistance	V_{DISH} = -2V			500	Ω
DLY Output Current	DLY = GND	3		5	µA
DLY Sink Current	EN = GND, V_{DLY} = 0.4V	5			mA
DLY Enable Threshold	Rising	1.60		1.70	V

Note 1: Guaranteed by design. Not production tested.

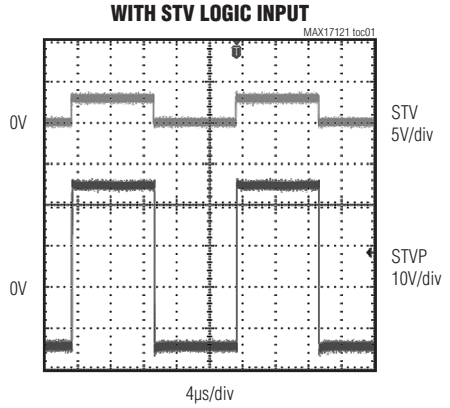
Note 2: Limits are 100% production tested at T_A = +25°C. Maximum and minimum limits over temperature are guaranteed by design and characterization.

Dual High-Voltage Scan Drivers for TFT LCD

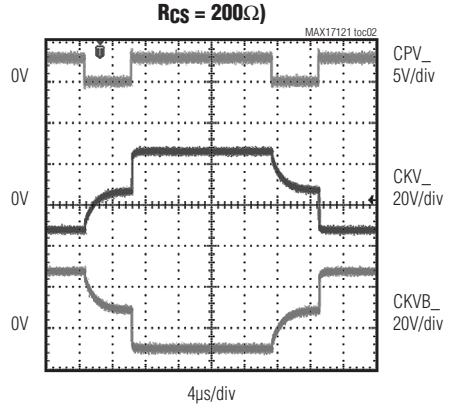
Typical Operating Characteristics

(Circuit of Figure 1, V_{VDD} = V_{EN} = 3.3V, V_{VON} = 25V, V_{VOFF} = -15V, T_A = +25°C, unless otherwise noted.)

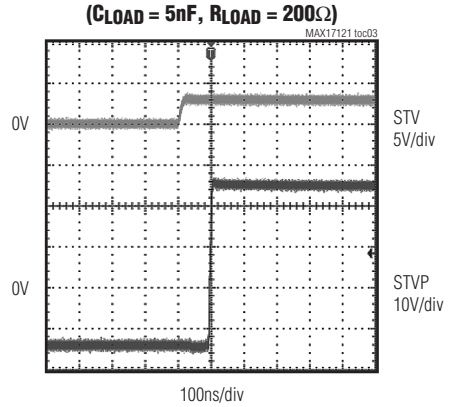
STVP OUTPUT WAVEFORM WITH STV LOGIC INPUT



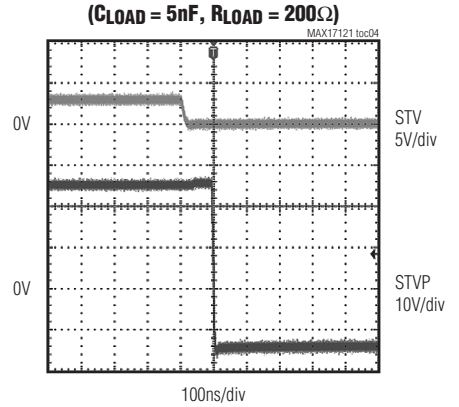
CKV_ AND CKVB_ OUTPUT WAVEFORMS WITH CPV LOGIC INPUT (STV = 0V, C_{LOAD} = 5nF, R_{LOAD} = 50Ω, R_{CS} = 200Ω)



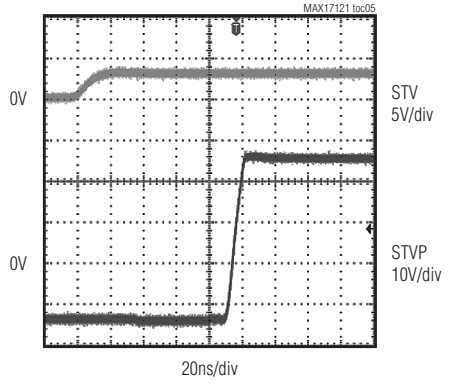
STV-TO-STVP RISING EDGE PROPAGATION DELAY (C_{LOAD} = 5nF, R_{LOAD} = 200Ω)



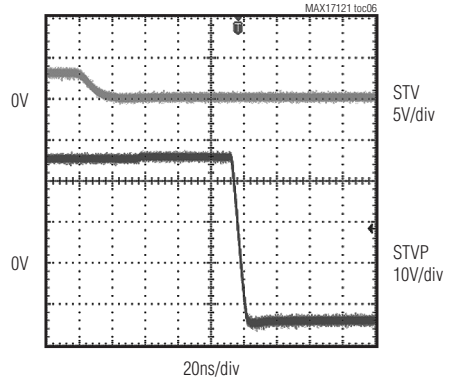
STV-TO-STVP FALLING EDGE PROPAGATION DELAY (C_{LOAD} = 5nF, R_{LOAD} = 200Ω)



STVP SLEW RATE ON RISING EDGE (C_{LOAD} = 5nF, R_{LOAD} = 200Ω)



STVP SLEW RATE ON FALLING EDGE (C_{LOAD} = 5nF, R_{LOAD} = 200Ω)

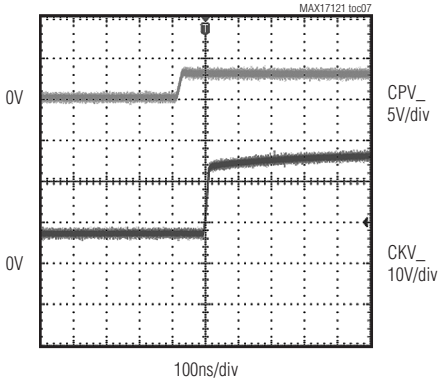


V_{IN} = 3.3V, G_{ON} = 25V, G_{OFF} = 15V

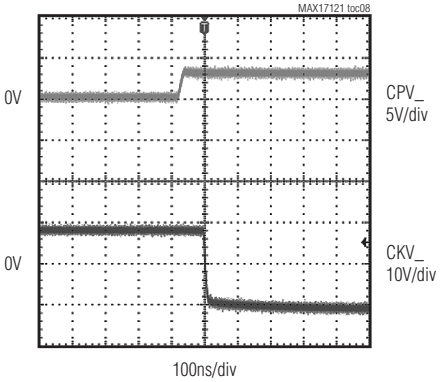
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{VDD} = V_{EN} = 3.3V, V_{VON} = 25V, V_{VOFF} = -15V, T_A = +25°C, unless otherwise noted.)

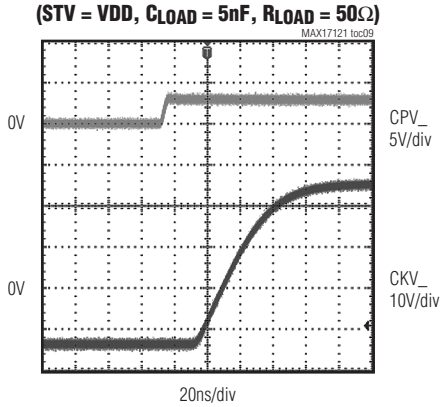
CPV_ TO CKV_ RISING EDGE PROPAGATION DELAY (STV = 0V, C_{LOAD} = 5nF, R_{LOAD} = 50Ω)



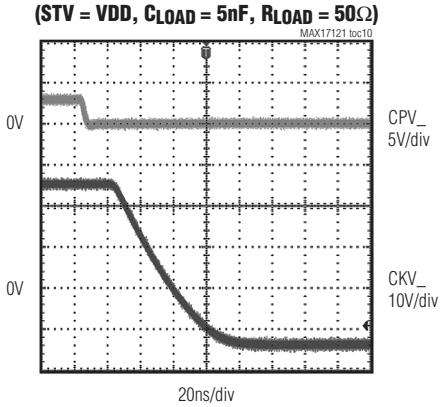
CPV_ TO CKV_ FALLING EDGE PROPAGATION DELAY (STV = 0V, C_{LOAD} = 5nF, R_{LOAD} = 50Ω)



CKV_ SLEW RATE ON RISING EDGE (STV = VDD, C_{LOAD} = 5nF, R_{LOAD} = 50Ω)

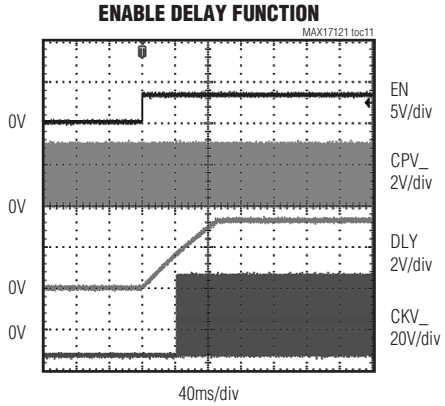


CKV_ SLEW RATE ON FALLING EDGE (STV = VDD, C_{LOAD} = 5nF, R_{LOAD} = 50Ω)



V_{IN} = 3.3V, G_{ON} = 25V, G_{OFF} = -15V

ENABLE DELAY FUNCTION



Pin Description

PIN	NAME	FUNCTION
1	CKVB1	High-Voltage Scan-Drive Output. CKVB1 is the inverse of CKV1 during active states and is high impedance whenever CKV1 is high impedance.
2	STVP	High-Voltage Scan-Drive Output. STVP is connected to VOFF when STV is low and is connected to VON when STV is high and CPV1 is low. When both STV and CPV1 are high, STVP is high impedance.
3	CKVB2	High-Voltage Scan-Drive Output. CKVB2 is the inverse of CKV2 during active states and is high impedance whenever CKV2 is high impedance.
4	CKVBCS2	CKVB2 Charge-Sharing Connection. CKVBCS2 connects to CKVCS2 whenever CPV2 and STV are both low (to make CKV2 and CKVB2 high impedance) to allow CKV2 to connect to CKVB2, sharing charge between the capacitive loads on these two outputs.
5	CKVCS2	CKV2 Charge-Sharing Connection. CKVCS2 connects to CKVBCS2 whenever CPV2 and STV are both low (to make CKV2 and CKVB2 high impedance) to allow CKVB2 to connect to CKV2, sharing charge between the capacitive loads on these two outputs.
6	CKV2	High-Voltage Scan-Drive Output. When enabled, CKV2 toggles between its high state (connected to VON) and its low state (connected to VOFF) on each falling edge of the CPV2 input. Further, CKV2 is high impedance whenever CPV2 and STV are both low.
7	STV	Vertical Sync Input. The rising edge of STV begins a frame of data. The STV input is used to generate the high-voltage STVP output.
8	CPV1	Vertical Clock-Pulse Input. CPV1 controls the timing of the CKV1 and CKVB1 outputs, which change state (by first sharing charge) on its falling edge.
9	CPV2	Vertical Clock-Pulse Input. CPV2 controls the timing of the CKV2 and CKVB2 outputs, which change state (by first sharing charge) on its falling edge.
10, 13, 17, 20	N.C.	Not Connected
11	EN	Enables the MAX17121. Drive EN high to start up the MAX17121 after a delay time, which is set by a capacitor at DLY.
12	DLY	Startup Delay Setting. Connect a capacitor to adjust the delay based on $t_{DELAY} = C_{DLY} \times 410k\Omega$.
14, 21	GND	Ground
15	DISH	VOFF Discharge Connection. Pulling DISH below ground activates an internal connection between VOFF and GND, rapidly discharging the VOFF supply. Typically, DISH is capacitively connected to VDD, so that when VDD falls, VOFF is discharged.
16	VDD	Supply Input. VDD is the logic supply input for the scan driver. Bypass to GND through a minimum 0.1µF capacitor.
18	VOFF	Gate-Off Supply. VOFF is the negative supply voltage for the CKV_, CKVB_, and STVP high-voltage driver outputs. Bypass to GND with a minimum of 1µF ceramic capacitor.
19	VON	Gate-On Supply. VON is the positive supply voltage for the CKV_, CKVB_, and STVP high-voltage driver outputs. Bypass to GND with a minimum of 1µF ceramic capacitor.

Pin Description (continued)

PIN	NAME	FUNCTION
22	CKV1	High-Voltage Scan-Drive Output. When enabled, CKV1 toggles between its high state (connected to VON) and its low state (connected to VOFF) on each falling edge of the CPV1 input. Further, CKV1 is high impedance whenever CPV1 and STV are both low.
23	CKVCS1	CKV1 Charge-Sharing Connection. CKVCS1 connects to CKVBCS1 whenever CPV1 and STV are both low (to make CKV1 and CKVB1 high impedance) to allow CKVB1 to connect to CKV1, sharing charge between the capacitive loads on these two outputs.
24	CKVBCS1	CKVB1 Charge-Sharing Connection. CKVBCS1 connects to CKVCS1 whenever CPV1 and STV are both low (to make CKV1 and CKVB1 high impedance) to allow CKV1 to connect to CKVB1, sharing charge between the capacitive loads on these two outputs.
—	EP	Exposed Pad. EP is not connected in the IC. The EP should be connected to the ground plane on the PCB to improve thermal performance.

Dual High-Voltage Scan Drivers for TFT LCD

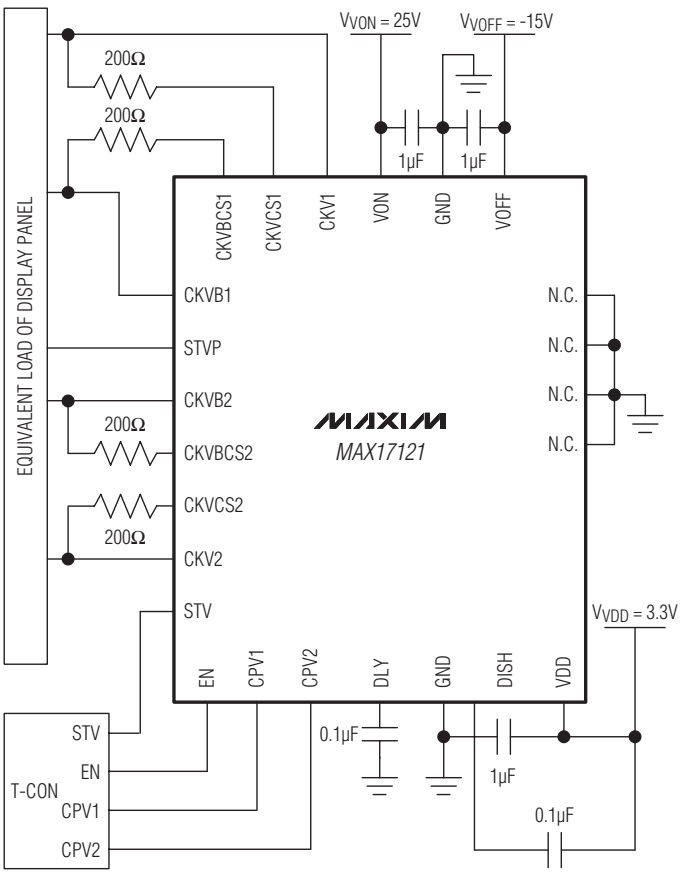


Figure 1. Typical Operating Circuit

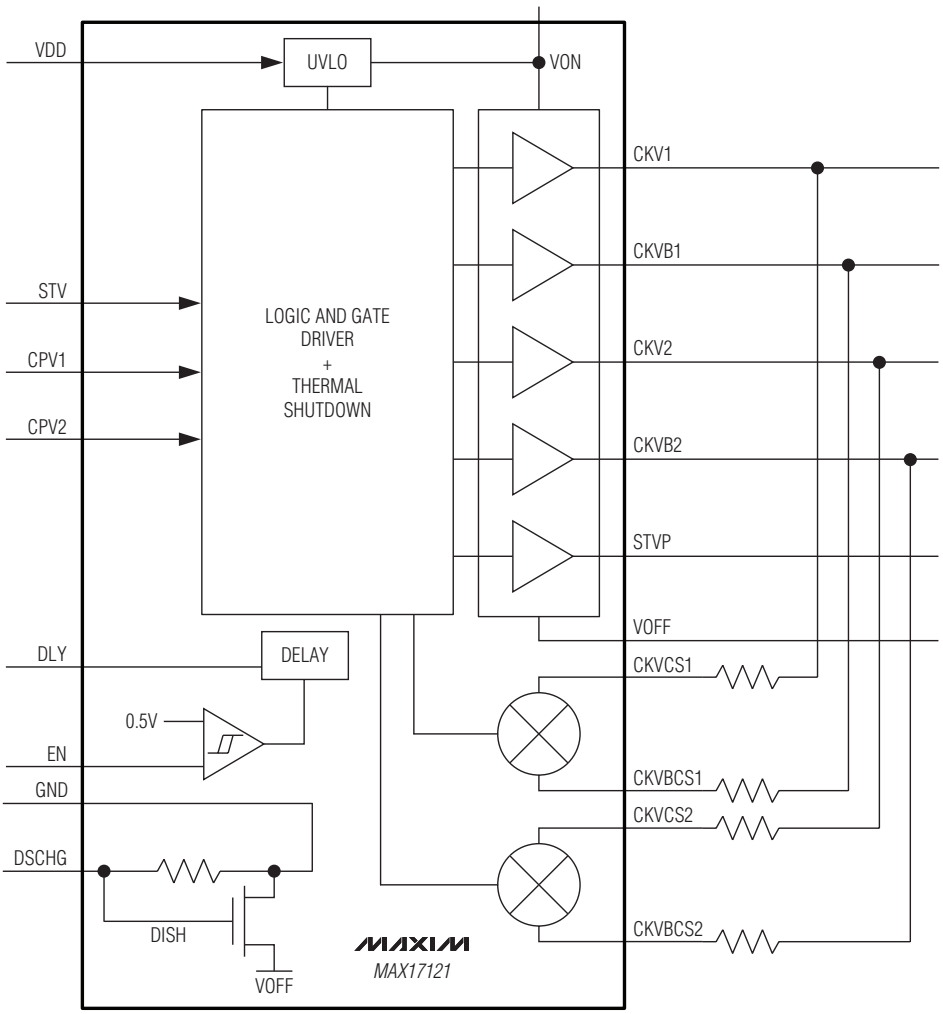


Figure 2. Functional Diagram

Detailed Description

The MAX17121 contains two high-voltage level-shifting scan drivers for active-matrix TFT LCDs. Figure 2 is the functional diagram.

Undervoltage Lockout on VDD

The undervoltage-lockout (VDD-UVLO) circuit on VDD compares the input voltage at VDD with the VDD-UVLO (2V typ) to ensure that the input voltage is high enough for reliable operation. There is 100mV of hysteresis to prevent supply transients from causing a restart. When the VDD voltage is below VDD-UVLO, the scan-driver outputs are high impedance.

Undervoltage Lockout on VON

The undervoltage-lockout (VON-UVLO) circuit on VON compares the input voltage at VON with the VON-UVLO (12V typ) to ensure that the input voltage is high enough for reliable operation. There is 1V of hysteresis to prevent supply transients from causing a restart. When the VON voltage is below VON-UVLO, the scan-driver outputs are high impedance.

Dual High-Voltage Scan Drivers for TFT LCD

High-Voltage Level-Shifting Scan Driver

The MAX17121 includes 2 two-channel high-voltage level-shifting scan drivers. The scan-driver outputs (CKV1, CKV2, CKVB1, CKVB2, and STVP) swing between the power-supply rails (VON and VOFF) according to their corresponding input logic levels. The states of the CKV1, CKVB1, and STVP outputs are determined by the input logic levels present on STV and CPV1. The states of the CKV2 and CKVB2 outputs are determined by the input logic levels present on STV and CPV2 (see Figure 3, Table 1, and Table 2).

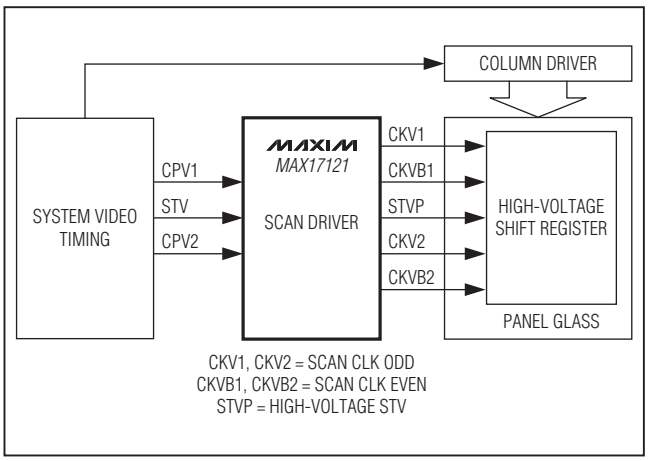


Figure 3. Scan-Driver System Diagram

STV comprises the vertical timing signals. CPV1 and CPV2 are the TFT gate-logic timing signals. These signals have CMOS input logic levels set by the VDD supply voltage. CKV1 and CKV2 are scan clock outputs, which are complementary to scan clock outputs CKVB1 and CKVB2, respectively. These output signals swing from VON to VOFF, which have a maximum upper level of +40V, a minimum lower level of -30V, and a combined maximum range of V_{ON} - V_{OFF} = 65V. Their low-output impedance enables them to swiftly drive capacitive loads. Input pins CKVCS1, CKVBSC1, CKVSC2, and CKVBCS2 allow the charge in the panel equivalent capacitors to be shared. This reduces the power loss in state transition.

Table 1. STVP Logic

VON	EN	V_{DLY}	INPUT SIGNALS		OUTPUT (STVP)
			STV	CPV1	
> UVLO	H	H*	L	X	L
			H	L	H
			H	H	High-Z
		L*	X	X	L
	L	X	X	X	L
< UVLO	X	X	X	X	High-Z

H = high, L = low, High-Z = high impedance, X = don't care, H = V_{DLY} > 1/2 x V_{VDD}, L* = V_{DLY} < 1/2 x V_{VDD}.*

Table 2. CKV_, CKVB_ Logic

VON	EN	V_{DLY}	INPUT SIGNALS		OUTPUTS		
			STV	CPV_	CKV_	CKVB_	CHARGE SHARING
> UVLO	H	H*	L	L	High-Z	High-Z	Yes
			L	↑	TOGGLE	TOGGLE	No
			H	L	VOFF	VON	No
			H	H	VON	VOFF	No
		L*	X	X	VOFF	VOFF	No
	Low	X	X	X	VOFF	VOFF	No
< UVLO	X	X	X	X	High-Z		No

H = high, L = low, High-Z = high impedance, ↑ = rising edge, X = don't care, H = V_{DLY} > 1/2 x V_{VDD}, L x = V_{DLY} < 1/2 x V_{VDD}.*

Enable Function

EN is an active-high logic input that enables/disables the MAX17121 output drive. Drive EN high to enable the MAX17121 scan driver. When EN is low, all the drivers' outputs are pulled to VOFF.

Delay Function

The DLY input sets the delay time in startup when the MAX17121 is enabled and the scan-driver outputs are enabled. The delay time is adjustable by choosing a different capacitor at DLY. Calculate the delay capacitance as:

$$C_{DLY} = t_{DELAY}/410k\Omega$$

The delay enable trip point is $V_{VDD}/2$. Before V_{DLY} reaches this threshold, scan-driver outputs stay in the same state as EN is low.

If there is no delay needed in the startup, connect DLY to VDD.

VOFF Rapid-Discharge Function (DISH Input)

The DISH input controls a switch between VOFF and GND. When DISH is pulled below ground by at least 1V, VOFF is rapidly discharged to GND. Typically, DISH is capacitively coupled to VDD so that if VDD falls suddenly, VOFF is quickly discharged to GND.

Thermal-Overload Protection

The thermal-overload protection prevents excessive power dissipation from overheating the device. When the junction temperature exceeds T_J = +160°C, a thermal sensor immediately shuts down the scan-driver outputs. The outputs are set to high impedance. Once the device cools down by approximately 15°C, the device reactivates.

The thermal-overload protection protects the IC in the event of overheat conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of T_J = +150°C.

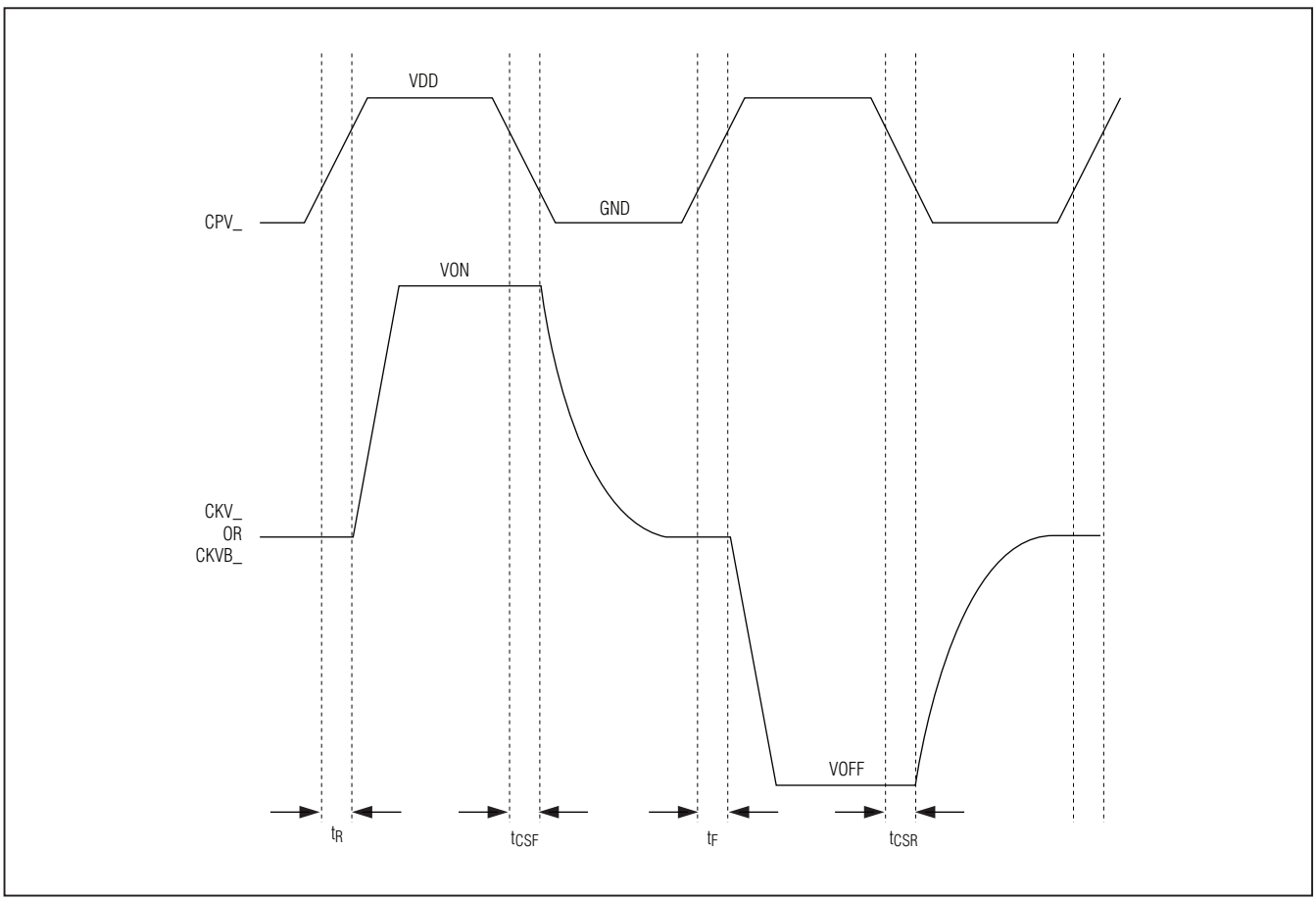


Figure 4. CKV Timing

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Applications Information

Power Dissipation

An IC's maximum power dissipation depends on the thermal resistance from the die to the ambient environment and the ambient temperature. The thermal resistance depends on the IC package, PCB copper area, other thermal mass, and airflow.

The MAX17121, with its exposed backside paddle soldered to 1in^2 of PCB copper, can dissipate approximately 27.8mW into +70°C still air. More PCB copper, cooler ambient air, and more airflow increase the possible dissipation, while less copper or warmer air decreases the IC's dissipation capability.

Scan-Driver Outputs

The power dissipated by the scan-driver outputs (CKV1, CKVB1, STVP, CKV2, and CKVB2) depends on the scan frequency, the capacitive load, and the difference between the VON and VOFF supply voltages. Assuming each output driver's the same capacitance, the power loss is:

$$PD_{SCAN} = 7 \times f_{SCAN} \times C_{PANEL} \times (V_{GON} - V_{GOFF})^2$$

where f_{SCAN} is the scan frequency of the panel, C_{PANEL} is the panel model capacitive load, V_{GON} and V_{GOFF} are the positive gate-on and negative gate-off voltages.

If all the scan drivers operate at a frequency of f_{SCAN} = 50kHz, the load of the six outputs is C_{PANEL} = 5nF, and the supply voltage difference is V_{VON} - V_{VOFF} = 30V, then the power dissipated is 1.125W.

PCB Layout and Grounding

Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

- Place the VON, VOFF, and VDD pin bypass capacitors as close as possible to the device. The ground connections of the VON, VOFF, and VDD bypass capacitors should be connected directly to the GND pin with a wide trace.
- Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.
- Connect the MAX17121's exposed paddle to the GND copper plane, and the copper plane area should be maximized to improve thermal dissipation.
- Minimize the length and maximize the width of the traces between the CKV, CKVB, and STV output nodes and the panel load for best transient responses.

Refer to the MAX17121 Evaluation Kit for an example of proper board layout.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
24 TQFN-EP	T+2444	21-0139

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