



## Complete 10µs CMOS 12-Bit ADC

MAX172

### General Description

The MAX172 is a complete 12-Bit analog-to-digital converter (ADC) that combines high speed, low power consumption, and an on-chip voltage reference. The conversion time is 10µs. The buried zener reference provides low drift and low noise performance.

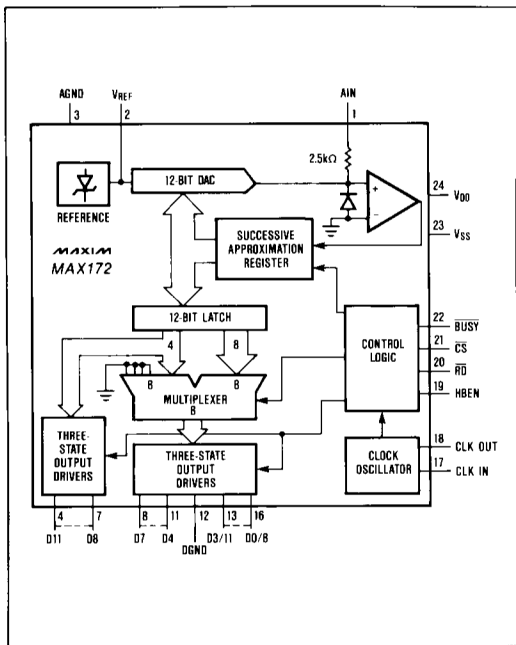
External component requirements are limited to only decoupling capacitors for the power supply and reference voltages. On-chip clock circuitry is also included which can either be driven from an external source, or in stand-alone applications, can be used with a crystal.

The MAX172 uses a standard microprocessor interface architecture. Three-state data outputs are controlled by Read (RD) and Chip Select (CS) inputs. Data access and bus release times of 90 and 75ns respectively ensure compatibility with most popular microprocessors without resorting to wait states.

### Applications

- Digital Signal Processing (DSP)
- High Accuracy Process Control
- High Speed Data Acquisition
- Electro-Mechanical Systems

### Functional Diagram



### Features

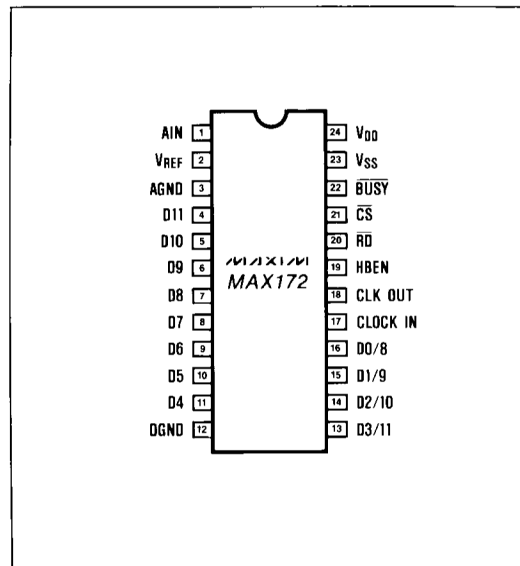
- ◆ 12-Bit Resolution and Linearity
- ◆ 10µs Conversion Time
- ◆ No Missing Codes
- ◆ On-Chip Voltage Reference
- ◆ 90ns Access Time
- ◆ 215mW Max Power Consumption
- ◆ 24-Lead Narrow DIP Package
- ◆ Pin-for-Pin AD7572 Replacement

### Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	ERROR (LSB)	PKG CODE
MAX172ACNG	0°C to +70°C	24 Plastic DIP	±0.5	N24-3
MAX172BCNG	0°C to +70°C	24 Plastic DIP	±1	N24-3
MAX172ACWG	0°C to +70°C	24 Wide SO	±0.5	W24-1
MAX172BCWG	0°C to +70°C	24 Wide SO	±1	W24-1
MAX172CC/D	0°C to +70°C	Dice*	±1	—
MAX172AEAG	-40°C to +85°C	24 Plastic DIP	±0.5	N24-3
MAX172BEAG	-40°C to +85°C	24 Plastic DIP	±1	N24-3
MAX172AMRG	-55°C to +125°C	24 CERDIP	±0.5	R24-4
MAX172BMRG	-55°C to +125°C	24 CERDIP	±1	R24-4

\* Consult factory for dice specifications

### Pin Configuration



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## ABSOLUTE MAXIMUM RATINGS

V <sub>DD</sub> to DGND	-0.3V to +7V
V <sub>SS</sub> to DGND	+0.3V to -17V
AGND to DGND	-0.3V, V <sub>DD</sub> + 0.3V
AIN to AGND	-15V to +15V
Digital Input Voltage to DGND (Pins 17, 19-21)	-0.3V, V <sub>DD</sub> + 0.3V
Digital Output Voltage to DGND (pins 4-11, 13-16, 18, 22)	-0.3V, V <sub>DD</sub> + 0.3V

### Operating Temperature Ranges

MAX172XC	0°C to +70°C
MAX172XE	-40°C to +85°C
MAX172XM	-55°C to +125°C
Storage Temperature Range	-65°C to +160°C
Power Dissipation (any Package) to +75°C	1000mW
Derates Above +75°C by	10mW/°C
Lead Temperature (Soldering 10 seconds)	+300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = +5V  $\pm$  5%, V<sub>SS</sub> = -12V or -15V  $\pm$  5%; Slow Memory Mode; T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub> unless otherwise noted, f<sub>CLK</sub> = 1.25MHz)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
<b>ACCURACY</b>							
Resolution				12			Bits
Integral NonLinearity	INL	MAX172A	T <sub>A</sub> = 25°C			+1/2	LSB
		MAX172AC/AE				+1/2	
		MAX172AM				+3/4	
		MAX172B				$\pm$ 1	
Differential NonLinearity	DNL	Guaranteed Monotonic Over Temp.				+1	LSB
Offset Error (Note 1)		MAX172B	T <sub>A</sub> = 25°C T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>			+4 +6	LSB
		MAX172A	T <sub>A</sub> = 25°C T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>			$\pm$ 3 +4	
Full Scale Error (Note 2)		MAX172B	T <sub>A</sub> = 25°C			+15	LSB
		MAX172A	T <sub>A</sub> = 25°C			+10	
Full Scale Tempco (Notes 3, 4)						+45	ppm/°C
<b>ANALOG INPUT</b>							
Input Voltage Range				0		5	V
Input Current		AIN = 0V to +5V				3.5	mA
<b>INTERNAL REFERENCE</b>							
V <sub>REF</sub> Output Voltage		T <sub>A</sub> = 25°C		-5.2	-5.25	-5.3	V
V <sub>REF</sub> Output Tempco (Note 5)					40		ppm/°C
Output Current Sink Capability		(Note 6)				500	$\mu$ A
<b>LOGIC INPUTS</b>							
Input Low Voltage	V <sub>IL</sub>	CS, RD, HBEN, CLKIN				0.8	V
Input High Voltage	V <sub>IH</sub>	CS, RD, HBEN, CLKIN		2.4			V
Input Capacitance (Note 7)	C <sub>IN</sub>	CS, RD, HBEN, CLKIN				10	pF
Input Current	I <sub>IN</sub>	CS, RD, HBEN CLKIN	VIN = 0 to V <sub>DD</sub>			+10 +20	$\mu$ A
<b>LOGIC OUTPUTS</b>							
Output Low Voltage	V <sub>OL</sub>	D11-D0/8, BUSY, CLKOUT I <sub>SINK</sub> = 1.6mA				0.4	V
Output High Voltage	V <sub>OH</sub>	D11-D0/8, BUSY, CLKOUT I <sub>SOURCE</sub> = 200 $\mu$ A		4			V
Floating State Leakage Current	I <sub>LKG</sub>	D11-D0/8, V <sub>OUT</sub> = 0V to V <sub>DD</sub>				+10	$\mu$ A
Floating State Output Capacitance (Note 7)	C <sub>OUT</sub>					15	pF

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MAX172

## ELECTRICAL CHARACTERISTICS (Continued)

( $V_{DD} = +5V \pm 5\%$ ,  $V_{SS} = -12V$  or  $-15V \pm 5\%$ ; Slow Memory Mode;  $T_A = T_{MIN}$  to  $T_{MAX}$  unless otherwise noted,  $f_{CLK} = 1.25MHz$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>CONVERSION TIME</b>						
MAX172	$t_{CONV}$	Synchronous (12.5 clock cycles) Asynchronous (12 to 13 clock cycles)	9.6		10 10.4	$\mu s$
<b>POWER SUPPLY REJECTION</b>						
$V_{DD}$ Only		FS Change, $V_{SS} = -15V$ , $V_{DD} = 4.75V$ to $5.25V$		$\pm 1/2$		LSB
$V_{SS}$ Only		FS Change, $V_{DD} = 5V$ , $V_{SS} = -5\%$ to $+5\%$		$\pm 1/8$		LSB
<b>POWER REQUIREMENTS</b>						
$V_{DD}$		$\pm 5\%$ for Specified Performance		5		V
$V_{SS}$ (Note 8)		$\pm 5\%$ for Specified Performance		-12 or -15		V
$I_{DD}$		$\overline{CS} = \overline{RD} = V_{DD}$ , AIN = 5V		5	7	mA
$I_{SS}$		$\overline{CS} = \overline{RD} = V_{DD}$ , AIN = 5V		8	12	mA
Power Dissipation		$V_{DD} = +5V$ , $V_{SS} = -15V$		145	215	mW

**Note 1:** Typical change over temp is +1 LSB.

**Note 2:**  $V_{DD} = +5V$ ,  $V_{SS} = -15V$ , FS = +5.000V, Ideal last code transition = FS - 3/2LSB.

**Note 3:** Full Scale TC =  $\Delta FS / \Delta T$ , where  $\Delta FS$  is full scale change from  $T_A = 25^\circ C$  to  $T_{MIN}$  or  $T_{MAX}$ .

**Note 4:** Includes internal reference drift.

**Note 5:**  $V_{REF} TC = \Delta V_{REF} / \Delta T$ , where  $\Delta V_{REF}$  is reference voltage change from  $T_A = 25^\circ C$  to  $T_{MIN}$  or  $T_{MAX}$ .

**Note 6:** Output current should not change during conversion.

**Note 7:** Guaranteed by design, not subject to test.

**Note 8:** Functional operation at  $V_{SS} = -12V \pm 5\%$  is guaranteed by testing offset error and full scale error.

## TIMING CHARACTERISTICS (Note 9)

( $V_{DD} = +5V$ ,  $V_{SS} = -12V$  or  $-15V$ ;  $T_A = T_{MIN}$  to  $T_{MAX}$  unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	$T_A = 25^\circ C$			MAX172C/E		MAX172M		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
CS to $\overline{RD}$ Setup Time	$t_1$		0			0		0		ns
$\overline{RD}$ to BUSY Delay	$t_2$	$C_L = 50pF$		90	190		230		270	ns
Data Access Time (Note 10)	$t_3$	$C_L = 20pF$ $C_L = 100pF$		60	90		110		120	ns
$\overline{RD}$ Pulse Width	$t_4$		$t_3$			$t_3$		$t_3$		
CS to $\overline{RD}$ Hold Time	$t_5$		0			0		0		ns
Data Setup Time After BUSY (Note 10)	$t_6$				70		90		100	ns
Bus Relinquish Time (Note 11)	$t_7$		20		75	20	85	20	90	ns
HBEN to $\overline{RD}$ Setup Time	$t_8$		0			0		0		ns
HBEN to $\overline{RD}$ Hold Time	$t_9$		0			0		0		ns
Delay Between Read Operations	$t_{10}$		200			200		200		ns

**Note 9:** Timing specifications are sample tested at  $25^\circ C$  to ensure compliance. All input control signals are specified with  $t_1 = t_1 = 5ns$  (10% to 90% of +5V) and timed from a voltage level of +1.6V.

**Note 10:**  $t_3$  and  $t_6$  are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.

**Note 11:**  $t_7$  is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

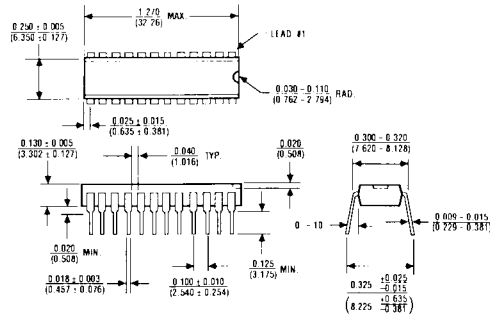
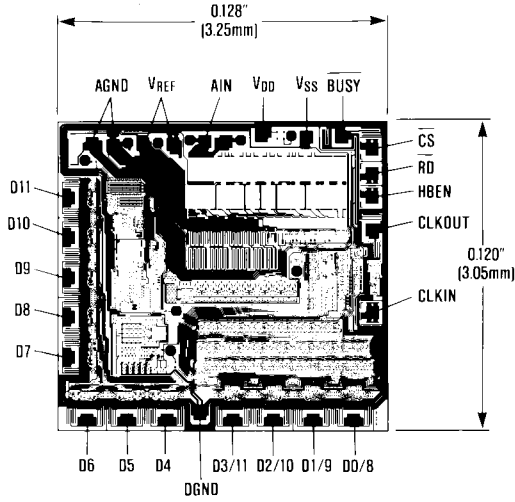
For additional information on using the MAX172 please refer to MAX162 data sheet.

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**MAX172**

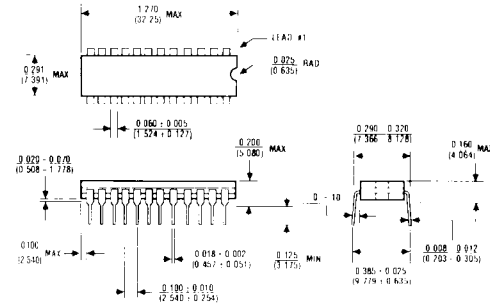
## Chip Topography

## Package Information



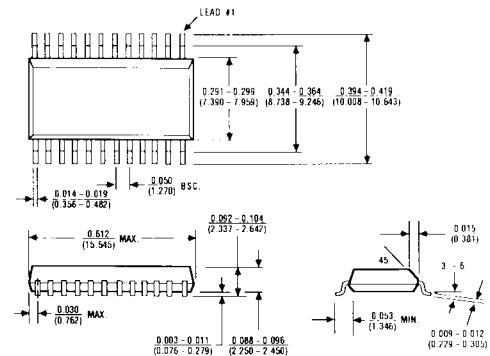
**24 Lead Plastic Narrow DIP (NG)**

$\theta_{JA} = 120^{\circ}\text{C/W}$   
 $\theta_{JC} = 60^{\circ}\text{C/W}$



**24 Lead Narrow CERDIP (RG)**

$\theta_{JA} = 80^{\circ}\text{C/W}$   
 $\theta_{JC} = 40^{\circ}\text{C/W}$



**24 Lead Small Outline, Wide (WG)**

$\theta_{JA} = 85^{\circ}\text{C/W}$   
 $\theta_{JC} = 45^{\circ}\text{C/W}$

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