19-4438; Rev 0; 1/09

EVALUATION KIT AVAILABLE

Dual-Phase, Quick-PWM Controller for IMVP6+ CPU Core Power Supplies

MAX17410

General Description

The MAX17410 is a 2-/1-phase interleaved Quick-PWM™ step-down VID power-supply controller for notebook IMVP6+ CPUs. True out-of-phase operation reduces input ripple current requirements and output voltage ripple while easing component selection and layout difficulties. The Quick-PWM control scheme provides instantaneous response to fast load current steps. Active voltage positioning reduces power dissipation and bulk output capacitance requirements and allows ideal positioning compensation for tantalum, polymer, or ceramic bulk output capacitors.

The MAX17410 is intended for two different CPU core applications: either bucking down the battery directly to create the core voltage, or bucking down the +5V system supply. The single-stage conversion method allows this device to directly step down high-voltage batteries for the highest possible efficiency. Alternatively, 2-stage conversion (stepping down the +5V system supply instead of the battery) at higher switching frequency provides the minimum possible physical size.

A slew-rate controller allows controlled transitions between VID codes. A thermistor-based temperature sensor provides programmable thermal protection. A power monitor provides a buffered analog voltage output proportional to the power delivered to the load.

The MAX17410 is available in a 48-pin, 7mm x 7mm TQFN package.

Applications

IMVP6+ Core Supply

Multiphase CPU Core Supply

Voltage-Positioned, Step-Down Converters

Notebook/Desktop Computers

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17410GTM+	-40°C to +105°C	48 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

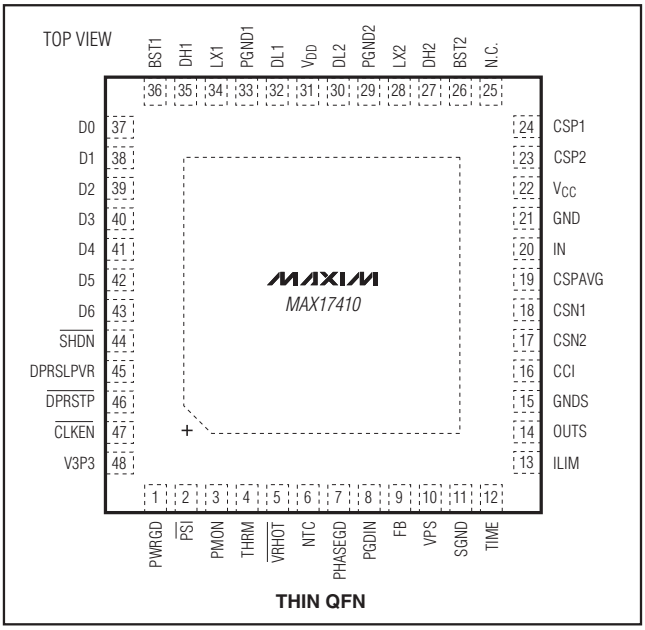
**EP = Exposed pad.*

Quick-PWM is a trademark of Maxim Integrated Products, Inc.

Features

- Dual-/Single-Phase Interleaved Quick-PWM Controller
- ±0.5% V_{OUT} Accuracy Over Line, Load, and Temperature
- 7-Bit IMVP6+ DAC
- Dynamic Phase Selection Optimizes Active/Sleep Efficiency
- Transient Phase Overlap Reduces Output Capacitance
- Active Voltage Positioning with Adjustable Gain
- Accurate Lossless Current Balance
- Accurate Droop and Current Limit
- Remote Output and Ground Sense
- Adjustable Output Slew-Rate Control
- Power-Good Window Comparator
- Power Monitor
- Programmable Thermal-Fault Protection
- Phase Fault Output (PHASEGD)
- Drives Large Synchronous Rectifier FETs
- 4.5V to 26V Battery Input Range
- Output Overvoltage and Undervoltage Protection
- Soft-Startup and Soft-Shutdown
- Integrated Boost Switches
- Low-Profile 7mm x 7mm, 48-Pin TQFN Package

Pin Configuration



Dual-Phase, Quick-PWM Controller for IMVP6+ CPU Core Power Supplies

ABSOLUTE MAXIMUM RATINGS

V_{CC}, V_{DD}, V3P3 to GND .....-0.3V to +6V
D0–D6, $\overline{PSI}$, DPRSLPVR, $\overline{DPRSTP}$ to GND .....-0.3V to +6V
CSPAVG, CSP_, CSN_, ILIM to GND .....-0.3V to +6V
PWRGD, PHASEGD, $\overline{VRHOT}$ to GND .....-0.3V to +6V
FB, OUTS, CCI, TIME, PMON to GND.....-0.3V to (V_{CC} + 0.3V)
PGDIN, NTC, THRM to GND .....-0.3V to (V_{CC} + 0.3V)
$\overline{CLKEN}$ to GND .....-0.3V to (V_{3P3} + 0.3V)
VPS to OUTS .....-0.3V to +0.3V
$\overline{SHDN}$ to GND (Note 1).....-0.3V to +30V
IN to GND .....-0.3V to +30V
GNDS, SGND, PGND_ to GND .....-0.3V to +0.3V
DL_ to GND .....-0.3V to (V_{DD} + 0.3V)
BST_ to V_{DD}.....-0.3V to +30V
LX_ to BST_ .....-6V to +0.3V
DH_ to LX_ .....-0.3V to (V_{BST} - +0.3V)
Continuous Power Dissipation (48-pin, 7mm x 7mm TQFN)
Up to +70°C 2222mW
Derating Above +70°C .....27.8mW/°C
Operating Temperature Range .....-40°C to +105°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: $\overline{SHDN}$ may be forced to 12V for the purpose of debugging prototype breadboards using the no-fault test mode.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGDIN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, V_{V3P3} = 3.3V, $V_{DPRSLPVR}$ = $V_{\overline{DPRSTP}}$ = V_{GNDS} = $V_{PGND\_}$ = 0, CSPAVG = CSP_ = CSN_ = OUTS = 1.0000V, R_{FB} = 3.57kΩ from FB to VPS, [D6–D0] = [0101000]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range		V_{CC}, V_{DD}		4.5		5.5	V
		V3P3		3.0		3.6	
		IN		4.5		26	
DC Output Voltage Accuracy	V_{OUT}	Measured at FB with respect to GNDS, includes load regulation error (Note 2)	DAC codes from 0.8125V to 1.5000V	-0.5		+0.5	%
			DAC codes from 0.3750V to 0.8000V	-7		+7	mV
			DAC codes from 0 to 0.3625V	-20		+20	
Boot Voltage	V_{BOOT}			1.192	1.200	1.209	V
Line Regulation Error		V_{CC} = 4.5V to 5.5V, V_{IN} = 4.5V to 26V			0.1		%
OUTS Input Bias Current		VPS floating, T_A = +25°C		-0.1		+0.1	µA
OUTS-to-VPS Resistance				3.5	10	40	Ω
SGND-to-AGND Resistance					2.5		Ω
GNDS Input Range				-200		+200	mV
GNDS Gain	A_{GNDS}	$\Delta V_{OUT}/\Delta V_{GNDS}$		0.97	1.00	1.03	V/V
GNDS Input Bias Current	I_{GNDS}	V(OUTS, GNDS) = 1.0V		-15	-10	-4	µA
TIME Regulation Voltage	V_{TIME}	R_{TIME} = 71.5kΩ		1.985	2.000	2.015	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGDIN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, V_{V3P3} = 3.3V, $V_{DPRSLPVR}$ = $V_{\overline{DPRSTP}}$ = V_{GNDS} = $V_{PGND\_}$ = 0, CSPAVG = CSP_ = CSN_ = OUTS = 1.0000V, R_{FB} = 3.57kΩ from FB to VPS, [D6–D0] = [0101000]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIME Slew-Rate Accuracy		R_{TIME} = 71.5kΩ (12.5mV/µs nominal)	-10		+10	%
		R_{TIME} = 35.7kΩ (25mV/µs nominal) to 178kΩ (5mV/µs nominal)	-15		+15	
		Soft-start and soft-shutdown: R_{TIME} = 35.7kΩ (3.125mV/µs nominal) to 178kΩ (0.625mV/µs nominal)	-16		+30	
		Slow: $V_{\overline{DPRSTP}}$ = $V_{DPRSLPVR}$ = 5V, 1/4 normal slew rate, R_{TIME} = 35.7kΩ (6.25mV/µs nominal) to 178kΩ (1.25mV/µs nominal)	-12		+25	
On-Time Accuracy	t_{ON}	V_{IN} = 10V, V_{FB} = 1.0V, V_{CCI} = (1.0V + V_{DIODE}), measured at DH_, 300kHz per phase nominal (Note 3)	300	333	366	ns
Minimum Off-Time	$t_{OFF(MIN)}$	Measured at DH_ (Note 3)		300	375	ns
BIAS CURRENTS						
Quiescent Supply Current (V_{CC})	I_{CC}	Measured at V_{CC}, $V_{DPRSLPVR}$ = 5V, FB forced above the regulation point		3	6	mA
Quiescent Supply Current (V_{DD})	I_{DD}	Measured at V_{DD}, $V_{DPRSLPVR}$ = 0, FB forced above the regulation point, T_A = +25°C		0.02	1	µA
Quiescent Supply Current (V3P3)	I_{3P3}	Measured at V3P3, FB forced within the $\overline{CLKEN}$ power-good window, T_A = +25°C		0.01	1	µA
Quiescent Supply Current (IN)	I_{IN}	Measured at IN, V_{IN} = 10V		15	25	µA
Shutdown Supply Current (V_{CC})	$I_{CC,SDN}$	Measured at V_{CC}, $\overline{SHDN}$ = GND, T_A = +25°C		0.01	1	µA
Shutdown Supply Current (V_{DD})	$I_{DD,SDN}$	Measured at V_{DD}, $\overline{SHDN}$ = GND, T_A = +25°C		0.01	1	µA
Shutdown Supply Current (V3P3)	$I_{3P3,SDN}$	Measured at V3P3, $\overline{SHDN}$ = GND, T_A = +25°C		0.01	1	µA
Shutdown Supply Current (IN)	$I_{IN,SDN}$	Measured at IN, V_{IN} = 26V, $\overline{SHDN}$ = GND, V_{CC} = 0V or 5V, T_A = +25°C		0.01	0.1	µA
FAULT PROTECTION						
Output Overvoltage-Protection Threshold	V_{OVP}	Skip mode after output reaches the regulation voltage or PWM mode, measured at FB with respect to the voltage target set by the VID code (see Table 4)	250	300	350	mV
		Soft-start, soft-shutdown, skip mode, and output has not reached the regulation voltage; measured at FB	1.75	1.80	1.85	V
		Minimum OVP threshold; measured at FB		0.8		
Output Overvoltage-Propagation Delay	t_{OVP}	FB forced 25mV above trip threshold		10		µs

Dual-Phase, Quick-PWM Controller for IMVP6+ CPU Core Power Supplies

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGDIN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, V_{V3P3} = 3.3V, $V_{DPRSLPVR}$ = $V_{\overline{DPRSTP}}$ = V_{GNDS} = $V_{PGND\_}$ = 0, CSPAVG = CSP_ = CSN_ = OUTS = 1.0000V, R_{FB} = 3.57kΩ from FB to VPS, [D6–D0] = [0101000]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Undervoltage-Protection Threshold	V_{UVP}	Measured at FB with respect to the voltage target set by the VID code; see Table 4		-450	-400	-350	mV
Output Undervoltage-Propagation Delay	t_{UVP}	FB forced 25mV below trip threshold			10		µs
$\overline{CLKEN}$ Startup Delay and Boot Time Period	t_{BOOT}	Measured from the time when FB reaches the boot target voltage (Note 2)		20	60	100	µs
PWRGD Startup Delay		Measured at startup from the time when $\overline{CLKEN}$ goes low		3	6.5	10	ms
$\overline{CLKEN}$ and PWRGD Threshold		Measured at FB with respect to the voltage target set by the VID code; see Table 4, 20mV hysteresis (typ)	Lower threshold, falling edge (undervoltage)	-350	-300	-250	mV
			Upper threshold, rising edge (overvoltage)	+150	+200	+250	
$\overline{CLKEN}$ and PWRGD Delay		FB forced 25mV outside the PWRGD trip thresholds			10		µs
PHASEGD Delay		V(CCI, FB) forced 25mV outside trip thresholds			10		µs
$\overline{CLKEN}$, PWRGD, and PHASEGD Transition Blanking Time (VID Transitions)	t_{BLANK}	Measured from the time when FB reaches the target voltage (Note 2)			20		µs
PHASEGD Transition Blanking Time (Phase 2 Enable Transitions)		Number of DH2 pulses for which PHASEGD is blanked after phase 2 is enabled			32		Pulses
$\overline{CLKEN}$ Output Low Voltage		Low state, I_{SINK} = 3mA				0.4	V
$\overline{CLKEN}$ Output High Voltage		High state, I_{SOURCE} = 3mA		V3P3 - 0.4			V
PWRGD, PHASEGD Output Low Voltage		Low state, I_{SINK} = 3mA				0.4	V
PWRGD, PHASEGD Leakage Current		High-impedance state; PWRGD, PHASEGD forced to 5V; T_A = +25°C				1	µA
CSN_ Pulldown Resistances in Shutdown		$\overline{SHDN}$ = 0, measured after soft-shutdown completed (DL = low)			10		Ω
V_{CC} Undervoltage-Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, 65mV typical hysteresis, controller disabled below this level		4.05	4.27	4.48	V
THERMAL PROTECTION							
THRM, NTC Pullup Current	I_{THRM}, I_{NTC}	V_{THRM} = V_{NTC} = 1V		40	50	60	µA
Ratio of NTC Pullup Current to THRM Pullup Current	I_{NTC}/I_{THRM}	V_{THRM} = V_{NTC} = 1V		0.995	1	1.025	µA/µA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGDIN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, V_{V3P3} = 3.3V, $V_{DPRSLPVR}$ = $V_{\overline{DPRSTP}}$ = V_{GNDS} = $V_{PGND\_}$ = 0, CSPAVG = CSP_ = CSN_ = OUTS = 1.0000V, R_{FB} = 3.57kΩ from FB to VPS, [D6–D0] = [0101000]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{VRHOT}$ Trip Threshold		Measured at NTC with respect to THRM, V_{THRM} = 1V, falling edge; typical hysteresis = 100mV		-12		+12	mV
$\overline{VRHOT}$ Delay	$t_{\overline{VRHOT}}$	V_{NTC} forced 25mV below V_{THRM}, V_{THRM} = 1V, falling edge			10		µs
$\overline{VRHOT}$ Output On-Resistance	$R_{ON(\overline{VRHOT})}$	Low state			2	8	Ω
$\overline{VRHOT}$ Leakage Current		High-impedance state, $\overline{VRHOT}$ forced to 5V, T_A = +25°C				1	µA
Thermal-Shutdown Threshold	T_{SHDN}	Typical hysteresis = 15°C			+160		°C
VALLEY CURRENT LIMIT, DROOP, CURRENT BALANCE, AND CURRENT MONITOR							
Current-Limit Threshold Voltage (Positive)	V_{LIMIT}	$V_{CSP\_}$ - $V_{CSN\_}$	V_{TIME} - V_{ILIM} = 100mV	7	10	13	mV
			V_{TIME} - V_{ILIM} = 500mV	45	50	55	
			ILIM = V_{CC}	20	22.5	25	
Current-Limit Threshold Voltage (Negative) Accuracy	$V_{LIMIT(NEG)}$	$V_{CSP\_}$ - $V_{CSN\_}$, nominally -125% of V_{LIMIT}		-4		+4	mV
Current-Limit Threshold Voltage (Zero Crossing)	V_{ZERO}	V_{AGND} - $V_{LX\_}$, DPRSLPVR = 5V			1		mV
CSPAVG, CSP_, CSN_ Common-Mode Input Range				0		2	V
Phase 2 Disable Threshold		Measured at CSP2		3	V_{CC} - 1	V_{CC} - 0.4	V
CSPAVG, CSP_, CSN_ Input Current	I_{CSPAVG}, $I_{CSP\_}$, $I_{CSN\_}$	T_A = +25°C		-0.2		+0.2	µA
ILIM Input Current	I_{ILIM}	T_A = +25°C		-0.1		+0.1	µA
Droop Amplifier Offset		[V_{CSPAVG} - (V_{CSN1} + V_{CSN2})/2] at I_{FB} = 0	T_A = +25°C	-0.5		+0.5	mV
			T_A = 0°C to +85°C	-0.75		+0.75	
Droop Amplifier Transconductance	$G_{m(FB)}$	$\Delta I_{FB}/\Delta$[V_{CSPAVG} - (V_{CSN1} + V_{CSN2})/2], V_{FB} = $V_{CSN\_}$ = 0.45V to 1.5V		1.180	1.2	1.216	mS
Power Monitor Output Voltage for Typical HFM Conditions	V_{PMON}	V(OUTS, GNDS) = 1.200V, I_{PMON} = 0µA	[V_{CSPAVG} - (V_{CSN1} + V_{CSN2})/2] = 15mV, V(TIME, ILIM) = 225mV	1.65	1.7	1.743	V
			[V_{CSPAVG} - (V_{CSN1} + V_{CSN2})/2] = 15mV, V(TIME, ILIM) = 500mV	0.738	0.765	0.792	
Power Monitor Gain Referred to Output Voltage V(OUTS, GNDS)	A_{PMON}/V_{OUT}	[V_{CSPAVG} - (V_{CSN1} + V_{CSN2})/2] = 15mV, V(TIME, ILIM) = 225mV, I_{PMON} = 0µA		1.375	1.4167	1.452	V/V
Power Monitor Gain Referred to [V_{CSPAVG} - (V_{CSN1} + V_{CSN2})/2]	A_{PMON}/V_{CS}	V(CSN, GNDS) = 1.200V, V(TIME, ILIM) = 225mV, I_{PMON} = 0µA		104	113.33	123	V/V

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGDIN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, V_{V3P3} = 3.3V, $V_{DPRSLPVR}$ = $V_{\overline{DPRSTP}}$ = V_{GNDS} = $V_{PGND\_}$ = 0, CSPAVG = CSP_ = CSN_ = OUTS = 1.0000V, R_{FB} = 3.57kΩ from FB to VPS, [D6–D0] = [0101000]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power Monitor Load Regulation		Measured at PMON with respect to unloaded voltage	I_{PMON} = 0 to 500µA	-6			µV/µA
			I_{PMON} = -100µA		50		mV
Current Balance Amplifier Offset		(V_{CSP1} - V_{CSN1}) - (V_{CSP2} - V_{CSN2}) at I_{CCI} = 0		-1.0		+1.0	mV
Current Balance Amplifier Transconductance	$G_{m(CCI)}$	$\Delta I_{CCI}/\Delta[(V_{CSP1} - V_{CSN1}) - (V_{CSP2} - V_{CSN2})]$, $V_{CSN\_}$ = 0.45V to 1.5V			200		µS
GATE DRIVERS							
DH_ Gate-Driver On-Resistance	$R_{ON(DH\_)}$	BST_ - LX_ forced to 5V	High state (pullup)		0.9	2.5	Ω
			Low state (pulldown)		0.7	2.0	
DL_ Gate-Driver On-Resistance	$R_{ON(DL\_)}$	High state (pullup)			0.7	2.0	Ω
		Low state (pulldown)			0.25	0.7	
DH_ Gate-Driver Source Current	$I_{DH\_(SOURCE)}$	DH_ forced to 2.5V, BST_ - LX_ forced to 5V			2.2		A
DH_ Gate-Driver Sink Current	$I_{DH\_(SINK)}$	DH_ forced to 2.5V, BST_ - LX_ forced to 5V			2.7		A
DL_ Gate-Driver Source Current	$I_{DL\_(SOURCE)}$	DL_ forced to 2.5V			2.7		A
DL_ Gate-Driver Sink Current	$I_{DL\_(SINK)}$	DL_ forced to 2.5V			8		A
Driver Propagation Delay	$t_{DH\_DL\_}$	DH_ low to DL_ high			20		ns
	$t_{DL\_DH\_}$	DL_ low to DH_ high			20		
DL_ Transition Time		DL_ falling, $C_{DL\_}$ = 3nF			20		ns
		DL_ rising, $C_{DL\_}$ = 3nF			20		
DH_ Transition Time		DH_ falling, $C_{DH\_}$ = 3nF			20		ns
		DH_ rising, $C_{DH\_}$ = 3nF			20		
Internal BST_ Switch On-Resistance	$R_{ON(BST\_)}$				10	20	Ω
LOGIC AND I/O							
Logic Input High Voltage	V_{IH}	$\overline{SHDN}$, PGDIN, DPRSLPVR		2.3			V
Logic Input Low Voltage	V_{IL}	$\overline{SHDN}$, PGDIN, DPRSLPVR				1.0	V
Low-Voltage Logic Input High Voltage	V_{IHLV}	$\overline{PSI}$, D0–D6, $\overline{DPRSTP}$		0.67			V
Low-Voltage Logic Input Low Voltage	V_{ILLV}	$\overline{PSI}$, D0–D6, $\overline{DPRSTP}$				0.33	V
Logic Input Current		T_A = +25°C, PGDIN		-1.5	-1	-0.5	µA
		T_A = +25°C, $\overline{SHDN}$, DPRSLPVR, $\overline{PSI}$, $\overline{DPRSTP}$, D0–D6 = 0 or 5V		-1		+1	

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGDIN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, V_{V3P3} = 3.3V, $V_{DPRSLPVR}$ = $V_{\overline{DPRSTP}}$ = V_{GNDS} = $V_{PGND\_}$ = 0, CSPAVG = CSP_ = CSN_ = OUTS = 1.0000V, R_{FB} = 3.57kΩ from FB to VPS, [D6–D0] = [0101000]; **T_A = -40°C to +105°C**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range		V_{CC}, V_{DD}		4.5		5.5	V
		V3P3		3.0		3.6	
		IN		4.5		26	
DC Output Voltage Accuracy	V_{OUT}	Measured at FB with respect to GNDS, includes load regulation error (Note 2)	DAC codes from 0.8125V to 1.5000V	-0.75		+0.75	%
			DAC codes from 0.3750V to 0.8000V	-10		+10	mV
			DAC codes from 0 to 0.3625V	-25		+25	
Boot Voltage	V_{BOOT}			1.185		1.215	V
OUTS to VPS Resistance				3.5		40	Ω
GNDS Input Range				-200		+200	mV
GNDS Gain	A_{GNDS}	$\Delta V_{OUT}/\Delta V_{GNDS}$		0.97		1.03	V/V
GNDS Input Bias Current	I_{GNDS}	V(OUTS, GNDS) = 1.0V		-15		-4	µA
TIME Regulation Voltage	V_{TIME}	R_{TIME} = 71.5kΩ		1.985		2.015	V
TIME Slew-Rate Accuracy		R_{TIME} = 71.5kΩ (12.5mV/µs nominal)		-10		+10	%
		R_{TIME} = 35.7kΩ (25mV/µs nominal) to 178kΩ (5mV/µs nominal)		-15		+15	
		Soft-start and soft-shutdown: R_{TIME} = 35.7kΩ (3.125mV/µs nominal) to 178kΩ (0.625mV/µs nominal)		-16		+30	
		Slow: $V_{\overline{DPRSTP}}$ = $V_{DPRSLPVR}$ = 5V, 1/4 normal slew rate, R_{TIME} = 35.7kΩ (6.25mV/µs nominal) to 178kΩ (1.25mV/µs nominal)		-12		+25	
On-Time Accuracy	t_{ON}	V_{IN} = 10V, V_{FB} = 1.0V, V_{CCI} = (1.0V + V_{DIODE}), measured at DH_, 300kHz per phase nominal (Note 3)		290	333	376	ns
Minimum Off-Time	$t_{OFF(MIN)}$	Measured at DH_ (Note 3)				375	ns
BIAS CURRENTS							
Quiescent Supply Current (V_{CC})	I_{CC}	Measured at V_{CC}, $V_{DPRSLPVR}$ = 5V, FB forced above the regulation point				6	mA
Quiescent Supply Current (IN)	I_{IN}	Measured at IN, V_{IN} = 10V				25	µA

Dual-Phase, Quick-PWM Controller for IMVP6+ CPU Core Power Supplies

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGDIN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, V_{V3P3} = 3.3V, $V_{DPRSLPVR}$ = $V_{\overline{DPRSTP}}$ = V_{GNDS} = $V_{PGND\_}$ = 0, CSPAVG = CSP_ = CSN_ = OUTS = 1.0000V, R_{FB} = 3.57kΩ from FB to VPS, [D6–D0] = [0101000]; **T_A = -40°C to +105°C**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FAULT PROTECTION							
Output Overvoltage-Protection Threshold	V_{OVP}	Skip mode after output reaches the regulation voltage or PWM mode; measured at FB with respect to the voltage target set by the VID code (see Table 4)		250		350	mV
		Soft-start, soft-shutdown, skip mode, and output has not reached the regulation voltage; measured at FB		1.75		1.85	V
Output Undervoltage-Protection Threshold	V_{UVP}	Measured at FB with respect to the voltage target set by the VID code (see Table 4)		-450		-350	mV
$\overline{CLKEN}$ Startup Delay and Boot Time Period	t_{BOOT}	Measured from the time when FB reaches the boot target voltage (Note 2)		20		100	µs
PWRGD Startup Delay		Measured at startup from the time when $\overline{CLKEN}$ goes low		3		10	ms
$\overline{CLKEN}$ and PWRGD Threshold		Measured at FB with respect to the voltage target set by the VID code (see Table 4), 20mV hysteresis (typ)	Lower threshold, falling edge (undervoltage)	-350		-250	mV
			Upper threshold, rising edge (overvoltage)	+150		+250	
$\overline{CLKEN}$ Output Low Voltage		Low state, I_{SINK} = 3mA				0.4	V
$\overline{CLKEN}$ Output High Voltage		High state, I_{SOURCE} = 3mA		V3P3 - 0.4			V
PWRGD, PHASEGD Output Low Voltage		Low state, I_{SINK} = 3mA				0.4	V
PWRGD, PHASEGD Leakage Current		High-impedance state; PWRGD, PHASEGD forced to 5V; T_A = +25°C				1	µA
V_{CC} Undervoltage-Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, 65mV typical hysteresis, controller disabled below this level		4.0		4.5	V
THERMAL PROTECTION							
THRM, NTC Pullup Current	I_{THRM}, I_{NTC}	V_{THRM} = V_{NTC} = 1V		40		60	µA
Ratio of NTC Pullup Current to THRM Pullup Current	I_{NTC}/I_{THRM}	V_{THRM} = V_{NTC} = 1V		0.993		1.03	µA/µA
$\overline{VRHOT}$ Trip Threshold		Measured at NTC with respect to THRM, V_{THRM} = 1V, falling edge; typical hysteresis = 100mV		-12		+12	mV
$\overline{VRHOT}$ Output On-Resistance	$R_{ON(\overline{VRHOT})}$	Low state				8	Ω

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGDIN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, V_{V3P3} = 3.3V, $V_{DPRSLPVR}$ = $V_{\overline{DPRSTP}}$ = V_{GNDS} = $V_{PGND\_}$ = 0, CSPAVG = CSP_ = CSN_ = OUTS = 1.0000V, R_{FB} = 3.57kΩ from FB to VPS, [D6–D0] = [0101000]; **T_A = -40°C to +105°C**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
VALLEY CURRENT LIMIT, DROOP, CURRENT BALANCE, AND CURRENT MONITOR							
Current-Limit Threshold Voltage (Positive)	V_{LIMIT}	$V_{CSP\_}$ - $V_{CSN\_}$	V_{TIME} - V_{ILIM} = 100mV	7		13	mV
			V_{TIME} - V_{ILIM} = 500mV	45		55	
			ILIM = V_{CC}	20		25	
Current-Limit Threshold Voltage (Negative) Accuracy	$V_{LIMIT(NEG)}$	$V_{CSP\_}$ - $V_{CSN\_}$, nominally -125% of V_{LIMIT}		-5		+5	mV
CSPAVG, CSP_, CSN_ Common-Mode Input Range				0		2	V
Phase 2 Disable Threshold		Measured at CSP2		3		V_{CC} - 0.4	V
Droop Amplifier Offset		[V_{CSPAVG} - (V_{CSN1} + V_{CSN2})/2] at I_{FB} = 0	T_A = +25°C	-0.75		+0.75	mV
			T_A = 0°C to +85°C	-1		+1	
Droop Amplifier Transconductance	$G_{m(FB)}$	$\Delta I_{FB}/\Delta[V_{CSPAVG} - (V_{CSN1} + V_{CSN2})/2]$, V_{FB} = V_{CSN-} = 0.45V to 1.5V		1.173		1.224	mS
Power Monitor Output Voltage for Typical HFM Conditions	V_{PMON}	V(OUTS, GNDS) = 1.200V, I_{PMON} = 0µA	[V_{CSPAVG} - (V_{CSN1} + V_{CSN2})/2] = 15mV, V(TIME, ILIM) = 225mV	1.627		1.768	V
			[V_{CSPAVG} - (V_{CSN1} + V_{CSN2})/2] = 15mV, V(TIME, ILIM) = 500mV	0.734		0.796	
Power Monitor Gain Referred to Output Voltage V(OUTS, GNDS)	$A_{PMON/VOUT}$	[V_{CSPAVG} - (V_{CSN1} + V_{CSN2})/2] = 15mV, V(TIME, ILIM) = 225mV, I_{PMON} = 0µA		1.375		1.452	V/V
Power Monitor Gain Referred to [V_{CSPAVG} - (V_{CSN1} + V_{CSN2})/2]	$A_{PMON/VCS}$	V(CSN, GNDS) = 1.200V, V(TIME, ILIM) = 225mV, I_{PMON} = 0µA		104		123	V/V
Power Monitor Load Regulation		Measured at PMON with respect to unloaded voltage	I_{PMON} = 0 to 500µA	-6			µV/µA
Current Balance Amplifier Offset		(V_{CSP1} - V_{CSN1}) - (V_{CSP2} - V_{CSN2}) at I_{CCI} = 0		-1.5		+1.5	mV

Dual-Phase, Quick-PWM Controller for IMVP6+ CPU Core Power Supplies

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGDIN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, V_{V3P3} = 3.3V, $V_{DPRSLPVR}$ = $V_{\overline{DPRSTP}}$ = V_{GNDS} = $V_{PGND\_}$ = 0, CSPAVG = CSP_ = CSN_ = OUTS = 1.0000V, R_{FB} = 3.57kΩ from FB to VPS, [D6–D0] = [0101000]; **T_A = -40°C to +105°C**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GATE DRIVERS							
DH_ Gate-Driver On-Resistance	$R_{ON(DH\_)}$	BST_ - LX_ forced to 5V	High state (pullup)			2.5	Ω
			Low state (pulldown)			2.0	
DL_ Gate-Driver On-Resistance	$R_{ON(DL\_)}$	High state (pullup)				2.0	Ω
		Low state (pulldown)				0.7	
Internal BST_ Switch On-Resistance	$R_{ON(BST\_)}$	$I_{BST\_}$ = 10mA				20	Ω
LOGIC AND I/O							
Logic Input High Voltage	V_{IH}	$\overline{SHDN}$, PGDIN, DPRSLPVR		2.3			V
Logic Input Low Voltage	V_{IL}	$\overline{SHDN}$, PGDIN, DPRSLPVR				1.0	V
Low-Voltage Logic Input High Voltage	V_{IHLV}	$\overline{PSI}$, D0–D6, $\overline{DPRSTP}$		0.67			V
Low-Voltage Logic Input Low Voltage	V_{ILLV}	$\overline{PSI}$, D0–D6, $\overline{DPRSTP}$				0.33	V

Note 2: DC output accuracy specifications refer to the trip level of the error amplifier. The output voltage has a DC regulation higher than the trip level by 50% of the output ripple. When pulse skipping, the output rises by approximately 1.5% when transitioning from continuous conduction to no load.

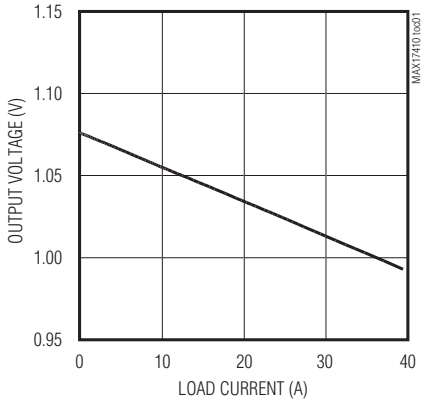
Note 3: On-time and minimum off-time specifications are measured from 50% to 50% at the DL_ and DH_ pins, with LX_ forced to GND, BST_ forced to 5V, and a 500pF capacitor from DH_ to LX_ to simulate external MOSFET gate capacitance. Actual in-circuit times might be different due to MOSFET switching speeds.s

Dual-Phase, Quick-PWM Controller for IMVP6+ CPU Core Power Supplies

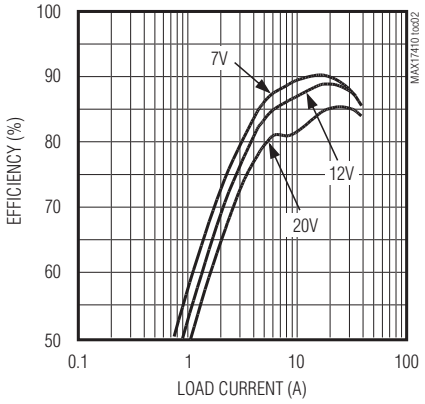
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = 12V, V_{CC} = V_{DD} = 5V, $\overline{SHDN}$ = V_{CC}, D0–D6 set for 1.1500V, T_A = +25°C, unless otherwise specified.)

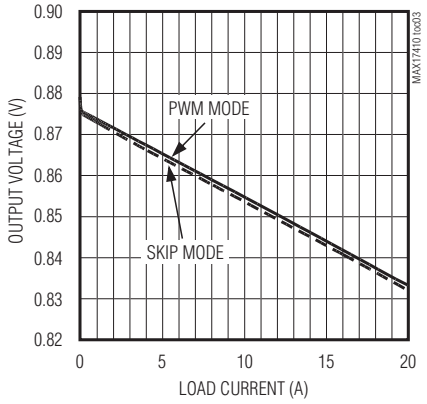
2-PHASE OUTPUT VOLTAGE vs. LOAD CURRENT ($V_{OUT(HFM)}$ = 1.075V)



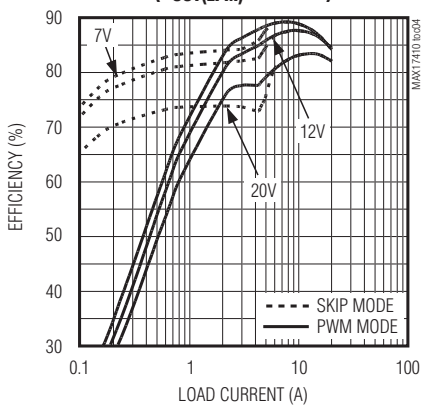
2-PHASE EFFICIENCY vs. LOAD CURRENT ($V_{OUT(HFM)}$ = 1.075V)



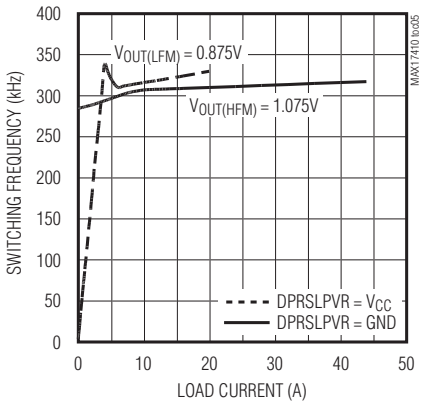
1-PHASE OUTPUT VOLTAGE vs. LOAD CURRENT ($V_{OUT(HFM)}$ = 0.875V)



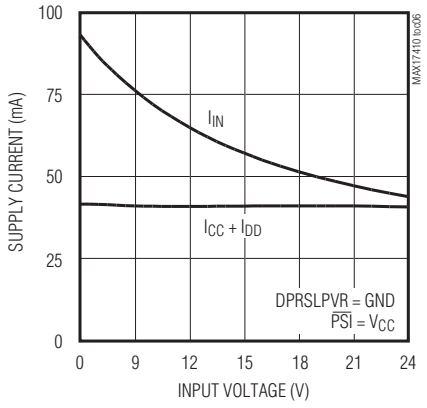
1-PHASE EFFICIENCY vs. LOAD CURRENT ($V_{OUT(LFM)}$ = 0.875V)



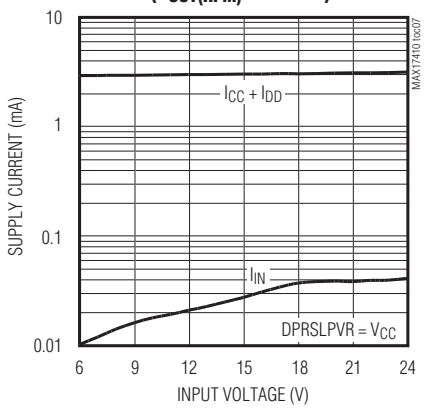
SWITCHING FREQUENCY vs. LOAD CURRENT



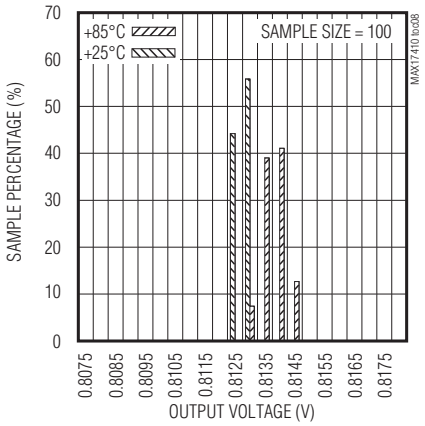
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE ($V_{OUT(HFM)}$ = 1.075V)



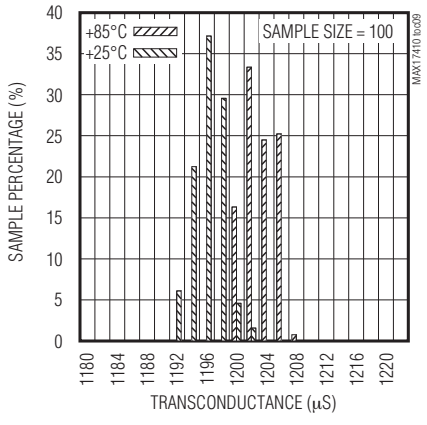
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE AT SKIP MODE ($V_{OUT(HFM)}$ = 1.075V)



0.8125V OUTPUT-VOLTAGE DISTRIBUTION



Gm(FB) TRANSCONDUCTANCE DISTRIBUTION

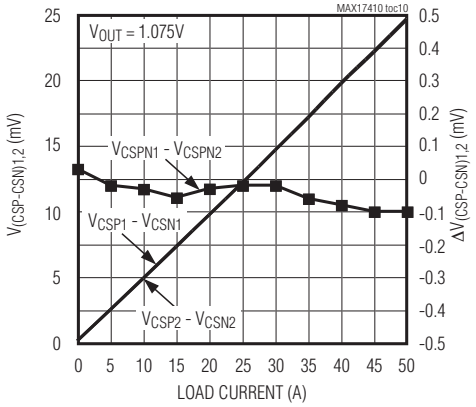


Dual-Phase, Quick-PWM Controller for IMVP6+ CPU Core Power Supplies

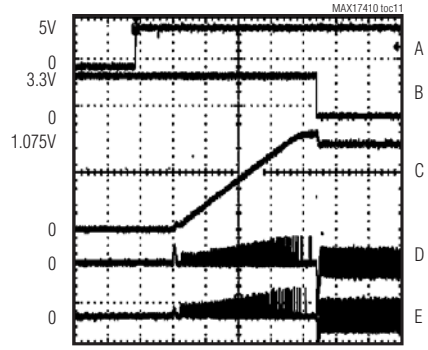
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{CC} = V_{DD} = 5V, $\overline{SHDN}$ = V_{CC}, D0–D6 set for 1.1500V, T_A = +25°C, unless otherwise specified.)

CURRENT BALANCE vs. LOAD CURRENT

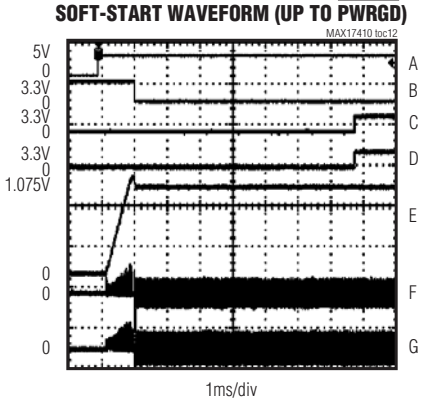


SOFT-START WAVEFORM (UP TO $\overline{CLKEN}$)



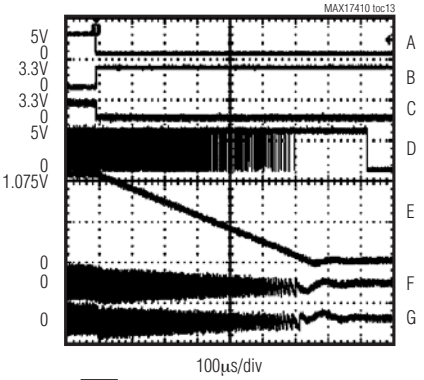
A. $\overline{SHDN}$, 5V/div
B. $\overline{CLKEN}$, 3.3V/div
C. V_{OUT}, 500mV/div
D. I_{LX1}, 10A/div
E. I_{LX2}, 10A/div
I_{OUT} = 0

SOFT-START WAVEFORM (UP TO $\overline{PWRGD}$)



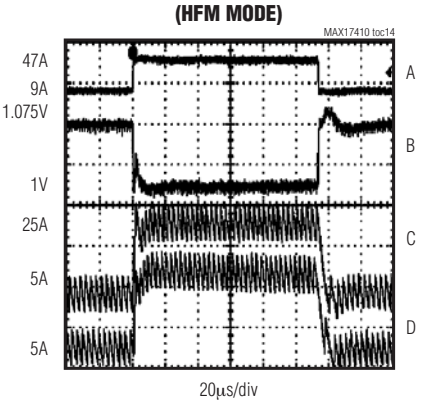
A. $\overline{SHDN}$, 10V/div
B. $\overline{CLKEN}$, 6.6V/div
C. PWRGD, 10V/div
D. PHASEGD, 10V/div
E. V_{OUT}, 500mV/div
F. I_{LX1}, 10A/div
G. I_{LX2}, 10A/div
I_{OUT} = 0

SHUTDOWN WAVEFORM



A. $\overline{SHDN}$, 10V/div
B. PWRGD, 10V/div
C. $\overline{CLKEN}$, 6.6V/div
D. DL1, 5V/div
E. V_{OUT}, 500mV/div
F. I_{LX1}, 10A/div
G. I_{LX2}, 10A/div

LOAD-TRANSIENT RESPONSE (HFM MODE)

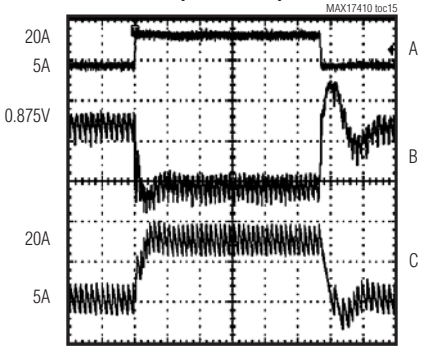


A. I_{OUT} = 9A–47A
B. V_{OUT}, 50mV/div
C. I_{LX1}, 10A/div
D. I_{LX2}, 10A/div

Typical Operating Characteristics (continued)

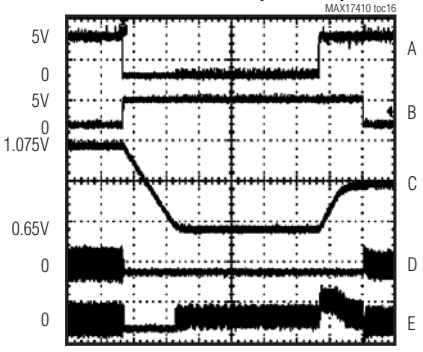
(Circuit of Figure 1, V_{IN} = 12V, V_{CC} = V_{DD} = 5V, $\overline{SHDN}$ = V_{CC}, D0–D6 set for 1.1500V, T_A = +25°C, unless otherwise specified.)

LOAD-TRANSIENT RESPONSE (LFM MODE)



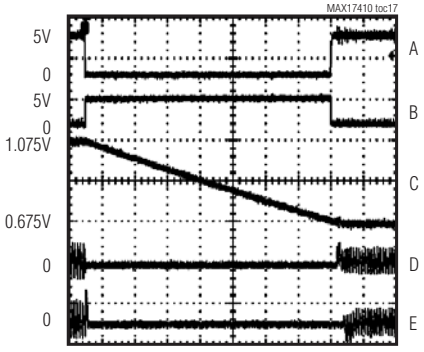
A. I_{OUT} = 5A–20A
B. V_{OUT}, 20mV/div
C. I_{LX1}, 10A/div
$\overline{PSI}$ = GND
DPRSLPVR = GND

ENTERING DEEPER SLEEP EXITING TO LFM (SLOW C4)



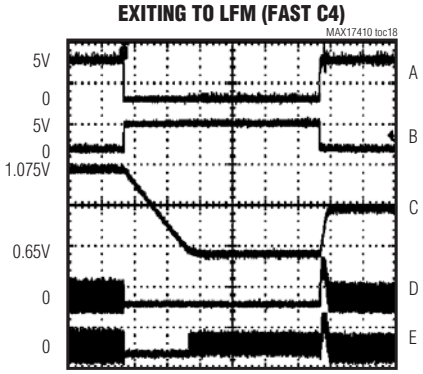
A. $\overline{DPRSTP}$, 5V/div
B. DPRSLPVR, 10V/div
C. V_{OUT}, 200mV/div
D. I_{LX2}, 10A/div
E. I_{LX1}, 10A/div
I_{OUT} = 3A

ENTERING DEEPER SLEEP EXITING TO NEAREST VID



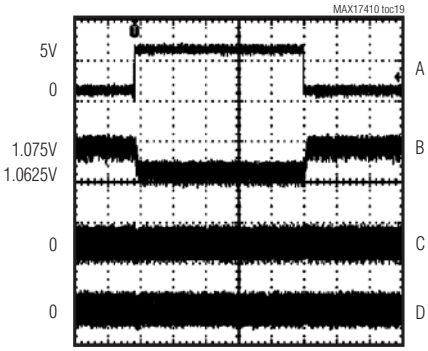
A. $\overline{DPRSTP}$, 5V/div
B. DPRSLPVR, 10V/div
C. V_{OUT}, 200mV/div
D. I_{LX2}, 10A/div
E. I_{LX1}, 10A/div
I_{OUT} = 3Av

ENTERING DEEPER SLEEP EXITING TO LFM (FAST C4)



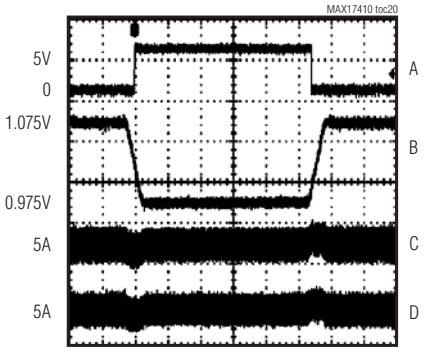
A. $\overline{DPRSTP}$, 5V/div
B. DPRSLPVR, 10V/div
C. V_{OUT}, 200mV/div
D. I_{LX2}, 10A/div
E. I_{LX1}, 10A/div
I_{OUT} = 3Av

D0 12.5mV DYNAMIC VID CODE CHANGE



A. VID0, 5V/div
B. V_{OUT}, 20mV/div
C. I_{LX1}, 10A/div
D. I_{LX2}, 10A/div

D3 10mV DYNAMIC VID CODE CHANGE



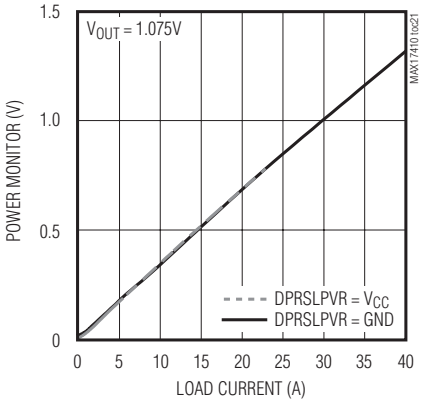
A. D3, 5V/div
B. V_{OUT}, 50mV/div
I_{OUT}, = 10A
C. I_{LX1}, 10A/div
D. I_{LX2}, 10A/div

Dual-Phase, Quick-PWM Controller for IMVP6+ CPU Core Power Supplies

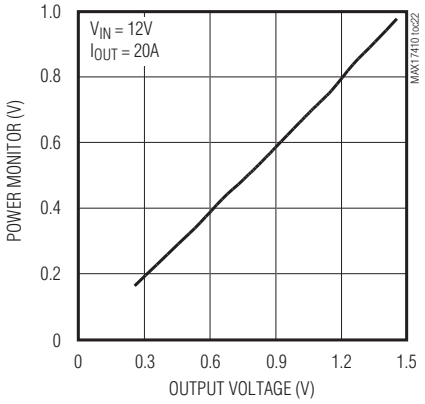
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{CC} = V_{DD} = 5V, $\overline{SHDN}$ = V_{CC}, D0–D6 set for 1.1500V, T_A = +25°C, unless otherwise specified.)

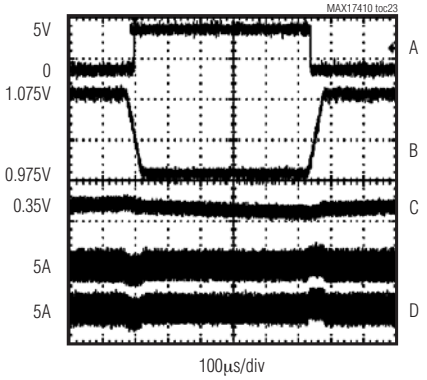
MAX17410 POWER MONITOR vs. LOAD CURRENT



MAX17410 POWER MONITOR vs. OUTPUT VOLTAGE

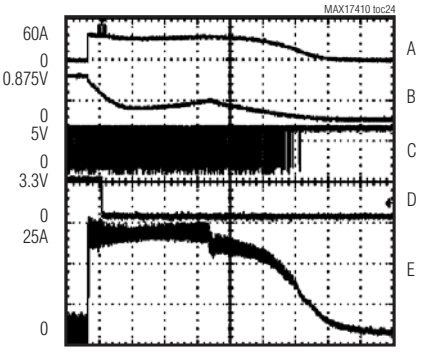


POWER MONITOR VID TRANSITION RESPONSE



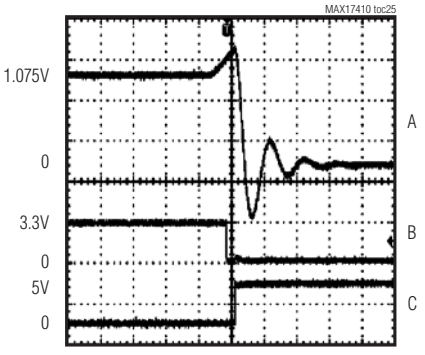
A. D3, 5V/div
B. V_{OUT}, 50mV/div
I_{OUT} = 10A
C. V_{PMON}, 50mV/div
D. I_{LX1}, 10A/div
E. I_{LX2}, 10A/div

OUTPUT UNDERVOLTAGE FAULT



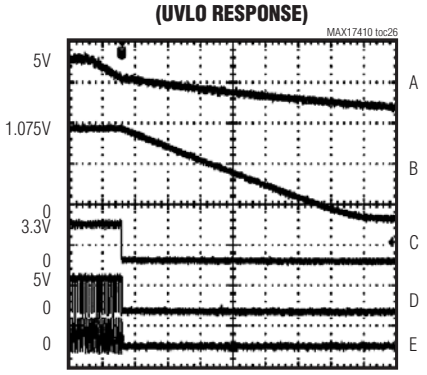
A. I_{OUT}, 100A/div
B. V_{OUT}, 500mV/div
C. DL, 5V/div
D. PWRGD, 3.3V/div
E. I_{LX1}, 10A/div

OUTPUT OVERVOLTAGE WAVEFORM



A. V_{OUT}, 500mV/div
B. PWRGD, 3.3V/div
C. DL1, 5V/div
DPRSLPVR = V_{CC}

BIAS SUPPLY REMOVAL (UVLO RESPONSE)



A. 5V BIAS SUPPLY, 2V/div
B. V_{OUT}, 500mV/div
C. PWRGD, 3.3V/div
D. DL1, 5V/div
E. I_{LX1}, 10A/div
I_{OUT} = 5A

Pin Description

PIN	NAME	FUNCTION
1	PWRGD	Open-Drain Power-Good Output. After output voltage transitions, except during power-up and power-down, if FB is in regulation, then PWRGD is high impedance. PWRGD is low during startup, continues to be low while the output is at the boot voltage, and stays low until 5ms (typ) after $\overline{CLKEN}$ goes low, after which it starts monitoring the FB voltage and goes high if FB is within the PWRGD threshold window. PWRGD is forced low during soft-shutdown and while in shutdown. PWRGD is forced high impedance whenever the slew-rate controller is active (output voltage transitions), and continues to be forced high impedance for an additional 20µs after the transition is completed. The PWRGD upper threshold is blanked during any downward output voltage transition that happens when the controller is in skip mode, and stays blanked until the slew-rate-controlled internal-transition-related PWRGD blanking period is complete and the output reaches regulation. A pullup resistor on PWRGD causes additional finite shutdown current.
2	$\overline{PSI}$	Power-State Indicator. This low-voltage logic input indicates power usage and sets the operating mode together with DPRSLPVR as shown in the truth table below. While DPRSLPVR is low, if $\overline{PSI}$ is forced low, the controller is immediately set to 1-phase forced-PWM mode. The controller returns to 2-phase forced-PWM mode when $\overline{PSI}$ is forced high. DPRSLPVR / $\overline{PSI}$ / Mode 1 / 0 / Very low current (1-phase skip) 1 / 1 / Low current (approx 3A) (1-phase skip) 0 / 0 / Intermediate power potential (1-phase PWM) 0 / 1 / Max power potential (full-phase PWM: 2-phase or 1-phase as set by user at CSP2) The controller is in 2-phase skip mode during startup, but is in 2-phase forced-PWM mode during soft-shutdown, irrespective of the DPRSLPVR and $\overline{PSI}$ logic levels. The controller is also in 2-phase skip mode while in boot mode, but is in 2-phase forced-PWM mode during the transition from boot mode to VID mode, irrespective of the DPRSLPVR and $\overline{PSI}$ logic levels. However, if phase 2 is disabled by connecting CSP2 to V_{CC}, then only phase 1 is active in the above modes.
3	PMON	Power Monitor Output: $V(PWR) = K_{PWR} \times V(OUTS, GNDS) \times V(CSPAVG, CSN)/V(TIME, ILIM)$ where K_{PWR} = 21.25 typical. If ILIM is externally connected to a 5V rail to enable the internal default/preset current-limit threshold, then the V(TIME, ILIM) value to be used in the above equation is 225mV. Do not use the power monitor in any configuration that would cause its output V(PMON) to exceed (V_{CC} - 0.5V). PMON is pulled to ground when the MAX17410 is in shutdown.
4	THRM	Resistive Input of Thermal Comparator. Connect a resistor to ground to set the $\overline{VRHOT}$ threshold. THRM and NTC have matched 50µA current sources, so the resistance value = the NTC resistance at the desired high temperature. $\overline{VRHOT}$ is pulled low when the voltage at NTC goes below the voltage at THRM.
5	$\overline{VRHOT}$	Open-Drain Output of Internal Comparator. $\overline{VRHOT}$ is pulled low when the voltage at NTC goes below the voltage at THRM. $\overline{VRHOT}$ is high impedance in shutdown.
6	NTC	Thermistor Input of Thermal Comparator. Connect a standard thermistor to ground. THRM and NTC have matched 50µA current sources, so the resistance value = the NTC resistance at the desired high temperature. $\overline{VRHOT}$ is pulled low when the voltage at NTC goes below the voltage at THRM.

Dual-Phase, Quick-PWM Controller for IMVP6+ CPU Core Power Supplies

Pin Description (continued)

PIN	NAME	FUNCTION
7	PHASEGD	Open-Drain Phase-Good Output. Used to signal the system that one of the two phases either has a fault condition or is not matched with the other. Detection is done by identifying the need for a large (more than 40%) on-time difference between phases to achieve or move towards current balance. PHASEGD is low in shutdown, and when phase 2 is disabled by connecting CSP2 to V_{CC}. PHASEGD is forced high impedance whenever the slew-rate controller is active (output voltage transitions), and when phase 2 is disabled by the DPRSLPVR and/or $\overline{PSI}$ inputs. When phase 2 is reenabled, PHASEGD stays high impedance for 32 DH2 pulses, after which it monitors the difference between the on-times of the two phases. PHASEGD is also forced high impedance when V_{FB} is below 0.5V.
8	PGDIN	Power-Good Logic Input. Indicates the power status of other system rails and used for supply sequencing. Connect this pin to the 5V supply rail or float it if the feature is not needed. During startup, after soft-starting to the boot voltage, the output voltage remains at V_{BOOT}, and the $\overline{CLKEN}$ and PWRGD outputs remain high and low, respectively, as long as the PGDIN input stays low. When PGDIN later goes high, the output is allowed to transition to the voltage set by the VID code, and $\overline{CLKEN}$ is allowed to go low. During normal operation, if PGDIN goes low, the controller immediately forces $\overline{CLKEN}$ high and PWRGD low, and slews the output to the boot voltage while in 2-phase skip mode at 1/8 the normal slew rate set by the TIME resistor. The output then stays at the boot voltage until the controller is turned off or power cycled, or until PGDIN goes high again.
9	FB	Feedback Voltage Input, and Output of the Voltage-Positioning Transconductance Amplifier. The voltage at the FB pin is compared with the slew-rate-controlled target voltage by the error comparator (fast regulation loop), as well as by the internal voltage integrator (slow, accurate regulation loop). Having sufficient ripple signal at FB that is in-phase with the sum of the inductor currents is essential for cycle-by-cycle stability. Connect resistor R_{FB} between FB and VPS to set the droop based on the voltage-positioning gain requirements: $R_{FB} = R_{DROOP}/[R_{SENSE} \times G_{m(FB)}]$ where R_{DROOP} is the desired voltage-positioning slope, $G_{m(FB)}$ = 1.2mS typ, and R_{SENSE} is the effective current-sense resistance that is used to provide the (CSPAVG, CSN_) current-sense voltage. If lossless sensing (inductor DCR sensing) is used, consider using a thermistor as part of the CSPAVG filter network to minimize the temperature dependence of the voltage-positioning slope. FB is high impedance in shutdown.
10	VPS	Internally Shorted to OUTS Through a 10Ω Resistance
11	SGND	Internally Shorted SGND (Pin 11) to AGND (Pin 21)
12	TIME	Slew-Rate Adjustment Pin. The total resistance R_{TIME} from TIME to GND sets the internal slew rate. SLEW RATE = (12.5mV/µs) x (71.5kΩ/R_{TIME}) where R_{TIME} is between 35.7kΩ and 178kΩ. This “normal” slew rate applies to transitions into and out of the low-power pulse-skipping modes and to the transition from boot mode to VID. The slew rate for startup and for entering shutdown is always 1/8 of normal. If DPRSLPVR and $\overline{DPRSTP}$ are both high, then the slew rate is reduced to 1/4 of normal. If the VID DAC inputs are clocked, the slew rate for all other VID transitions is set by the rate at which they are clocked, up to a maximum slew rate equal to the normal slew rate defined above.
13	ILIM	Current-Limit Adjust Input. The valley positive current-limit threshold voltages at V(CSP_, CSN_) are precisely 1/10 the differential voltage V(TIME, ILIM) over a 0.1V to 0.5V range of V(TIME, ILIM). The valley negative current-limit thresholds are typically -125% of the corresponding valley positive current-limit thresholds. Connect ILIM to V_{CC} to get the default current-limit threshold setting of 22.5mV typ.

Pin Description (continued)

PIN	NAME	FUNCTION
14	OUTS	Output Remote Sense. Internally shorted to VPS through a 10Ω resistance. OUTS is also the voltage feedback input to the power monitor.
15	GNDS	Feedback Remote-Sense Input, Negative Side. Normally connected to GND directly at the load. GNDS internally connects to a transconductance amplifier that fine tunes the output voltage—compensating for voltage drops from the regulator ground to the load ground.
16	CCI	Current-Balance Compensation. Connect a 470pF capacitor between CCI and the positive side of the feedback remote-sense input (or between CCI and GND). CCI is internally forced low in shutdown.
17	CSN2	Negative Input of the Output Current Sense of Phase 2. This pin should be connected to the negative side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing.
18	CSN1	Negative Input of the Output Current Sense of Phase 1. This pin should be connected to the negative side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing.
19	CSPAVG	Positive Input of the Output Current-Sense Averaging Network. This input should be connected to the positive current-sense averaging network (see the standard 2-phase IMVP6+ application circuit of Figure 1) and is utilized for load line control and power monitoring (input of the transconductance amplifiers used for FB and PMON).
20	IN	Input Sense for On-Time Control. An internal resistor sets the switching frequency to 300kHz per phase. IN is high impedance in shutdown.
21	GND	Analog Ground Connect
22	V_{CC}	Controller Supply Voltage. Connect to a 4.5V to 5.5V source. Bypass to GND with 1µF minimum.
23	CSP2	Positive Input of the Output Current Sense of Phase 2. This pin should be connected to the positive side of the output current-sensing resistor, or to the filtering capacitor if the DC resistance of the output inductor is used for current sensing. This pin is utilized for current limit and current balance only. Connect CSP2 to V_{CC} to disable phase 2 and use the MAX17410 as a single-phase controller. In this configuration, connect LX2 to GND, connect BST2 to V_{DD}, CSN2 to CSN1, and float DH2, DL2, CCI, and PHASEGD.
24	CSP1	Positive Input of the Output Current Sense of Phase 1. This pin should be connected to the positive side of the output current-sensing resistor, or to the filtering capacitor if the DC resistance of the output inductor is used for current sensing. This pin is utilized for current limit and current balance only.
25	N.C.	No Connection. Not internally connected.
26	BST2	Phase 2 Boost Flying Capacitor Connection. BST2 is the internal upper supply rail for the DH2 high-side gate driver. An internal switch between V_{DD} and BST2 charges the BST2 - LX2 flying capacitor while the low-side MOSFET is on (DL2 pulled high).
27	DH2	Phase 2 High-Side Gate-Driver Output. DH2 swings from LX2 to BST2. Low in shutdown.
28	LX2	Phase 2 Inductor Connection. LX2 is the internal lower supply rail for the DH2 high-side gate driver. Also used as an input to phase 2's zero-crossing comparator.
29	PGND2	Power Ground. PGND2 is the internal lower supply rail for the DL2 low-side gate driver.
30	DL2	Phase 2 Low-Side Gate-Driver Output. DL2 swings from PGND2 to V_{DD}. DL2 is forced low in shutdown. DL2 is forced high when an output overvoltage fault is detected, overriding any negative current-limit condition that might be present. DL2 is forced low in skip mode after detecting an inductor current zero crossing.
31	V_{DD}	Supply Voltage Input for the DL_ Drivers. V_{DD} is also the supply voltage used to internally recharge the BST_ - LX_ flying capacitor during the times the respective DL_ are high. Connect V_{DD} to the 4.5V to 5.5V system supply voltage. Bypass V_{DD} to GND with a 1µF or greater ceramic capacitor.

Dual-Phase, Quick-PWM Controller for IMVP6+ CPU Core Power Supplies

Pin Description (continued)

PIN	NAME	FUNCTION
32	DL1	Phase 1 Low-Side Gate-Driver Output. DL1 swings from PGND1 to V_{DD}. DL1 is forced low in shutdown. DL1 is forced high when an output overvoltage fault is detected, overriding any negative current-limit condition that might be present. DL1 is forced low in skip mode after detecting an inductor current zero crossing.
33	PGND1	Power Ground. PGND1 is the internal lower supply rail for the DL1 low-side gate driver.
34	LX1	Phase 1 Inductor Connection. LX1 is the internal lower supply rail for the DH1 high-side gate driver. Also used as an input to phase 1's zero-crossing comparator.
35	DH1	Phase 1 High-Side Gate-Driver Output. DH1 swings from LX1 to BST1. Low in shutdown.
36	BST1	Phase 1 Boost Flying Capacitor Connection. BST1 is the internal upper supply rail for the DH1 high-side gate driver. An internal switch between V_{DD} and BST1 charges the BST1 - LX1 flying capacitor, while the low-side MOSFET is on (DL1 pulled high).
37–43	D0–D6	Low-Voltage (1.0V Logic) VID DAC Code Inputs. The D0–D6 inputs do not have internal pullups. These 1.0V logic inputs are designed to interface directly with the CPU. The output voltage is set by the VID code indicated by the logic-level voltages on D0–D6 (see Table 4).
44	$\overline{SHDN}$	Shutdown Control Input. Connect to V_{CC} for normal operation. Connect to ground to put the IC into the 1µA (max at T_A = +25°C) shutdown state. During startup, the output voltage is ramped up at 1/8 the slew rate set by the TIME resistor to the boot voltage. During the transition from normal operation to shutdown, the output voltage is ramped down at 1/8 the slew rate set by the TIME resistor. Forcing $\overline{SHDN}$ to 11V ~ 13V disables overvoltage protection, undervoltage protection, and thermal shutdown, clears the fault latches, disables transient phase overlap, disables soar suppression, and turns off the internal BST_-to-V_{DD} switches. However, internal diodes still exist between BST_ and V_{DD} in this state.
45	DPRSLPVR	3.3V Logic Input. Indicates power usage and sets the operating mode together with $\overline{PSI}$ as shown in the truth table below. When DPRSLPVR is forced high, the controller is immediately set to 1-phase automatic pulse-skipping mode. The controller returns to forced-PWM mode when DPRSLPVR is forced low **and** the output is in regulation. The PWRGD upper threshold is blanked during any downward output voltage transition that happens when the controller is in skip mode, and stays blanked until the slew-rate-controlled internal-transition-related PWRGD blanking period is complete and the output reaches regulation. During this blanking period, the overvoltage fault threshold is changed from a tracking [VID + 300mV] threshold to a fixed 1.8V threshold. DPRSLPVR / $\overline{PSI}$ / Mode 1 / 0 / Very low current (1-phase skip) 1 / 1 / Low current (approx 3A) (1-phase skip) 0 / 0 / Intermediate power potential (1-phase PWM) 0 / 1 / Max power potential (full-phase PWM: 2-phase or 1-phase as set by user at CSP2) The controller is in 2-phase skip mode during startup, but is in 2-phase forced-PWM mode during soft-shutdown, irrespective of the DPRSLPVR and $\overline{PSI}$ logic levels. The controller is in 2-phase skip mode while in boot mode, but is in 2-phase forced-PWM mode during the transition from boot mode to VID mode, irrespective of the DPRSLPVR and $\overline{PSI}$ logic levels. However, if phase 2 is disabled by connecting CSP2 to V_{CC}, then only phase 1 is active in the above modes.

Pin Description (continued)

PIN	NAME	FUNCTION
46	$\overline{DPRSTP}$	Low-Voltage Logic Input Signal. This is usually the logical complement of the DPRSLPVR signal. However, there is a special condition during C4 exit when both $\overline{DPRSTP}$ and DPRSLPVR could temporarily be simultaneously high. If this happens, the MAX17410 reduces the slew rate to 1/4 the normal (R_{TIME}-based) slew rate for the duration of this condition. The slew rate returns to normal when this condition is exited. Note that only DPRSLPVR and $\overline{PSI}$ (but **not** $\overline{DPRSTP}$) determine the mode of operation (PWM vs. skip and number of active phases). DPRSLPVR / $\overline{DPRSTP}$ / Functionality 0 / 0 / Normal slew rate, 1- or 2-phase forced-PWM mode (DPRSLPVR low ➔ $\overline{DPRSTP}$ is ignored) 0 / 1 / Normal slew rate, 1- or 2-phase forced-PWM mode (DPRSLPVR low ➔ $\overline{DPRSTP}$ is ignored) 1 / 0 / Normal slew rate, 1-phase automatic pulse-skipping mode 1 / 1 / Slew rate reduced to 1/4th of normal, 1-phase automatic pulse-skipping mode
47	$\overline{CLKEN}$	Clock Enable CMOS Push-Pull Logic Output Powered by V3P3. This inverted logic output indicates when the output voltage sensed at FB is in regulation. $\overline{CLKEN}$ is forced high in shutdown and during soft-start and soft-stop transitions. $\overline{CLKEN}$ is forced low during dynamic VID transitions and for an additional 20µs after the transition is completed. $\overline{CLKEN}$ is the inverse of PWRGD, except for the 5ms PWRGD startup delay period after $\overline{CLKEN}$ is pulled low. See the startup timing diagram (Figure 9). The $\overline{CLKEN}$ upper threshold is blanked during any downward output voltage transition that happens when the controller is in skip mode, and stays blanked until the slew-rate-controlled internal-transition-related PWRGD blanking period is complete **and** the output reaches regulation.
48	V3P3	3.3V Supply Input for the $\overline{CLKEN}$ CMOS Push-Pull Logic Output. Connect to the 3.0V to 3.6V system supply voltage.
—	EP	Exposed Backplate (Paddle) of Package. Internally connected to analog ground. Connect to the ground plane through a thermally enhanced via.

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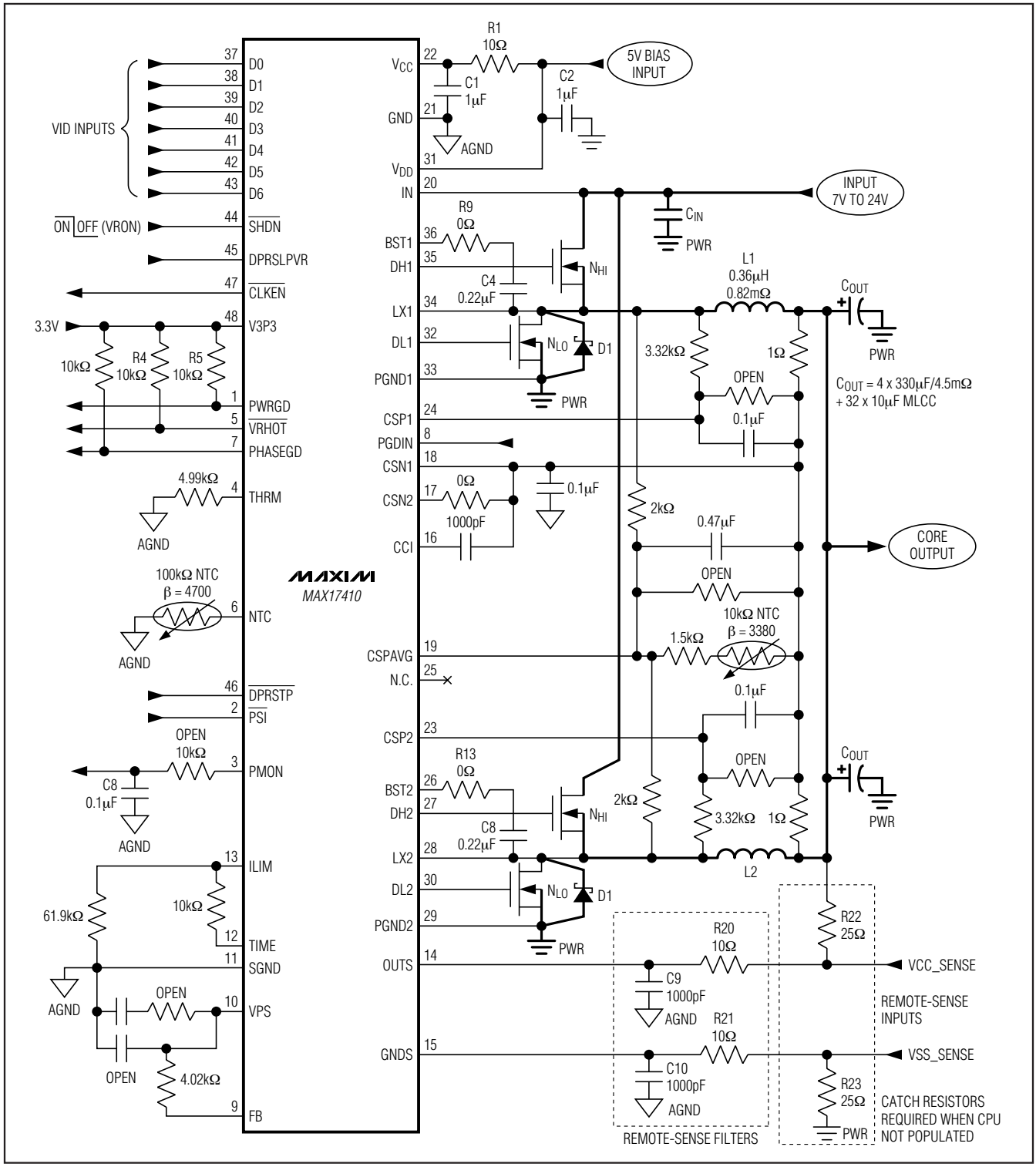

Figure 1. Standard 2-Phase IMVP6+ Application Circuit

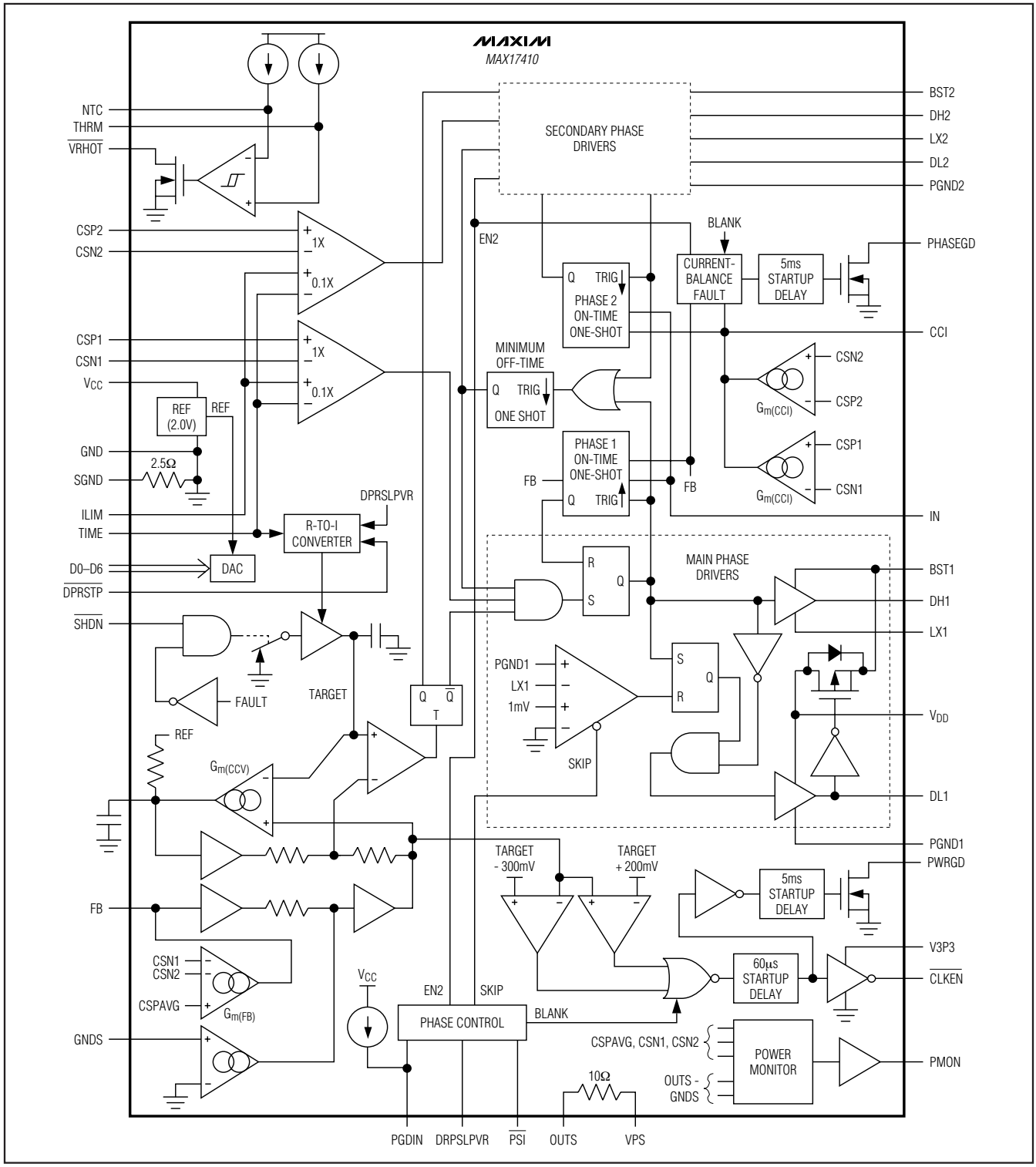

Figure 2. Functional Diagram

Dual-Phase, Quick-PWM Controller for IMVP6+ CPU Core Power Supplies

Table 1. Component Selection for Standard Applications

DESIGN PARAMETERS	IMVP6+ SV	IMVP6+ LV
Circuit	Figure 1	Figure 1
Input Voltage Range	7V to 20V	7V to 20V
Maximum Load Current	44A (34A)	23A (19A)
Transient Load Current	35A (10A/µs)	18A (10A/µs)
Load Line	-2.1mV/A	-4mV/A
Inductance (L)	NEC/Tokin MPC1055LR36 0.36µH, 32A, 0.8mΩ	NEC/Tokin MPC1055LR36 0.36µH, 32A, 0.8mΩ
High-Side MOSFET (N_H)	Siliconix 1x Si4386DY 7.8mΩ/9.5mΩ (typ/max)	Siliconix 1x Si4386DY 7.8mΩ/9.5mΩ (typ/max)
Low-Side MOSFET (N_L)	Siliconix 2x Si4642DY 3.9mΩ/4.7mΩ (typ/max)	Siliconix 2x Si4642DY 3.9mΩ/4.7mΩ (typ/max)
Output Capacitors (C_{OUT})	3x 330µF, 6mΩ, 2.5V Panasonic EEFSX0D0D331XR 28x 10µF, 6V ceramic (0805)	3x 330µF, 6mΩ, 2.5V Panasonic EEFSX0D0D331XR 28x 10µF, 6V ceramic (0805)
Input Capacitors (C_{IN})	4x 10µF, 25V ceramic (1210)	4x 10µF, 25V ceramic (1210)
TIME-ILIM Resistance (R1)	10kΩ	6.19kΩ
ILIM-GND Resistance (R2)	61.9kΩ	64.9kΩ
FB Resistance (R_{FB})	4.02kΩ	7.68kΩ
LX-CSP Resistance (R5)	2kΩ	2kΩ
CSP-CSN Series Resistance (R6)	1.50kΩ	1.50kΩ
Parallel NTC Resistance (R7)	open	open
DCR Sense NTC (NTC1)	10kΩ NTC B = 3380 TDK NTCG163JH103F	10kΩ NTC B = 3380 TDK NTCG163JH103F
DCR Sense Capacitance (C_{SENSE})	0.47µF, 6V ceramic (0805)	0.47µF, 6V ceramic (0805)

Table 2. Component Suppliers

MANUFACTURER	WEBSITE
AVX Corporation	www.avxcorp.com
BI Technologies	www.bitechnologies.com
Central Semiconductor Corp.	www.centralsemi.com
Fairchild Semiconductor	www.fairchildsemi.com
International Rectifier	www.irf.com
KEMET Corp.	www.kemet.com
NEC/TOKIN America, Inc.	www.nec-tokin.com
Panasonic Corp.	www.panasonic.com

MANUFACTURER	WEBSITE
Pulse Engineering	www.pulseeng.com
Renesas Technology Corp.	www.renesas.com
SANYO Electric Co., Ltd.	www.sanyodevice.com
Sumida Corp.	www.sumida.com
Taiyo Yuden	www.t-yuden.com
TDK Corp.	www.component.tdk.com
TOKO America, Inc.	www.tokoam.com
Vishay/Siliconix	www.vishay.com

MAX17410 Detailed Description

Free-Running, Constant On-Time PWM Controller with Input Feed-Forward

The Quick-PWM control architecture is a pseudo-fixed-frequency, constant-on-time, current-mode regulator with voltage feed-forward (Figure 2). This architecture relies on the output filter capacitor's ESR to act as the current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose period is inversely proportional to the input voltage, and directly proportional to the output voltage or the difference between the main and secondary inductor currents (see the *On-Time One-Shot* section). Another one-shot sets a minimum off-time. The on-time one-shot triggers when the error comparator goes low, the inductor current of the selected phase is below the valley current-limit threshold, and the minimum off-time one-shot times out. The controller maintains 180° out-of-phase operation by alternately triggering the main and secondary phases after the error comparator drops below the output-voltage set point.

Dual 180° Out-of-Phase Operation

The two phases in the MAX17410 operate 180° out-of-phase to minimize input and output filtering requirements, reduce electromagnetic interference (EMI), and improve efficiency. This effectively lowers component count—reducing cost, board space, and component power requirements—making the MAX17410 ideal for high-power, cost-sensitive applications.

Typically, switching regulators provide power using only one phase instead of dividing the power among several phases. In these applications, the input capacitors must support high instantaneous current requirements. The high RMS ripple current can lower efficiency due to I^2R power loss associated with the input capacitor's effective series resistance (ESR). Therefore, the system typically requires several low-ESR input capacitors in parallel to minimize input voltage ripple, to reduce ESR-related power losses, and to meet the necessary RMS ripple current rating.

With the MAX17410, the controller shares the current between two phases that operate 180° out-of-phase, so the high-side MOSFETs never turn on simultaneously during normal operation. The instantaneous input current of either phase is effectively halved, resulting in reduced input voltage ripple, ESR power loss, and RMS ripple current (see the *Input Capacitor Selection* section). Therefore, the same performance may be achieved with fewer or less expensive input capacitors.

+5V Bias Supply (V_{CC} and V_{DD})

The Quick-PWM controller requires an external +5V bias supply in addition to the battery. Typically, this +5V bias supply is the notebook's 95% efficient +5V system supply. Keeping the bias supply external to the IC improves efficiency and eliminates the cost associated with the +5V linear regulator that would otherwise be needed to supply the PWM circuit and gate drivers. If stand-alone capability is needed, the +5V bias supply can be generated with an external linear regulator.

The +5V bias supply must provide V_{CC} (PWM controller) and V_{DD} (gate-drive power), so the maximum current drawn is:

$$I_{BIAS} = I_{CC} + f_{SW}\left(Q_{G(LOW)} + Q_{G(HIGH)}\right)$$

where I_{CC} is provided in the *Electrical Characteristics* table, f_{SW} is the switching frequency, and $Q_{G(LOW)}$ and $Q_{G(HIGH)}$ are the MOSFET data sheet's total gate-charge specification limits at V_{GS} = 5V.

V_{IN} and V_{DD} can be connected together if the input power source is a fixed +4.5V to +5.5V supply. If the +5V bias supply is powered up prior to the battery supply, the enable signal ($\overline{SHDN}$ going from low to high) must be delayed until the battery voltage is present to ensure startup.

Switching Frequency

IN (Pin 20) Open-Circuit Protection

The MAX17410 input sense (IN) is used to adjust the on-time. An internal resistor sets the switching frequency to 300kHz per phase. IN is high impedance in shutdown.

On-Time One-Shot

The core of each phase contains a fast, low-jitter, adjustable one-shot that sets the high-side MOSFET's on-time. The one-shot for the main phase varies the on-time in response to the input and feedback voltages. The main high-side switch on-time is inversely proportional to the input voltage as measured by the V+ input, and proportional to the feedback voltage (V_{FB}):

$$t_{ON(MAIN)} = \frac{t_{SW}\left(V_{FB} + 0.075V\right)}{V_{IN}}$$

where the switching period (t_{SW} = 1/f_{SW}) is set to 3.3µs internally, and 0.075V is an approximation to accommodate the expected drop across the low-side MOSFET switch.

Dual-Phase, Quick-PWM Controller for IMVP6+ CPU Core Power Supplies

The one-shot for the secondary phase varies the on-time in response to the input voltage and the difference between the main and secondary inductor currents. Two identical transconductance amplifiers integrate the difference between the master and slave current-sense signals. The summed output is internally connected to CCI, allowing adjustment of the integration time constant with a compensation network connected between CCI and FB. The resulting compensation current and voltage are determined by the following equations:

$$I_{CCI} = G_m\left(V_{CSP1} - V_{CSN1}\right) - G_m\left(V_{CSP2} - V_{CSP2}\right)$$

$$V_{CCI} = V_{FB} + I_{CCI}Z_{CCI}$$

where Z_{CCI} is the impedance at the CCI output. The secondary on-time one-shot uses this integrated signal (V_{CCI}) to set the secondary high-side MOSFET's on-time. When the main and secondary current-sense signals become unbalanced, the transconductance amplifiers adjust the secondary on-time, which increases or decreases the secondary inductor current until the current-sense signals are properly balanced:

$$t_{ON(SEC)} = t_{SW}\left(\frac{V_{CCI} + 0.075V}{V_{IN}}\right)$$

$$= t_{SW}\left(\frac{V_{FB} + 0.075V}{V_{IN}}\right) + t_{SW}\left(\frac{I_{CCI}Z_{CCI}}{V_{IN}}\right)$$

$$= \left(\text{Main On-time}\right) + \left(\text{Secondary Current Balance Correction}\right)$$

This algorithm results in a nearly constant switching frequency and balanced inductor currents despite the lack of a fixed-frequency clock generator. The constant switching frequency allows the inductor ripple-current operating point to remain relatively constant, resulting in easy design methodology and predictable output voltage ripple.

On-times translate only roughly to switching frequencies. The on-times guaranteed in the *Electrical Characteristics* table are influenced by switching delays in the external high-side MOSFET. Resistive losses, including the inductor, both MOSFETs, output capacitor ESR, and PCB copper losses in the output and ground tend to raise the switching frequency at higher output currents. Also, the dead-time effect increases the effective on-time, reducing the switching frequency. It occurs only during forced-PWM operation and dynamic output voltage transitions when the inductor current reverses at light or negative load currents. With reversed inductor current, the inductor's EMF causes LX to go high earlier than normal, extending the on-time by a period equal to the DH rising dead time. For loads above the critical conduction point, where the dead-time effect is no longer a factor, the actual switching frequency (per phase) is:

$$f_{SW} = \frac{\left(V_{OUT} + V_{DIS}\right)}{t_{ON}\left(V_{IN} + V_{DIS} - V_{CHG}\right)}$$

where V_{DIS} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PCB resistances; V_{CHG} is the sum of the parasitic voltage drops in the inductor charge path, including high-side switch, inductor, and PCB resistances; and t_{ON} is the on-time as defined in the *Electrical Characteristics* table.

Current Sense

The output current of each phase is sensed. Low offset amplifiers are used for current balance, voltage-positioning gain, and current limit. Sensing the current at the output of each phase offers advantages, including less noise sensitivity, more accurate current sharing between phases, and the flexibility of using either a current-sense resistor or the DC resistance of the output inductor.

Using the DC resistance (R_{DCR}) of the output inductor allows higher efficiency. In this configuration, the initial tolerance and temperature coefficient of the inductor's DCR must be accounted for in the output-voltage droop-error budget and power monitor. This current-sense method uses an RC filtering network to extract the current information from the output inductor (see Figure 3). The resistive divider used should provide a current-sense resistance (R_{CS}) low enough to meet the current-limit requirements, and the time constant of the RC network should match the inductor's time constant (L/R_{CS}):

$$R_{CS} = \left(\frac{R2}{R1 + R2}\right)R_{DCR}$$

and:

$$R_{CS} = \frac{L}{C_{EQ}}\left[\frac{1}{R1} + \frac{1}{R2}\right]$$

where R_{CS} is the required current-sense resistance, and R_{DCR} is the inductor's series DC resistance. Use the worst-case inductance and R_{DCR} values provided by the inductor manufacturer, adding some margin for the inductance drop over temperature and load. To minimize the current-sense error due to the current-sense inputs' bias current ($I_{CSP\_}$ and $I_{CSN\_}$), choose R1 ll R2 to be less than 2kΩ and use the above equation to

determine the sense capacitance (C_{EQ}). Choose capacitors with 5% tolerance and resistors with 1% tolerance specifications. Temperature compensation is recommended for this current-sense method. See the *Voltage Positioning and Loop Compensation* section for detailed information.

When using a current-sense resistor for accurate output-voltage positioning, the circuit requires a differential RC filter to eliminate the AC voltage step caused by the equivalent series inductance (L_{ESL}) of the current-sense resistor (see Figure 3). The ESL-induced voltage step does not affect the average current-sense voltage, but results in a significant peak current-sense voltage error that results in unwanted offsets in the regulation voltage and results in early current-limit detection. Similar to the inductor DCR sensing method, the RC filter's time constant should match the L/R time constant formed by the current-sense resistor's parasitic inductance:

$$\frac{L_{ESL}}{R_{SENSE}} = C_{EQ}R1$$

where L_{ESL} is the equivalent series inductance of the current-sense resistor, R_{SENSE} is current-sense resistance value, C_{EQ} and R1 are the time-constant matching components.

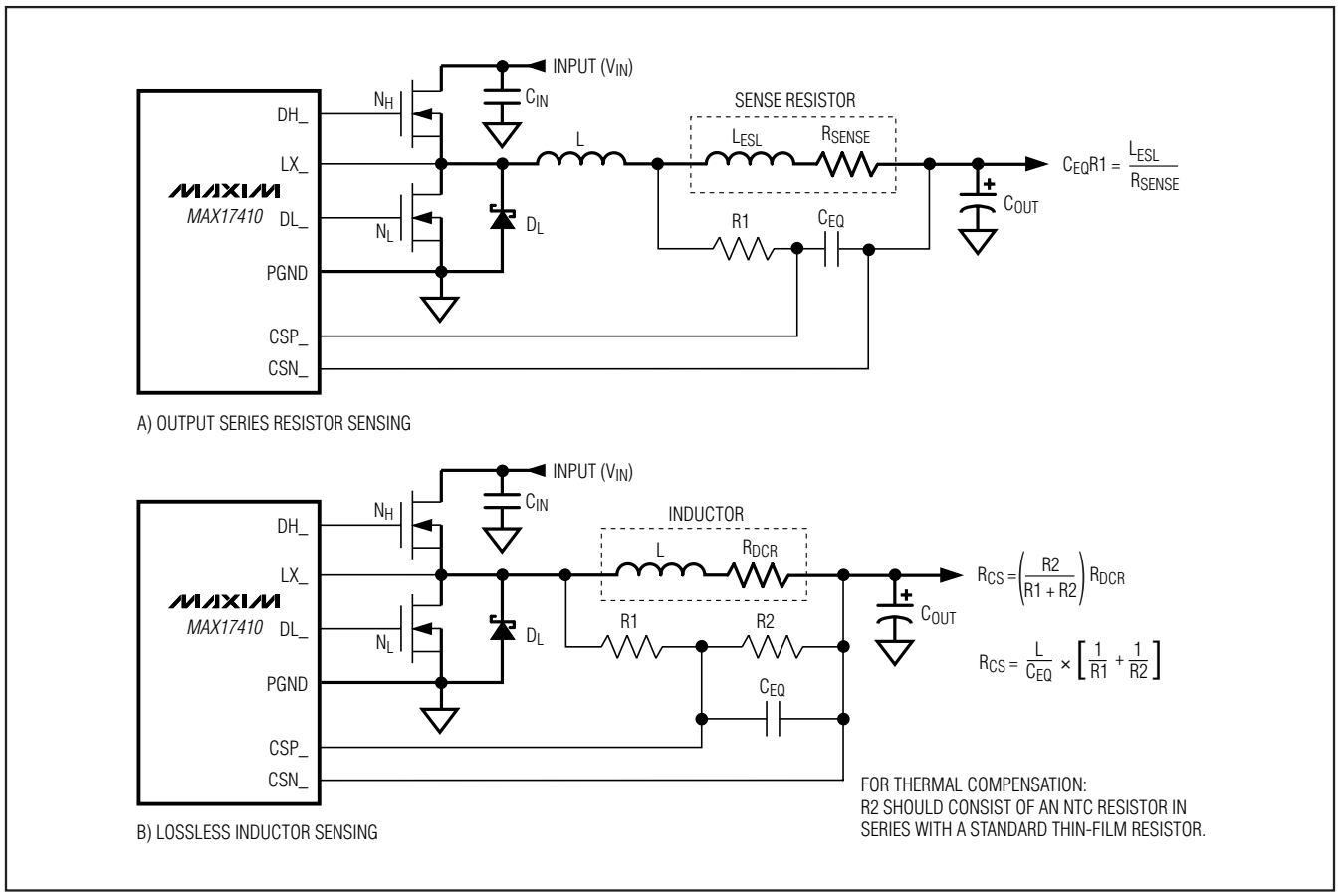

Figure 3. Current-Sense Methods

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Current Balance

The MAX17410 integrates the difference between the current-sense voltages and adjusts the on-time of the secondary phase to maintain current balance. The current balance now relies on the accuracy of the current-sense resistors instead of the inaccurate, thermally sensitive on-resistance of the low-side MOSFETs. With active current balancing, the current mismatch is determined by the current-sense resistor values and the offset voltage of the transconductance amplifiers:

$$I_{OS(IBAL)} = I_{LMAIN} - I_{LSEC} = \frac{V_{OS(IBAL)}}{R_{CS}}$$

where R_{CS} is the effective sense resistance and $V_{OS(IBAL)}$ is the current-balance offset specification in the *Electrical Characteristics* table.

The worst-case current mismatch occurs immediately after a load transient due to inductor value mismatches resulting in different di/dt for the two phases. The time it takes the current-balance loop to correct the transient imbalance depends on the mismatch between the inductor values and switching frequency.

Current Limit

The current-limit circuit employs a unique "valley" current-sensing algorithm that uses current-sense resistors between the current-sense inputs (CSP_ to CSN_) as the current-sensing elements. If the current-sense signal of the selected phase is above the current-limit threshold, the PWM controller does not initiate a new cycle until the inductor current of the selected phase drops below the valley current-limit threshold. When either phase trips the current limit, both phases are effectively current limited since the interleaved controller does not initiate a cycle with either phase.

Since only the valley current is actively limited, the actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the current-sense resistance, inductor value, and battery voltage. When combined with the undervoltage protection circuit, this current-limit method is effective in almost every circumstance.

The positive valley current-limit threshold voltage at CSP to CSN equals precisely 1/10th the differential TIME to ILIM voltage over a 0.1V to 0.5V range (10mV to 50mV current-sense range). Connect ILIM directly to V_{CC} to set the default current-limit threshold setting of 22.5mV (typ).

The negative current-limit threshold (forced-PWM mode only) is nominally -125% of the corresponding valley current-limit threshold. When the inductor current drops below the negative current limit, the controller immediately activates an on-time pulse—DL turns off, and DH turns on—allowing the inductor current to remain above the negative current threshold.

Carefully observe the PCB layout guidelines to ensure that noise and DC errors do not corrupt the current-sense signals seen by the current-sense inputs (CSP_, CSN_).

Feedback Adjustment Amplifiers

Voltage-Positioning Amplifier (Steady-State Droop)

The MAX17410 include a transconductance amplifier for adding gain to the voltage-positioning sense path. The amplifier's input is generated by summing the current-sense inputs, which differentially sense the voltage across either current-sense resistors or the inductor's DCR. The amplifier's output connects directly to the regulator's voltage-positioned feedback input (FB), so the resistance between FB and the output-voltage sense point determines the voltage-positioning gain:

$$V_{OUT} = V_{TARGET} - R_{FB}I_{FB}$$

where the target voltage (V_{TARGET}) is defined in the *Nominal Output Voltage Selection* section, and the FB amplifier's output current (I_{FB}) is determined by the average value of the current-sense voltages:

$$I_{FB} = G_{m(FB)} \times V_{CSPAVG-CSN}$$

where $V_{CS} = V_{CSPAVG-CSN}$ is the average current-sense voltage between the CSPAVG and the CSN_ pins, and $G_{m(FB)}$ is typically 1.2mS as defined in the *Electrical Characteristics* table.

Differential Remote Sense

The MAX17410 includes differential, remote-sense inputs to eliminate the effects of voltage drops along the PCB traces and through the processor's power pins. The feedback-sense node connects to the voltage-positioning resistor (R_{FB}). The ground-sense (GNDS) input connects to an amplifier that adds an offset directly to the target voltage, effectively adjusting the output voltage to counteract the voltage drop in the ground path. Connect the voltage-positioning resistor (R_{FB}), and ground-sense (GNDS) input directly to the processor's remote-sense outputs as shown in Figure 1.

Integrator Amplifier

An integrator amplifier forces the DC average of the FB voltage to equal the target voltage. This transconductance amplifier integrates the feedback voltage and provides a fine adjustment to the regulation voltage (Figure 2), allowing accurate DC output-voltage regulation regardless of the output ripple voltage. The integrator amplifier has the ability to shift the output voltage by ±100mV (typ). The differential input voltage range is at least ±60mV total, including DC offset and AC ripple.

The MAX17410 disables the integrator by connecting the amplifier inputs together at the beginning of all VID transitions done in pulse-skipping mode (DPRSLPVR = high). The integrator remains disabled until 20µs after the transition is completed (the internal target settles) and the output is in regulation (edge detected on the error comparator).

Transient Overlap Operation

When a transient occurs, the response time of the controller depends on how quickly it can slew the inductor current. Multiphase controllers that remain 180° out-of-phase when a transient occurs actually respond slower than an equivalent single-phase controller. To provide fast transient response, the MAX17410 supports a phase overlap mode that allows the dual regulators to operate in-phase when heavy load transients are detected, effectively reducing the response time. After either high-side MOSFET turns off, if the output voltage does not exceed the regulation voltage when the minimum off-time expires, the controller simultaneously turns on both high-side MOSFETs during the next on-time cycle. This maximizes the total inductor current slew rate. The phases remain overlapped until the output voltage exceeds the regulation voltage after the minimum off-time expires.

After the phase overlap mode ends, the controller automatically begins with the opposite phase. For example, if the secondary phase provided the last on-time pulse before overlap operation began, the controller starts switching with the main phase when overlap operation ends.

Nominal Output Voltage Selection

The nominal no-load output voltage (V_{TARGET}) is defined by the selected voltage reference (VID DAC) plus the remote ground-sense adjustment (V_{GNDS}) as defined in the following equation:

$$V_{TARGET} = V_{FB} = V_{DAC} + V_{GNDS}$$

where V_{DAC} is the selected VID voltage. On startup, the MAX17410 slews the target voltage from ground to the preset boot voltage.

DAC Inputs (D0–D6)

The digital-to-analog converter (DAC) programs the output voltage using the D0–D6 inputs. D0–D6 are low-voltage (1.0V) logic inputs, designed to interface directly with the CPU. Do not leave D0–D6 unconnected. Changing D0–D6 initiates a transition to a new output voltage level. Change D0–D6 together, avoiding greater than 20ns skew between bits. Otherwise, incorrect DAC readings may cause a partial transition to the wrong voltage level followed by the intended transition to the correct voltage level, lengthening the overall transition time. The available DAC codes and resulting output voltages are compatible with the IMVP6/IMVP6+ (Table 4) specifications.

Suspend Mode

When the processor enters low-power deeper sleep mode, the IMVP6 CPU sets the VID DAC code to a lower output voltage and drives DPRSLPVR high. The MAX17410 responds by slewing the internal target voltage to the new DAC code, switching to single-phase operation, and letting the output voltage gradually drift down to the deeper sleep voltage. During the transition, the MAX17410 blanks both the upper and lower PWRGD and $\overline{CLKEN}$ thresholds until 20µs after the internal target reaches the deeper sleep voltage. Once the 20µs timer expires, the MAX17410 re-enables the lower PWRGD and $\overline{CLKEN}$ threshold, but keeps the upper threshold blanked. PHASEGD remains blanked high impedance while DPRSLPVR is high.

Table 3. Operating Mode Truth Table

INPUTS				PHASE OPERATION*	OPERATING MODE
$\overline{SHDN}$	$\overline{DPRSTP}$	DPRSLPVR	$\overline{PSI}$		
GND	X	X	X	DISABLED	Low-Power Shutdown Mode. DL1 and DL2 forced low, and the controller is disabled. The supply current drops to 1µA (max).
Rising	X	X	X	Multiphase Skipping 1/8 R_{TIME} Slew Rate	Startup/Boot. When $\overline{SHDN}$ is pulled high, the MAX17410 begins the startup sequence and ramps the output voltage up to the boot voltage. See Figure 9.

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Table 3. Operating Mode Truth Table (continued)

INPUTS				PHASE OPERATION*	OPERATING MODE
$\overline{SHDN}$	$\overline{DPRSTP}$	DPRSLPVR	$\overline{PSI}$		
High	X	Low	High	Multiphase Forced-PWM Nominal R_{TIME} Slew Rate	Full Power. The no-load output voltage is determined by the selected VID DAC code (D0–D6, Table 4).
High	X	Low	Low	1-Phase Forced-PWM Nominal R_{TIME} Slew Rate	Intermediate Power. The no-load output voltage is determined by the selected VID DAC code (D0–D6, Table 4). When $\overline{PSI}$ is pulled low, the MAX17410 immediately disables phase 2—DH2, and DL2 pulled low.
High	Low	High	X	1-Phase Pulse-Skipping Nominal R_{TIME} Slew Rate	Deeper Sleep Mode. The no-load output voltage is determined by the selected VID DAC code (D0–D6, Table 4). When DPRSLPVR is pulled high, the MAX17410 immediately enters 1-phase pulse-skipping operation allowing automatic PWM/PFM switchover under light loads. The PWRGD and $\overline{CLKEN}$ upper thresholds are blanked. DH2 and DL2 are pulled low.
High	High	High	X	1-Phase Pulse-Skipping 1/4th R_{TIME} Slew Rate	Deeper Sleep Slow Exit Mode. The no-load output voltage is determined by the selected VID DAC code (D0–D6, Table 4). When $\overline{DPRSTP}$ is pulled high while DPRSLPVR is already high, the MAX17410 remains in 1-phase pulse-skipping operation allowing automatic PWM/PFM switchover under light loads. The PWRGD and $\overline{CLKEN}$ upper thresholds are blanked. DH2 and DL2 are pulled low.
Falling	X	X	X	Multiphase Forced-PWM 1/8th R_{TIME} Slew Rate	Shutdown. When $\overline{SHDN}$ is pulled low, the MAX17410 immediately pulls PWRGD and PHASEGD low, $\overline{CLKEN}$ becomes high impedance, all enabled phases are activated, and the output voltage is ramped down to ground. Once the output reaches 0V, the controller enters the low-power shutdown state. See Figure 9.
High	X	X	X	DISABLED	Fault Mode. The fault latch has been set by the MAX17410 UVP or thermal-shutdown protection, or by the OVP protection. The controller will remain in FAULT mode until V_{CC} power is cycled or $\overline{SHDN}$ toggled.

**Multiphase Operation = All enabled phases active.*
X = Don't care.

Table 4. IMVP6+ Output Voltage VID DAC Codes

D6	D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE (V)
0	0	0	0	0	0	0	1.5000
0	0	0	0	0	0	1	1.4875
0	0	0	0	0	1	0	1.4750
0	0	0	0	0	1	1	1.4625
0	0	0	0	1	0	0	1.4500
0	0	0	0	1	0	1	1.4375
0	0	0	0	1	1	0	1.4250
0	0	0	0	1	1	1	1.4125
0	0	0	1	0	0	0	1.4000
0	0	0	1	0	0	1	1.3875
0	0	0	1	0	1	0	1.3750
0	0	0	1	0	1	1	1.3625

Table 4. IMVP6+ Output Voltage VID DAC Codes (continued)

D6	D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE (V)
0	0	0	1	1	0	0	1.3500
0	0	0	1	1	0	1	1.3375
0	0	0	1	1	1	0	1.3250
0	0	0	1	1	1	1	1.3125
0	0	1	0	0	0	0	1.3000
0	0	1	0	0	0	1	1.2875
0	0	1	0	0	1	0	1.2750
0	0	1	0	0	1	1	1.2625
0	0	1	0	1	0	0	1.2500
0	0	1	0	1	0	1	1.2375
0	0	1	0	1	1	0	1.2250
0	0	1	0	1	1	1	1.2125
0	0	1	1	0	0	0	1.2000
0	0	1	1	0	0	1	1.1875
0	0	1	1	0	1	0	1.1750
0	0	1	1	0	1	1	1.1625
0	0	1	1	1	0	0	1.1500
0	0	1	1	1	0	1	1.1375
0	0	1	1	1	1	0	1.1250
0	0	1	1	1	1	1	1.1125
0	1	0	0	0	0	0	1.1000
0	1	0	0	0	0	1	1.0875
0	1	0	0	0	1	0	1.0750
0	1	0	0	0	1	1	1.0625
0	1	0	0	1	0	0	1.0500
0	1	0	0	1	0	1	1.0375
0	1	0	0	1	1	0	1.0250
0	1	0	0	1	1	1	1.0125
0	1	0	1	0	0	0	1.0000
0	1	0	1	0	0	1	0.9875
0	1	0	1	0	1	0	0.9750
0	1	0	1	0	1	1	0.9625
0	1	0	1	1	0	0	0.9500
0	1	0	1	1	0	1	0.9375
0	1	0	1	1	1	0	0.9250
0	1	0	1	1	1	1	0.9125
0	1	1	0	0	0	0	0.9000
0	1	1	0	0	0	1	0.8875
0	1	1	0	0	1	0	0.8750
0	1	1	0	0	1	1	0.8625
0	1	1	0	1	0	0	0.8500
0	1	1	0	1	0	1	0.8375
0	1	1	0	1	1	0	0.8250
0	1	1	0	1	1	1	0.8125
0	1	1	1	0	0	0	0.8000
0	1	1	1	0	0	1	0.7875
0	1	1	1	0	1	0	0.7750
0	1	1	1	0	1	1	0.7625
0	1	1	1	1	0	0	0.7500
0	1	1	1	1	0	1	0.7375
0	1	1	1	1	1	0	0.7250
0	1	1	1	1	1	1	0.7125
1	0	0	0	0	0	0	0.7000
1	0	0	0	0	0	1	0.6875
1	0	0	0	0	1	0	0.6750
1	0	0	0	0	1	1	0.6625
1	0	0	0	1	0	0	0.6500
1	0	0	0	1	0	1	0.6375
1	0	0	0	1	1	0	0.6250
1	0	0	0	1	1	1	0.6125
1	0	0	1	0	0	0	0.6000
1	0	0	1	0	0	1	0.5875
1	0	0	1	0	1	0	0.5750
1	0	0	1	0	1	1	0.5625
1	0	0	1	1	0	0	0.5500
1	0	0	1	1	0	1	0.5375
1	0	0	1	1	1	0	0.5250
1	0	0	1	1	1	1	0.5125
1	0	1	0	0	0	0	0.5000
1	0	1	0	0	0	1	0.4875
1	0	1	0	0	1	0	0.4750
1	0	1	0	0	1	1	0.4625
1	0	1	0	1	0	0	0.4500
1	0	1	0	1	0	1	0.4375
1	0	1	0	1	1	0	0.4250
1	0	1	0	1	1	1	0.4125
1	0	1	1	0	0	0	0.4000
1	0	1	1	0	0	1	0.3875

Table 4. IMVP6+ Output Voltage VID DAC Codes (continued)

D6	D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE (V)
1	0	1	1	0	1	0	0.3750
1	0	1	1	0	1	1	0.3625
1	0	1	1	1	0	0	0.3500
1	0	1	1	1	0	1	0.3375
1	0	1	1	1	1	0	0.3250
1	0	1	1	1	1	1	0.3125
1	1	0	0	0	0	0	0.3000
1	1	0	0	0	0	1	0.2875
1	1	0	0	0	1	0	0.2750
1	1	0	0	0	1	1	0.2625
1	1	0	0	1	0	0	0.2500
1	1	0	0	1	0	1	0.2375
1	1	0	0	1	1	0	0.2250
1	1	0	0	1	1	1	0.2125
1	1	0	1	0	0	0	0.2000
1	1	0	1	0	0	1	0.1875
1	1	0	1	0	1	0	0.1750
1	1	0	1	0	1	1	0.1625
1	1	0	1	1	0	0	0.1500
1	1	0	1	1	0	1	0.1375
1	1	0	1	1	1	0	0.1250
1	1	0	1	1	1	1	0.1125
1	1	1	0	0	0	0	0.1000
1	1	1	0	0	0	1	0.0875
1	1	1	0	0	1	0	0.0750
1	1	1	0	0	1	1	0.0625
1	1	1	0	1	0	0	0.0500
1	1	1	0	1	0	1	0.0375
1	1	1	0	1	1	0	0.0250
1	1	1	0	1	1	1	0.0125
1	1	1	1	0	0	0	0
1	1	1	1	0	0	1	0
1	1	1	1	0	1	0	0
1	1	1	1	0	1	1	0
1	1	1	1	1	0	0	0
1	1	1	1	1	0	1	0
1	1	1	1	1	1	0	0
1	1	1	1	1	1	1	0

Output-Voltage Transition Timing

The MAX17410 performs mode transitions in a controlled manner, automatically minimizing input surge currents. This feature allows the circuit designer to achieve nearly ideal transitions, guaranteeing just-in-time arrival at the new output voltage level with the lowest possible peak currents for a given output capacitance.

At the beginning of an output voltage transition, the MAX17410 blanks both PWRGD thresholds, preventing the PWRGD open-drain output from changing states during the transition. The controller enables the lower PWRGD threshold approximately 20µs after the slew-rate controller reaches the target output voltage, but the upper PWRGD threshold is enabled only if the controller remains in forced-PWM operation. If the controller enters pulse-skipping operation, the upper PWRGD threshold remains blanked. The slew rate (set by resistor R_{TIME}) must be set fast enough to ensure that the transition may be completed within the maximum allotted time.

The MAX17410 automatically controls the current to the minimum level required to complete the transition in the calculated time. The slew-rate controller uses an internal capacitor and current-source programmed by R_{TIME} to transition the output voltage. The total transition time depends on R_{TIME}, the voltage difference, and the accuracy of the slew-rate controller (C_{SLEW} accuracy). The slew rate is not dependent on the total output capacitance, as long as the surge current is less than the current limit. For all dynamic VID transitions, the transition time (t_{TRAN}) is given by:

$$t_{TRAN} = \frac{|V_{NEW} - V_{OLD}|}{(dV_{TARGET}/dt)}$$

where $dV_{TARGET}/dt = 12.5mV/\mu s \times 71.5k\Omega/R_{TIME}$ is the slew rate, V_{OLD} is the original output voltage, and V_{NEW} is the new target voltage. See the time slew-rate accuracy in the *Electrical Characteristics* table for slew-rate limits. For soft-start and shutdown, the controller automatically reduces the slew rate to 1/8th.

The output voltage tracks the slewed target voltage, making the transitions relatively smooth. The average inductor current per phase required to make an output voltage transition is:

$$I_L \cong \frac{C_{OUT}}{\eta_{TOTAL}} \times \left(dV_{TARGET}/dt\right)$$

where dV_{TARGET}/dt is the required slew rate, C_{OUT} is the total output capacitance, and η_{TOTAL} is the number of active phases.

Deeper Sleep Transitions

When DPRSLPVR goes high, the MAX17410 immediately disables phase 2 (DH2 and DL2 forced low), blanks PHASEGD high impedance, and enters pulse-skipping operation (see Figures 4 and 5). If the VIDs are set to a lower voltage setting, the output drops at a rate determined by the load and the output capacitance. The internal target still ramps as before, and PWRGD remains blanked high impedance until 20µs after the output voltage reaches the internal target. Once this time expires, PWRGD monitors only the lower threshold.

Fast C4E Deeper Sleep Exit: When exiting deeper sleep (DPRSLPVR pulled low) while the output voltage still exceeds the deeper sleep voltage, the MAX17410 quickly slews (50mV/µs min regardless of R_{TIME} setting) the internal target voltage to the DAC code provided by the processor as long as the output voltage is above the new target. The controller remains in skip mode until the output voltage equals the internal target. Once the internal target reaches the output voltage, phase 2 is enabled. The controller blanks PWRGD, PHASEGD, and $\overline{CLKEN}$ (forced high impedance) until 20µs after the transition is completed. See Figure 4.

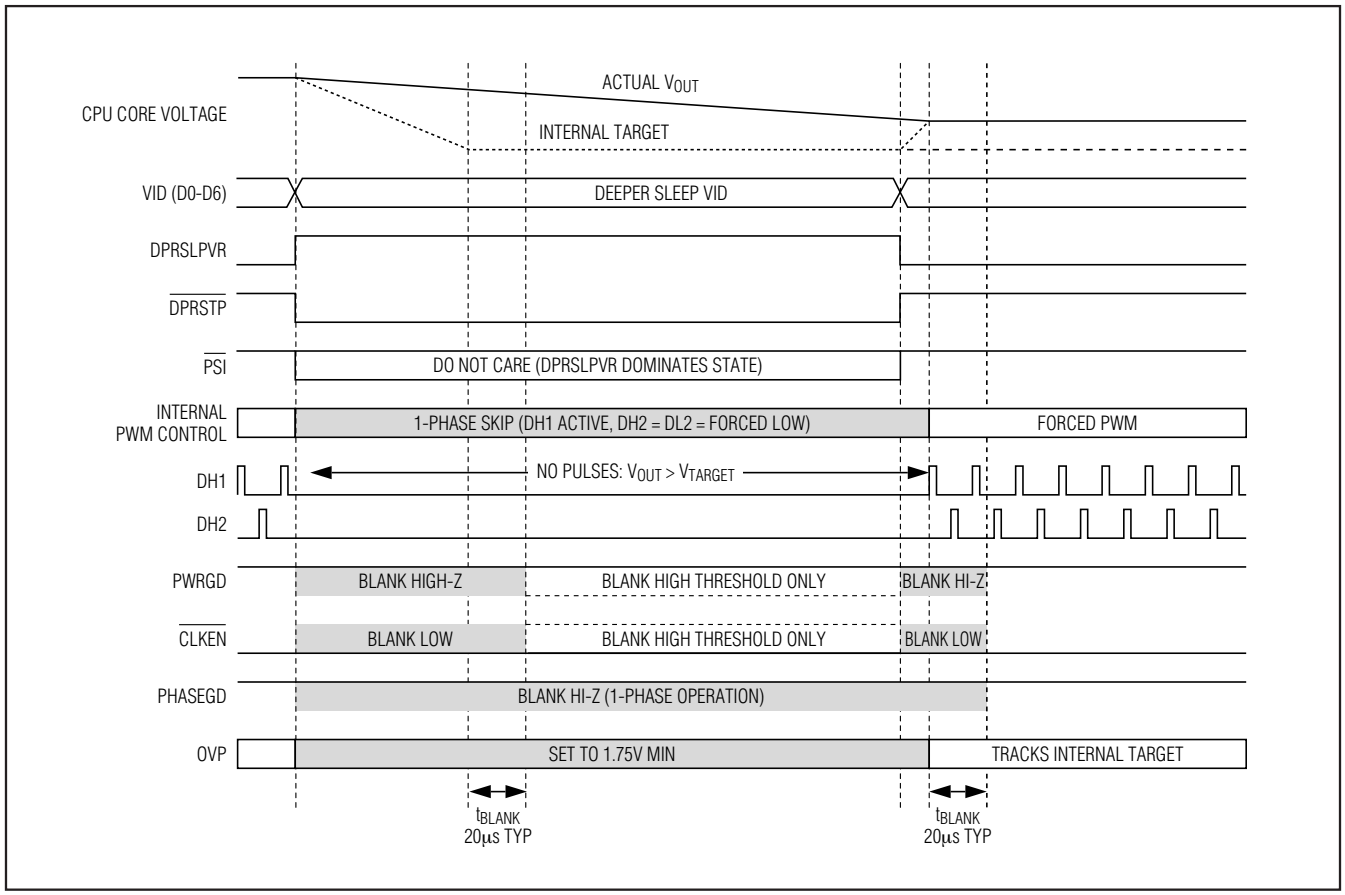

Figure 4. C4E (C4 Early Exit) Transition

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Standard C4 Deeper Sleep Exit: When exiting deeper sleep (DPRSLPVR pulled low) while the output voltage is regulating to the deeper sleep voltage, the MAX17410 immediately activates all enabled phases and ramps the output voltage to the LFM DAC code provided by the processor at the slew rate set by R_{TIME}. The controller blanks PWRGD, PHASEGD, and $\overline{CLKEN}$ (forced high impedance) until 20µs after the transition is completed. See Figure 5.

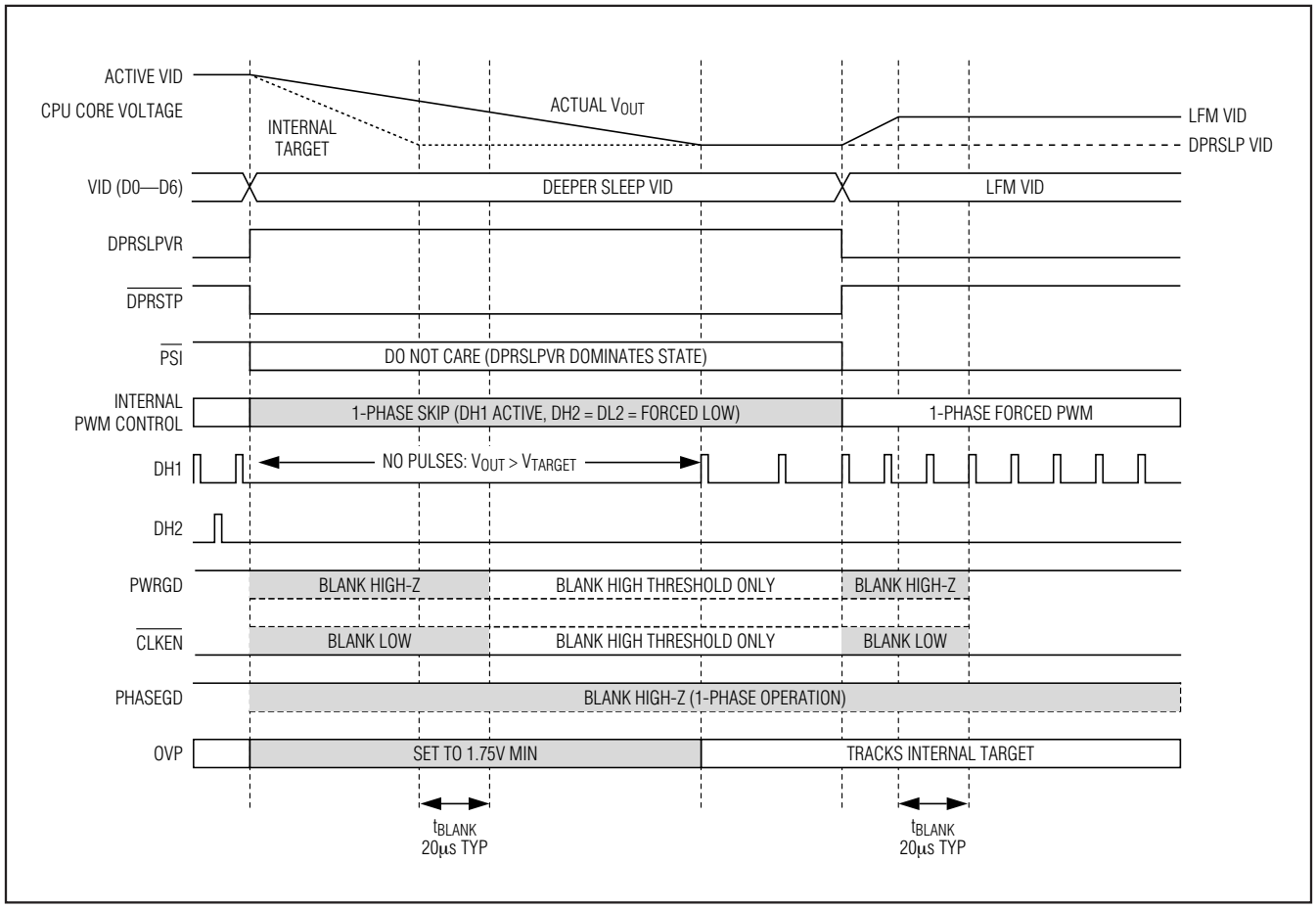

Figure 5. Standard C4 Transition

Slow C4 Deeper Sleep Exit: When exiting deeper sleep (DPRSLPVR high, $\overline{DPRSTP}$ pulled high) while the output voltage is regulating to the deeper sleep voltage, the MAX17410 remains in 1-phase skip mode and ramps the output voltage to the LFM DAC code provided by the processor at 1/4 the slew rate set by R_{TIME}. The controller blanks PWRGD, PHASEGD, and $\overline{CLKEN}$ (forced high impedance) until 20µs after the transition is completed. See Figure 6.

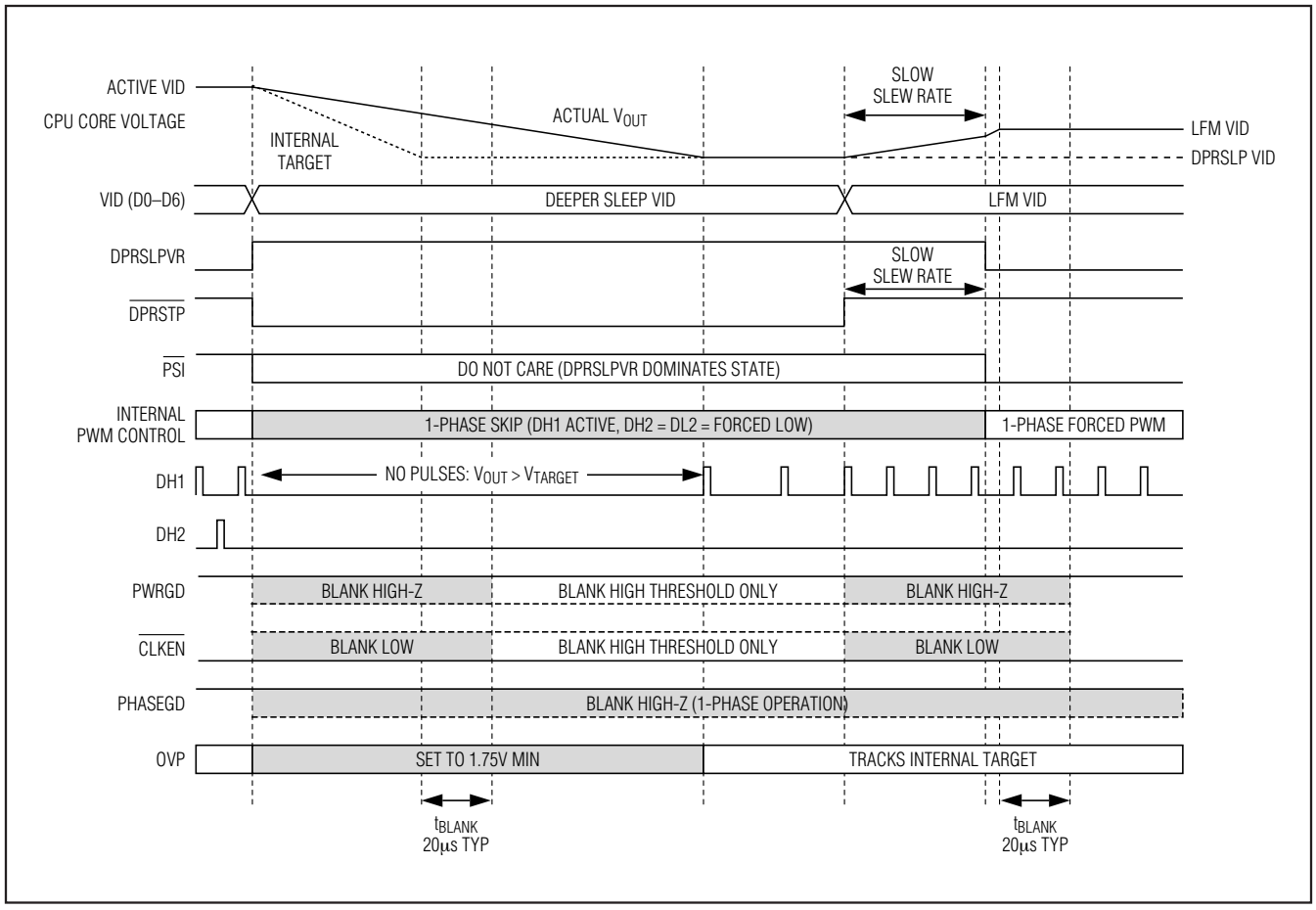

Figure 6. Slow C4 Transition

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$\overline{PSI}$ Transitions

When $\overline{PSI}$ is pulled low, the MAX17410 immediately disables phase 2 (DH2 and DL2 forced low), blanks PHASEGD high impedance, and enters single-phase PWM operation (see Figure 7). When $\overline{PSI}$ is pulled high, the MAX17410 enables phase 2. PHASEGD is blanked high impedance for 32 switching cycles on DH2, allowing sufficient time/cycles for phase 1 and 2 to achieve current balance. In a typical IMVP-6 application, the VID is reduced by 1 LSB (12.5mV) when $\overline{PSI}$ is pulled low, and increased by 1 LSB when $\overline{PSI}$ is pulled high.

Forced-PWM Operation (Normal Mode)

During soft-start, soft-shutdown, and normal operation—when the CPU is actively running (DPRSLPVR = low, Table 5)—the MAX17410 operates with the low-noise, forced-PWM control scheme. Forced-PWM operation disables the zero-crossing comparators of all active phases, forcing the low-side gate-drive waveforms to constantly be the complement of the high-side gate-drive waveforms. This keeps the switching frequency constant and allows the inductor current to reverse under light loads, providing fast, accurate negative output voltage transitions by quickly discharging the output capacitors.

Forced-PWM operation comes at a cost: the no-load +5V bias supply current remains between 10mA to 50mA per phase, depending on the external MOSFETs and switching frequency. To maintain high efficiency under light load conditions, the processor may switch the controller to a low-power pulse-skipping control scheme after entering suspend mode.

$\overline{PSI}$ determines how many phases are active when operating in forced-PWM mode (DPRSLPVR = low). When $\overline{PSI}$ is pulled low, the main phase remains active but the secondary phase is disabled (DH2 and DL2 forced low).

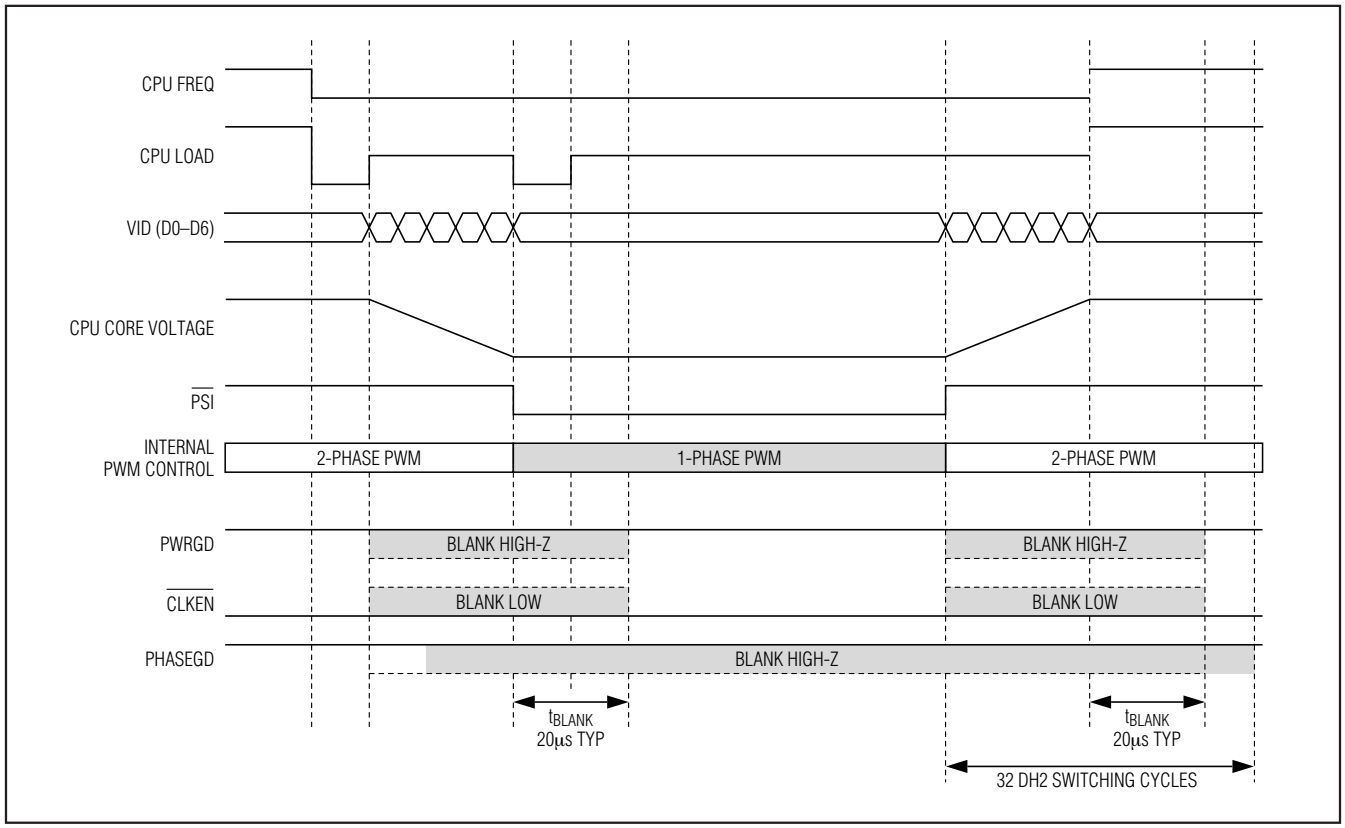

Figure 7. $\overline{PSI}$ Transition

Light-Load Pulse-Skipping Operation (Deeper Sleep)

When DPRSLPVR is pulled high, the MAX17410 operates with a single-phase pulse-skipping mode. The pulse-skipping mode enables the driver's zero-crossing comparator, so the controller pulls DL1 low when its current-sense inputs detect "zero" inductor current. This keeps the inductor from discharging the output capacitors and forces the controller to skip pulses under light load conditions to avoid overcharging the output.

When pulse-skipping, the controller blanks the upper PWRGD and $\overline{CLKEN}$ thresholds, and also blanks PHASEGD high impedance. Upon entering pulse-skipping operation, the controller temporarily sets the OVP threshold to 1.80V, preventing false OVP faults when the transition to pulse-skipping operation coincides with a VID code change. Once the error amplifier detects that the output voltage is in regulation, the OVP threshold tracks the selected VID DAC code. The MAX17410 automatically uses forced-PWM operation during soft-start and soft-shutdown, regardless of the DPRSLPVR and $\overline{PSI}$ configuration.

Automatic Pulse-Skipping Switchover

In skip mode (DPRSLPVR = high), an inherent automatic switchover to PFM takes place at light loads (Figure 8). This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. The zero-crossing comparator senses the inductor current across the low-side MOSFETs. Once V_{LX} drops below the zero-crossing comparator threshold (see the *Electrical Characteristics* table), the comparator forces DL low (Figure 2). This mechanism causes the threshold between pulse-skipping PFM and non-skipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation. The PFM/PWM crossover occurs when the load current of each phase is equal to 1/2 the peak-to-peak ripple current, which is a function of the inductor value (Figure 8). For a battery input range of 7V to 20V, this threshold is relatively constant, with only a minor dependence on the input voltage due to the typically low duty cycles. The total load current at the PFM/PWM crossover threshold ($I_{LOAD(SKIP)}$) is approximately:

$$I_{LOAD(SKIP)} = \eta_{TOTAL}\left(\frac{t_{SW}V_{OUT}}{L}\right)\left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right)$$

where η_{TOTAL} is the number of active phases.

The switching waveforms may appear noisy and asynchronous when light loading activates pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs between PFM noise and light-load efficiency are made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load-transient response, especially at low input voltage levels.

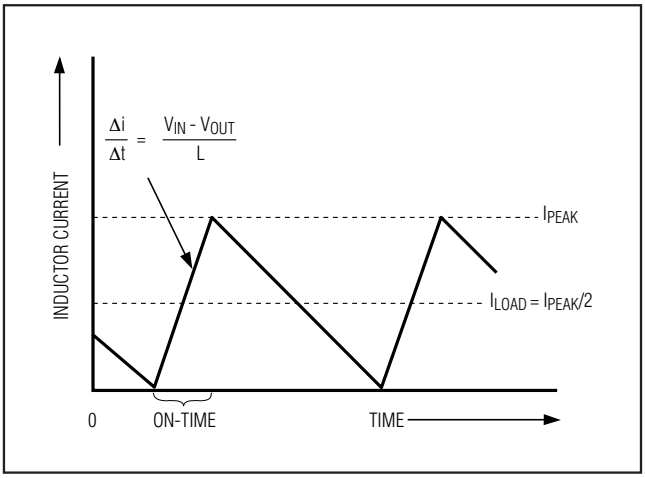

Figure 8. Pulse-Skipping/Discontinuous Crossover Point

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Power-Up Sequence (POR, UVLO)

The MAX17410 is enabled when $\overline{SHDN}$ is driven high (Figure 9). The reference powers up first. Once the reference exceeds its undervoltage lockout threshold, the internal analog blocks are turned on and masked by a 150µs one-shot delay. The PWM controller then begins switching.

Power-on reset (POR) occurs when V_{CC} rises above approximately 2V, resetting the fault latch and preparing the controller for operation. The V_{CC} undervoltage lockout (UVLO) circuitry inhibits switching until V_{CC} rises above 4.25V. The controller powers up the reference once the system enables the controller, V_{CC} above 4.25V and $\overline{SHDN}$ driven high. With the reference in regulation, the controller ramps the output voltage to the boot voltage (1.2V) at 1/8th the slew rate set by R_{TIME}:

$$t_{TRAN(START)} = \frac{8V_{BOOT}}{(dV_{TARGET}/dt)}$$

where dV_{TARGET}/dt = 12.5mV/µs x 71.5kΩ/R_{TIME} is the slew rate. The soft-start circuitry does not use a variable current limit, so full output current is available immediately. $\overline{CLKEN}$ is pulled low approximately 60µs after the MAX17410 reaches the boot voltage. At the same time, the MAX17410 slews the output to the voltage set at the VID inputs at the programmed slew rate. PWRGD and PHASEGD becomes high impedance approximately 5ms after $\overline{CLKEN}$ is pulled low. The MAX17410 automatically uses forced-PWM operation during soft-start and soft-shutdown, regardless of the DPRSLPVR and $\overline{PSI}$ configuration.

For automatic startup, the battery voltage should be present before V_{CC}. If the controller attempts to bring the output into regulation without the battery voltage present, the fault latch trips. The controller remains shut down until the fault latch is cleared by toggling $\overline{SHDN}$ or cycling the V_{CC} power supply below 0.5V.

If the V_{CC} voltage drops below 4.25V, the controller assumes that there is not enough supply voltage to make valid decisions. To protect the output from overvoltage faults, the controller shuts down immediately and forces a high-impedance output.

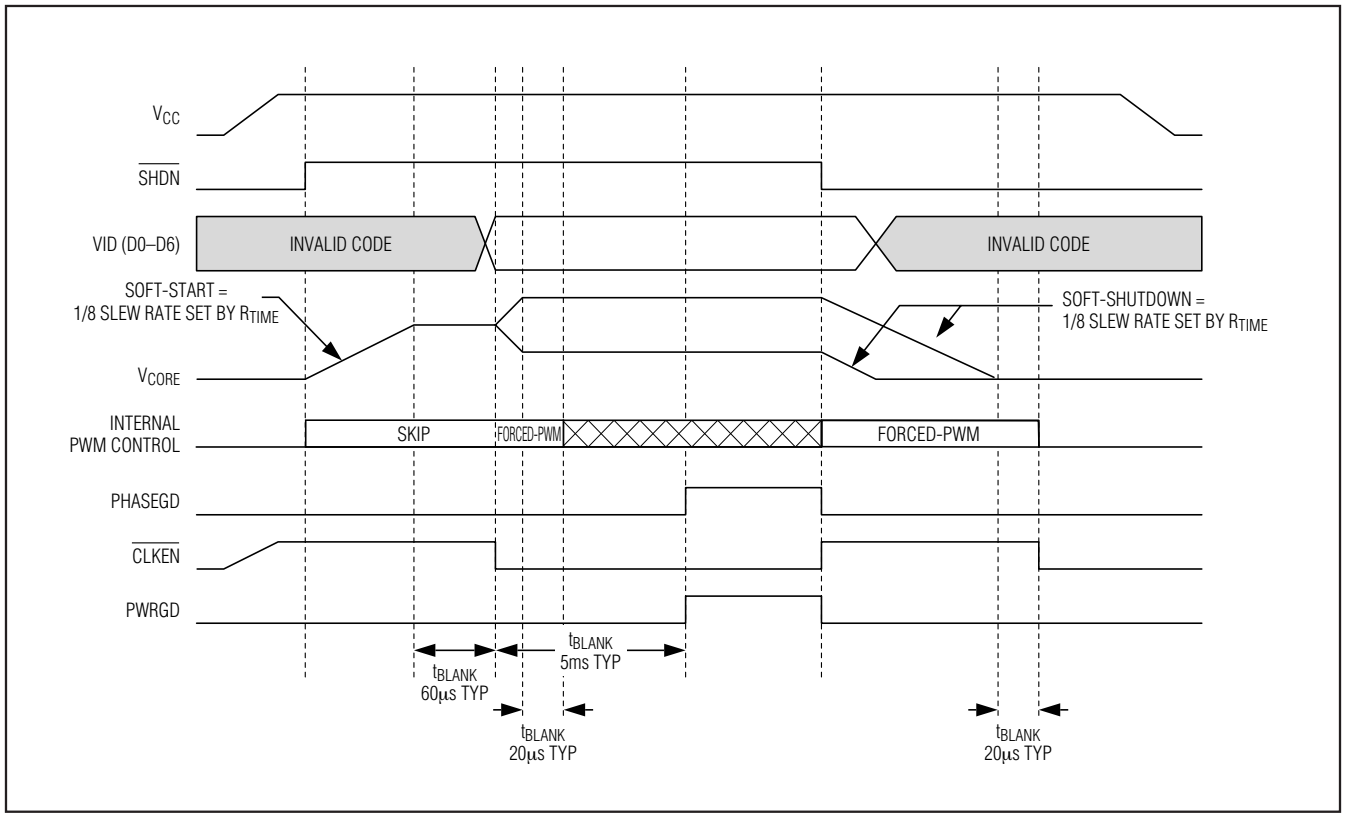

Figure 9. Power-Up and Shutdown Sequence Timing Diagram

Shutdown

When $\overline{SHDN}$ goes low, the MAX17410 enters low-power shutdown mode. PWRGD is pulled low immediately, and the output voltage ramps down at 1/8th the slew rate set by R_{TIME}:

$$t_{TRAN(SHDN)} = \frac{8V_{OUT}}{(dV_{TARGET}/dt)}$$

where dV_{TARGET}/dt = 12.5mV/µs x 71.5kΩ/R_{TIME} is the slew rate. Slowly discharging the output capacitors by slewing the output over a long period of time keeps the average negative inductor current low (damped response), thereby eliminating the negative output-voltage excursion that occurs when the controller discharges the output quickly by permanently turning on the low-side MOSFET (underdamped response). This eliminates the need for the Schottky diode normally connected between the output and ground to clamp the negative output-voltage excursion. After the controller reaches the zero target, the MAX17410 shuts down completely—the drivers are disabled (DL1 and DL2 driven high), the reference turns off, and the supply current drops below 1µA.

When a fault condition—output UVLO or thermal shutdown—activates the shutdown sequence, the protection circuitry sets the fault latch to prevent the controller from restarting. To clear the fault latch and reactivate the controller, toggle $\overline{SHDN}$ or cycle V_{CC} power below 0.5V.

Power Monitor (PMON)

The MAX17410 include a single-quadrant multiplier used to determine the actual output power based on the inductor current (the differential CS input) and output voltage (CSN to GNDS). The buffered output of this multiplier is connected to PWR and provides a voltage relative to the output power dissipation:

V(PMON) = Kpwr x V(OUTS, GNDS) x V(CSPAVG, CSN) / V(TIME, ILIM)

where V_{CSP} - V_{CSN} = I_{LOAD} x R_{SENSE}, and the power monitor scale factor (Kpwr) is typically 21.25. If ILIM is externally connected to a 5V rail to enable the internal default/preset current-limit threshold, then the V(TIME, ILIM) value to be used in the above equation is 225mV. Do not use the power monitor in any configuration that would cause its output V(PMON) to exceed (V_{CC} - 0.5V).

PMON is pulled to ground when the MAX17410 is in shutdown.

The power monitor allows the system to accurately monitor the CPU's power dissipation and quickly predict if the system is about to overheat before the significantly slower temperature sensor signals an overtemperature alert.

Phase Fault (PHASEGD)

The MAX17410 includes a phase fault output that signals the system that one of the two phases either has a fault condition or is not matched with the other. Detection is done by identifying the need for a large on-time difference between phases to achieve or move towards current balance. PHASEGD is forced low when V_{CCI} is below (0.6 x V_{FB}) or above (1.4 x V_{FB}).

PHASEGD is high impedance when the controller operates in one-phase mode (DPRSLPVR high, or $\overline{PSI}$ low and DPRSLPVR low). On exit to two-phase mode, PHASEGD is forced high impedance for 32 switching cycles on DH2.

PHASEGD is low in shutdown. PHASEGD is forced high impedance whenever the slew-rate controller is active (output voltage transitions).

Temperature Comparator ($\overline{VRHOT}$)

$\overline{VRHOT}$ is an open-drain output of the internal comparator. $\overline{VRHOT}$ is pulled low when the voltage at NTC goes below the voltage at THRM. $\overline{VRHOT}$ is high impedance in shutdown.

Fault Protection (Latched)

Output Overvoltage Protection

The overvoltage protection (OVP) circuit is designed to protect the CPU against a shorted high-side MOSFET by drawing high current and blowing the battery fuse. The MAX17410 continuously monitors the output for an overvoltage fault. The controller detects an OVP fault if the output voltage exceeds the set VID DAC voltage by more than 300mV, regardless of the operating state. During pulse-skipping operation (DPRSLPVR = high), the OVP threshold tracks the VID DAC voltage.

When the OVP circuit detects an overvoltage fault while in multiphase mode (DPRSLPVR = low, $\overline{PSI}$ = high), the MAX17410 immediately forces DL1 and DL2 high, pulls DH1 and DH2 low. This action turns on the synchronous-rectifier MOSFETs with 100% duty and, in turn, rapidly discharges the output filter capacitor and forces the output low. If the condition that caused the overvoltage (such as a shorted high-side MOSFET) persists, the battery fuse will blow. Toggle $\overline{SHDN}$ or cycle the V_{CC} power supply below 0.5V to clear the fault latch and reactivate the controller.

When an overvoltage fault occurs while in one-phase operation (DPRSLPVR = high, or $\overline{PSI}$ = low), the MAX17410 immediately forces DL1 high, pulls DH1 low. DL2 and DH2 remain low as phase two was disabled. DL2 is forced high only when the output falls below the UV threshold.

Overvoltage protection can be disabled through the no-fault test mode (see the *No-Fault Test Mode* section).

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Output Undervoltage Protection

The output UVP function is similar to foldback current limiting, but employs a timer rather than a variable current limit. If the MAX17410 output voltage is 400mV below the target voltage, the controller activates the shutdown sequence and sets the fault latch. Once the controller ramps down to zero, it forces DL1 and DL2 high, and pulls DH1 and DH2 low. Toggle $\overline{SHDN}$ or cycle the V_{CC} power supply below 0.5V to clear the fault latch and reactivate the controller.

UVP can be disabled through the no-fault test mode (see the *No-Fault Test Mode* section).

Thermal-Fault Protection

The MAX17410 features a thermal fault-protection circuit. When the junction temperature rises above +160°C, a thermal sensor sets the fault latch and activates the soft-shutdown sequence. Once the controller ramps down to zero, it forces DL1 and DL2 high, and pulls DH1 and DH2 low. Toggle $\overline{SHDN}$ or cycle the V_{CC} power supply below 0.5V to clear the fault latch and reactivate the controller after the junction temperature cools by 15°C.

Thermal shutdown can be disabled through the no-fault test mode (see the *No-Fault Test Mode* section).

No-Fault Test Mode

The latched fault-protection features can complicate the process of debugging prototype breadboards since there are (at most) a few milliseconds in which to determine what went wrong. Therefore, a "no-fault" test mode is provided to disable the fault protection—overvoltage protection, undervoltage protection, and thermal shutdown. Additionally, the test mode clears the fault latch if it has been set. The no-fault test mode is entered by forcing 11V to 13V on $\overline{SHDN}$.

MOSFET Gate Drivers

The DH and DL drivers are optimized for driving moderate-sized high-side and larger low-side power MOSFETs. This is consistent with the low duty factor seen in notebook applications, where a large V_{IN} - V_{OUT} differential exists. The high-side gate drivers (DH) source and sink 2.2A, and the low-side gate drivers (DL) source 2.7A and sink 8A. This ensures robust gate drive for high-current applications. The DH_ floating high-side MOSFET drivers are powered by internal boost switch charge pumps at BST_, while the DL_ synchronous-rectifier drivers are powered directly by the 5V bias supply (V_{DD}).

Adaptive dead-time circuits monitor the DL and DH drivers and prevent either FET from turning on until the other is fully off. The adaptive driver dead time allows operation without shoot-through with a wide range of MOSFETs, minimizing delays and maintaining efficiency.

There must be a low-resistance, low-inductance path from the DL and DH drivers to the MOSFET gates for the adaptive dead-time circuits to work properly; otherwise, the sense circuitry in the MAX17410 interprets the MOSFET gates as "off" while charge actually remains. Use very short, wide traces (50 mils to 100 mils wide if the MOSFET is 1in from the driver).

The internal pulldown transistor that drives DL low is robust, with a 0.25Ω (typ) on-resistance. This helps prevent DL from being pulled up due to capacitive coupling from the drain to the gate of the low-side MOSFETs when the inductor node (LX) quickly switches from ground to V_{IN}. Applications with high input voltages and long inductive driver traces may require rising LX edges do not pull up the low-side MOSFETs' gate, causing shoot-through currents. The capacitive coupling between LX and DL created by the MOSFET's gate-to-drain capacitance (C_{RSS}), gate-to-source capacitance (C_{ISS} - C_{RSS}), and additional board parasitics should not exceed the following minimum threshold:

$$V_{GS(TH)} > V_{IN}\left(\frac{C_{RSS}}{C_{ISS}}\right)$$

Typically, adding a 4700pF between DL and power ground (C_{NL} in Figure 10), close to the low-side MOSFETs, greatly reduces coupling. Do not exceed 22nF of total gate capacitance to prevent excessive turn-off delays.

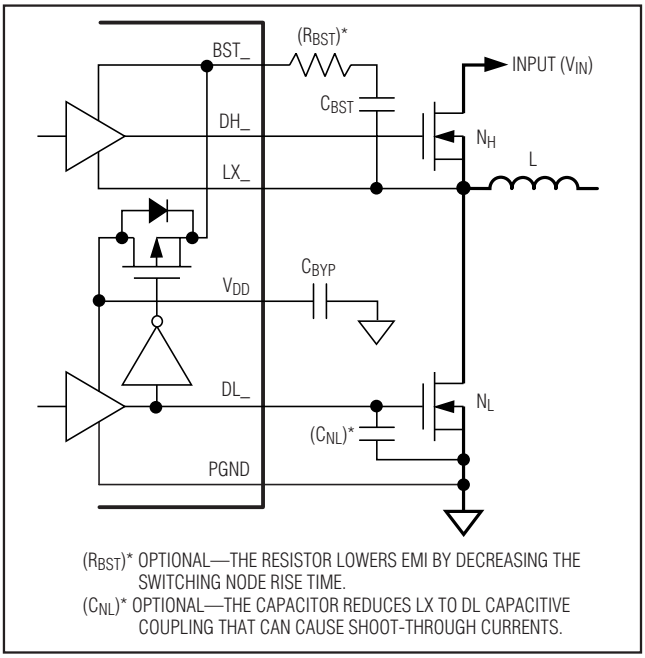

Figure 10. Gate-Drive Circuit

Alternatively, shoot-through currents may be caused by a combination of fast high-side MOSFETs and slow low-side MOSFETs. If the turn-off delay time of the low-side MOSFET is too long, the high-side MOSFETs can turn on before the low-side MOSFETs have actually turned off. Adding a resistor less than 5Ω in series with BST slows down the high-side MOSFET turn-on time, eliminating the shoot-through currents without degrading the turn-off time (R_{BST} in Figure 10). Slowing down the high-side MOSFET also reduces the LX node rise time, thereby reducing EMI and high-frequency coupling responsible for switching noise.

Multiphase Quick-PWM Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

- **Input Voltage Range:** The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case high AC adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest input voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.
- **Maximum Load Current:** There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements, and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components. Modern notebook CPUs generally exhibit $I_{LOAD} = I_{LOAD(MAX)}$ x 80%.

For multiphase systems, each phase supports a fraction of the load, depending on the current balancing. When properly balanced, the load current is evenly distributed among each phase:

$$I_{LOAD(PHASE)} = \frac{I_{LOAD}}{\eta_{TOTAL}}$$

where η_{TOTAL} is the total number of active phases.

- **Switching Frequency:** This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage, due to MOSFET switching losses that are proportional to frequency and V_{IN}^2. The optimum frequency is also a moving target, due to rapid improvements in MOSFET technology that are making higher frequencies more practical.
- **Inductor Operating Point:** This choice provides trade-offs between size vs. efficiency and transient response vs. output noise. Low inductor values provide better transient response and smaller physical size, but also result in lower efficiency and higher output noise due to increased ripple current. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 20% and 50% ripple current.

Inductor Selection

The switching frequency and operating point (% ripple current or LIR) determine the inductor value as follows:

$$L = \eta_{TOTAL}\left(\frac{V_{IN} - V_{OUT}}{f_{SW} I_{LOAD(MAX)} LIR}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)$$

where η_{TOTAL} is the total number of phases.

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = \left(\frac{I_{LOAD(MAX)}}{\eta_{TOTAL}}\right)\left(1 + \frac{LIR}{2}\right)$$

Transient Response

The inductor ripple current impacts transient-response performance, especially at low V_{IN} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The amount of output sag is also a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time. For a dual-phase controller, the worst-case output sag voltage may be determined by:

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$$V_{SAG} = \frac{L\left(\Delta I_{LOAD(MAX)}\right)^2 \left[\left(\frac{V_{OUT}t_{SW}}{V_{IN}}\right) + t_{OFF(MIN)}\right]}{2C_{OUT}V_{OUT}\left[\left(\frac{\left(V_{IN} - 2V_{OUT}\right)t_{SW}}{V_{IN}}\right) - 2t_{OFF(MIN)}\right]} + \frac{\Delta I_{LOAD(MAX)}}{2C_{OUT}}\left[\left(\frac{V_{OUT}t_{SW}}{V_{IN}}\right) + t_{OFF(MIN)}\right]$$

where $t_{OFF(MIN)}$ is the minimum off-time (see the *Electrical Characteristics* table).

The amount of overshoot due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{\left(\Delta I_{LOAD(MAX)}\right)^2 L}{2\eta_{TOTAL}C_{OUT}V_{OUT}}$$

where η_{TOTAL} is the total number of active phases.

Setting the Current Limit

The minimum current-limit threshold must be high enough to support the maximum load current when the current limit is at the minimum tolerance value. The valley of the inductor current occurs at $I_{LOAD(MAX)}$ minus half the ripple current; therefore:

$$I_{LIMIT(LOW)} > \left(\frac{I_{LOAD(MAX)}}{\eta_{TOTAL}}\right)\left(1 - \frac{LIR}{2}\right)$$

where η_{TOTAL} is the total number of active phases, and $I_{LIMIT(LOW)}$ equals the minimum current-limit threshold voltage divided by the current-sense resistor (R_{SENSE}). For the 22.5mV default setting, the minimum current-limit threshold is 19.5mV.

Output Capacitor Selection

The output filter capacitor must have low enough effective series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements.

In CPU V_{CORE} converters and other applications where the output is subject to large load transients, the output capacitor's size typically depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$\left(R_{ESR} + R_{PCB}\right) \le \frac{V_{STEP}}{\Delta I_{LOAD(MAX)}}$$

In non-CPU applications, the output capacitor's size often depends on how much ESR is needed to maintain an acceptable level of output-ripple voltage. The output-ripple voltage of a step-down controller equals the total inductor ripple current multiplied by the output capacitor's ESR. When operating multiphase systems out-of-phase, the peak inductor currents of each phase are staggered, resulting in lower output ripple voltage by reducing the total inductor ripple current. For multiphase operation, the maximum ESR to meet ripple requirements is:

$$R_{ESR} \le \left[\frac{V_{IN}f_{SW}L}{\left(V_{IN} - \eta_{TOTAL}V_{OUT}\right)V_{OUT}}\right]V_{RIPPLE}$$

where η_{TOTAL} is the total number of active phases and f_{SW} is the switching frequency per phase. The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of polymer types).

When using low-capacity ceramic filter capacitors, capacitor size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the V_{SAG} and V_{SOAR} equations in the *Transient Response* section).

Output Capacitor Stability Considerations

For Quick-PWM controllers, stability is determined by the value of the ESR zero relative to the switching frequency. The boundary of instability is given by the following equation:

$$f_{ESR} \le \frac{f_{SW}}{\pi}$$

where:

$$f_{ESR} = \frac{1}{2\pi R_{EFF}C_{OUT}}$$

and:

$$R_{EFF} = R_{ESR} + R_{DROOP} + R_{PCB}$$

where C_{OUT} is the total output capacitance, R_{ESR} is the total equivalent-series-resistance, R_{DROOP} is the voltage-positioning gain, and R_{PCB} is the parasitic board resistance between the output capacitors and sense resistors.

For a standard 300kHz application, the ESR zero frequency must be well below 95kHz, preferably below 50kHz. Tantalum, Sanyo POSCAP, and Panasonic SP capacitors in wide-spread use at the time of publication have typical ESR zero frequencies below 50kHz. In the standard application circuit, the ESR needed to support a 30mV$_{P-P}$ ripple is 30mV/(40A x 0.3) = 2.5mΩ. Four 330µF/2.5V Panasonic SP (type SX) capacitors in parallel provide 1.5mΩ (max) ESR. With a 2mΩ droop and 0.5mΩ PCB resistance, the typical combined ESR results in a zero at 30kHz.

Ceramic capacitors have a high ESR zero frequency, but applications with significant voltage positioning can take advantage of their size and low ESR. Do not put high-value ceramic capacitors directly across the output without verifying that the circuit contains enough voltage positioning and series PCB resistance to ensure stability. When only using ceramic output capacitors, output overshoot (V_{SOAR}) typically determines the minimum output capacitance requirement.

Unstable operation manifests itself in two related but distinctly different ways: double-pulsing and feedback loop instability. Double-pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output voltage signal. This “fools” the error comparator into triggering a new cycle immediately after the minimum off-time period has expired. Double-pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability due to insufficient ESR. Loop instability can result in oscillations at the output after line or load steps. Such perturbations are usually damped, but can cause the output voltage to rise above or fall below the tolerance limits.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output-voltage ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under/overshoot.

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. The multiphase Quick-PWM controllers operate out-of-phase, while the Quick-PWM slave controllers provide selectable out-of-phase or in-phase on-time triggering. Out-of-phase operation reduces the RMS input current by dividing the input current between several staggered stages. For duty cycles less than 100%/η_{TOTAL} per phase, the I_{RMS} requirements may be determined by the following equation:

$$I_{RMS} = \left(\frac{I_{LOAD}}{\eta_{TOTAL} V_{IN}} \right) \sqrt{\eta_{TOTAL} V_{OUT} \left(V_{IN} - \eta_{TOTAL} V_{OUT} \right)}$$

where η_{TOTAL} is the total number of out-of-phase switching regulators. The worst-case RMS current requirement occurs when operating with $V_{IN} = 2\eta_{TOTAL}V_{OUT}$. At this point, the above equation simplifies to $I_{RMS} = 0.5 \times I_{LOAD}/\eta_{TOTAL}$.

For most applications, non-tantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to inrush surge currents typical of systems with a mechanical switch or connector in series with the input. If the Quick-PWM controller is operated as the second stage of a two-stage power-conversion system, tantalum input capacitors are acceptable. In either configuration, choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal circuit longevity.

Power MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability when using high-voltage (> 20V) AC adapters. Low-current applications usually require less attention.

The high-side MOSFET (N_H) must be able to dissipate the resistive losses plus the switching losses at both $V_{IN(MIN)}$ and $V_{IN(MAX)}$. Calculate both of these sums. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to losses at $V_{IN(MAX)}$, with lower losses in between. If the losses at $V_{IN(MIN)}$ are significantly higher than the losses at $V_{IN(MAX)}$, consider increasing the size of N_H (reducing $R_{DS(ON)}$ but with higher C_{GATE}). Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher than the losses at $V_{IN(MIN)}$, consider reducing the size of N_H (increasing $R_{DS(ON)}$ to lower C_{GATE}). If V_{IN} does not vary over a wide range, the minimum power dissipation occurs where the resistive losses equal the switching losses.

Choose a low-side MOSFET that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., one or two 8-pin SOs, DPAK, or D^{2}PAK), and is reasonably priced. Make sure that the DL gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic gate-to-drain capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems may occur (see the *MOSFET Gate Driver* section).

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MOSFET Power Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET (N_H), the worst-case power dissipation due to resistance occurs at the minimum input voltage:

$$PD\ (N_H\ Resistive) = \left(\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{I_{LOAD}}{\eta_{TOTAL}}\right)^2 R_{DS(ON)}$$

where η_{TOTAL} is the total number of phases.

Generally, a small high-side MOSFET is desired to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power dissipation often limits how small the MOSFET can be. Again, the optimum occurs when the switching losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses do not usually become an issue until the input is greater than approximately 15V.

Calculating the power dissipation in the high-side MOSFET (N_H) due to switching losses is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PCB layout characteristics. The following switching-loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on N_H:

$$PD\ (N_H\ Switching) = \left(\frac{V_{IN(MAX)}I_{LOAD}f_{SW}}{\eta_{TOTAL}}\right)\left(\frac{Q_{G(SW)}}{I_{GATE}}\right) + \frac{C_{OSS}V_{IN}{}^2f_{SW}}{2}$$

where C_{OSS} is the N_H MOSFET's output capacitance, $Q_{G(SW)}$ is the charge needed to turn on the N_H MOSFET, and I_{GATE} is the peak gate-drive source/sink current (2.2A, typ).

Switching losses in the high-side MOSFET can become an insidious heat problem when maximum AC adapter voltages are applied, due to the squared term in the C x $V_{IN}{}^2$ x f_{SW} switching-loss equation. If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low battery voltages becomes extraordinarily hot when biased from $V_{IN(MAX)}$, consider choosing another MOSFET with lower parasitic capacitance.

For the low-side MOSFET (N_L), the worst-case power dissipation always occurs at maximum input voltage:

$$PD\ (N_L\ Resistive) = \left[1-\left(\frac{V_{OUT}}{V_{IN(MAX)}}\right)\right]\left(\frac{I_{LOAD}}{\eta_{TOTAL}}\right)^2 R_{DS(ON)}$$

The worst case for MOSFET power dissipation occurs under heavy overloads that are greater than $I_{LOAD(MAX)}$ but are not quite high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, you can "over design" the circuit to tolerate:

$$I_{LOAD} = \eta_{TOTAL}\left(I_{VALLEY(MAX)} + \frac{\Delta I_{INDUCTOR}}{2}\right)$$

$$= \eta_{TOTAL}I_{VALLEY(MAX)} + \left(\frac{I_{LOAD(MAX)}LIR}{2}\right)$$

where $I_{VALLEY(MAX)}$ is the maximum valley current allowed by the current-limit circuit, including threshold tolerance and on-resistance variation. The MOSFETs must have a good size heatsink to handle the overload power dissipation.

Choose a Schottky diode (D_L) with a forward voltage low enough to prevent the low-side MOSFET body diode from turning on during the dead time. Select a diode that can handle the load current per phase during the dead times. This diode is optional and can be removed if efficiency is not critical.

Boost Capacitors

The boost capacitors (C_{BST}) must be selected large enough to handle the gate-charging requirements of the high-side MOSFETs. Typically, 0.1µF ceramic capacitors work well for low-power applications driving medium-sized MOSFETs. However, high-current applications driving large, high-side MOSFETs require boost capacitors larger than 0.1µF. For these applications, select the boost capacitors to avoid discharging the capacitor more than 200mV while charging the high-side MOSFETs' gates:

$$C_{BST} = \frac{N \times Q_{GATE}}{200mV}$$

where N is the number of high-side MOSFETs used for one regulator, and Q_{GATE} is the gate charge specified in the MOSFET's data sheet. For example, assume (2) IRF7811W n-channel MOSFETs are used on the high side. According to the manufacturer's data sheet, a single IRF7811W has a maximum gate charge of 24nC (V_{GS} = 5V). Using the above equation, the required boost capacitance would be:

$$C_{BST} = \frac{2 \times 24nC}{200mV} = 0.24\mu F$$

Selecting the closest standard value, this example requires a 0.22µF ceramic capacitor.

Current-Balance Compensation (CCI)

The current-balance compensation capacitor (C_{CCI}) integrates the difference between the main and secondary current-sense voltages. The internal compensation resistor (R_{CCI} = 200kΩ) improves transient response by increasing the phase margin. This allows the dynamics of the current-balance loop to be optimized. Excessively large capacitor values increase the integration time constant, resulting in larger current differences between the phases during transients. Excessively small capacitor values allow the current loop to respond cycle-by-cycle but can result in small DC current variations between the phases. Likewise, excessively large resistor values can also cause DC current variations between the phases. Small resistor values reduce the phase margin, resulting in marginal stability in the current-balance loop. For most applications, a 470pF capacitor from CCI to the switching regulator's output works well.

Connecting the compensation network to the output (V_{OUT}) allows the controller to feed-forward the output voltage signal, especially during transients. To reduce noise pick-up in applications that have a widely distributed layout, it is sometimes helpful to connect the compensation network to the quiet analog ground rather than V_{OUT}.

Voltage Positioning and Loop Compensation

Voltage positioning dynamically lowers the output voltage in response to the load current, reducing the output capacitance and processor's power dissipation requirements. The controller uses a transconductance amplifier to set the transient and DC output-voltage droop (Figure 2) as a function of the load. This adjustability allows flexibility in the selected current-sense resistor value or inductor DCR, and allows smaller current-sense resistance to be used, reducing the overall power dissipated.

Steady-State Voltage Positioning

Connect a resistor (R_{FB}) between FB and V_{OUT} to set the DC steady-state droop (load line) based on the required voltage-positioning slope (R_{DROOP}):

$$R_{FB} = \frac{R_{DROOP}}{R_{SENSE} G_{m(FB)}}$$

where the effective current-sense resistance (R_{SENSE}) depends on the current-sense method (see the *Current Sense* section), and the voltage-positioning amplifier's transconductance ($G_{m(FB)}$) is typically 1.2mS as defined in the *Electrical Characteristics* table. The controller uses the CSPAVG pin to get the average inductor current from the positive current-sense averaging network.

When the inductors' DCR is used as the current-sense element ($R_{SENSE} = R_{DCR}$), the current-sense inputs should include an NTC thermistor to minimize the temperature dependence of the voltage-positioning slope.

Minimum Input Voltage Requirements and Dropout Performance

The output-voltage adjustable range for continuous-conduction operation is restricted by the nonadjustable minimum off-time one-shot and the number of phases. For best dropout performance, use the slower (200kHz) on-time settings. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on- and off-times. Manufacturing tolerances and internal propagation delays introduce an error to the on-times. This error is greater at higher frequencies. Also, keep in mind that transient response performance of buck regulators operated too close to dropout is poor, and bulk output capacitance must often be added (see the V_{SAG} equation in the *Transient Response* section).

The absolute point of dropout is when the inductor current ramps down during the minimum off-time (ΔI_{DOWN}) as much as it ramps up during the on-time (ΔI_{UP}). The ratio $h = \Delta I_{UP}/\Delta I_{DOWN}$ is an indicator of the ability to slew the inductor current higher in response to increased load, and must always be greater than 1. As h approaches 1, the absolute minimum dropout point, the inductor current cannot increase as much during each switching cycle and V_{SAG} greatly increases unless additional output capacitance is used.

A reasonable minimum value for h is 1.5, but adjusting this up or down allows trade-offs between V_{SAG}, output capacitance, and minimum operating voltage. For a given value of h, the minimum operating voltage can be calculated as:

$$V_{IN(MIN)} = \eta_{TOTAL}\left[\frac{V_{FB} - V_{DROOP} + V_{DIS}}{1 - \eta_{TOTAL} h \times t_{OFF(MIN)} f_{SW}}\right] + V_{CHG} - V_{DIS} + V_{DROOP}$$

where η_{TOTAL} is the total number of out-of-phase switching regulators, V_{FB} is the voltage-positioning droop, V_{DIS} and V_{CHG} are the parasitic voltage drops in the discharge and charge paths (see the on-time one-shot parameter), $t_{OFF(MIN)}$ is from the *Electrical Characteristics* table. The absolute minimum input voltage is calculated with h = 1.

Dual-Phase, Quick-PWM Controller for IMVP6+ CPU Core Power Supplies

If the calculated $V_{IN(MIN)}$ is greater than the required minimum input voltage, then reduce the operating frequency or add output capacitance to obtain an acceptable V_{SAG}. If operation near dropout is anticipated, calculate V_{SAG} to be sure of adequate transient response.

Dropout Design Example:

V_{FB} = 1.4V

f_{SW} = 300kHz

$t_{OFF(MIN)}$ = 400ns

V_{DROOP} = 3mV/A x 30A = 90mV

$V_{DROP1} = V_{DROP2}$ = 150mV (30A load)

h = 1.5 and η_{TOTAL} = 2

$$V_{IN(MIN)} = 2 \times \left[\frac{1.4V - 90mV + 150mV}{1 - 2 \times (0.4\mu s \times 1.5 \times 300kHz)} \right] + 150mV - 150mV + 90mV = 4.96V$$

Calculating again with h = 1 gives the absolute limit of dropout:

$$V_{IN(MIN)} = 2 \times \left[\frac{1.4V - 90mV + 150mV}{1 - 2 \times (0.4\mu s \times 1.0 \times 300kHz)} \right] + 150mV - 150mV + 90mV = 4.07V$$

Therefore, V_{IN} must be greater than 4.1V, even with very large output capacitance, and a practical input voltage with reasonable output capacitance would be 5.0V.

Applications Information

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention. If possible, mount all of the power components on the top side of the board with their ground terminals flush against one another. Refer to the MAX17410 evaluation kit specification for a layout example and follow these guidelines for good PCB layout:

1) Keep the high-current paths short, especially at the ground terminals. This is essential for stable, jitter-free operation.
2) Connect all analog grounds to a separate solid copper plane, which connects to the GND pin of the Quick-PWM controller. This includes the V_{CC} bypass capacitor and GNDS bypass capacitors.
3) Keep the power traces and load connections short. This is essential for high efficiency. The use of thick copper PCBs (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PCB traces is a difficult task that must be approached in terms of fractions of centimeters, where a single mΩ of excess trace resistance causes a measurable efficiency penalty.
4) Keep the high-current, gate-driver traces (DL_, DH_, LX_, and BST_) short and wide to minimize trace resistance and inductance. This is essential for high-power MOSFETs that require low-impedance gate drivers to avoid shoot-through currents.
5) CSP_ and CSN_ connections for current limiting and voltage positioning must be made using Kelvin sense connections to guarantee the current-sense accuracy.
6) When trade-offs in trace lengths must be made, it is preferable to allow the inductor-charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
7) Route high-speed switching nodes away from sensitive analog areas (CCI, FB, CSP_, CSN_, etc.).

Layout Procedure

1) Place the power components first, with ground terminals adjacent (low-side MOSFET source, C_{IN}, C_{OUT}, and D1 anode). If possible, make all these connections on the top layer with wide, copper-filled areas.
2) Mount the controller IC adjacent to the low-side MOSFET. The DL gate traces must be short and wide (50 mils to 100 mils wide if the MOSFET is 1in from the controller IC).
3) Group the gate-drive components (BST diodes and capacitors, V_{DD} bypass capacitor) together near the controller IC.

4) Make the DC-DC controller ground connections as shown in the standard application circuits. This diagram can be viewed as having four separate ground planes: input/output ground, where all the high-power components go; the power ground plane, where the GND pin and V_{DD} bypass capacitor go; the master's analog ground plane where sensitive analog components, the master's GND pin, and V_{CC} bypass capacitor go; and the slave's analog ground plane where the slave's GND pin and V_{CC} bypass capacitor go. The master's GND plane must meet the GND plane only at a single point directly beneath the IC. Similarly, the slave's GND plane must meet the GND plane only at a single point directly beneath the IC. The respective master and slave ground planes should connect to the high-power output ground with a short metal trace from GND to the source of the low-side MOSFET (the middle of the star ground). This point must also be very close to the output capacitor ground terminal.

5) Connect the output power planes (V_{CORE} and system ground planes) directly to the output filter capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the CPU as is practical.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
48 TQFN-EP	T4877+6	**21-0144**

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