Click here for production status of specific part numbers.

MAX17557 4.5V to 60V, Synchronous Step-Down Controller

General Description

The MAX17557 is a synchronous step-down controller that drives nMOSFETs. The device uses a constant-frequency, peak-current-mode architecture.

The IC supports current sensing using either an external current-sense resistor for accuracy or an inductor DCR for improved system efficiency. Current foldback limits MOSFET power dissipation under short-circuit conditions.

The IC can start up monotonically into a prebiased output. The device can be operated in forced pulse-width modulation (PWM), or discontinuous-conduction mode (DCM) to enable high efficiency under full-load and light-load conditions. The device features a programmable soft-stop enable (SSTPEN) or disable function.

The IC operates over the -40°C to +125°C temperature range and is available in a lead (Pb)-free, 20-pin TQFN, 4mm x 4mm package with an exposed pad.

Applications

- Industrial Power Supplies
- Distributed DC Power Systems
- Motion Control
- Programmable Logic Controllers
- Computerized Numerical Control

Benefits and Features

- Wide Range of Operation
  - Wide 4.5V to 60V Input Voltage Range
  - Wide 0.8V to 24V Output Voltage Range
  - R_{SENSE} or Inductor DCR Current-Sensing
  - 100kHz to 2.2MHz Adjustable Frequency with External Clock Synchronization
  - Available in a Lead (Pb)-Free 20-Pin, 4mm x 4mm TQFN-EP Package
- Enhances Power Efficiency
  - Low-Impedance Gate Drives for High Efficiency
  - DCM Operation at Light Loads
  - Auxiliary Bootstrap LDO
- Operates Reliably in Adverse Industrial Environments
  - Programmable Soft-Stop Enable or Disable Function
  - Adjustable Soft-Start
  - Current Foldback Limits MOSFET Heat Dissipation During a Short-Circuit Condition
  - Overtemperature Protection
  - High Industrial Ambient Operating Temperature Range (-40°C to +125°C) and Junction Temperature Range (-40°C to +150°C)

***Ordering Information* appears at end of data sheet.**

19-100075; Rev 2; 5/18

maxim integrated™

Absolute Maximum Ratings

V_{IN} to PGND .....-0.3V to +65V
CSP, CSN to GND.....-0.3V to +26V
CSP to CSN .....-0.3V to +0.3V
LX, BST to PGND.....-0.3V to +65V
BST to LX.....-0.3V to +6V
BST to V_{CCINT} .....-0.3V to +65V
DH to LX .....-0.3V to (V_{BST} + 0.3)V
DL to PGND .....-0.3V to (V_{CCINT} + 0.3)V
EN, SSTPEN, V_{CCINT} to GND.....-0.3V to +6V
V_{CCEXT} to GND .....-0.3V to +26V
PGND to GND.....-0.3V to +0.3V
PGOOD to GND.....-0.3V to V_{IN} + 0.3V
COMP, SS, RT, ILIMSEL, MODE/SYNC .....-0.3V to +6V
GND to EP.....-0.3V to +0.3V
Continuous Power Dissipation at +70°C
(multilayer board).....2051.30mW
Power Deration (multilayer board) .....25.6mW/°C
Operating Temperature Range (Note 1)..... -40°C to +125°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Junction temperature greater than +125°C degrades operating lifetimes.

Package Information

PACKAGE TYPE: 20 TQFN	
Package Code	T2044+3C
Outline Number	**21-0139**
Land Pattern Number	**90-0037**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	39°C/W
Junction to Case (θ_{JC})	6°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = 24V, T_A = -40°C to +125°C, unless otherwise noted. Typical Values are at T_A = 25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY						
Input Voltage Range	V_{IN}		4.5		60	V
		V_{CCINT} = V_{IN}	4.5		5.5	
Quiescent Supply Current (DCM)	I_{QNS}	No switching EN = unconnected, V_{FB} = 0.81V	0.5	1.5	2.5	mA
Quiescent Supply Current (PWM)	I_{QS}	EN = unconnected, f_{SW} = 350 kHz, Switching	1	1.8	3.5	mA
Shutdown Supply Current	I_{STBY}	EN = GND	0.1	6	20	µA
V_{CCINT} REGULATOR						
V_{CCINT} Output Voltage	V_{CCINT}	6V < V_{IN} < 60V, I_{VCCINT} = 1mA	4.95	5.15	5.3	V
		6V < V_{CCEXT} < 24V, I_{VCCINT} = 1mA, (V_{CCINT} supplied from V_{CCEXT})	4.95	5.15	5.3	
V_{CCINT} Load Regulation		V_{IN} = 12V, I = 0mA to 30 mA, V_{CCEXT} = 0V, (V_{CCINT} supplied from V_{IN})	5	13	25	mV
		V_{CCEXT} = 12V, I_{VCCINT} = 0 A to 30mA, (V_{CCINT} supplied from V_{CCEXT})	5	13	25	
V_{CCINT} Short-Circuit Output Current		V_{IN} = 8.5V, V_{CCEXT} = 0V, V_{CCINT} = 4V	40	85	140	mA
		V_{CCEXT} = 8.5V, V_{CCINT} = 4V, V_{CCINT} supplied from V_{CCEXT}	45	85	140	
V_{CCINT} Dropout Voltage		V_{IN} = 4.5V, V_{CCEXT} = 0V, I_{VCCINT} = 45mA		270	550	mV
		V_{CCINT} supplied from V_{CCEXT}, V_{CCEXT} = 4.7V, I_{VCCINT} = 45mA		100	400	
V_{CCEXT} Switchover Voltage		V_{CCEXT} rising	4.55	4.7	4.85	V
V_{CCEXT} Switchover Voltage Hysteresis			0.2	0.25	0.35	V
V_{CCINT} UVLO		V_{CCINT} rising	4.14	4.35	4.55	V
		V_{CCINT} falling	3.65	3.85	4.05	
OSCILLATOR						
Switching Frequency	f_{SW}	RT = 187kΩ	90	100	110	kHz
		RT = 93.1kΩ	180	200	220	
		RT = open	325	350	375	
		RT = 6.98kΩ	1950	2200	2450	
Switching Frequency Adjustable Range	f_{SW}		100		2200	kHz
MODE/SYNC						
Minimum SYNC Pulse Width			50			ns

Electrical Characteristics (continued)

(V_{IN} = 24V, T_A = -40°C to +125°C, unless otherwise noted. Typical Values are at T_A = 25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNC Frequency Capture Range		Frequency set by RT	1.1 × f_{SW}		1.4 × f_{SW}	kHz
MODE/SYNC Logic Low Threshold		When used as SYNC			0.8	V
MODE/SYNC Logic High Threshold		When used as SYNC	2			V
MODE/SYNC Threshold	V_{M_DCM}	MODE = V_{CC} (DCM Mode)	2			V
	V_{M_PWM}	MODE = GND (PWM Mode)			0.6	
GATE DRIVER						
DH to BST On-Resistance		Source 100mA	0.8	1.2	2.1	Ω
DH to LX On-Resistance		Sink 100mA	0.22	0.4	0.8	Ω
DL to V_{CCINT} On-Resistance		Source 100mA	0.8	1.2	2.1	Ω
DL to PGND On-Resistance		Sink 100mA	0.22	0.4	0.8	Ω
DH Minimum Controlled On-Time	DH_MIN_t_{ON}		70	130	175	ns
DL Minimum Guaranteed On-Time	DL_MIN_ t_{ON}	Skip/Mode = V_{CCINT}, FB = 0.76V	80	120	160	ns
Dead Time	t_{DT}	DH_ falling to DL_ rising, C_{LOAD} = 6nF		30		ns
		DL_ falling to DH_ rising, C_{LOAD} = 6nF		25		
DH Transition Time		DH_ rising, C_{LOAD} = 6nF		35		ns
		DH_ falling, C_{LOAD} = 6nF		15		
DL Transition Time		DL_ rising, C_{LOAD} = 6nF		35		ns
		DL_ falling, C_{LOAD} = 6nF		15		
SOFT START						
Soft-Start Current	I_{SS}	V_{SS} = 0.5V	4.5	5	5.5	µA
Soft-Stop Current	I_{SST}	V_{SS} = 0.5V	-4.5	-5	-5.5	µA
ENABLE						
EN Logic-High Threshold		EN_ rising	1.2	1.25	1.3	V
EN Hysteresis				160		mV
EN Bias Pullup Current		$V_{EN\_}$ = 0.5V	0.9	2	3	µA
CURRENT SENSE AMPLIFIER						
CSP, CSN Common Mode Voltage Range					24	V
CSP to CSN Input Operating Voltage Range	$V_{CSP\_}$ - $V_{CSN\_}$	0 < V_{CSN} < 24V	-50		100	mV

Electrical Characteristics (continued)

(V_{IN} = 24V, T_A = -40°C to +125°C, unless otherwise noted. Typical Values are at T_A = 25°C.) (Note 2)

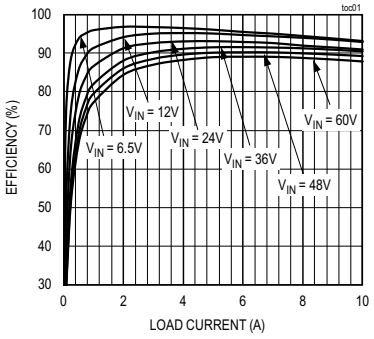
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Sense Amplifier Gain	G_{CS}		12	13.3	14.5	V/V
CSP Input Bias current		0 < V_{CSP} < 24V	-2.8	0	2.8	µA
CSN Input Bias current		V_{CSP} = V_{CSN}, 0.8V < V_{CSN} < 24V	-5		650	µA
CURRENT LIMIT						
Cycle-by-Cycle Peak Positive Current Limit Threshold	V_{CS}	Equivalent at CSP - CSN G_{SA} = 13.3	65	75	85	mV
ILIMSEL Threshold Voltage		Latchoff	3.3			V
		Brickwall + foldback			0.8	
SSTPEN THRESHOLD						
Low-Voltage Threshold		Soft-stop disabled			0.8	V
High-Voltage Threshold		Soft-stop enabled	3.3			V
ERROR AMPLIFIER						
Regulation Voltage	V_{FB}		785	800	812	mV
FB Input Leakage Current			-100	0	+100	nA
Transconductance	g_M		1.65	2	2.3	mA/V
Open-Loop Gain				72		dB
Open-Loop Bandwidth				10		MHz
POWER-GOOD OUTPUTS						
PGOOD UV Threshold	UV_TH	V_{FB} rising		0.740		V_{FB}
		V_{FB} falling		0.720		
PGOOD OV Threshold	OV_TH	V_{FB} rising		0.880		V_{FB}
		V_{FB} falling		0.860		
PGOOD Delay		Rise UV, OV		20		µs
		Fall UV, OV		10		
PGOOD Output Leakage		PGOOD = 40V, T_A = 25°C	-1	0	+1	µA
PGOOD Output-Low Voltage		I_PGOOD = 1mA, EN = 0V		120		mV
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold				165		°C
Thermal-Shutdown Hysteresis				10		°C

Note 2: All Electrical Specifications are 100% production tested at T_A = +25°C. Specifications over the operating temperature range are guaranteed by design and characterization.

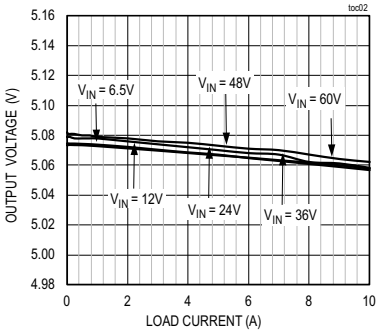
Typical Operating Characteristics

(V_{EN} = V_{IN} = 24V, V_{SSTPEN} = GND, V_{SGND} = V_{PGND} = 0V, C_{VCC} = 10µF, C_{BST} = 0.47µF, C_{SS} = 15000pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

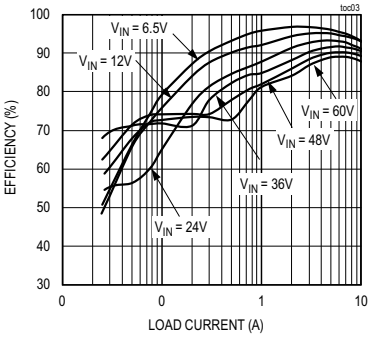
EFFICIENCY vs. LOAD CURRENT
(5V OUTPUT, PWM MODE, FIGURE 8 CIRCUIT)



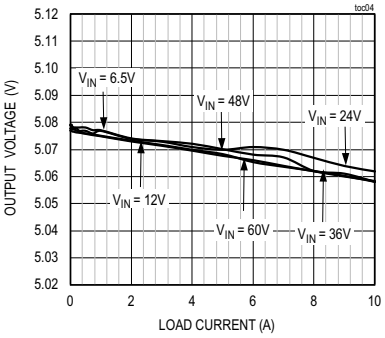
LOAD AND LINE REGULATION
(5V OUTPUT, PWM MODE, FIGURE 8 CIRCUIT)



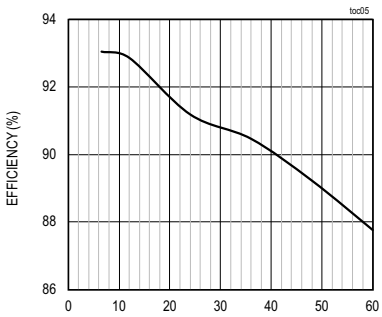
EFFICIENCY vs. LOAD CURRENT
(5V OUTPUT, DCM MODE, FIGURE 8 CIRCUIT)



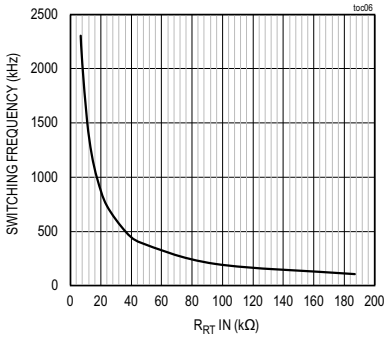
LOAD AND LINE REGULATION
(5V OUTPUT, DCM MODE, FIGURE 8 CIRCUIT)



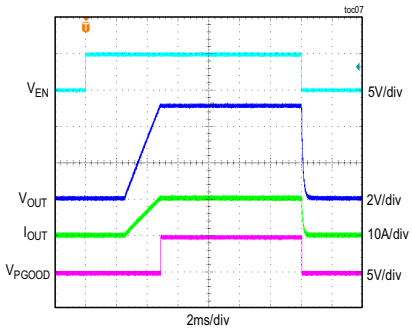
EFFICIENCY vs. INPUT VOLTAGE
(5V OUTPUT, PWM MODE, FIGURE 8 CIRCUIT)



SWITCHING FREQUENCY vs. RT RESISTANCE
(5V OUTPUT)



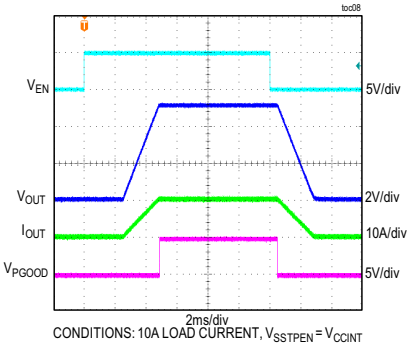
SOFT-START/SHUTDOWN FROM EN
(5V OUTPUT, PWM MODE, FIGURE 8 CIRCUIT)



Typical Operating Characteristics (continued)

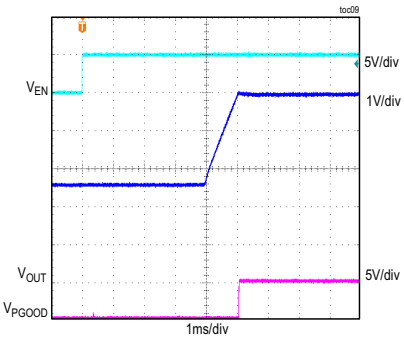
(V_{EN} = V_{IN} = 24V, V_{SSTPEN} = GND, V_{SGND} = V_{PGND} = 0V, C_{VCC} = 10µF, C_{BST} = 0.47µF, C_{SS} = 15000pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

SOFT-START/SHUTDOWN FROM EN
(5V OUTPUT, PWM MODE, FIGURE 8 CIRCUIT)



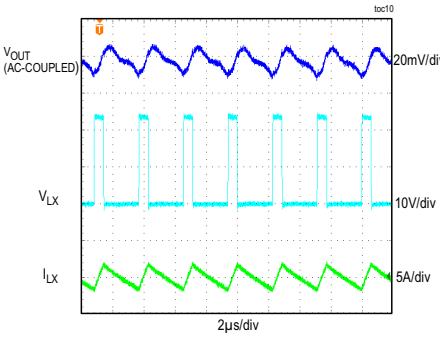
CONDITIONS: 10A LOAD CURRENT, V_{SSTPEN} = V_{CCINT}
PGOOD IS PULLED UP TO V_{CCINT} WITH A 100kΩ RESISTOR

SOFT-START WITH 2.5V PREBIAS
(5V OUTPUT, PWM MODE, FIGURE 8 CIRCUIT)



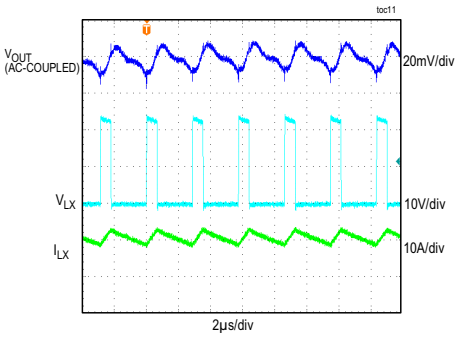
PGOOD IS PULLED UP TO V_{CCINT} WITH A 100kΩ RESISTOR

STEADY-STATE SWITCHING WAVEFORMS
(5V OUTPUT, PWM MODE, FIGURE 8 CIRCUIT)



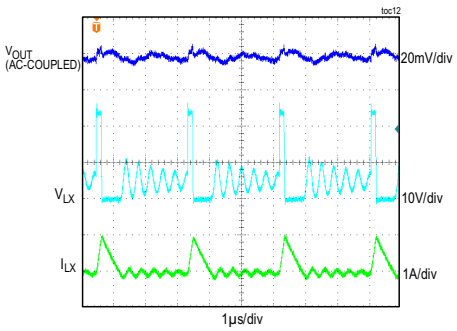
CONDITIONS: NO LOAD

STEADY-STATE SWITCHING WAVEFORMS
(5V OUTPUT, PWM MODE, FIGURE 8 CIRCUIT)



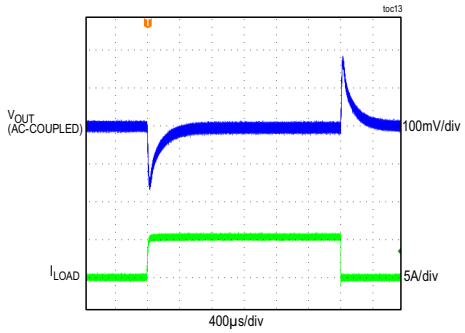
CONDITIONS: 10A LOAD CURRENT

STEADY-STATE SWITCHING WAVEFORMS
(5V OUTPUT, DCM MODE, FIGURE 8 CIRCUIT)



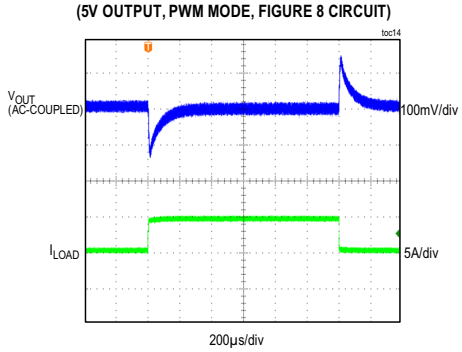
CONDITIONS: 0.1A LOAD CURRENT

LOAD TRANSIENT RESPONSE
(5V OUTPUT, PWM MODE, FIGURE 8 CIRCUIT)



CONDITIONS: LOAD CURRENT STEPPED FROM 0A TO 5A

LOAD TRANSIENT RESPONSE
(5V OUTPUT, PWM MODE, FIGURE 8 CIRCUIT)

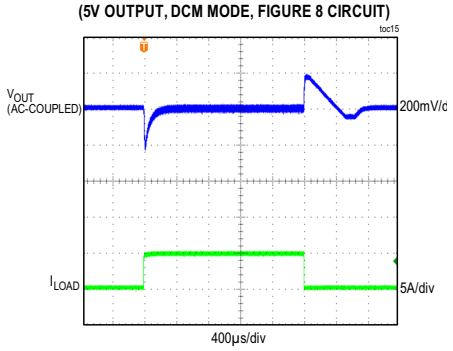


CONDITIONS: LOAD CURRENT STEPPED FROM 5A TO 10A

Typical Operating Characteristics (continued)

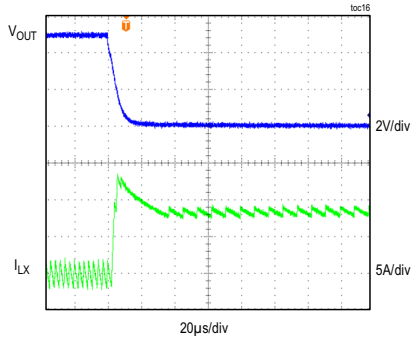
(V_{EN} = V_{IN} = 24V, V_{SSTPEN} = GND, V_{SGND} = V_{PGND} = 0V, C_{VCC} = 10µF, C_{BST} = 0.47µF, C_{SS} = 15000pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

LOAD TRANSIENT RESPONSE
(5V OUTPUT, DCM MODE, FIGURE 8 CIRCUIT)

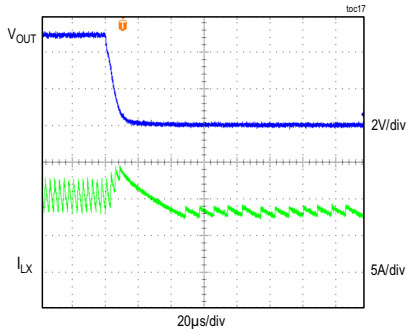


CONDITIONS: LOAD CURRENT STEPPED FROM 0.1A TO 5A

OVERCURRENT PROTECTION
(5V OUTPUT, PWM MODE, FIGURE 8 CIRCUIT)

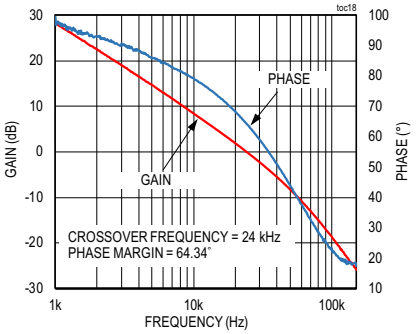


SHORT-CIRCUIT UNDER STEADY-STATE
(5V OUTPUT, PWM MODE, FIGURE 8 CIRCUIT)



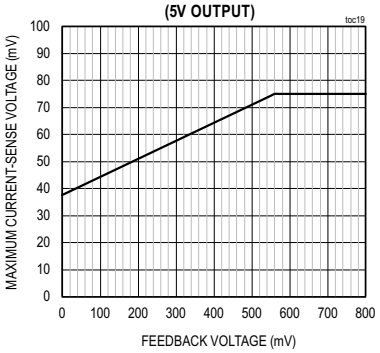
CONDITIONS: 10A LOAD CURRENT

BODE PLOT
(5V OUTPUT, FIGURE 8 CIRCUIT)

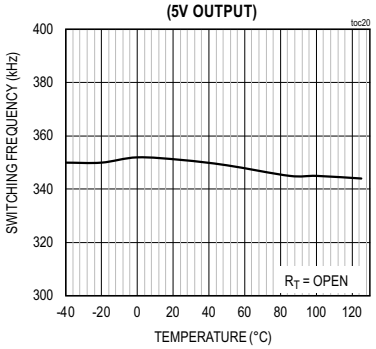


CONDITIONS: 10A LOAD CURRENT

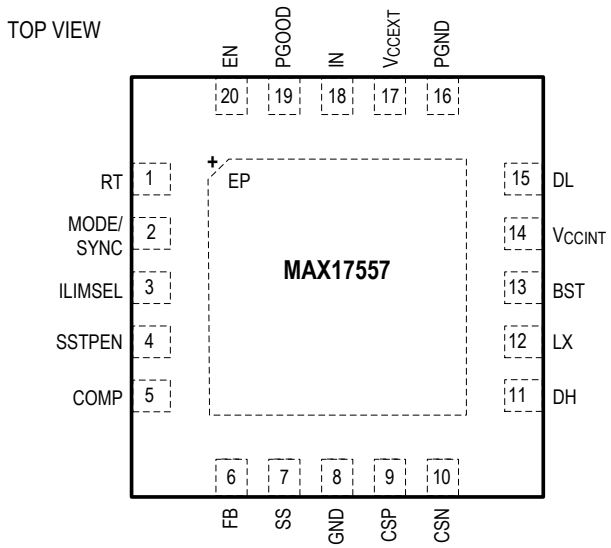
MAXIMUM CURRENT-SENSE VOLTAGE
vs. FEEDBACK VOLTAGE
(5V OUTPUT)



SWITCHING FREQUENCY vs. TEMPERATURE
(5V OUTPUT)



Pin Configurations



20-PIN TQFN
4mm × 4mm

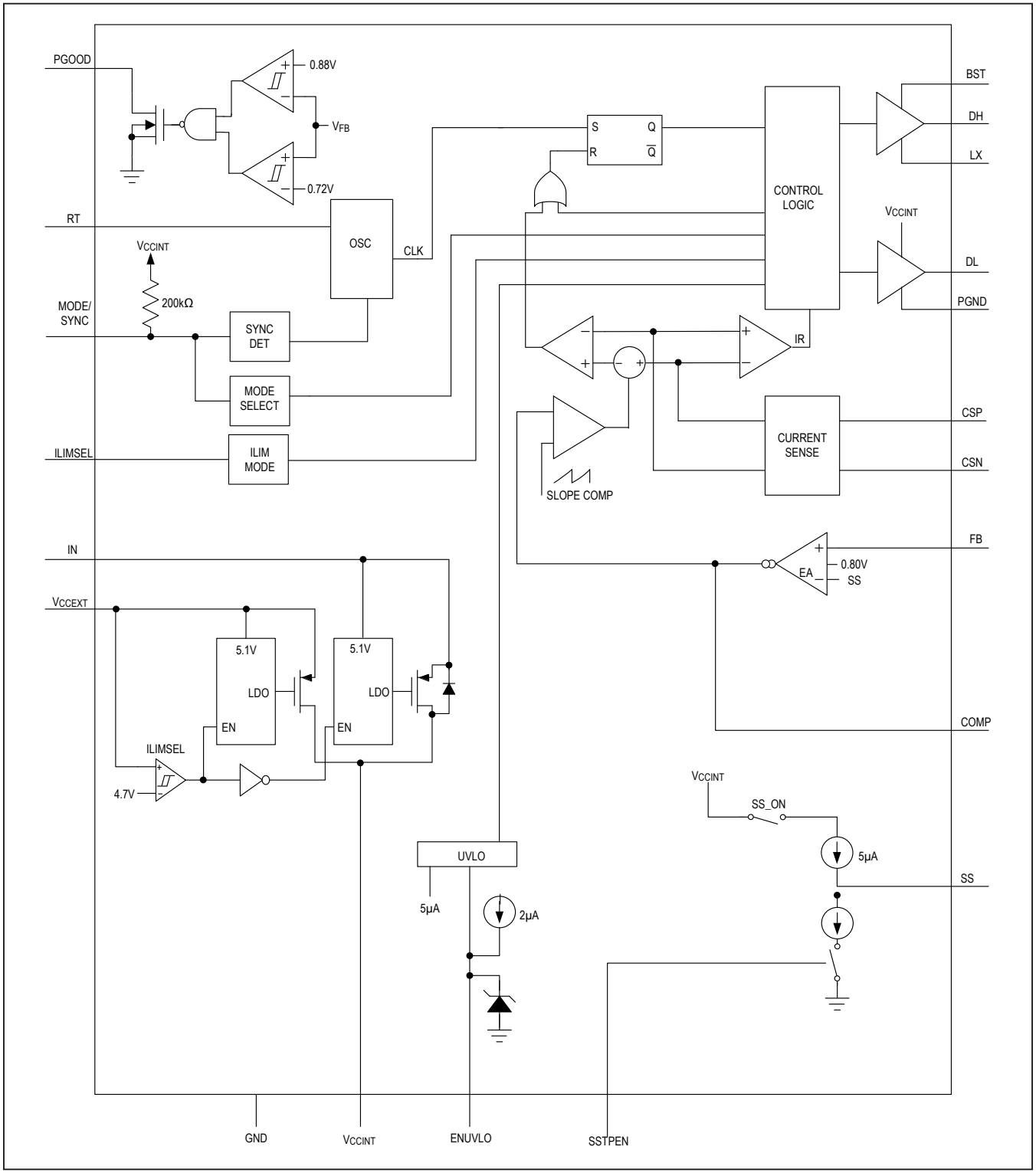
Pin Description

PIN	NAME	FUNCTION
1	RT	Programmable Switching Frequency Input. Connect a resistor from RT to GND to set the regulator's switching frequency. Leave RT open for the default 350kHz frequency.
2	MODE/ SYNC	Mode Selection and External Clock Synchronization Input. The MODE/SYNC pin configures the device to operate in pulse-width modulation (PWM) mode or discontinuous-conduction mode (DCM) of operation. Connect MODE/SYNC to GND for constant-frequency PWM operation at all loads. Connect MODE/SYNC to V_{CCINT} for DCM operation. The device can be synchronized to an external clock using this pin. See the *"Mode Selection and External Synchronization (MODE/SYNC)"* section for more details.
3	ILIMSEL	Input to Select the Device Operation Under Current Limit. Connect to GND to select Foldback mode or connect to V_{CC} to select Latchoff mode.
4	SSTPEN	Enable Soft-Stop. Connect to GND for no soft-stop; connect to V_{CCINT} to enable soft-stop feature.
5	COMP	Error Amplifier Output and Compensation Network Connection Node. Connect the COMP to the compensation network as shown in the circuit of Figure 5.

Pin Description (continued)

PIN	NAME	FUNCTION
6	FB	Feedback Voltage Input. Connect the FB to the midpoint of a resistor-divider from output to GND. See the circuit in Figure 2 for details.
7	SS	Output-Voltage Soft-Start Time Programming. Connect a capacitor from SS to GND to program output-voltage soft-start time.
8	GND	Signal Ground Connection. Connect to the PGND plane at a single point. Refer to the MAX17557 evaluation kit data sheet PCB layout for an example grounding scheme.
9	CSP	Current-Sense Amplifier Positive Input. Connect to positive terminal of current sense signal.
10	CSN	Current-Sense Amplifier Negative Input. Connect to negative terminal of current sense signal.
11	DH	High-Side MOSFET Driver Output. Connect to gate of high-side MOSFET.
12	LX	Switching Node Connection Input. Connect to output filter inductor.
13	BST	Bootstrap Capacitor Connection Input. Connect a capacitor between the BST and LX pins. See the *Bootstrap Capacitor Selection* section for more details. Connect a capacitor between BST and LX.
14	V_{CCINT}	Internal LDO Output. Connect a minimum 4.7µF low ESR ceramic capacitor between V_{CCINT} and PGND.
15	DL	Low-Side Driver Output. Connect to gate of low-side MOSFET.
16	PGND	Power Ground. Connect to the source terminal of the external low-side MOSFETs and V_{CCINT} bypass capacitor return terminal. Refer to the MAX17557 evaluation kit data sheet PCB layout for an example.
17	V_{CCEXT}	External Power-Supply Input for Internal LDO. Apply a voltage between 4.7V and 24V to disconnect the LDO that operates from IN, and power internal circuitry with the LDO connected to V_{CCEXT}. Add a local bypassing capacitor of 1µF on the V_{CCEXT} pin to PGND. Also, add a 2.2Ω resistor from the buck converter output node to the V_{CCEXT} pin to limit V_{CCINT} bypass capacitor discharge current and to protect the V_{CCEXT} pin from reaching absolute maximum rating (-0.3V) during an output short-circuit condition. Connect the V_{CCEXT} pin to PGND when the pin is not being used.
18	IN	Supply Input. Bypass with minimum 1µF low-ESR ceramic capacitor to PGND.
19	PGOOD	Open-Drain Power-Good Pin of Controller. Pullup with external resistor to a maximum of 5.5V.
20	EN	Enable Input for Controller. Either leave unconnected or connect to a voltage between 1.25V and 6V to enable. Connect to GND to disable.
—	EP	Exposed Pad. Always connect EP to the GND pin of the IC. Also, connect EP to a large GND plane with several thermal vias for the best thermal performance. Refer to the MAX17557 EV kit data sheet for an example of the correct method for EP connection and thermal vias.

Functional (or Block) Diagram



Detailed Description

The MAX17557 is a synchronous step-down controller that operates from a 4.5V to 60V wide input-supply range with programmable output voltage ranging from 0.8V up to 24V. The IC uses constant frequency, peak current-mode control for the control loop.

The frequency of the device can be adjusted from 100kHz to 2.2MHz using a resistor at the RT pin. The device provides an adjustable soft-start and can start up monotonically with a prebiased output voltage. The device can be operated in forced pulse-width modulation (PWM) mode or discontinuous-conduction mode (DCM) to enable high efficiency under full-load and light-load conditions. Other features include open-drain PGOOD output and enable (EN) input.

Internal LDO (V_{CCINT})

The IC has two internal 100mA low-dropout (LDO) linear regulators that power V_{CCINT}. One regulator is powered from IN, while the other is powered from V_{CCEXT}. At any time, one of the two regulators is in operation depending on the voltage levels at V_{CCEXT}. If V_{CCEXT} voltage is greater than 4.7V (typ) then V_{CCINT} is powered from the V_{CCEXT} regulator. If V_{CCEXT} is lower than 4.55V (typ), then V_{CCINT} is powered from the IN regulator. Powering V_{CCINT} from V_{CCEXT} increases efficiency at higher input voltages. V_{CCEXT} can be connected to the switching regulator output if that output voltage is greater than 4.7V (typ). The maximum voltage limit on V_{CCEXT} is 24V. V_{CCINT} output voltage powers the gate drivers and internal control circuitry. V_{CCINT} should be decoupled to PGND with at least a 4.7µF low-ESR ceramic capacitor. The IC employs an undervoltage-lockout (UVLO) circuit that forces the converter off when V_{CCINT} falls below 3.85V (typ). The converter is enabled again when V_{CCINT} > 4.35V (typ). Add a local bypassing capacitor of 1µF on the V_{CCEXT} pin to PGND. Also, add a 2.2Ω resistor from the buck converter output node to the V_{CCEXT} pin to limit V_{CCINT} bypass capacitor discharge current and to protect the V_{CCEXT} pin from reaching absolute maximum rating (-0.3V) during an output short-circuit condition. Connect the V_{CCEXT} pin to PGND when the pin is not being used.

Low-Side Gate Driver (DL)

Low-side external MOSFET gate driver is powered from V_{CCINT}. Under normal operating conditions, the lowside gate-driver output (DL) is always the complement of the high-side gate-driver output (DH). A dedicated circuitry monitors the DH and DL outputs and prevents either gate-drive signal from turning on until the other gate-drive signal is fully off. Thus, the circuit allows DH to turn on only when DL has been turned off. Similarly, it prevents DL from turning on until DH has been turned off. There must be a low-impedance path from the DL and DH pins to the external MOSFET gates to ensure that the gate driver's circuitry works properly. To minimize impedance, very short, wide traces should be used in the PCB layout. The internal pull-down transistor that drives the DL low is robust with a 0.4Ω (typ) on-resistance. This low on-resistance helps prevent DL from being pulled up during the fast rising of the LX node, due to capacitive coupling from the drain to the gate of the low-side synchronous rectifier MOSFET.

High-Side Gate Driver (DH)

High-side gate driver is powered from the bootstrap capacitors connected between BST and LX. The bootstrap capacitor normally gets charged to V_{CCINT} during each switching cycle through an external Schottky diode, when the low-side MOSFET turns on. The high-side MOSFET is turned on by closing an internal switch between BST and DH. This provides the necessary gate-to-source voltage to turn on the high-side MOSFET. See the Bootstrap Capacitor Selection section to choose the right size of the bootstrap capacitor.

Shutdown and Startup (EN and SS)

The controller of the IC can be shut down and enabled using the EN pin. Pulling of this pin below 1.25V (typ) shuts down the controller. Pulling EN below 0.7V disables controller and most internal circuits, including the V_{CCINT} LDOs. In this state, the device draws only 10µA (typ) of quiescent current. The EN pin can be open or externally pulled up to a voltage between 1.25V (typ) and 5.5V to turn on the controller. Figure 1 shows the possible EN pin configurations.

Voltage on the SS pin controls the startup of controller's output voltage. When the voltage on the SS pin is less than the 0.8V internal reference, the device regulates the FB voltage to the SS pin voltage instead of the 0.8V internal fixed reference. This allows the SS pin to be used to program the output-voltage soft-start time by connecting an external capacitor from the SS pin to GND. An internal 5µA pullup current charges this capacitor, creating a voltage ramp on the SS pin. As the SS voltage rises linearly from 0 to 0.8V, the output voltage rises smoothly from zero to its final value.

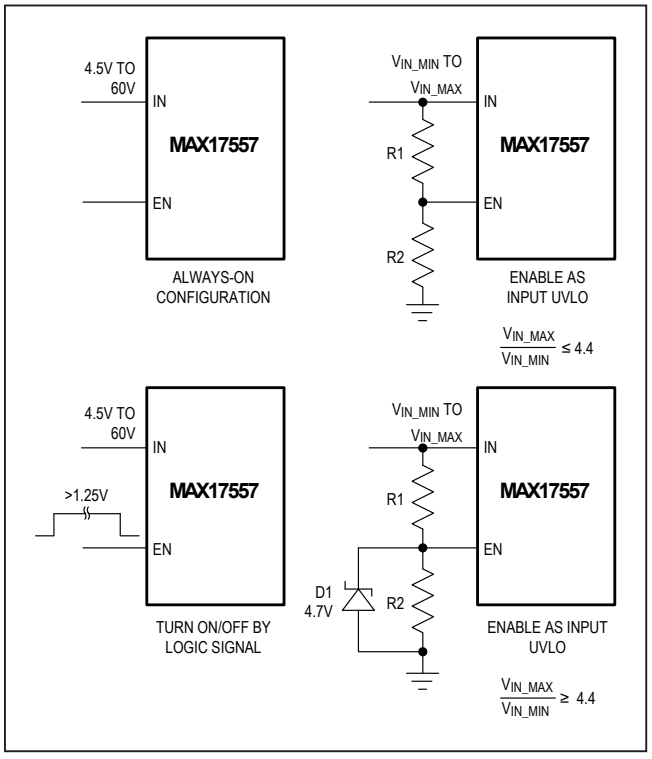


Figure 1. Possible EN Pin Configurations

Mode Selection and External Synchronization (MODE/SYNC)

The MAX17557 can be configured to operate either in DCM mode for high light-load efficiency or fixed-frequency PWM mode. The logic state of the MODE pin is latched when V_{CC} and EN voltages exceed the respective UVLO rising thresholds and all internal voltages are ready to allow LX switching. If the MODE pin is grounded at power-up, the device operates in constant-frequency PWM mode at all loads. Finally, if the MODE pin is connected to VCC at power-up, the device operates in constant-frequency DCM mode at light loads. State changes on the MODE pin are ignored during normal operation.

DCM MODE

In DCM mode, the device turns off the low-side MOSFET of the regulator close to the zero-crossing of the inductor current in each switching cycle. This operation minimizes negative current in the inductor, reducing loss due to current flowing from the output to the input. Therefore, the inductor current in each cycle is a triangular waveform whose peak is proportional to the load current demand. Under heavy loads, the controller operates at a constant frequency while adjusting the peak current in the inductor for load and input-voltage variations. However, under light-load and/or high input-voltage conditions, there exists a minimum on-time constraint for the controller. The minimum on-time is the smallest controllable pulse width that the controller can generate. This imposes a lower limit on the peak inductor current that can be programmed in the inductor and causes a fixed amount of energy to be delivered to the output, regardless of the energy requirement of the load. If the load is such that the amount of energy delivered during minimum on-time is more than the load energy, the output voltage rises above its nominal set value. This results in skipping switching cycles to regulate the average output voltage to the set point. This operation results in an effective switching frequency that is lower than the programmed switching frequency, which improves the regulator efficiency. As the load current increases to a point where the valley of the inductor current rises above zero, the regulator operation moves into PWM mode.

PWM MODE

The device operates in PWM mode whenever MODE is connected to GND. The inductor current can go negative in this mode. In PWM mode, under normal operating conditions, the high-side MOSFET turns on at an edge of the internal clock. An internal error amplifier compares the feedback voltage at the FB pin to a fixed internal reference voltage and generates an error current. This error current flows through the compensation network at the COMP pin and generates control voltage for the inner current loop. The on time of the high-side MOSFET in a switching cycle is determined by comparing the control voltage at the COMP pin with the sum of the current-sense voltage at CSP, CSN, and the internal slope-compensation voltage. The inductor current ramps up during the high-side MOSFET turn-on time. Once the high-side MOSFET is turned off, the low-side MOSFET is turned on. During low-side MOSFET turn-on time, the inductor current ramps down. The low-side MOSFET remains on until the next clock edge. PWM mode of operation has the advantages of low output voltage ripple and constant-frequency operation, which is beneficial in applications that are sensitive to operating frequency. Under the minimum on-time conditions described in the *DCM MODE* section, the device also skips high-side turn-on events in PWM mode to regulate the output voltage. This results in low-frequency operation with regard to inductor current and output-voltage-ripple waveforms.

External Frequency Synchronization

The internal oscillator of the MAX17557 can be synchronized to an external clock signal on the MODE/SYNC pin. The external synchronization clock frequency must be between 1.1 × f_{SW} and 1.4 × f_{SW}, where f_{SW} is the frequency programmed by the RT resistor. When an external clock is applied to MODE/SYNC pin, the internal oscillator frequency changes to external clock frequency (from the original frequency based on the RT setting) after detecting 16 external clock edges. The converter operates in PWM mode during synchronization operations. When the external clock is applied on-fly then the mode of operation changes to PWM from the initial state of DCM/PWM. When the external clock is removed on-fly then the internal oscillator frequency changes to the RT set frequency and the converter continues to operate in PWM mode. The minimum external clock pulse-width high should be greater than 50ns. See the *Mode Selection and External Synchronization (MODE/SYNC)* section in the *Electrical Characteristics* table for details.

Frequency Selection (RT)

The selection of switching frequency is a tradeoff between efficiency and component size. Low-frequency operation increases efficiency by reducing MOSFET switching losses and gate-drive losses, but requires a larger inductor and/or capacitor to maintain low output-ripple voltage. The switching frequency of the device can be programmed between 100kHz and 2.2MHz using the RT pin. Leave the RT pin unconnected to configure the default switching frequency (350kHz). The following formula can be used to find the required resistor for a given switching frequency:

$$R_{RT} = \frac{19 \times 10^3}{f_{SW}} - 1.7$$

where R_{RT} is in kΩ and f_{SW} is in kHz. Leaving the RT pin open causes the device to operate at the default switching frequency of 350kHz.

Power-Good

The IC features an open-drain power-good (PGOOD) pin. The PGOOD pin pulls low when the FB-pin voltage is outside ±10% of the 0.8V reference voltage. During soft-start, PGOOD is low. When the FB-pin voltage is within -10% of the reference voltage, PGOOD can be pulled up by an external resistor to a source voltage no greater than 6V.

Foldback Current Limit

Under overload conditions, when the output voltage falls to less than 70% of its nominal level, foldback current limiting is activated. In this mode, the peak inductor current is progressively lowered from 100% to 50% of programmed value, in proportion to the FB voltage. Foldback current-limit mode is disabled during the soft-start duration.

Latchoff Mode

In latch-off mode, the controller gets shut down once the overcurrent occurs. To restart the part, either enable (EN) or the power supply to the MAX17557 must be cycled to turn on the part again. For more information, refer to the current limit function block diagram shown in Figure 2.

Peak Current-Limit

The IC provides cycle-by-cycle peak current limiting. Under overload or short-circuit conditions, the IC regulates the cycle-by-cycle peak current-sense voltage across the current-sense pins to the peak current-limit threshold of 75mV until output voltage falls to approximately 70% of its nominal value. If the output voltage falls below 70% of its nominal value, foldback current-limit operation commences, where the peak current-limit threshold is lowered proportional to the fall in the output voltage, as measured at the FB pin.

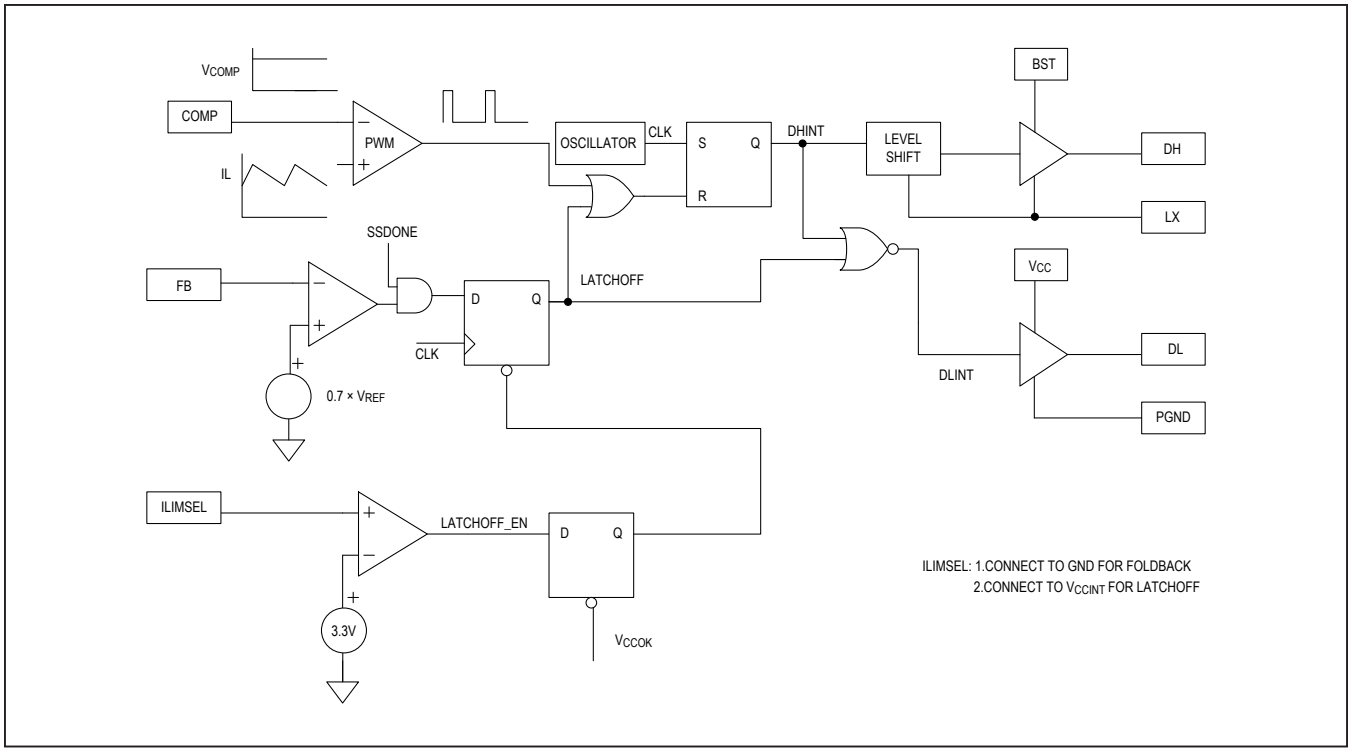


Figure 2. Current Limit Function Block Diagram

Startup Into Prebiased Output

The IC supports monotonic startup into a prebiased output voltage. During startup, if the FB pin voltage is higher than the SS pin voltage, the high-side MOSFET is held off and the low-side MOSFET is turned on for a duration of 150ns for every 10 clock cycles to refresh the BST capacitor. This causes a slightly negative average inductor current that can slowly discharge the output. Once the SS pin voltage reaches FB voltage, normal soft-start operation occurs, and the output voltage smoothly ramps up from the prebiased value.

Operating Input Voltage Range

For a step-down converter, the minimum and maximum operating input voltages for a given output voltage should be calculated as follows:

$$V_{IN\_MIN} = \frac{V_{OUT} + I_{LOAD(MAX)} \times (R_{DS(ON)\_LOW} + DCR)}{1 - f_{SW\_MAX} \times t_{DT} + DH\_MIN\_t_{ON}} + I_{LOAD(MAX)} \times (R_{DS(ON)\_HI} - R_{DS(ON)\_LOW})$$

$$V_{IN\_MAX} = \frac{V_{OUT}}{(f_{SW\_MAX} \times DH\_MIN\_t_{ON})}$$

where,

V_{OUT} = Steady-state output voltage,

$I_{LOAD(MAX)}$ = Maximum load current,

DCR = DC resistance of the inductor,

f_{SW_MAX} = Maximum switching frequency,

$R_{DS(ON)\_HI}$ and $R_{DS(ON)\_LOW}$ = On-state resistances of the high-side and low-side MOSFETs,

$DH\_MIN\_t_{ON}$ is the worst-case minimum off-time (160ns), and $DL\_MIN\_t_{ON}$ is the worst-case minimum on-time (175ns) from the *Electrical Characteristics* table.

Thermal-Shutdown Protection

Thermal-shutdown protection limits total power dissipation in the IC. When the junction temperature of the device exceeds +165°C, an on-chip thermal sensor shuts down the device, allowing it to cool. The thermal sensor turns the device on again after the junction temperature cools by 10°C. The device restarts with soft-start when recovering from thermal shutdown.

Applications Information

Setting the Input Undervoltage-Lockout Level

The EN pin can be used as input undervoltage-lockout detectors with a typical hysteresis of 100mV. As shown in Figure 1 the input voltage at which the controller of the IC turns on, can be set with a resistor divider connected to EN from IN to GND. Select R2 = 10kΩ and calculate R1 based on the following equation:

$$R1 = R2 \times \frac{(V_{INUVLO} - 1.25)}{1.25}$$

where V_{INUVLO} is the input voltage at which the controller should be enabled.

Setting the Output Voltage

The output voltage of controller is set by connecting a resistor-divider to FB from output to GND (Figure 3). Select R1 using the following equation, based on the offset introduced on the output voltage by the FB leakage. Let α be the offset introduced on the output voltage:

$$R1 \le \frac{\alpha}{I_{FB}}$$

where I_{FB} is the FB leakage current (±100nA max). For example, for V_{OUT} = 5V, α = 0.1% of V_{OUT} (= 5mV).

$$R1 \le 50k\Omega$$

Calculate R2 with the following equation:

$$R2 = \frac{R1}{\left(\frac{V_{OUT}}{0.8} - 1\right)}$$

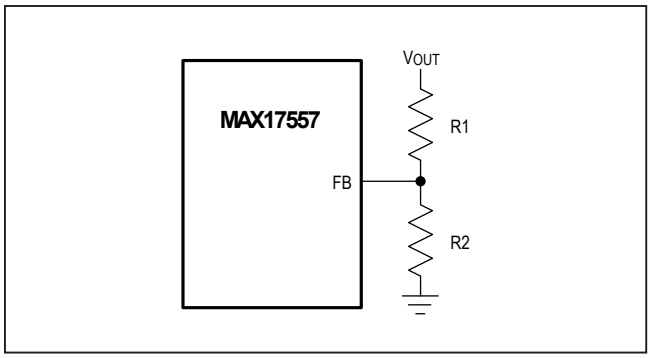


Figure 3. Output-Voltage Programming

Soft-Start Capacitor

Soft-start time is programmed by connecting a capacitor from the SS pin to GND. An internal 5µA current source charges the capacitor at the SS pin providing a linear ramping voltage for output-voltage reference. The soft-start time is calculated based on the following equation:

$$t_{SS} = C_{SS} \times \frac{0.8\,V}{5\,\mu A}$$

Soft-Stop Enable (SSTPEN)

The device's soft-stop enable pin (SSTPEN) enables or disables the soft-stop functionality during the device's power-down using the EN pin. Soft-stop time is equal to soft-start time, which can be programmed by connecting a capacitor from the SS pin to GND. Connect the SSTPEN pin to V_{CCINT} to enable the soft-stop function; connect the SSTPEN pin to GND to disable it. For more information, refer to the soft-stop function timing diagram as shown in Figure 4. The soft-stop function is available only in PWM mode.

Inductor Selection

Three key inductor parameters must be specified to selectoutput inductor:

1) Inductance (L).
2) Inductor saturation current (I_{SAT}).
3) DC resistance of inductor (DCR).

The required inductance (L) is calculated based on the ratio of inductor peak-to-peak ripple AC current to its DC average current (LIR). A good compromise between size and loss is a 30% peak-to-peak ripple current to average-current ratio (LIR = 0.3). The switching frequency, input voltage, output voltage, and selected LIR then determine the inductor value as follows:

$$L = \frac{V_{OUT} \times (1 - D)}{LIR \times I_{LOAD} \times f_{SW}}$$

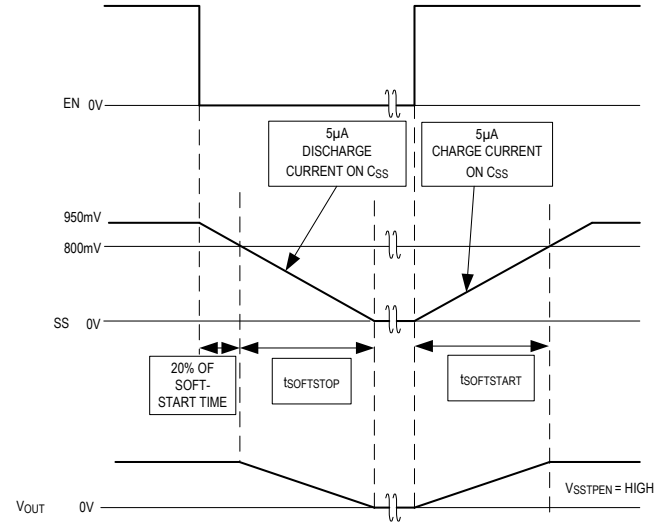
where,

V_{OUT} = Output voltage,

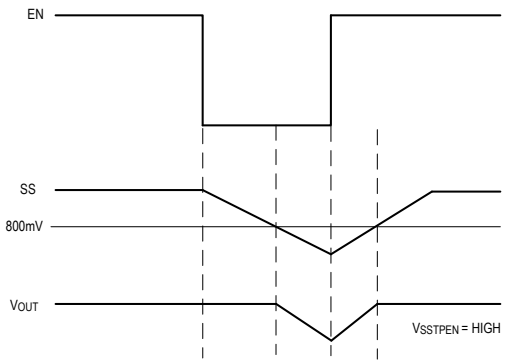
D = Operating duty cycle (= V_{OUT}/V_{IN}),

I_{LOAD} = Full-load current,

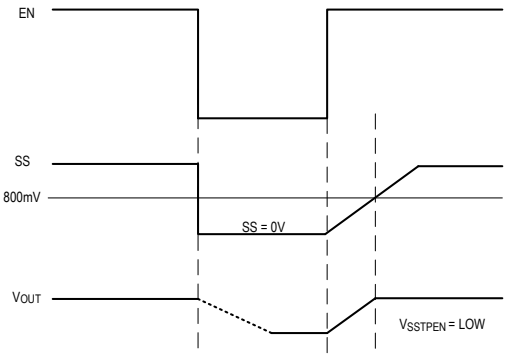
f_{SW} = Operating switching frequency.



A) THE PERFORMANCE CHARACTERISTICS WITH SOFT-STOP FUNCTION ENABLED WITH RESPECT TO EN SIGNAL POWER DOWN/UP



B) THE PERFORMANCE CHARACTERISTICS WITH SOFT-STOP FUNCTION ENABLED WITH RESPECT TO EN SIGNAL POWER DOWN/UP



C) THE PERFORMANCE CHARACTERISTICS WITH SOFT-STOP FUNCTION DISABLED WITH RESPECT TO EN SIGNAL POWER DOWN/UP

Figure 4. Soft-Stop Function Timing Diagram

The minimum inductor saturation current should be equal to or greater than maximum inductor peak current given by the following equation:

Maximum Inductor Peak Current = Maximum Load Current + ΔI_{LPK-PK} (max)

where ΔI_{LPK-PK} (max) is the maximum inductor ripple current and can be calculated as follows:

$$\Delta I_{LPK-PK}(max) = \frac{V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{INMAX}}\right)}{L \times f_{SW}}$$

Selecting an inductor with lower DCR improves efficiency, but there is a lower limit for DCR based on the minimum peak-to-peak current-sense signal required at the current sense pins, as described in the Current Sensing (CSP and CSN) section.

Current Sensing (CSP and CSN)

The CSP and CSN pins are the inputs to the internal current-sense amplifiers. The common-mode operating voltage range on these pins is 0 to 24V, enabling the IC to regulate output voltages up to a nominal 24V. Whether the current sensing is done by an external current-sense resistor or inductor DCR, the desired current-sense resistance is calculated using the following equation:

$$R_{SENSE} = \frac{V_{CS}}{I_{LOAD(MAX)} + \frac{\Delta I_{LPK-PK}(MAX)}{2}}$$

where,

R_{SENSE} = Desired current-sense resistor,

V_{CS} = 75mV (typ),

$I_{LOAD(MAX)}$ = Maximum load current.

To ensure that the application delivers full-load current over the full operating temperature range, select the minimum value for the V_{CS} parameter from the Electrical Characteristics table. It should be noted that the magnitude of current-sense ripple voltage is critical for a good signal-to-noise ratio to ensure minimum duty-cycle jitter. The worst-case current-sense ripple voltage occurs at minimum operating input voltage, and should be set in the 7mV to 12mV range. The following equation can be used to calculate the worst-case current-sense ripple voltage at the CSP, CSN pins:

$$\Delta V_{CSmin} = \Delta IL_{PK-PK(min)} \times R_{SENSE}$$

where $\Delta_{ILPK-PK(min)}$ is the minimum inductor current ripple, which occurs at minimum operating input voltage. $\Delta I_{LPK-PK(min)}$ can be calculated using the following equation:

$$\Delta I_{LPK-PK}(min) = \frac{V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{INMIN}}\right)}{L \times f_{SW}}$$

If ΔV_{CSMIN} is less than the target value, the selected output inductance should be lowered, and R_{SENSE} should be iteratively recalculated until ΔV_{CSMIN} is equal to or greater than the target value (7mV to 10mV, depending on PCB layout), and V_{CSMAX}, as calculated by the following equation is less than the selected V_{CS} from the *Electrical Characteristics* table.

$$V_{CS} = R_{SENSE} \times \left[I_{LOAD(MAX)} + \frac{\Delta I_{LPK-PK}(max)}{2}\right]$$

Because of PCB layout-related noise, operation at the minimum operating voltage should be checked for jitter before finalizing the worst-case current-sense voltage. Care should be taken to ensure that current-sense filter components should be placed close to the IC's current-sense pins. The current-sense traces should be short and differentially routed.

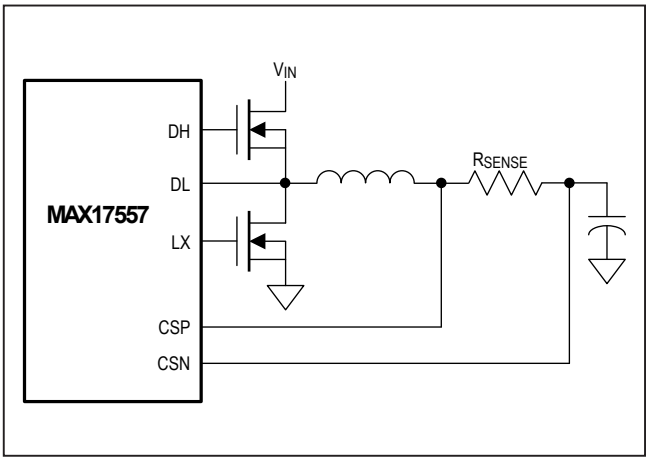


Figure 5. Typical Current Sensing Using an External Resistor

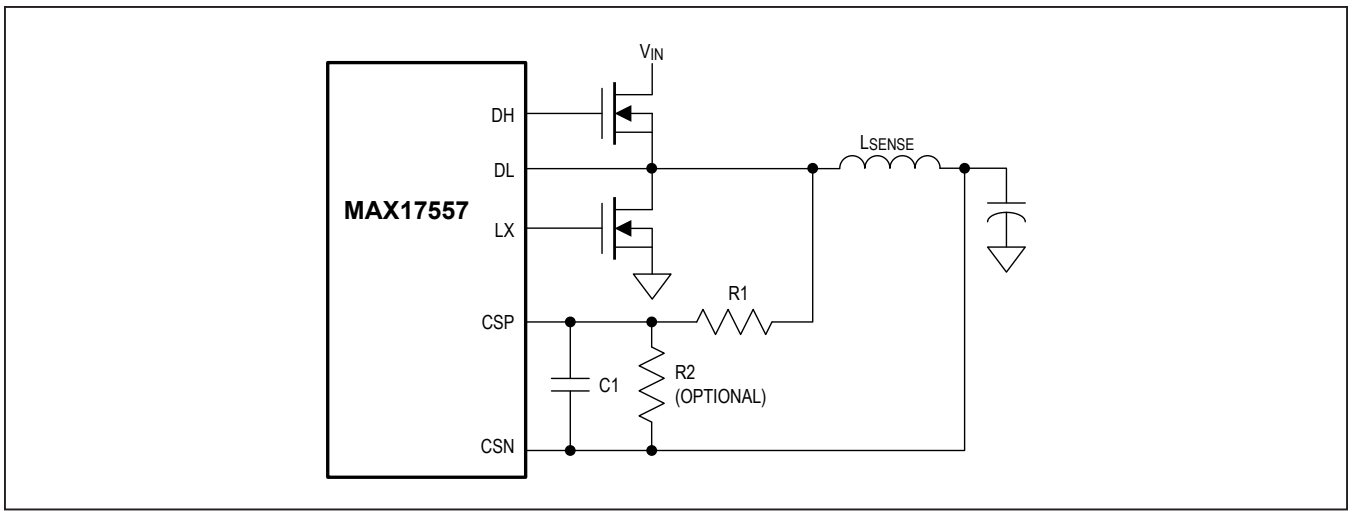


Figure 6. Typical Current Sensing Using Inductor DCR

Current-Sensing Using an External Sense Resistor

A typical current-sensing circuit using a discrete resistor is shown in Figure 5. The power rating of R_{SENSE} should be selected using the following equation for dissipation in R_{SENSE}:

$$\text{Power losses in } R_{SENSE} = \left[I_{LOAD}^{2} + \frac{\Delta IL^{2}}{12} \right] \times R_{SENSE}$$

Current-Sensing Using Inductor DCR

Current-sensing using inductor DCR current improves the system efficiency compared to current sensing using an external sense resistor. The disadvantage of DCR current sensing is that the current limit is not as accurate in comparison to the sense resistor because of wider variation of inductor DCR over temperature, and initial tolerance specified by manufacturers. A typical DCR current-sensing circuit is shown in Figure 6. Place C1 across the CS pin. Usually C1 is selected in the 0.1µF to 0.47µF range. Calculate R1 (if R2 is not used) based on following equation:

$$R1 = \frac{L}{DCR \times C1}$$

R2 is used in applications where DCR of inductor is greater than the desired current-sense resistance. In this case, calculate R1 and R2 using the following equation:

$$RP = \frac{L}{DCR \times C1}$$

where RP is the parallel combination of R1 and R2 (= [R1 x R2]/[R1 + R2]).

$$R1 = \frac{DCR \times RP}{R_{SENSE}}$$

$$R2 = \frac{R1 \times RP}{R1 - RP}$$

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. Use low-ESR ceramic capacitors at the input. Calculate the input capacitance required for a specified input-ripple ΔV_{IN} using the following equations, by neglecting the ripple component due to ESR of input capacitor:

$$C_{IN} = \frac{I_{LOAD} \times D \times (1 - D)}{\eta \times \Delta V_{IN} \times f_{SW}}$$

where,

$D = V_{OUT}/V_{IN}$

η = Efficiency of power conversion.

The input capacitor RMS current requirement (C_{INRMS}) can be calculated by the following equation:

$$CIN_{RMS} = I_{LOAD(MAX)} \times \sqrt{D \times (1 - D)}$$

where $I_{LOAD(MAX)}$ is the maximum value of load current, $D = V_{OUT}/V_{IN}$.

Output Capacitor Selection

The key selection parameters for the output capacitor are capacitance value, ESR, and voltage rating. These parameters affect the overall stability, output-ripple voltage, and transient response. The steady-state output ripple (ΔV_{OUTSS}) has two components (by neglecting the ESL of the output capacitors): one component is due to the voltage drop across the ESR (ΔV_{OUTESR_SS}) and the other component is due to the variation in charge stored in the output capacitor (ΔV_{OUTQ_SS}). By neglecting the output-voltage drop due to ESL of output capacitor, approximate output voltage ripple under steady-state is given by:

$$\Delta V_{OUTSS} \approx \Delta V_{OUTESR\_SS} + \Delta V_{OUTQ\_SS}$$

where ΔV_{OUTSS} is the output-voltage ripple under steady state:

$$\Delta V_{OUTESR\_SS} = \Delta IL_{PK-PK} \times ESR$$

$$\Delta V_{OUTQ\_SS} = \frac{\Delta IL_{PK-PK}}{8 \times f_{SW} \times C_{OUT}}$$

Calculate the required C_{OUT} and ESR based on the above equations. For ceramic output capacitors, V_{OUTQ_SS} contributes to approximately 80% of the total output-ripple voltage, ΔV_{OUTQSS_SS}. For electrolytic output capacitors, ΔV_{OUTQ_SS} contributes approximately 50% of the total output-voltage ripple. Low-ESR capacitors should be used.

The output capacitors are also usually sized to support a step load of 50% of the maximum output current in the application, so the output-voltage deviation is contained to 3% of the output voltage change. The minimum required output capacitance can be calculated as follows:

$$C_{OUT} = \frac{1}{2} \times \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

$$t_{RESPONSE} \cong \frac{0.33}{f_{CO}}$$

where,

I_{STEP} = Load current step

$t_{RESPONSE}$ = Response time of the controller

ΔV_{OUT} = Allowable output-voltage deviation

f_{CO} = Crossover frequency

f_{SW} = Switching frequency

Desired crossover frequency that should be chosen between $f_{SW}/10$ and $f_{SW}/20$, subject to a maximum of 70kHz. Actual derating of ceramic capacitors with DC-bias voltage must be considered while selecting the output capacitor. Derating curves are available from all major ceramic capacitor manufacturers.

Select the highest value of capacitance upon calculating the required capacitance from both the methods.

Loop Compensation

The IC uses an internal transconductance error amplifier with its inverting input and output available to the user for external frequency compensation. The output capacitor and compensation network determine the loop stability for a given output inductor and output capacitor. The controller uses a peak current-mode control scheme that regulates the output voltage by forcing the required current through the external inductor. Current-mode control eliminates the double pole in the feedback loop caused by the inductor and output capacitor in the case of voltage-mode control, resulting in a smaller phase shift and requiring less elaborate error-amplifier compensation. Typical type-2 compensation used with peak current-mode control is shown in Figure 7. Calculate the compensation resistor (R_Z) using the following equation:

$$R_Z = \frac{2 \times \pi \times f_{CO} \times C_{OUT} \times G_{CS} \times R_{SENSE}}{g_M \times G_{FB}}$$

where,

f_{CO} = Crossover frequency

C_{OUT} = Output capacitance

G_{CS} = Current-sense amplifier gain

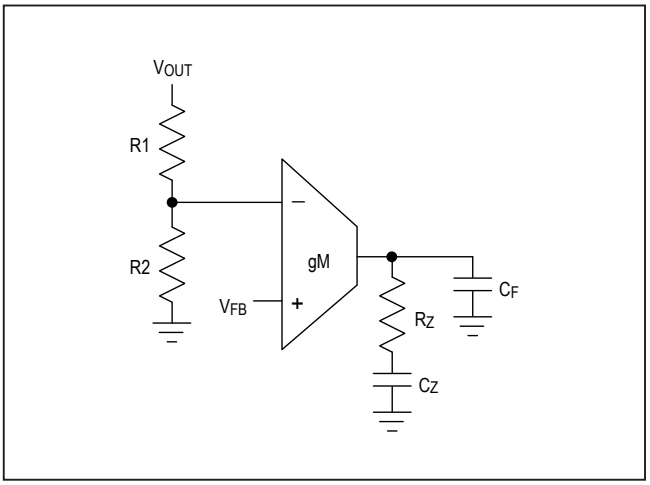


Figure 7. Loop Compensation

R_{SENSE} = Effective current-sense resistor across the CSP and CSN pins

g_M = Internal transconductance amplifier gain

G_{FB} = Output-voltage feedback divider gain, which is equal to (0.8V/output voltage)

C_Z is calculated using the following equation:

$$C_Z = \frac{1}{2 \times \pi \times f_{P\_Load} \times R_Z}$$

where f_{P_Load} is the load-pole frequency approximated by the following equation:

$$f_{P\_Load} = \frac{1}{2 \times \pi \times C_{OUT} \times \left(\frac{V_{OUT}}{I_{LOAD}}\right)}$$

Calculate C_F using the following equation:

$$C_F = \frac{1}{2 \times \pi \times R_Z \times f_{P\_EA}}$$

where f_{P_EA} is the pole frequency created by R_Z and C_F given by the minimum of ESR zero frequency calculated by the following equation or $f_{SW/2}$.

$$f_{Z\_ESR} = \frac{1}{2 \times \pi \times C_{OUT} \times ESR}$$

When the output capacitor is composed of n identical capacitors in parallel, the resulting C_{OUT} = n x C_{OUT} (each), and ESR = ESR (each)/n. Note that the location of f_{Z_ESR} for a parallel combination of same capacitors is the same as for an individual capacitor.

Bootstrap Capacitor Selection

The selected high-side nMOSFET determines the appropriate bootstrap capacitance values according to the following equation:

$$C_{BST} = \frac{\Delta Q_{Gate}}{\Delta V_{BST}}$$

where ΔQ_{Gate} is the total gate charge of the high-side MOSFET and ΔV_{BST} is the voltage variation allowed on the high-side MOSFET driver after turn-on. Choose ΔV_{BST} so the available gate-drive voltage is not significantly degraded (e.g., ΔV_{BST} = 100mV) when determining C_{BST}. The bootstrap capacitor should be a low-ESR ceramic capacitor. A minimum value of 100nF is recommended.

MOSFET Selection

The controller drives two external logic-level nMOSFETs as the circuit switch elements. The key selection parameters to choose these MOSFETs include:

- On-resistance ($R_{DS(ON)}$)
- Maximum drain-to-source voltage ($V_{DS(MAX)}$)
- Miller Plateau voltage on HSMOSFET Gate (V_{MIL})
- Total gate charge (Q_{Gate})
- Output capacitance (C_{OSS})
- Power-dissipation rating and package thermal resistance

Both nMOSFETs must be logic-level types with guaranteed on-resistance specifications at V_{GS} = 4.5V. The duty cycles for the high-side and low-side external MOSFETs can be calculated as follows:

$$D = \frac{V_{OUT}}{V_{IN}}$$

High-side MOSFET duty cycle:

Low-side MOSFET duty cycle = 1 – D

High-side MOSFET losses can be approximated using following formula:

$$P_{HSMOSFET} = P_{HSMOSFET\_Conduction} + P_{HSMOSFET\_Switching}$$

$$P_{HSMOSFET\_Conduction} = I_{LOAD(MAX)}^2 \times R_{DS(ON)\_HS} \times D$$

$$P_{HSMOSFET\_Switching} = f_{SW} \times \left[\frac{V_{IN} \times I_{LOAD(MAX)}}{2} \times \frac{Q_{SW} \times R_{DR}}{V_{CCINT} - V_{MIL}}\right] + \left[V_{IN} \times Q_{rr}\right] + \left[\frac{1}{2} \times C_{OSSHS} \times V_{IN}^2\right] + \left[\frac{1}{2} \times C_{OSSLS} \times V_{IN}\right]^2$$

where,

f_{SW} = Operating switching frequency,

$I_{LOAD(MAX)}$ = Maximum load current in the application,

Q_{SW} = Switching charge of the high-side MOSFET, which can be obtained from the MOSFET data sheet,

R_{DR} = Sum of the DH pin driver resistance and the HSMOSFET internal gate resistance,

V_{MIL} - V_{GS} on HSMOSFET gate that produces $I_{DS} = I_{LOAD(MAX)}$

Q_{rr} = Reverse-recovery charge of low-side MOSFET body diode (if external Schottky is not placed across lowside MOSFET),

C_{OSSHS} = Effective output capacitance of the high-side MOSFET,

C_{OSSLS} = Effective output capacitance of the low-side MOSFET.

Low-side MOSFET losses can be approximated using the following formula:

$$P_{LSMOSFET} = I_{LOAD(MAX)}^2 \times R_{DS(ON)\_LS} \times (1-D) + V_D \times I_{LOAD(MAX)} \times t_{DT} \times f_{SW} \times 2$$

where V_D is the forward-drop of the LSMOSFET body diode and t_{DT} is the dead time from the *Electrical Characteristics* table.

Take the $R_{DS(ON)}$ variation with temperature into account while calculating the above losses and ensure that the losses of each MOSFET do not exceed their power rating. Using a low Q_{rr} Schottky diode across the low side MOSFET reduces the high-side MOSFET losses.

Power Dissipation within the MAX17557

Gate-charge losses are dissipated by the drivers. Therefore, the gate-driver current taken from the internal LDO regulator and resulting power dissipation must be checked. If V_{CCEXT} is not used to power V_{CCINT}, calculate the approximate IC losses as follows:

$$P_{MAX17557} = V_{IN} \times \left[(Q_{Gate} \times f_{SW}) + I_{QNS}\right]$$

If V_{CCEXT} is used to power the V_{CCINT}, use the following equation to calculate the approximate IC losses:

$$P_{MAX17557} = V_{CCEXT} \times \left[(Q_{Gate} \times f_{SW}) + I_{QNS}\right]$$

where QGate is the total gate charge of high-side and low-side MOSFETs and I_{QNS} is the supply current given in the *Electrical Characteristics* table.

Calculate the IC junction temperature using the following equation and ensure that this value does not exceed +125°C:

$$T_J = \left[P_{MAX17557} \times Rth_{JA}\right] + T_A$$

where,

T_J = IC junction temperature,

$P_{MAX17557}$ = Power losses in the IC,

Rth_{JA} = IC junction-to-ambient thermal resistance, which is typically 39°C/W for a multilayer board,

T_A = Maximum ambient temperature.

PCB Layout Guidelines

Careful PCB layout is critical to achieve low losses, low output noise, and clean and stable operation. Use the following guidelines for PCB layout:

- Keep input bypass capacitors as close as possible across the drain of the high-side MOSFET and source of the low-side MOSFET.
- If external Schottky diodes are used across the low-side MOSFET, keep the Schottky very close and right across the low-side MOSFET.
- Keep IN, V_{CCINT}, V_{CCEXT} bypass capacitors and the BST capacitor near the IC pins.
- Route high-speed switching nodes (BST, LX, DH, and DL) away from the sensitive analog areas (RT, COMP, CS, and FB).
- The gate current traces must be short and wide. Use multiple small vias to route these signals if routed from one layer of the PCB to another layer.
- Route current-sense lines parallel, short, and next to each other to minimize the loop formed by these lines.
- Keep current-sense filter capacitors nearer to IC current-sense pins and on the same side of the IC.
- Group all GND-referred and feedback components close to the IC.
- Keep the FB and compensation-network nets as small as possible to prevent noise pickup.
- If possible, place all power components on the top side of the board and run the power-stage currents using traces or copper fills on the top side only, without adding vias.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PCBs (2oz or higher) to enhance efficiency and minimize trace inductance and resistance.
- On the top side, lay out a large PGND copper area for the output and connect the bottom terminals of the input bypass capacitors, output capacitors, and the source terminals of the low-side MOSFET to that area.
- Refer to the MAX17557 evaluation kit data sheet PCB layout for an example.

Typical Application Circuit

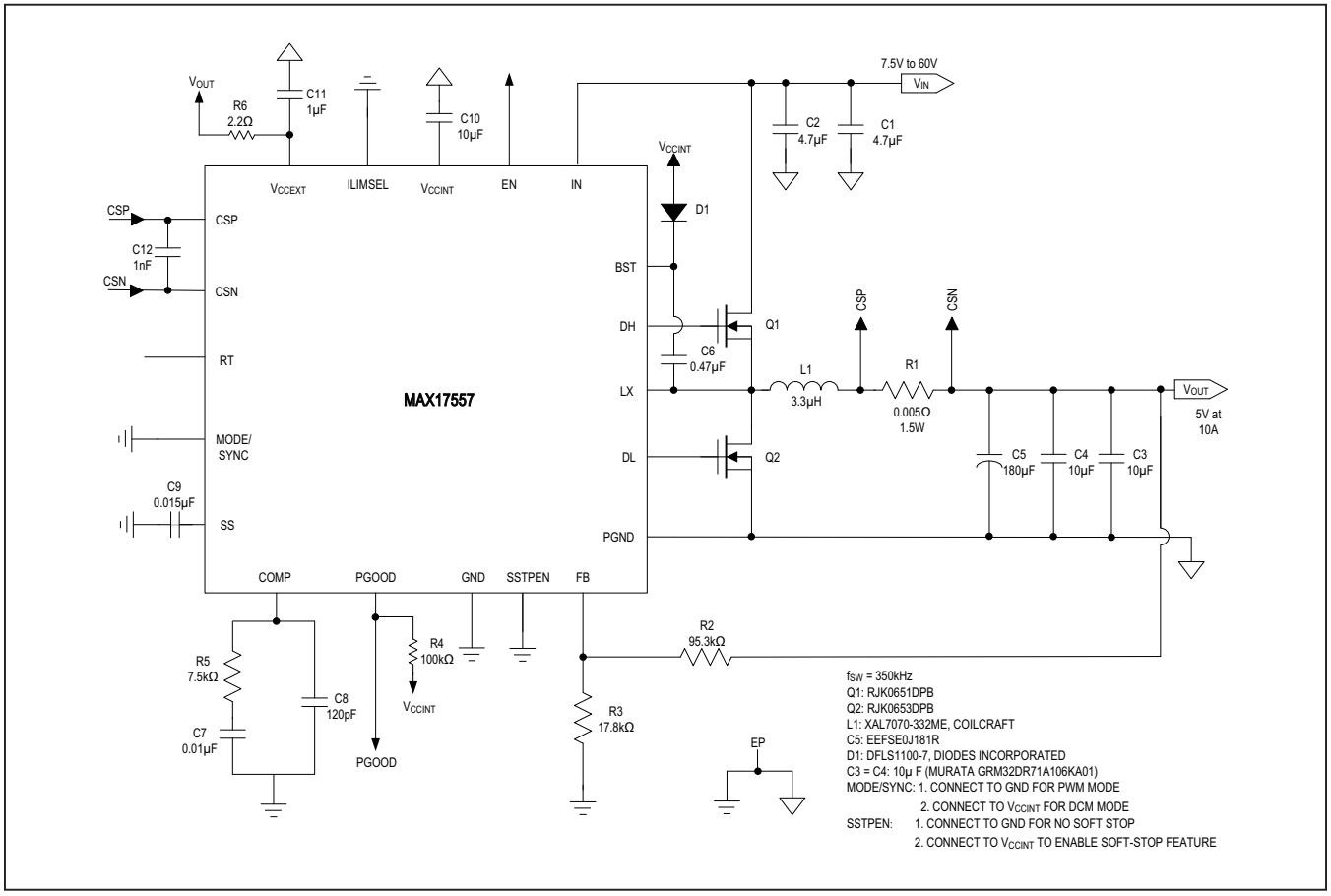


Figure 8. Wide-Input Voltage, High-Efficiency 5V Output Buck Converter with Resistor-Based Current Sensing (R1).

Typical Application Circuit (continued)

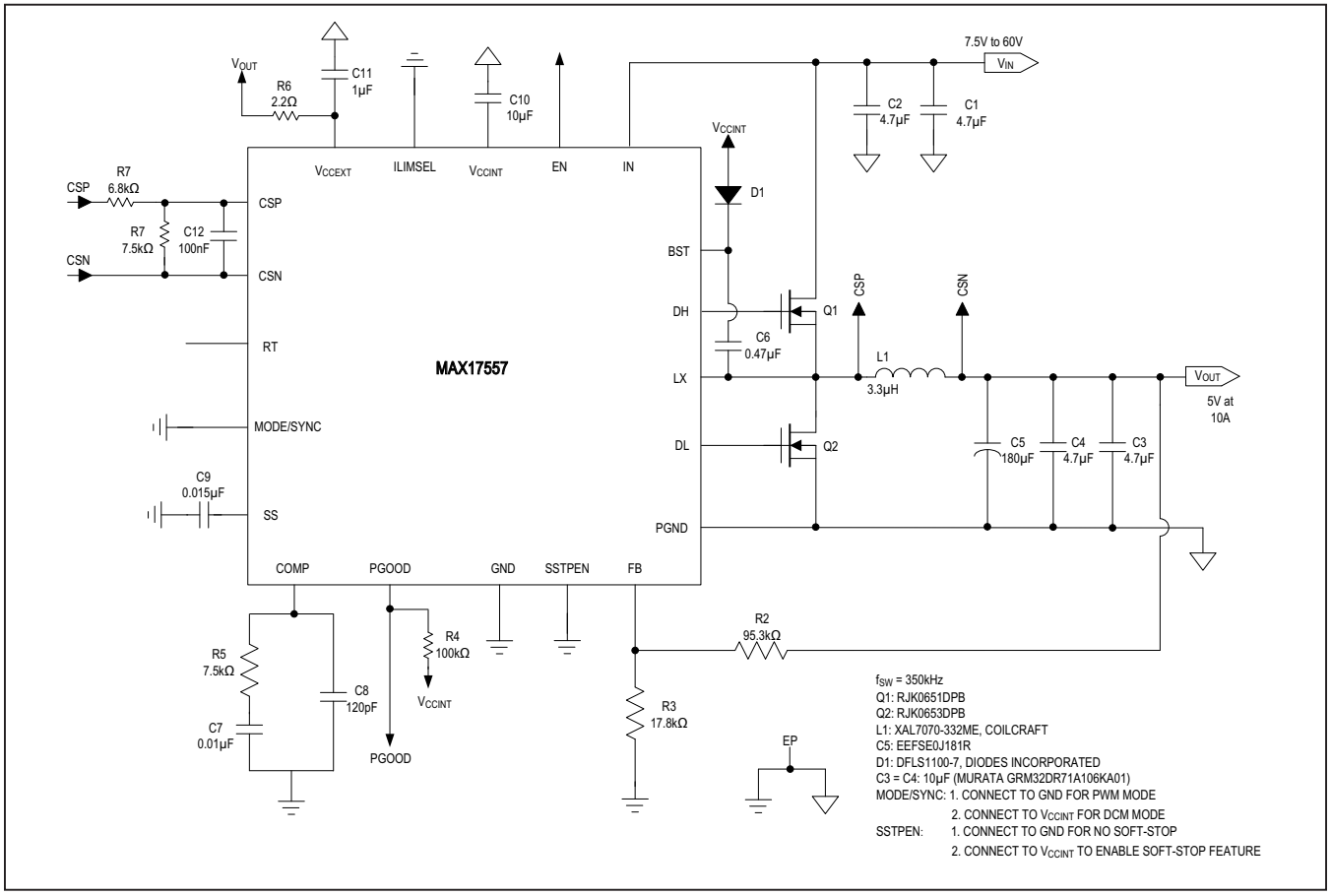


Figure 9. Wide Input Voltage, High-Efficiency 5V Output Buck Converter with Inductor DCR Current Sensing (L1).

Chip Information

PROCESS: BiCMOS

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17557ATP+	-40°C to +125°C	20 TQFN

+Denotes a lead(Pb)-free/RoHS-compliant package.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/17	Initial release	—
1	3/18	Updated the *Detailed Description, Benefits and Features, Absolute Maximum Ratings,* and *Typical Operating Characteristics* sections. Updated the *Electrical Characteristics* and *Pin Description* tables, and *Pin Configuration*. Replaced all TOCs, *Functional (or Block) Diagram*, and *Typical Application Circuits* (Figures 7 and 8). Added the *Mode Selection and External Synchronization (MODE/SYNC), DCM Mode, PWM Mode, External Frequency Synchronization,* and *Soft-Stop Enable (SSTPEN)* sections.	1–9, 11–19, 21–22
2	5/18	Updated the *Absolute Maximum Ratings, Detailed Description, Internal LDO (V_{CCINT}), Mode Selection and External Synchronization (MODE/SYNC), Latchoff Mode, Setting the Output Voltage, Soft-Stop Enable (SSTPEN),* and *Current-Sensing Using an External Sense Resistor* sections. Updated the *Electrical Characteristics* and *Pin Description* tables, *Pin Configuration,* TOC07_TOC09, and *Functional (or Block) Diagram.* Added new Figures 2 and 4 and renumbered existing figures and references.	2, 4, 6–7 9–12, 14–18

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