MAX17760

4.5V to 76V, 300mA, High-Efficiency, Synchronous Step-Down DC-DC Converter

General Description

The Himalaya series of voltage regulator ICs, power modules, and chargers enable cooler, smaller, and simpler power supply solutions. The MAX17760 is a high-efficiency, high-voltage, Himalaya synchronous step-down DC-DC converter with integrated MOSFETs operating over an input-voltage range of 4.5V to 76V. The device can deliver up to 300mA current. Output voltage is programmable from 0.8V up to 88% of input voltage (V_{IN}). Built-in control loop compensation eliminates the need for external components.

The MAX17760 features a peak-current-mode control architecture. The device can be operated in either the forced pulse-width modulation (PWM) or pulse-frequency modulation (PFM) control schemes. Forced PWM mode provides constant frequency operation at all loads for frequency sensitive applications, while PFM mode provides superior light-load efficiency by skipping pulses. The device integrates an open drain $\overline{\text{RESET}}$ output voltage monitor, adjustable input undervoltage lockout (EN/UVLO) and programmable soft-start.

The feedback voltage regulation accuracy over -40°C to +125°C is +1.6% to -1.7%. The MAX17760 is available in a compact 12-pin (3mm x 3mm) TDFN package. Simulation models are available.

Applications

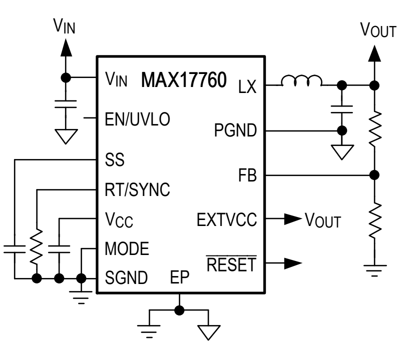
- Industrial Control Power Supplies
- General Purpose Point-of-Load
- Distributed Supply Regulation
- Base Station Power Supplies
- Wall Transformer Regulation
- High Voltage Single-Board Systems

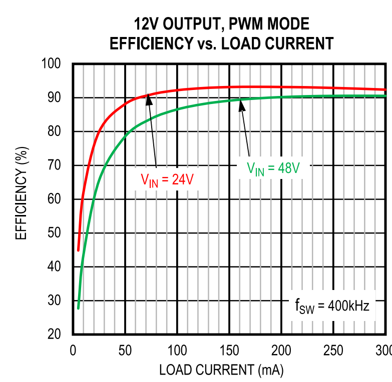
Benefits and Features

- Reduces External Components and Total Cost
  - No Schottky—Synchronous Operation
  - Internal Compensation Components
  - All-Ceramic Capacitors, Compact Layout
- Reduces Number of DC-DC Regulators to Stock
  - Wide 4.5V to 76V Input
  - Adjustable Output Range from 0.8V up to 88% of V_{IN}
  - Up to 300mA Output Current
  - 200kHz, 300kHz, 400kHz, and 600kHz Programmable Switching Frequency with External Clock Synchronization.
- Reduces Power Dissipation
  - 93% Peak Efficiency
  - PFM Mode Enables Enhanced Light-Load Efficiency
  - EXTVCC Bootstrap Input for Improved Efficiency
  - 5μA Shutdown Current
- Operates Reliably in Adverse Industrial Environments
  - Built-in Hiccup Mode Overload Protection
  - Programmable Soft-Start and Prebiased Power-up
  - Built-in Output-Voltage Monitoring with $\overline{\text{RESET}}$
  - Programmable EN/UVLO Threshold
  - Overtemperature Protection
  - CISPR 22 Class B Compliant
  - Wide -40°C to +125°C Ambient Operating Temperature Range/ -40°C to +150°C Junction Temperature Range

***Ordering Information** appears at end of data sheet.*

Simplified Application Circuit





Absolute Maximum Ratings

V_{IN} to SGND .... -0.3V to +80V
EN/UVLO to SGND .... -0.3 to min((V_{IN} + 0.3V), 26V)
EXTVCC to SGND .... -0.3V to +26V
LX to PGND .... -0.3 to (V_{IN} + 0.3V)
FB, RESET, SS, MODE, V_{CC}, RT/SYNC to SGND . -0.3V to +6V
PGND to SGND .... -0.3V to +0.3V
LX Total RMS Current .... ±0.6A
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 24.4mW/°C above +70°C.) 1951.2mW
Output Short-Circuit Duration .... Continuous
Operating Temperature Range (Note 1) .... -40°C to +125°C
Junction Temperature .... +150°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering, 10s) .... +300°C
Soldering Temperature (reflow) .... +260°C

Note 1: Junction temperature greater than +125°C degrades operating lifetimes.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

12 TDFN

Package Code	TD1233+1C
Outline Number	21-0664
Land Pattern Number	90-0397
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	41°C/W
Junction to Case (θ_{JC})	8.5°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{IN} = 24V, EN/UVLO = unconnected, $R_{RT/SYNC}$ = 69.8kΩ (f_{SW} = 400 kHz), V_{MODE} = V_{PGND} = V_{SGND} = V_{EXTVCC} = 0V, C_{VCC} = 1µF, V_{FB} = 1V, LX = SS = RESET = unconnected, T_A = T_J = -40°C to 125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (V_{IN})						
Input Voltage Range	V_{IN}		4.5		76	V
Input Shutdown Current	I_{IN-SH}	$V_{EN/UVLO}$ = 0V (shutdown mode)	2.5	5	10	µA
Input Quiescent Current	I_{Q_PFM}	MODE = Unconnected, V_{EXTVCC} = 5V		75		µA
	I_{Q_PWM}	V_{FB} = 0.75V, Normal switching mode		2.5		mA
ENABLE/UVLO (EN/UVLO)						
EN/UVLO Threshold	V_{ENR}	$V_{EN/UVLO}$ rising	1.19	1.215	1.24	V
	V_{ENF}	$V_{EN/UVLO}$ falling	1.09	1.115	1.14	
	V_{ENT}	$V_{EN/UVLO}$ falling, true shutdown		0.7		
EN/UVLO Pullup Current	$I_{EN/UVLO}$	$V_{EN/UVLO}$ = 1.215V	2.2	2.5	2.8	µA

Electrical Characteristics (continued)

(V_{IN} = 24V, EN/UVLO = unconnected, $R_{RT/SYNC}$ = 69.8kΩ (f_{SW} = 400 kHz), V_{MODE} = V_{PGND} = V_{SGND} = V_{EXTVCC} = 0V, C_{VCC} = 1μF, V_{FB} = 1V, LX = SS = $\overline{RESET}$ = unconnected, T_A = T_J = -40°C to 125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LINEAR REGULATOR (V_{CC})						
V_{CC} Output Voltage Range	V_{CC}	6V ≤ V_{IN} ≤ 76V, 0mA < I_{VCC} < 5mA	4.75	5	5.25	V
V_{CC} Current Limit	$I_{VCC-MAX}$	V_{CC} = 4.3V, V_{IN} = 12V	13	26	52	mA
V_{CC} Dropout Voltage	V_{CC-DO}	V_{IN} = 4.5V, I_{VCC} = 5mA			0.27	V
V_{CC} UVLO	V_{CC-UVR}	V_{CC} rising	4.05	4.2	4.35	V
	V_{CC-UVF}	V_{CC} falling	3.65	3.8	3.95	
EXTVCC Operating Voltage Range			4.85		24	V
EXTVCC Switchover Threshold		V_{EXTVCC} rising	4.65	4.74	4.85	V
		Hysteresis		0.3		
EXTVCC Dropout Voltage	EXTVCC-DO	V_{EXTVCC} = 4.75V, I_{VCC} = 5mA			0.1	V
EXTVCC Current Limit	$I_{VCC-MAX}$	V_{CC} = 4.3V, V_{EXTVCC} = 5V	13	21	34	mA
POWER MOSFETS						
High-Side pMOS On-Resistance	R_{DS-ONH}	I_{LX} = 0.15A, sourcing		1.8	3.6	Ω
Low-Side nMOS On-Resistance	R_{DS-ONL}	I_{LX} = 0.15A, sinking		0.55	1.1	Ω
LX Leakage Current	I_{LX-LKG}	V_{LX} = (V_{PGND} + 1V) to (V_{IN} - 1V), T_A = +25°C	-1		+1	μA
SOFT-START (SS)						
Charging Current	I_{SS}		4.7	5	5.3	μA
FEEDBACK (FB)						
FB Regulation Voltage	V_{FB-REG}	V_{MODE} = 0V (PWM mode)	0.788	0.802	0.815	V
		MODE = Unconnected (PFM mode)	0.788	0.813	0.827	
FB Input Leakage Current	I_{FB}	T_A = +25°C	-100		+100	nA
CURRENT LIMIT						
Peak Current Limit Threshold	$I_{PEAK-LIMIT}$		532	640	755	mA
Negative Current Limit Threshold	$I_{SINK-LIMIT}$	V_{MODE} = 0V (PWM mode)	238	270	302	mA
		MODE = Unconnected (PFM mode)		2.5		
PFM Current Limit	I_{PFM}	MODE = Unconnected	185	240	310	mA
MODE						
PFM Mode Threshold	V_{TH_PFM}	Rising	1	1.22	1.44	V
		Hysteresis		0.175		
MODE Pullup Current at Power-Up				2.5		μA

Electrical Characteristics (continued)

(V_{IN} = 24V, EN/UVLO = unconnected, $R_{RT/SYNC}$ = 69.8kΩ (f_{SW} = 400 kHz), V_{MODE} = V_{PGND} = V_{SGND} = V_{EXTVCC} = 0V, C_{VCC} = 1μF, V_{FB} = 1V, LX = SS = $\overline{RESET}$ = unconnected, T_A = T_J = -40°C to 125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 2)

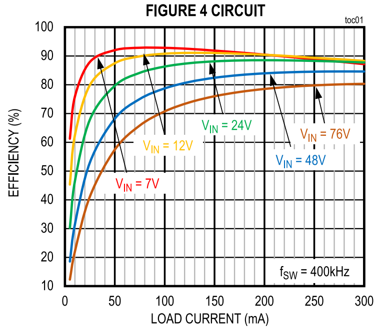
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR (RT/SYNC)						
Switching Frequency	f_{SW}	$R_{RT/SYNC}$ = 140kΩ	180	200	220	kHz
		$R_{RT/SYNC}$ = 93.1kΩ	270	300	330	
		$R_{RT/SYNC}$ = 69.8kΩ	360	400	440	
		$R_{RT/SYNC}$ = 46.4kΩ	540	600	660	
Switching Frequency Adjustable Range			200		600	kHz
Minimum On-Time	t_{ON-MIN}			70	110	ns
Maximum Duty Cycle	D_{MAX}		88	93	97	%
Hiccup Timeout Period	$t_{HIC-TOUT}$			51		ms
SYNC Frequency Capture Range			1.15 x f_{SW} (typ)		1.4 x f_{SW} (typ)	
SYNC Threshold	V_{IH}		2.1			V
	V_{IL}				0.8	
$\overline{RESET}$						
$\overline{RESET}$ Output Level Low		$I_{\overline{RESET}}$ = 10mA			0.4	V
$\overline{RESET}$ Output Leakage Current		T_A = +25°C			1	μA
FB Threshold for $\overline{RESET}$ Deassertion	V_{FB-OKR}	V_{FB} rising		95		%
FB Threshold for $\overline{RESET}$ Assertion	V_{FB-OKF}	V_{FB} falling		92		%
$\overline{RESET}$ Delay after FB Reaches 95% Regulation				2.1		ms
THERMAL SHUTDOWN						
Thermal Shutdown Threshold		Temperature rising		160		°C
		Hysteresis		20		

Note 2: Electrical specifications are production tested at T_A = +25ºC. Specifications over the entire operating temperature range are guaranteed by design and characterization.

Typical Operating Characteristics

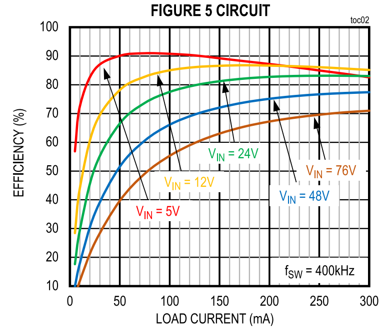
(V_{IN} = 24V, V_{SGND} = V_{PGND} = 0V, C_{VCC} = 1µF, EN/UVLO = unconnected, C_{SS} = 5600pF, T_A = +25°C, unless otherwise noted. All voltages are referenced to SGND, unless otherwise noted.)

EFFICIENCY vs. LOAD CURRENT
FIGURE 4 CIRCUIT



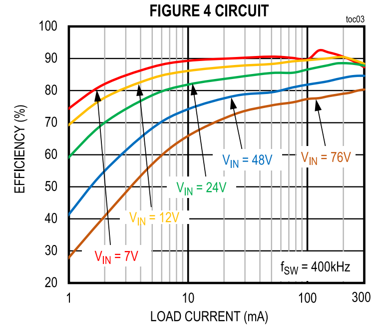
CONDITIONS: 5V OUTPUT, PWM MODE

EFFICIENCY vs. LOAD CURRENT
FIGURE 5 CIRCUIT



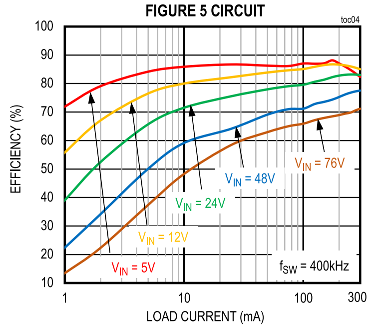
CONDITIONS: 3.3V OUTPUT, PWM MODE

EFFICIENCY vs. LOAD CURRENT
FIGURE 4 CIRCUIT



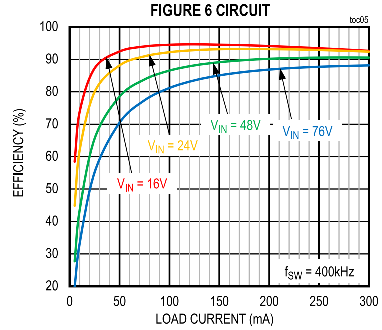
CONDITIONS: 5V OUTPUT, PFM MODE

EFFICIENCY vs. LOAD CURRENT
FIGURE 5 CIRCUIT



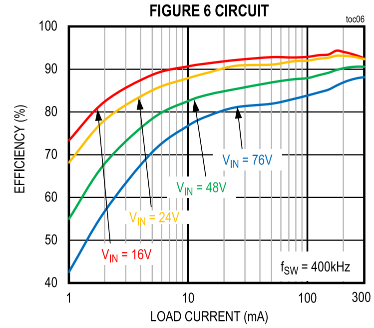
CONDITIONS: 3.3V OUTPUT, PFM MODE

EFFICIENCY vs. LOAD CURRENT
FIGURE 6 CIRCUIT



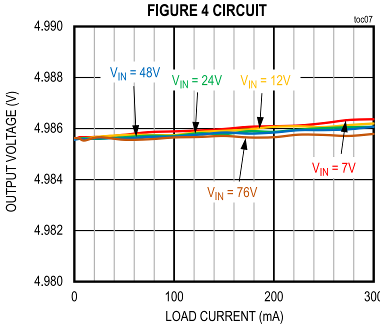
CONDITIONS: 12V OUTPUT, PWM MODE

EFFICIENCY vs. LOAD CURRENT
FIGURE 6 CIRCUIT



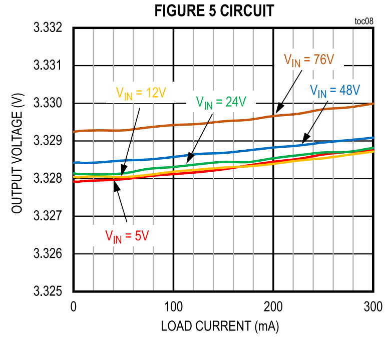
CONDITIONS: 12V OUTPUT, PFM MODE

LINE AND LOAD REGULATION
FIGURE 4 CIRCUIT



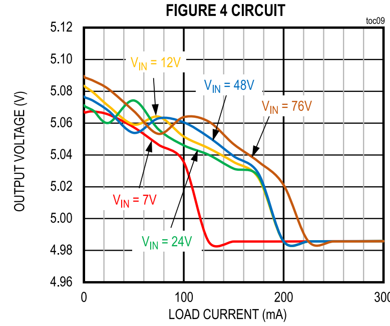
CONDITIONS: 5V OUTPUT, PWM MODE

LINE AND LOAD REGULATION
FIGURE 5 CIRCUIT



CONDITIONS: 3.3V OUTPUT, PWM MODE

LINE AND LOAD REGULATION
FIGURE 4 CIRCUIT

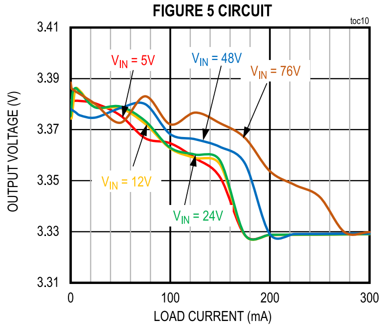


CONDITIONS: 5V OUTPUT, PFM MODE

Typical Operating Characteristics (continued)

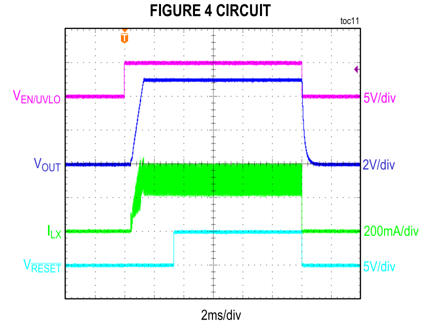
(V_{IN} = 24V, V_{SGND} = V_{PGND} = 0V, C_{VCC} = 1μF, EN/UVLO = unconnected, C_{SS} = 5600pF, T_A = +25°C, unless otherwise noted. All voltages are referenced to SGND, unless otherwise noted.)

LINE AND LOAD REGULATION
FIGURE 5 CIRCUIT



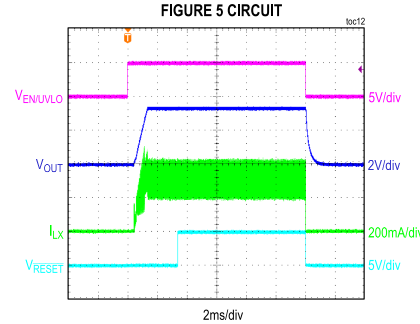
CONDITIONS: 3.3V OUTPUT, PFM MODE

SOFT-START/SHUTDOWN THROUGH EN/UVLO
FIGURE 4 CIRCUIT



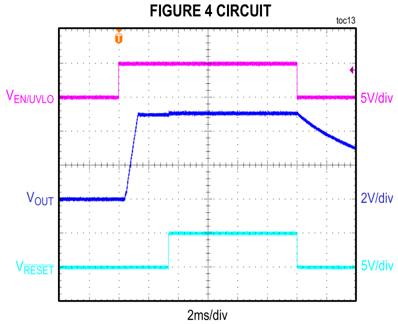
CONDITIONS: 5V OUTPUT, PWM MODE, 16.67Ω LOAD

SOFT-START/SHUTDOWN THROUGH EN/UVLO
FIGURE 5 CIRCUIT



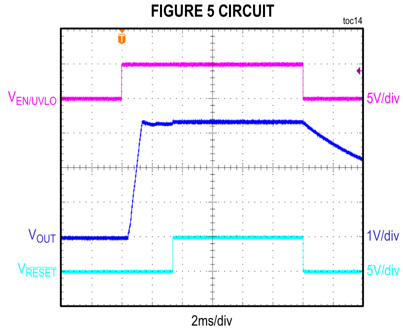
CONDITIONS: 3.3V OUTPUT, PWM MODE, 11Ω LOAD

SOFT-START/SHUTDOWN THROUGH EN/UVLO
FIGURE 4 CIRCUIT



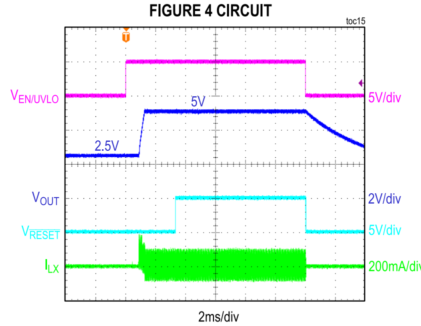
CONDITIONS: 5V OUTPUT, PFM MODE, 1000Ω LOAD

SOFT-START/SHUTDOWN THROUGH EN/UVLO
FIGURE 5 CIRCUIT



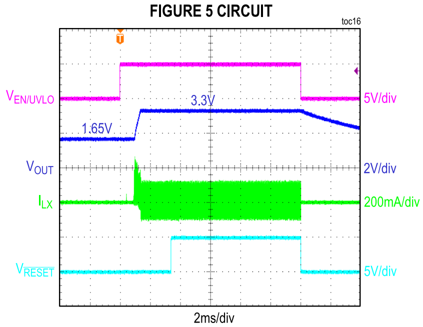
CONDITIONS: 3.3V OUTPUT, PFM MODE, 660Ω LOAD

SOFT-START WITH PREBIAS OF VOLTAGE 2.5V
FIGURE 4 CIRCUIT



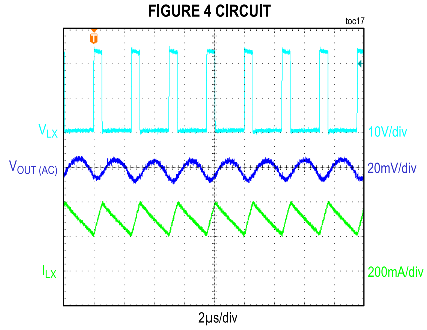
CONDITIONS: 5V OUTPUT, PWM MODE, 1000Ω LOAD

SOFT-START WITH PREBIAS OF VOLTAGE 1.65V
FIGURE 5 CIRCUIT



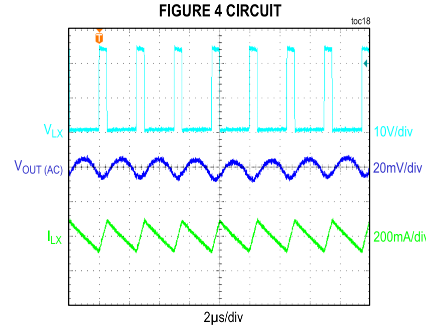
CONDITIONS: 3.3V OUTPUT, PWM MODE, 660Ω LOAD

STEADY-STATE PERFORMANCE
FIGURE 4 CIRCUIT



CONDITIONS: 5V OUTPUT, PWM MODE, 300mA LOAD

STEADY-STATE PERFORMANCE
FIGURE 4 CIRCUIT

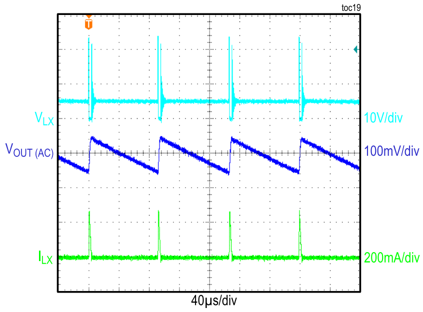


CONDITIONS: 5V OUTPUT, PWM MODE, NO LOAD

Typical Operating Characteristics (continued)

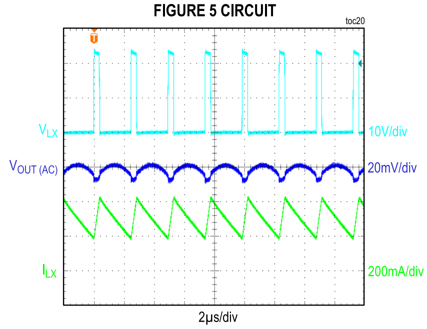
(V_{IN} = 24V, V_{SGND} = V_{PGND} = 0V, C_{VCC} = 1μF, EN/UVLO = unconnected, C_{SS} = 5600pF, T_A = +25°C, unless otherwise noted. All voltages are referenced to SGND, unless otherwise noted.)

STEADY-STATE PERFORMANCE
FIGURE 4 CIRCUIT



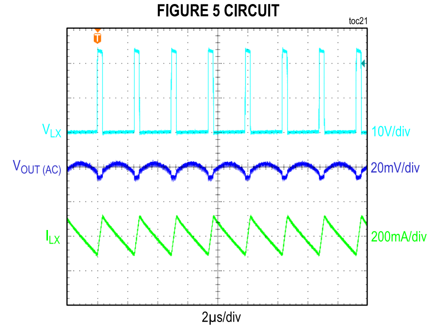
CONDITIONS: 5V OUTPUT, PFM MODE, 5mA LOAD

STEADY-STATE PERFORMANCE
FIGURE 5 CIRCUIT



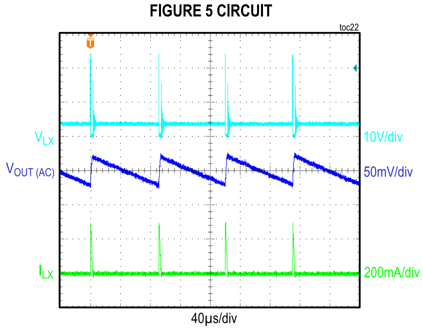
CONDITIONS: 3.3V OUTPUT, PWM MODE, 300mA LOAD

STEADY-STATE PERFORMANCE
FIGURE 5 CIRCUIT



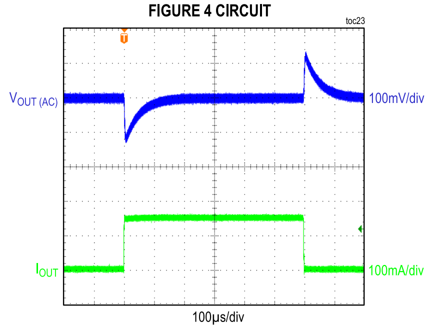
CONDITIONS: 3.3V OUTPUT, PWM MODE, NO LOAD

STEADY-STATE PERFORMANCE
FIGURE 5 CIRCUIT



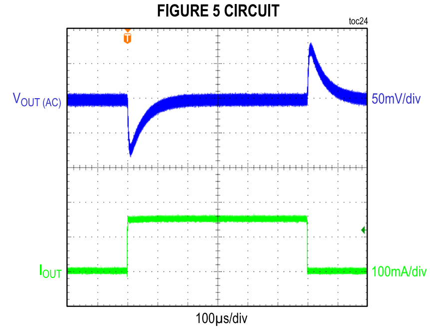
CONDITIONS: 3.3V OUTPUT, PFM MODE, 5mA LOAD

LOAD TRANSIENT BETWEEN 0mA AND 150mA
FIGURE 4 CIRCUIT



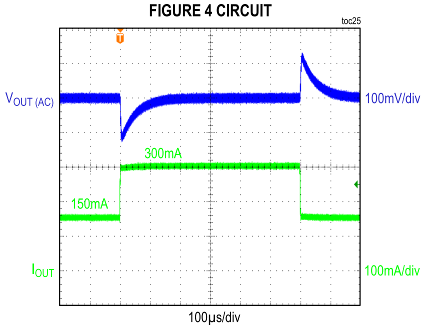
CONDITIONS: 5V OUTPUT, PWM MODE

LOAD TRANSIENT BETWEEN 0mA AND 150mA
FIGURE 5 CIRCUIT



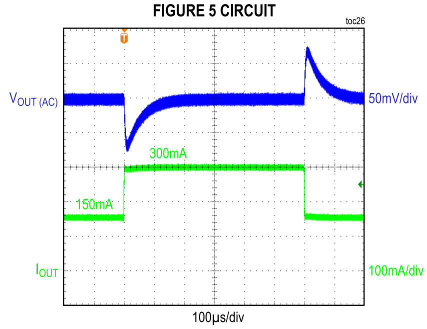
CONDITIONS: 3.3V OUTPUT, PWM MODE

LOAD TRANSIENT BETWEEN 150mA AND 300mA
FIGURE 4 CIRCUIT



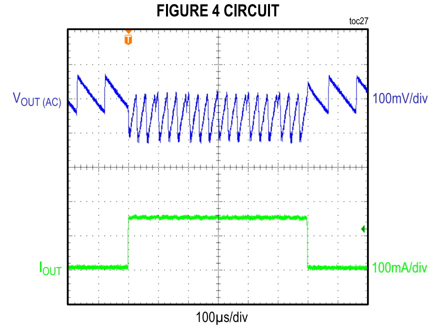
CONDITIONS: 5V OUTPUT, PWM MODE

LOAD TRANSIENT BETWEEN 150mA AND 300mA
FIGURE 5 CIRCUIT



CONDITIONS: 3.3V OUTPUT, PWM MODE

LOAD TRANSIENT BETWEEN 5mA AND 150mA
FIGURE 4 CIRCUIT

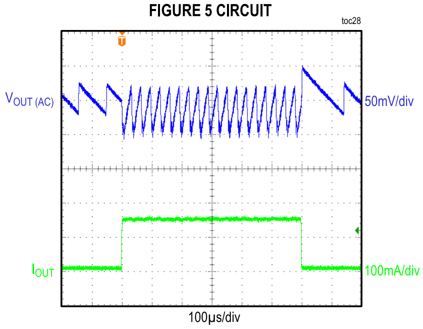


CONDITIONS: 5V OUTPUT, PFM MODE

Typical Operating Characteristics (continued)

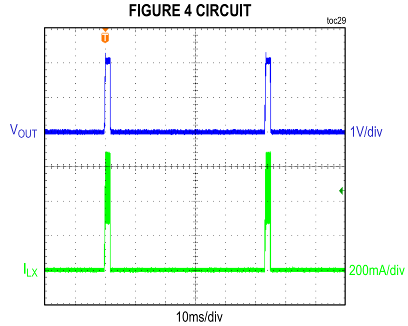
(V_{IN} = 24V, V_{SGND} = V_{PGND} = 0V, C_{VCC} = 1μF, EN/UVLO = unconnected, C_{SS} = 5600pF, T_A = +25°C, unless otherwise noted. All voltages are referenced to SGND, unless otherwise noted.)

LOAD TRANSIENT BETWEEN 5mA AND 150mA
FIGURE 5 CIRCUIT



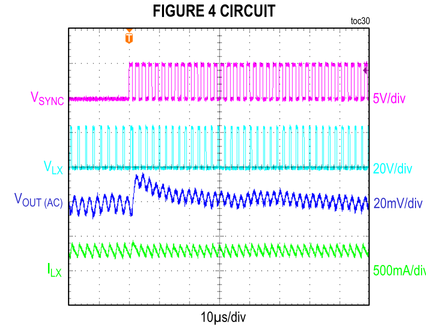
CONDITIONS: 3.3V OUTPUT, PFM MODE

OVERLOAD PROTECTION
FIGURE 4 CIRCUIT



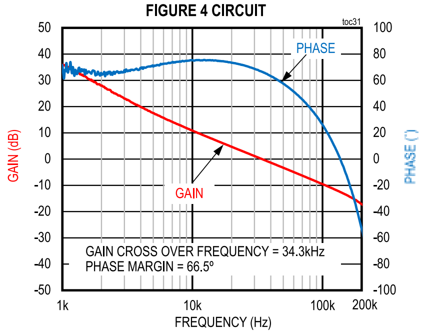
CONDITIONS: 5V OUTPUT, PWM MODE, R_LOAD = 4.4Ω

EXTERNAL CLOCK SYNCHRONIZATION
FIGURE 4 CIRCUIT



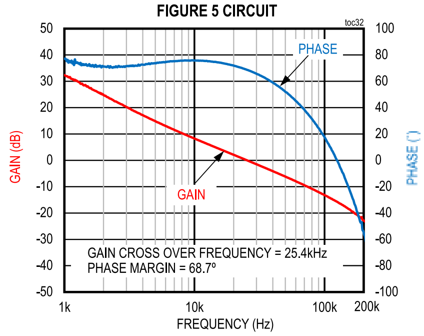
CONDITIONS: 5V OUTPUT, PWM MODE, 300mA LOAD, f_{SW} = 400kHz, EXTERNAL CLOCK FREQUENCY = 460kHz

BODE PLOT
FIGURE 4 CIRCUIT



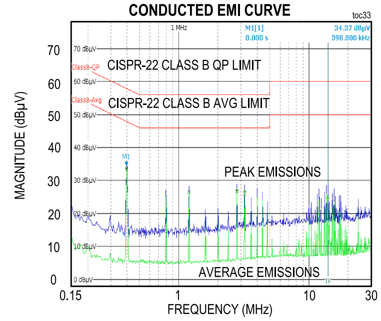
CONDITIONS: 5V OUTPUT, PWM MODE, 300mA LOAD

BODE PLOT
FIGURE 5 CIRCUIT



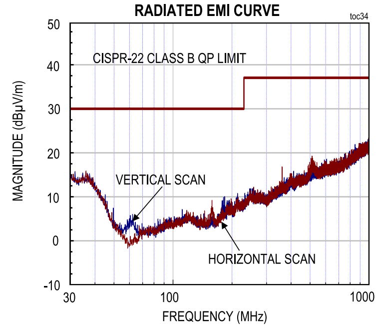
CONDITIONS: 3.3V OUTPUT, PWM MODE, 300mA LOAD

5V OUTPUT, 300mA LOAD CURRENT,
CONDUCTED EMI CURVE



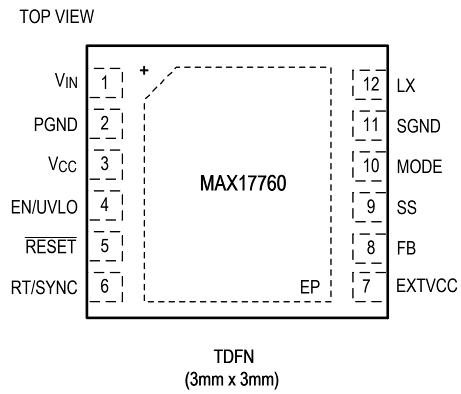
CONDITIONS: MEASURED ON THE MAX17760EVKITB# WITH L2 = 22μH, C15 = 1μF/100V/X7R/1206, C16 = 4.7μF/100V/X7R/1206

5V OUTPUT, 300mA LOAD CURRENT,
RADIATED EMI CURVE



CONDITIONS: MEASURED ON THE MAX17760EVKITB#

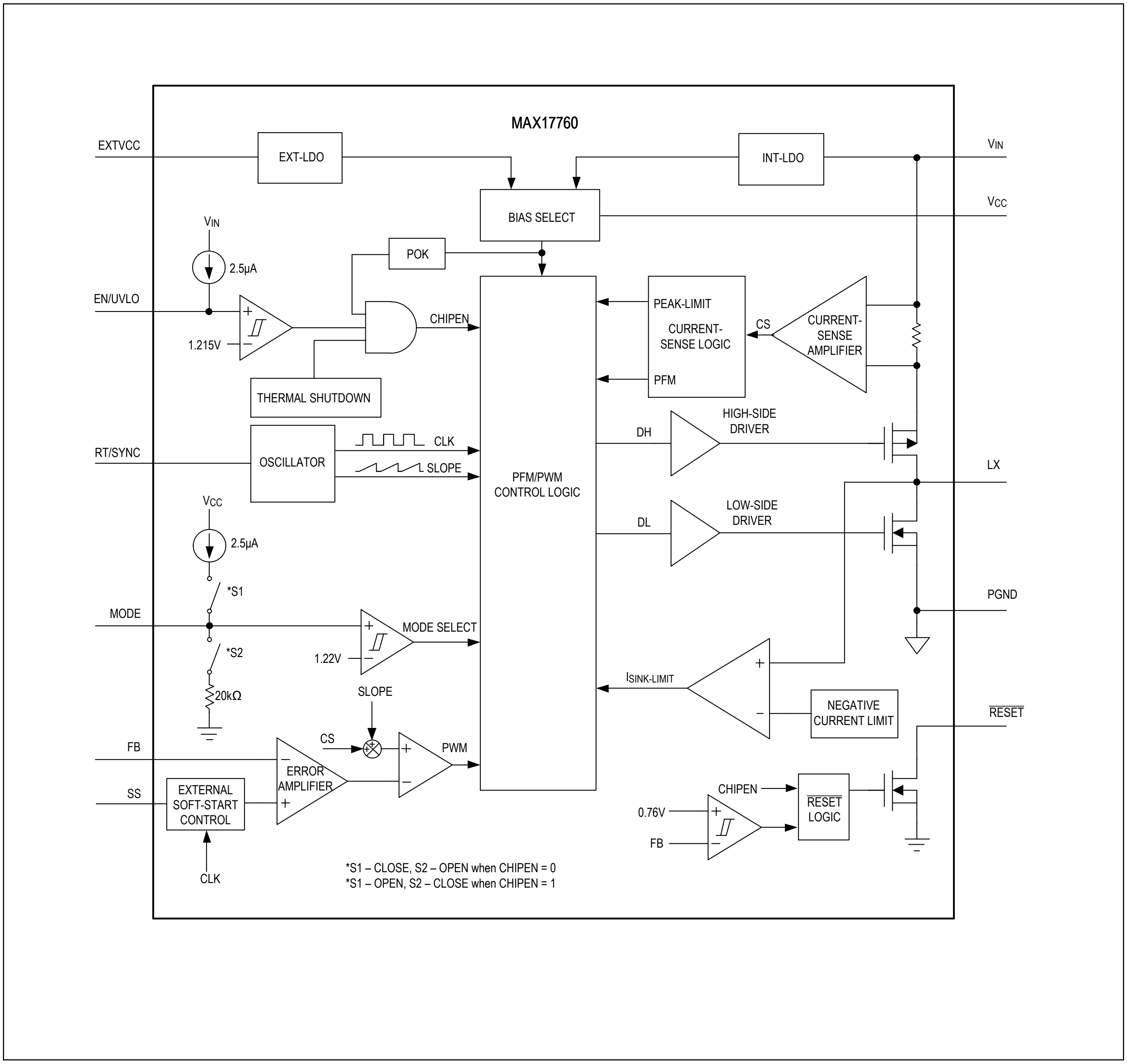
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	V_{IN}	Power Supply Input Pin. 4.5V to 76V input-supply range. Decouple to PGND with a 1μF capacitor. Place the capacitor close to the V_{IN} and PGND pins.
2	PGND	Power Ground. Refer to the MAX17760 EV kit data sheet for the recommended PCB layout and routing.
3	V_{CC}	5V LDO Output. Bypass V_{CC} with a 1μF ceramic capacitor to PGND. LDO doesn't support external loading on V_{CC}.
4	EN/UVLO	Enable/Undervoltage Lockout Pin. Drive EN/UVLO high to enable the output. Connect to the center of a resistor-divider between V_{IN} and SGND to set the input voltage at which the device turns on. Leave the pin unconnected for always-on operation.
5	$\overline{RESET}$	Open-Drain $\overline{RESET}$ Output. The $\overline{RESET}$ output is driven low when FB drops below 92% of its set value. $\overline{RESET}$ goes high 2.1ms after FB rises above 95% of its set value.
6	RT/SYNC	Programmable Switching Frequency and External Clock Synchronization Input. Connect a resistor from RT/SYNC to SGND to set the converter's switching frequency between 200kHz and 600kHz. An external clock can be connected to the RT/SYNC to synchronize the device with an external clock in PWM mode. See the *Switching Frequency Selection and External Clock Synchronization (RT/SYNC)* section for more details.
7	EXTVCC	External Power Supply Input for the EXT-LDO. Connect EXTVCC to the buck converter output for an output voltage between 5V and 24V. When EXTVCC is not used, connect it to SGND. See the *Linear Regulator (V_{CC} and EXTVCC)* section for more details.
8	FB	Feedback Input. Connect FB to the center node of an external resistor-divider from the output to SGND to set the output voltage. See the *Adjusting Output Voltage* section for more details.
9	SS	Soft-Start Input. Connect a capacitor from SS to SGND to set the soft-start time.
10	MODE	MODE Selection. The MODE pin configures the device to operate either in PWM or PFM mode of operation. Leave MODE unconnected for PFM operation. Connect MODE to SGND for constant-frequency PWM operation at all loads.
11	SGND	Signal Ground.
12	LX	Switching Node. Connect LX pin to the switching-side of the inductor.
—	EP	Exposed Pad. Connect EP to SGND. Refer to the MAX17760 EV kit data sheet for the recommended method of PCB layout, routing, and thermal vias.

Functional Block Diagram



Detailed Description

The MAX17760 is a high-efficiency, high voltage, synchronous step-down DC-DC converter with integrated MOSFETs operating over an input-voltage range of 4.5V to 76V. The device can deliver up to 300mA current. Output voltage is programmable from 0.8V up to 88% of V_{IN}. Built-in control loop compensation eliminates the need for external components. The feedback-voltage regulation accuracy over -40°C to +125°C is +1.6% to -1.7%.

The device features a peak-current-mode control architecture. An internal transconductance error amplifier produces an integrated error voltage at an internal node, which sets the duty cycle using a PWM comparator, a high-side current-sense amplifier, and a slope-compensation generator. At each rising edge of the clock, the high-side MOSFET turns on and remains on until either the appropriate or maximum duty cycle is reached, or the peak current limit is detected. During the high-side MOSFET on-time, the inductor current ramps up. During the rest of the switching cycle, the high-side MOSFET turns off and the low-side MOSFET turns on. The inductor releases the stored energy as its current ramps down and provides current to the output. The internal low R_{DSON} pMOS/nMOS switches ensure high efficiency at full load.

The MAX17760 features a MODE pin that can be used to program the device in PWM or PFM control schemes. The device also features adjustable-input undervoltage lockout (EN/UVLO), adjustable soft-start (SS), open-drain $\overline{RESET}$, and external clock synchronization (RT/SYNC) features. The MAX17760 offers a low minimum on-time that allows to operate for a wide range of input supply at a given switching frequency.

Mode Selection

The MAX17760 supports PWM and PFM mode of operation. The device detects the MODE pin status at power-up and latches the MODE of operation. Leave the MODE pin unconnected for PFM operation. At power-up the MAX17760 pullup the MODE pin with a 2.5μA current. If the MODE pin exceeds the PFM mode threshold (V_{TH_PFM}), the part latches PFM mode and pulls down MODE with a 20kΩ internal resistor. Connect MODE to SGND for constant-frequency forced PWM operation at all loads. The mode of operation cannot be changed on-the-fly after power-up.

In PWM mode, the inductor current is allowed to go negative. PWM operation provides constant frequency operation irrespective of loading, and is useful in applications sensitive to switching frequency.

PFM mode provides high efficiency at light load conditions by disabling negative inductor current and additionally skipping pulses. In PFM mode, the inductor current is forced to a fixed peak of I_{PFM} (240mA typ) every clock cycle until the output rises to 102.3% of the set nominal output voltage. Once the output reaches 102.3% of the set nominal output voltage, both the high-side and low-side FETs are turned off and the device enters hibernation until the load discharges the output to 101.1% of the set nominal output voltage. Most of the internal blocks are turned off in hibernate operation to reduce quiescent current. After the output falls below 101.1% of the set nominal output voltage, the device comes out of hibernate operation, turns on all internal blocks, and again commences the process of delivering pulses of energy to the output until it reaches 102.3% of the set nominal output voltage. The advantage of PFM mode is higher efficiency at light loads because of lower quiescent current drawn from supply. However, the output voltage ripple is higher compared to PWM mode of operation and switching frequency is not constant at light loads.

Linear Regulator (V_{CC} and EXTVCC)

The MAX17760 integrates two internal low-dropout (LDO) linear regulators INT-LDO and EXT-LDO that power V_{CC}. INT-LDO is powered from V_{IN} and turns on when $V_{EN/UVLO}$ > V_{ENT} (0.7V typ). EXT-LDO is powered from EXTVCC. At any time, only one of these two linear regulators operates, depending on the EXTVCC voltage. If EXTVCC is greater than 4.74V (typ), V_{CC} is powered from the EXTVCC. If EXTVCC is lower than 4.44V (typ), V_{CC} is powered from V_{IN}. Powering V_{CC} from EXTVCC increases efficiency at higher input voltages. Typical V_{CC} output voltage is 5V. Bypass V_{CC} to SGND with a 1μF low-ESR ceramic capacitor. V_{CC} powers the internal blocks and both low-side and high-side MOSFET drivers.

The MAX17760 employs an undervoltage-lockout circuit that forces the converter off when V_{CC} voltage falls below V_{CC-UVF} (3.8V typ). The buck converter enables when the V_{CC} voltage rises above V_{CC-UVR} (4.2 typ).

EXTVCC should be connected to the output capacitor with an R-C filter as shown in Figure 4. Without this R-C filter, the absolute maximum rating of EXTVCC (-0.3V) can be exceeded under short-circuit conditions, due to oscillations between the ceramic output capacitor and the inductance of the short-circuit path. In general, parasitic board or wiring inductance should be minimized and the output voltage under short-circuit operation should be verified to ensure that the absolute maximum rating of EXTVCC is not exceeded.

Switching Frequency Selection and External Clock Synchronization (RT/SYNC)

The MAX17760 can be programmed to one of the four discrete switching frequencies 200KHz, 300kHz, 400kHz, and 600kHz, by connecting a resistor from RT/SYNC to SGND. Table 1 provides resistor values for different switching frequencies.

The MAX17760 can be synchronized to an external clock coupled to the RT/SYNC pin through a 22pF capacitor as shown in Figure 1. The external clock must be applied after $\overline{\text{RESET}}$ is asserted high for proper configuration of the internal loop compensation. If the external clock frequency is within the allowed SYNC frequency range (1.15 to 1.4 times the nominal internal clock frequency f_{SW}), the internal clock synchronizes to the external clock within 1 clock cycle. The allowed external clock duty cycle range is 10% to 80%.

Table 1. Switching Frequency vs. RT/SYNC Resistor

SWITCHING FREQUENCY (kHz)	$R_{RT/SYNC}$ (kΩ)
200	140
300	93.1
400	69.8
600	46.4

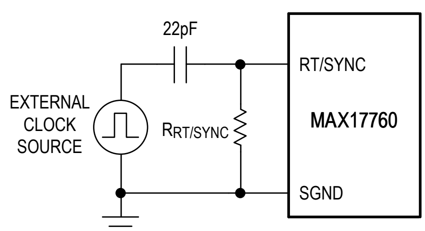


Figure 1. External Clock Synchronization

Operating Input Voltage Range

The minimum and maximum operating input voltages for a given output-voltage setting should be calculated as follows:

$$V_{IN(MIN)} = \frac{V_{OUT} + \left(I_{OUT(MAX)} \times \left(R_{DCR(MAX)} + R_{DS\text{-}ONL(MAX)}\right)\right)}{D_{MAX}} + (I_{OUT(MAX)} \times (R_{DS\text{-}ONH(MAX)} - R_{DS\text{-}ONL(MAX)}))$$

$$V_{IN(MAX)} = \frac{V_{OUT}}{f_{SW(MAX)} \times t_{ON\text{-}MIN(MAX)}}$$

where:

V_{OUT} = Steady-state output voltage

$I_{OUT(MAX)}$ = Maximum load current

$R_{DCR(MAX)}$ = Worst-case DC resistance of the inductor

$f_{SW(MAX)}$ = Maximum switching frequency

D_{MAX} = Minimum specification of maximum duty ratio (0.88)

$t_{ON\text{-}MIN(MAX)}$ = Worst-case minimum switch on-time (110 ns)

$R_{DS\text{-}ONL(MAX)}$ and $R_{DS\text{-}ONH(MAX)}$ = Worst-case on-state resistances of low-side and high-side internal MOSFETs, respectively.

Overcurrent Protection/Hiccup Mode

The device features a hysteretic peak current-limit protection scheme to protect the internal FETs and inductor under output short-circuit conditions. When the inductor peak current exceeds $I_{PEAK\text{-}LIMIT}$, the high-side switch is turned off and the low-side switch is turned on. After the current is reduced to 290mA (typ), the high-side switch is turned on at the rising edge of the next clock pulse. The device enters a hiccup timeout period t_{HIC_TOUT} (51ms typ) if 16 consecutive peak current limit events are detected. After the hiccup time-out period has elapsed, the device restarts. If the overcurrent condition persists, the device remains in hiccup current limit mode until the overcurrent fault is removed.

$\overline{\text{RESET}}$ Output

The device features a $\overline{\text{RESET}}$ comparator to monitor the output voltage. The open-drain $\overline{\text{RESET}}$ output requires an external pullup resistor. $\overline{\text{RESET}}$ goes high 2.1ms after the regulator output increases above 95% of the designed nominal regulated voltage. $\overline{\text{RESET}}$ goes low when the regulator output voltage drops to below 92% of the nominal regulated voltage. $\overline{\text{RESET}}$ also goes low during thermal shutdown.

Prebiased Output

When the device starts into a prebiased output, both the high-side and the low-side switches are turned off so that the converter does not sink current from the output. High-side and low-side switches do not start switching until the PWM comparator commands the first PWM pulse, at which point switching commences. The output voltage is then smoothly ramped up to the target value in alignment with the internal reference.

Thermal-Shutdown Protection

Thermal shutdown protection limits junction temperature of the device. When the junction temperature of the device exceeds +160°C, an on-chip thermal sensor shuts down the device, allowing the device to cool. The thermal sensor turns the device on with soft-start after the junction temperature cools by 20°C. Carefully evaluate the total power dissipation (see the *Power Dissipation* section) to avoid unwanted triggering of the thermal shutdown protection in normal operation.

Applications Information

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit switching. The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

where, $I_{OUT(MAX)}$ is the maximum load current. I_{RMS} has a maximum value when the input voltage equals twice the output voltage ($V_{IN} = 2 \times V_{OUT}$), so

$$I_{RMS(MAX)} = \frac{I_{OUT(MAX)}}{2}.$$

Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal long-term reliability. Use low-ESR ceramic capacitors with high-ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Calculate the input capacitance using the following equation:

$$C_{IN} = \frac{I_{OUT(MAX)} \times D \times (1 - D)}{\eta \times f_{SW} \times \Delta V_{IN}}$$

where:

$D = V_{OUT}/V_{IN}$ and is the duty ratio of the controller

f_{SW} = Switching frequency

ΔV_{IN} = Allowable input-voltage ripple

η = Efficiency

In applications where the source is located distant from the device input, an appropriate electrolytic capacitor should be added in parallel to the ceramic capacitor to provide necessary damping for potential oscillations caused by the inductance of the longer input power path and input ceramic capacitor.

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}) and DC resistance (R_{DCR}). The switching frequency and output voltage determine the inductor value as follows:

$$L = \frac{4 \times V_{OUT}}{f_{SW}}$$

where V_{OUT} = Output voltage

f_{SW} = Switching frequency

Select a low-loss inductor closest to the calculated value with acceptable dimensions and having the lowest possible DC resistance. The saturation current rating (I_{SAT}) of the inductor must be high enough to ensure that saturation can occur only above the peak current-limit value.

Output Capacitor Selection

X7R ceramic output capacitors are preferred due to their stability over temperature in industrial applications. The output capacitors are sized to support a step load of 50% of the maximum output current in the application, so the output-voltage deviation is contained to 3% of the output-voltage change. The minimum required output capacitance can be calculated as follows:

$$C_{OUT} = \frac{1}{2} \times \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

$$t_{RESPONSE} \cong \frac{0.35}{f_C}$$

where:

I_{STEP} = Load current step

$t_{RESPONSE}$ = Response time of the controller

ΔV_{OUT} = Allowable output-voltage deviation

f_C = Target closed-loop crossover frequency

f_{SW} = Switching frequency.

Select f_C to be the minimum of 1/10th of f_{SW} and 30kHz. Actual derating of ceramic capacitors with DC-bias voltage must be considered while selecting the output capacitor. Derating curves are available from all major ceramic capacitor manufacturers.

Soft-Start Capacitor Selection

The device implements adjustable soft-start operation to reduce inrush current. A capacitor connected from the SS pin to SGND programs the soft-start time. The selected output capacitance (C_{SEL}) and the output voltage (V_{OUT}) determine the minimum required soft-start capacitor as follows:

$$C_{SS} \geq 30 \times 10^{-6} \times C_{SEL} \times V_{OUT}$$

The soft-start time (t_{SS}) is related to the capacitor connected at SS (C_{SS}) by the following equation:

$$t_{SS} = \frac{C_{SS}}{6.25 \times 10^{-6}}$$

For example, to program a 0.9ms soft-start time, a 5.6nF capacitor should be connected from the SS pin to SGND. Note that, during startup, the device operates at half the programmed switching frequency until the output voltage reaches 80% of set output nominal voltage.

Setting the Input Undervoltage-Lockout Level

Drive EN/UVLO high to enable the output. Leave the pin unconnected for always-on operation. Set the voltage at which each converter turns on with a resistive voltage-divider connected from V_{IN} to SGND (see Figure 2). Connect the center node of the divider to EN/UVLO pin.

Choose R1 as follows:

$$R1 \leq \left(110000 \times V_{INU}\right)$$

where V_{INU} is the input voltage at which the MAX17760 is required to turn on and R1 is in Ω. Calculate the value of R2 as follows:

$$R2 = \frac{R1 \times 1.215}{\left(V_{INU} - 1.215 + (2.5\mu \times R1)\right)}$$

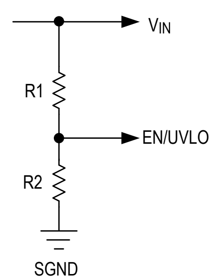


Figure 2. Setting the Input Undervoltage Lockout Level

Adjusting Output Voltage

Set the output voltage with a resistive voltage-divider connected from the output voltage node (V_{OUT}) to SGND (see Figure 3). Connect the center node of the divider to the FB pin. Use the following procedure to choose the resistive voltage-divider values:

Calculate resistor R3 from the output to the FB pin as follows:

$$R3 = \frac{15 \times V_{OUT}}{0.8}$$

where R3 is in kΩ.

Calculate resistor R4 from the FB pin to SGND as follows:

$$R4 = \frac{R3 \times 0.8}{\left(V_{OUT} - 0.8\right)}$$

R4 is in kΩ.

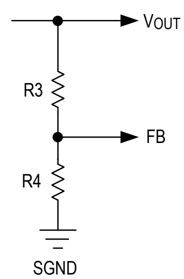


Figure 3. Adjusting Output Voltage

Power Dissipation

At a particular operating condition, the power losses that lead to a temperature rise of the device are estimated as follows:

$$P_{LOSS} = \left(P_{OUT} \times \left(\frac{1}{\eta} - 1\right)\right) - \left(I_{OUT}^2 \times R_{DCR}\right)$$
$$P_{OUT} = V_{OUT} \times I_{OUT}$$

where:

P_{OUT} = Output power

η = Efficiency of the converter

R_{DCR} = DC resistance of the inductor (see the *Typical Operating Characteristics* for more information on efficiency at typical operating conditions).

For a typical multilayer board, the thermal performance metrics for the package are given below:

$$\theta_{JA} = 41°C/W$$
$$\theta_{JC} = 8.5°C/W$$

The junction temperature of the device can be estimated at any given maximum ambient temperature ($T_{A(MAX)}$) from the following equation:

$$T_{J(MAX)} = T_{A(MAX)} + \left(\theta_{JA} \times P_{LOSS}\right)$$

If the application has a thermal-management system that ensures that the exposed pad of the device is maintained at a given temperature ($T_{EP(MAX)}$) by using proper heat sinks, then the junction temperature of the device can be estimated at any given maximum ambient temperature as:

$$T_{J(MAX)} = T_{EP(MAX)} + \left(\theta_{JC} \times P_{LOSS}\right)$$

Note: Junction temperatures greater than +125°C degrades operating lifetimes.

PCB Layout Guidelines

All connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents. Since inductance of a current-carrying loop is proportional to the area enclosed by the loop, if the loop area is made very small, inductance is reduced. Additionally, small-current loop areas reduce radiated EMI.

A ceramic input filter capacitor should be placed close to the V_{IN} pins of the IC. This eliminates as much trace inductance effects as possible and gives the IC a cleaner voltage supply. A bypass capacitor for the V_{CC} pin also should be placed close to the pin to reduce effects of trace impedance.

When routing the circuitry around the IC, the analog small signal ground and the power ground for switching currents must be kept separate. They should be connected together at a point where switching activity is minimum. This helps keep the analog ground quiet. The ground plane should be kept continuous (unbroken) as far as possible. No trace carrying high switching current should be placed directly over any ground plane discontinuity.

PCB layout also affects the thermal performance of the design. A number of thermal throughputs that connect to a large ground plane should be provided under the exposed pad of the device for efficient heat dissipation.

For a sample layout that ensures first pass success, refer to the MAX17760 EV Kit layout available at www.maximintegrated.com.

Typical Application Circuits

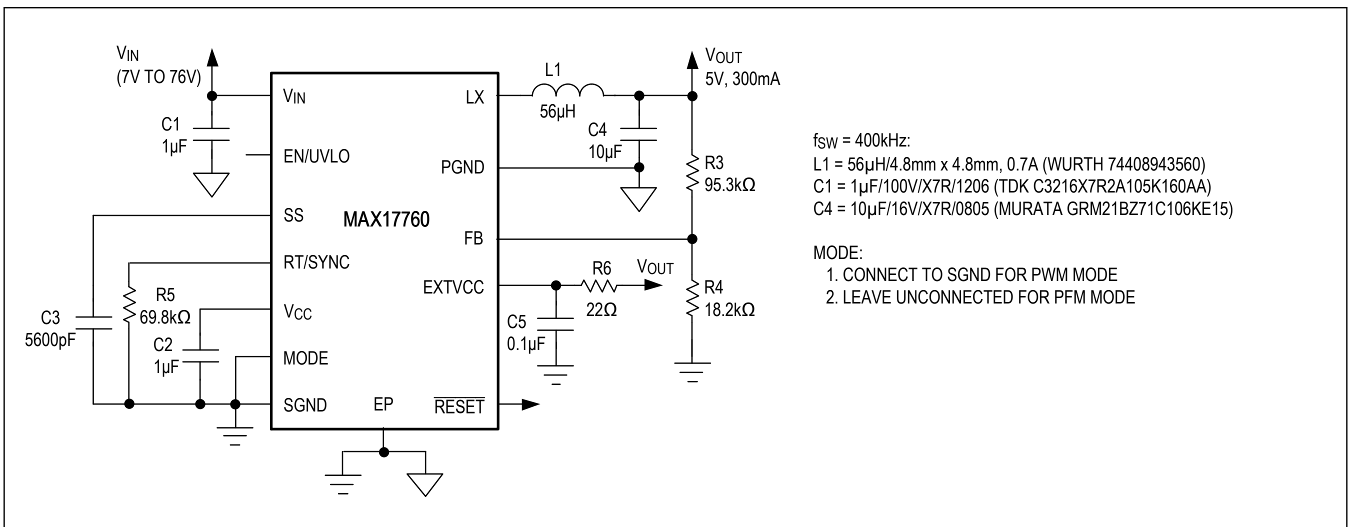


Figure 4. 5V Output with 400kHz Switching Frequency

Typical Application Circuits (continued)

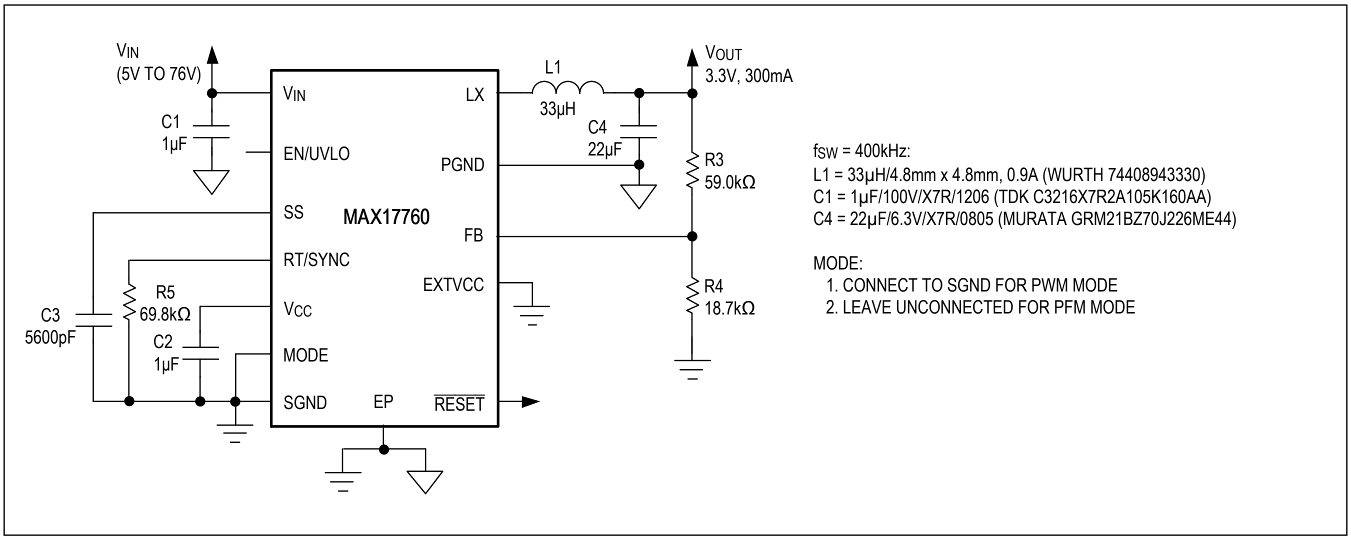


Figure 5. 3.3V Output with 400kHz Switching Frequency

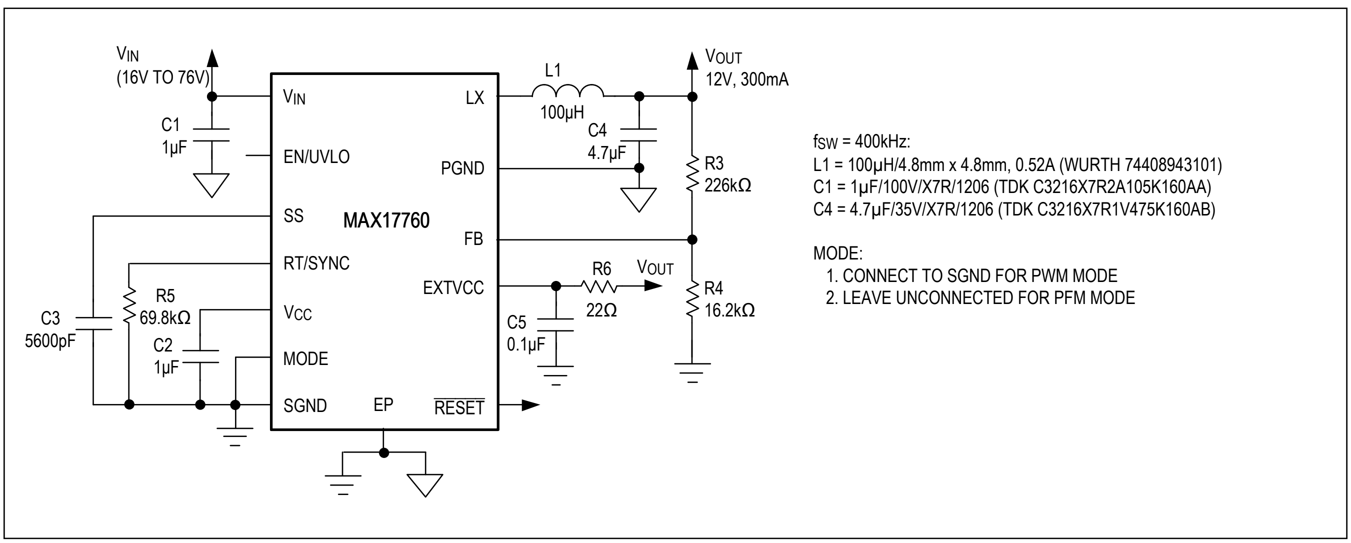


Figure 6. 12V Output with 400kHz Switching Frequency

Ordering Information

PART NUMBER	TEMP. RANGE	PIN-PACKAGE
MAX17760ATC+	-40°C to +125°C	12 TDFN - EP* (3mm x 3mm)
MAX17760ATC+T	-40°C to +125°C	12 TDFN - EP* (3mm x 3mm)

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/20	Initial release	—