Click here for production status of specific part numbers.

MAX19505–MAX19507/ MAX19515–MAX19517 Evaluation Kits

Evaluate: MAX19505–MAX19507/ MAX19515–MAX19517

General Description

The MAX19505–MAX19507/MAX19515–MAX19517 evaluation kits (EV kits) are fully assembled and tested circuit boards that contain all the components necessary to evaluate the performance of this family of 8-bit and 10-bit analog-to-digital converters (ADCs). The EV kits also include Windows® 7/10-compatible software that provides a simple graphical user interface (GUI) for exercising the programmable features of the MAX19505/ MAX19507/MAX19515–MAX19517.

The MAX19505–MAX19507/MAX19515–MAX19517 EV kits accept a single-ended analog input from an analog signal source. The EV kits provide an on-board circuit that transforms this analog single-ended signal into a differential signal. The ADC digital output can be captured easily with a basic logic analyzer. The EV kits can operate from a single 3.6V nominal power supply and provide on-board regulation for the analog, clock, digital, and logic circuitry.

Part Selection Table

PART	RESOLUTION (Bits)	SPEED (Msps)
MAX19505ETM+	8	65
MAX19506ETM+	8	100
MAX19507ETM+	8	130
MAX19515ETM+	10	65
MAX19516ETM+	10	100
MAX19517ETM+	10	130

Features

- Single Power-Supply Operation
- Low-Voltage and Low-Power Operation
- On-Board Single-Ended to Differential Transformer Circuitry
- Differential or Single-Ended Clock Configuration
- On-Board Clock-Shaping Circuit with Adjustable Duty Cycle
- On-Board SPI™ Interface Circuit
- User-Selectable Supply Voltages
- Lead(Pb)-Free and RoHS Compliant
- Fully Assembled and Tested

Ordering Information

PART	TYPE
MAX19505EVKIT+	EV Kit
MAX19506EVKIT+	EV Kit
MAX19507EVKIT+	EV Kit
MAX19515EVKIT+	EV Kit
MAX19516EVKIT+	EV Kit
MAX19517EVKIT+	EV Kit

+Denotes lead(Pb)-free and RoHS compliant.

Component List

REF DES	QTY	DESCRIPTION
C1, C40	2	4.7µF Tantalum Capacitor SMT (3528), 16V, 20%
C2, C27, C28, C76, C77	5	10µF Ceramic Capacitor; SMT (0805), 6.3V, 20%, X5R
C3	1	1µF Ceramic Capacitor SMT (0402), 6.3V; TOL = 10%, X5R
C4, C5	2	8pF Ceramic Capacitor SMT (0402), TOL = ±0.25pF

REF DES	QTY	DESCRIPTION
C6, C7, C29, C48-C53, C66-C73	17	0.1µF Ceramic Capacitor SMT (0402), 10V; 10%; X5R
C25, C26	2	0.1µF Ceramic Capacitor SMT (0603), 50V, 10%, X7R
C30, C31	2	100pF Ceramic Capacitor SMT (0402), 50V, 5%, C0G
C43, C79, C81-C89	11	0.1µF Ceramic Capacitor SMT (0402), 10V, 10%, X7R

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Component List (continued)

REF DES	QTY	DESCRIPTION
C54, C55, C75, C78	4	0.01µF Ceramic Capacitor SMT (0603), 25V, 10%
C80	1	3.3µF Ceramic Capacitor SMT (0402), 6.3V, 20%, X5R
CLK, SYNC, VINA, VINB	4	SMA Connector, 5 Pins
D2	1	Schottky Diode, PIV = 70V, PD = 0.25W
DS1-DS4	4	Green LED SMT (0603)
GND, VSUPPLY	2	Banana Connector
J1, J8-J10, JU6, JU7, JU9, JU10	8	2 Pin Header
J5	1	48 Pin Header
J6	1	USB MINI B-TYPE SMT Connector, Right Angle, 9 PINS
J7	1	10 Pin Header
JU1-JU3	3	4 Pin Header
L1, L2	2	28 Ferrite-Bead Inductor SMT (0603), 25%; 4A
MH1-MH4	4	5/8IN Round-Thru Hole Spacer; No Thread; M3.5; Nylon
R1, R3-R12, R45, R58-R63, R70-R75	24	47 Resistor SMT (0402), 5%, 0.1W
R2, R43, R44	3	100kΩ Resistor (0603), 5%; 0.1W
R19-R22	4	75Ω Resistor (0603), 0.1%, 0.10W
R23-R26	4	121Ω Resistor (0603), 0.1%, 0.10W
R27-R41, R47-R49	18	0Ω Resistor; 0402, 0%, 0.10W
R42, R54, R55	3	49.9Ω Resistor (0603), 1%, 0.10W
R46	1	10kΩ Resistor, 10%, 0.5W
R56, R57, R65	3	100Ω Resistor (0603), 1%, 0.10W
R64	1	0Ω Resistor (0603), 5%, 0.10W
R66-R68, R83-R85	6	10kΩ Resistor (0603), 5%, 0.10W
R69	1	2.2kΩ Resistor (0603), 2.2kΩ, 5%, 0.10W
R76-R78	3	75Ω Resistor (0603), 1%, 0.10W

REF DES	QTY	DESCRIPTION
R81	1	1kΩ Resistor (0603), 5%, 0.10W
R82	1	12kΩ Resistor (0603), 1%, 0.10W
S1	1	Surface Mount Tactile Switch, SMT
T1-T4	4	0.4-800MHz Transformer, SMT
T5	1	0.20MHz TO 400MHz, Transformer, SMT
TP1, TP2	2	Orange Test Point
TP3	1	Black Test Point
U1	1	ADC, Dual-Channel, 10-BIT, 130Msps, TQFN 48-EP
U2	1	Ultra-Low-Noise, High PSRR, Low-Dropout, Linear Regulator
U3	1	Usb, Quad High Speed USB to Multipurpose UART/MPSSE IC, LQFP 64 12X12
U4	1	4-Bit Dual-Supply Bus Transceiver With Configurable Voltage Translation And 3-State Output, TSSOP 16
U9	1	EEPROM, 2K, 16-BIT MICROWIRE Compatible Serial EEPROM, NSOIC8 150MIL
U10	1	TINYLOGIC, ULP-AS Dual Inverter, SC70-6
U11, U12	2	16-BIT Buffer/Driver with 3-State Outputs, TSSOP 48
U14, U15	2	LOW-NOISE LDO regulator PIN-Selectable Output Voltage. TDFN8 2X2
USB3V3	1	Red Test Point
Y1	1	Crystal, SMT, 18pF, 12MHz
PCB	1	PCB: MAX19517
J2-J4	0	Not Installed, 2 Pin Header
R13-R18, R50, R52, R53	0	Not Installed, (0603) Resistor
C32-C35	0	Not Installed, (0402) Non-Polar Capacitor
R51	0	Not Installed, (0402) Resistor

EV Kit-Specific Component List

PART	DESIGNATION	DESCRIPTION
MAX19505EVKIT+	U1	8-bit 65Msps dual ADC (48 TQFN) Maxim MAX19505ETM+
MAX19506EVKIT+		8-bit 100Msps dual ADC (48 TQFN) Maxim MAX19506ETM+
MAX19507EVKIT+		8-bit 130Msps dual ADC (48 TQFN) Maxim MAX19507ETM+
MAX19515EVKIT+		10-bit 65Msps dual ADC (48 TQFN) Maxim MAX19515ETM+
MAX19516EVKIT+		10-bit 100Msps dual ADC (48 TQFN) Maxim MAX19516ETM+
MAX19517EVKIT+		10-bit 130Msps dual ADC (48 TQFN) Maxim MAX19517ETM+

Component Suppliers

SUPPLIER	PHONE	WEBSITE
Central Semiconductor Corp.	631-435-1110	www.centralsemi.com
Coilcraft, Inc.	847-639-6400	www.coilcraft.com
Diodes, Inc.	805-446-4800	www.diodes.com
Fairchild Semiconductor	888-522-5372	www.fairchildsemi.com
Future Technology Devices International Ltd.	—	www.ftdichip.com
IRC, Inc.	361-992-7900	www.irctt.com
Mini-Circuits	718-934-4500	www.minicircuits.com
Murata Electronics North America, Inc.	770-436-1300	www.murata-northamerica.com
Panasonic Corp.	800-344-2112	www.panasonic.com
Link Instruments	973-808-8990	www.linkinstruments.com
Susumu International USA	208-328-0307	www.susumu-usa.com
Taiyo Yuden	800-348-2496	www.t-yuden.com
TDK Corp.	847-803-6100	www.component.tdk.com
Texas Instruments Inc.	972-644-5580	www.ti.com

Note: *Indicate that you are using the MAX19505, MAX19506, MAX19507, MAX19515, MAX19516, or MAX19517 when contacting these component suppliers.*

MAX19505–MAX19507/ MAX19515–MAX19517 EV Kit Files

FILE	DESCRIPTION
MAX195xxDualADCEVKit SoftwareInstaller.exe	Installs the EV kit files on your computer
MAX195xxGUI.exe	Application program
ftd2xx.dll	Supporting Library
MaximStyle.dll	Supporting Library
libMPSSE.dll	Supporting Library
FTD2XX_NET.dll	Supporting Library
unins000.exe	Uninstalls the EV kit software

Quick Start

Recommended Equipment

- Single nominal 3.6V, 1A DC power supply
- Signal generator with low phase noise and low jitter for clock input (e.g., HP 8644B)
- Signal generator for analog signal input (e.g., HP 8644B)
- Logic analyzer (recommended, IO3232A)
- Analog bandpass filters (e.g., K&L Microwave) for input and clock signal
- User-supplied Windows 7/10 PC with two spare USB ports

Note: In the following sections, software-related items are identified by bolding. Text in **bold** refers to items from the EV kit software. Text in **bold and underlined** refers to items from the Windows operating system.

Procedure

The MAX19505–MAX19507/MAX19515–MAX19517 EV kits are fully assembled and tested surface-mount boards. Follow the steps below to verify board operation. **Caution: Do not turn on power supplies or enable signal generators until all connections are completed**.

1) Verify that shunts are installed across pins 1-3 of jumpers JU1, JU2, and JU3 (SPI connected).
2) Verify that no shunts are installed across jumpers JU6 (device enabled) and JU7 (SPI enabled).
3) Verify that shunts are installed across jumpers JU9 (AVDD connected) and JU10 (OVDD connected).
4) Verify that shunt is installed across jumper J1, and no jumper is installed across J8 (AVDD = 1.8V).
5) Verify that shunt is installed across jumper J8, and no jumper is installed across J10 (OVDD = 1.8V).
6) Connect the clock generator output to the clock bandpass filter input.
7) Connect the output of the clock bandpass filter to the CLK SMA connector.
8) Connect the output of the analog signal generator to the input of the signal bandpass filter. Keep the cable connection between the signal generators, filters, and EV kit board as short as possible for optimum dynamic performance.
9) Connect the output of the signal bandpass filter to the VINA SMA connector. Note: It is recommended that a 3dB or 6dB attenuation pad be used to reduce reflections and distortion from the bandpass filter.
10) If using IO3200, apply power to the IO3232A by connecting the USB cable from the computer's type-A USB port to the IO3232A module's mini-USB port.
11) Connect the MAX195xx J5 header pins to the logic analyzer (See Connecting the IO3232A to the EV Kit below, if applicable).
12) Connect the power supply to V_{SUPPLY}. Connect the ground terminal of this supply to the corresponding GND pad.
13) Connect the USB cable from the computer's type-A USB port to the EV kit board's Mini USB port.
14) Visit **www.maximintegrated.com** and search for the device EV Kit to download the latest version of the MAX195xx EV kit software and install it on your computer by running the INSTALL.EXE program. The program files are copied and icons are created in the Windows **Start** menu.
15) Start the MAX195xx program by opening its icon in the **Start** menu.
16) Turn on the 5V power supply.
17) Enable the signal generators.
18) Set the clock signal generator for an output amplitude of $2V_{P-P}$ or higher (recommended +16dBm to +19dBm for optimum AC performance for input frequencies > 100MHz) and the frequency (f_{CLK}) as appropriate.
19) Set the analog input signal generators for an output amplitude of less than or equal to $2V_{P-P}$ and to the desired frequency.
20) Verify that the two signal generators are phase locked to each other. Adjust the output power level of the signal generators to overcome cable, bandpass filter, and attenuation pad losses at the input.
21) Collect data using the logic analyzer.

Detailed Description of Software

Updating Registers

To send the new register values to the device through the SPI interface, click the **Update Registers** button after the settings are changed.

Application Menu

This menu contains 3 options, **File**, **Device** and **Help**. These options allow the user to Exit the program, choose their MAX195xx device, and view the splash screen, respectively. The user should select a device upon startup, as this will adjust the **Output Timing Controls** to the device's default settings.

User-Interface Panel

The program's main window contains two tabs, **Input/Output/Clock** (Figure 1) and **Power Management** (Figure 2), that provide controls for the MAX195xx software-configurable features. The **Input/Output/Clock** tab provides controls for **Output Format**, **Input Common Mode**, **Output CMOS Termination**, **Output Timing Control**, and **Clock Controls**. The **Power Management** tab provides controls for **Power Management** and **Output Driver Power Mgmt. Controls**. Changes to the controls result in a write operation that updates the appropriate registers of the ADC. A status bar is also provided at the bottom of the program's main window and is used to verify command module and device connectivity. For reference, a list of registers and their content is provided in a column on the right side of the program's main window.

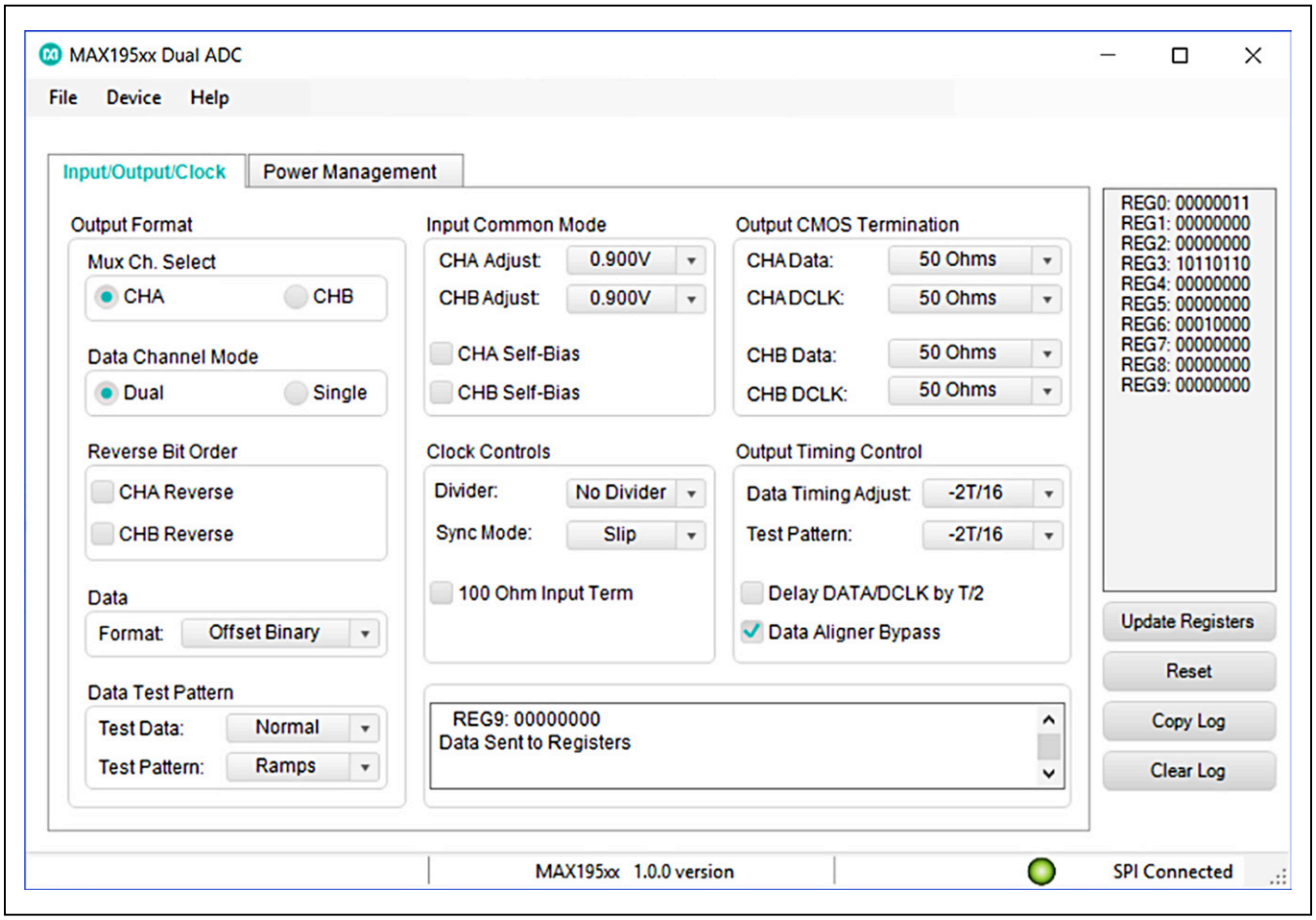


Figure 1. MAX195xx EV Kit Software (Input/Output/Clock Tab)

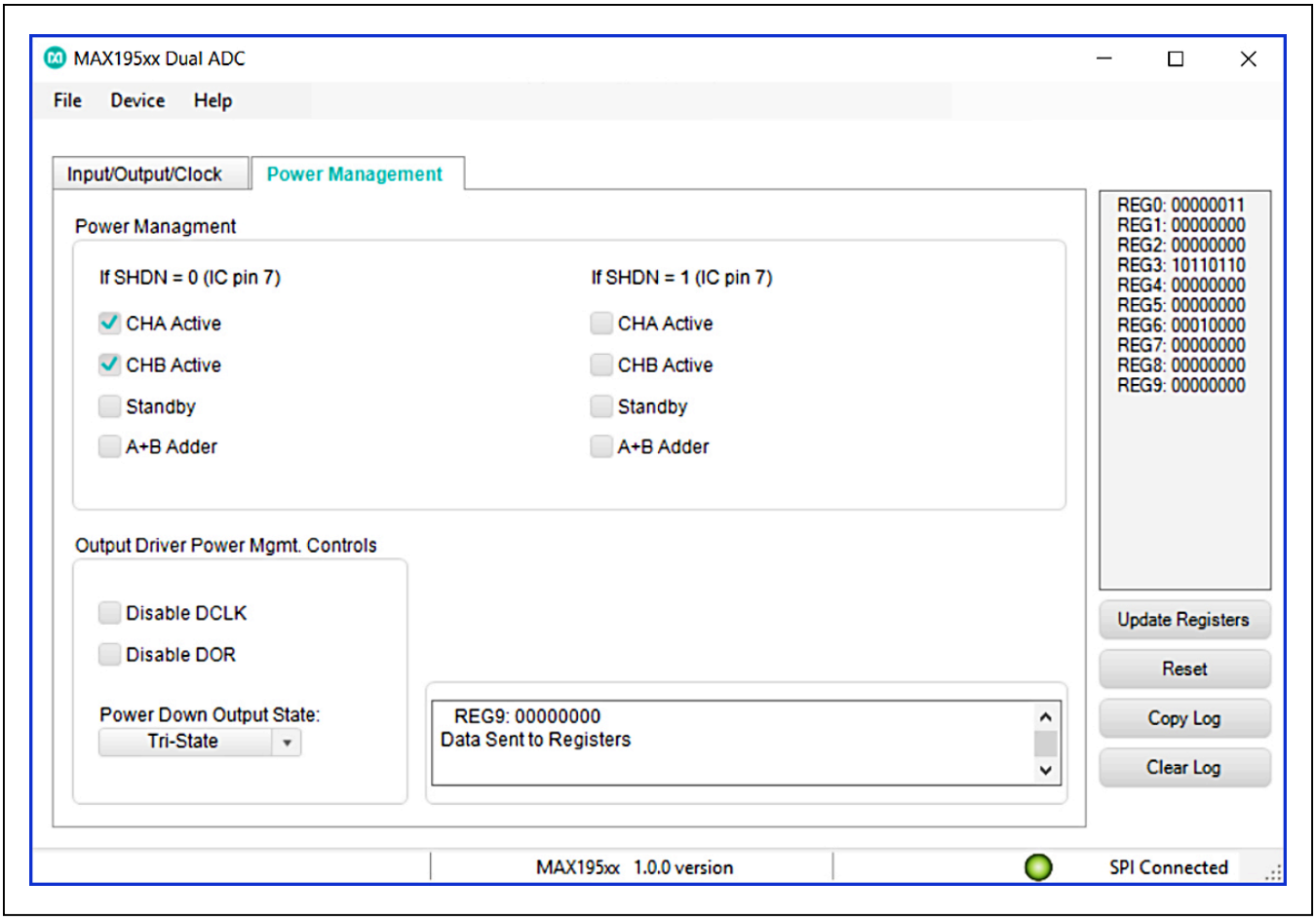


Figure 2. MAX195xx EV Kit Software (Power Management Tab)

Input/Output/Clock Tab

Output Format

The **Output Format** group box contains several functions that format the output data. The option to select between single or dual data channels or set the multiplexer between channels A or B is available through proper selection of the radio buttons in the **Data Channel Mode** and **Mux Ch. Select** group boxes. The **CHA Reverse** and **CHB Reverse** checkboxes in the **Reverse Bit Order** group box allow the user to reverse the bit order of channels A and B, respectively.

The **Format** drop-down list in the **Data** group box configures the output data to two's complement, offset binary, or gray code. The **Test Data** drop-down list in the **Data Test Pattern** group box gives the user the option to choose between normal and test data modes. When **Test Data mode** is selected, the **Test Pattern** drop-down list becomes active. The **Test Pattern** drop-down list allows the user to choose between ramping or alternating test pattern data.

Input Common Mode

The **CHA Adjust** and **CHB Adjust** drop-down lists set the input common-mode voltage according to the value selected. The **CHA Self-Bias** and **CHB Self-Bias** checkboxes apply common-mode voltages to input pins when checked, and disable common-mode inputs when unchecked.

Output CMOS Termination

The **Output CMOS Termination** group box contains independent controls to set the CMOS back termination of **CHA Data** and **CHB Data** and **CHA DCLK** and **CHB DCLK**. The **CHA Data** and **CHB Data** drop-down lists set the data termination, while the **CHA DCLK** and **CHB DCLK** drop-down lists sets the DCLK termination.

Output Timing Control

The **Output Timing Control** group box contains controls to make adjustments to data and DCLK timing. The **Data Timing Adjust** drop-down list adjusts DATA timing by the selected value. The **DCLK Timing Adjust** drop-down list adjusts DCLK timing by the selected value. By checking the **Delay DATA/DCLK by T/2** checkbox, DATA and DCLK outputs are delayed by a factor of T/2. The **Data Aligner Bypass** checkbox bypasses the data aligner delay line when checked. For more details on output timing control, refer to the respective IC data sheet.

Clock Controls

The **Clock Controls** group box contains controls for manipulating the clock. The **Divider** drop-down list sets the clock divider. The **Sync Mode** drop-down list sets clock synchronization to either slip or edge mode. In slip mode, the divided output is forced to skip a state transition on the third rising edge of the input clock (CLK) after the rising edge of SYNC. In edge mode, the divided output is forced to state 0 on the third rising edge of CLK. The **100 Ohm Input Term**. checkbox switches 100Ω across differential clock inputs when checked. For more details on clock synchronization and control, refer to the respective IC data sheet.

Power Management Tab

Power Management Controls

The **Power Management** group box contains two sets of controls. The first set is used only when the SHDN pin on the EV kit is set low; the second set is used only when the SHDN pin on the EV kit is set high. When checked, the **CHA Active** and **CHB Active** checkboxes activate channel A and channel B, respectively, and power down/standby channel A and channel B when unchecked. The **Standby** checkbox toggles between standby mode when checked and full power-down mode when unchecked, as long as **CHA Active** or **CHB Active** checkboxes are unchecked. The **A+B Adder** mode checkbox toggles between A+B adder mode when checked and normal dual mode when unchecked. For more details on power management, refer to the respective IC data sheet.

Output Driver Power Management Controls

The **Output Driver Power Mgmt. Controls** group box contains controls to disable the digital clock (DCLK) and out-of-range indicator (DOR). The **Disable DCLK** checkbox disables the DCLK when checked and the **Disable DOR** checkbox disables DOR. Note: Disable DCLK and disable DOR applies to CMOS modes only. The **Power Down Output State** drop-down list sets the digital output high, low, or to tri-state during power-down. For more details on output driver power management control, refer to the respective IC data sheet.

User Log

The **User Log** is in each tab. The **User Log** keeps track of all settings when the **Update Registers** button is pressed. When the user switches tabs, the contents are updated between both tabs. The **User Log** can also be used to take notes, and hitting the **Copy Log** button will copy the log to the clipboard.

Detailed Description of Hardware

The MAX19505–MAX19507/MAX19515–MAX19517 evaluation kits (EV kits) are fully assembled and tested circuit boards that contain all the components necessary to evaluate the performance of this family of 8-bit and 10-bit analog-to-digital converters (ADCs).

The ADCs accept differential input signals; however, on-board transformers (T1–T4) convert a readily available single-ended source output to the required differential signal. The input signals of the ADCs can be measured using a differential oscilloscope probe at headers J2 and J3.

Output drivers (U11 and U12) buffer the output signals of the data converter. The digital outputs of each EV kit are accessible at header J5.

Each EV kit is designed as a four-layer PCB to optimize the performance of this family of ADCs. Separate analog, digital, clock, and buffer power planes minimize noise coupling between analog and digital signals. The 100Ω differential microstrip transmission lines are used for analog and clock inputs. The 50Ω microstrip transmission lines are used for all digital outputs. The trace lengths of the 100Ω differential input lines are matched to within a few thousandths of an inch to minimize layout-dependent input-signal skew.

Using the IO3232A with the EV Kit

The Logic Analyzer Pattern Generator (IO3200) is one of the many instrument options to evaluate the performance of this specific family of evaluation kits. While it is simple enough to use, this method does require the user to download the IO3200 software from the following link: www.linkinstruments.com

Connecting the IO3232A to the EV Kit

The IO3232A can be connected to the MAX195xx boards using the following pin ordering. It is not essential to match the pins exactly as specified below, as they are a recommended connection sequence.

Power Supplies

The MAX195xx EV kits operate from a single DC power supply (VSUPPLY) and provide on-board regulation to power the analog, digital, and clock-shaping circuit blocks. The nominal voltage input for the VSUPPLY is at 3.6V. The maximum voltage supported by the MAX195xx EV kits is 5V, and the minimum voltages are represented in Table 1 and Table 2 based on the user's desired regulated voltage. The analog and clock (AVDD) are regulated to a desired voltage (1.8V, 2.5V, 3.0V, or 3.3V) through the MAX8902A (U14), a pin-selectable linear regulator. The digital output and logic circuitry (OVDD and VLOGIC) are both regulated to a desired voltage (1.8V, 2.5V, 3.0V, or 3.3V) through the MAX8902A (U15). J1, J8, J9, and J10 are provided to select the desired output of U14 and U15. See Table 2 and Table 3 for AVDD and OVDD/VLOGIC supply options. Jumpers JU9 and JU10 are provided to either disconnect or measure current through AVDD and OVDD, respectively.

Clock Input

The data converter allows for either differential or single-ended signals to drive the clock inputs. The MAX195xx EV kits support both methods.

In single-ended operation, the clock signal is applied to the ADC through a buffer (U10). In differential mode, an on-board transformer converts a user-supplied single-ended analog input and generates a differential analog signal, which is then applied to the ADC's input pins.

Table 1. J5 Header and IO3232A Pin Relationships

J5 HEADER FROM EV KIT	IO3232A PINS
DCLKA	Ext. clk0 (interchangeable with DCLKB)
DORA	PIN 10
D9A:D0A	PINS 9:0, respectively
D9B:D0B	PINS 25:16, respectively
DORB	PIN 26
DCLKB	Ext. clk0 (interchangeable with DCLKA)

Configuring the EV Kits for Single-Ended Clock Operation

To configure the MAX195xx EV kits for single-ended clock operation, the following modifications must be made to the clock circuit:

1) Remove 0Ω resistors at locations R47, R48, and R49.
2) Install 0Ω resistors at locations R51 and R52.
3) Install a 49.9Ω ±1% resistor at location R50.

In single-ended clock configuration, potentiometer R46 can be utilized to control the duty cycle of the clock input signal. Measure the clock input at J4 and adjust R46 until the desired duty cycle is achieved.

Input Signal

Although this family of ADCs accepts differential analog input signals, the EV kits only require single-ended analog input signals. Insertion losses due to a series-connected filter and the interconnecting cables decrease the amount of power seen at the EV kit input. Account for these losses when setting the signal generator amplitude. On-board transformers (T1–T4) convert the single-ended analog input signals and generate the recommended differential analog signals at the ADCs' differential input pins. The input circuit supports input frequencies from 1MHz to 400MHz.

Table 2. MAX8902A Output Voltage for AVDD (J1 and J9)

J1	J9	AVDD	VSUPPLY MIN
OPEN	INSTALL	1.8V*	2.1V
OPEN	OPEN	2.5V	2.8V
INSTALL	INSTALL	3.0V	3.3V
INSTALL	OPEN	3.3V	3.6V

**Default*

Table 3. MAX8902A Output Voltage for OVDD and VLOGIC (J8 and J10)

J8	J10	OVDD/VLOGIC	VSUPPLY MIN
OPEN	INSTALL	1.8V*	2.1V
OPEN	OPEN	2.5V	2.8V
INSTALL	INSTALL	3.0V	3.3V
INSTALL	OPEN	3.3V	3.6V

**Default*

Output Signal

The MAX19505, MAX19506, and MAX19507 feature two 8-bit, parallel, CMOS-compatible digital outputs that transmit the converted analog input signals. The higher resolution MAX19515, MAX19516, and MAX19517 feature two 10-bit, parallel, CMOS-compatible digital outputs that transmit the converted analog input signals. Each set of 8-bit or 10-bit digital outputs also includes a clock bit (DCLKA/B) and overrange bit (DORA/B) to accommodate data synchronization and error detection. See the *Output Bit Locations* section for more details on how to configure these 8-bit and 10-bit converter outputs.

Output Bit Locations

Two drivers (U11 and U12) buffer the digital outputs of the individual ADCs. These drivers are able to drive large capacitive loads, which may be present at the logic analyzer connection. The outputs of the buffers are connected to J5.

Serial Port Enable ($\overline{SPEN}$)

The $\overline{SPEN}$ pin selects the means of programming the internal registers of the MAX19505–MAX19507/MAX19515–MAX19517 ADCs. $\overline{SPEN}$ is set high or low based on the settings of jumper JU7, shown in Table 4. When a shunt on JU7 is installed, the 3-wire serial port is disabled and the part can be programmed through jumpers JU1, JU2, and JU3 in parallel mode. When JU7 is left open, $\overline{SPEN}$ is pulled to GND through R44. Refer to the respective IC data sheet for more information on $\overline{SPEN}$ and parallel programming. Note that when the serial port is enabled, jumpers JU1, JU2, and JU3 must be set to pins 1-3 for proper operation.

Shutdown (SHDN)

The MAX19505–MAX19507/MAX19515–MAX19517 ADCs can also be placed in a low-power shutdown mode through jumper JU6. This pin has different effects depending on the state of $\overline{SPEN}$. When in SPI programming mode, SHDN can select between two power-management states. When in parallel programming mode, SHDN can enable/disable the IC.

When SPI programming is enabled ($\overline{SPEN}$ = 0), the SHDN pin is a toggle switch between two power-management states, shown in Figure 2 under the **Power Management** group box of the software interface. When a shunt is installed on JU6, SHDN is connected to AVDD and the user can select the appropriate settings for **CHA Active**, **CHB Active**, **Standby**, and **A+B Adder** mode under the label ****Use when SHDN = 1 (IC pin 7)****. When no shunt is installed on JU6, SHDN is connected to GND through R43 and the user can select the appropriate settings for **CHA Active**, **CHB Active**, **Standby**, and **A+B Adder** mode under the label ****Use when SHDN = 0 (IC pin 7)****.

When parallel programming mode is enabled ($\overline{SPEN}$ = 1), the SHDN pin enables/disables the IC according to the settings in Table 5.

Table 4. Jumper JU7 Functions

SHUNT POSITION	$\overline{SPEN}$ PIN	3-WIRE SERIAL PORT
Installed	Connected to AVDD	Disabled (parallel programming mode)
Not installed*	Connected to GND though a 100kΩ pulldown resistor	Enabled (SPI programming)

**Default position.*

Table 5. Jumper JU6 Functions ($\overline{SPEN}$ = AVDD)

SHUNT POSITION	SHDN PIN	POWER STATE ($\overline{SPEN}$ = AVDD)
Installed	Connected to AVDD	Complete power-down
Not installed*	Connected to GND through a 100kΩ pulldown resistor	CHA + CHB active

**Default position.*

Parallel Programming

Limited feature selection is available as an alternative to full programmability through the serial port. If the serial port is disabled by setting the $\overline{SPEN}$ pin high, the serial port pins ($\overline{CS}$, SCLK, SDIN) become feature selection pins (OUTSEL, DIV, FORMAT) that require an analog control network.

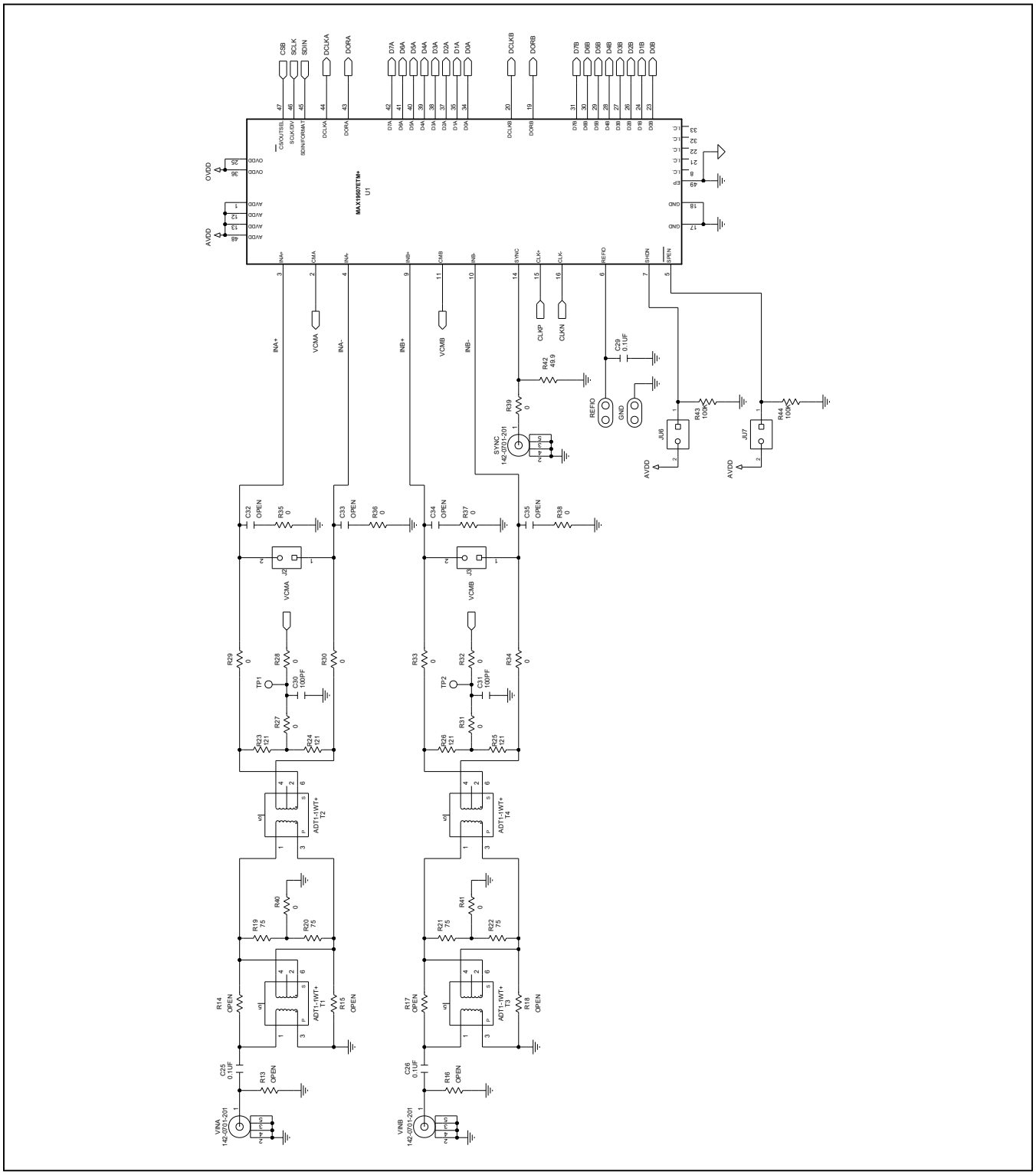
Jumpers JU1, JU2, JU3, and JU7 control the feature selection when the serial port is disabled (parallel programming is enabled). See Table 6 for functionality.

Table 6. Parallel Programming Feature Selection

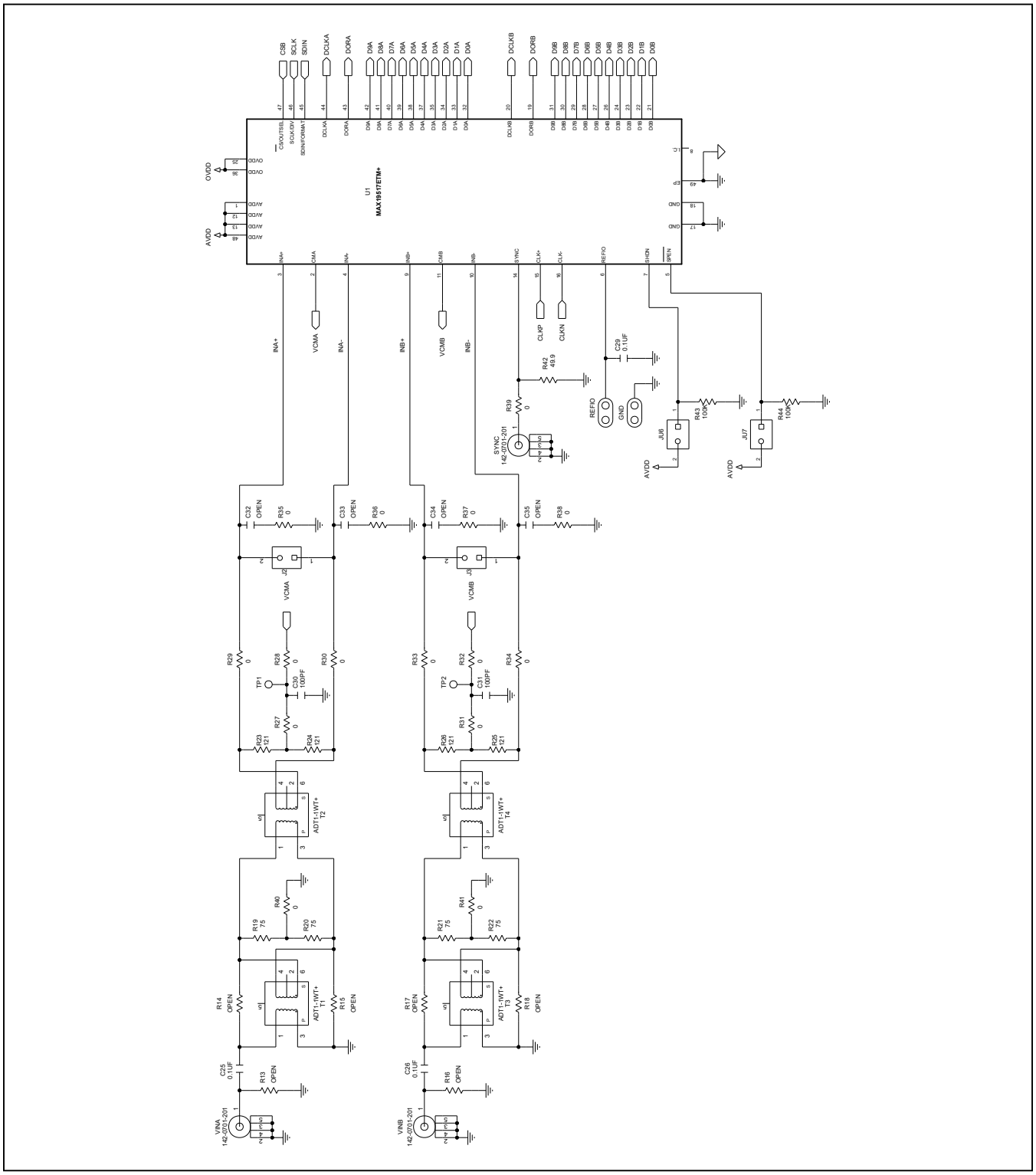
SCLK/DIV (JU1)	SDIN/FORMAT (JU2)	$\overline{CS}$/OUTSEL (JU3)	$\overline{SPEN}$ (JU7)	DESCRIPTION
SCLK	SDIN	$\overline{CS}$	0	Serial port active. Features are programmed through the serial port.
X	0	X	1	Two's complement
X	VDD	X	1	Offset binary
X	(Unconnected pin)	X	1	Gray code
0	X	X	1	Clock divide-by-1
VDD	X	X	1	Clock divide-by-2
(Unconnected pin)	X	X	1	Clock divide-by-4
X	X	0	1	CMOS (dual bus)
X	X	VDD	1	MUX CMOS (channel A data bus)
X	X	(Unconnected pin)	1	MUX CMOS (channel B data bus)

X = Don't care.

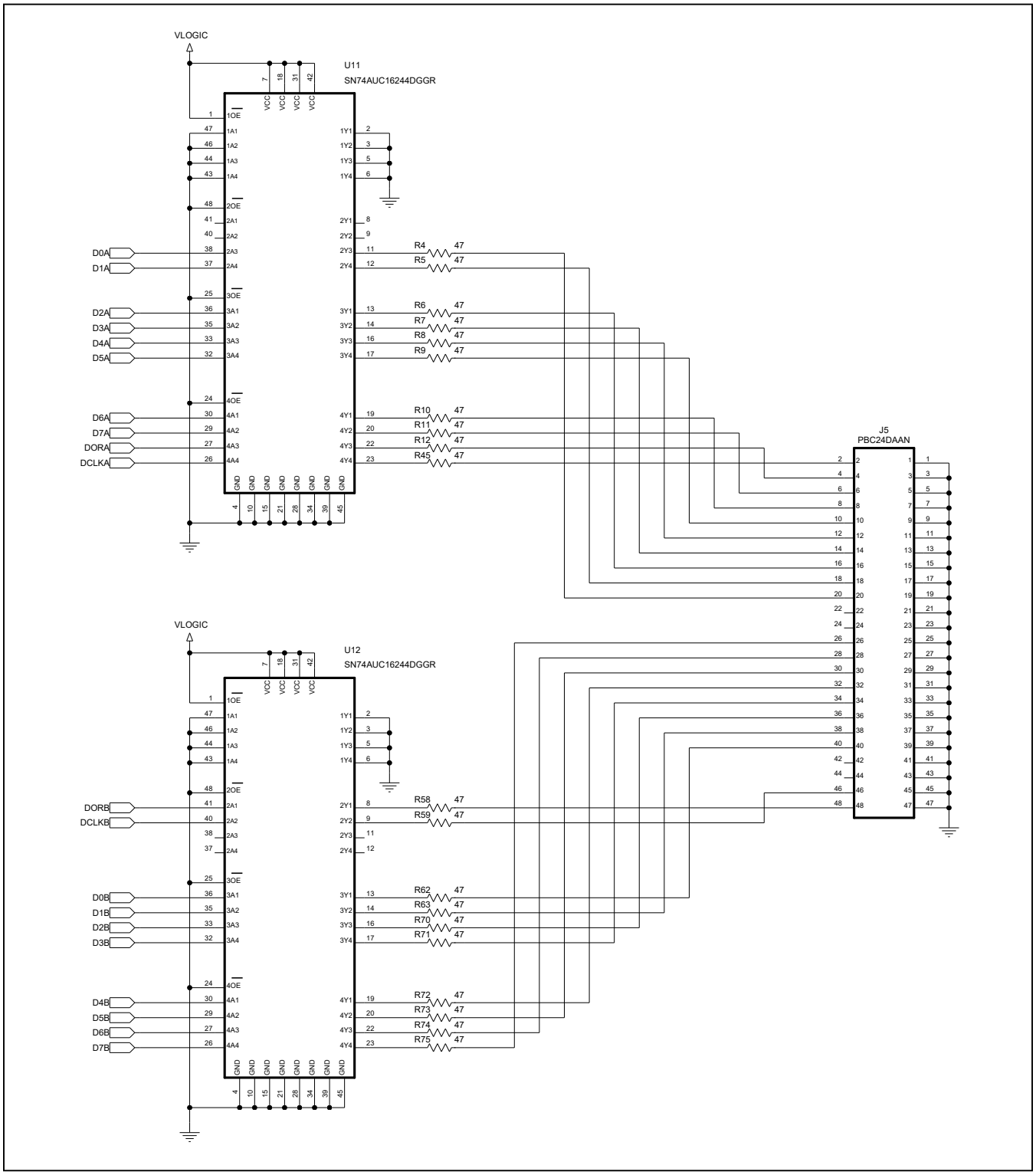
MAX19505/MAX19506/MAX19507 EV Kit Schematics (Sheet 1 of 5)



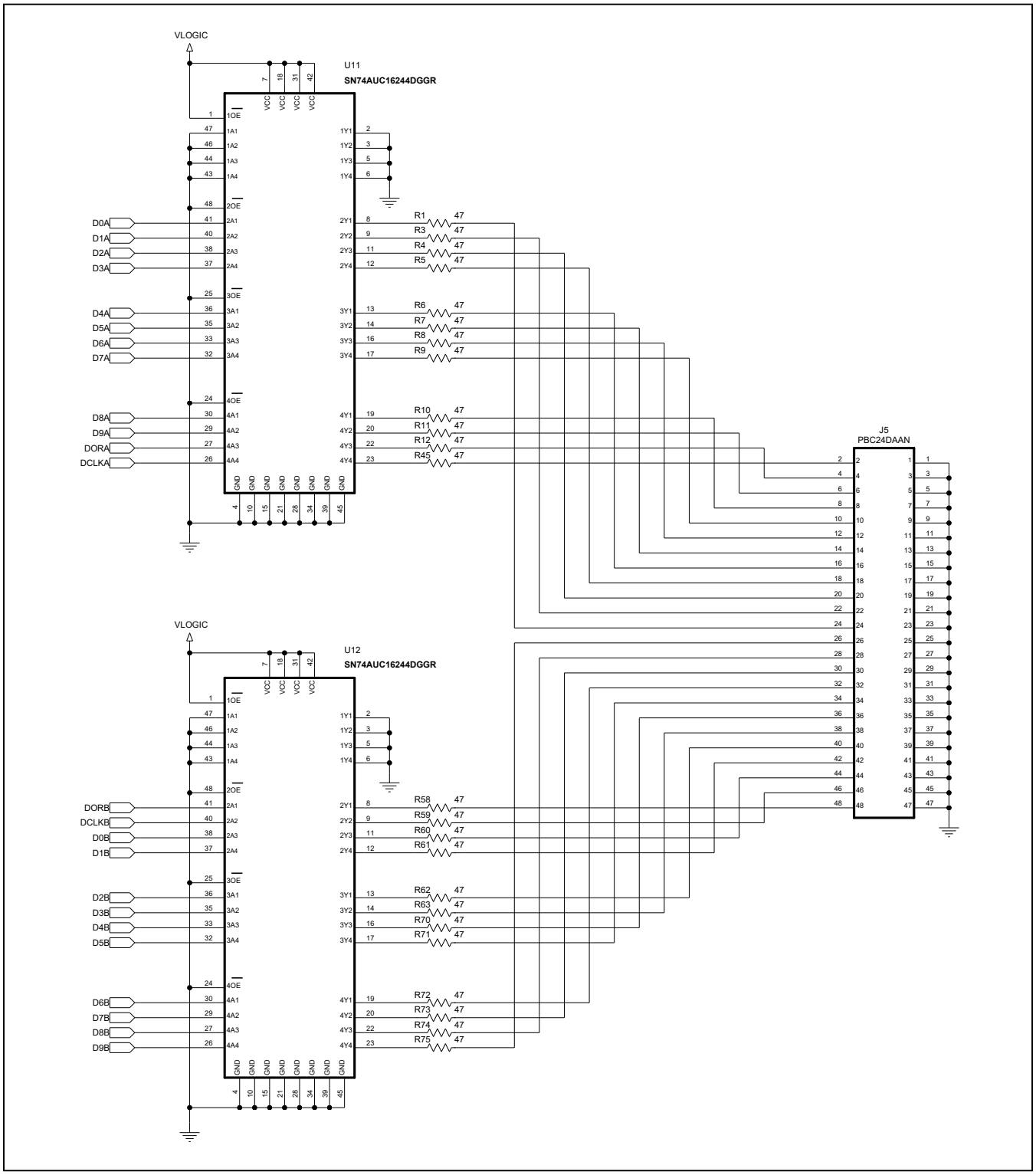
MAX19515/MAX19516/MAX19517 EV Kit Schematics (Sheet 1 of 5)



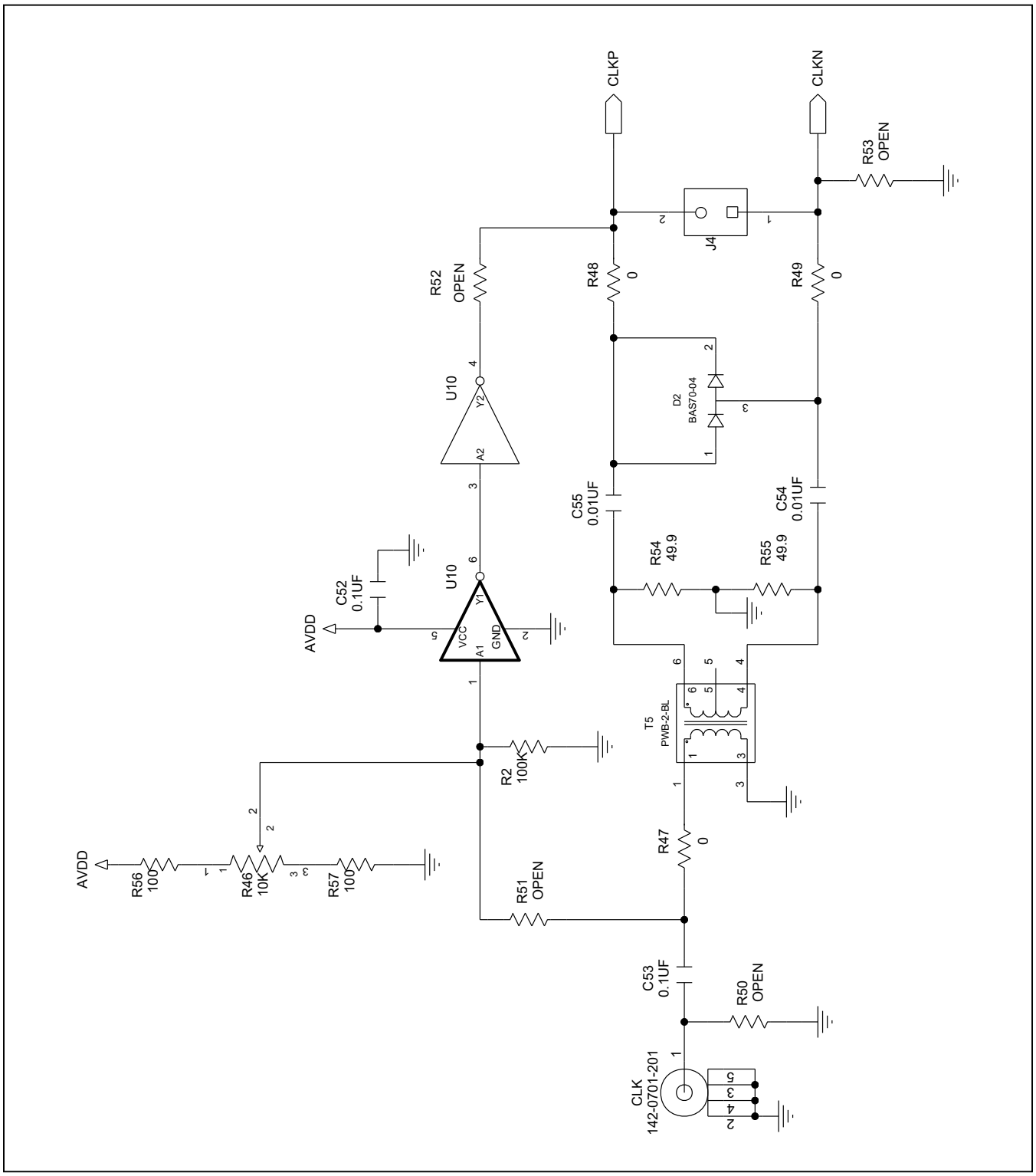
MAX19505/MAX19506/MAX19507 EV Kit Schematics (Sheet 2 of 5)



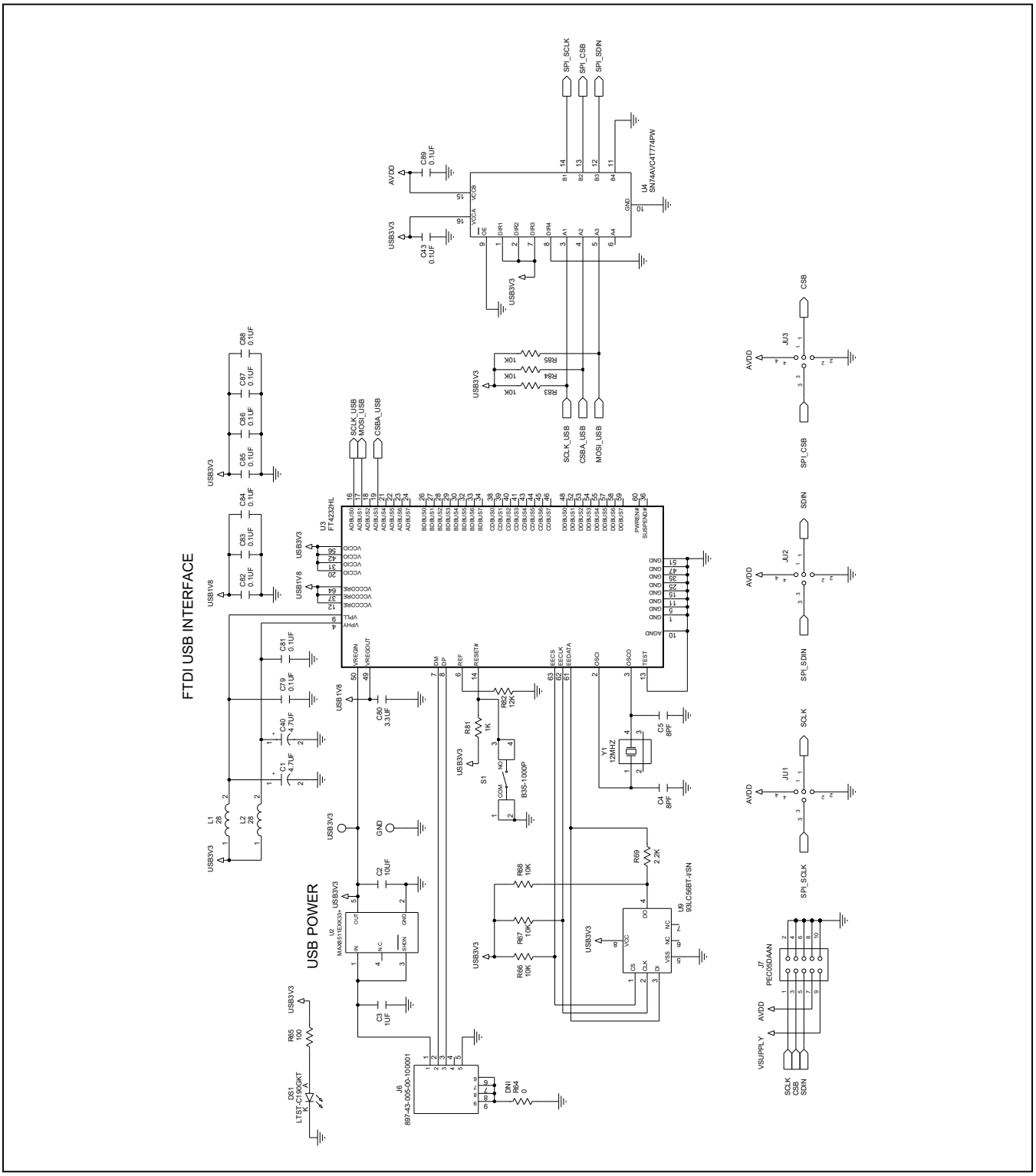
MAX19515/MAX19516/MAX19517 EV Kit Schematics (Sheet 2 of 5)



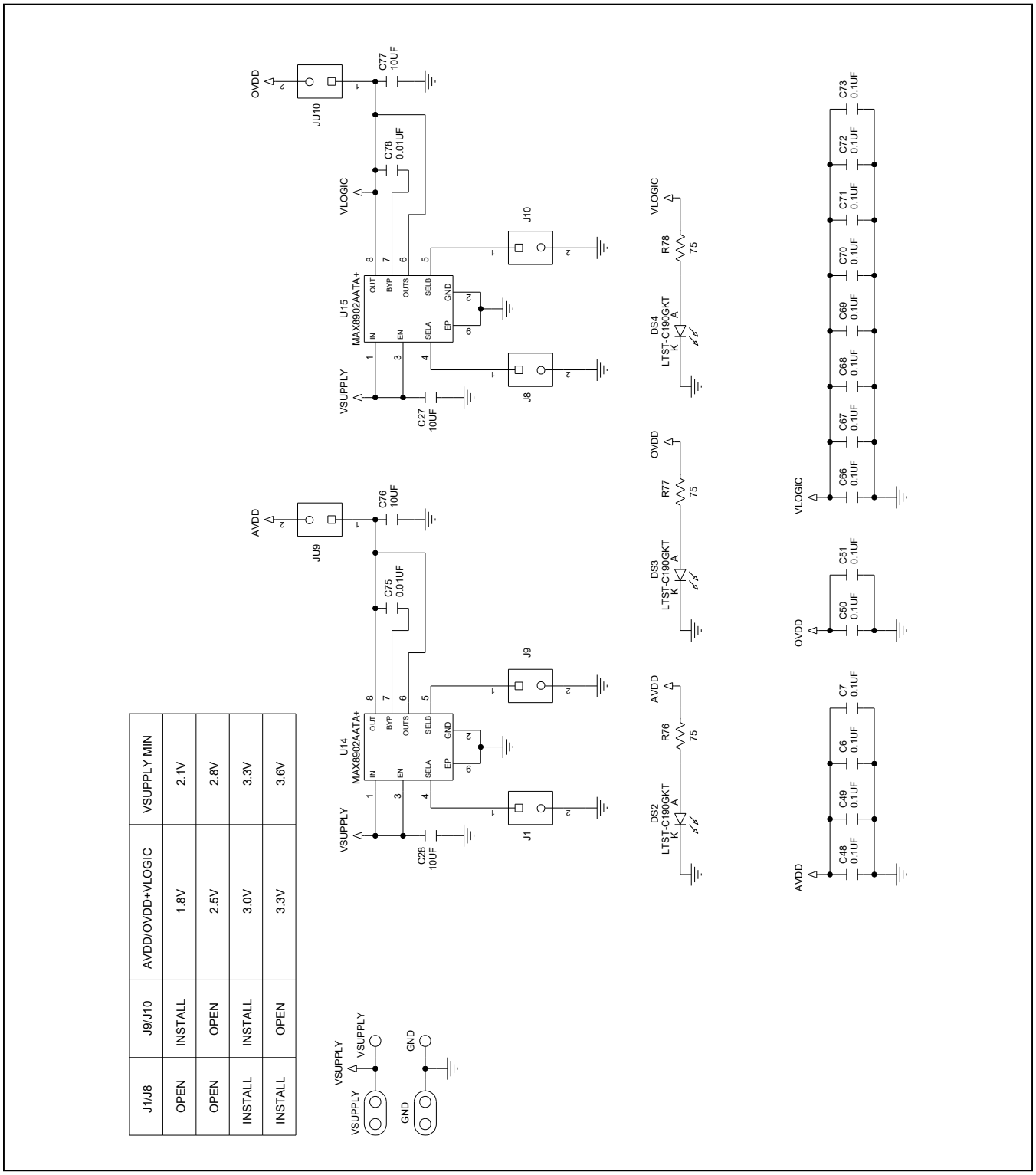
MAX19505–MAX19507/MAX19515–MAX19517 EV Kit Schematics (Sheet 3 of 5)



MAX19505–MAX19507/MAX19515–MAX19517 EV Kit Schematics (Sheet 4 of 5)

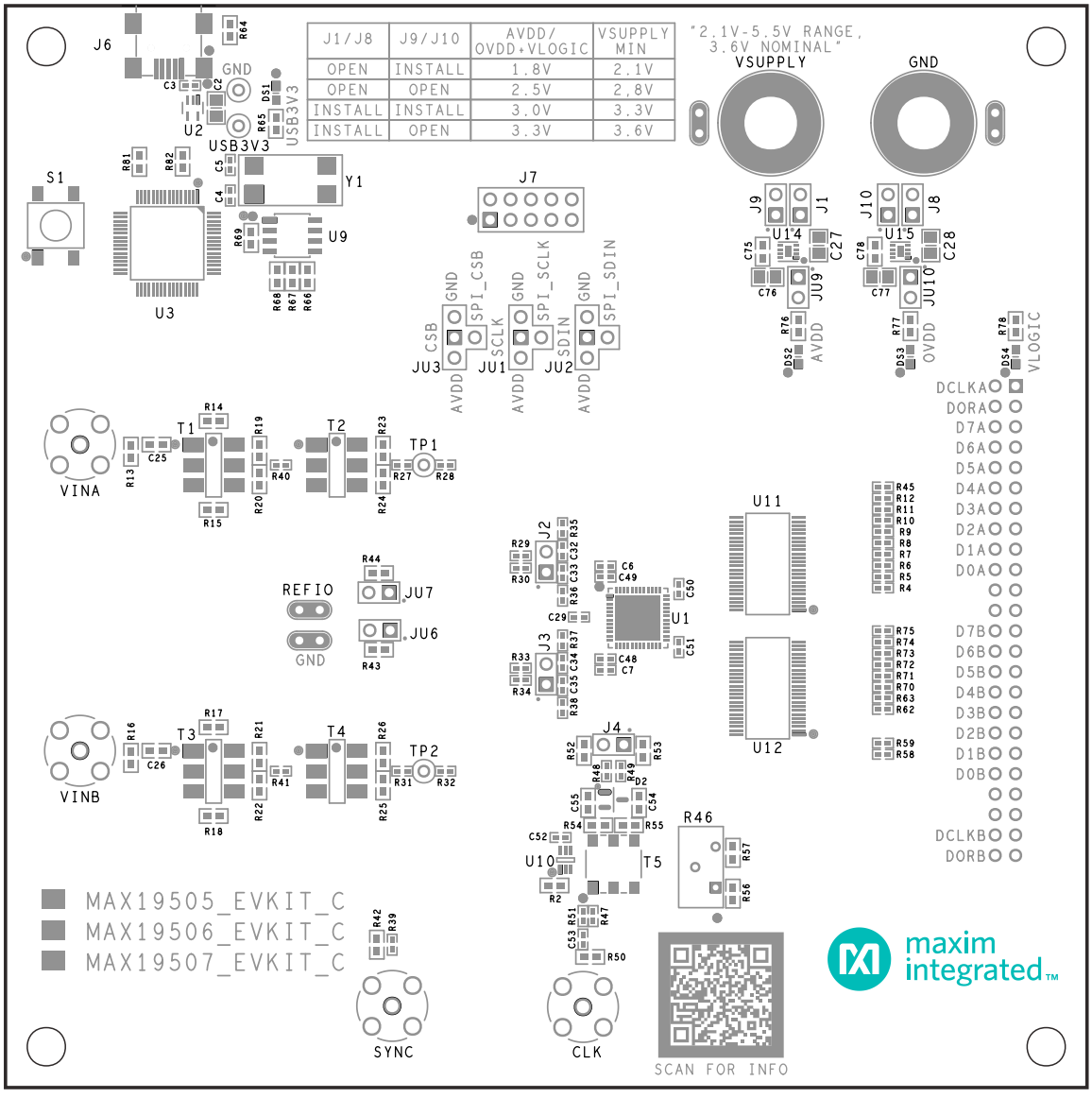


MAX19505–MAX19507/MAX19515–MAX19517 EV Kit Schematics (Sheet 5 of 5)



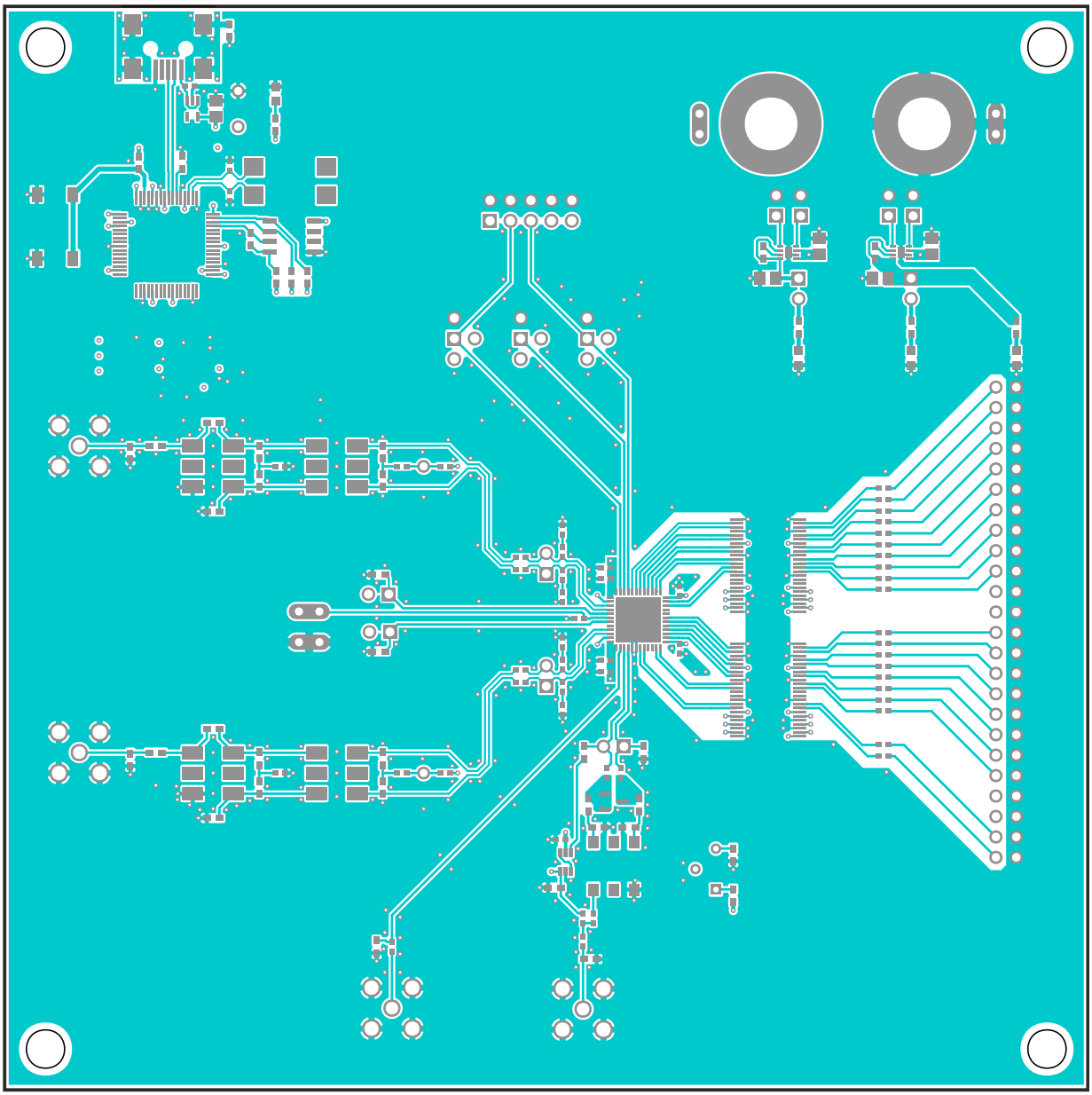
J1/J8	J9/J10	AVDD/OVDD+VLOGIC	VSUPPLY MIN
OPEN	INSTALL	1.8V	2.1V
OPEN	OPEN	2.5V	2.8V
INSTALL	INSTALL	3.0V	3.3V
INSTALL	OPEN	3.3V	3.6V

MAX19505–MAX19507/MAX1915–MAX19517 EV Kit PCB Layout Diagrams



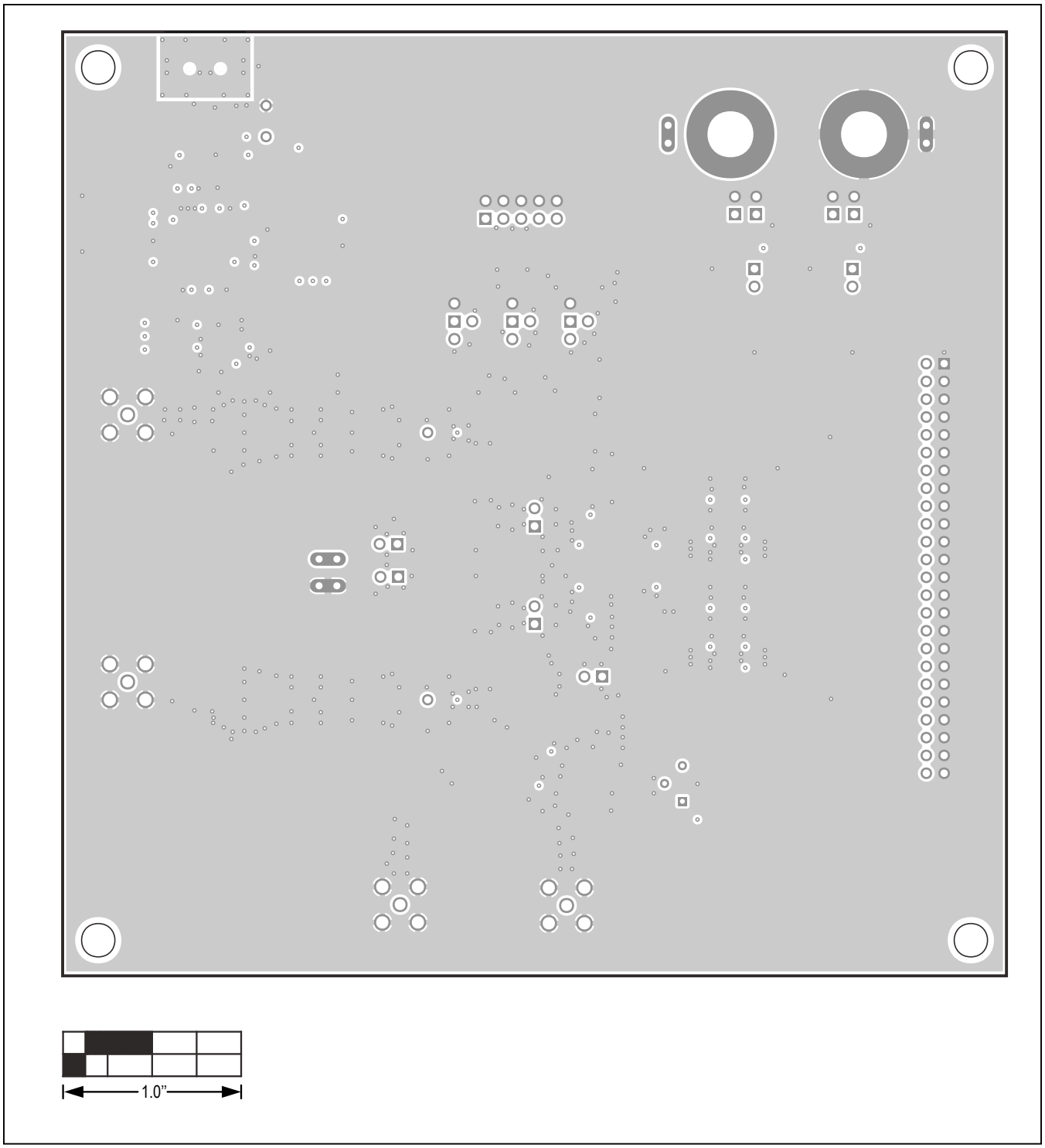
MAX19505/MAX19506/MAX19507 EV Kit PCB Layout—Top Silkscreen

MAX19505–MAX19507/MAX1915–MAX19517 EV Kit PCB Layout Diagrams (cont'd)



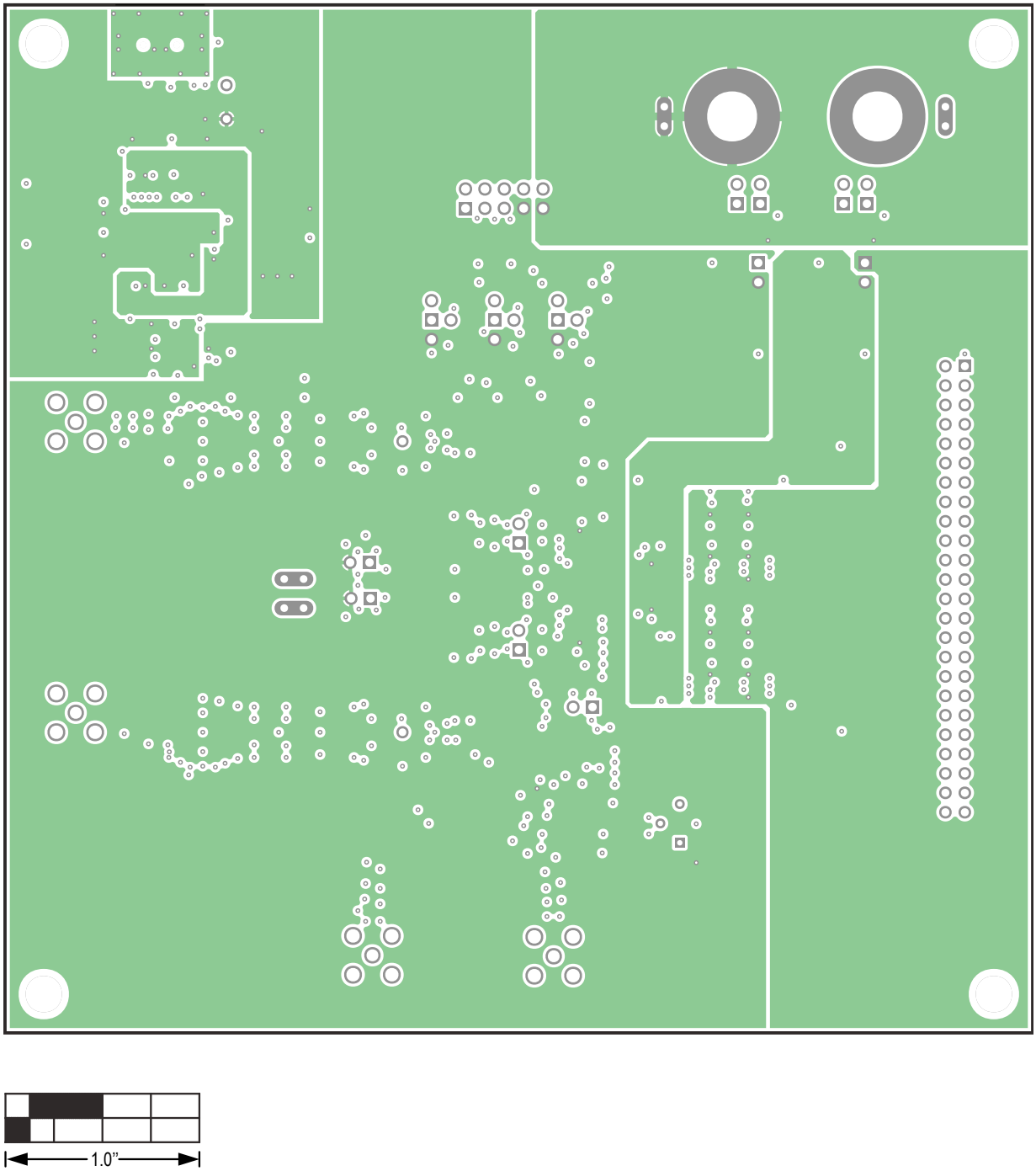
MAX19505/MAX19506/MAX19507 EV Kit PCB Layout—Top Layer

MAX19505–MAX19507/MAX1915–MAX19517 EV Kit PCB Layout Diagrams (cont'd)



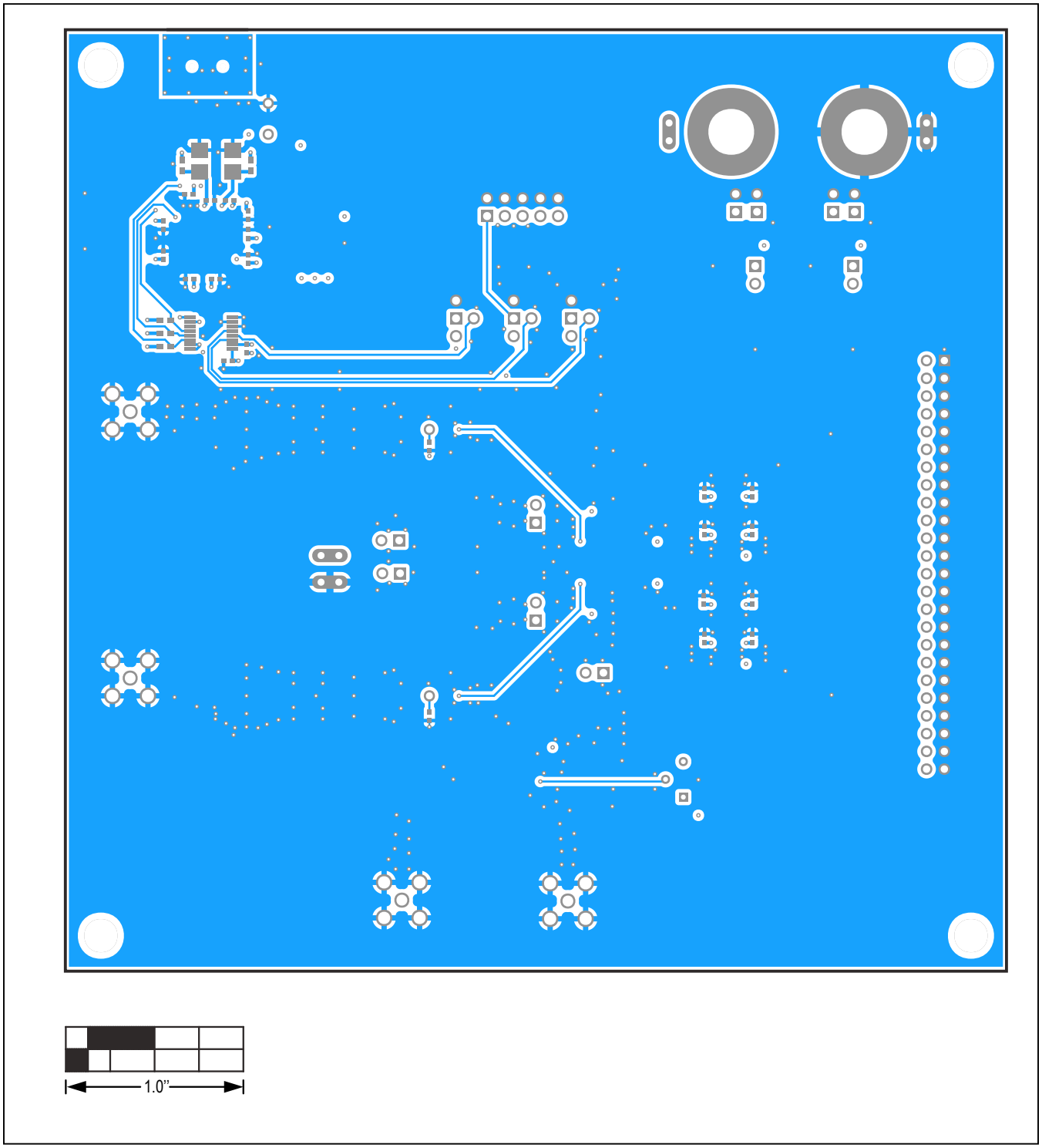
MAX19505/MAX19506/MAX19507 EV Kit PCB Layout—Internal 2

MAX19505–MAX19507/MAX1915–MAX19517 EV Kit PCB Layout Diagrams (cont'd)



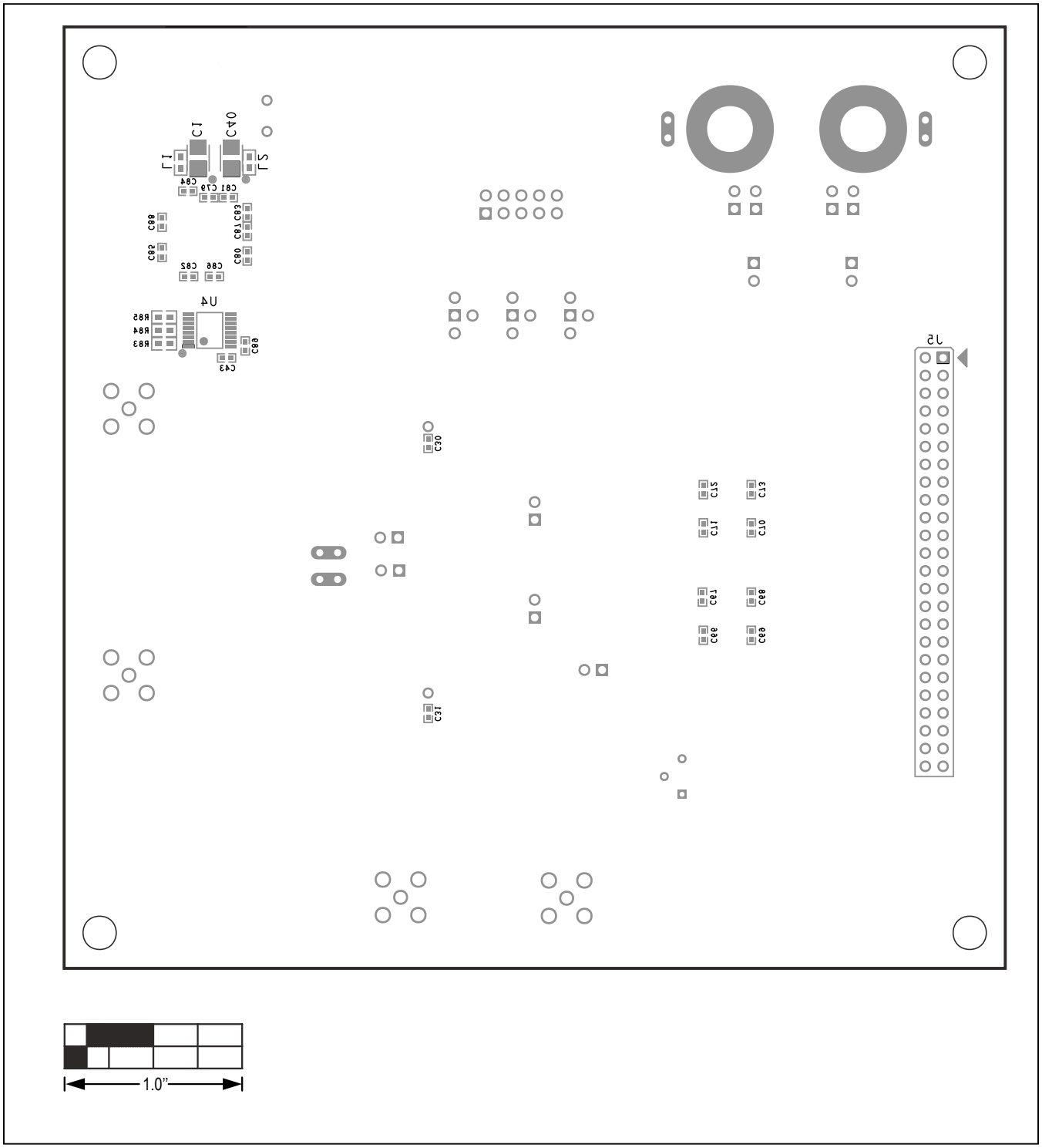
MAX19505/MAX19506/MAX19507 EV Kit PCB Layout—Internal 3

MAX19505–MAX19507/MAX1915–MAX19517 EV Kit PCB Layout Diagrams (cont'd)



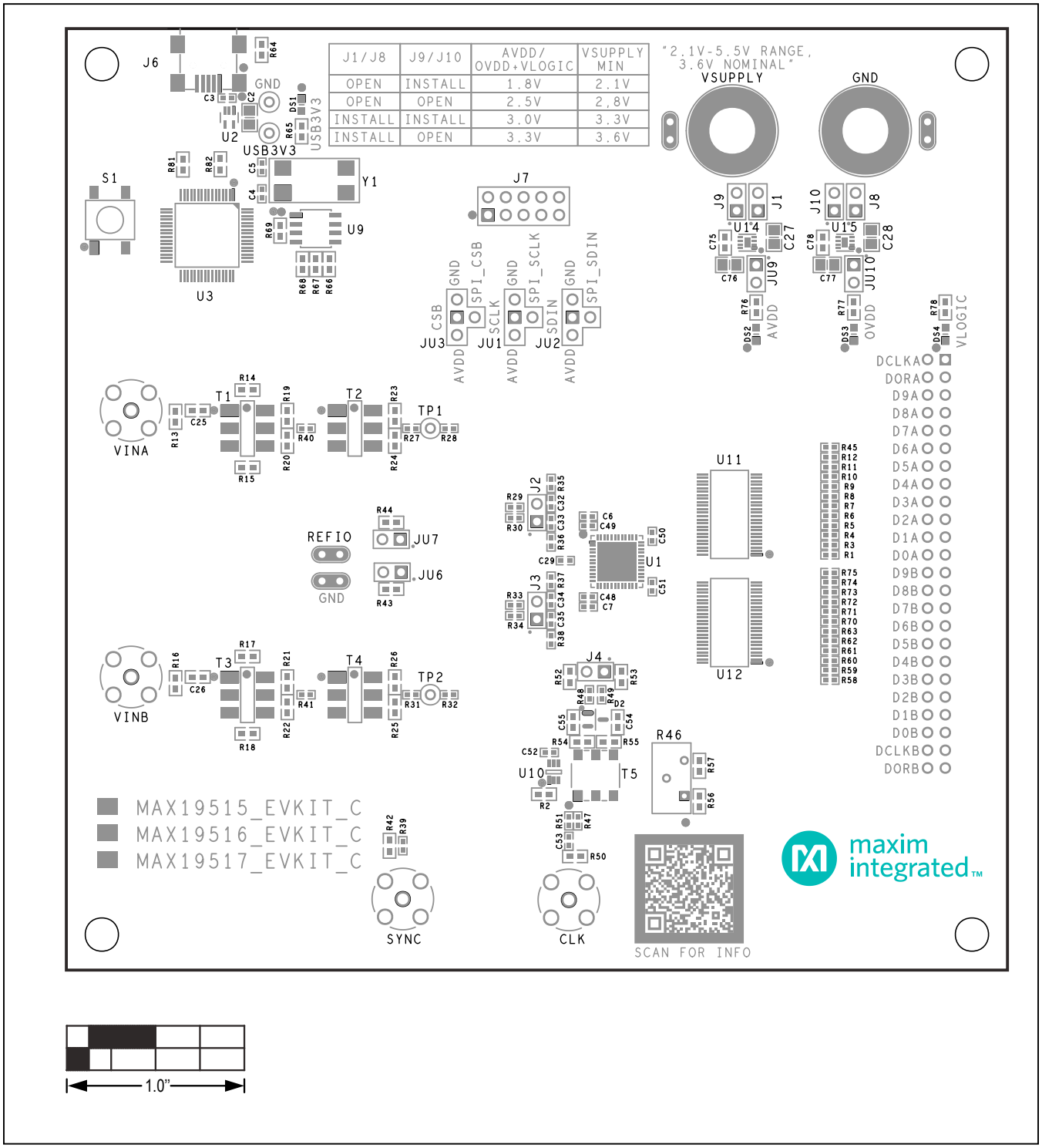
MAX19505/MAX19506/MAX19507 EV Kit PCB Layout—Bottom Layer

MAX19505–MAX19507/MAX1915–MAX19517 EV Kit PCB Layout Diagrams (cont'd)



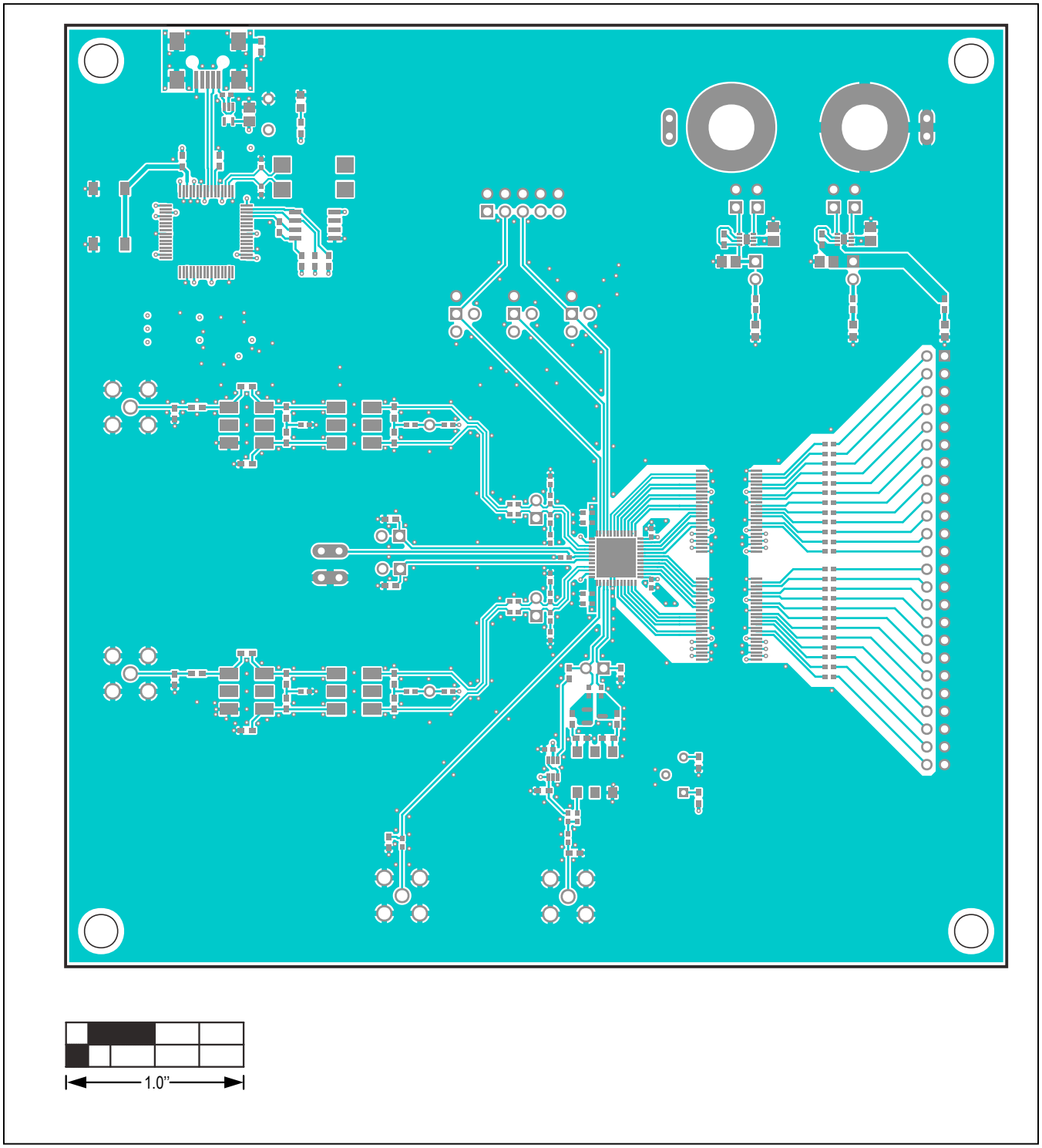
MAX19505/MAX19506/MAX19507 EV Kit PCB Layout—Bottom Silkscreen

MAX19505–MAX19507/MAX1915–MAX19517 EV Kit PCB Layout Diagrams (cont'd)



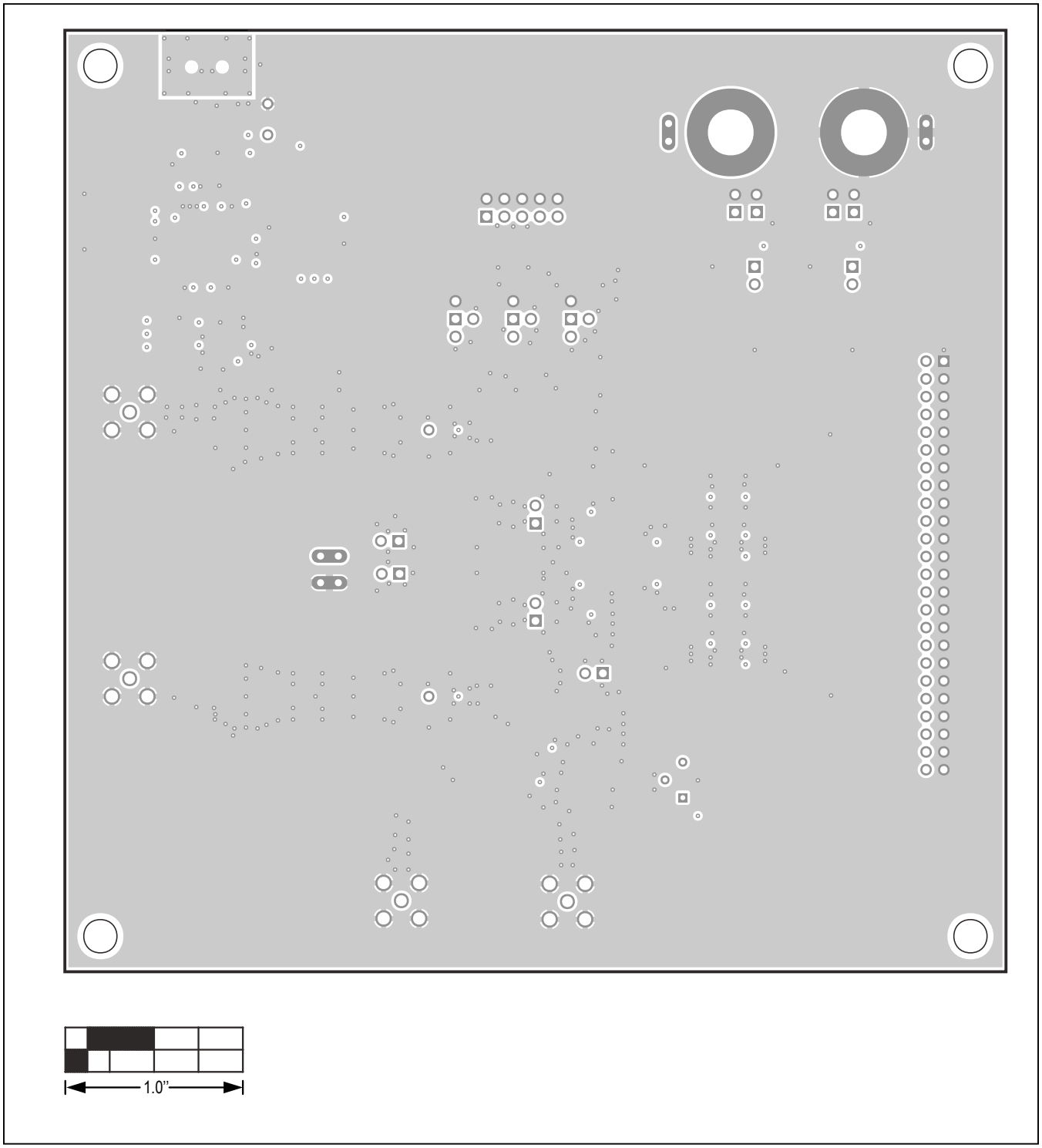
MAX19515/MAX19516/MAX19517 EV Kit PCB Layout—Top Silkscreen

MAX19505–MAX19507/MAX1915–MAX19517 EV Kit PCB Layout Diagrams (cont'd)



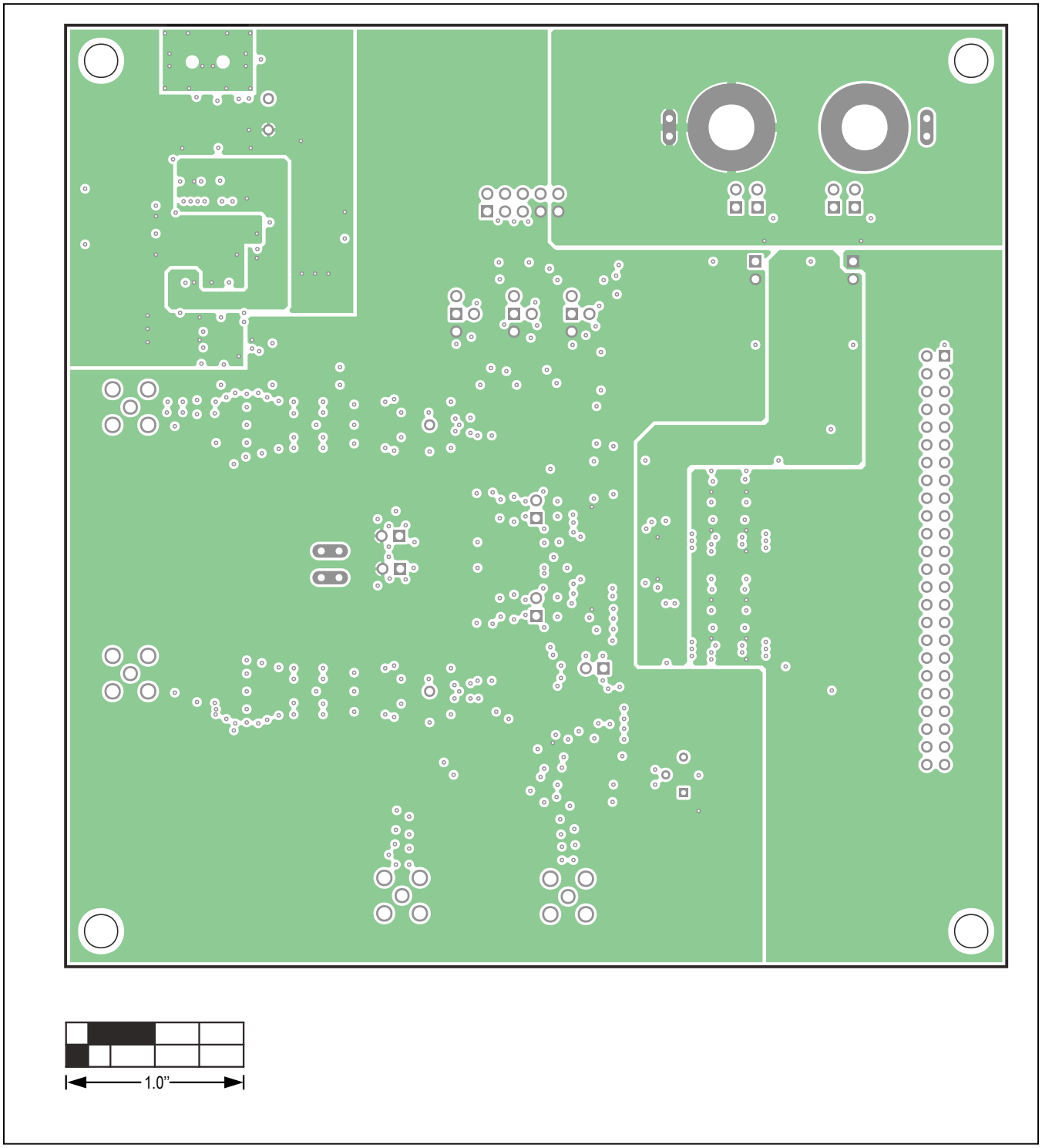
MAX19515/MAX19516/MAX19517 EV Kit PCB Layout—Top Layer

MAX19505–MAX19507/MAX1915–MAX19517 EV Kit PCB Layout Diagrams (cont'd)



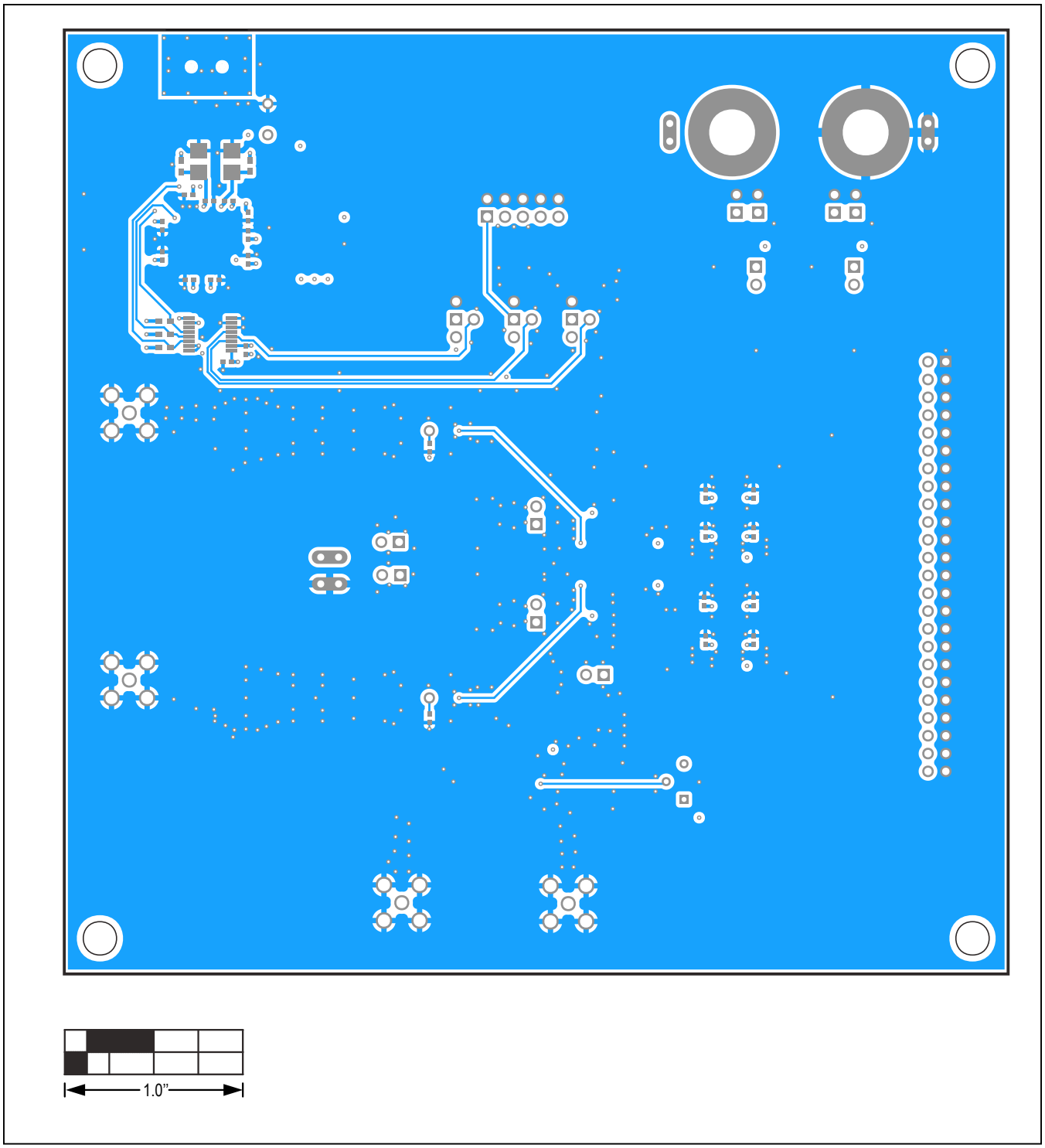
MAX19515/MAX19516/MAX19517 EV Kit PCB Layout—Internal 2

MAX19505–MAX19507/MAX1915–MAX19517 EV Kit PCB Layout Diagrams (cont'd)



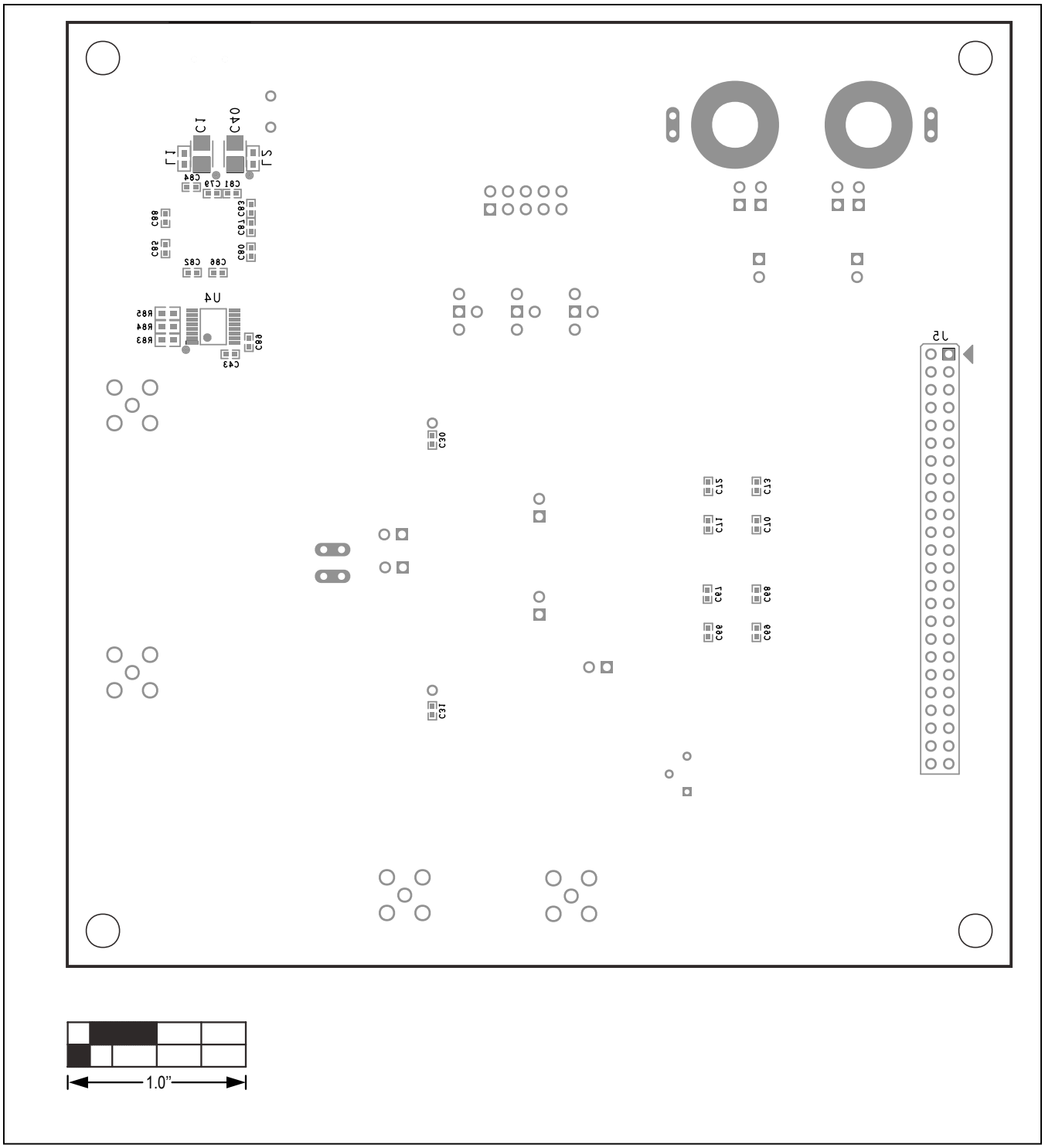
MAX19515/MAX19516/MAX19517 EV Kit PCB Layout—Internal 3

MAX19505–MAX19507/MAX1915–MAX19517 EV Kit PCB Layout Diagrams (cont'd)



MAX19515/MAX19516/MAX19517 EV Kit PCB Layout—Bottom Layer

MAX19505–MAX19507/MAX1915–MAX19517 EV Kit PCB Layout Diagrams (cont'd)



MAX19515/MAX19516/MAX19517 EV Kit PCB Layout—Bottom Silkscreen

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/08	Initial release	—
1	7/09	Corrected connector name on DCEP board	5, 10
2	7/19	Updated to match Rev C and Rev D hardware, plus updated GUI	1–30

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