19-2373; Rev 0; 4/02

EVALUATION KIT AVAILABLE

MAXIM

Low-Cost, High-Frequency, Current-Mode PWM Buck Controller

General Description

The MAX1953/MAX1954/MAX1957 is a family of versatile, economical, synchronous current-mode, pulse-width modulation (PWM) buck controllers. These step-down controllers are targeted for applications where cost and size are critical.

The MAX1953 operates at a fixed 1MHz switching frequency, thus significantly reducing external component size and cost. Additionally, excellent transient response is obtained using less output capacitance. The MAX1953 operates from low 3V to 5.5V input voltage and can supply up to 10A of output current. Selectable current limit is provided to tailor to the external MOSFETs' on-resistance for optimum cost and performance. The output voltage is adjustable from 0.8V to $0.86V_{IN}$.

With the MAX1954, the drain-voltage range on the high-side FET is 3V to 13.2V and is independent of the supply voltage. It operates at a fixed 300kHz switching frequency and can be used to provide up to 25A of output current with high efficiency. The output voltage is adjustable from 0.8V to $0.86V_{HSD}$.

The MAX1957 features a tracking output voltage range of 0.4V to $0.86V_{IN}$ and is capable of sourcing or sinking current for applications such as DDR bus termination and PowerPC™/ASIC/DSP core supplies. The MAX1957 operates from a 3V to 5.5V input voltage and at a fixed 300kHz switching frequency.

The MAX1953/MAX1954/MAX1957 provide a COMP pin that can be pulled low to shut down the converter in addition to providing compensation to the error amplifier. An input undervoltage lockout (ULVO) is provided to ensure proper operation under power-sag conditions to prevent the external power MOSFETs from overheating. Internal digital soft-start is included to reduce inrush current. The MAX1953/MAX1954/MAX1957 are available in tiny 10-pin μMAX packages.

Applications

Printers and Scanners

Graphic Cards and Video Cards

PCs and Servers

Microprocessor Core Supply

Low-Voltage Distributed Power

Telecommunications and Networking

PowerPC is a trademark of Motorola, Inc.

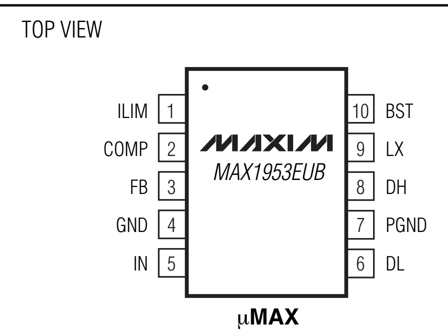
Features

- **Low-Cost Current-Mode Controllers**
- **Fixed-Frequency PWM**
- **MAX1953**
  - **1MHz Switching Frequency**
  - **Small Component Size, Low Cost**
  - **Adjustable Current Limit**
- **MAX1954**
  - **3V to 13.2V Input Voltage**
  - **25A Output Current Capability**
  - **93% Efficiency**
  - **300kHz Switching Frequency**
- **MAX1957**
  - **Tracking 0.4V to $0.86V_{IN}$ Output Voltage Range**
  - **Sinking and Sourcing Capability of 3A**
- **Shutdown Feature**
- **All N-Channel MOSFET Design for Low Cost**
- **No Current-Sense Resistor Needed**
- **Internal Digital Soft-Start**
- **Thermal Overload Protection**
- **Small 10-Pin μMAX Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1953EUB	-40°C to +85°C	10 μMAX
MAX1954EUB	-40°C to +85°C	10 μMAX
MAX1957EUB	-40°C to +85°C	10 μMAX

Pin Configurations



Pin Configurations continued at end of data sheet.

Low-Cost, High-Frequency, Current-Mode PWM Buck Controller

ABSOLUTE MAXIMUM RATINGS

IN, FB to GND ....-0.3V to +6V
LX to BST ....-6V to +0.3V
BST to GND ....-0.3V to +20V
DH to LX ....-0.3V to (V_{BST} + 0.3V)
DL, COMP to GND ....-0.3V to (V_{IN} + 0.3V)
HSD, ILIM, REFIN to GND ....-0.3V to 14V
PGND to GND ....-0.3V to +0.3V
I_{DH}, I_{DL} ....±100mA (RMS)
Continuous Power Dissipation (T_A = +70°C)
(derate 5.6mW/°C above +70°C) 444mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 5V, V_{BST} - V_{LX} = 5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage Range		3.0		5.5	V
HSD Voltage Range	MAX1954 only (Note 2)	3.0		13.2	V
Quiescent Supply Current	V_{FB} = 1.5V, no switching		1	2	mA
Standby Supply Current (MAX1953/ MAX1957)	V_{IN} = V_{BST} = 5.5V, COMP = GND		220	350	µA
Standby Supply Current (MAX1954)	V_{IN} = V_{BST} = 5.5V, V_{HSD} = 13.2V, COMP = GND		220	350	µA
Undervoltage Lockout Trip Level	Rising and falling V_{IN}, 3% hysteresis	2.50	2.78	2.95	V
Output Voltage Adjust Range (V_{OUT})		0.8		0.86 x V_{IN}	V
ERROR AMPLIFIER					
FB Regulation Voltage	**T_A = 0°C to +85°C** (MAX1953/MAX1954)	0.788	0.8	0.812	V
	T_A = -40°C to +85°C (MAX1953/MAX1954)	0.776	0.8	0.812	
	MAX1957 only	V_{REFIN} - 8mV	V_{REFIN}	V_{REFIN} + 8mV	
Transconductance		70	110	160	µS
FB Input Leakage Current	V_{FB} = 0.9V		5	500	nA
REFIN Input Bias Current	V_{REFIN} = 0.8V, MAX1957 only		5	500	nA
FB Input Common-Mode Range		-0.1		1.5	V
REFIN Input Common-Mode Range	MAX1957 only	-0.1		1.5	V
Current-Sense Amplifier Voltage Gain Low	ILIM = GND (MAX1953 only)	5.67	6.3	6.93	V/V
Current-Sense Amplifier Voltage Gain	V_{ILIM} = V_{IN} or ILIM = open (MAX1953 only)	3.15	3.5	3.85	V/V
	MAX1954/MAX1957				

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 5V, V_{BST} - V_{LX} = 5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

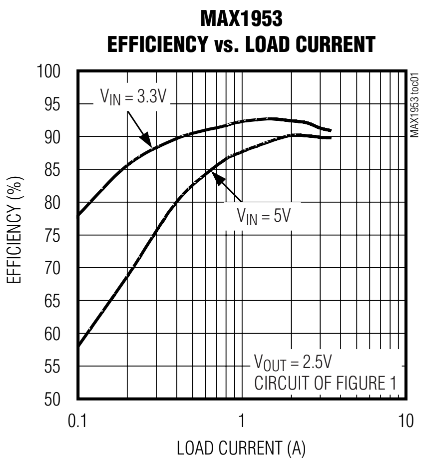
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ILIM Input Impedance	MAX1953 only	50	125	200	kΩ
Current-Limit Threshold	V_{PGND} - V_{LX}, ILIM = GND (MAX1953 only)	85	105	125	mV
	V_{PGND} - V_{LX}, ILIM = open (MAX1953 only)	190	210	235	
	V_{PGND} - V_{LX}, ILIM = IN (MAX1953 only)	290	320	350	
	V_{PGND} – V_{LX} (MAX1954/MAX1957 only)	190	210	235	
OSCILLATOR					
Switching Frequency	MAX1953	0.8	1	1.2	MHz
	MAX1954/MAX1957	240	300	360	kHz
Maximum Duty Cycle	Measured at DH	86	89	96	%
Minimum Duty Cycle	MAX1953, measured at DH		15	18	%
	MAX1954/MAX1957, measured at DH		4.5	5.5	
SOFT-START					
Soft-Start Period	MAX1953		4		ms
	MAX1954/MAX1957		3.4		
FET DRIVERS					
DH On-Resistance, High State			2	3	Ω
DH On-Resistance, Low State			1.5	3	Ω
DL On-Resistance, High State			2	3	Ω
DL On-Resistance, Low State			0.8	2	Ω
LX, BST Leakage Current	V_{BST} = 10.5V, V_{LX} = V_{IN} = 5.5V, MAX1953/MAX1957			20	µA
LX, BST, HSD Leakage Current	V_{BST} = 18.7V, V_{LX} = 13.2V, V_{IN} = 5.5V V_{HSD} = 13.2V (MAX1954 only)			30	µA
THERMAL PROTECTION					
Thermal Shutdown	Rising temperature		160		°C
Thermal Shutdown Hysteresis			15		°C
SHUTDOWN CONTROL					
COMP Logic Level Low	3V ≤ V_{IN} ≤ 5.5V			0.25	V
COMP Logic Level High	3V ≤ V_{IN} ≤ 5.5V	0.8			V
COMP Pullup Current				100	µA

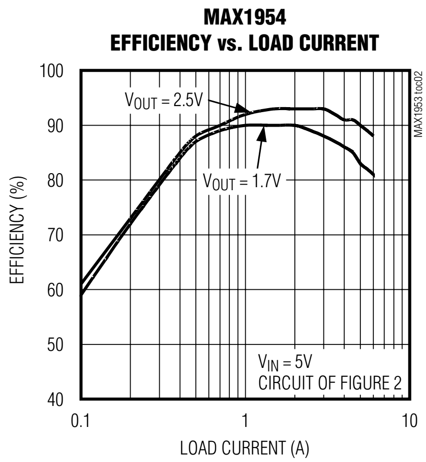
Note 1: Specifications to -40°C are guaranteed by design and not production tested.
Note 2: HSD and IN are externally connected for applications where V_{HSD} < 5.5V.

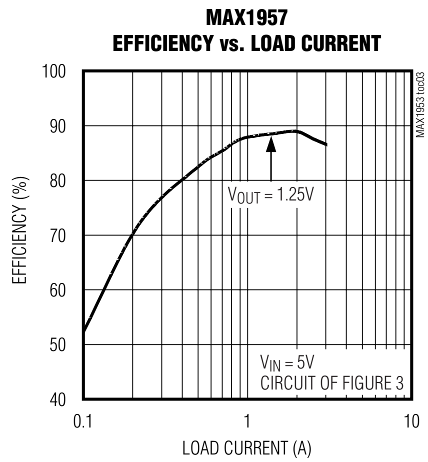
Low-Cost, High-Frequency, Current-Mode PWM Buck Controller

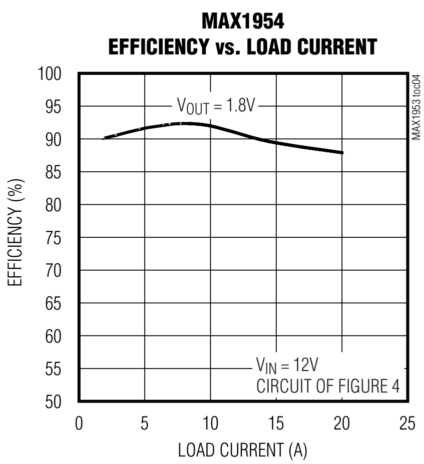
Typical Operating Characteristics

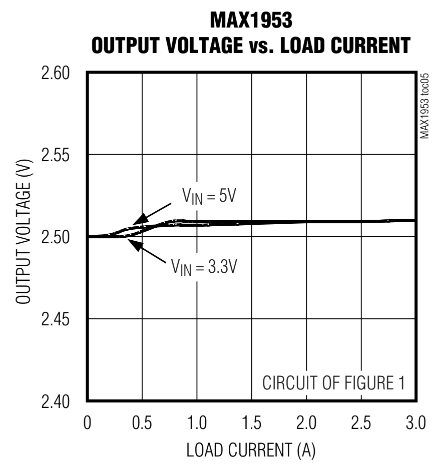
(T_A = +25°C, unless otherwise noted.)

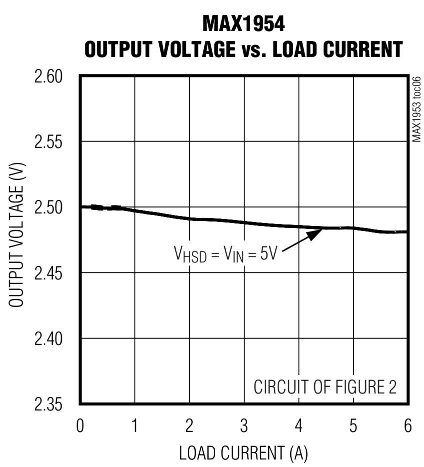


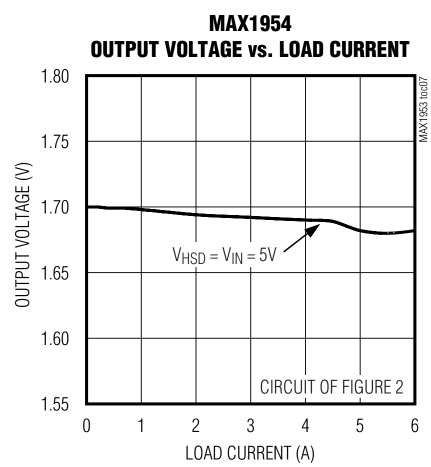






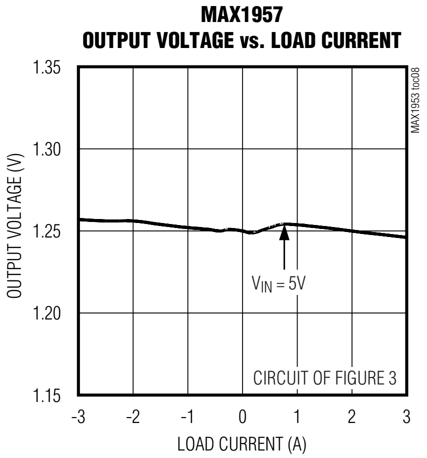


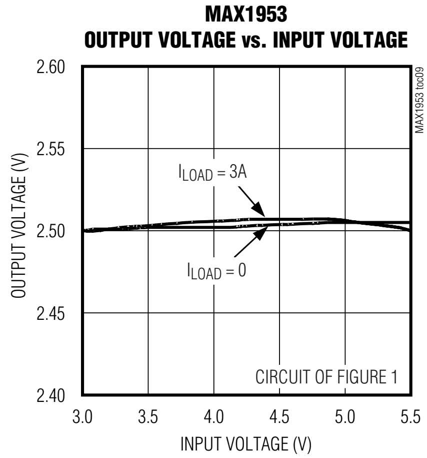


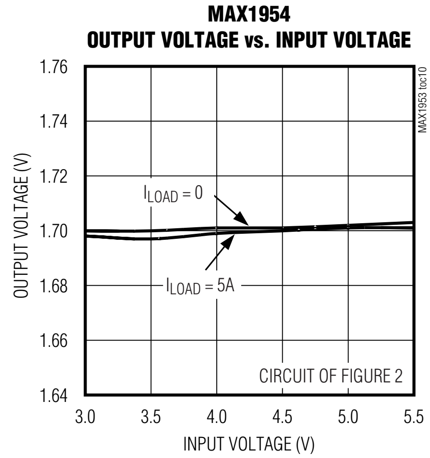


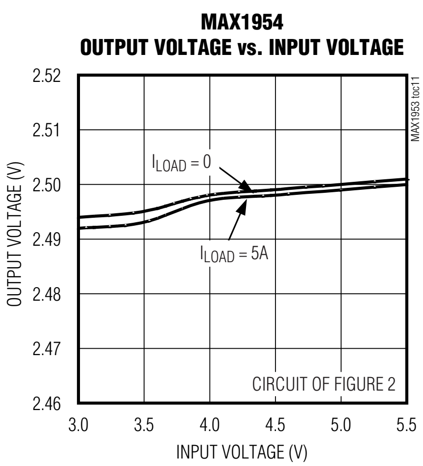
Typical Operating Characteristics (continued)

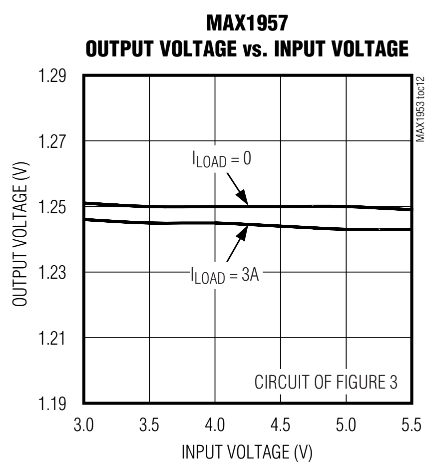
(T_A = +25°C, unless otherwise noted.)

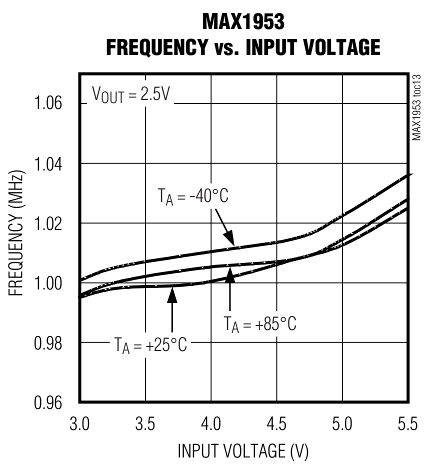


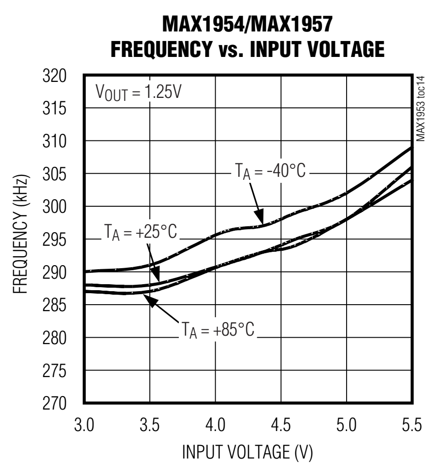








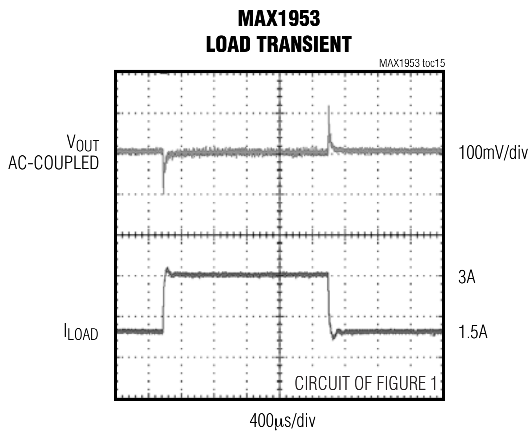


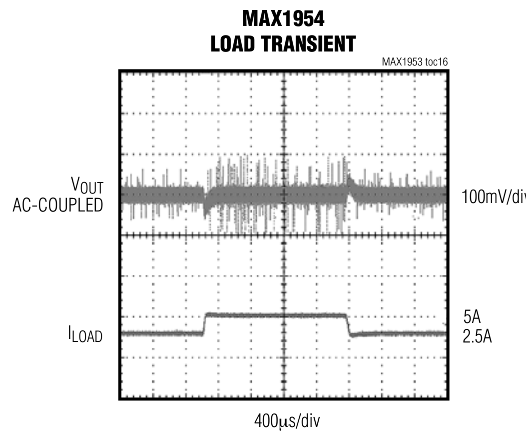


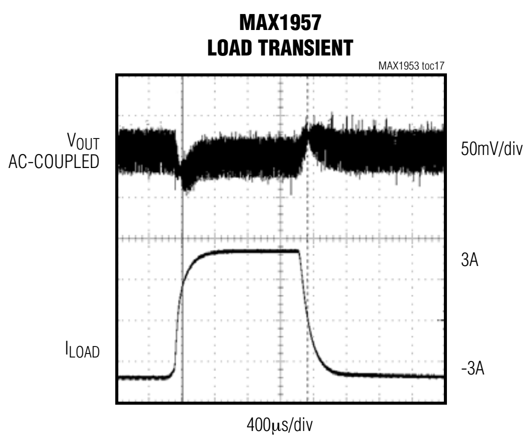
Low-Cost, High-Frequency, Current-Mode PWM Buck Controller

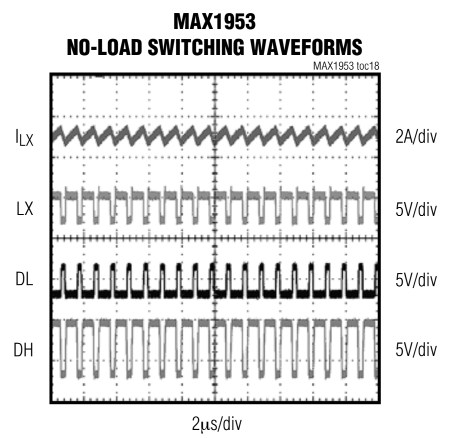
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)





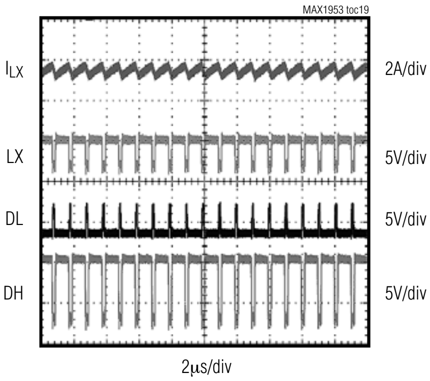




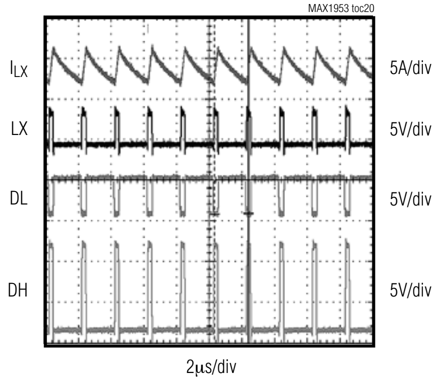
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

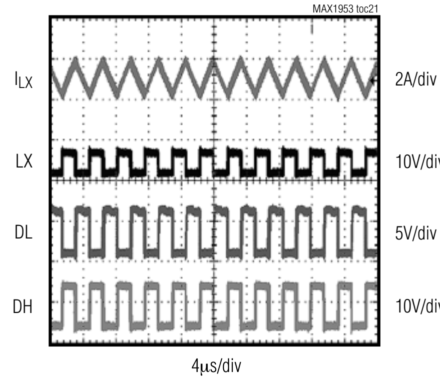
MAX1953
FULL-LOAD SWITCHING WAVEFORMS



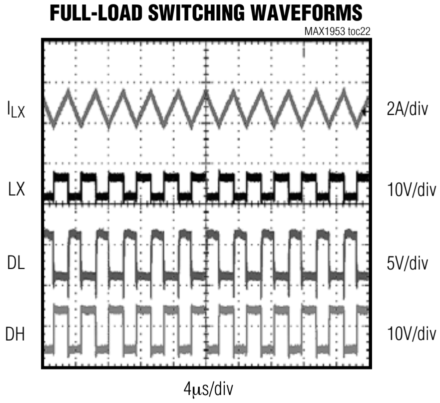
MAX1953
SHORT-CIRCUIT SWITCHING WAVEFORMS



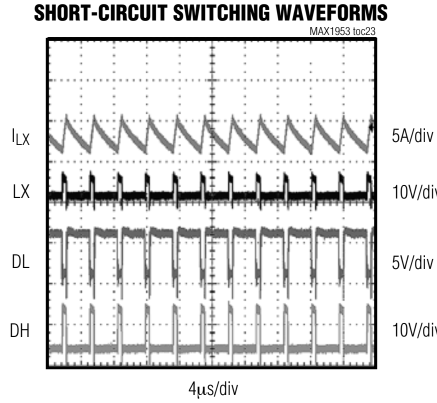
MAX1954/MAX1957
NO-LOAD SWITCHING WAVEFORMS



MAX1954/MAX1957
FULL-LOAD SWITCHING WAVEFORMS



MAX1954/MAX1957
SHORT-CIRCUIT SWITCHING WAVEFORMS

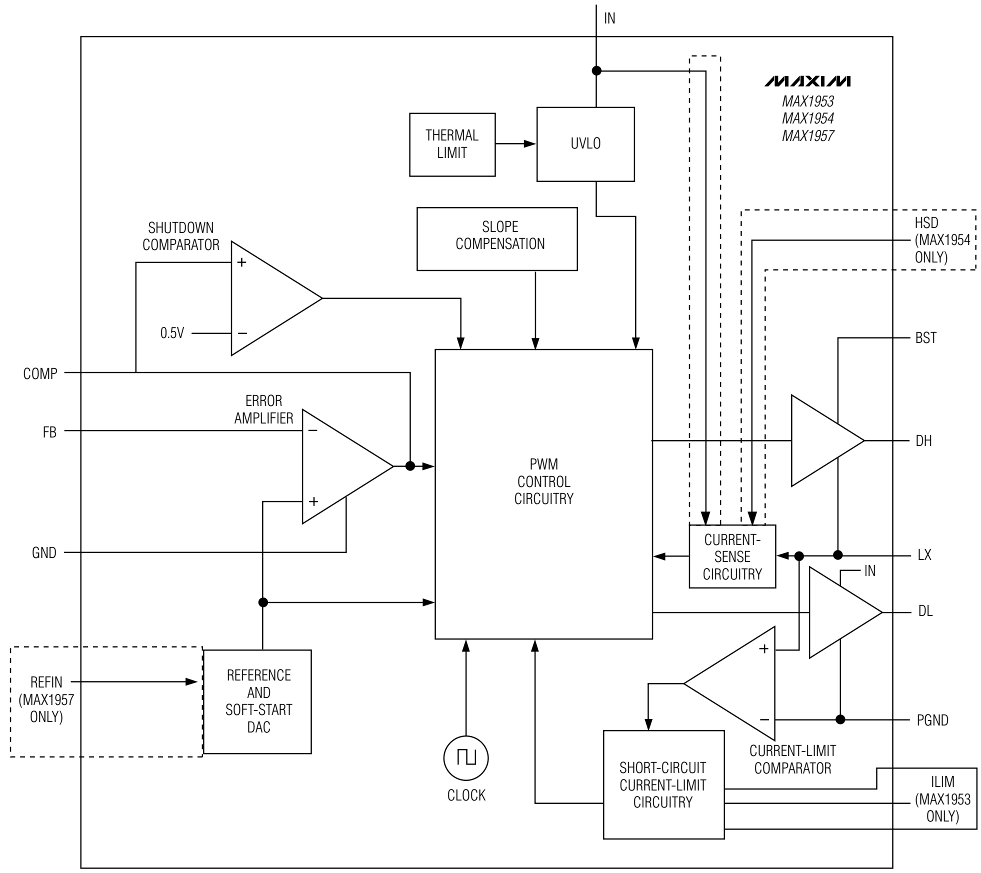


Low-Cost, High-Frequency, Current-Mode PWM Buck Controller

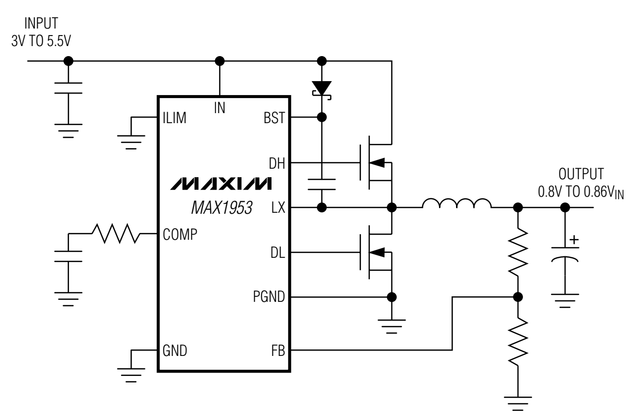
Pin Description

PIN			NAME	FUNCTION
MAX1953	MAX1954	MAX1957		
1	—	—	ILIM	ILIM Sets the Current-Limit Threshold for the Low-Side N-Channel MOSFET, as well as the Current-Sense Amplifier Gain. Connect to IN for 320mV, leave floating for 210mV, or connect to GND for 105mV current-limit threshold.
—	1	—	HSD	HSD Senses the Voltage at the Drain of the High-Side N-Channel MOSFET. Connect to the high-side MOSFET drain using a Kelvin connection.
—	—	1	REFIN	REFIN Sets the FB Regulation Voltage. Drive REFIN with the desired FB regulation voltage using an external resistor-divider. Bypass to GND with a 0.1µF capacitor.
2	2	2	COMP	Compensation and Shutdown Control Pin. Connect an RC network to compensate control loop. Drive to GND to shut down the IC.
3	3	3	FB	Feedback Input. Regulates at V_{FB} = 0.8V (MAX1953/MAX1954) or REFIN (MAX1957). Connect FB to a resistor-divider to set the output voltage (MAX1953/MAX1954). Connect to output through a decoupling resistor (MAX1957).
4	4	4	GND	Ground
5	5	5	IN	Input Voltage (3V to 5.5V). Provides power for the IC. For the MAX1953/MAX1957, IN serves as the current-sense input for the high-side MOSFET. Connect to the drain of the high-side MOSFET (MAX1953/MAX1957). Bypass IN to GND close to the IC with a 0.22µF (MAX1954) capacitor. Bypass IN to GND close to the IC with 10µF and 4.7µF in parallel (MAX1953/MAX1957) capacitors. Use ceramic capacitors.
6	6	6	DL	Low-Side Gate-Drive Output. Drives the synchronous-rectifier MOSFET. Swings from PGND to V_{IN}.
7	7	7	PGND	Power Ground. Connect to source of the synchronous rectifier close to the IC.
8	8	8	DH	High-Side Gate-Drive Output. Drives the high-side MOSFET. DH is a floating driver output that swings from V_{LX} to V_{BST}.
9	9	9	LX	Master Controller Current-Sense Input. Connect LX to the junction of the MOSFETs and inductor. LX is the reference point for the current limit.
10	10	10	BST	Boost Capacitor Connection for High-Side Gate Driver. Connect a 0.1µF ceramic capacitor from BST to LX and a Schottky diode to IN.

Functional Diagram



Typical Operating Circuit



Detailed Description

The MAX1953/MAX1954/MAX1957 are single-output, fixed-frequency, current-mode, step-down, PWM, DC-DC converter controllers. The MAX1953 switches at 1MHz, allowing the use of small external components for small applications. Table 1 lists suggested components.

The MAX1954 switches at 300kHz for higher efficiency and operates from a wider range of input voltages. Figure 1 is the MAX1953 typical application circuit. The MAX1953/MAX1954/MAX1957 are designed to drive a pair of external N-channel power MOSFETs in a synchronous buck topology to improve efficiency and cost compared with a P-channel power MOSFET topology.

The on-resistance of the low-side MOSFET is used for short-circuit current-limit sensing, while the high-side MOSFET on-resistance is used for current-mode feedback and current-limit sensing, thus eliminating the need for current-sense resistors. The MAX1953 has three selectable short-circuit current-limit thresholds: 105mV, 210mV, and 320mV. The MAX1954 and MAX1957 have 210mV fixed short-circuit current-limit thresholds. The MAX1953/MAX1954/MAX1957 accept input voltages from 3V to 5.5V. The MAX1954 is configured with a high-side drain input (HSD) allowing an extended input voltage range of 3V to 13.2V that is independent of the input supply (Figure 2). The MAX1957 is tailored for tracking output voltage applications such as DDR bus termination supplies, referred to as V_{TT}. It utilizes a resistor-divider network connected to REFIN to keep the 1/2 ratio tracking between V_{TT} and V_{DDQ} (Figure 3). The MAX1957 can source and sink up to 3A. Figure 4 shows the MAX1954 20A circuit.

DC-DC Converter Control Architecture

The MAX1953/MAX1954/MAX1957 step-down converters use a PWM, current-mode control scheme. An internal transconductance amplifier establishes an integrated error voltage. The heart of the PWM controller is an open-loop comparator that compares the integrated voltage-feedback signal against the amplified current-sense signal plus the slope compensation ramp, which are summed into the main PWM comparator to preserve inner-loop stability and eliminate inductor staircasing. At each rising edge of the internal clock, the high-side MOSFET turns on until the PWM comparator trips or the maximum duty cycle is reached. During this on-time, current ramps up through the inductor, storing energy in a magnetic field and sourcing current to the output. The current-mode feedback system regulates the peak inductor current as a function of the output voltage error signal. The circuit acts as a switch-mode transconductance amplifier and pushes the output LC filter pole normally found in a voltage-mode PWM to a higher frequency.

During the second half of the cycle, the high-side MOSFET turns off and the low-side MOSFET turns on. The inductor releases the stored energy as the current ramps down, providing current to the output. The output capacitor stores charge when the inductor current exceeds the required load current and discharges when the inductor current is lower, smoothing the voltage across the load. Under overload conditions, when the inductor current exceeds the selected current-limit (see the *Current Limit Circuit* section), the high-side MOSFET is not turned on at the rising clock edge and the low-side MOSFET remains on to let the inductor current ramp down.

The MAX1953/MAX1954/MAX1957 operate in a forced-PWM mode. As a result, the controller maintains a constant switching frequency, regardless of load, to allow for easier postfiltering of the switching noise.

Table 1. Suggested Components

DESIGNATION	MAX1953	MAX1954	MAX1957	20A CIRCUIT
C1	10µF, 6.3V X5R CER Taiyo Yuden JMK212BJ106MG	0.22µF, 10V X7R CER Kemet C0603C224M8RAC	3 x 22µF, 6.3V X5R CER Taiyo Yuden JMK316BJ226ML	0.22µF, 10V X7R CER Kemet C0603C224M8RAC
C2	0.1µF, 50V X7R CER Taiyo Yuden UMK107BJ104KA	10µF, 6.3V X5R CER Taiyo Yuden JMK212BJ106MG	0.1µF, 50V X7R CER Taiyo Yuden UMK107BJ104KA	10µF, 6.3V X5R CER Taiyo Yuden JMK212BJ106MG
C3	10µF, 6.3V X5R CER Taiyo Yuden JMK212BJ106MG	0.1µF, 50V X7R CER Taiyo Yuden UMK107BJ104KA	270µF, 2V SP Polymer Panasonic EEFUEOD271R	10µF, 6.3V X5R CER Taiyo Yuden JMK212BJ106MG

Table 1. Suggested Components (continued)

DESIGNATION	MAX1953	MAX1954	MAX1957	20A CIRCUIT
C4	10µF, 6.3V X5R CER Taiyo Yuden JMK212BJ106MG	180µF, 4V SP Polymer Panasonic EEFUEOG181R	270µF, 2V SP Polymer Panasonic EEFUEOD271R	10µF, 6.3V X5R CER Taiyo Yuden JMK212BJ106MG
C5	4.7µF, 6.3V X5R CER Taiyo Yuden JMK212BJ475MG	—	270µF, 2V SP Polymer Panasonic EEFUEOD271R	10µF, 6.3V X5R CER Taiyo Yuden JMK212BJ106MG
C6	10µF, 6.3V X5R CER Taiyo Yuden JMK212BJ106MG	—	10µF, 6.3V X5R CER Taiyo Yuden JMK212BJ106MG	10µF, 6.3V X5R CER Taiyo Yuden JMK212BJ106MG
C7	—	—	4.7µF, 6.3V X5R CER Taiyo Yuden JMK212BJ475MG	0.1µF, 50V X7R CER Taiyo Yuden UMK107BJ104KA
C8	—	—	0.1µF, 50V X7R CER Taiyo Yuden UMK107BJ104KA	270µF, 2V SP polymer Panasonic EEFUEOD271R
C9-C13	—	—	—	270µF, 2V SP polymer Panasonic EEFUEOD271R
C14	—	—	1500pF, 50V X7R CER Murata GRM39X7R152K50	—
C_C	270pF, 10V X7R CER Kemet C0402C271M8RAC	1000pF, 10V X7R CER Kemet C0402C102M8RAC	470pF, 50V X7R CER Murata GRM39X7R471K50	560pF, 10V X7R CER Kemet C0402C561M8RAC
C_f	—	47pF, 10V C0G CER Kemet C0402C470K8GAC	68pF, 50V COG CER Murata GRM39COG680J50	15pF, 10V C0G CER Kemet C0402C150K8GAC
D1	Schottky diode Central Semiconductor CMPSH1-4	Schottky diode Central Semiconductor CMPSH1-4	Schottky diode Central Semiconductor CMPSH1-4	Schottky diode Central Semiconductor CMPSH1-4
L1	1µH 3.6A Toko 817FY-1R0M	2.7µH 6.6A Coilcraft DO3316-272HC	2.7µH 6.6A Coilcraft DO3316-272HC	0.8µH 27.5A Sumida CEP125U-0R8
N1-N2	Dual MOSFET 20V 5A Fairchild FDS6898A	Dual MOSFET 20V Fairchild FDS6890A	Dual MOSFET 20V Fairchild FDS6898A	N-channel 30V International Rectifier IRF7811W
N3-N4	—	—	—	N-channel 30V Siliconix Si4842DY
R1	16.9kΩ 1%	9.09kΩ 1%	2kΩ 1%	10kΩ 1%
R2	8.06kΩ 1%	8.06kΩ 1%	2kΩ 1%	8.06kΩ 1%
R3			10kΩ 5%	
R_C	33kΩ 5%	62kΩ 5%	51.1kΩ 5%	270kΩ 5%

Low-Cost, High-Frequency, Current-Mode PWM Buck Controller

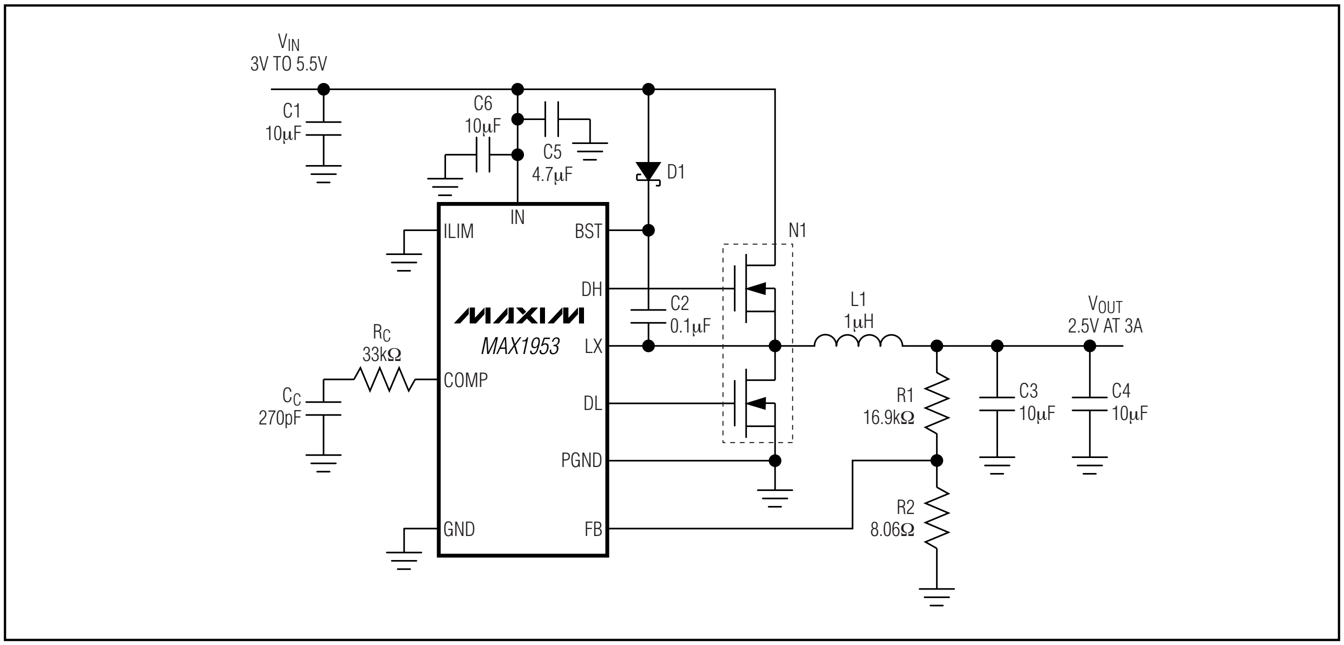


Figure 1. Typical Application Circuit for the MAX1953

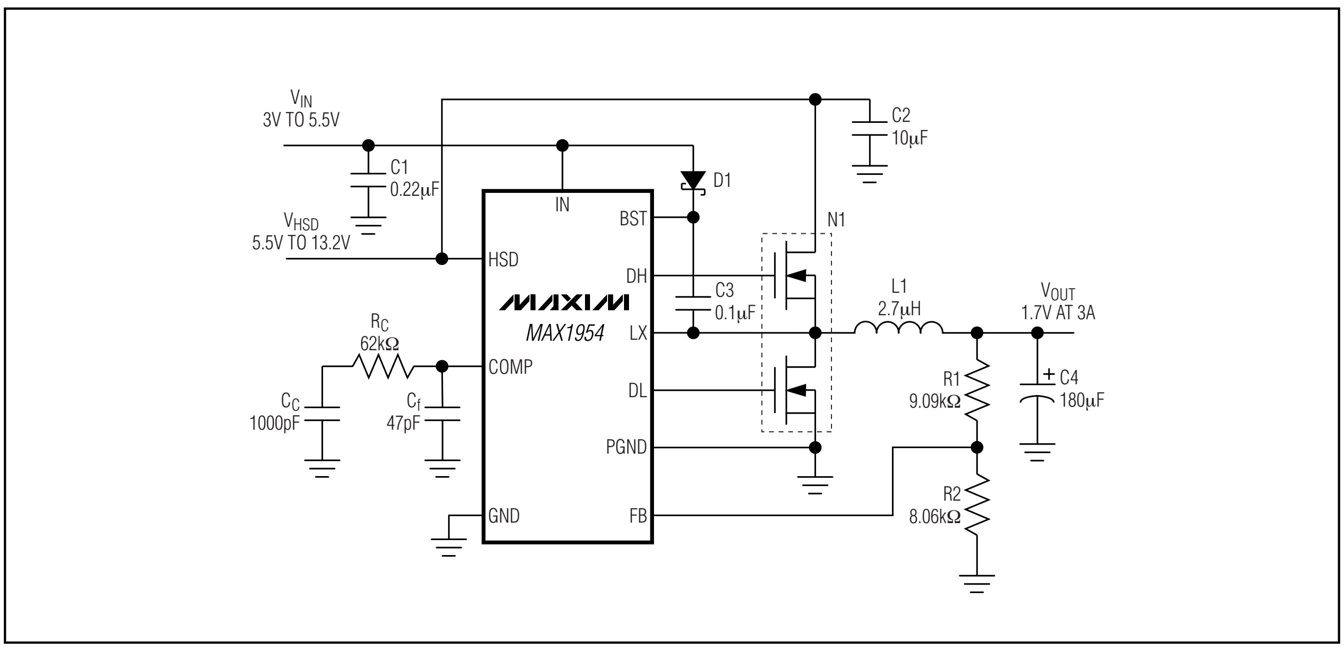


Figure 2. Typical Application Circuit for the MAX1954

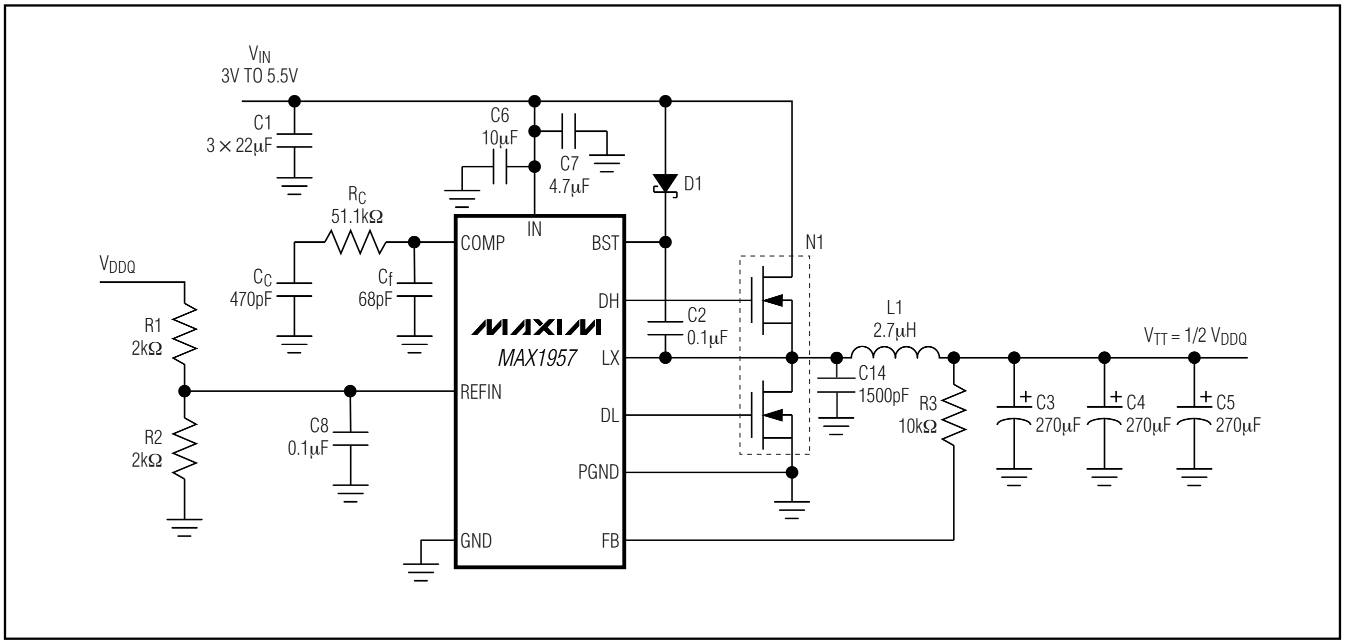


Figure 3. Typical Application Circuit for the MAX1957

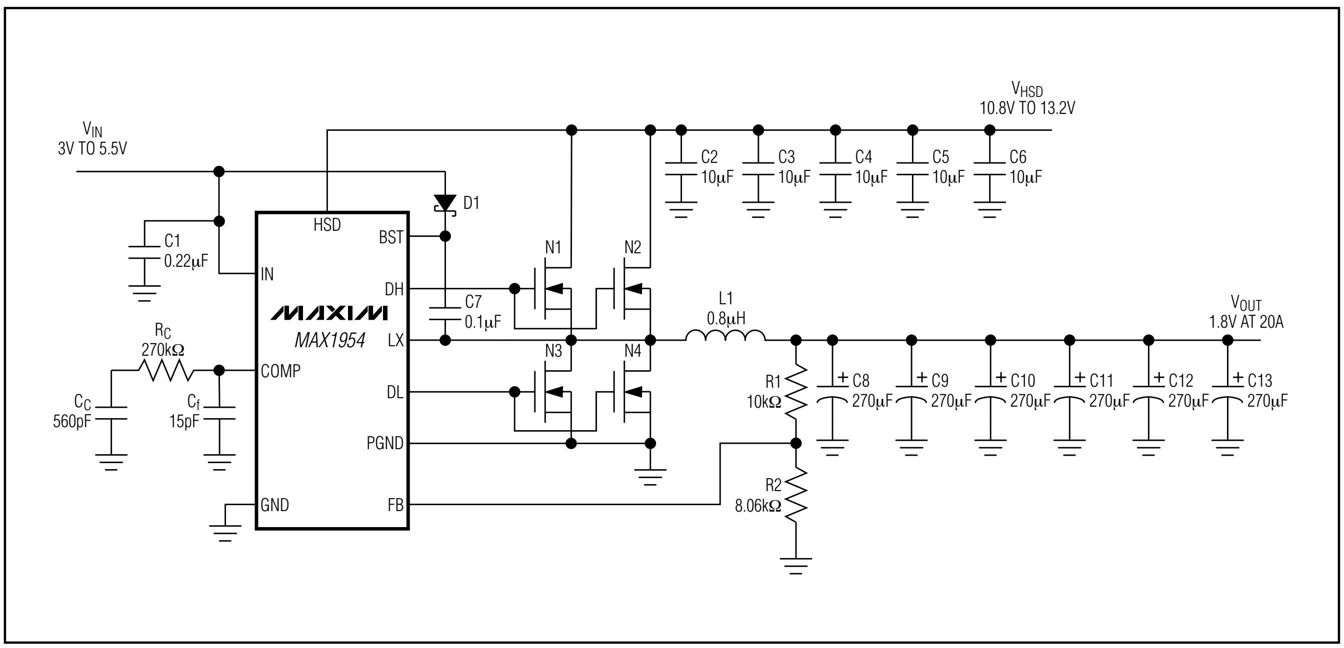


Figure 4. 20A Circuit

Low-Cost, High-Frequency, Current-Mode PWM Buck Controller

Current-Sense Amplifier

The MAX1953/MAX1954/MAX1957s' current-sense circuit amplifies (A_V = 3.5 typ) the current-sense voltage (the high-side MOSFET's on-resistance ($R_{DS(ON)}$) multiplied by the inductor current). This amplified current-sense signal and the internal-slope compensation signal are summed (V_{SUM}) together and fed into the PWM comparator's inverting input. The PWM comparator shuts off the high-side MOSFET when V_{SUM} exceeds the integrated feedback voltage (V_{COMP}).

Current-Limit Circuit

The current-limit circuit employs a lossless current-limiting algorithm that uses the low-side and high-side MOSFETs' on-resistances as the sensing elements. The voltage across the high-side MOSFET is monitored for current-mode feedback, as well as current limit. This signal is amplified by the current-sense amplifier and is compared with a current-sense voltage. If the current-sense signal is larger than the set current-limit voltage, the high-side MOSFET turns off. Once the high-side MOSFET turns off, the low-side MOSFET is monitored for current limit. If the voltage across the low-side MOSFET ($R_{DS(ON)} \times I_{INDUCTOR}$) does not exceed the short-circuit current limit, the high-side MOSFET turns on normally. In this condition, the output drops smoothly out of regulation. If the voltage across the low-side MOSFET exceeds the short-circuit current-limit threshold at the beginning of each new oscillator cycle, the MAX1953/MAX1954/MAX1957 do not turn on the high-side MOSFET.

In the case where the output is shorted, the low-side MOSFET is monitored for current limit. The low-side MOSFET is held on to let the current in the inductor ramp down. Once the voltage across the low-side MOSFET drops below the short-circuit current-limit threshold, the high-side MOSFET is pulsed. Under this condition, the frequency of the MAX1953/MAX1954/MAX1957 appears to decrease because the on-time of the low-side MOSFET extends beyond a clock cycle.

The actual peak output current is greater than the short-circuit current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the low-side MOSFET on-resistance, inductor value, input voltage, and output voltage.

The short-circuit current-limit threshold is preset for the MAX1954/MAX1957 at 210mV. The MAX1953, however, has three options for the current-limit threshold: connect ILIM to IN for a 320mV threshold, connect ILIM to GND for 105mV, or leave floating for 210mV.

Synchronous Rectifier Driver (DL)

Synchronous rectification reduces conduction losses in the rectifier by replacing the normal Schottky catch diode with a low-resistance MOSFET switch. The MAX1953/MAX1954/MAX1957 use the synchronous rectifier to ensure proper startup of the boost gate-driver circuit and to provide the current-limit signal. The DL low-side waveform is always the complement of the DH high-side drive waveform. A dead-time circuit monitors the DL output and prevents the high-side MOSFET from turning on until DL is fully off, thus preventing cross-conduction or shoot-through. In order for the dead-time circuit to work properly, there must be a low-resistance, low-inductance path from the DL driver to the MOSFET gate. Otherwise, the sense circuitry in the MAX1953/MAX1954/MAX1957 can interpret the MOSFET gate as OFF when gate charge actually remains. The dead time at the other edge (DH turning off) is determined through gate sensing as well.

High-Side Gate-Drive Supply (BST)

Gate-drive voltage for the high-side switch is generated by a flying capacitor boost circuit (Figure 5). The capacitor between BST and LX is charged from the V_{IN} supply up to V_{IN}, minus the diode drop while the low-side MOSFET is on. When the low-side MOSFET is switched off, the stored voltage of the capacitor is stacked above LX to provide the necessary turn-on voltage (V_{GS}) for the high-side MOSFET. The controller then closes an internal switch between BST and DH to turn the high-side MOSFET on.

Undervoltage Lockout

If the supply voltage at IN drops below 2.75V, the MAX1953/MAX1954/MAX1957 assume that the supply voltage is too low to make valid decisions, so the UVLO circuitry inhibits switching and forces the DL and DH gate drivers low. After the voltage at IN rises above 2.8V, the controller goes into the startup sequence and resumes normal operation.

Startup

The MAX1953/MAX1954/MAX1957 start switching when the voltage at IN rises above the UVLO threshold. However, the controller is not enabled unless all four of the following conditions are met:

- V_{IN} exceeds the 2.8V UVLO threshold.
- The internal reference voltage exceeds 92% of its nominal value (V_{REF} > 1 V).
- The internal bias circuitry powers up.
- The thermal overload limit is not exceeded.

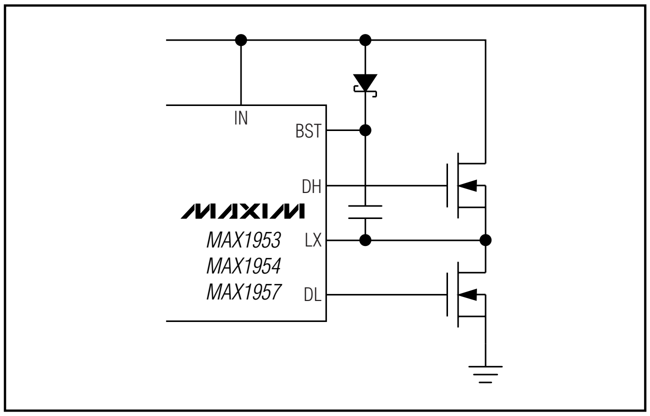


Figure 5. DH Boost Circuit

Once these conditions are met, the step-down controller enables soft-start and starts switching. The soft-start circuitry gradually ramps up to the feedback-regulation voltage in order to control the rate-of-rise of the output voltage and reduce input surge currents during startup. The soft-start period is 1024 clock cycles ($1024/f_S$, MAX1954/MAX1957) or 4096 clock cycles ($4096/f_S$, MAX1953) and the internal soft-start DAC ramps the voltage up in 64 steps. The output reaches regulation when soft-start is completed, regardless of output capacitance and load.

Shutdown

The MAX1953/MAX1954/MAX1957 feature a low-power shutdown mode. Use an open-collector transistor to pull COMP low to shut down the IC. During shutdown, the output is high impedance. Shutdown reduces the quiescent current (I_Q) to approximately 220µA.

Thermal Overload Protection

Thermal overload protection limits total power dissipation in the MAX1953/MAX1954/MAX1957. When the junction temperature exceeds T_J = +160°C, an internal thermal sensor shuts down the device, allowing the IC to cool. The thermal sensor turns the IC on again after the junction temperature cools by 15°C, resulting in a pulsed output during continuous thermal overload conditions.

Design Procedures

Setting the Output Voltage

To set the output voltage for the MAX1953/MAX1954, connect FB to the center of an external resistor-divider connected between the output to GND (Figures 1 and 2). Select R2 between 8kΩ and 24kΩ, and then calculate R1 by:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right)$$

where V_{FB} = 0.8V. R1 and R2 should be placed as close to the IC as possible.

For the MAX1957, connect FB directly to the output through a decoupling resistor of 10kΩ to 21kΩ (Figure 3). The output voltage is then equal to the voltage at REFIN. Again, this resistor should be placed as close to the IC as possible.

Determining the Inductor Value

There are several parameters that must be examined when determining which inductor is to be used. Input voltage, output voltage, load current, switching frequency, and LIR. LIR is the ratio of inductor current ripple to DC load current. A higher LIR value allows for a smaller inductor, but results in higher losses and higher output ripple. A good compromise between size, efficiency, and cost is an LIR of 30%. Once all of the parameters are chosen, the inductor value is determined as follows:

$$L = \frac{V_{OUT} \times \left(V_{IN} - V_{OUT}\right)}{V_{IN} \times f_S \times I_{LOAD(MAX)} \times LIR}$$

where f_S is the switching frequency. Choose a standard value close to the calculated value. The exact inductor value is not critical and can be adjusted in order to make trade-offs among size, cost, and efficiency. Lower inductor values minimize size and cost, but they also increase the output ripple and reduce the efficiency due to higher peak currents. By contrast, higher inductor values increase efficiency, but eventually resistive losses due to extra turns of wire exceed the benefit gained from lower AC current levels.

For any area-restricted applications, find a low-core loss inductor having the lowest possible DC resistance. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 300kHz.

Low-Cost, High-Frequency, Current-Mode PWM Buck Controller

The chosen inductor's saturation current rating must exceed the expected peak inductor current (IPEAK). Determine IPEAK as:

$$I_{PEAK} = I_{LOAD(MAX)} + \left(\frac{LIR}{2}\right) \times I_{LOAD(MAX)}$$

Setting the Current Limit

The MAX1953/MAX1954/MAX1957 use a lossless current-sense method for current limiting. The voltage drops across the MOSFETs created by their on-resistances are used to sense the inductor current. Calculate the current-limit threshold as follows:

$$V_{CS} = \frac{0.8V}{A_{CS}}$$

where A_{CS} is the gain of the current-sense amplifier. A_{CS} is 6.3 for the MAX1953 when ILIM is connected to GND and 3.5 for the MAX1954/MAX1957, and for the MAX1953 when ILIM is connected to IN or floating. The 0.8V is the usable dynamic range of COMP (V_{COMP}).

Initially, the high-side MOSFET is monitored. Once the voltage drop across the high-side MOSFET exceeds V_{CS}, the high-side MOSFET is turned off and the low-side MOSFET is turned on. The voltage across the low-side MOSFET is then monitored. If the voltage across the low-side MOSFET exceeds the short-circuit current limit, a short-circuit condition is determined and the low-side MOSFET is held on. Once the monitored voltage falls below the short-circuit current-limit threshold, the MAX1953/MAX1954/MAX1957 switch normally. The short-circuit current-limit threshold is fixed at 210mV for the MAX1954/ MAX1957 and is selectable for the MAX1953.

When selecting the high-side MOSFET, use the following method to verify that the MOSFET's $R_{DS(ON)}$ is sufficiently low at the operating junction temperature (T_J):

$$R_{DS(ON)N1} \le \frac{0.8V}{A_{CS} \times I_{PEAK}}$$

The voltage drop across the low-side MOSFET at the valley point and at $I_{LOAD(MAX)}$ is:

$$V_{VALLEY} = R_{DS(ON)} \times \left(I_{LOAD(MAX)} - \left(\frac{LIR}{2}\right) \times I_{LOAD(MAX)}\right)$$

where $R_{DS(ON)}$ is the maximum value at the desired maximum operating junction temperature of the MOSFET. A good general rule is to allow 0.5% additional resistance for each °C of MOSFET junction temperature rise. The calculated V_{VALLEY} must be less than V_{CS}. For the MAX1953, connect ILIM to GND for a short-circuit current-limit voltage of 105mV, to V_{IN} for 320mV or leave ILIM floating for 210mV.

MOSFET Selection

The MAX1953/MAX1954/MAX1957 drive two external, logic-level, N-channel MOSFETs as the circuit switch elements. The key selection parameters are:

- **On-Resistance ($R_{DS(ON)}$):** The lower, the better.
- **Maximum Drain-to-Source Voltage (V_{DSS}):** Should be at least 20% higher than the input supply rail at the high side MOSFET's drain.
- **Gate Charges (Q_g, Q_{gd}, Q_{gs}):** The lower, the better.

For a 3.3V input application, choose a MOSFET with a rated $R_{DS(ON)}$ at V_{GS} = 2.5V. For a 5V input application, choose the MOSFETs with rated $R_{DS(ON)}$ at $V_{GS} \le$ 4.5V. For a good compromise between efficiency and cost, choose the high-side MOSFET (N1) that has conduction losses equal to switching loss at the nominal input voltage and output current. The selected low-side and high-side MOSFETs (N2 and N1, respectively) must have $R_{DS(ON)}$ that satisfies the current-limit setting condition above. For N2, make sure that it does not spuriously turn on due to dV/dt caused by N1 turning on, as this would result in shoot-through current degrading the efficiency. MOSFETs with a lower Q_{gd}/Q_{gs} ratio have higher immunity to dV/dt.

For proper thermal management design, the power dissipation must be calculated at the desired maximum operating junction temperature, $T_{J(MAX)}$. N1 and N2 have different loss components due to the circuit operation. N2 operates as a zero-voltage switch; therefore, major losses are the channel conduction loss (P_{N2CC}) and the body diode conduction loss (P_{N2DC}):

USE $R_{DS(ON)}$ AT $T_{J(MAX)}$

$$P_{N2CC} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times I^2_{LOAD} \times R_{DS(ON)}$$

$$P_{N2DC} = 2 \times I_{LOAD} \times V_F \times t_{DT} \times f_S$$

where V_F is the body diode forward-voltage drop, t_{dt} is the dead time between N1 and N2 switching transitions, and f_S is the switching frequency.

N1 operates as a duty-cycle control switch and has the following major losses: the channel conduction loss (P_{N1CC}), the voltage and current overlapping switching loss (P_{N1SW}), and the drive loss (P_{N1DR}).

$$P_{N1CC} = \left(\frac{V_{OUT}}{V_{IN}}\right) \times I^2_{LOAD} \times R_{DS(ON)} \left(\text{USE } R_{DS(ON)} \text{ AT } T_{J(MAX)}\right)$$

$$P_{N2SW} = V_{IN} \times I_{LOAD} \times \left(\frac{Q_{GS} + Q_{GD}}{I_{GATE}}\right) \times f_S$$

where I_{GATE} is the average DH driver output current capability determined by:

$$I_{GATE} \cong \frac{1}{2} \times \frac{V_{IN}}{R_{DH} + R_{GATE}}$$

where R_{DH} is the high-side MOSFET driver's on-resistance (3Ω max) and R_{GATE} is the internal gate resistance of the MOSFET (~ 2Ω):

$$P_{N1DR} = Q_G \times V_{GS} \times f_S \times \frac{R_{GATE}}{R_{GATE} + R_{DH}}$$

where V_{GS} ~ V_{IN}. In addition to the losses above, allow about 20% more for additional losses due to MOSFET output capacitances and N2 body diode reverse recovery charge dissipated in N1 that exists, but is not well defined in the MOSFET data sheet. Refer to the MOSFET data sheet for the thermal-resistance specification to calculate the PC board area needed to maintain the desired maximum operating junction temperature with the above calculated power dissipations.

The minimum load current must exceed the high-side MOSFET's maximum leakage current over temperature if fault conditions are expected.

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents defined by the following equation:

$$I_{RMS} = \frac{I_{LOAD} \times \sqrt{V_{OUT} \times \left(V_{IN} - V_{OUT}\right)}}{V_{IN}}$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage (V_{IN} = 2 x V_{OUT}), where $I_{RMS(MAX)}$ = I_{LOAD}/2. Ceramic capacitors are recommended due to their low ESR and ESL at high frequency, with relatively low cost. Choose a capacitor that exhibits less than 10°C temperature rise at the maximum operating RMS current for optimum long-term reliability.

Output Capacitor

The key selection parameters for the output capacitor are the actual capacitance value, the equivalent series resistance (ESR), the equivalent series inductance (ESL), and the voltage-rating requirements. These parameters affect the overall stability, output voltage ripple, and transient response. The output ripple has three components: variations in the charge stored in the output capacitor, the voltage drop across the capacitor's ESR, and the voltage drop across the ESL caused by the current into and out of the capacitor:

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)} + V_{RIPPLE(ESL)}$$

The output voltage ripple as a consequence of the ESR, ESL, and output capacitance is:

$$V_{RIPPLE(ESR)} = I_{P-P} \times ESR$$

$$V_{RIPPLE(C)} \frac{I_{P-P}}{8 \times C_{OUT} \times f_S}$$

$$V_{RIPPLE(ESL)} = \left(\frac{V_{IN}}{L}\right) ESL$$

$$I_{P-P} = \left(\frac{V_{IN} - V_{OUT}}{f_S \times L}\right) \times \left(\frac{V_{OUT}}{V_{IN}}\right)$$

where I_{P-P} is the peak-to-peak inductor current (see the *Determining the Inductor Value* section). These equations are suitable for initial capacitor selection, but final values should be chosen based on a prototype or evaluation circuit.

As a general rule, a smaller current ripple results in less output voltage ripple. Since the inductor ripple current is a factor of the inductor value and input voltage, the output voltage ripple decreases with larger inductance, and increases with higher input voltages. Ceramic capacitors are recommended for the MAX1953 due to its 1MHz switching frequency. For the MAX1954/MAX1957, using polymer, tantalum, or aluminum electrolytic capacitors is recommended. The aluminum electrolytic capacitor is the least expensive; however, it has higher ESR. To compensate for this, use a ceramic capacitor in parallel to reduce the switching ripple and noise. For reliable and safe operation, ensure that the capacitor's voltage and ripple-current ratings exceed the calculated values.

The MAX1953/MAX1954/MAX1957s' response to a load transient depends on the selected output capacitors. In general, more low-ESR output capacitance results in better transient response. After a load transient, the output voltage instantly changes by ESR × ΔI_{LOAD}. Before the controller can respond, the output voltage deviates further, depending on the inductor and output capacitor values. After a short period of time (see the *Typical Operating Characteristics*), the controller responds by regulating the output voltage back to its nominal state. The controller response time depends on its closed-loop bandwidth. With a higher bandwidth, the response time is faster, preventing the output voltage from further deviation from its regulating value.

Compensation Design

The MAX1953/MAX1954/MAX1957 use an internal transconductance error amplifier whose output compensates the control loop. The external inductor, high-side MOSFET, output capacitor, compensation resistor, and compensation capacitors determine the loop stability. The inductor and output capacitors are chosen based on performance, size, and cost. Additionally, the compensation resistor and capacitors are selected to optimize control-loop stability. The component values shown in the *Typical Application Circuits* (Figures 1 through 4) yield stable operation over the given range of input-to-output voltages and load currents.

The controller uses a current-mode control scheme that regulates the output voltage by forcing the required current through the external inductor. The MAX1953/MAX1954/MAX1957 use the voltage across the high-side MOSFET's on-resistance ($R_{DS(ON)}$) to sense the inductor current. Current-mode control eliminates the double pole in the feedback loop caused by the inductor and output capacitor, resulting in a smaller phase shift and requiring less elaborate error-amplifier compensation. A simple single-series R_C and C_C is all that is needed to have a stable high bandwidth loop in applications where ceramic capacitors are used for output filtering. For other types of capacitors, due to the higher capacitance and ESR, the frequency of the zero created by the capacitance and ESR is lower than the desired close loop crossover frequency. Another compensation capacitor should be added to cancel this ESR zero.

The basic regulator loop may be thought of as a power modulator, output feedback divider, and an error amplifier. The power modulator has DC gain set by g_{mc} x R_{LOAD}, with a pole and zero pair set by R_{LOAD}, the output capacitor (C_{OUT}), and its equivalent series resistance (R_{ESR}).

Below are equations that define the power modulator:

$$G_{MOD} = g_{mc} \times \frac{R_{LOAD} \times (f_S \times L)}{R_{LOAD} + \left(f_S \times L\right)}$$

where $R_{LOAD} = V_{OUT}/I_{OUT(MAX)}$, and $g_{mc} = 1/(A_{CS} \times R_{DS(ON)})$, where A_{CS} is the gain of the current-sense amplifier and $R_{DS(ON)}$ is the on-resistance of the high-side power MOSFET. A_{CS} is 6.3 for the MAX1953 when ILIM is connected to GND, and 3.5 for the MAX1954/MAX1957 and for the MAX1953 when ILIM is connected to V_{IN} or floating. The frequencies at which the pole and zero due to the power modulator occur are determined as follows:

$$f_{pMOD} = \frac{1}{2\pi \times C_{OUT} \times \left(\frac{R_{LOAD} \times \left(f_S \times L\right) + R_{ESR}}{R_{LOAD} + \left(f_S \times L\right)}\right)}$$

$$f_{zMOD} = \frac{1}{2\pi \times C_{OUT} \times R_{ESR}}$$

The feedback voltage-divider used has a gain of $G_{FB} = V_{FB}/V_{OUT}$, where V_{FB} is equal to 0.8V. The transconductance error amplifier has DC gain, $G_{EA(DC)} = gm \times R_O$. R_O is typically 10MΩ. A dominant pole is set by the compensation capacitor (C_C), the amplifier output resistance (R_O), and the compensation resistor (R_C). A zero is set by the compensation resistor (R_C) and the compensation capacitor (C_C).

There is an optional pole set by C_f and R_C to cancel the output capacitor ESR zero if it occurs before crossover frequency (f_C):

$$f_{pdEA} = \frac{1}{2\pi \times C_C \times (R_O + R_C)}$$

$$fzEA = \frac{1}{2\pi \times C_C \times R_C}$$

$$fpEA = \frac{1}{2\pi \times C_f \times R_C}$$

The crossover frequency (f_C) should be much higher than the power modulator pole f_{pMOD}. Also, the crossover frequency should be less than 1/5 the switching frequency:

$$f_{pMOD} << f_C < \frac{f_S}{5}$$

Table 2. Suggested Manufacturers

MANUFACTURER	COMPONENT	PHONE	WEBSITE
Central Semiconductor	Diode	631-435-1110	www.centralsemi.com
Coilcraft	Inductors	800-322-2645	www.coilcraft.com
Fairchild	MOSFETs	800-341-0392	www.fairchildsemi.com
Kemet	Capacitors	864-963-6300	www.kemet.com
Panasonic	Capacitors	714-373-7366	www.panasonic.com
Taiyo Yuden	Capacitors	408-573-4150	www.t-yuden.com
Toko	Inductors	800-745-8656	www.toko.com

so the loop-gain equation at the crossover frequency is:

$$G_{EA(f_C)} \times G_{MOD(f_C)} \times \frac{V_{FB}}{V_{OUT}} = 1$$

For the case where f_{ZESR} is greater than f_C:

$$G_{EA(f_C)} = g_{mEA} \times R_C$$

and

$$G_{MOD(f_C)} = g_{mc} \times \frac{R_{LOAD} \times (f_S \times L)}{R_{LOAD} + (f_S \times L)} \times \frac{f_{pMOD}}{f_C}$$

then R_C is calculated as:

$$R_C = \frac{V_{OUT}}{g_{mEA} \times V_{FB} \times G_{MOD(f_C)}}$$

where g_{mEA} = 110µS.

The error amplifier compensation zero formed by R_C and C_C should be set at the modulator pole f_{pMOD}. C_C is calculated by:

$$C_C = \frac{\frac{V_{OUT}}{I_{OUT(MAX)}} \times (f_S \times L)}{\frac{V_{OUT}}{I_{OUT(MAX)}} + (f_S \times L)} \times \frac{C_{OUT}}{R_C}$$

As the load current decreases, the modulator pole also decreases. However, the modulator gain increases accordingly, and the crossover frequency remains the same. For the case where f_{ZESR} is less than f_C, add another compensation capacitor C_f from COMP to GND to cancel the ESR zero at f_{ZESR}. C_f is calculated by:

$$C_f = \frac{1}{2\pi \times R_C \times f_{ZESR}}$$

Figure 6 illustrates a numerical example that calculates R_C and C_C values for the typical application circuit of Figure 1 (MAX1953).

Applications Information

See Table 2 for suggested manufacturers of the components used with the MAX1953/MAX1954/MAX1957.

PC Board Layout Guidelines

Careful PC board layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention. Follow these guidelines for good PC board layout:

1) Place decoupling capacitors as close to IC pins as possible. Keep separate power ground plane (connected to pin 7) and signal ground plane (connected to pin 4).
2) Input and output capacitors are connected to the power ground plane; all other capacitors are connected to the signal ground plane.
3) Keep the high current paths as short as possible.
4) Connect the drain leads of the power MOSFET to a large copper area to help cool the device. Refer to the power MOSFET data sheet for recommended copper area.
5) Ensure all feedback connections are short and direct. Place the feedback resistors as close to the IC as possible.
6) Route high-speed switching nodes away from sensitive analog areas (FB, COMP).
7) Place the high-side MOSFET as close as possible to the controller and connect IN (MAX1953/MAX1957) or HSD (MAX1954) and LX to the MOSFET.
8) Use very short, wide traces (50mils to 100mils wide if the MOSFET is 1in from the device).

Chip Information

TRANSISTOR COUNT: 2930

PROCESS: BiCMOS

$V_{OUT} = 2.5V$

$I_{OUT(MAX)} = 3A$

$C_{OUT} = 20\mu F$

$L = 1\mu H$

$R_{ESR} = 0.0025\Omega$

$g_{mEA} = 110\mu S$

$A_{VCS} = 6.3A$

$R_{DS(ON)} = 0.013\Omega$

$$g_{mc} = \frac{1}{A_{VCS} \times R_{DS(ON)}} = 12.21S$$

$f_S = 1MHz$

$$R_{LOAD} = \frac{V_{OUT}}{I_{OUT(MAX)}} = \frac{2.5V}{3A} = 0.833\Omega$$

$$f_{pMOD} = \frac{1}{2\pi \times C_{OUT} \times \left(\frac{R_{LOAD} \times (f_S \times L)}{R_{LOAD}(f_S \times L)} + R_{ESR}\right)} = \frac{1}{2\pi \times 20\mu F \times \left(\frac{0.833\Omega \times 1MHz \times 1\mu H}{0.833\Omega + (1MHz \times 1\mu H)} + 0.0025\Omega\right)} = 17.42kHz$$

$$f_{zESR} = \frac{1}{2\pi \times C_{OUT} \times R_{ESR}} = \frac{1}{2\pi \times 20\mu F \times .0025\Omega} = 3.2MHz$$

Pick the crossover frequency (f_C) at < 1/5 the switching frequency (f_S). We choose 100kHz < f_{zESR}, so C_F is not needed. The power modulator gain at f_C is:

$$G_{MOD(f_C)} = g_{mc} \times \frac{R_{LOAD} \times (f_S \times L)}{R_{LOAD}(f_S \times L)} \times \frac{f_{pMOD}}{f_C} = 12.21S \times \frac{0.833\Omega \times (1MHz \times 1\mu H)}{0.833\Omega + (1MHz \times 1\mu H)} \times \frac{17.42kHz}{100kHz} = 0.967$$

then:

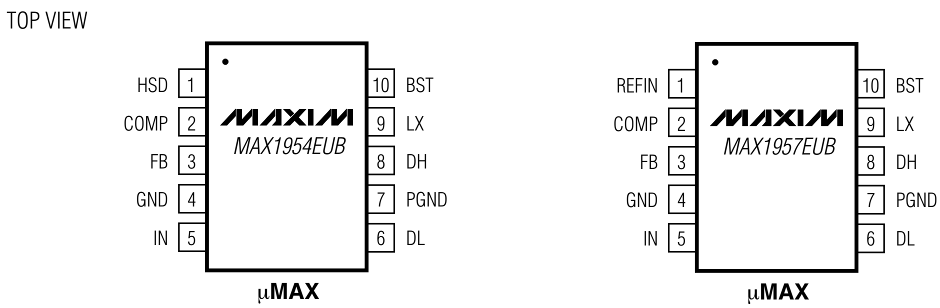
$$R_C = \frac{V_{OUT}}{g_{mEA} \times V_{FB} \times G_{MOD(f_C)}} = \frac{2.5V}{110\mu S \times 0.8V \times .937} \approx 33k\Omega$$

And:

$$C_C = \frac{\frac{V_{OUT}}{I_{OUT(MAX)}} \times (f_S \times L)}{\frac{V_{OUT}}{I_{OUT(MAX)}} + (f_S \times L)} \times \frac{C_{OUT}}{R_C} = \frac{\frac{2.5V}{3A} \times (1MHz \times 1\mu H)}{\frac{2.5V}{3A} + (1MHz \times 1\mu H)} \times \frac{20\mu F}{33k\Omega} \approx 270pF$$

Figure 6. Numerical Example to Calculate R_C and C_C Values of the Typical Operating Circuit of Figure 1 (MAX1953)

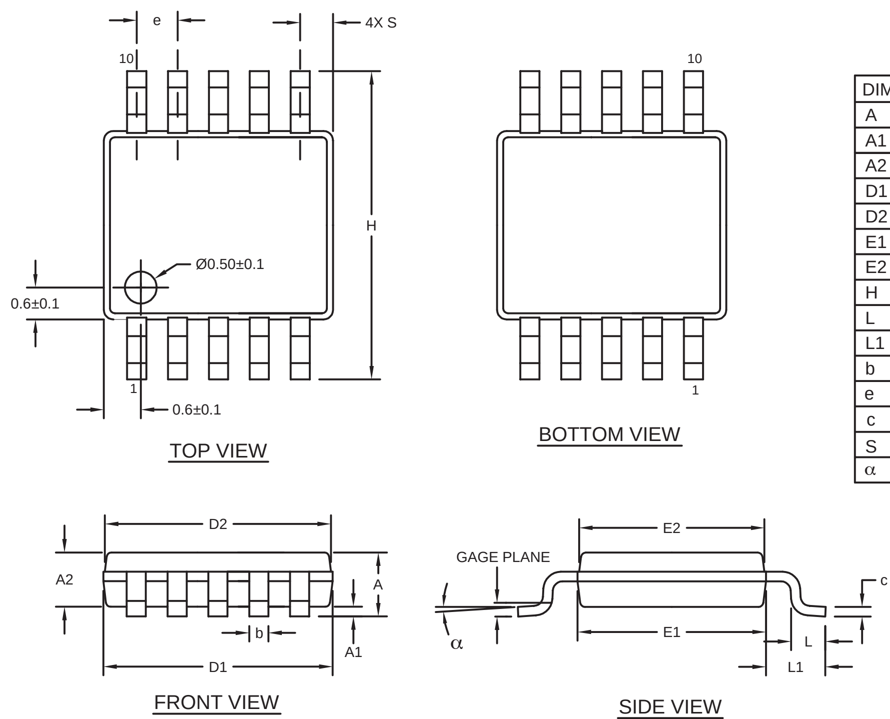
Pin Configurations (continued)



Low-Cost, High-Frequency, Current-Mode PWM Buck Controller

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



10LUMAX.EPS

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0°	6°	0°	6°

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-BA.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, 10L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0061	I	1/1