MAX19777

3Msps, Low-Power, Serial 12-Bit ADC

General Description

The MAX19777 is a 12-bit, compact, high-speed, lowpower, successive approximation analog-to-digital converter (ADC). This high-performance ADC includes a high dynamic range sample-and-hold, as well as a high-speed serial interface.

The MAX19777 features dual, single-ended analog inputs connected to the ADC core using a 2:1 MUX.

This ADC operates from a 2.2V to 3.3V supply and consumes only 6.2mW at 3Msps. The device includes a full power-down mode and fast wake up for optimal power management and a high-speed 3-wire serial interface. The 3-wire serial interface directly connects to SPI, QSPI™, and MICROWIRE® devices without external logic.

Excellent dynamic performance, low voltage, low power, ease-of-use, and small package size make this converter ideal for portable, battery-powered data-acquisition applications, as well as for other applications that demand low power consumption and minimal space.

This ADC is available in an 8-pin wafer-level package (WLP). This device operates over the -40°C to +125°C temperature range.

Benefits and Features

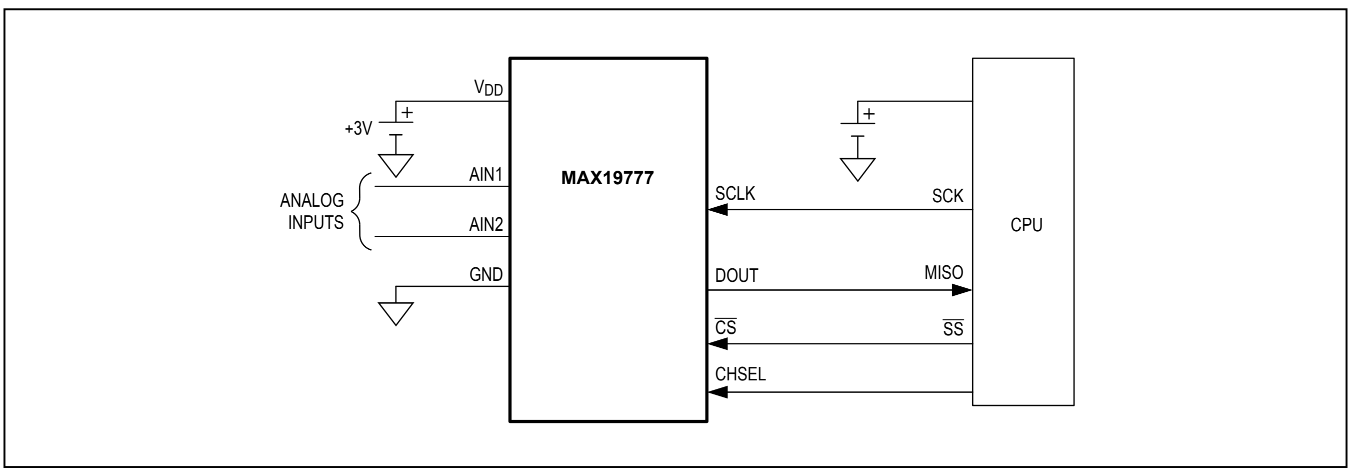
- 3Msps Conversion Rate, No Pipeline Delay
- 12-Bit Resolution
- 2-Channel, Single-Ended Analog Inputs
- Low-Noise 72.5dB SNR
- 2.2V to 3.3V Supply Voltage
- Low Power
  - 6.2mW at 3Msps
  - Very Low Power Consumption at 2.5μA/ksps
- 2μA Power-Down Current
- SPI/QSPI/MICROWIRE-Compatible Serial Interface
- 8-Pin, 0.857mm x 1.431mm WLP Package
- Wide -40°C to +125°C Operation

Applications

- Data Acquisition
- Portable Data Logging
- Medical Instrumentation
- Battery-Operated Systems
- Communication Systems
- Automotive Systems

***Ordering Information* continued at end of data sheet.**

Typical Operating Circuit



Absolute Maximum Ratings

V_{DD} to GND ....-0.3V to +3.6V
AIN1, AIN2, $\overline{CS}$, SCLK, CHSEL, DOUT TO GND
.........................-0.3V to the lower of (V_{DD} + 0.3V) and +3.6V
Input/Output Current (all pins)...50mA
Continuous Power Dissipation (T_A = +70°C)
8-pin WLP (derate 11.6mW/°C above +70°C)............872mW

Operating Temperature Range........................ -40°C to +125°C
Junction Temperature..+150°C
Storage Temperature Range........................... -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow)......................................+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{DD} = 2.2V to 3.3V. f_{SCLK} = 48MHz, 50% duty cycle, 3Msps. C_{DOUT} = 10pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			12			Bits
Integral Nonlinearity	INL	2Msps, V_{DD} MAX	-1.5		+1.5	LSB
		2Msps, V_{DD} MIN	-2		+2	
		3Msps		±3		
Differential Nonlinearity	DNL	2Msps, V_{DD} MAX	-1		+1.2	LSB
		1Msps, V_{DD} MAX	-0.95		+1.2	
Offset Error	OE	V_{DD} MAX	-4		+10	LSB
Gain Error	GE	V_{DD} MAX	-7		+7	LSB
Total Unadjusted Error	TUE			4		LSB
Channel-to-Channel Offset Matching				±0.4		LSB
Channel-to-Channel Gain Matching				±0.05		LSB
DYNAMIC PERFORMANCE ($f_{AIN\_}$ = 10kHz)						
Signal-to-Noise and Distortion	SINAD	2Msps	70	72		dB
		3Msps		69		
Signal-to-Noise Ratio	SNR	2Msps	71	72.5		dB
		3Msps		69		
Total Harmonic Distortion	THD			-83		dB
Spurious-Free Dynamic Range	SFDR			83		dB
Intermodulation Distortion	IMD	f_1 = 1.0003MHz, f_2 = 0.99955MHz		-84		dB
Full-Power Bandwidth		-3dB point		40		MHz
Full-Linear Bandwidth		SINAD > 68dB		2.5		MHz
Small-Signal Bandwidth				45		MHz

Electrical Characteristics (continued)

(V_{DD} = 2.2V to 3.3V. f_{SCLK} = 48MHz, 50% duty cycle, 3Msps. C_{DOUT} = 10pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Crosstalk				-90		dB
CONVERSION RATE						
Throughput			0.03		3	Msps
Conversion Time			260			ns
Acquisition Time	t_{ACQ}		52			ns
Aperture Delay		From $\overline{CS}$ falling edge		4		ns
Aperture Jitter				15		ps
Serial-Clock Frequency	f_{CLK}		0.48		48	MHz
ANALOG INPUT (AIN1, AIN2)						
Input Voltage Range	$V_{AIN\_}$		0		V_{DD}	V
Input Leakage Current	I_{ILA}			0.002	±1	µA
Input Capacitance	$C_{AIN\_}$	Track		20		pF
		Hold		4		
DIGITAL INPUTS (SCLK, $\overline{CS}$, CHSEL)						
Digital Input High Voltage	V_{IH}		0.75 x V_{DD}			V
Digital Input Low Voltage	V_{IL}				0.25 x V_{DD}	V
Digital Input Hysteresis	V_{HYST}			0.15 x V_{DD}		V
Digital Input Leakage Current	I_{IL}	Inputs at GND or V_{DD}		0.001	±1	µA
Digital Input Capacitance	C_{IN}			2		pF
DIGITAL OUTPUT (DOUT)						
Output High Voltage	V_{OH}	I_{SOURCE} = 200µA	0.85 x V_{DD}			V
Output Low Voltage	V_{OL}	I_{SINK} = 200µA			0.15 x V_{DD}	V
High-Impedance Leakage Current	I_{OL}				±1.0	µA
High-Impedance Output Capacitance	C_{OUT}			4		pF

Electrical Characteristics (continued)

(V_{DD} = 2.2V to 3.3V. f_{SCLK} = 48MHz, 50% duty cycle, 3Msps. C_{DOUT} = 10pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Positive Supply Voltage	V_{DD}		2.2		3.3	V
Positive Supply Current (Full-Power Mode)	I_{VDD}	Full-Power Mode, 2Msps		2.8	3.6	mA
Positive Supply Current (Full-Power Mode), No Clock	I_{VDD}	Full-Power Mode, No Clock		2.0	2.8	mA
Power-Down Current	I_{PD}	Leakage only		1.3	10	µA
Line Rejection		V_{DD} = +2.2V to +3.3V		0.7		LSB/V
TIMING CHARACTERISTICS (Note 1)						
Quiet Time	t_Q	(Note 2)	4			ns
$\overline{CS}$ Pulse Width	t_1	(Note 2)	10			ns
$\overline{CS}$ Fall to SCLK Setup	t_2	(Note 2)	5			ns
$\overline{CS}$ Falling Until DOUT High-Impedance Disabled	t_3	(Note 2)	1			ns
Data Access Time After SCLK Falling Edge	t_4	Figure 2			23	ns
SCLK Pulse Width Low	t_5	Percentage of clock period (Note 2)	40		60	%
SCLK Pulse Width High	t_6	Percentage of clock period (Note 2)	40		60	%
Data Hold Time From SCLK Falling Edge	t_7	Figure 3	5			ns
SCLK Falling Until DOUT High-Impedance	t_8	Figure 4 (Note 2)	2.5		14	ns
Power-Up Time		Conversion cycle (Note 2)			1	Cycle

Note 1: All timing specifications given are with a 10pF capacitor.
Note 2: Guaranteed by design in characterization; not production tested.
Note 3: Limits are 100% tested at T_A=25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

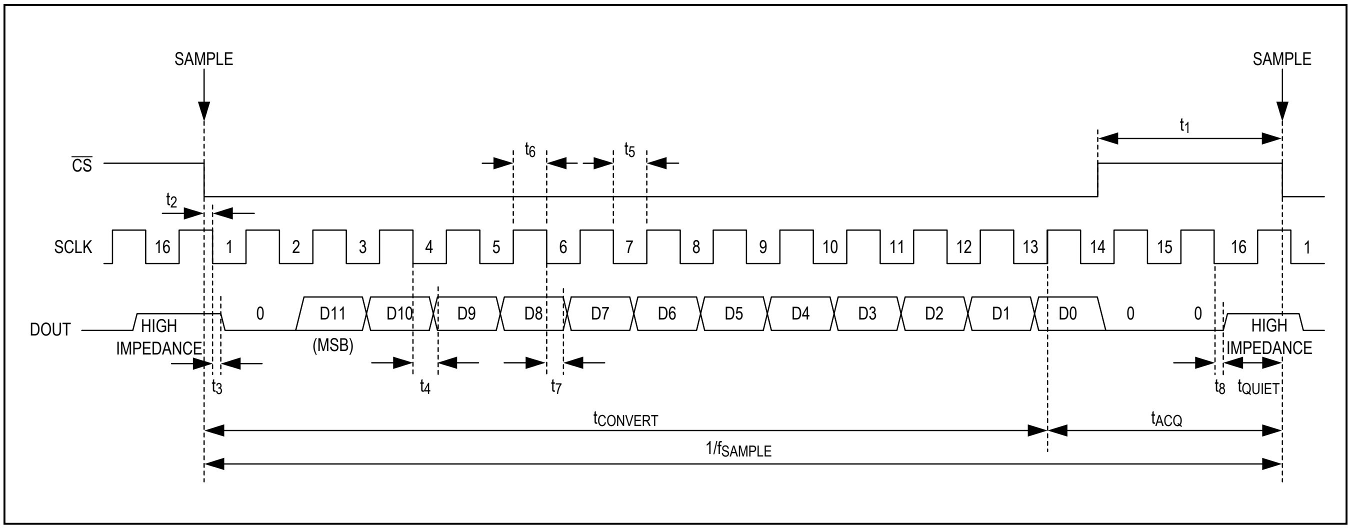


Figure 1. Interface Signals for Maximum Throughput, 12-Bit Devices

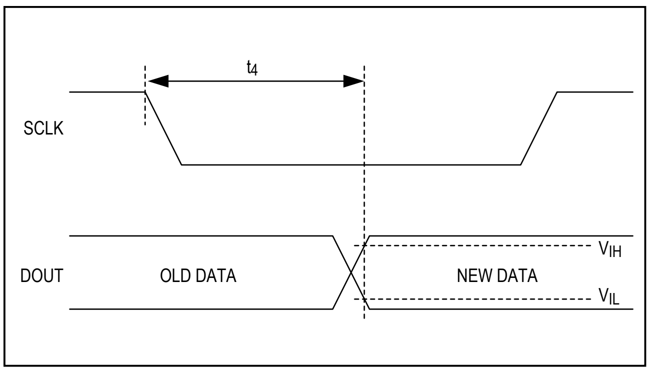


Figure 2. Setup Time After SCLK Falling Edge

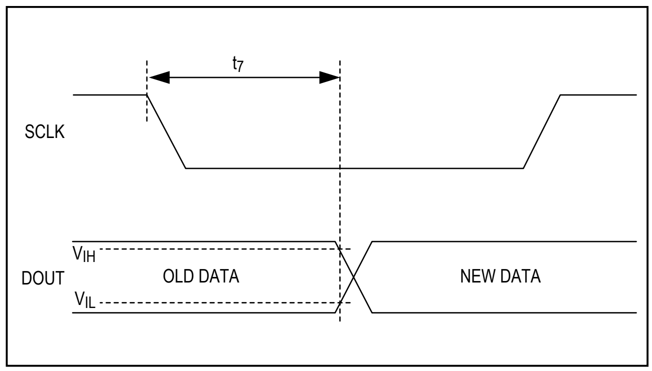


Figure 3. Hold Time After SCLK Falling Edge

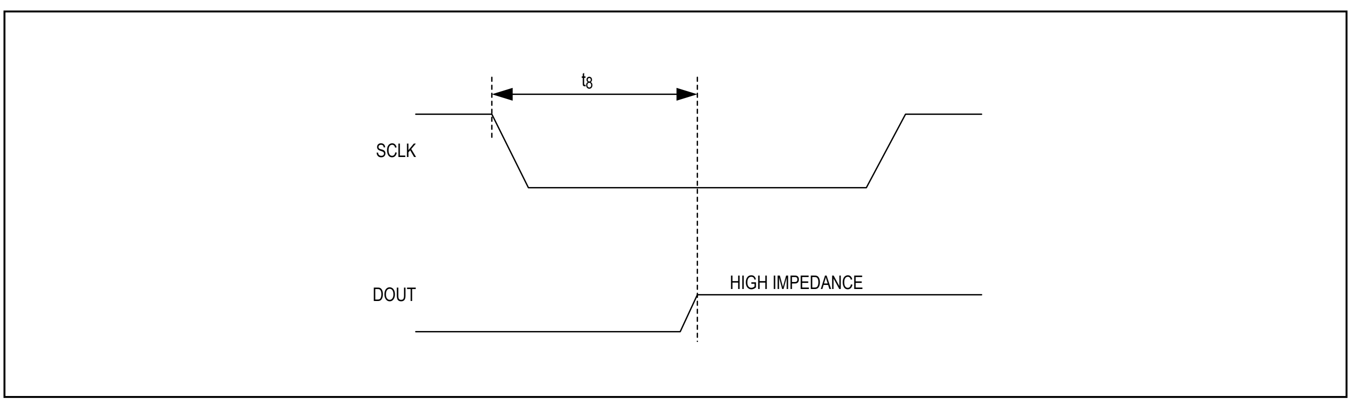
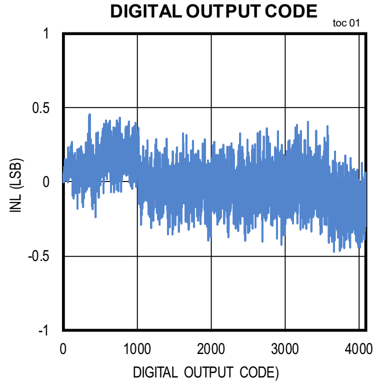


Figure 4. SCLK Falling Edge DOUT Three-State

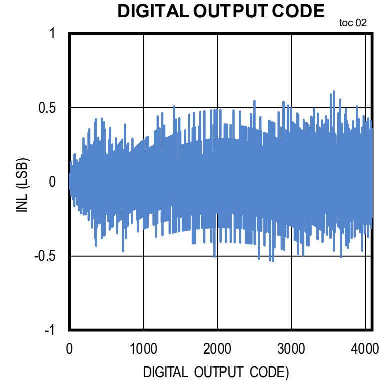
Typical Operating Characteristics

(MAX19777AZA+, T_A = +25°C, unless otherwise noted.)

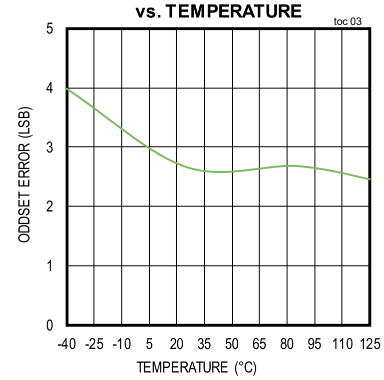
INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE



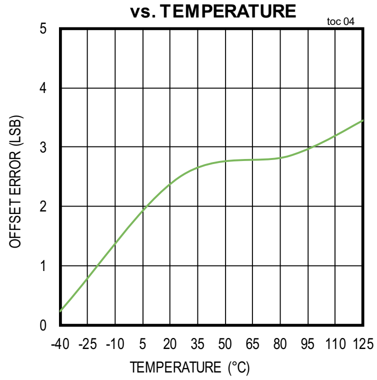
DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE



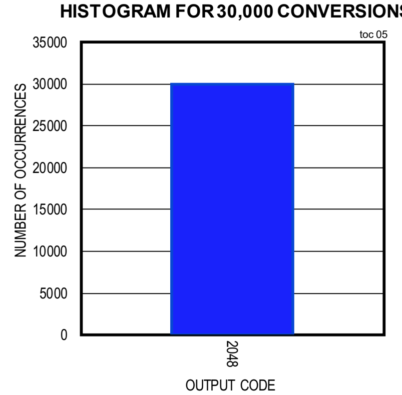
OFFSET ERROR vs. TEMPERATURE



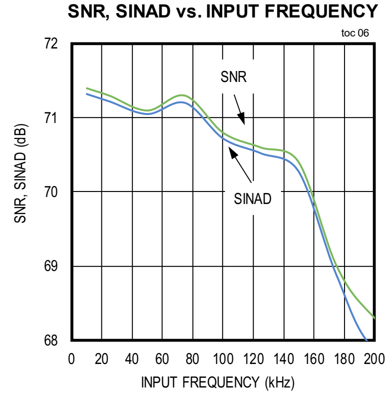
GAIN ERROR vs. TEMPERATURE



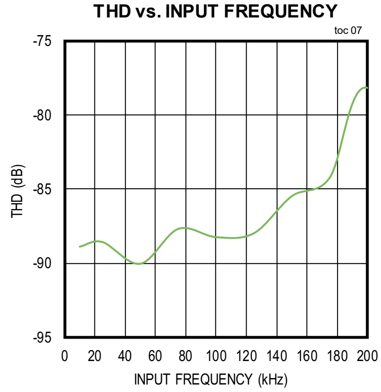
HISTOGRAM FOR 30,000 CONVERSIONS



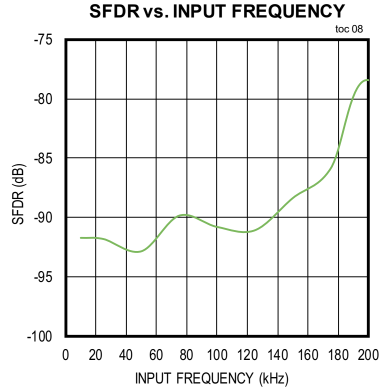
SNR, SINAD vs. INPUT FREQUENCY



THD vs. INPUT FREQUENCY

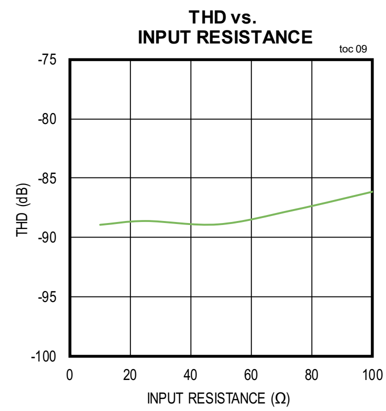


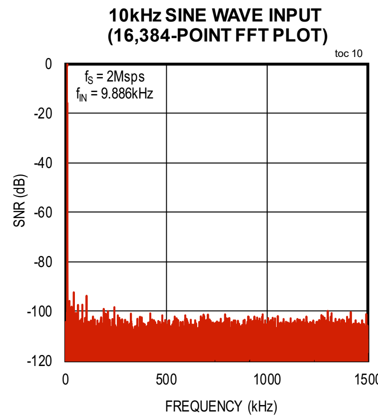
SFDR vs. INPUT FREQUENCY

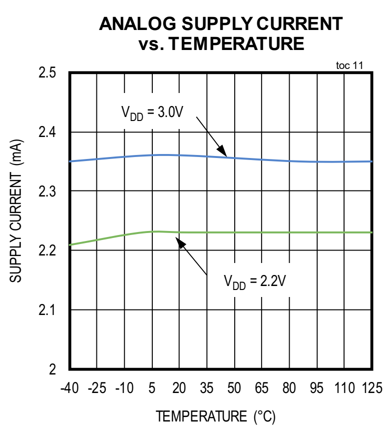


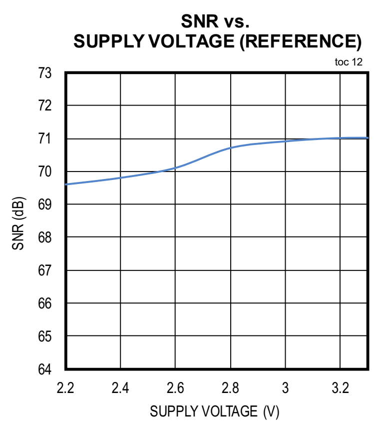
Typical Operating Characteristics (continued)

(MAX19777AZA+, T_A = +25°C, unless otherwise noted.)

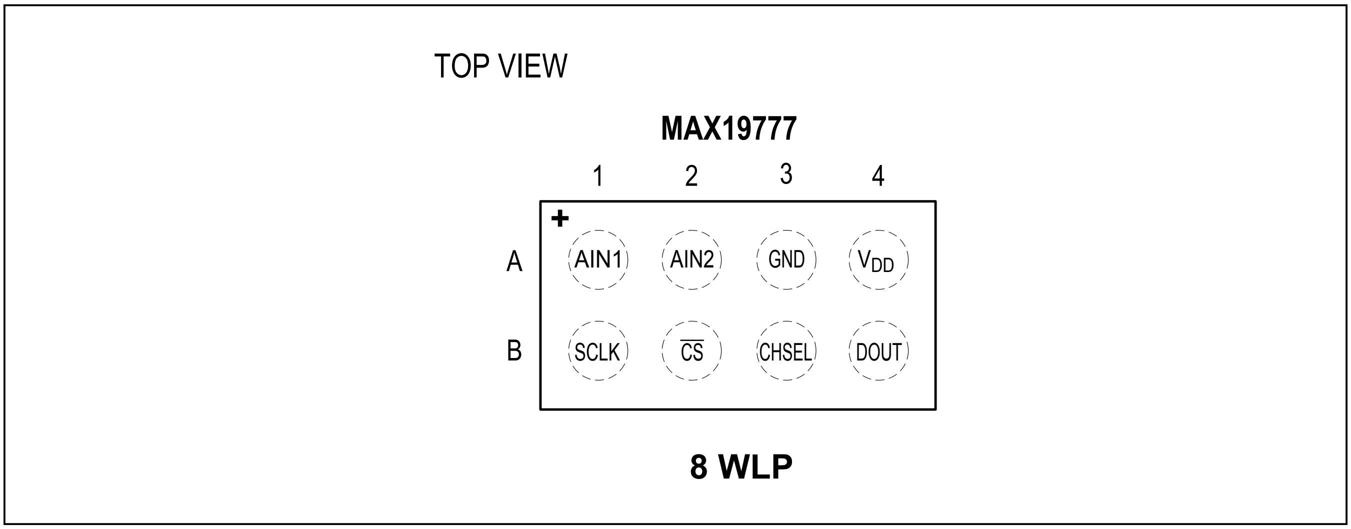








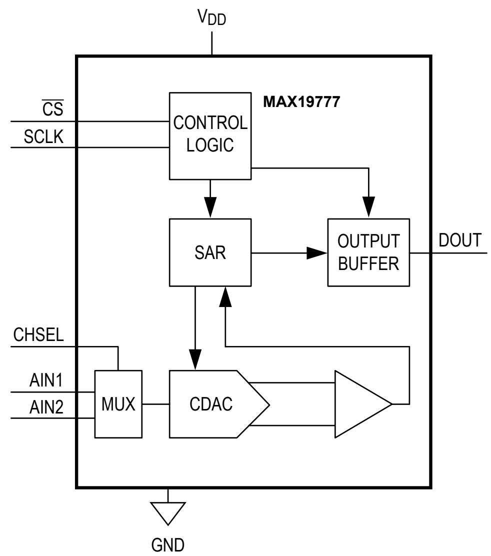
Bump Configuration



Bump Descriptions

PIN	NAME	FUNCTION
A1	AIN1	Analog Input Channel 1. Single-ended analog input with respect to GND with range of 0V to V_{DD}.
A2	AIN2	Analog Input Channel 2. Single-ended analog input with respect to GND with range of 0V to V_{DD}.
A3	GND	Ground. Connect GND directly the GND ground plane.
A4	V_{DD}	Positive Supply Voltage. Bypass V_{DD} with a 10µF || 0.1µF capacitor to GND. V_{DD} range is 2.2V to 3.3V. For the WLP, V_{DD} also defines the signal range of the input signal AIN: 0V to V_{DD}.
B1	SCLK	Serial Clock Input. SCLK drives the conversion process. DOUT is updated on the falling edge of SCLK. See Figure 2 and Figure 3.
B2	$\overline{CS}$	Active-Low Chip-Select Input. The falling edge of $\overline{CS}$ samples the analog input signal, starts a conversion, and frames the serial data transfer.
B3	CHSEL	Channel Select. Set CHSEL high to select AIN2 for conversion. Set CHSEL low to select AIN1 for conversion.
B4	DOUT	Three-State Serial Data Output. ADC conversion results are clocked out on the falling edge of SCLK, MSB first. See Figure 1.

Functional Diagrams



Detailed Description

The MAX19777 is a fast, 12-bit, low-power, single-supply ADC. The device operates from a 2.2V to 3.3V supply and consume only 8.4mW (V_{DD} = 3V)/6.2mW (V_{DD} = 2.2V) at 3Msps. The 3Msps device is capable of sampling at full rate when driven by a 48MHz clock.

The conversion result appears at DOUT, MSB first, with a leading zero followed by the 12-bit result. A 12-bit result is followed by two trailing zeros. See Figure 1 and Figure 5.

The input signal range for AIN1/AIN2 is defined as 0V to V_{DD} with respect to GND.

This ADC includes a power-down feature allowing minimized power consumption at 2.5µA/ksps for lower throughput rates. The wake up and power-down feature is controlled by using the SPI interface as described in the *Operating Modes* section.

Serial Interface

The device features a 3-wire serial interface that directly connects to SPI, QSPI, and MICROWIRE device without external logic. Figure 1 and Figure 5 show the interface signals for a single conversion frame to achieve maximum throughput.

The falling-edge of $\overline{CS}$ defines the sampling instant. Once $\overline{CS}$ transitions low, the external clock signal (SCLK) controls the conversion.

The SAR core successively extracts binary-weighted bits in every clock cycle. The MSB appears on the data bus during the 2nd clock cycle with a delay outlined in the timing specifications. All extracted data bits appear successively on the data bus with the LSB appearing during the 13th clock cycle for 12-bit operation. The serial data stream of conversion bits is preceded by a leading "zero" and succeeded by trailing "zeros." The data output (DOUT) goes into high-impedance state during the 16th clock cycle.

To sustain the maximum sample rate, the device has to be resampled immediately after the 16th clock cycle. For lower sample rates, the $\overline{CS}$ falling edge can be delayed leaving DOUT in a high-impedance condition. Pull $\overline{CS}$ high after the 10th SCLK falling edge (see the *Operating Modes* section).

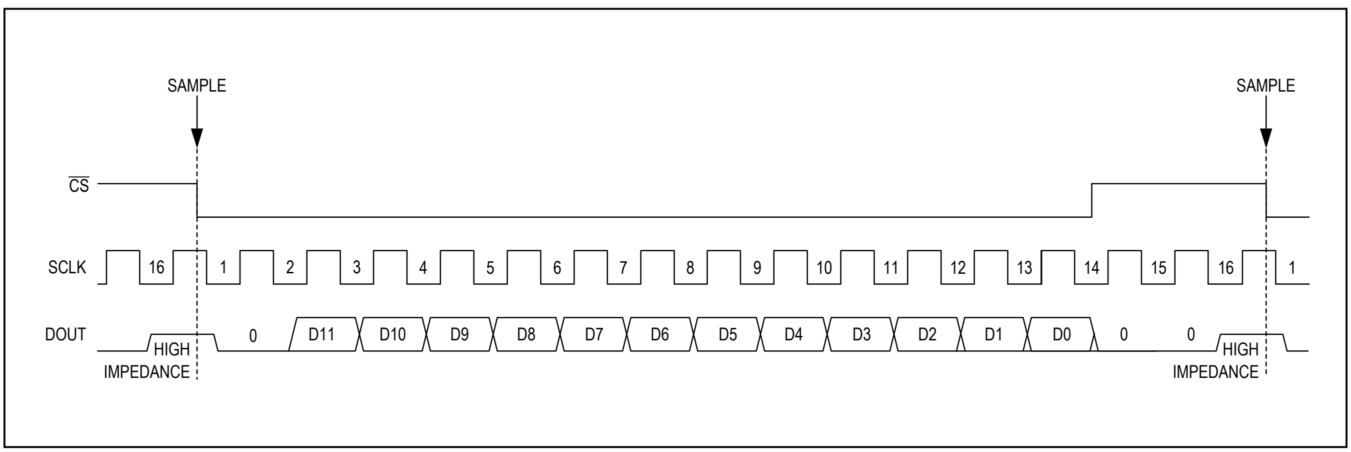


Figure 5. 12-Bit Timing Diagrams

Analog Input

The devices produce a digital output that corresponds to the analog input voltage within the specified operating range of 0 to V_{DD} for the dual-channel device.

Figure 6 shows an equivalent circuit for the analog input AIN1/AIN2. Internal protection diodes D1/D2 confine the analog input voltage within the power rails (V_{DD}, GND). The analog input voltage can swing from GND - 0.3V to V_{DD} + 0.3V without damaging the device.

The electric load presented to the external stage driving the analog input varies depending on which mode the ADC is in: track mode vs. conversion mode. In track mode, the internal sampling capacitor C_S (16pF) has to be charged through the resistor R (R = 50Ω) to the input voltage. For faithful sampling of the input, the capacitor voltage on C_S has to settle to the required accuracy during the track time.

The source impedance of the external driving stage in conjunction with the sampling switch resistance affects the settling performance. The THD vs. Input Resistance graph in the *Typical Operating Characteristics* shows THD sensitivity as a function of the signal source impedance. Keep the source impedance at a minimum for high dynamic performance applications. Use a high-performance op amp, such as the MAX4430, to drive the analog input, thereby decoupling the signal source and the ADC.

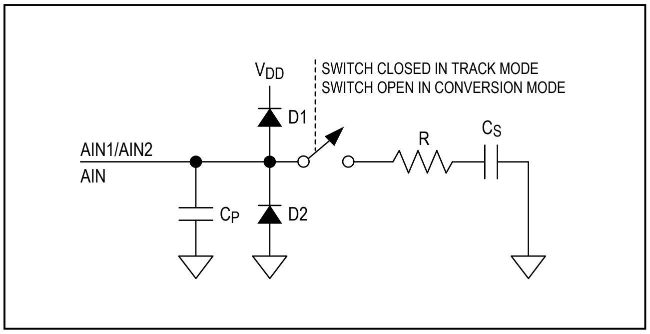


Figure 6. Analog Input Circuit

While the ADC is in conversion mode, the sampling switch is open presenting a pin capacitance, C_P (C_P = 5pF), to the driving stage. See the *Applications Information* section for information on choosing an appropriate buffer for the ADC.

ADC Transfer Function

The output format is straight binary. The code transitions midway between successive integer LSB values such as 0.5 LSB, 1.5 LSB, etc. The LSB size for dual-channel devices is $V_{DD}/2^n$, where n is the resolution. The ideal transfer characteristic is shown in Figure 10.

Operating Modes

The ICs offer two modes of operation: normal mode and power-down mode. The logic state of the $\overline{CS}$ signal during a conversion activates these modes. The power-down mode can be used to optimize power dissipation with respect to sample rate.

Normal Mode

In normal mode, the devices are powered up at all times, thereby achieving their maximum throughput rates. Figure 7 shows the timing diagram of these devices in normal mode. The falling edge of $\overline{CS}$ samples the analog input signal, starts a conversion, and frames the serial data transfer.

To remain in normal mode, keep $\overline{CS}$ low until the falling edge of the 10th SCLK cycle. Pulling $\overline{CS}$ high after the 10th SCLK falling edge keeps the part in normal mode. However, pulling $\overline{CS}$ high before the 10th SCLK falling edge terminates the conversion, DOUT goes into high-impedance mode, and the device enters power-down mode. See Figure 8.

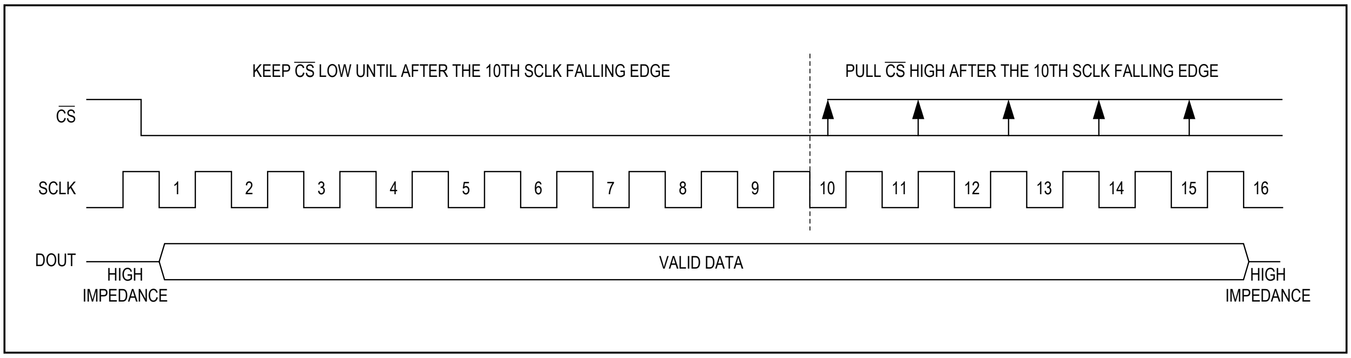


Figure 7. Normal Mode

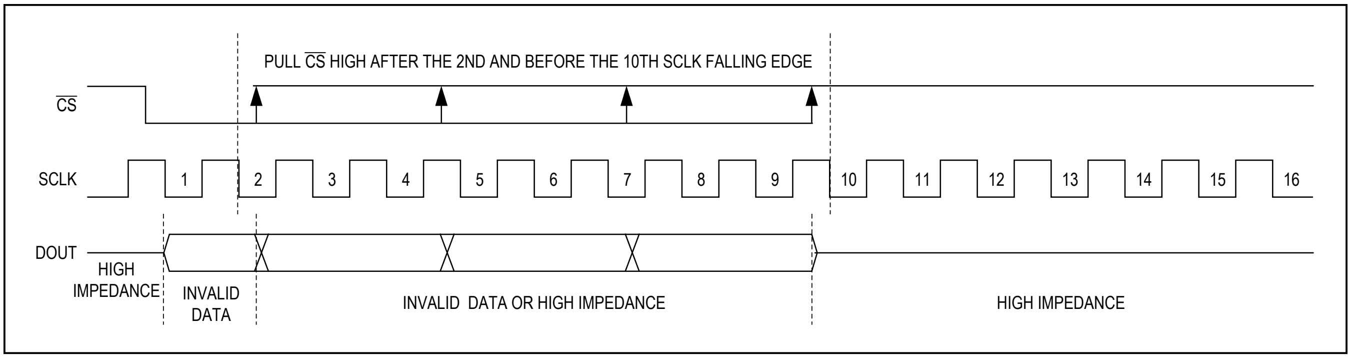


Figure 8. Entering Power-Down Mode

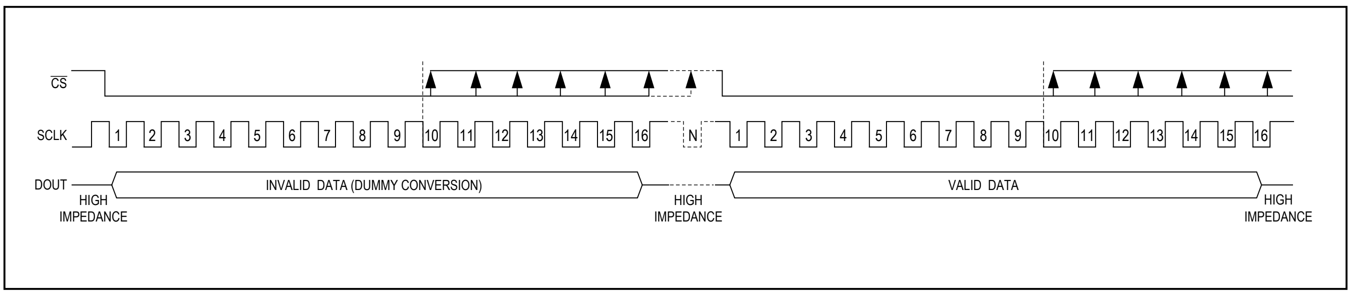


Figure 9. Exiting Power-Down Mode

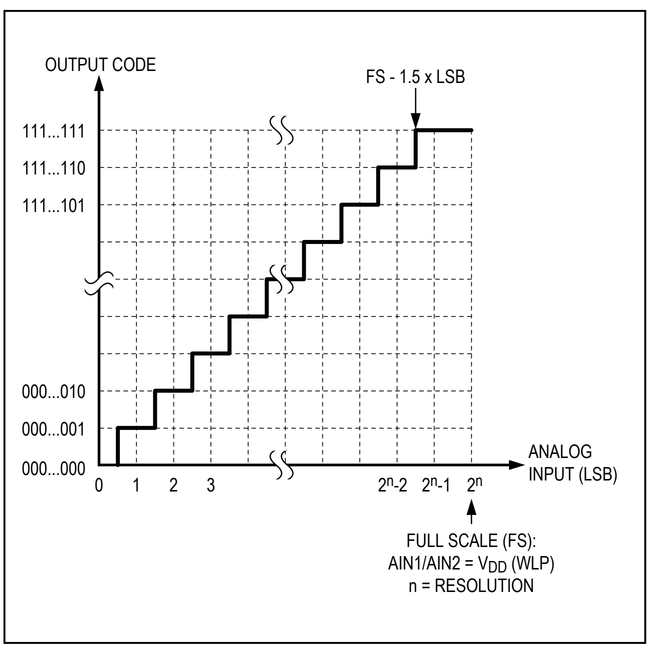


Figure 10. ADC Transfer Function

Power-Down Mode

In power-down mode, all bias circuitry is shut down drawing typically only 1.3μA of leakage current. To save power, put the device in power-down mode between conversions. Using the power-down mode between conversions is ideal for saving power when sampling the analog input infrequently.

Entering Power-Down Mode

To enter power-down mode, drive $\overline{CS}$ high between the 2nd and 10th falling edges of SCLK (see Figure 8). By pulling $\overline{CS}$ high, the current conversion terminates and DOUT enters high impedance.

Exiting Power-Down Mode

To exit power-down mode, implement one dummy conversion by driving $\overline{CS}$ low for at least 10 clock cycles (see Figure 9). The data on DOUT is invalid during this dummy conversion. The first conversion following the dummy cycle contains a valid conversion result.

The power-up time equals the duration of the dummy cycle, and is dependent on the clock frequency. The power-up time for 3Msps operation (48MHz SCLK) is 333ns.

Supply Current vs. Sampling Rate

For applications requiring lower throughput rates, the user can reduce the clock frequency (f_{SCLK}) to lower the sample rate. Figure 11 shows the typical supply current (I_{VDD}) as a function of sample rate (f_S) for the 3Msps devices. The part operates in normal mode and is never powered down.

The user can also power down the ADC between conversions by using the power-down mode. Figure 12 shows for the 3Msps device that as the sample rate is reduced, the device remains in the power-down state longer and the average supply current (I_{VDD}) drops accordingly.

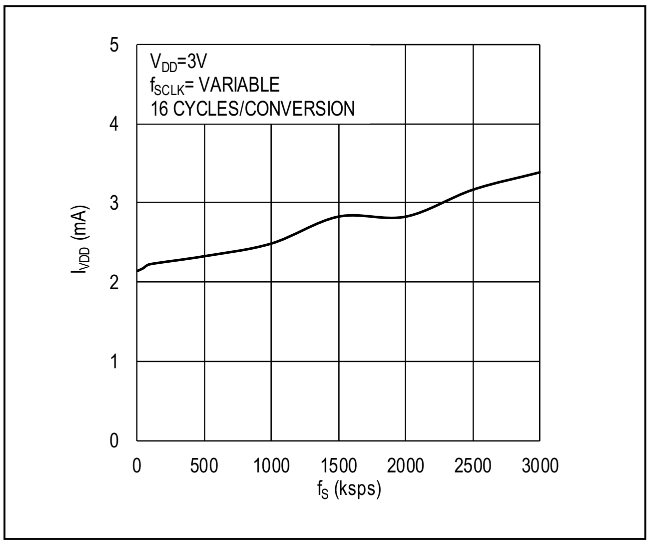


Figure 11. Supply Current vs. Sample Rate (Normal Operating Mode, 3Msps Devices)

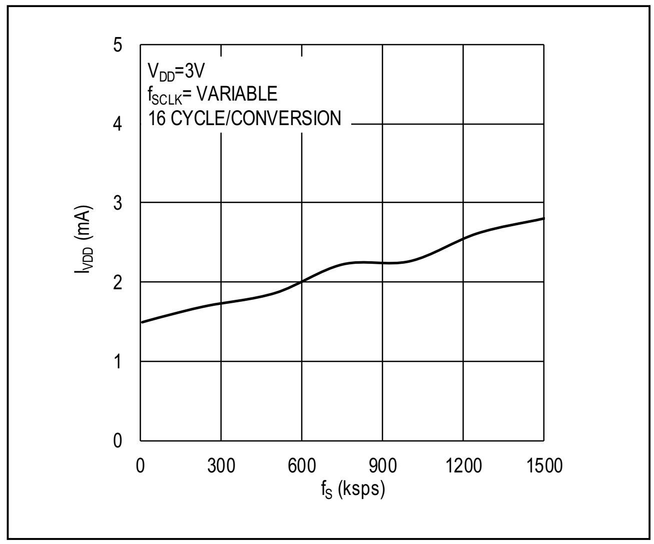


Figure 12. Supply Current vs. Sample Rate (Device Powered Down Between Conversions, 3Msps Devices)

Dual-Channel Operation

The MAX19777 features dual-input channels. This device uses a channel-select (CHSEL) input to select between analog input AIN1 (CHSEL = 0) or AIN2 (CHSEL = 1). As shown in Figure 13, the CHSEL signal is required to change between the 2nd and 12th clock cycle within a regular conversion to guarantee proper switching between channels.

14-Cycle Conversion Mode

The ICs can operate with 14 cycles per conversion. Figure 14 shows the corresponding timing diagram. Observe that DOUT does not go into high-impedance mode. Also, observe that t_{ACQ} needs to be sufficiently long to guarantee proper settling of the analog input voltage. See the *Electrical Characteristics* table for t_{ACQ} requirements and the *Analog Input* section for a description of the analog inputs.

Applications Information

Layout, Grounding, and Bypassing

For best performance, use PCBs with a solid ground plane. Ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another or digital lines underneath the ADC package. Noise in the V_{DD} power supply affects the ADC's performance. Bypass V_{DD} to ground with 0.1µF and 10µF bypass capacitors. Minimize capacitor lead and trace lengths for best supply-noise rejection.

Choosing an Input Amplifier

It is important to match the settling time of the input amplifier to the acquisition time of the ADC. The conversion results are accurate when the ADC samples the input signal for an interval longer than the input signal's worst-case settling time. By definition, settling time is the interval between the application of an input voltage step and the

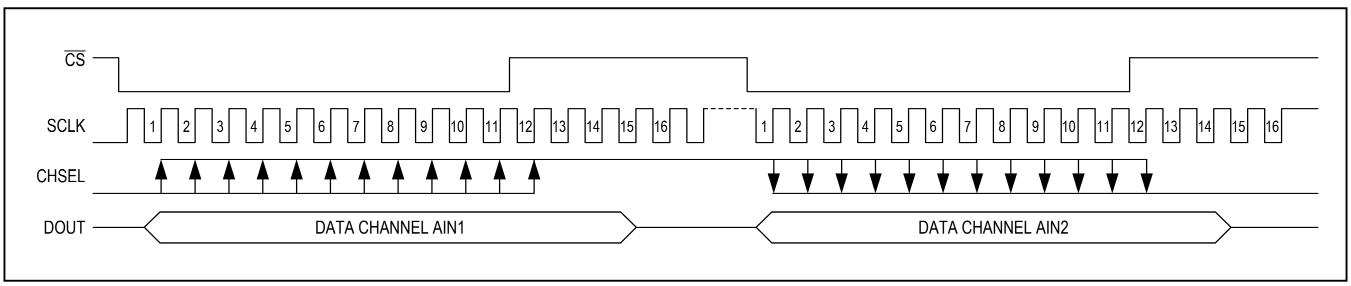


Figure 13. Channel Select Timing Diagram

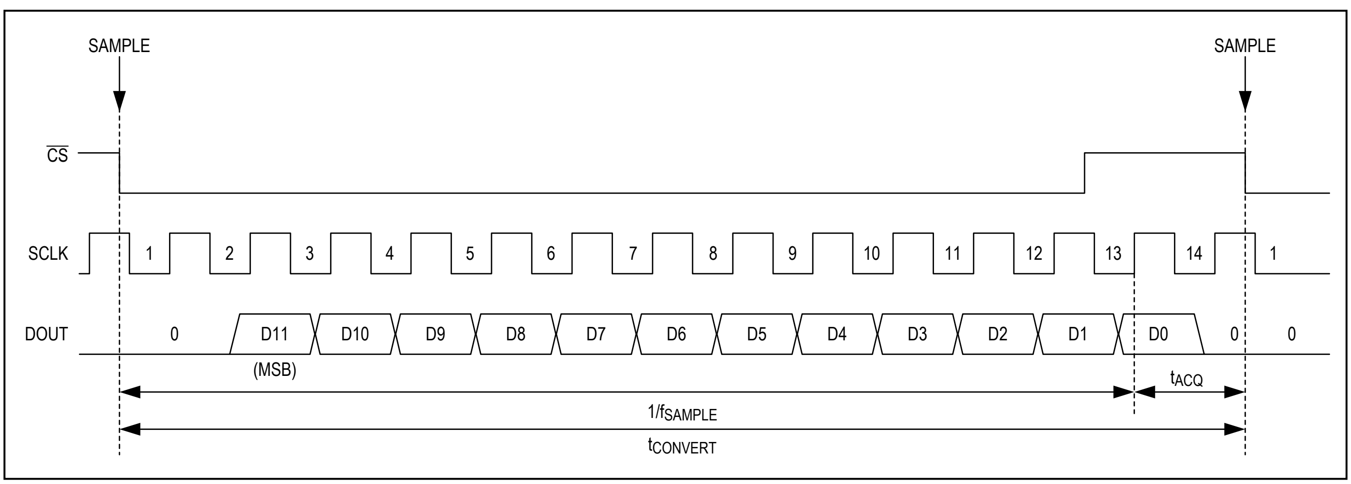


Figure 14. 14-Clock Cycle Operation

point at which the output signal reaches and stays within a given error band centered on the resulting steady-state amplifier output level. The ADC input sampling capacitor charges during the sampling cycle, referred to as the acquisition period. During this acquisition period, the settling time is affected by the input resistance and the input sampling capacitance. This error can be estimated by looking at the settling of an RC time constant using the input capacitance and the source impedance over the acquisition time period.

Figure 15 shows a typical application circuit. The MAX4430, offering a settling time of 37ns at 16 bits, is an excellent choice for this application. See the THD vs. Input Resistance graph in the *Typical Operating Characteristics*.

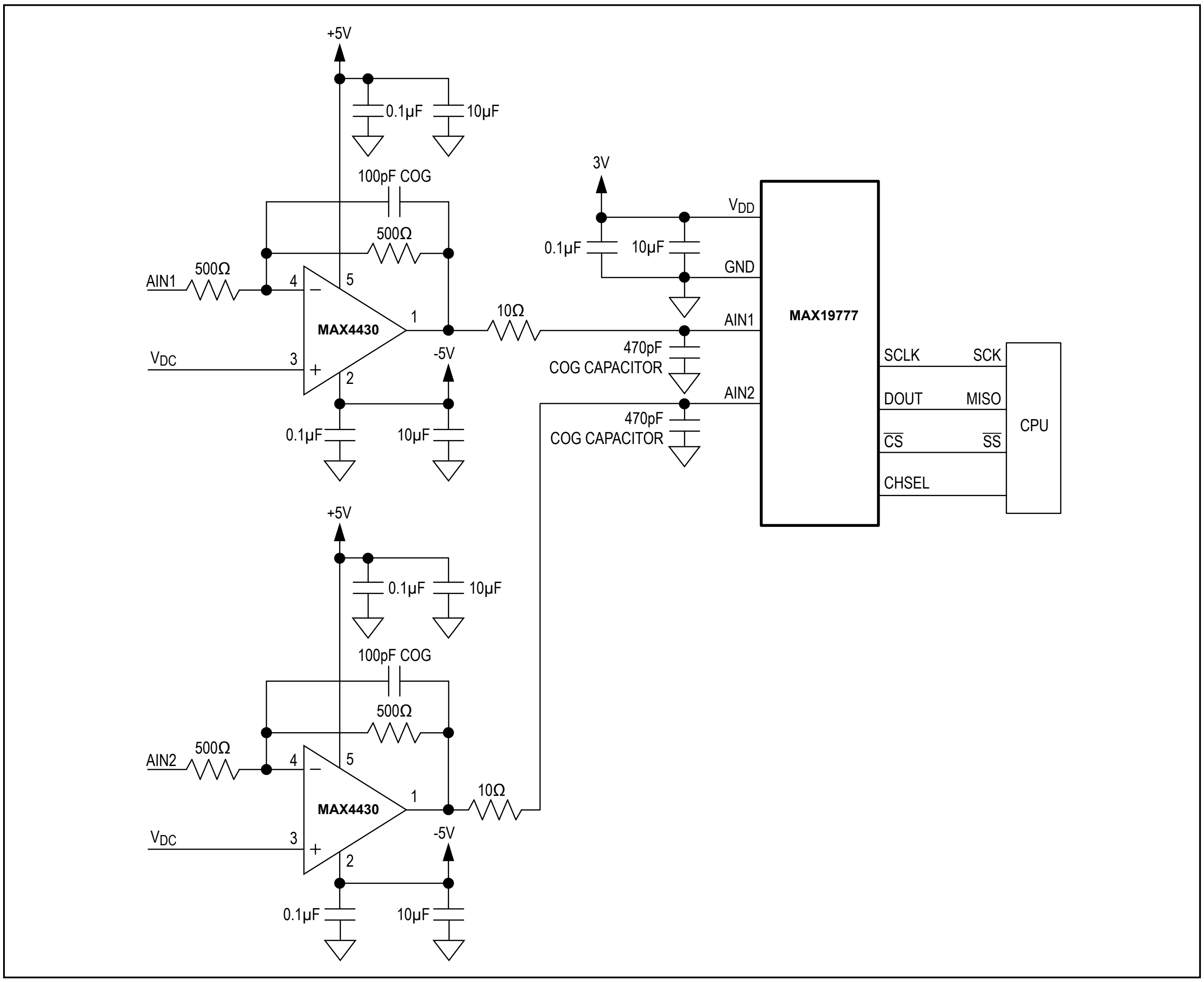


Figure 15. Typical Application Circuit

Definitions

For the MAX19777, V_{REF} is internally tied to V_{DD}.

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. For this device, the straight line is a line drawn between the end points of the transfer function after offset and gain errors are nulled.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of ±1 LSB or less guarantees no missing codes and a monotonic transfer function.

Offset Error

The deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, that is, AGND + 0.5 LSB.

Gain Error

The deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal after adjusting for the offset error, that is, V_{REF} - 1.5 LSB.

Aperture Jitter

Aperture jitter (t_{AJ}) is the sample-to-sample variation in the time between the samples.

Aperture Delay

Aperture delay (t_{AD}) is the time between the falling edge of sampling clock and the instant when an actual sample is taken.

Signal-to-Noise Ratio (SNR)

SNR is a dynamic figure of merit that indicates the converter's noise performance. For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$\text{SNR (dB) (MAX)} = (6.02 \times N + 1.76)\ \text{(dB)}$$

In reality, there are other noise sources such as thermal noise, reference noise, and clock jitter that also degrade SNR. SNR is computed by taking the ratio of the RMS signal to the RMS noise. RMS noise includes all spectral components to the Nyquist frequency excluding the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Ratio and Distortion (SINAD)

SINAD is a dynamic figure of merit that indicates the converter's noise and distortion performance. SINAD is computed by taking the ratio of the RMS signal to the RMS noise plus distortion. RMS noise plus distortion includes all spectral components to the Nyquist frequency excluding the fundamental and the DC offset:

$$\text{SINAD(dB)} = 20 \times \log\left[\frac{\text{SIGNAL}_{RMS}}{(\text{NOISE} + \text{DISTORTION})_{RMS}}\right]$$

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$\text{THD} = 20 \times \log\left(\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1}\right)$$

where V_1 is the fundamental amplitude and V_2–V_5 are the amplitudes of the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range (SFDR)

SFDR is a dynamic figure of merit that indicates the lowest usable input signal amplitude. SFDR is the ratio of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest spurious component, excluding DC offset. SFDR is specified in decibels with respect to the carrier (dBc).

Full-Power Bandwidth

Full-power bandwidth is the frequency at which the input signal amplitude attenuates by 3dB for a full-scale input.

Full-Linear Bandwidth

Full-linear bandwidth is the frequency at which the signal-to-noise ratio and distortion (SINAD) is equal to a specified value.

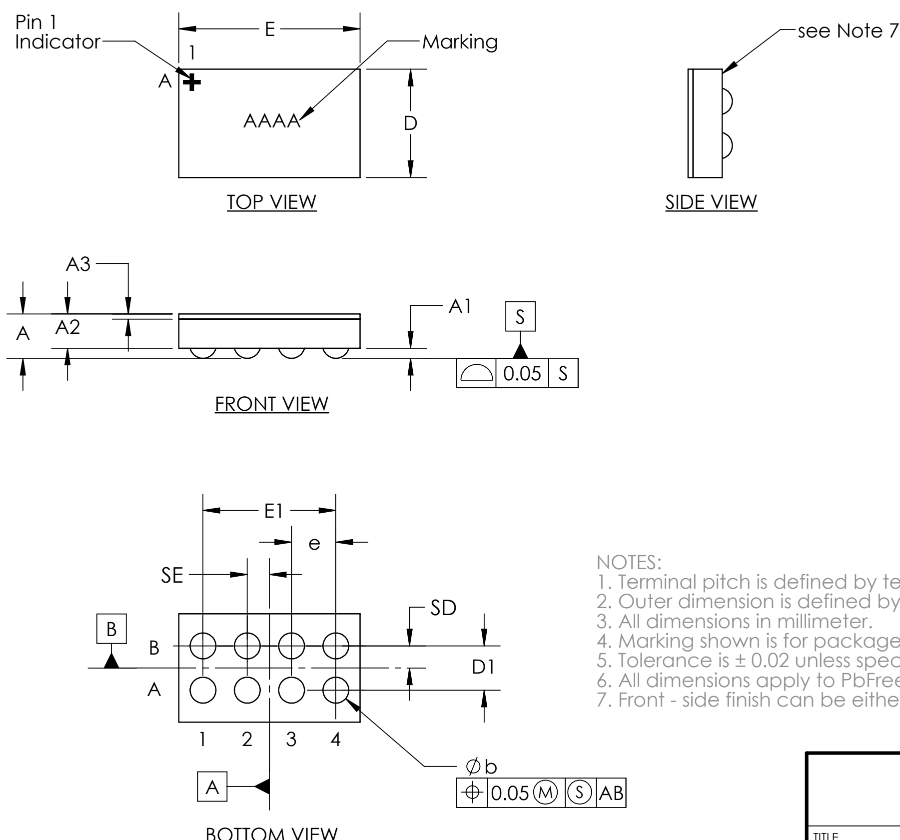
Intermodulation Distortion

Any device with nonlinearities creates distortion products when two sine waves at two different frequencies (f_1 and f_2) are applied into the device. Intermodulation distortion (IMD) is the total power of the IM2 to IM5 intermodulation products to the Nyquist frequency relative to the total input power of the two input tones, f_1 and f_2. The individual input tone levels are at -6dBFS.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 WLP	Z80B1+1	21-100166	Refer to Application Note 1891



COMMON DIMENSIONS	
A	0.35 ±0.02
A1	0.08 ±0.01
A2	0.27 REF
A3	0.040 BASIC
b	Ø0.21 ±0.03
D	0.857 ±0.025
E	1.432 ±0.025
D1	0.35 BASIC
E1	1.05 BASIC
e	0.35 BASIC
SD	0.175 BASIC
SE	0.175 BASIC
DEPOPULATED BUMPS: NONE	

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

- DRAWING NOT TO SCALE -

maxim integrated™

TITLE PACKAGE OUTLINE 8 BUMPS ULTRA THIN WLP PKG. 0.35 mm PITCH, Z80B1+1

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-100166	A	1/1

Ordering Information

PART	PIN-PACKAGE	BITS	SPEED (Msps)	NO. OF CHANNELS	TOP MARK
MAX19777AZA+	8 WLP	12	3	2	AAAH
MAX19777AZA+T	8 WLP	12	3	2	AAAH

Note: *Devices specified over the -40°C to +125°C operating temperature range.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
T= Tape and reel.

Chip Information

PROCESS: CMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/17	Initial release	—

