Click here for production status of specific part numbers.

MAX20019/MAX20020

3.2MHz, 500mA Dual Step-Down Converters for Automotive Cameras

General Description

MAX20019/MAX20020 are 2.2MHz and 3.2MHz dual step-down converters with integrated high-side and low-side MOSFETs. The high-voltage step-down converter is designed for continuous operation up to 17V input voltages. The output voltage is factory preset. Buck 1 is preset to 3.3V, 3.0V, or 2.8V. Buck 2 is preset to 1.8V, 1.5V, 1.2V, or 1V. Another option is Buck 1 preset to 5V and Buck 2 preset to 3.3V.

The low-voltage buck features fixed-frequency PWM-mode operation with a switching frequency of 2.2MHz or 3.2MHz. High-frequency operation allows for an all-ceramic capacitor design and small-size external components. The low-resistance on-chip switches ensure high efficiency while minimizing critical inductance. A 500mV enable hysteresis on the MAX20019 allows the use of long, low-cost coax cables, even during slow start-up situations. The MAX20020's Buck 1 starts after V_{SUP} is greater than 5.5V and Buck 1 is driven by the EN input.

Protection features include overvoltage (OV) protection, cycle-by-cycle current limit, and thermal shutdown with automatic recovery. The buck converters operate 180° out-of-phase from each other to minimize input-current ripple.

Applications

- Surround-View Camera Power Supplies
- Automotive Point-of-Load

Benefits and Features

- Small Solution Size
  - 2mm x 3mm x 0.75mm 10-pin TDFN with an Exposed Pad
  - 2.2MHz and 3.2MHz Operation Allows Smaller System Size
  - No External Components Needed for Soft-Start
- Cable Flexibility
  - 500mV Enable Hysteresis Allows for Long, Low-Cost Cables During Slow Starts
- EMI Solutions
  - Optional Spread-Spectrum Frequency Modulation
  - Pinout Placement Allows for Tight PCB Layout of Switching Nodes
- Self-Protected
  - Overvoltage Protection, Thermal Shutdown, Short-Circuit Protection
- Automotive Ready
  - Wide 3.5V to 17V Input Voltage Range for Power-Over-Coax
  - Automotive Temperature Range -40°C to +125°C
  - AEC-Q100 Qualified

Ordering Information and Typical Operating Circuits appear at end of data sheet.

19-100040; Rev 9; 1/19

maxim integrated™

Absolute Maximum Ratings

SUP, EN, LX1 to PGND* ..... -0.3V to +18V
OUT2 to PGND ..... -0.3V to (V_{PV2} + 0.3)V
BST to LX1 ..... -0.3V to +6V
PV2, LX2 to PGND* ..... -0.3V to +6V
AGND to PGND ..... -0.3V to +0.3V
BIAS to AGND ..... -0.3V to +6.0V
LX1 Short-Circuit Duration ..... Continuous
LX2 Short-Circuit Duration ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
derate 15.7mW/°C above +70°C 1253.9mW

Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C
Lead Temperature ..... +300°C

**LX1 has internal clamp diodes to PGND/AGND and SUP. LX2 has internal clamp diodes to PV2 and PGND. Applications that forward bias these diodes should take care not to exceed the IC's package power-dissipation limits.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 10 TDFN	
Package Code	T1032+2C
Outline Number	**21-100125**
Land Pattern Number	**90-100079**
PACKAGE TYPE: 10 SWTDFN	
Package Code	T1032Y+2C
Outline Number	**21-100197**
Land Pattern Number	**90-100079**
THERMAL RESISTANCE, SINGLE-LAYER BOARD	
Junction to Ambient (θ_{JA})	87.5°C/W
Junction to Case (θ_{JC})	11.7°C/W
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	63.8°C/W
Junction to Case (θ_{JC})	11.7°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{SUP} = 8V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{SUP}	MAX20019	3.5		17	V
		MAX20020 V_{SUP} rising	5.5		17	
		MAX20020 V_{SUP} falling	5			
Supply Current	I_{SUP}	EN = high, no switching, V_{OUT1} = 3.3V, V_{OUT2} = 1.8V		2.5	3.5	mA
Shutdown Supply Current	$I_{SUP\_SHUTDOWN}$	V_{EN} = 0V (MAX20019 only)		20	30	µA
		V_{EN} = 0V, V_{SUP} < 4V (MAX20020 only)		20	30	
BIAS Regulator Voltage	V_{BIAS}	V_{SUP} = 6V to 16V, I_{BIAS} = 0mA to 15mA, C_{BIAS} = 2.2µF		4.75		V
BIAS Undervoltage Lockout	V_{UVBIAS}	V_{BIAS} falling		2.7	2.9	V
BIAS Undervoltage-Lockout Hysteresis	$V_{UVBIASHYS}$			400	650	mV
Thermal-Shutdown Threshold				175		°C
Thermal-Shutdown-Threshold Hysteresis				15		°C
BUCK CONVERTER (OUT1)						
Output Voltage	V_{OUT1}	f_{SW} = 3.2MHz, 6V < V_{SUP} < 9V, I_{OUT1} = 0mA to 500mA, V_{OUT1} = 3.3V, 3.0V, 2.8V	-3		+3	%
		f_{SW} = 2.2MHz, 6V < V_{SUP} < 9V, I_{OUT1} = 0mA to 500mA, V_{OUT1} = 3.3V, 3.0V, or 2.8V	-3		+3	
Line Regulation		6V < V_{SUP} < 17V		0.4		%/V
DMOS Peak Current-Limit Threshold	I_{MAX}		0.8	1	1.2	A
High-Side DMOS $R_{DS(ON)}$	R_{ON_HS1}	I_{LX1} = 500mA, V_{BIAS} = 5V		250	500	mΩ
Low-Side DMOS $R_{DS(ON)}$	R_{ON_LS1}	I_{LX1} = 500mA, V_{BIAS} = 5V		200	500	mΩ
Soft-Start Ramp Time	t_{SS1}	f_{SW} = 3.2MHz		1.3		ms
		f_{SW} = 2.2MHz		1.8		
LX1 Rise Time	$t_{RISE, LX1}$			4		ns
LX1 Leakage Current		T_A = +25°C			1	µA
BST Leakage Current		T_A = +25°C			1	µA
Minimum On-Time	t_{ON}				100	ns

Electrical Characteristics (continued)

(V_{SUP} = 8V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM Switching Frequency	f_{SW}			3	3.2	3.4	MHz
		Contact factory		2	2.2	2.4	
Spread Spectrum					±3		%
Maximum Duty Cycle				96			%
OUT1 Pulldown Resistance		V_{OUT1} = 3.3V, internal feedback-divider			330		kΩ
V_{OUT1} Debounce Time		Debounce time on V_{OUT1} falling to 90% before V_{OUT2} starts shutdown; restart once V_{OUT1} > 95%			25		µs
BUCK CONVERTER (OUT2)							
Voltage Accuracy	V_{OUT2}	0A < I_{OUT2} < 500mA, V_{OUT2} = 1.0V		-3.5		+3.5	%
		0A < I_{OUT2} < 500mA, V_{OUT2} = 1.8V, 1.5V or 1.2V		-3		+3	
		0A < I_{OUT2} < 160mA, V_{OUT2} = 1.82V		-3		+3	
High-Side pMOS $R_{DS(ON)}$	R_{ON_HS2}	I_{LX2} = 200mA, V_{PV2} = 2.8V			110	250	mΩ
Low-Side nMOS $R_{DS(ON)}$	R_{ON_LS2}	I_{LX2} = 200mA, V_{PV2} = 2.8V			170	350	mΩ
Current-Limit Threshold	I_{LIM2}			0.8	1	1.2	A
Soft-Start Ramp Time	t_{SS2}	f_{SW} = 3.2MHz			1.3		ms
		f_{SW} = 2.2MHz			1.8		
OUT2 Enable Time	t_{EN2}	Time from OUT1 soft-start done until OUT2 begins soft-starts	f_{SW} = 2.2MHz		1.8		ms
			f_{SW} = 3.2MHz		1.3		
LX2 Leakage Current		V_{PV2} = 2.8V, V_{LX2} = V_{PGND} or V_{PV2}, T_A = +25°C				1	µA
LX Rise/Fall Time		V_{PV2} = 2.8V, I_{OUT2} = 200mA			4		ns
Duty-Cycle Range						100	%
OUT2 Discharge Resistance	R_{OUT2_dis}	Turn on when EN is low, thermal shutdown, or overvoltage			500		Ω
OUT2 Pulldown Resistance		V_{OUT2} = 1.8V, internal feedback-divider			180		kΩ
OUT1, OUT2 Phasing		(Note 2)			180		°
Overvoltage-Protection Threshold		V_{OUT2} rising			107		%
		V_{OUT2} falling			105		

Electrical Characteristics (continued)

(V_{SUP} = 8V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 1)

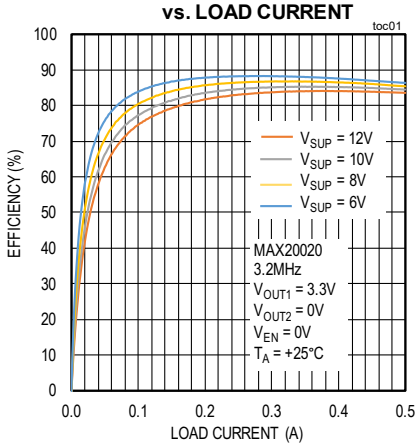
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC LEVEL (EN)						
Input Rising Threshold	V_{EN}	MAX20019	1.0	1.5	2.2	V
Input Hysteresis		Falling hysteresis (MAX20019)		0.5		V
Input Rising Threshold		V_{SUP} rising (MAX20020)		5		V
Input Falling Threshold		V_{SUP} falling (MAX20020)		4.5		V
Input Current		Logic input only, T_A = +25°C		1	1	µA
EN Input High Threshold	V_{EN}	MAX20020, V_{SUP} > 5V, V_{EN} rising	2.4			V
EN Input Low Threshold		MAX20020, V_{SUP} > 5V, V_{EN} falling			0.6	V

Note 1: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage are guaranteed by design and characterization. Typical values are at T_A = +25°C.

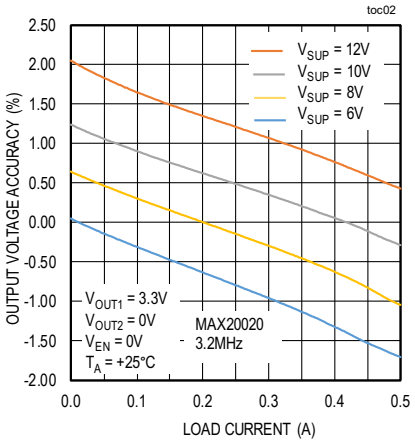
Note 2: Guaranteed by design; not production tested.

Typical Operating Characteristics

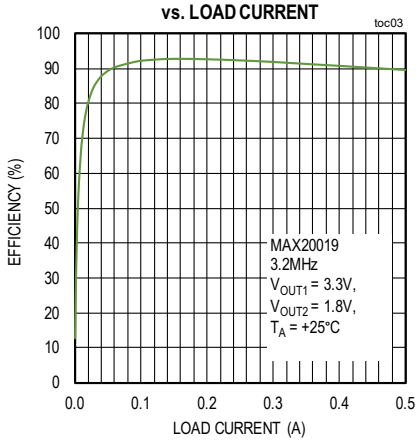
BUCK1 3.2MHz EFFICIENCY vs. LOAD CURRENT



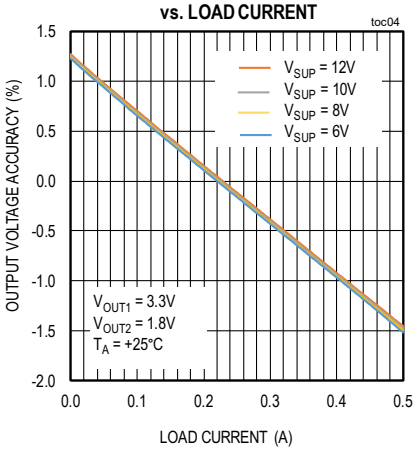
V_{OUT1} vs. LOAD CURRENT



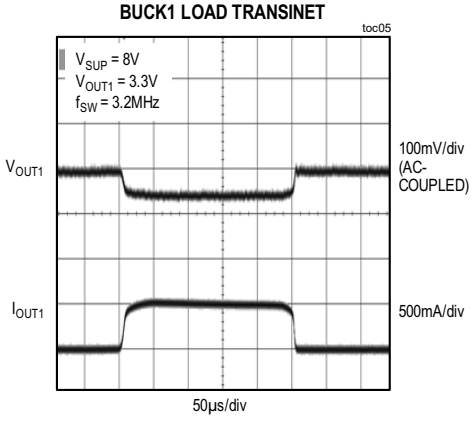
BUCK2 3.2MHz EFFICIENCY vs. LOAD CURRENT



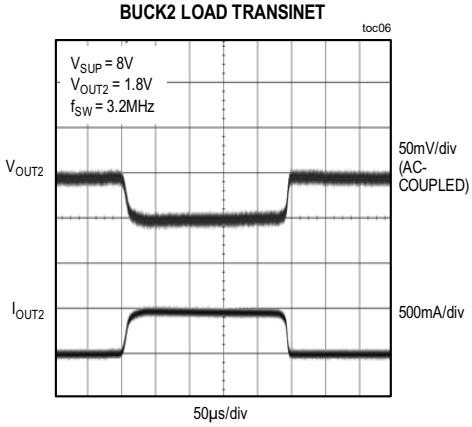
BUCK2 OUTPUT VOLTAGE vs. LOAD CURRENT



BUCK1 LOAD TRANSINET

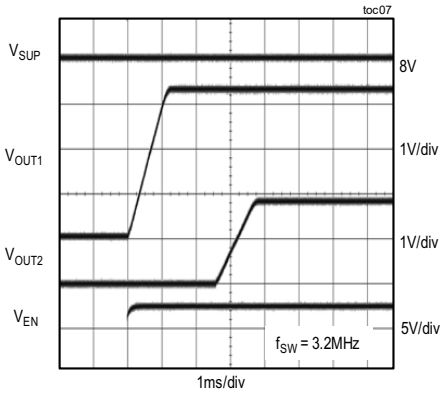


BUCK2 LOAD TRANSINET

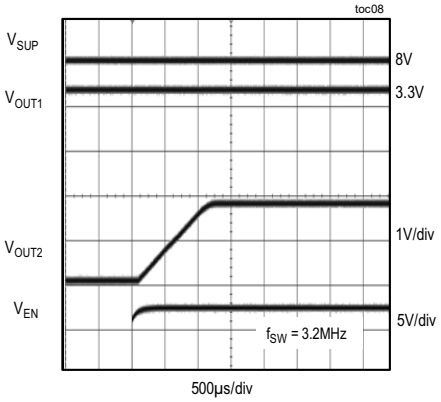


Typical Operating Characteristics (continued)

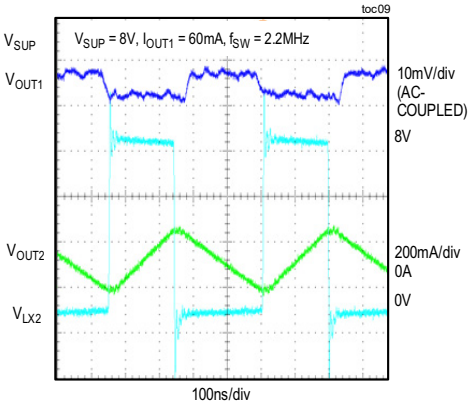
MAX20019 STARTUP



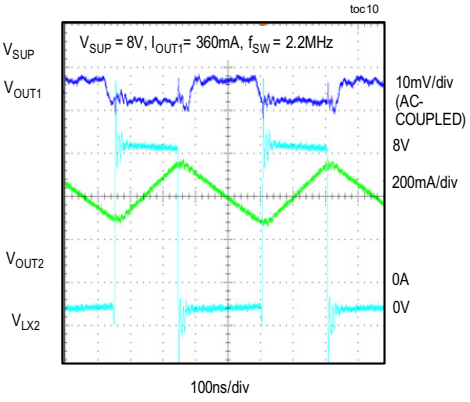
MAX20020 EN BUCK2 STARTUP



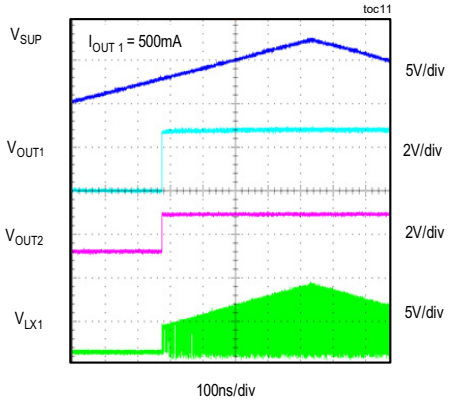
MAX20019 60mA OUTPUT1 RIPPLE



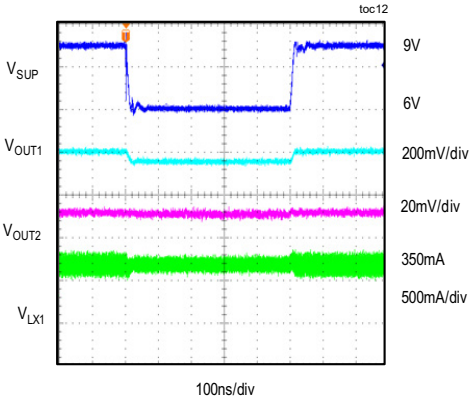
MAX20019 360mA OUTPUT1 RIPPLE



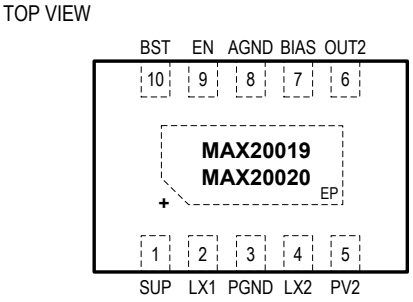
SLOW V_{SUP} - RISING



LINE TRANSIENT



Pin Configuration



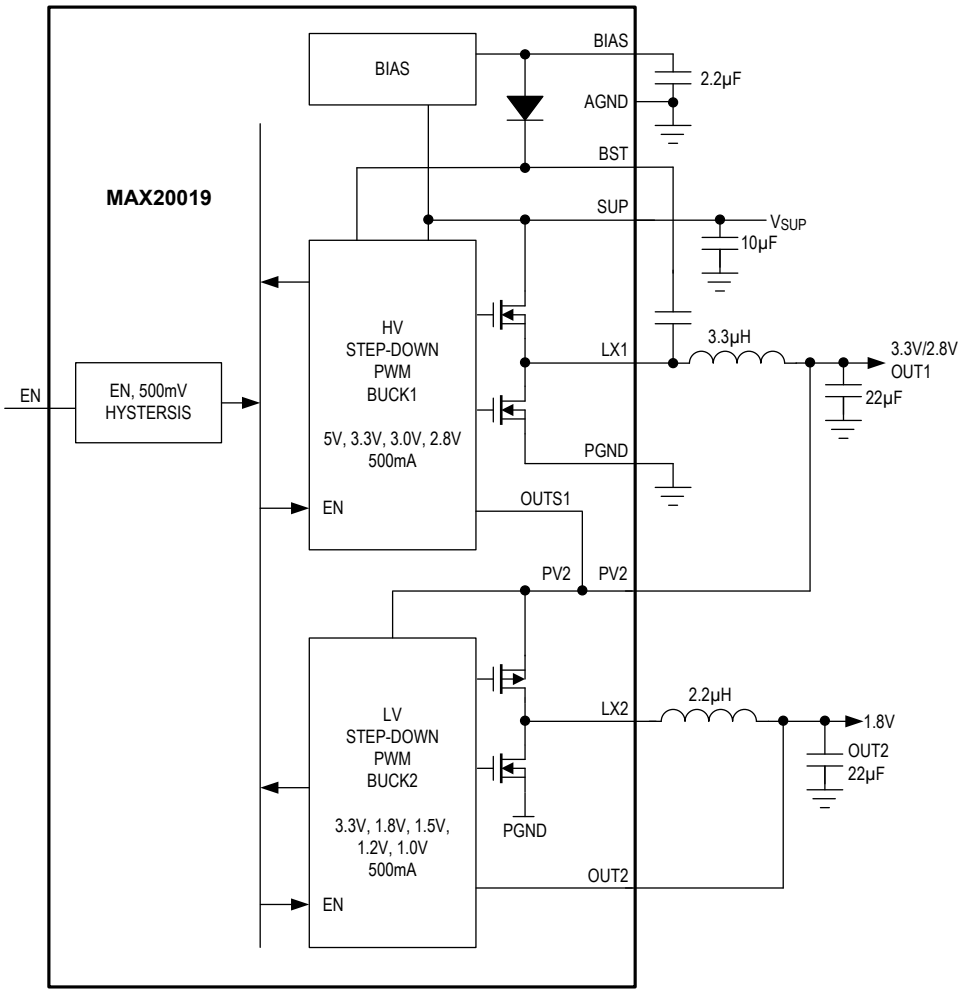
TDFN/SWTDFN
(3mm x 2mm)

*EP = EXPOSED PAD, CONNECTED TO GROUND

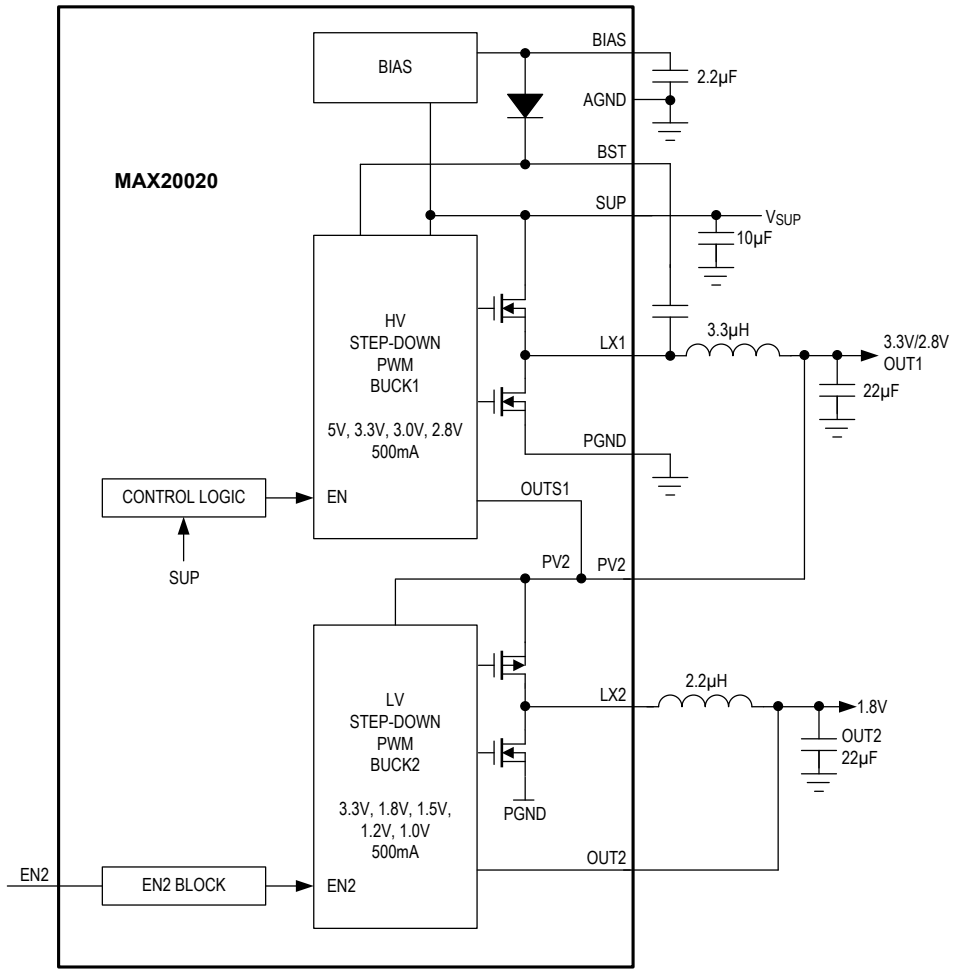
Pin Description

PIN	NAME	FUNCTION
1	SUP	Voltage-Supply Input and Internal High-Side Switch Supply Input. SUP powers the internal linear regulator and power to the internal switches of Buck 1. Connect a 10µF capacitor to ground. See the *Input Capacitor* section.
2	LX1	Inductor Switching Node for Buck 1. Shutdown-discharge resistance when part is disabled. See the *Inductor Selection* section for component values.
3	PGND	Power Ground. Connect PGND and AGND together. Connect to the exposed pad. Refer to the EV kit layout for details.
4	LX2	Inductor Switching Node for Buck 2. See the *Inductor Selection* section for details.
5	PV2	Buck 2 Voltage Input and Voltage-Feedback Sense of Switching-Regulator Output 1. Connect to the output capacitor of Buck 1 with a very short and wide trace. See the *PCB Layout Guidelines* section.
6	OUT2	Voltage Feedback Sense of Switching Regulator Output 2. The discharge resistor is enabled when EN = 0, overvoltage on Buck 2, or thermal shutdown occurs.
7	BIAS	Linear Regulator Output. BIAS powers up the internal circuitry. Bypass with a 2.2µF capacitor to ground.
8	AGND	Analog Ground. Connect PGND and AGND together at the input capacitor. See the *PCB Layout Guidelines* section.
9	EN	High-Voltage-Tolerant Enable Input with Hysteresis. Driving the MAX20019 EN high enables Buck 1 and Buck 2 based on the timing in the *Electrical Characteristics* table. Driving the MAX20020 EN high enables Buck 2.
10	BST	High-Side Driver Supply. Connect a 0.1µF capacitor between LX1 and BST for proper operation.
—	EP	Exposed Pad. Must be connected to ground plane on PCB, but is not a current-carrying path, only needed for thermal transfer.

Functional Diagrams



Functional Diagrams (continued)



Detailed Description

The MAX20019/MAX20020 are small, dual synchronous step-down converters with integrated high-side and low-side MOSFETs. The low-side MOSFET enables fixed-frequency forced-PWM (FPWM) operation. The high-voltage step-down converters operate up to 17V input voltages. The switching frequency is set to 3.2MHZ or factory programmable to 2.2MHz allowing for small component size. The devices' output voltage is factory preset with Buck 1 set to 3.3V, 3.0V, or 2.8V, and Buck 2 preset to 1.8V, 1.5V, 1.2V, or 1V. Buck 1 can be set to 5V with Buck 2 set to 3.3V. The Buck 1 converter can run at 96% duty cycle in dropout and the Buck 2 converter can run at 100% duty cycle in dropout.

The MAX20019 EN pin uses a 500mV hysteresis to accommodate for long and high-impedance cables. The MAX20020 Buck 1 starts when V_{SUP} > 5.5V (rising), and EN enables Buck 2. Protection features include cycle-by-cycle current limit, Buck 2 overvoltage monitoring and pulldown, and thermal shutdown with automatic recovery. Spread spectrum improves EMI performance.

DC-DC Converter Control Architecture

The step-down converter uses a PWM peak current-mode-control scheme, with a load-line architecture. Peak current-mode control provides several advantages over voltage-mode control, including precise control of the inductor current on a cycle-by-cycle basis, simpler compensation.

The output voltage is positioned slightly positive at no load (still within the tolerance window), to take advantage of the fact that any load disturbance is a load step only. This increases the amount of margin available to the undershoot that occurs on a load step, allowing a reduction in the required output capacitance. As the load increases, a small but controlled amount of load regulation ("load-line") error occurs, so that at heavier loads the voltage is positioned slightly below nominal. This takes advantage of the fact that any load disturbance is load released, increasing the amount of margin available to the overshoot that occurs.

Maximum Duty-Cycle Operation

The Buck 1 converter has a maximum duty cycle of 96% (typ). The IC monitors the off-time (time for which the low-side FET is on) in PWM every switching cycle. Once the minimum off-time is reached, the low-side FET is forced on for 150ns (typ) every 8µs (3.2MHz) and 12µs (2.2MHz). The input voltage at which the devices enter dropout changes depending on the input voltage, output voltage, switching frequency, load current, and the efficiency of the design.

The Input voltage at which the devices enter dropout can be approximated as:

$$V_{SUP} = (V_{OUT1} + (I_{OUT1} \times R_{ON\_HS}))/0.96$$

Note: The equation above does not take into account the efficiency and switching frequency, but is a god first-order approximation. Use the R_{ON_HS} number from the Max column in the *Electrical Characteristics* table.

The Buck 2 converter can operate at 100% duty cycle since the high-side MOSFET is a p-channel.

Linear Regulator Output (BIAS)

The devices include a 5V linear regulator (V_{BIAS}) that provides power to the internal circuit blocks. Connect a 2.2µF ceramic capacitor from BIAS to AGND.

System Enable (EN)

The MAX20019 uses an enable control input (EN) to activate the devices from their low-power shutdown mode. EN is high-voltage compatible and can be connected to SUP. The MAX20020 EN only controls the Buck 2 converter and requires V_{SUP} > 5.5V and V_{OUT1} to have reached regulation before powering up Buck 2 (see the *Startup and Soft-Start* section).

A logic-low at the MAX20019 EN shuts down the device. During shutdown, the internal linear regulator and gate drivers turn off. Shutdown is the lowest power state. Driving the MAX20020 EN pin low while V_{SUP} > 5V only shuts down the OUT2 converter.

Startup and Soft-Start

The ICs feature an internal soft-start timer and delay timer. Figure 1 and Figure 2 show startup timing, delay timing between Buck 1, Buck 2, and EN effect on timing.

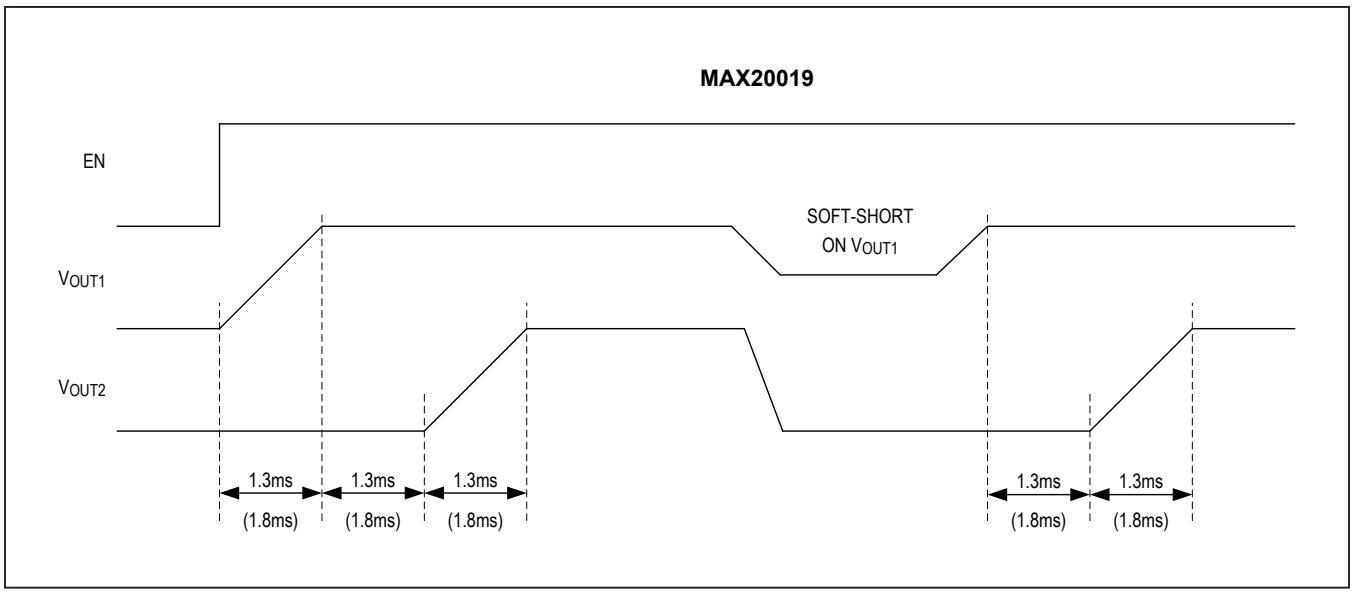


Figure 1. MAX20019 Soft-Start Timing for 3.2MHz (2.2MHz)

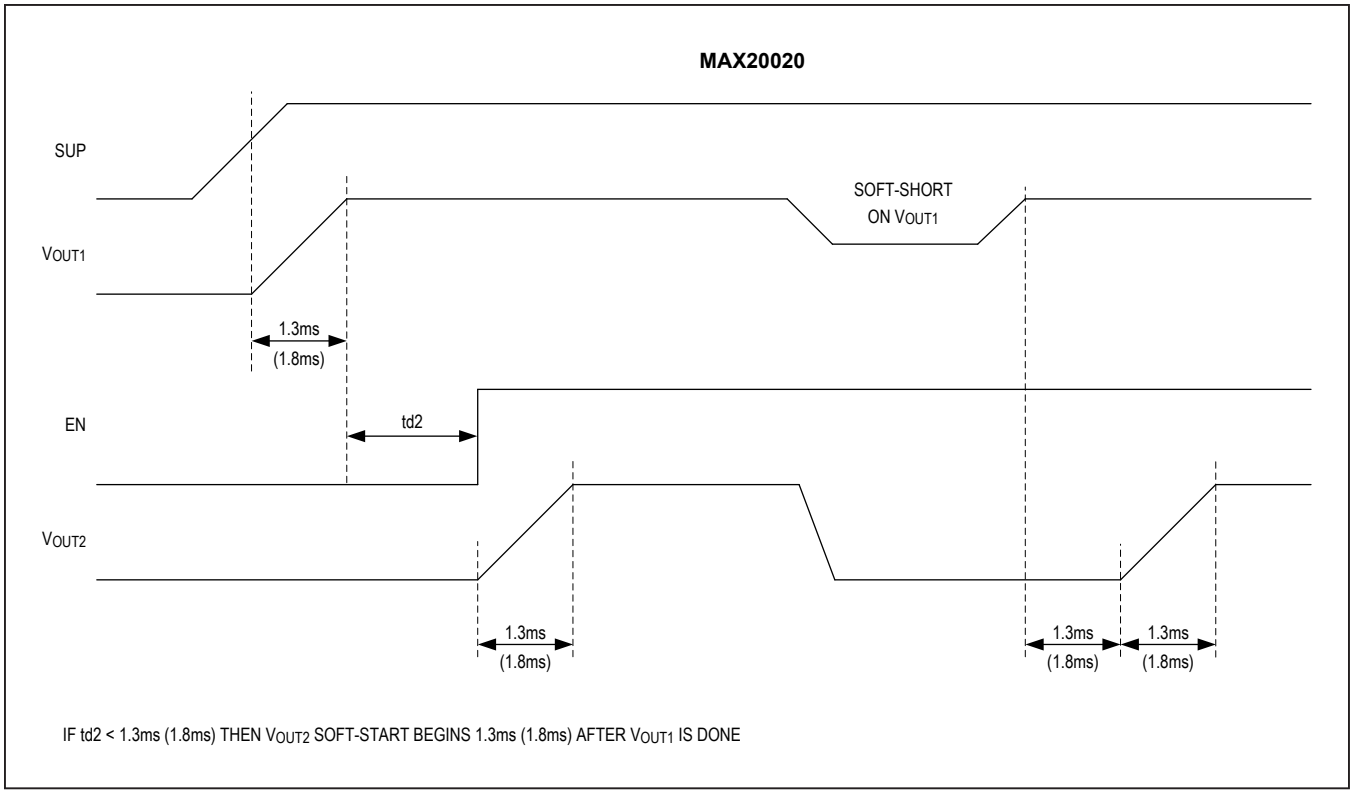


Figure 2. MAX20020 Soft-Start Timing for 3.2MHz (2.2MHz)

Current Limit/ Short-Circuit Condition

The devices have fault protection designed to protect them against abnormal conditions. If either output is shorted, then that respective converter implements a cycle-by-cycle current limit. If V_{OUT1} is below 90% of the factory-preset voltage, V_{OUT2} is disabled. Buck 2 only reenters soft-start if V_{OUT1} recovers above 95%.

The device also has overtemperature protection. If the die temperature exceeds approximately 175°C, the device stops switching until the die temperature drops by approximately 15°C and then resumes operation, going through soft-start once again.

OUT2 Overvoltage Protection

OUT2 is monitored for overvoltage and responds by turning off the high-side and low-side MOSFETs and enabling the 500Ω pulldown resistor on OUT2. The overvoltage rising and falling thresholds are provided in the *Electrical Characteristics* table.

Internal Oscillator

The switching frequency (f_{SW}) is set at the factory to 2.2MHz or 3.2MHz for both converters. The higher 3.2MHZ frequency allows designs with lower inductor values and less output capacitance. Consequently, peak currents and I^2R losses are lower at higher switching frequencies, but core losses, gate-charge currents, and switching losses increase. If typical input voltage is expected over 10V, then values of V_{IN}, V_{OUT}, I_{OUT}, and DCR losses may require the 2.2MHz switching frequency due to minimum on-time constraints.

Applications Information

Output-Voltage Selection

Output voltages are set at the factory. Available options are shown in Table 1.

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DC}). To select inductance value, the ratio of inductor peak-to-peak AC current to DC average current (LIR) must be selected first. A good compromise between size and loss is a 30% peak-to-peak ripple current to average current ratio (LIR = 0.3). The switching frequency, input voltage, output voltage, and selected LIR then determine the inductor value as follows:

$$L1 = ((V_{SUP} - V_{OUT1}) \times V_{OUT1})/(V_{SUP} \times f_{SW} \times (I_{OUT1}+I_{PV2}) \times LIR)$$

and:

$$L2 = ((V_{PV2} - V_{OUT2}) \times V_{OUT2})/(V_{PV2} \times f_{SW} \times I_{OUT2} \times LIR)$$

where V_{SUP}, V_{OUT1}, V_{OUT2}, I_{OUT1}, and I_{OUT2} are typical values (so efficiency is optimum for typical conditions). The switching frequency is set by factory programming (see the *Internal Oscillator* section). Table 1 lists some of the inductor values for 300mA output current and several output voltages.

Table 1. Output-Voltage Selections

OUTPUT	VOLTAGE SELECTIONS (V)			
V_{OUT1}	5*	3.3	3	2.8
V_{OUT2}	3.3*	1.8	1.8	1.8
V_{OUT2}	—	1.5	1.5	1.5
V_{OUT2}	—	1.2	1.2	1.2
V_{OUT2}	—	1.0	1.0	1.0

**Contact factory for availability.*

Table 2. Inductor Values for Typical V_{IN}, V_{OUT}, and I_{OUT} Requirements

V_{SUP}/V_{OUT} (V)	8V (3.3V)	7V (3.3V)	7V (2.8V)	12V (3.3V*)	3.3V (1.8V)	2.8V (1.8V)
Inductor (µH), I_{LOAD} = 300mA	6.8	6.8	6.8	10	2.2	2.2
Inductor (µH), I_{LOAD} = 500mA	4.7	3.3	3.3	8.2	—	—

**f_{SW} = 2.2MHz.*

Input Capacitor

The recommended system input capacitor is 10µF with an X5R rating or better. The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching.

Output Capacitor

The minimum output capacitance should be 22µF ceramic with an X7S or X7R rating. The value and quality of this capacitor is critical, as it sets the dominant pole of the loop.

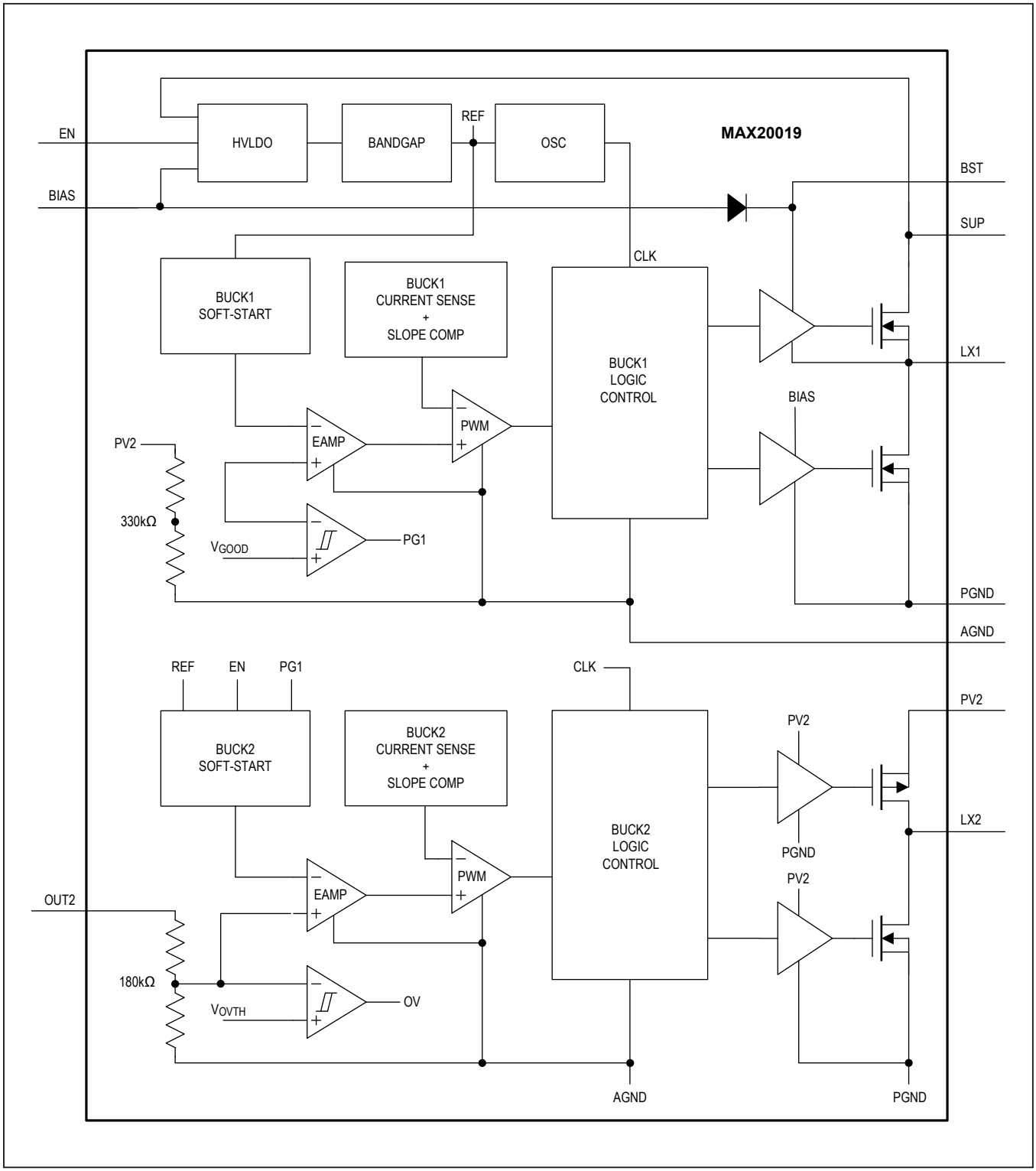
PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. Follow these guidelines for good PCB layout:

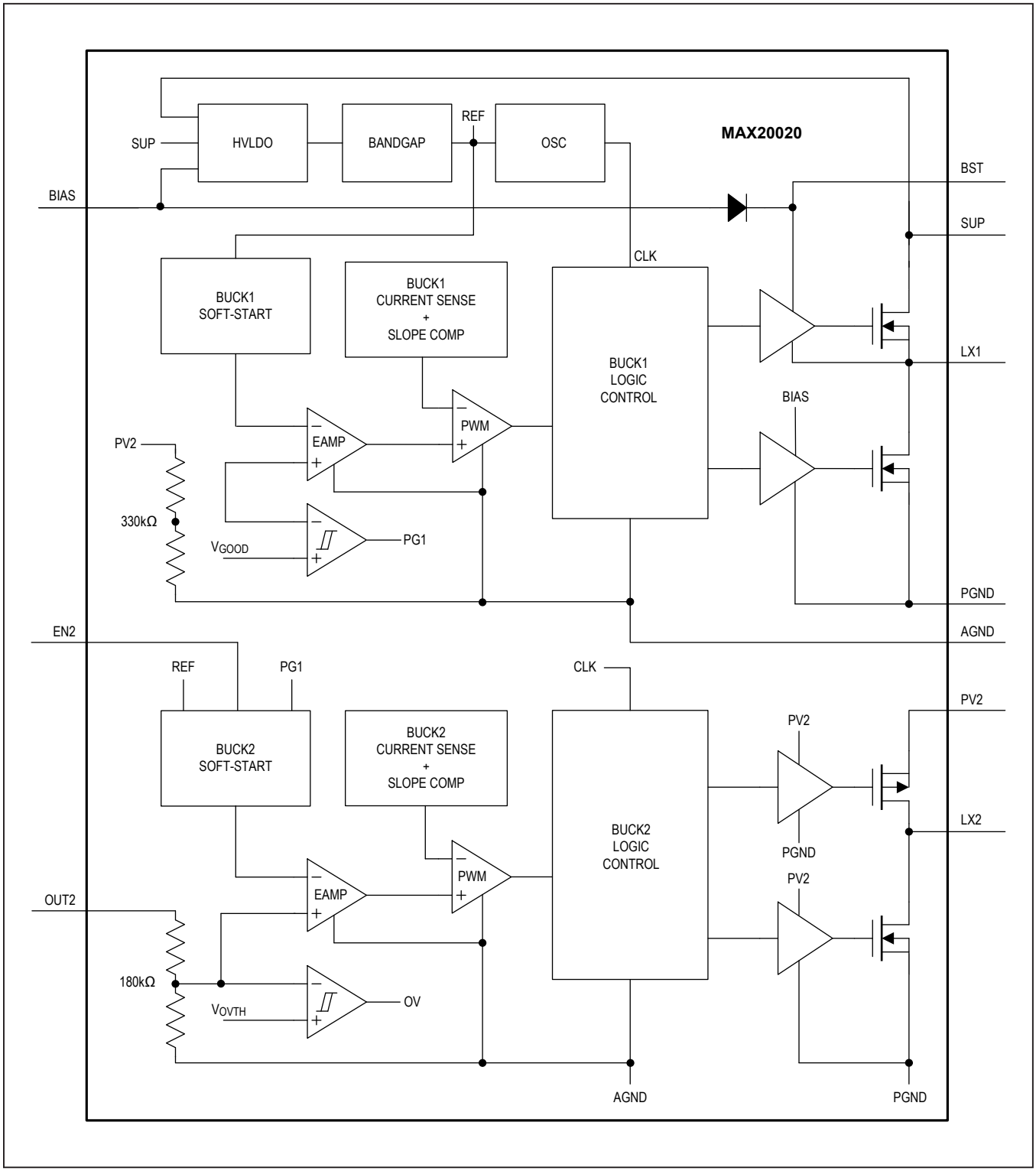
The power and the Buck 1 feedback signal use the same input pin, PV2. It is critical that this trace is short as possible from the output of Buck 1 to the input PV2. The width should be sufficient enough to carry the current for PV2 while not causing enough drop to cause regulation error in Buck 1.

1) Place a 0.1µF ceramic capacitor next to SUP and the IC.
2) Use a large contiguous copper plane under the device package. Ensure that all heat-dissipating components have adequate cooling. The bottom pad of the device must be soldered down to this copper plane for effective heat dissipation and getting the full power out of the device. Use multiple vias or a single large via in this plane for heat dissipation.
3) Isolate the power components and high-current path from the sensitive analog circuitry. This is essential to prevent any noise coupling into the analog signals.
4) Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. The high-current path comprising input capacitor, high-side FET, inductor, and the output capacitor, should be as short as possible.
5) The ground connection for the analog and power section should be close to the IC. This keeps the ground current loops to a minimum. In cases where only one ground is used, adequate isolation between analog return signals and high-power signals must be maintained.
6) Place the BIAS capacitor next to the BIAS pin and connect to AGND with a short and wide trace.

Simplified Typical Operating Circuits



Simplified Typical Operating Circuits (continued)



Ordering Information

PART	SEQUENCING	PIN-PACKAGE	OUT1 (V)	OUT2 (V)	f_{SW} (MHz)	SPREAD SPECTRUM
MAX20019ATBA/V+	Off	10 TDFN-EP*	3.3	1.8	3.2	On
MAX20019ATBA/VY+	Off	10 SWTDFN-EP*	3.3	1.8	3.2	On
MAX20019ATBB/V+	Off	10 TDFN-EP*	2.8	1.8	3.2	On
MAX20019ATBC/V+	Off	10 TDFN-EP*	3.3	1.2	3.2	On
MAX20019ATBD/V+	Off	10 TDFN-EP*	2.8	1.2	3.2	On
MAX20019ATBE/V+**	Off	10 TDFN-EP*	3.3	1.8	3.2	Off
MAX20019ATBF/V+**	Off	10 TDFN-EP*	2.8	1.8	3.2	Off
MAX20019ATBG/V+	Off	10 TDFN-EP*	3.3	1.2	3.2	Off
MAX20019ATBH/V+**	Off	10 TDFN-EP*	2.8	1.2	3.2	Off
MAX20019ATBI/V+	Off	10 TDFN-EP*	3.3	1.0	3.2	On
MAX20019ATBJ/V+	Off	10 TDFN-EP*	3.3	1.8	2.2	On
MAX20020ATBA/V+	On	10 TDFN-EP*	3.3	1.8	3.2	On
MAX20020ATBB/V+	On	10 TDFN-EP*	2.8	1.8	3.2	On
MAX20020ATBC/V+	On	10 TDFN-EP*	3.3	1.2	3.2	On
MAX20020ATBD/V+	On	10 TDFN-EP*	2.8	1.2	3.2	On
MAX20020ATBK/VY+**	On	10 SWTDFN-EP*	3.3	1.82	3.2	On

Note: All devices operate over the -40°C to +125°C automotive temperature range.

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
SW = Side-wettable TDFN package.
*EP = Exposed pad.
**Future product—contact factory for availability.

Contact factory for the following options:

- 2.2MHz or SS = Off
- OUT2: 1.5V or 1V
- OUT1 and OUT2: 5V and 3.3V

Chip Information

PROCESS: CMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/17	Initial release	—
1	9/17	Updated *Ordering Information* and *Package Information* tables	16
2	1/18	Added new row for Voltage Accuracy in *Electrical Characteristics* and added future product variant (MAX20020ATBK/V+) to *Ordering Information* tables	4, 16
3	1/18	Changed MAX20019ATBJ/V+ f_{SW} value in *Ordering Information* table from 3.2MHz to 2.2MHz	16
4	2/18	Removed future product status from MAX20019ATBA/VY+ and added future product status to MAX20020ATBA/V+ in *Ordering Information* table	16
4.1		Added future product status to MAX20019ATBC/V+, MAX20019ATBD/V+, and MAX20019ATBJ/V+ in *Ordering Information* table	16
5	4/18	Updated *Ordering Information* table and removed future product status from MAX20019ATBC/V+, MAX20020ATBB/V+, MAX20020ATBC/V+, MAX20020ATBD/V+, and MAX20020ATBK/VY+. Added future part designation to MAX20020ATBA/V+	16
5.1		Updated *Ordering Information* table and added future part designation to MAX20019ATBC/V+, MAX20020ATBB/V+, MAX20020ATBC/V+, MAX20020ATBD/V+, and MAX20020ATBK/VY+	16
6	6/18	Updated *Ordering Information* table and removed future part designation from MAX20019ATBC/V+, MAX20019ATBD/V+, MAX20020ATBA/V+, MAX20020ATBB/V+, MAX20020ATBC/V+, MAX20020ATBD/V+.	17
7	9/18	Updated *Ordering Information* table and removed future part designation from MAX20019ATBG/V+ and MAX20019ATBJ/V+.	17
8	11/18	Updated *Absolute Maximum Ratings* section and *Package Information* table.	2
9	1/19	Updated *Ordering Information* table to remove future part designation from MAX20019ATBI/V+	17

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