General Description

The MAX20047 is an automotive-grade, low-cost, small-footprint dual-port charger IC designed for automotive charging applications. It combines a fully synchronous 6A step-down buck converter with integrated high-side and low-side FETs capable of operating with input voltages from 3.5V to 36V and delivering 5.2V output voltage. The IC features integrated iPod®/iPhone® 1.0A and iPad® 2.1A dedicated charging modes.

The IC delivers up to 3A of charging current with 93% efficiency per port through integrated switches with programmable current limit and thermal foldback control. The buck converter switching frequency is programmable from 0.4MHz to 2.2MHz. Short-to-ground protection and overcurrent protection are also provided on the protected HVBUS outputs to protect the internal BUS power rail from an overcurrent fault. The MAX20047 offers short-to-battery up to +18V and can also be ordered with spread-spectrum operation to reduce EMI.

Applications

- USB Dedicated Charging Ports (DCP)
- Automotive Cigarette Lighter Adapters
- Power Supply for Linear Chargers

Ordering Information ***appears at end of data sheet.***

Benefits and Features

- Operating V_{IN} Range of 3.5V to 36V
- 40V Load-Dump Protection
- Synchronous DC-DC Converter with Integrated FETs
- 93% Charge Efficiency at 3A Charging
- 0.4MHz to 2.2MHz Programmable Switching Frequency by External Pin Settings
- Spread-Spectrum Operation
- Fixed 8ms Internal Soft-Start
- 5.20V Output
- 99% Duty-Cycle Operation with Low Dropout
- ±2% Output-Voltage Accuracy
- Input System Overvoltage and Short-Circuit Protection
- Accurate SRC_DMOS Current Limiting with Minimal Voltage Drop
  - Low R_{ON} 15mΩ Dual USB Power Switches
  - Adjustable SRC_DMOS Current Limit by External Pin Settings
  - Integrated Current Sensing
- Thermal Regulation and Thermal Shutdown
- Dual Autonomous Battery-Charging Ports with Portable Device Detection
  - Integrated Apple® 2.4A, 2.1A, 1.0A Detection
  - Integrated Samsung® Detection
  - Integrated DCP Detection
- Robust for the Automotive Environment
  - Short-to-Battery and Short-to-Ground Protection on Protected SRC_DMOS Output
  - Short-to-Battery and Short-to-PV Protection on Protected HVDP1, HVDM1, HVDP2, and HVDM2 Inputs
  - Tested to ISO 10605 and IEC 61000-4-2 ESD Standards
  - 20-Pin (5.0mm x 3.5mm) FC2-QFN Package
  - -40°C to +125°C Operating Temperature Range
  - AEC-Q100 Qualified

19-100165; Rev 0; 9/17

maxim integrated™

Absolute Maximum Ratings

SUPSW, HVEN to PGND .....-0.3V to +40V
LX to PGND.....-0.3V to V_{SUPSW} + 0.3V
BIAS to Ground .....-0.3V to +6.0V
COMP to Ground.....-0.3V to V_{BIAS} + 0.3V
G_DMOS to Ground.....-0.3V to +16.0V
AGND to PGND.....-0.3V to +0.3V
PV to PGND .....-03V to +6.0V
OUT to PGND .....-0.3V to V_{PV}
BST to LX.....-0.3V to +6.0V
S_DMOS1, S_DMOS2 to Ground.....-0.3V to V_{PV}
ILIM, CONFIG, FOSC to Ground .....-0.3V to V_{BIAS} + 0.3V
HVDP1, HVDP2, HVPM1, HVDM2 to Ground .....-0.3V to +18V
LX Continuous Current.....8A
Continuous Power Dissipation (T_A = +70°C)
(Single-Layer Board
derate 13.2mW/°C over +70°C) 1052.6mW
Operating Temperature Range..... -40°C to +125°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range.....-60°C to+150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

FC2-QFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....36°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....2°C/W

Note 1: Thermal resistance can be lowered with improved board design.
Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 FC2-QFN	F203A5F+1	21-100124	90-100045

Electrical Characteristics

(T_A = -40ºC to +125ºC. Typical values are at V_{SUPSW} = +14V and T_A = +25ºC, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{SUP}		3.5		36	V
Load-Dump-Event Supply Voltage	V_{SUP_LD}	t_{LD} < 1_s			40	V
Shutdown Supply Current	I_{SHDN}	V_{SUPSW} = 14V; HVEN = 0V, off state		6	15	µA
BIAS Regulator Voltage (Nominal)	V_{BIAS}	V_{SUPSW} = 14V, I_{BIAS} < 10mA, BIAS not switched over to V_{OUT}	4.7	4.96	5.45	V
BIAS Undervoltage Lockout (Rising)	$V_{UV\_BIAS\_R}$	V_{BIAS} rising	2.7	3	3.3	V
BIAS Undervoltage Lockout (Falling)	$V_{UV\_BIAS\_F}$			2.5		V
BIAS Current Limit	I_{BIAS}		50			mA

Electrical Characteristics (continued)

(T_A = -40ºC to +125ºC. Typical values are at V_{SUPSW} = +14V and T_A = +25ºC, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal-Shutdown Temperature	T_{SHDN}	T_J rising		165		°C
Thermal-Shutdown Hysteresis	T_{SHDN_HYS}			15		°C
Thermal-Foldback Temperature	T_{FLDBK}	T_J rising		140		°C
Thermal-Foldback Hysteresis	T_{FLDBK_HYS}			15		°C
STEP-DOWN DC-DC						
PWM-Mode Output Voltage	V_{OUT}		5.05	5.2		V
Load Regulation	V_{LOAD_REG}	30mA < I_{LOAD} < IMAX		0.5		%
Line Regulation	V_{LINE_REG}	6V < V_{SUPSW} < 36V		0.02		%/V
BST Input Current	I_{BST_ON}	High-side MOSFET on, V_{BST} - V_{LX} = 5V		1.5		mA
	I_{BST_OFF}	High-side MOSFET off, V_{BST} - V_{LX} = 5V		1.5		µA
LX Current Limit	I_{LX}		7.5	10	13	A
Spread-Spectrum Frequency	f_{SS}	Ordering option		±3		%
High-Side Switch On-Resistance	$R_{DS(ON)\_HS}$	V_{BIAS} = 5V, I_{LX} = 0.5A		35	76	mΩ
High-Side Switch Leakage	I_{LEAK_HS}	High-side MOSFET off, V_{SUPSW} = 36V, V_{LX} = 36V, T_A = +25°C		1	5	µA
Low-Side Switch On-Resistance	$R_{DS(ON)\_LS}$	V_{BIAS} = 5V, I_{LX} = 0.5A		18	35	mΩ
Low-Side Switch Leakage	I_{LEAK_LS}	Low-side MOSFET off, V_{SUPSW} = 36V, V_{LX} = 36V, T_A = +25°C		1	5	µA
Minimum On-Time	t_{ON_MIN}			65	100	ns
Maximum Duty Cycle	DC_{MAX}		95	98	99	%
Oscillator Frequency	f_{OSC}	R_{FOSC} = 73.2kΩ	363	400	437	kHz
		R_{FOSC} = 12.7kΩ		2.2		MHz
Soft-Start Time	t_{SS}		4	8	12	ms
HVEN PIN						
HVEN High Threshold	V_{HVEN_HI}		2.4			V
HVEN Low Threshold	V_{HVEN_LO}				0.6	V
HVEN Hysteresis	V_{HVEN_HYS}			0.2		V
HVEN Leakage Current	I_{HVEN}	T_A = +25°C		1	10	µA

Electrical Characteristics (continued)

(T_A = -40ºC to +125ºC. Typical values are at V_{SUPSW} = +14V and T_A = +25ºC, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
G_DMOS PIN (CHARGE PUMP)						
Unloaded Output Voltage	V_{OCHP}	Referenced to PV, internal discharge path 2MΩ to ground	7	9	11	V
Output Impedance	R_{OCHP}			50	75	kΩ
Output DC Current	I_{OCHP}	V_{G_DMOS} - PV > 8V (min), 10V (typ)		20		µA
HVDM_/HVDP_ DCP PINS						
HVDP_/HVDM_ Short Pulldown	R_{PD}		300	500	750	kΩ
HVDP_/HVDM_ Off-Leakage	I_{HVD_OFF}	HVDP_/HVDM_ = 18V, HVEN = 9V			50	µA
HVDP_/HVDM_ Overvoltage-Protection-Trip Threshold	V_{OV_DAT}			3.85	3.99	V
HVDM_/HVDP_ Overvoltage-Protection-Response Time	t_{OV_DAT}	HVDP_/HVDM_ OV rising		1.0	2.5	µs
SRC_DMOS1/SRC_DMOS2 USB POWER SWITCHES						
SRC_DMOS_ Protection Overvoltage	V_{OV_USB}	SRC_DMOS_ rising	5.5	5.8		V
SRC_DMOS_ Protection-Response Time	t_{OV_USB}			200		ns
SRC_DMOS_ Relative Protection-Trip Threshold	V_{OV_REL}	SRC_DMOS_ rising		V_{PV} + 0.300		V
SRC_DMOS_ Relative Protection-Response Time	t_{OV_REL}			500		ns
SRC_DMOS_ Undervoltage-Protection Trip Absolute	V_{UV_USB}	If ILIM < UV_USB, turn off; if ILIM > UV_USB, stay on	4.3	4.45	4.6	V
SRC_DMOS_ Undervoltage-Protection-Response Time	t_{UV_USB}	SRC_DMOS rising OV_REL, OV_USB (750ns typ rising)		300		ns
PV Undervoltage Protection	V_{UV_PV}	PV falling from 5V with slew rate of 0.5V/µs, switch turned off (with R_L= 50Ω on; SRC_DMOS measured when SRC_DMOS goes low)	3.65	3.85	4	V

Electrical Characteristics (continued)

(T_A = -40ºC to +125ºC. Typical values are at V_{SUPSW} = +14V and T_A = +25ºC, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VBUS Undervoltage-Protection-Response Time	t_{UV_PV}	PV falling from 5V with slew rate of 0.5V/µs, switch turned off (with R_L = 50Ω on, SRC_DMOS_ measured when SRC_DMOS_ goes low)		300		ns
USB FET On-Resistance	$R_{DS(ON)\_FET}$			15		mΩ
Forward-Current Limit	I_{LIM}	R_{ISET} = 68.1kΩ	1.8	2.1		A
		R_{ISET} = 49.9kΩ	2.1	2.41		
		R_{ISET} = 24.9kΩ	2.5	2.75		
		R_{ISET} = 15.8kΩ	3	3.3		
ILIM-Fault Discharge FET	$I_{LIM\_DIS\_FET}$			250		Ω
Continuous-Current-Limit Blanking-Timeout Period	t_{ILIM_BLANK}			2		ms
SRC_DMOS_ Output Rise Time	t_{DMOS_RISE}	From 10% to 90% of V_{OUT}, 2s after HVEN = high		0.4		ms
SRC_DMOS_ Output Fall Time	t_{DMOS_FALL}	From 90% to 10% of V_{OUT}		1.2		ms
SRC_DMOS_ OUT Autoreset Current	I_{RETRY}	In latched-off state, SRC_DMOS_ = 0V, diagnostic current		25		mA
SRC_DMOS_ OUT Autoreset Threshold	V_{RETRY}	In latched-off state, SRC_DMOS_ rising		0.5		V
SRC_DMOS_ Off-Leakage Current	I_{DMOS_LEAK}	V_{PV} = 5.5V, $V_{SRC\_DMOS\_}$ = 0V, T_A = +25°C		1		µA
CONFIG/ILIM RESISTORS CONVERTER						
Current Leakage	I_{LEAK}	0 to 5V	-1		+1	µA
TIMERS						
Low-Frequency Oscillator	f_{LFOSC}			110		kHz
High-Frequency Oscillator	f_{HFOSC}			8		MHz
DSCHG Timer	t_{DSCHG}			2		s
Hold Timer	t_{HOLD}	Referred to the LFOSC (CONFIG HOLD Time = 30 min)		30		min
		Referred to the LFOSC (CONFIG HOLD Time = 60 min)		60		

Electrical Characteristics (continued)

(T_A = -40ºC to +125ºC. Typical values are at V_{SUPSW} = +14V and T_A = +25ºC, unless otherwise noted.) (Note 3)

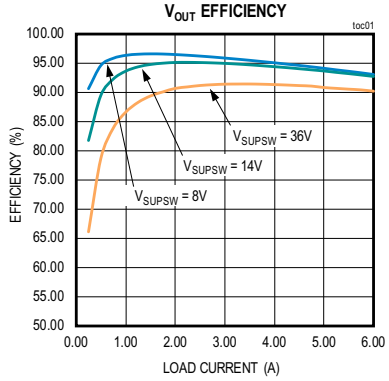
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal-Foldback USBSW Open Timer	t_{THM_USBSW}	Referred to the LFOSC		2		s
Fault Blank, Thermal-Foldback Debounce Time	$t_{BLANK\_THM\_FLDBK}$	Referred to the LFOSC		20		ms
Fault Blank, Thermal-Shutdown Debounce Time	$t_{BLANK\_THM\_SHD}$	Referred to the LFOSC		1		ms
Fault Blank, Overcurrent/ Undervoltage Debounce Timer	t_{BLANK}	Referred to the LFOSC		2		ms
Fault-Retry Timer	t_{RETRY}	Referred to the LFOSC		2		s
ESD						
ESD Protection Level	V_{ESD}	Human Body Model		±2		kV
		ISO 10605 Air Gap		±25		
		IEC 61000-4-2 Air Gap Discharge 330pF, 330Ω, device powered		±15		
		IEC 61000-4-2 Contact Discharge 330pF, 330Ω, device powered		±8		
		ISO 10605 (US OEMs) Air Gap Discharge 330pF, 2kΩ, device powered		±15		
		ISO 10605 (US OEMs) Contact Discharge 330pF, 2kΩ, device powered		±8		

Note 3: Specifications with minimum and maximum limits are 100% production tested at T_A = +25°C and are guaranteed over the operating temperature range by design and characterization. Actual typical values may vary and are not guaranteed.

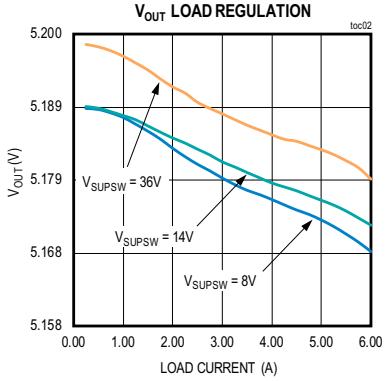
Typical Operating Characteristics

(TA = +25°C)

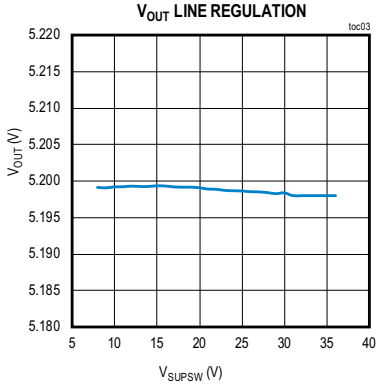
V_{OUT} EFFICIENCY



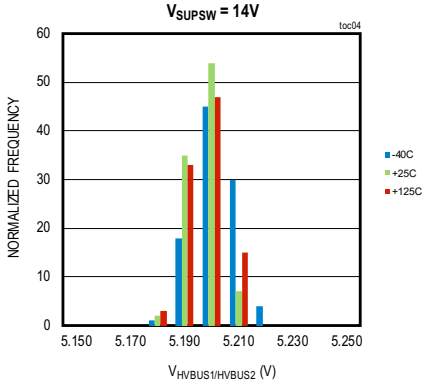
V_{OUT} LOAD REGULATION



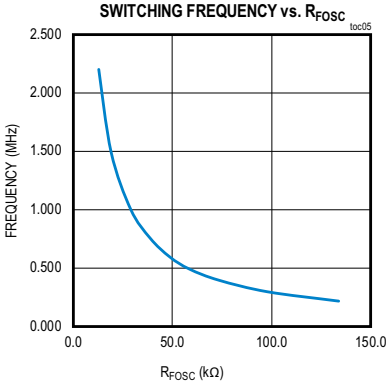
V_{OUT} LINE REGULATION



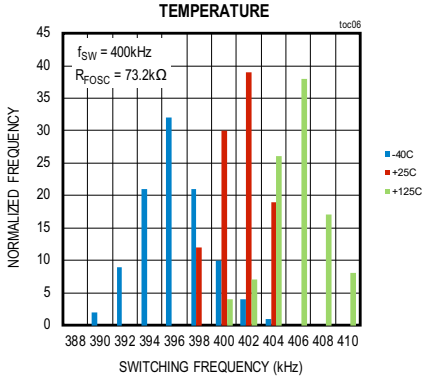
NO LOAD OUTPUT VOLTAGE
V_{SUPSW} = 14V



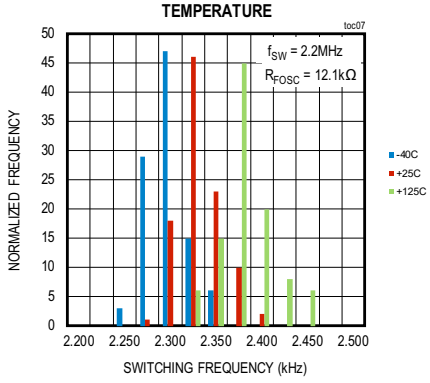
SWITCHING FREQUENCY vs. R_{FOSC}



SWITCHING FREQUENCY vs. TEMPERATURE



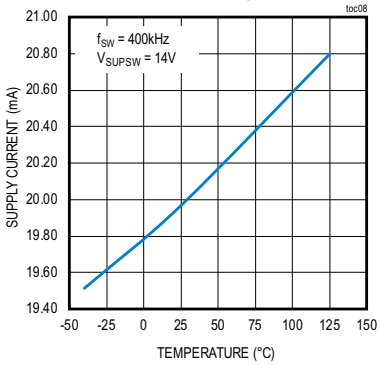
SWITCHING FREQUENCY vs. TEMPERATURE



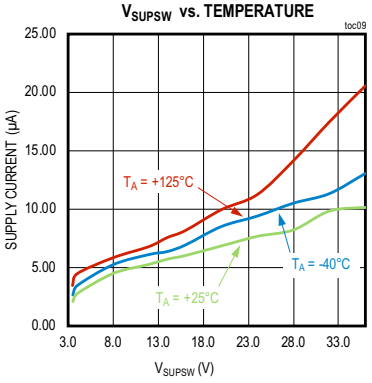
Typical Operating Characteristics (continued)

(TA = +25°C)

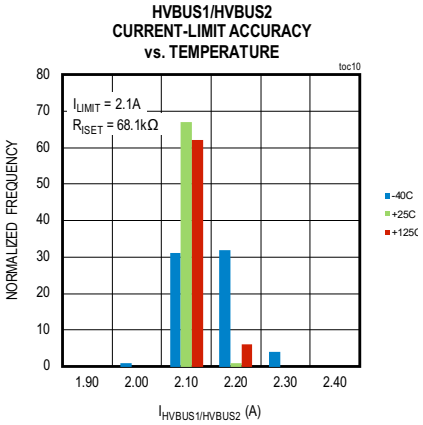
OPERATING SUPPLY CURRENT vs. TEMPERATURE



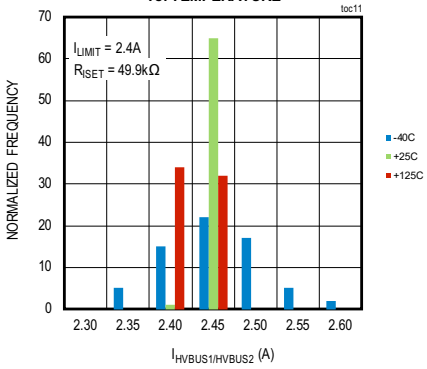
SHUTDOWN SUPPLY CURRENT vs. V_{SUPSW} vs. TEMPERATURE



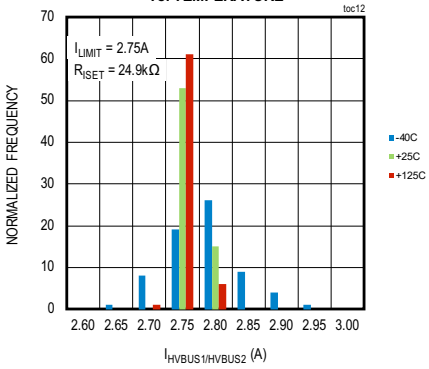
HVBUS1/HVBUS2 CURRENT-LIMIT ACCURACY vs. TEMPERATURE



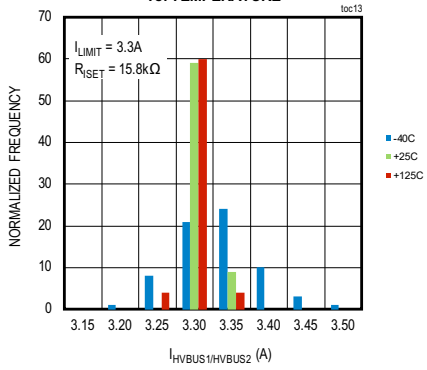
HVBUS1/HVBUS2 CURRENT-LIMIT ACCURACY vs. TEMPERATURE



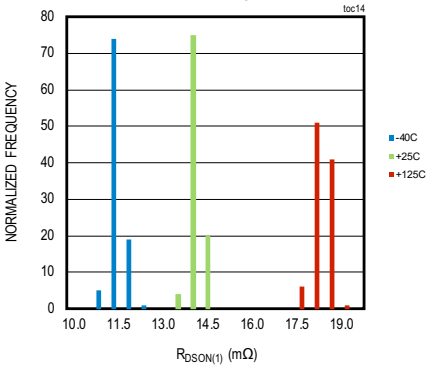
HVBUS1/HVBUS2 CURRENT-LIMIT ACCURACY vs. TEMPERATURE



HVBUS1/HVBUS2 CURRENT-LIMIT ACCURACY vs. TEMPERATURE



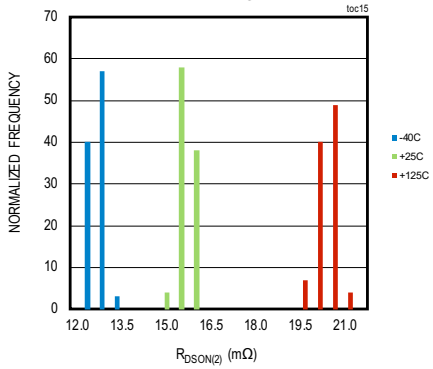
USB1 FET ON-RESISTANCE vs. TEMPERATURE



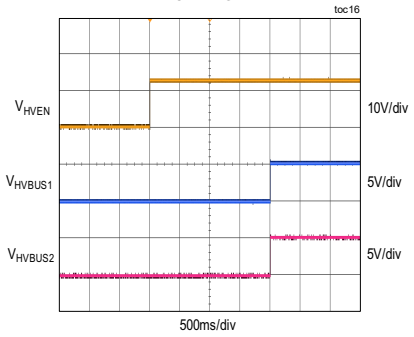
Typical Operating Characteristics (continued)

(TA = +25°C)

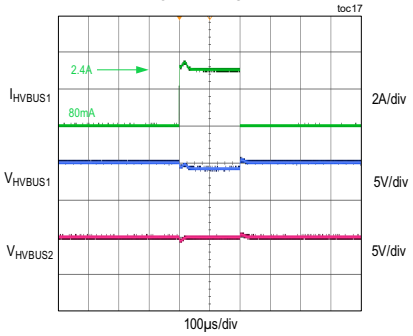
USB2 FET ON-RESISTANCE vs. TEMPERATURE



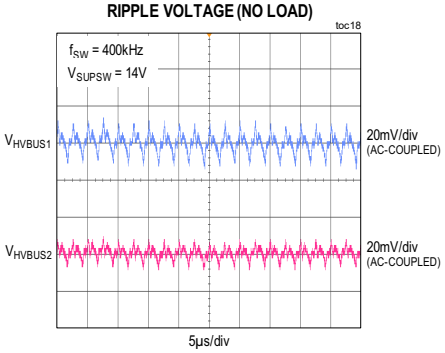
HVBUS1/HVBUS2 STARTUP



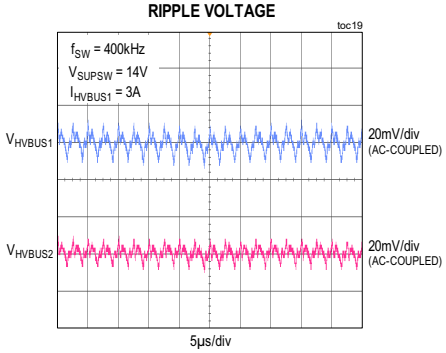
HVBUS1/HVBUS2 LOAD TRANSIENT



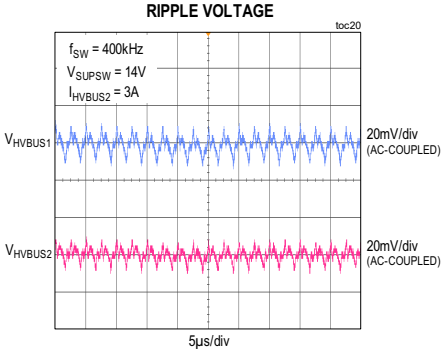
HVBUS1/HVBUS2 RIPPLE VOLTAGE (NO LOAD)



HVBUS1 RIPPLE VOLTAGE



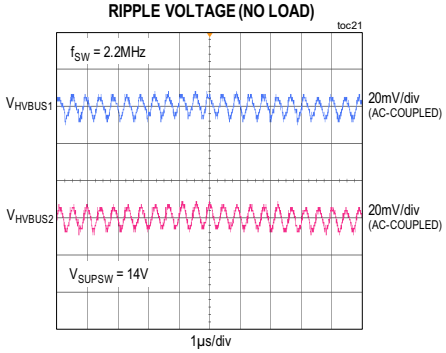
HVBUS2 RIPPLE VOLTAGE



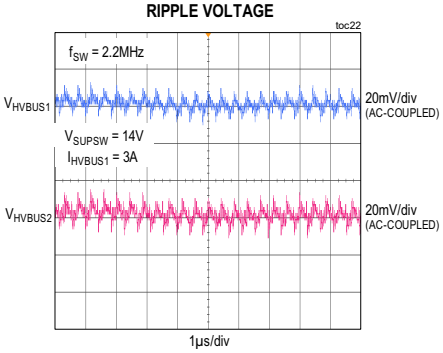
Typical Operating Characteristics (continued)

(TA = +25°C)

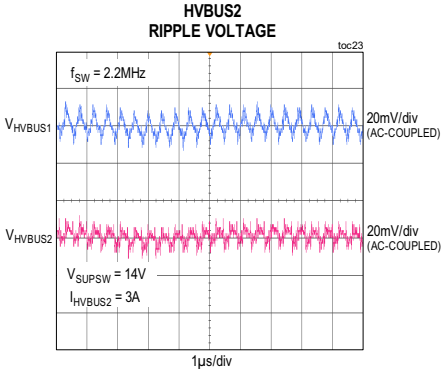
HVBUS1/HVBUS2
RIPPLE VOLTAGE (NO LOAD)



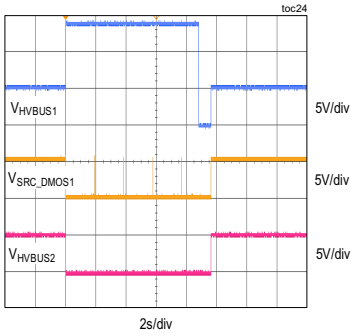
HVBUS1
RIPPLE VOLTAGE



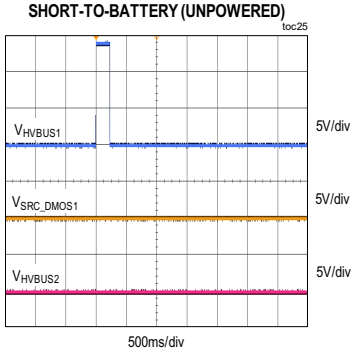
HVBUS2
RIPPLE VOLTAGE



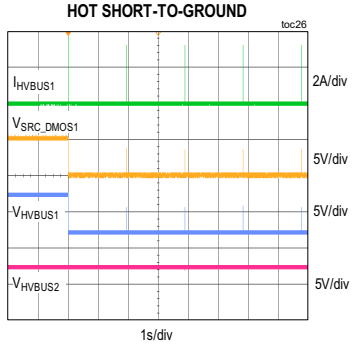
HVBUS1
SHORT-TO-BATTERY



HVBUS1/HVBUS2
SHORT-TO-BATTERY (UNPOWERED)



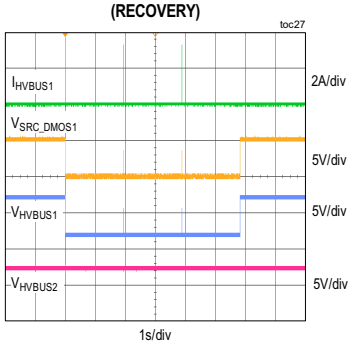
HVBUS1
HOT SHORT-TO-GROUND



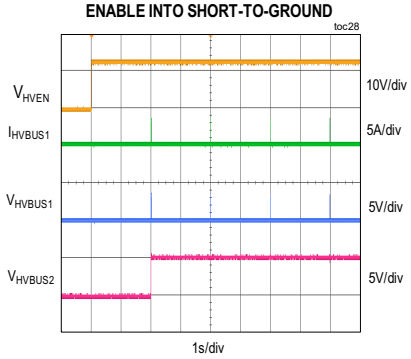
Typical Operating Characteristics (continued)

(TA = +25°C)

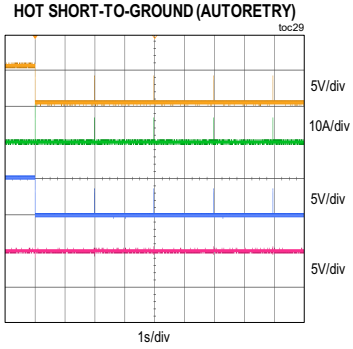
HVBUS1
HOT SHORT-TO-GROUND
(RECOVERY)



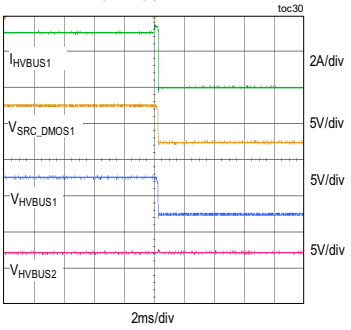
HVBUS1/HVBUS2
ENABLE INTO SHORT-TO-GROUND



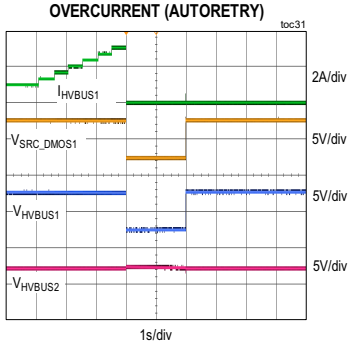
HVBUS1/HVBUS2
HOT SHORT-TO-GROUND (AUTORETRY)



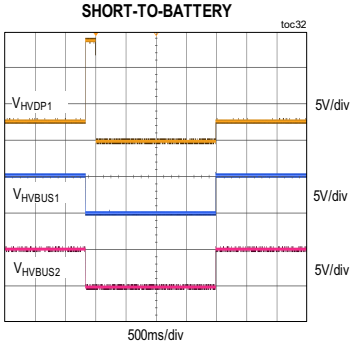
HVBUS1/HVBUS2
OVERCURRENT



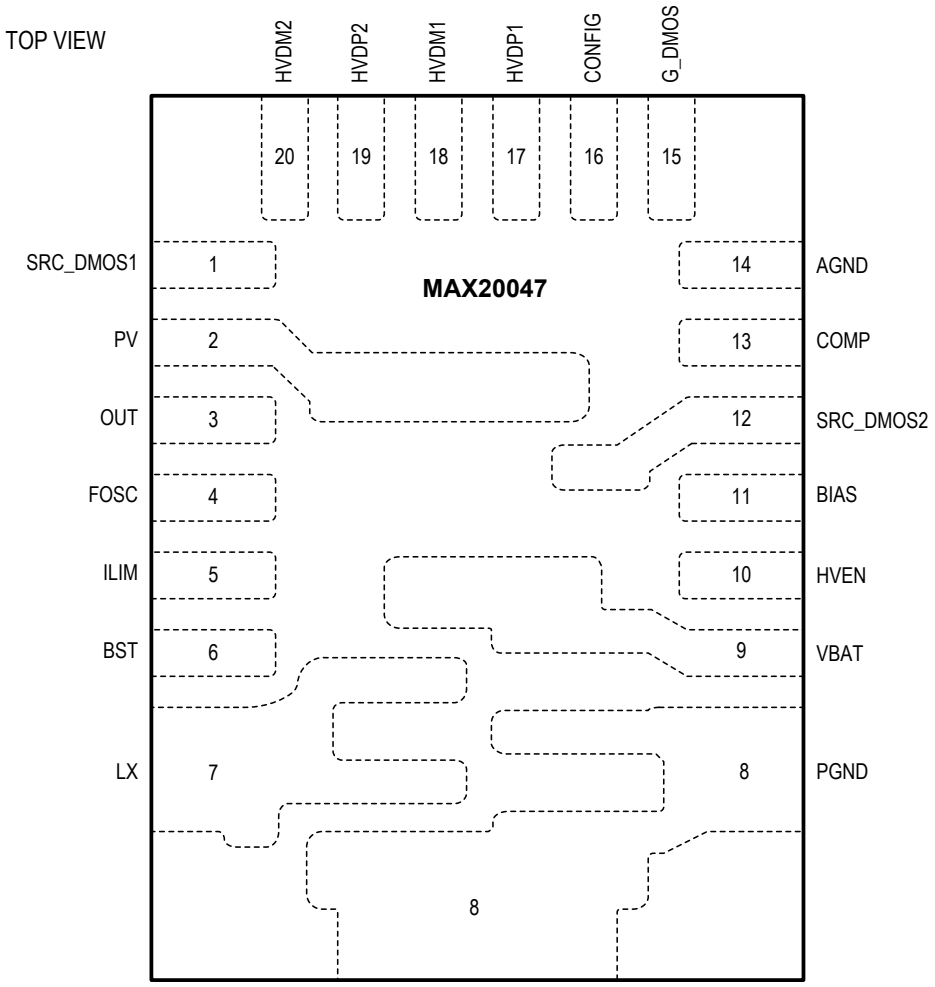
HVBUS1/HVBUS2
OVERCURRENT (AUTORETRY)



HVDP_/HVDM_
SHORT-TO-BATTERY



Pin Configuration

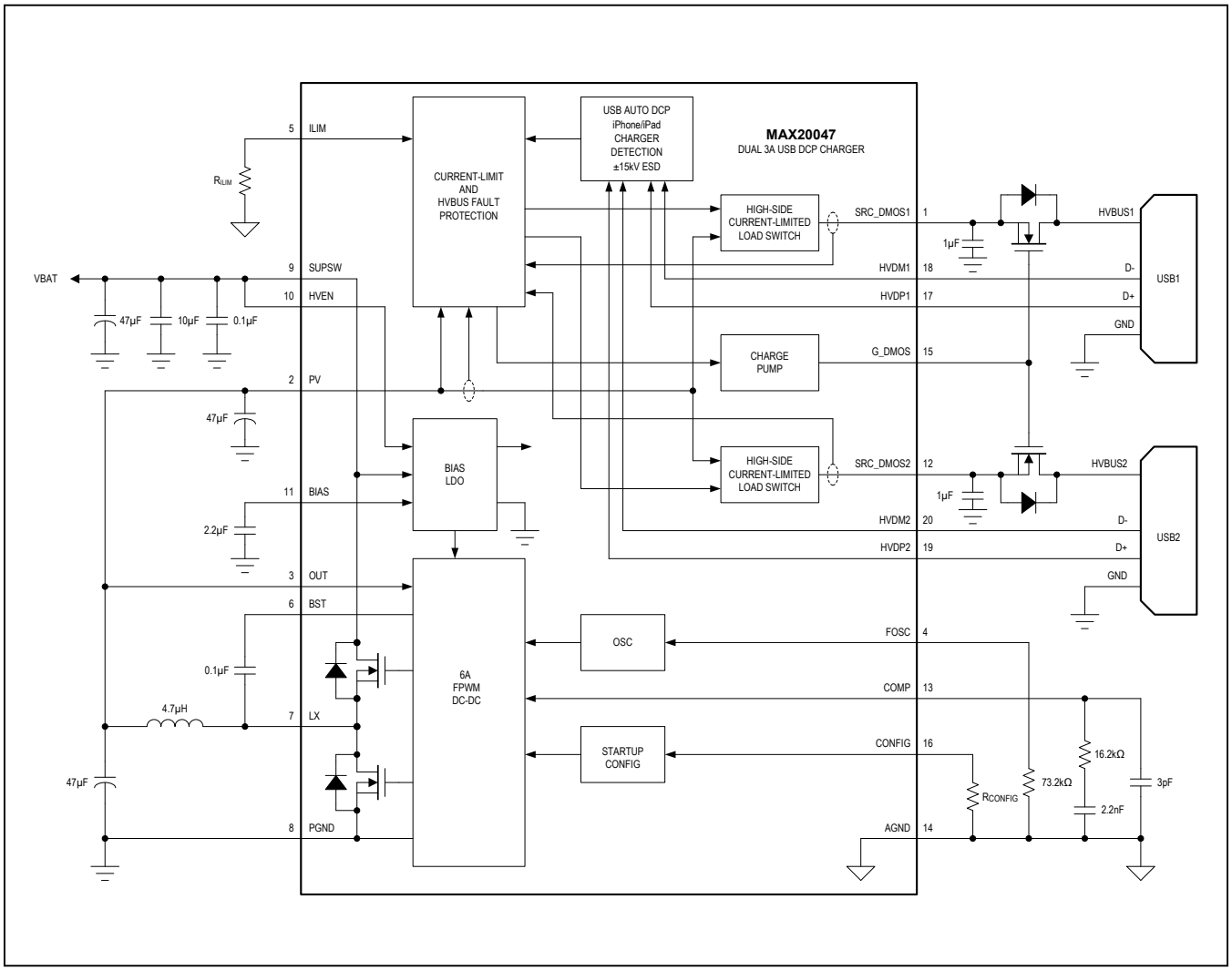


PGND
FC2-QFN
(5.0mm x 3.5mm)

Pin Description

PIN	NAME	FUNCTION
1	SRC_DMOS1	External DMOS Source Input. Connect to the source of the external n-channel DMOS device. Connect a 1µF ceramic capacitor between the SRC_DMOS2 pin and ground.
2	PV	SRC_DMOS1 and SRC_DMOS2 High-Side Current-Limited Switching-Supply Input. Connect PV to the DC-DC converter output (e.g., OUT). Connect a 47µF capacitor between PV and ground.
3	OUT	Synchronous Buck Feedback Voltage-Sense Input. Connect OUT to the output of the DC-DC converter.
4	FOSC	Synchronous Buck Switching-Frequency Setting. Connect a resistor between FOSC and ground to set the switching frequency.
5	ILIM	Synchronous Switching Power-MOSFET Forward-Current-Limit Set Point. Connect a resistor between ILIM and ground to set the current limit.
6	BST	Bootstrap Capacitor for the High-Side Power-MOSFET Driver. Connect a 0.1µF capacitor between BST and LX.
7	LX	Synchronous Buck Converter Output. Connect to the switched-side of the power inductor.
8	PGND	Power Ground. Ground return for the internal low-side power MOSFET.
9	SUPSW	Bias Supply Input and Internal High-Side Switch Supply. Connect a 47µF ceramic capacitor at the board edge. Connect a 10µF capacitor between SUPSW and PGND, as close as possible to the device.
10	HVEN	Active-High Enable Input for the Device (BIAS, DC-DC). HVEN is high-voltage compatible. Drive HVEN high to initiate the startup sequence and enable normal operation.
11	BIAS	5V Bias LDO Output. Connect a 2.2µF ceramic capacitor between BIAS and ground, as close as possible to the pin.
12	SRC_DMOS2	External DMOS Source Input. Connect to the source of the external n-channel DMOS device. Connect a 1µF ceramic capacitor between the SRC_DMOS2 pin and ground.
13	COMP	Error-Amplifier Output. Connect an RC network from COMP to ground for stable operation. See the *Compensation Network* section more details.
14	AGND	Analog Ground Return
15	G_DMOS	DMOS Gate-Drive Output. Connect to the gates of the external n-channel DMOS devices.
16	CONFIG	Sets the Hold Startup Configuration. Connect a resistor to ground for target operation (see Table 4)
17	HVDP1	Protected USB1 D+ Connection. Connect HVDP1 to the D+ pin on the USB1 connector.
18	HVDM1	Protected USB1 D- Connection. Connect HVDM1 to the D- pin on the USB1 connector.
19	HVDP2	Protected USB2 D+ Connection. Connect HVDP2 to the D+ pin on the USB2 connector.
20	HVDM2	Protected USB2 D- Connection. Connect HVDM2 to the D- pin on the USB2 connector.

Functional Diagram



Detailed Description

DC-DC Converter

The MAX20047 IC incorporates a 6A, current-mode, synchronous step-down converter as the charge source for its two 3A USB DCP ports. The DC-DC converter output voltage is 5.2V fixed, and regulates using FPWM. The IC can accept a 3.5V to 36V input voltage range. The wide input voltage range, along with its ability to operate at 99% duty cycle during undervoltage transients, makes the MAX20047 ideal for automotive applications.

Soft-Start

The soft-start feature reduces inrush current when the DC-DC converter starts up. When the DC-DC converter is enabled, the soft-start function gradually ramps the output voltage from 0 to 5.2V in approximately 8ms.

Programmable Oscillator with Spread-Spectrum Option

The DC-DC converter switching frequency is resistor programmable from 400kHz to 2.2MHz. The IC can also be ordered with spread-spectrum operation enabled (see the *Ordering Information* table for details. With spread spectrum enabled, EMI performance is improved as the internal oscillator frequency is modulated up/down ±3% relative to the selected operating frequency.

System Enable (HVEN)

The HVEN pin activates the device from the low-power shutdown mode. HVEN is compatible with inputs from automotive battery level down to 3.5V. HVEN turns on the internal regulator. Once V_{BIAS} is above the internal lockout threshold V_{UVBIAS} = 3V (typ), the converter activates and the output voltage ramps up with the programmed soft-start time.

A logic-low at HVEN shuts down the device. During shutdown, the internal linear regulator and gate drivers turn off. Shutdown is the lowest power state and reduces the quiescent current to 6µA (typ). Drive HVEN high to bring the device out of shutdown.

Maximum Duty-Cycle Operation

The device has a maximum 98% (typ) duty cycle. The IC monitors the on-time (time for which the high-side FET is on) in PWM mode every switching cycle. Once the on-time is detected continuously for 10µs, the low-side FET is forced on for 150ns (typ) every 10µs. The input voltage at which the device enters dropout changes depending on the input voltage, output voltage, switching frequency, load current, and the efficiency of the design.

The input voltage at which the device enters dropout can be approximated as shown in following equation:

$$V_{SUP} = \frac{V_{OUT} + (I_{OUT} \times R_{(ON)\_H})}{0.98}$$

Note: Equation 1 does not take into account the efficiency and switching frequency, but is a good first-order approximation. Use the $R_{DS(ON)\_HS}$ number from the max column in the *Electrical Characteristics* table.

Current-Limit Control

Upon exceeding the DC-DC converter current-limit threshold of 10A, the high-side FET is turned off and is held of until the current goes below the valley current threshold of 11A to prevent current runaway when OUT is at a very low value (this is set high intentionally). If OUT is above 2.5V when this occurs, the high-side FET is allowed to turn on again at the next clock cycle. If the current-limit threshold is reached and OUT is below 2.5V, the converter resets for 16ms and initiates a new soft-start cycle. If OUT is greater than 2.5V at the end of soft-start, it goes into normal operation. If OUT is below 2.5V, it resets for 16ms and initiates a new soft-start cycle again. This pattern repeats until OUT is greater than 2.5V at the end of soft-start.

Overtemperature Protection/Thermal Shutdown

Thermal-overload protection limits the total power dissipation, which could be destructive, so when the junction temperature exceeds 165°C, an internal thermal sensor shuts down the step-down converter, allowing the IC to cool. The thermal sensor turns the IC on again once the junction temperature cools by 15°C.

USB VBUS Fault Protection

The IC provides robust protection and fault recovery for the USB HVBUS1 and HVBUS2 pins. The device has an on-chip charge pump to provide the proper gate drive to control an external n-channel MOSFET, which functions as a load switch for the HVBUS output. Figure 1 shows the VBUS protection circuitry for one of the IC's two charger channels. The protection circuitry is duplicated for the other charger channel, permitting independent protection and fault recovery.

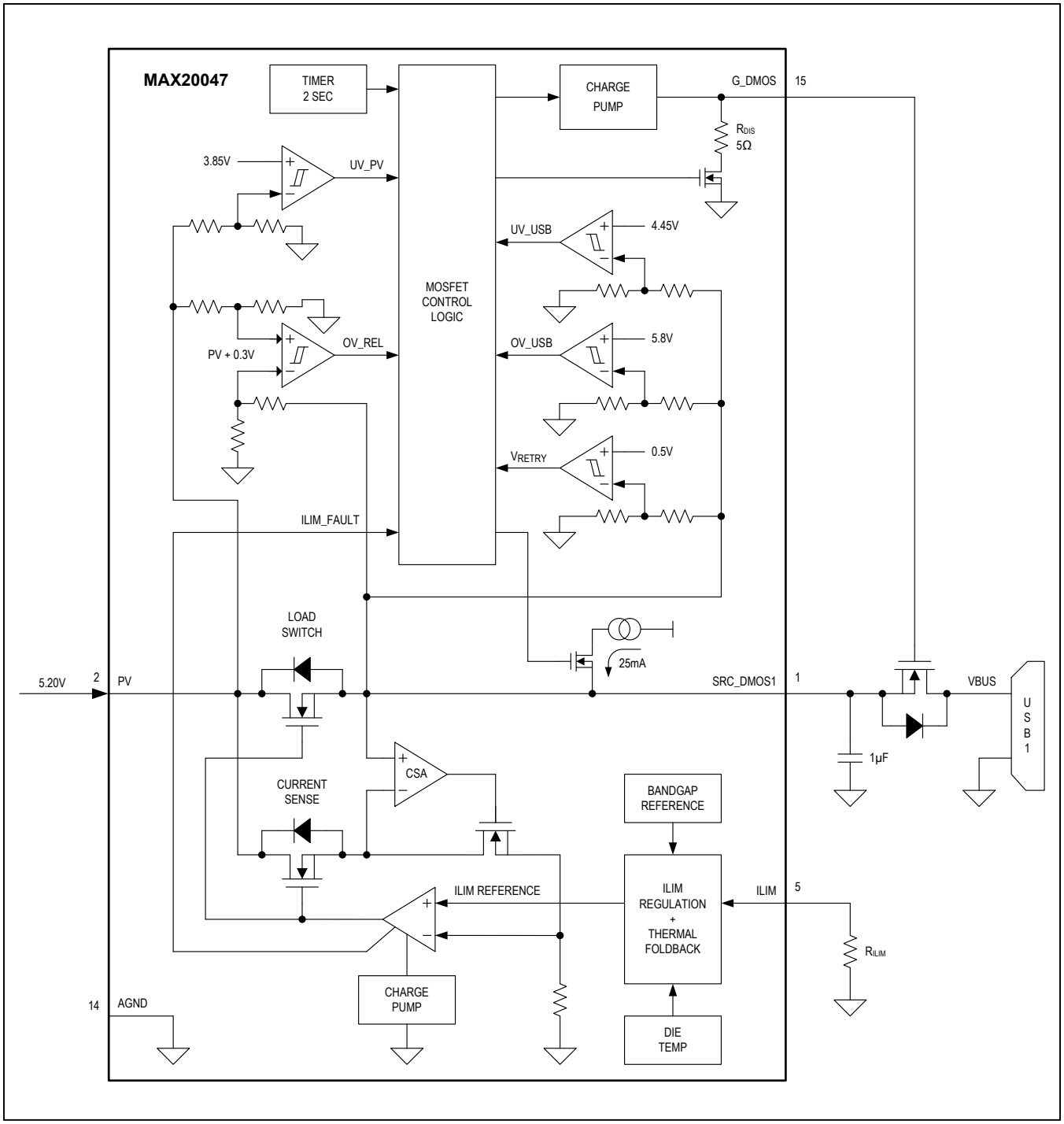


Figure 1. USB Fault Protection (HVBUS1)

VBUS Short-to-Battery Protection

The OV_USB threshold for both VBUS channels is continually monitored, and if the voltage on either VBUS channel exceeds 5.8V, the G_DMOS pin is immediately driven low, disabling the external DMOS MOSFETs. To ensure that the external MOSFETs are instantaneously turned off, an internal 5Ω discharge FET is also enabled, bleeding off any remaining gate charge. After 2s, the G_DMOS pin is driven high, enabling the external MOSFETs, with the OV_USB threshold again tested. If the OV_USB threshold is no longer tripped, power to both VBUS channels is restored; otherwise, the IC retries every 2s while the fault persists. Figure 2 illustrates the process.

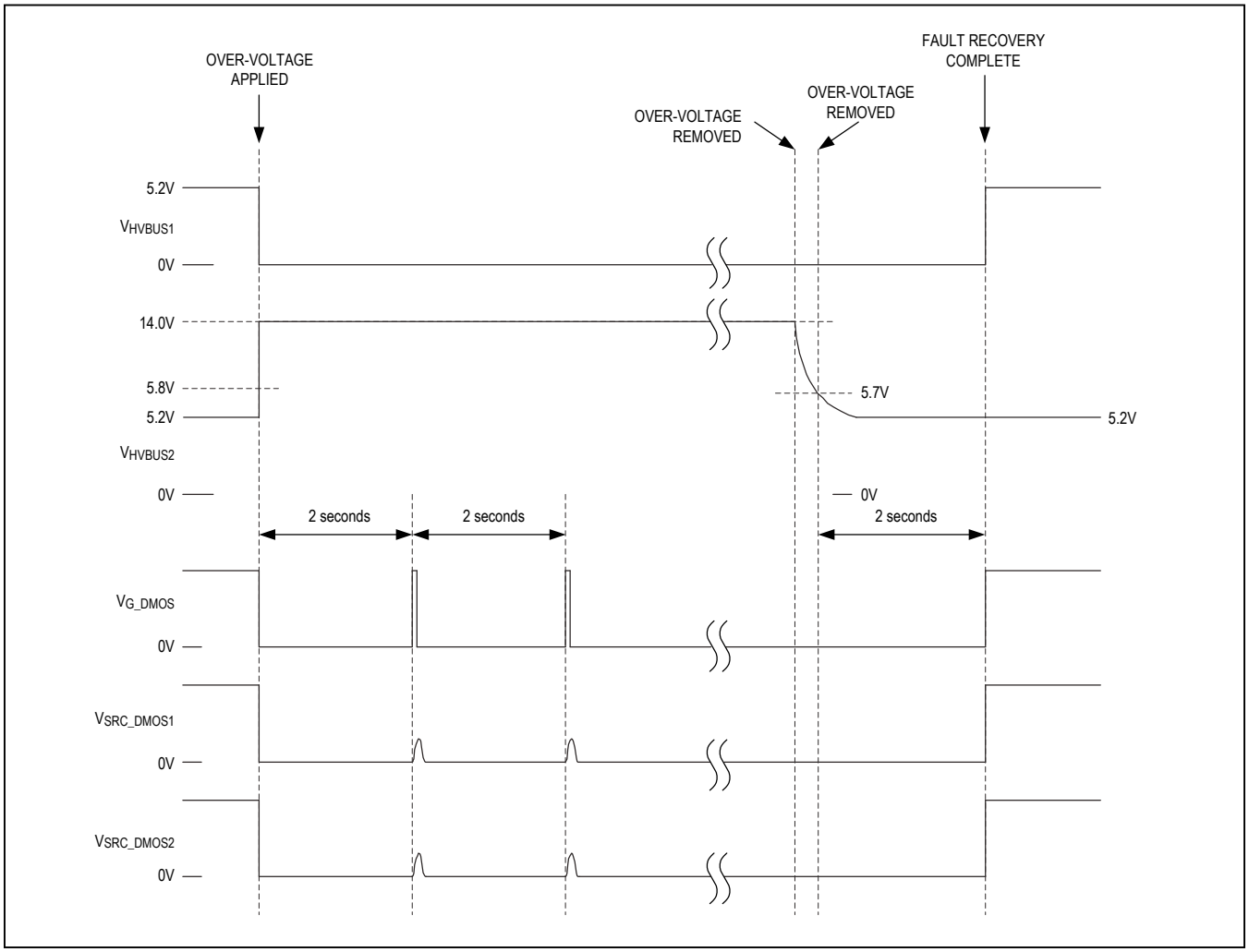


Figure 2. HVBUS2 Short-to-Battery

VBUS Short-to-Ground Protection

The IC also protects the VBUS channels against shorts to ground. The UV_USB threshold for both VBUS channels is continually monitored and if the voltage on either VBUS channel falls below 4.45V, the internal MOSFET for the affected channel is disabled instantaneously, disconnecting the channel from PV. The 25mA diagnostic current source is connected to the SRC_DMOS_ pin of the shorted channel, forcing a small current. When the short is removed and the voltage monitored by the V_{RETRY} comparator rises above the 0.5V threshold, the 2s timer is started. After the timer expires, the internal MOSFET for the previously shorted channel is enabled, reconnecting the VBUS channel to the PV supply. Figure 3 depicts how a short-to-ground on VBUS1 is detected and the fault recovered.

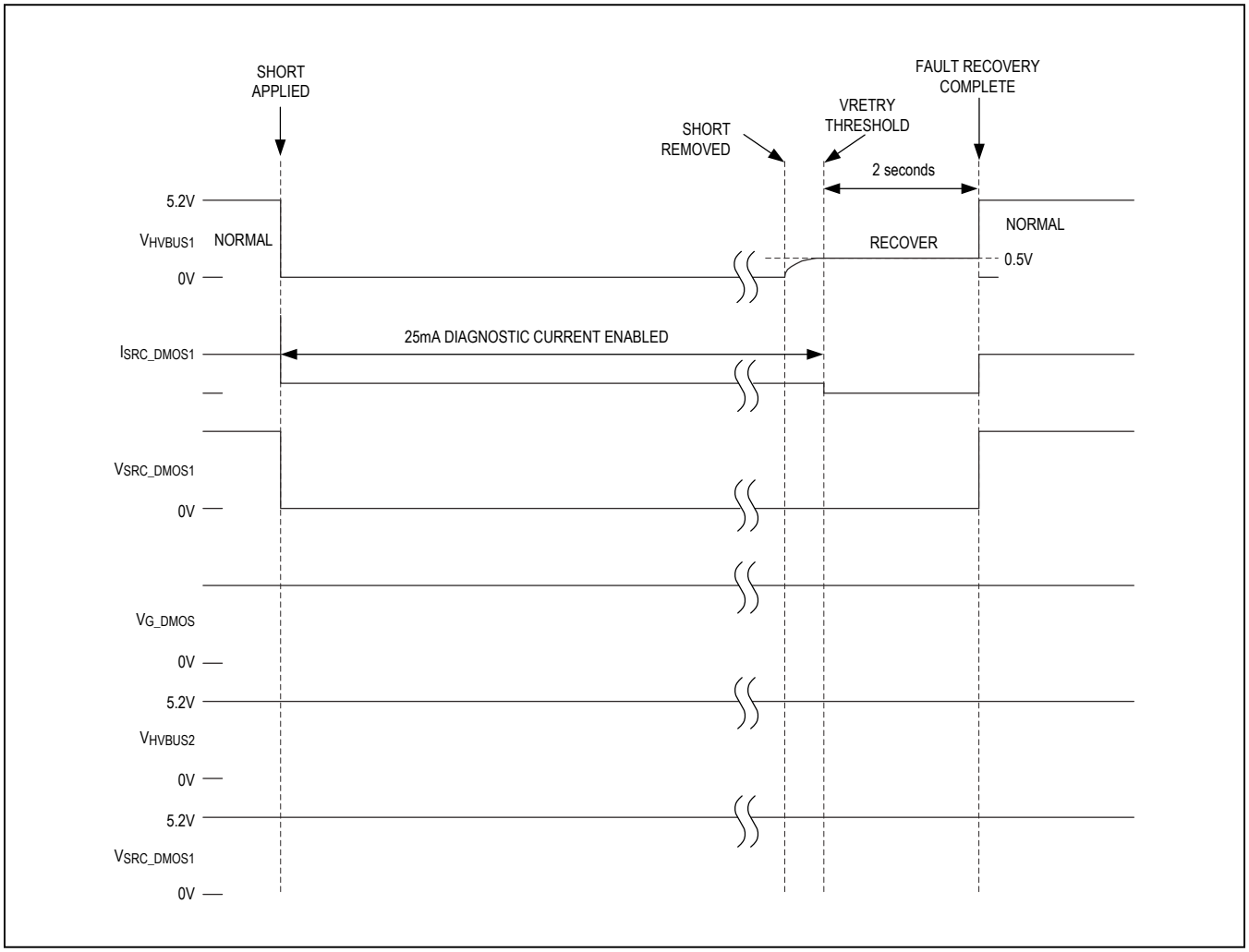


Figure 3. HVBUS1 Short-to-Ground

Thermal Foldback

If the die temperature reaches the 140°C foldback threshold, the DC-DC output current is reduced. Once the die temperature falls below tthe hermal trip point, a retry is attempted after 2s.

Table 1. Fault Table

FAULT CONDITION	ACTION	FAULT-DEBOUNCE TIME	RECOVERY ACTION	FAULT/ RETRY TIMER
• HVDP_/HVDM_ overvoltage	• Disable SRC_DMOS1 • Disable SRC_DMOS2 • Disable G_DMOS • Disable both DCP data switches • Reset DCP FSMs	0s	• Enable SRC_DMOS1 • Enable SRC_DMOS2 • Enable G_DMOS • Enable both DCP data switches • Enable DCP FSMs	2s
• SRC_DMOS1/ SRC_DMOS2 • Short-to-battery	• Disable SRC_DMOS1 • Disable SRC_DMOS2 • Disable G_DMOS • Disable both DCP data switches • Reset DCP FSMs	0s	• Enable SRC_DMOS1 • Enable SRC_DMOS2 • Enable G_DMOS • Enable both DCP data switches • Enable DCP FSMs	2s
• SRC_DMOS1/ • SRC_DMOS2 • Short-to-ground	• Disable Respective SRC_DMOS_ • Disable respective DCP data switches • Reset DCP FSMs	0s	• Enable respective SRC_DMOS_ • Enable respective DCP data switches and enable DCP FSMs	2s
• SRC_DMOS1/ SRC_DMOS2 • Overcurrent	• Disable respective SRC_DMOS_ • Disable respective DCP data switches • Reset DCP FSMs	2ms	• Enable respective SRC_DMOS_ • Enable respective DCP data switches • Enable DCP FSMs	2s
• SRC_DMOS1/ SRC_DMOS2 • Undervoltage	• Disable respective SRC_DMOS_ • Disable respective DCP data switches • Reset DCP FSMs	2ms	• Enable respective SRC_DMOS_ • Enable respective DCP data switches • Enable DCP FSMs	2s
• PV • Undervoltage	• Disable SRC_DMOS1 • Disable SRC_DMOS2 • Disable G_DMOS • Disable both DCP data switches • Reset DCP FSMs	0s	• Enable SRC_DMOS1 • Enable SRC_DMOS2 • Enable G_DMOS • Enable both DCP data switches • Enable DCP FSMs	2s

Table 1. Fault Table (continued)

FAULT CONDITION	ACTION	FAULT-DEBOUNCE TIME	RECOVERY ACTION	FAULT/ RETRY TIMER
• Thermal shutdown • +165°C	• Disable DC-DC converter • Disable SRC_DMOS1 • Disable SRC_DMOS2 • Disable G_DMOS • Disable both DCP data switches • Reset DCP FSMs	1ms	• Reset device	0s
• Thermal Foldback • +140°C	• Set ILIM to foldback value • Disable SRC_DMOS1 • Disable SRC_DMOS2 • Disable G_DMOS • Disable both DCP data switches • Reset DCP FSMs	20ms	• Restore ILIM to ILIM selection • Enable SRC_DMOS1 • Enable SRC_DMOS2 • Enable G_DMOS • Enable both DCP data switches • Enable DCP FSMs	2s

USB Automatic Charge Detection

The IC combines two USB dedicated charging ports (DCP) and automatic charge detection in one device.

The IC features an iPad/iPod/SSG/DCP-detection block for emulating and charging dedicated Apple, Samsung, and USB-IF DCPs. Autodetection mode's HVDP_/HVDM_ pins are connected to internal resistor-dividers to provide the proper Apple-compliant iPad bias voltage. Initially, if the iPad bias voltage is presented on the HVDP_/HVDM_ pins, the IC monitors the voltage to determine the type of device attached.

If the voltage at HVDM_ is +2.3V (typ) (PV x 0.46) or higher and the voltage at HVDP_ is +2.3V (typ) (PV x 0.46) or lower, the state remains unchanged and the iPhone termination resistors remain present. If the voltage at HVDM_ is forced below the +2.3V (typ) threshold, or if the voltage at HVDP_ is forced higher than the +2.3V threshold, the internal switch disconnects HVDM_ and HVDP_ from the resistor-divider (iPhone switch open) and HVDP_ and HVDM_ are shorted together for dedicated charging mode.

Hold Mode

When hold mode is enabled, an internal enable signal keeps the buck converter and logic circuitry powered. An internal hold timer determines how long the USB ports (i.e., buck converter, DCP charge detection) remain powered on. When the hold timer has expired, the internal enable signal is dropped and the IC is powered off.

When hold-only mode is enabled and the external HVEN is set low, the USB port must be discharged and remain in this state for 2s (typ) as USB-IF and Apple require this dead time when the USB port switches roles between on/off to DCP operation. The DCP circuitry is always active in hold mode; If HVEN is set high while still in hold mode, the 5V output must once again be discharged first for 2s duration.

ESD Protection

The IC requires no external ESD protection. All Maxim devices incorporate ESD protection structures to protect against electrostatic discharges encountered during handling, assembly, and system-level operation. When used with the configuration shown in the *Typical Application Circuit*, the IC is characterized for protection to the following limits:

- ±25kV ISO 10605 Air Gap
- ±8kV ISO 10605 Contact Discharge
- ±15kV IEC 61000-4-2 Air Gap
- ±8kV IEC 61000-4-2 Contact Discharge
- ±15kV 330Ω, 330pF Air Gap
- ±8kV 330Ω, 330pF Contact Discharge

Note: All application-level ESD testing is performed on the standard evaluation kit.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for test setup, test methodology, and test results.

Human Body Model

Figure 4 shows the Human Body Model and Figure 5 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. The IC helps users design equipment that meet Level 4 of IEC 61000-4-2. The main difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2. Because series resistance is lower in the IEC 61000-4-2 ESD test model (Figure 4), the ESD withstand voltage measured to this standard is generally lower than that measured using the Human Body Model (Figure 5). Figure 6 shows the current waveform for the ±8kV, IEC 61000-4-2 Level 4, ESD Contact Discharge test. The Air Gap Discharge test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

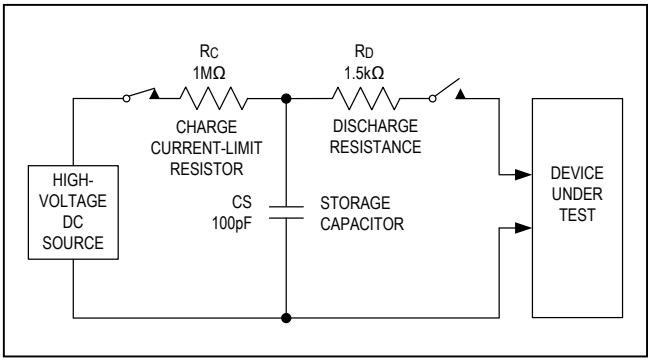


Figure 4. IEC 61000-4-2 ESD Test Model

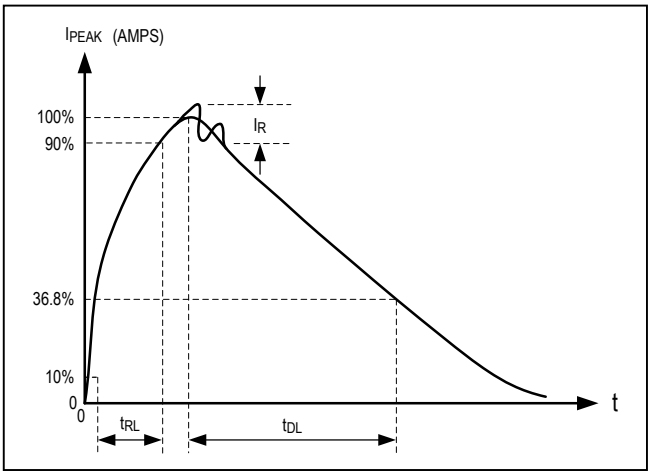


Figure 5. Human Body Current Waveform

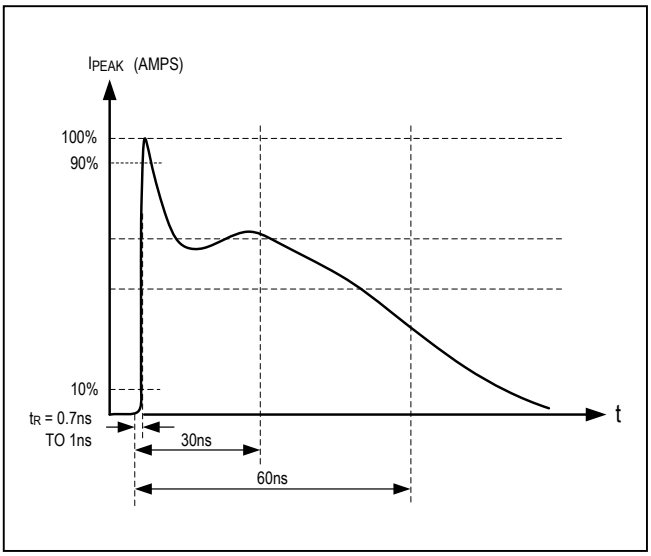


Figure 6. IEC 61000-4-2 ESD Generator Current Waveform

Applications Information

Component Selection

R_{FOSC} Selection

The switching frequency of the MAX20047 DC-DC IC is set by connecting a resistor between the FOSC pin and AGND. The internal oscillator can be tuned across a wide frequency range, providing greater system-design flexibility. The graph shown in Figure 7 plots frequency vs. R_{FOSC} resistance.

Table 2 lists switching frequencies set with standard 1% resistor values.

Spread-Spectrum Option

There is a version of the IC that enables the oscillator to run in spread-spectrum mode. This improves EMI performance by modulating the internal oscillator frequency up/down ±3% relative to the operating frequency. If the spread-spectrum option is desired, see the *Ordering Information* table for the correct part number.

Setting the VBUS Current Limit (ILIM)

ILIM is a multifunctional pin that can be used to program the VBUS current limit, the Apple divider-current, and the foldback-current threshold. Table 3 lists the configuration options for the ILIM pin.

Hold Mode

During device boot, the hold configuration is loaded with a value that depends on decoding/reading the external CONFIG resistor. For more details regarding the value loaded as a function of resistors connected, see Table 4.

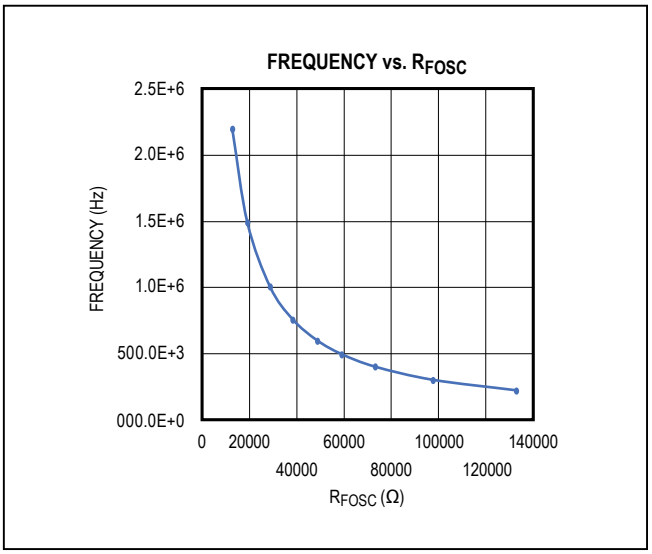


Figure 7. Frequency vs. R_{FOSC} Resistance

Table 2. Switching Frequencies

FOSC (kHz)	224,320	300,840	380,500	493,100	595,800	756,000	1,000,500	1,479,000	2,237,000
R_{FOSC} (kΩ)	133	97.6	73.2	59	48.7	38.3	28.7	19.1	12.7

Table 3. Configuration Options for ILIM Pin

ILIM PIN CONNECTION	APPLE DIVIDER (A)	ILIM (A)	FOLDBACK (A)
Connect to AGND	2.4	3.3	None
8,870Ω to AGND	2.4	3.3	2.41
15,800Ω to AGND	2.4	3.3	2.1
24,900Ω to AGND	2.4	2.75	2.1
35,700Ω to AGND	2.4	2.75	None
49,900Ω to AGND	2.1	2.41	None
68,100Ω to AGND	2.1	2.41	2.1
Connect to BIAS	1.0	2.1	None

Table 4. Configuration Pin Options

CONFIG PIN CONNECTION	LEVEL (AT 50µA)	HOLD MODE	HOLD TIME (MIN)
Connect to AGND	Ground	Disabled	N/A
24,900Ω to AGND	1.25V	Enabled	30
Connect to BIAS	V_{BIAS}	Enabled	60

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). The device is designed to operate with the ratio of inductor peak-to-peak AC current to DC average current (LIR) between 15% and 30% (typ). The switching frequency, input voltage, and output voltage then determine the inductor value as follows:

$$L_{MIN1} = \frac{(V_{SUPSW} - V_{OUT\_}) \times V_{OUT}}{V_{SUPSW} \times f_{SW} \times I_{MAX} \times 33\%}$$

where V_{SUPSW} and V_{OUT} are typical values (so that efficiency is optimum for typical conditions). The switching frequency is set by R_{FOSC}.

R_{CS} = 300mΩ

I_{MAX} = 6A

f_{SW} = The operating frequency is set by R_{FOSC}.

The next equation ensures that the inductor current downslope is less than the internal slope compensation. For this to be the case, the following equation needs to be satisfied:

$$-m \geq \frac{m2}{2}$$

where m2 = The inductor current downslope:

$$\frac{V_{OUT}}{L} \times R_{CS}$$

-m = Slope compensation: $\left[1.333 \frac{V}{\mu s}\right]$

Solving for L and adding a 1.5 multiplier to account for tolerances in the system:

$$L_{MIN2} = V_{OUT} \times \frac{R_{CS}}{2 \times m} \times 1.5$$

To satisfy both L_{MIN1} and L_{MIN2}, L_{MIN} must be set to the larger of the two:

$$L_{MIN} = Max\ (L_{MIN1}, L_{MIN2})$$

The maximum nominal inductor value recommended is 1.6 times the chosen value from the above formula.

$$L_{MAX} = 1.6 \times L_{MIN}$$

Select a nominal inductor value based on the following formula:

$$L_{MIN} < L_{NOM} < L_{MAX}$$

The best choice of inductor is usually the first standard inductor value greater than L_{MIN}.

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching.

Place a 4.7µF (or larger) ceramic capacitor directly from SUPSW to PGND positioned as close as possible to the pins. A bulk capacitor with higher ESR (such as an electrolytic capacitor) is normally required as well to lower the Q of the front-end circuit and provide the remaining capacitance needed to minimize input-voltage ripple.

The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{LOAD(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{SUPSW} - V_{OUT})}}{V_{SUPSW}}$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage:

$$V_{SUPSW} = 2 \times V_{OUT}$$

Therefore:

$$I_{RMS} = \frac{I_{LOAD(MAX)}}{V_{SUPSW}}$$

Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability.

The input-voltage ripple is comprised of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple-current capability at the input. Assume the contribution from the ESR and capacitor discharge equal to 50%. Calculate the input capacitance and ESR required for a specified input voltage ripple using the following equations:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{OUT} + \frac{\Delta I_L}{2}}$$

where:

$$\Delta I_L = \frac{(V_{SUPSW} - V_{OUT}) \times V_{OUT}}{V_{SUPSW} \times f_{SW} \times L}$$

and:

$$C_{IN} = \frac{I_{OUT} \times D(1-D)}{\Delta V_Q \times f_{SW}}$$

$$D = \frac{V_{OUT}}{V_{SUPSW}}$$

where: I_{OUT} is the maximum output current and D is the duty cycle.

Output Capacitor

The output filter capacitor must have low enough equivalent series resistance (ESR) to meet output-ripple and load-transient requirements. The output capacitance must be high enough to absorb the inductor energy while transitioning from full-load to no-load conditions, without tripping the overvoltage-fault protection. When using high-capacitance, low-ESR capacitors, the filter capacitor's ESR dominates the output-voltage ripple, so the size of the output capacitor depends on the maximum ESR required to meet the output-voltage ripple ($V_{RIPPLE(P-P)}$) specifications shown below:

$$V_{RIPPLE(P-P)} = ESR \times I_{LOAD(MAX)} \times LIR$$

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating, rather than capacitance value.

When using low-capacity filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent voltage droop and voltage rise from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem. However, low-capacity filter capacitors typically have high-ESR zeros that can affect the overall stability.

Compensation Network

The IC uses an internal transconductance error amplifier, with its inverting input and its output available to the user for external frequency compensation. The output capacitor and compensation network determine the loop stability. The inductor and the output capacitor are chosen based on performance, size, and cost. Additionally, the compensation network optimizes the control-loop stability.

The converter uses a current-mode-control scheme that regulates the output voltage by forcing the required current through the external inductor. The device uses the voltage drop across the high-side MOSFET to sense inductor current. Current-mode control eliminates the double pole in the feedback loop caused by the inductor and output capacitor, resulting in a smaller phase shift and requiring less elaborate error-amplifier compensation than voltage-mode control. Only a simple single-series resistor (R_C) and capacitor (C_C) are required to have a stable, high-bandwidth loop in applications where ceramic capacitors are used for output filtering (see Figure 3). For other types of capacitors, due to the higher capacitance and ESR, the frequency of the zero created by the capacitance and ESR is lower than the desired closed-loop crossover frequency. To stabilize a nonceramic output-capacitor loop, add another compensation capacitor (C_F) from COMP to ground to cancel this ESR zero.

The basic regulator loop is modeled as a power modulator, output feedback-divider, and an error amplifier (see Figure 8). The power modulator has a DC gain set by $g_m \times R_{LOAD}$, with a pole and zero pair set by R_{LOAD}, the output capacitor (C_{OUT}), and its ESR. The following equations help to approximate the value for the gain of the power modulator ($GAIN_{MOD(dc)}$), neglecting the effect of the ramp stabilization. Ramp stabilization is necessary when the duty cycle is above 50% and is internally done for the devices:

$$GAIN_{MOD(dc)} = g_{mc} \times R_{LOAD}$$

where:

$$R_{LOAD} = \frac{V_{OUT}}{I_{OUT(MAX)}}$$

and:

$$g_{mc} = 3s$$

In a current-mode step-down converter, the output capacitor, its ESR, and the load resistance introduce a pole at the following frequency:

$$f_{pMOD} = \frac{1}{2\pi \times C_{OUT} \times R_{LOAD}}$$

The output capacitor and its ESR also introduce a zero at:

$$f_{zMOD} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

When C_{OUT} is composed of "n" identical capacitors in parallel, the resulting C_{OUT} = n x $C_{OUT(EACH)}$, and ESR = ESR (EACH)/n. Note that the capacitor zero for a parallel combination of alike capacitors is the same as for an individual capacitor.

The feedback voltage-divider has a gain of $GAIN_{FB}$ = V_{FB}/V_{OUT}, where V_{FB} is 1V (typ).

The transconductance error amplifier has a DC gain of $GAIN_{EA(DC)}$ = g_{m_EA} x R_{OUT_EA}, where g_{m_EA} is the error-amplifier transconductance, which is 700µS (typ), and R_{OUT_EA} is the output resistance of the error amplifier (50MΩ).

A dominant pole (f_{dpEA}) is set by the compensation capacitor (C_C) and the amplifier output resistance (R_{OUT_EA}). A zero (f_{zEA}) is set by the compensation resistor (RC) and the compensation capacitor (C_C). There is an optional pole (f_{pEA}) set by C_F and R_C to cancel the output capacitor ESR zero if it occurs near the crossover frequency (f_C, where the loop gain equals 1 (0dB)). Thus:

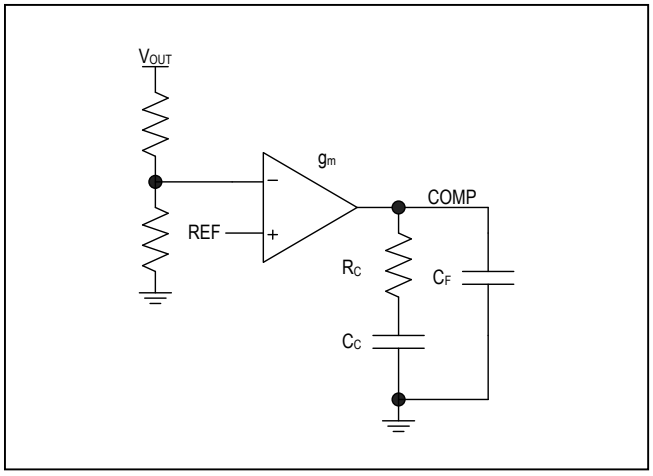


Figure 8. Compensation Network

$$f_{zEA} = \frac{1}{2\pi \times C_C \times R_C}$$

$$f_{dpEA} = \frac{1}{2\pi \times C_C \times \left(R_{OUT\_EA} + R_C\right)}$$

$$f_{PEA} = \frac{1}{2\pi \times C_F \times R_C}$$

The loop-gain crossover frequency (f_C) should be set below 1/5 of the switching frequency and much higher than the power-modulator pole (f_{pMOD}).

$$f_{pMOD} \ll f_C \le \frac{f_{SW}}{5}$$

The total loop gain as the product of the modulator gain, the feedback voltage-divider gain, and the error-amplifier gain at f_C should be equal to 1. So:

$$GAIN_{MOD}\left(f_C\right) \times \frac{V_{FB}}{V_{OUT}} \times GAIN_{EA}\left(f_C\right) = 1$$

For the case where f_{ZMOD} is greater than f_C:

$$GAIN_{EA(f_C)} = g_{m\_EA} \times R_C$$

Therefore:

$$GAIN_{MOD}\left(f_C\right) \times \frac{V_{FB}}{V_{OUT}} \times g_{m\_EA} \times R_C = 1$$

Solving for R_C:

$$R_C = \frac{V_{OUT}}{g_{m\_EA} \times V_{FB} \times GAIN_{MOD}\left(f_C\right)}$$

Set the error-amplifier compensation zero formed by R_C and C_C (f_{zEA}) at the f_{pMOD}. Calculate the value of C_C as follows:

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C}$$

If f_{zMOD} is less than 5 x f_C, add a second capacitor (C_F) from COMP to ground and set the compensation pole formed by R_C and C_F (f_{pAE}) at the f_{zMOD}. Calculate the value of C_F as follows:

$$C_F = \frac{1}{2\pi \times f_{zMOD} \times R_C}$$

As the load current decreases, the modulator pole also decreases; however, the modulator gain increases accordingly and the crossover frequency remains the same. For the case where f_{zMOD} is less than f_C:

The power-modulator gain at f_C is:

$$GAIN_{MOD(f_C)} = GAIN_{EA(dc)} \times \frac{f_{pMOD}}{f_{zMOD}}$$

The error-amplifier gain at f_C is:

$$GAIN_{EA(f_C)} = g_{m\_EA} \times R_C \times \frac{f_{zMOD}}{f_C}$$

Therefore:

$$GAIN_{MOD(f_C)} \times \frac{V_{FB}}{V_{OUT}} \times g_{m\_EA} \times R_C \times \frac{f_{zMOD}}{f_C} = 1$$

Solving for R_C:

$$R_C = \frac{V_{OUT} \times f_C}{g_{m\_EA} \times V_{FB} \times GAIN_{MOD(f_C)} \times f_{zMOD}}$$

Set the error-amplifier compensation zero formed by R_C and C_C at the f_{pMOD} (f_{zEA} = f_{zMOD}).

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C}$$

If f_{zMOD} is less than 5 x f_C, add a second capacitor (C_F) from COMP to ground. Set f_{pEA} = f_{zMOD} and calculate C_F as follows:

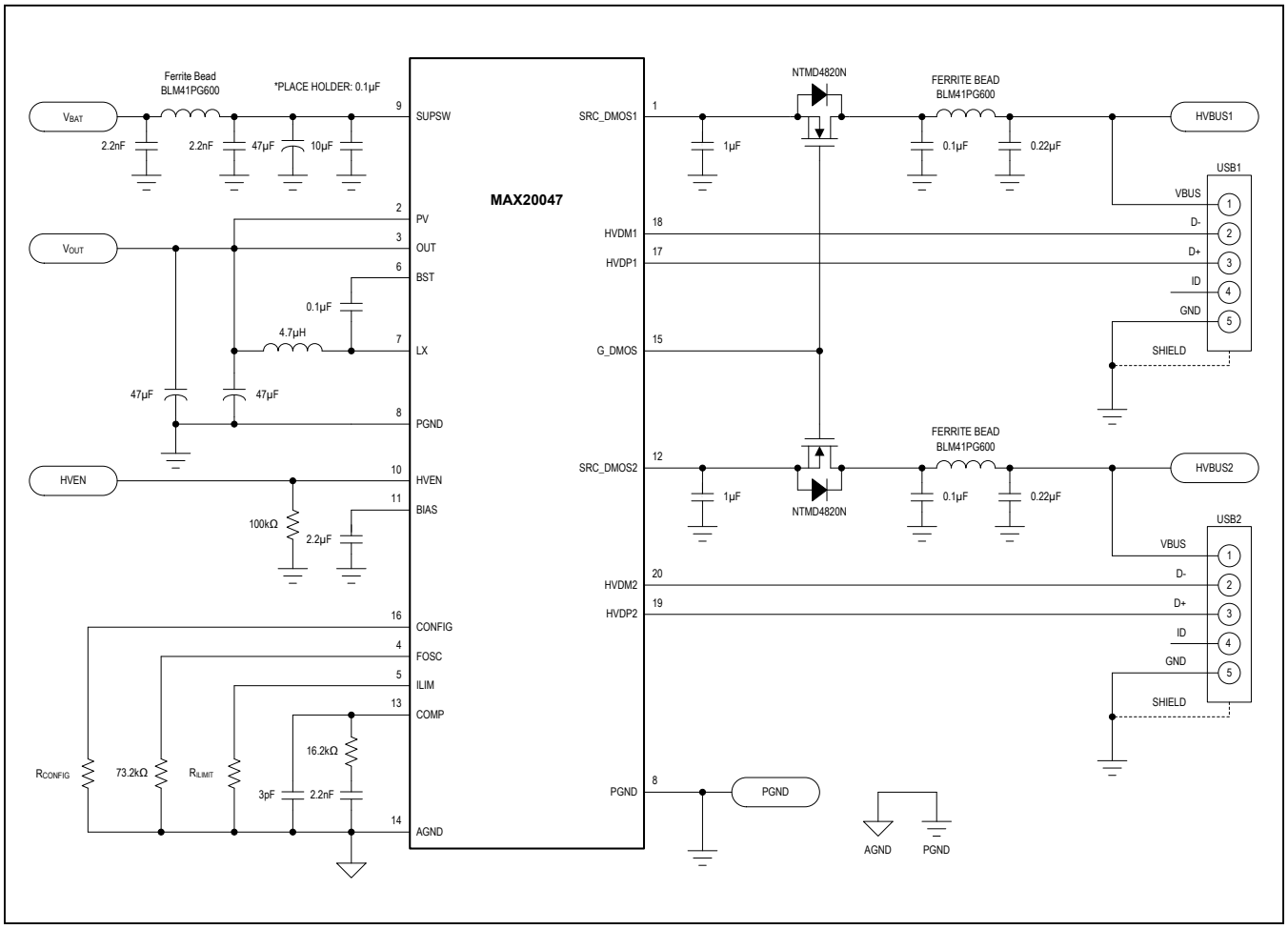
$$C_F = \frac{1}{2\pi \times f_{zMOD} \times R_C}$$

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. Follow these guidelines for good PCB layout:

- Place the ceramic input capacitor as close as possible to the SUPSW and PGND pins on the same side as the device. This will provide the best EMI rejection and minimize internal noise on the device, which can degrade performance.
- Use a large contiguous copper plane connected to the PGND pads. Ensure that all heat-dissipating components have adequate cooling. Use multiple vias to drop the PGND plane to the inner/bottom layers for maximum heat dissipation.
- Isolate the power components and high-current path from the sensitive analog circuitry. This is essential to prevent any noise coupling into the analog signals.
- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. The high-current path comprising input capacitor, high-side FET, inductor, and output capacitor should be as short as possible.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PCBs (2oz vs. 1oz) to enhance full-load efficiency.
- The analog signal lines should be routed away from the high-frequency planes. This ensures integrity of sensitive signals feeding back into the IC.
- The ground connection for the analog and power section should be close to the IC. This keeps the ground current loops to a minimum. In cases where only one ground is used, adequate isolation between analog return signals and high-power signals must be maintained.

Typical Application Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	SPREAD SPECTRUM
MAX20047AFPA/V+	-40°C to +125°C	20 FC-2QFN	Yes
MAX20047AFPB/V+	-40°C to +125°C	20 FC-2QFN	No

Note: *For variants with different options, contact factory.*
/V+ denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: CMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/17	Initial release	—

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