MAX20330A

Precision HV Capable ID Detector

General Description

The MAX20330A is an ID detection IC that detects the ID resistor values when it is enabled. The device automatically adjusts the detection current to check the wide range of the ID resistor values while keeping the average supply current low.

The MAX20330A supports the factory mode for direct system or battery current measurement. The device protects the internal supply from the overvoltage on ID pin up to 40V.

The device is available in an 8-bump (0.35mm pitch, 1.77mm x 1.03mm) wafer-level package (WLP) and operates over the -40°C to +85°C extended temperature range.

Applications

- Smart Phones
- Tablet PCs
- E-Readers

Benefits and Features

- Protects Battery Connected Modules with Minimum Power Consumption
  - Ultra-Low Shutdown Current: 2.8μA (Typ)
  - Ultra-Low ID Detection Current: 2μA (Typ)
- Flexible ID Detection and Support
  - Automatic and Manual ID Value Detection
  - Factory Mode Detection
  - Automatic Device Detection and Interrupt
- ID Overvoltage Protection
  - Blocking High-Voltage Input
- Provides Premium Security in System Reliability
  - High Input Voltage Tolerant
  - Thermal Shutdown Protection
- Space Saving
  - 8-Bump, 0.35mm Pitch, 1.77mm x 1.03mm WLP

***Ordering Information* appears at end of data sheet.**

Absolute Maximum Ratings

(All voltages referenced to GND.)
ID, $\overline{\text{EN}}$, PCON to GND ....-0.3V to +40V
SDA, SCL, $\overline{\text{INT}}$, V_{CC} to GND ....-0.3V to +6V
Continuous Current into all pins ....±0.1A
Continuous Power Dissipation (T_A = +70°C)
WLP (derate 10.9mW/°C above +70°C).....................872mW

Operating Temperature Range.......................... -40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range .... -65°C to +150°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....91.72°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{CC} = 2.6V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}						
V_{CC} Voltage Range	V_{CC}		2.6	3.3	5.5	V
V_{CC} Supply Current	I_{CC}	V_{CC} = 4.2V, I_{SRC} = 0mA , manual detection mode, ENb = 0		130	200	µA
V_{CC} Shutdown Current	I_{CC_SHDN}	V_{CC} = 4.2V, ENb = 1		2.8	5	µA
ID Current Source						
Current Source Accuracy			-5		+5	%
Current Source Open Voltage		ISRC = 2µA			2	V
Current Source	I_{ID}			2		µA
				6		µA
				18		µA
				54		µA
				162		µA
				2.5		mA
Average Current Source	I_{ID_AVG}	162µA max current , IS_PERIOD ≥ 130x, ISRC_MAN = 0			2	µA
PCON						
Open-Drain Voltage					36	V
Output Low Voltage	V_{OL}	I_{SINK} = 10mA		0.1	0.2	V
Leakage Current	I_{LEAK}	Open-drain, PCON < ID + 7V			1	µA

Electrical Characteristics (continued)

(V_{CC} = 2.6V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C) (Note 2)

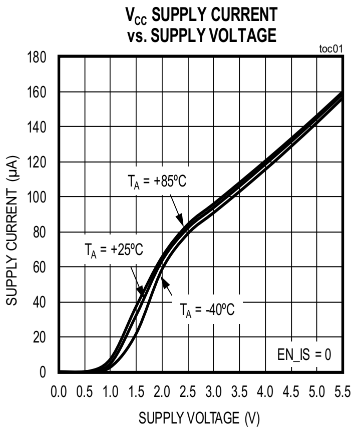
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC						
Resolution				8		Bit
Voltage Step				5.9		mV
Full-Scale Error			-2		+2	%
Noise Filtering				100		µs
Full Scale				1.5		V
DIGITAL SIGNALS (SDA, SCL, $\overline{INT}$)						
Output Low Voltage	V_{OL}	V_{IO} = 3.3V, I_{SINK} = 3mA			0.4	V
Leakage Current		V_{IO} = 2.6V, open-drain			1	µA
Input Logic-High	V_{IH}		1.4			V
Input Logic-Low	V_{IL}				0.4	V
Input Leakage Current		V_{IN} = 0V, V_{IN} = 2.6V	-1		+1	µA
DIGITAL SIGNAL ($\overline{EN}$)						
$\overline{EN}$ Logic-Low		With respect to V_{CC}		55		%V_{CC}
$\overline{EN}$ Hysteresis				20		%V_{CC}
Input Leakage Current	I_{IN}	V_{IN} = 0V, V_{IN} = 2.6V	-1		+1	µA
TIMING CHARACTERISTICS (Note 3)						
ID Current Source On Time	t_{IS_TDET}			Programmable		ms
ID Current Source Off Period Time	t_{IS_PERIOD}	ID off to ID turn on		Programmable		ms
$\overline{EN}$ Debounce Time				100		ms
Programmable Time Accuracy			-10		+10	%
I^2C Maximum Clock Frequency				400		kHz
THERMAL PROTECTION						
Thermal Shutdown				125		°C
Thermal Shutdown Hysteresis				20		°C

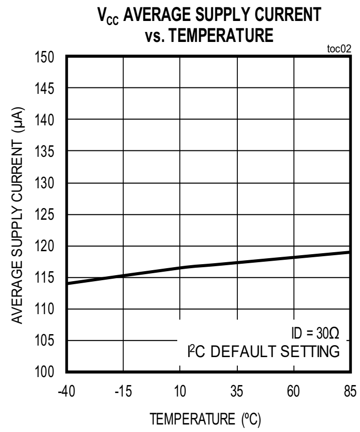
Note 2: All devices are 100% production tested at T_A = +25°C. Specifications over the operating temperature range are guaranteed by design.

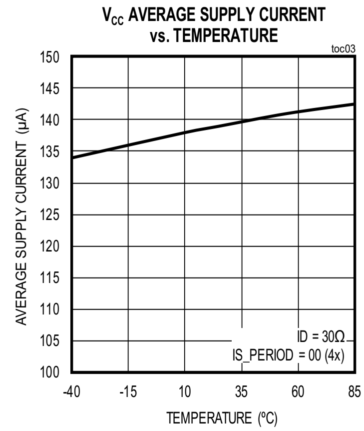
Note 3: All timing characteristics are measured using 20% and 80% level unless otherwise specified.

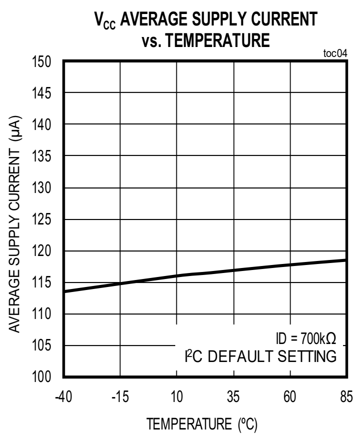
Typical Operating Characteristics

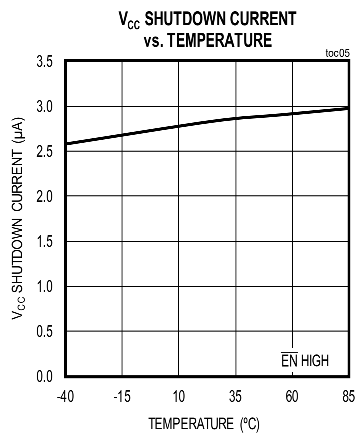
(V_{CC} = 4.2V, T_A = +25°C, unless otherwise noted.)

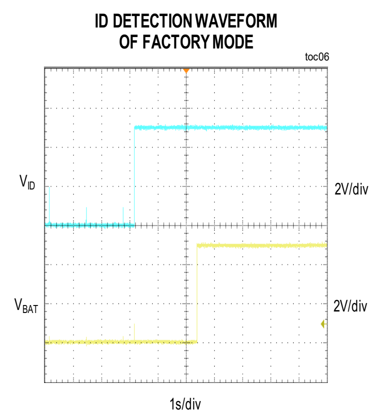


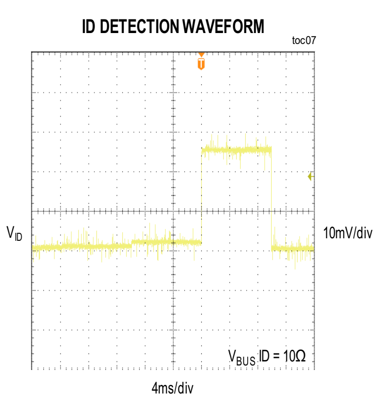


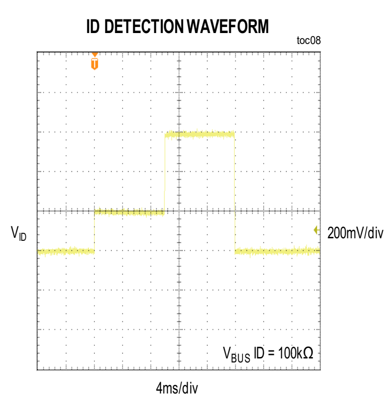


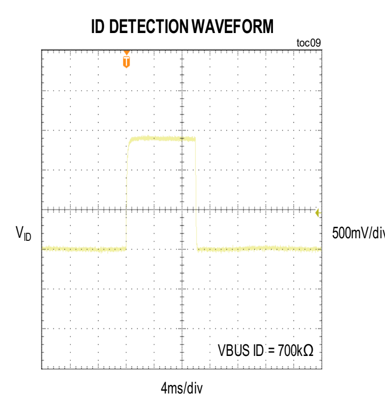




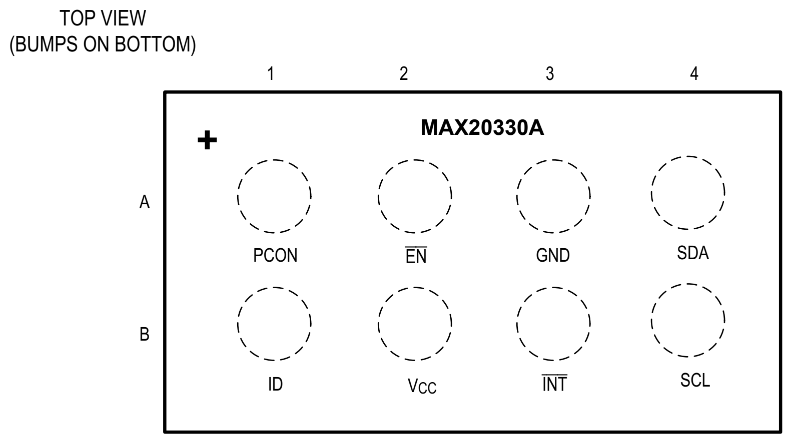








Bump Configuration



Bump Description

BUMP	NAME	FUNCTION
A1	PCON	External P-FET Control. Open-drain, high-voltage to drive an external, back-to-back open-drain in factory mode.
A2	$\overline{EN}$	Active-Low Enable ID Detection
A3	GND	Ground
A4	SDA	I^2C Data Line. Connect SDA to an external pullup resistor.
B1	ID	ID of USB Connector. For proper ESD and surge protection, place the external TVS on ID.
B2	V_{CC}	Supply for the I^2C Digital Block. Bypass V_{CC} to ground with a 0.1μF capacitor as close to the device as possible.
B3	$\overline{INT}$	Interrupt Output.
B4	SCL	I^2C Clock Line. Connect SCL to an external pullup resistor.

Functional Diagram

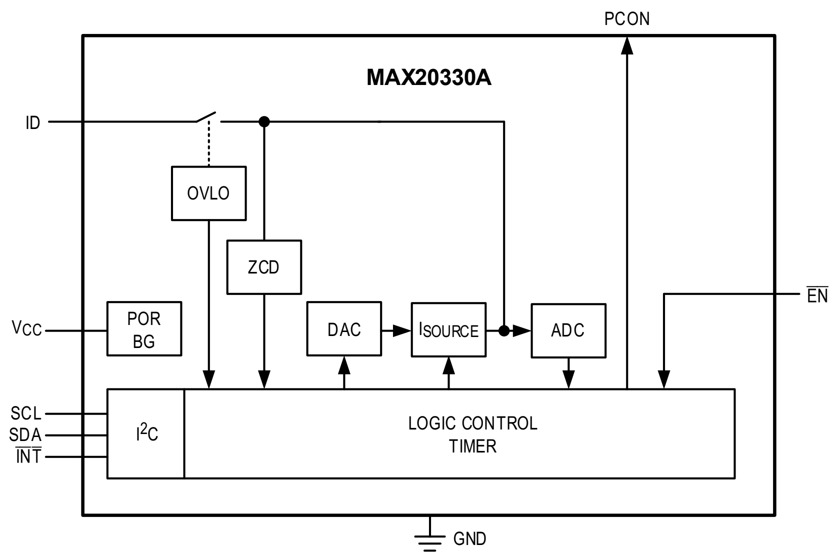


Table 1. Register Map

ADDRESS	NAME	TYPE	DEFAULT	DESCRIPTION
0x00	CHIP ID	Read Only	0x80	Device ID Register
0x01	CONTROL 1	RW	0x6A	System Control 1
0x02	STATUS	Read Only	0x00	Status Register
0x03	INTERRUPT	Clear on Read	0x00	Interrupt Register
0x04	MASK	RW	0xFF	Mask Register
0x06	I_SRC	RW	0x03	Current Source Threshold
0x07	I_SRC_TMR	RW	0x13	Current Source On Timer
0x08	CONTROL 2	RW	0x0C	System Control 2
0x09	PCON CTRL	RW	0x00	PCON Control
0x0A	ACCDET_REF	RW	0x6E	Accessory Detection Threshold
0x0B	ISRC_ADC	Read Only	0x00	Current Source Output
0x0D	FM_I_SET	RW	0x02	Factory Mode
0x0E	FM_HI_LIM	RW	0xAF	Factory Mode High Limit
0x0F	FM_LO_LIM	RW	0x82	Factory Mode Low Limit

Table 2. Detailed Register Map

CHIP ID 0x00 (**Read Only**)								
BIT	7	6	5	4	3	2	1	0
BIT NAME	CHIP_ID				CHIP_REV			
Reset Value	1	0	0	0	0	0	0	0
Description	Chip ID and Revision							
CONTROL 1 0x01 (Read/Write)								
BIT	7	6	5	4	3	2	1	0
BIT NAME	RFU	EN_IS	CZC	RFU	RFU	RFU	FM_ENb	ENb
Reset Value	0	1	1	0	1	0	1	0
RFU	Reserved for future use							
EN_IS	Current Source (I_SRC) Enable 0 = I_SRC disabled 1 = I_SRC enabled (default)							
CZC	Control of Zero-Crossing Detection 0 = CZC disabled 1 = CZC enabled (default)							
FM_ENb	Factory Mode Active-Low Enable 0 = FM is enabled 1 = FM is disabled (default)							
ENb	Device Active-Low Enable 0 = device is in active mode (default) 1 = device is in sleep mode							

Table 2. Detailed Register Map (continued)

STATUS 0x02 (Read Only)								
BIT	7	6	5	4	3	2	1	0
BIT NAME	VIN_OK	ZCS	EOC	TP_OUT	ACC_DET	THERM_ SHDN	ID_OVLO	OVLO_ ENb
Reset Value	0	0	0	0	0	0	0	0
VIN_OK	VIN (ID) is above 2.7V (typ) in factory mode 0 = ID is below 2.7V 1 = ID is above 2.7V							
ZCS	Zero-Crossing Flag (only valid when CZC = 1) 0 = no ZC 1 = ZC in last IS_TDET							
EOC	End of ADC Conversion 0 = no conversion since last read 1 = new ADC data since last read							
TP_OUT	Timer Period Out 0 = timer period not expired 1 = timer period expired							
ACC_DET	Accessory Detection Status 0 = no change 1 = accessory detected							
THERM_SHDN	Thermal Shutdown 0 = no thermal shutdown 1 = thermal shutdown							
ID_OVLO	ID Overvoltage 0 = ID not overvoltage 1 = ID overvoltage (2V typ)							
OVLO_ENb	$\overline{EN}$ Pin Status 0 = $\overline{EN}$ pin disabled (high) 1 = $\overline{EN}$ pin enabled (low)							

Table 2. Detailed Register Map (continued)

INTERRUPT 0x03 (Clear on Read)								
BIT	7	6	5	4	3	2	1	0
BIT NAME	VIN_OKi	ZCSi	EOCi	TP_OUTi	ACC_ DETi	THERM_ SHDNi	ID_OVLOi	OVLO_ ENbi
Reset Value	0	0	0	0	0	0	0	0
VIN_OKi	VIN (ID) is above 2.7V interrupt 0 = interrupt not occurred 1 = interrupt occurred							
ZCSi	ZCS Flag interrupt 0 = interrupt not occurred 1 = interrupt occurred							
EOCi	ADC EOC interrupt 0 = interrupt not occurred 1 = interrupt occurred							
TP_OUTi	Timer Period OUT interrupt 0 = interrupt not occurred 1 = interrupt occurred							
ACC_DETi	Accessory Detection interrupt 0 = interrupt not occurred 1 = interrupt occurred							
THERM_SHDNi	Thermal Shutdown interrupt 0 = interrupt not occurred 1 = interrupt occurred							
ID_OVLOi	ID OVLO interrupt 0 = interrupt not occurred 1 = interrupt occurred							
OVLO_ENbi	$\overline{EN}$ pin interrupt 0 = interrupt not occurred 1 = interrupt occurred							

Table 2. Detailed Register Map (continued)

MASK 0x04 (Read/Write)								
BIT	7	6	5	4	3	2	1	0
BIT NAME	VIN_OKm	ZCSm	EOCm	TP_ OUTm	ACC_ DETm	THERM_ SHDNm	ID_ OVLOm	OVLO_ ENbm
Reset Value	1	1	1	1	1	1	1	1
VIN_OKm	VIN (ID) is above 2.7V interrupt 0 = not masked 1 = masked							
ZCSm	ZCS interrupt 0 = not masked 1 = masked							
EOCm	ADC EOC interrupt 0 = not masked 1 = masked							
TP_OUTm	Timer Period OUT interrupt 0 = not masked 1 = masked							
ACC_DETm	Accessory Detection interrupt 0 = not masked 1 = masked							
THERM_SHDNm	Thermal Shutdown interrupt 0 = not masked 1 = masked							
ID_OVLOm	ID OVLO interrupt 0 = not masked 1 = masked							
OVLO_ENbm	$\overline{EN}$ pin interrupt 0 = not masked 1 = masked							

Table 2. Detailed Register Map (continued)

I_SRC 0x06 (Read/Write)								
BIT	7	6	5	4	3	2	1	0
BIT NAME	RFU	I_SRC_MON			RFU	I_SRC_SET		
Reset Value	0	0	0	0	0	0	1	1
RFU	Reserved for future use.							
I_SRC_MON (Read Only)	Current source monitor 000 = off 001 = 2µA 010 = 6µA 011 = 18µA 100 = 54µA 101 = 162µA 110 = 2500µA 111 = reserved							
I_SRC_SET	Current source set In auto mode, it is the maximum current source set. Above this value, the auto ID detection is skipped. In manual mode, it is the fixed current source set. 000 = off 001 = 2µA 010 = 6µA 011 = 18µA (default) 100 = 54µA 101 = 162µA 110 = 2500µA 111 = reserved							

Table 2. Detailed Register Map (continued)

I_SRC_TMR 0x07 (Read/Write)								
BIT	7	6	5	4	3	2	1	0
BIT NAME	RFU		IS_PERIOD		IS_INIT_ SET	IS_TDET		
Reset Value	0	0	0	1	0	0	1	1
RFU	Reserved for future use.							
IS_PERIOD	Repeat period, off period 00 = 4x 01 = 130x (default) 10 = 250x 11 = 1600x							
IS_INIT_SET	Set the initial value different from IS_PERIOD and IS_TDET for the ID detection auto-mode 0 = use IS_PERIOD and IS_TDET for the initial check (2μA) (default) 1 = use IS_PERIOD = 00 and IS_TDET = 101 as the initial value. If the current source needs to increase, then use the programmed IS_PERIOD and IS_TDET value for the current source larger than 2μA.							
IS_TDET	Current source on time for detection 000 = 2500μs 001 = 3500μs 010 = 4000μs 011 = 10000μs (default) 100 = 40000μs 101 = 100000μs 110 = 400000μs 111 = 1sec							

CONTROL2 0x08 (Read/Write)								
BIT	7	6	5	4	3	2	1	0
BIT NAME	RFU	RFU	RFU	RFU	AUT_ISRC_SCL		ISRC_MAN	ISRC_ST
Reset Value	0	0	0	0	1	1	0	0
RFU	Reserved for future use.							
AUT_ISRC_SCL	Automatic scaling for impedance detection reference 00 = 10% of full ADC scale 01 = 20% of full ADC scale 10 = 30% of full ADC scale 11 = 30% of full ADC scale (default)							
ISRC_MAN	Current source manual detection 0 = automatic scaling for detection when ENb = 0 (default) 1 = manual detection when ENb = 0, fixed based on I_SRC and ISRC_TMR register values (register 0x06 and 0x07)							
ISRC_ST	Current source manual start and ADC conversion. The bit is cleared after one impedance detection. 0 = disable (default) 1 = start one manual impedance detection							

Table 2. Detailed Register Map (continued)

PCON CTRL 0x09 (Read/Write)								
BIT	7	6	5	4	3	2	1	0
BIT NAME	RFU	RFU	RFU	RFU	PCON_ RDY	RFU	PCON_ EN	PCON_ MAN
Reset Value	0	0	0	0	0	0	0	0
RFU	Reserved for future use							
PCON_RDY (Read Only)	PCON output is ready to be on as ADC value is within factory mode range. The PCON output will be turned on if the next immediate ADC value is 0xFF with 150μA. 0 = PCON output is disabled 1 = PCON output is ready							
PCON_EN	Open-drain output for the external P-FET control output enable in manual mode 0 = output is disabled (output is hi-Z) (default) 1 = output is enabled (output is active low)							
PCON_MAN	PCON output manual control 0 = PCON output is controlled by the automatic factory mode (default) 1 = PCON output is controlled by the PCON_EN bit							
ACCDET_REF 0x0A (Read/Write)								
BIT	7	6	5	4	3	2	1	0
BIT NAME	ACC_DET_TH							
Reset Value	0	1	1	0	1	1	1	0
ACC_DET_TH	Accessory Detection Threshold Accessory is detected (ACC_DET = 1) if ADC_1 (0x0B) final reading is lower than ACC_DET_TH							
ISRC_ADC 0x0B (Read Only)								
BIT	7	6	5	4	3	2	1	0
BIT NAME	ADC_1							
Reset Value	0	0	0	0	0	0	0	0
ADC_1	ID ADC reading: 0V to 1.5V Voltage step 5.9mV (typ)							
FM_I_SET 0x0D (Read/Write)								
BIT	7	6	5	4	3	2	1	0
BIT NAME	RFU					FIS		
Reset Value	0	0	0	0	0	0	1	0
FIS	The current source set for the factory mode resistor value. 000 = off (no factory mode) 001 = 2μA 010 = 6μA (default) 011 = 18μA 100 = 54μA 101 = 162μA 110 = 2500μA 111 = off (no factory mode)							

Table 2. Detailed Register Map (continued)

FM_HI_LIM 0x0E (Read/Write)								
BIT	7	6	5	4	3	2	1	0
BIT NAME	FHL							
Reset Value	1	0	1	0	1	1	1	1
FHL	The factory mode ADC value high limit value 1010 1111 = 1032.5mV (172kΩ)							
FM_LO_LIM 0x0F (Read/Write)								
BIT	7	6	5	4	3	2	1	0
BIT NAME	FLL							
Reset Value	1	0	0	0	0	0	1	0
FLL	The factory mode ADC value low limit value 1000 0010 = 767mV (127.8kΩ)							

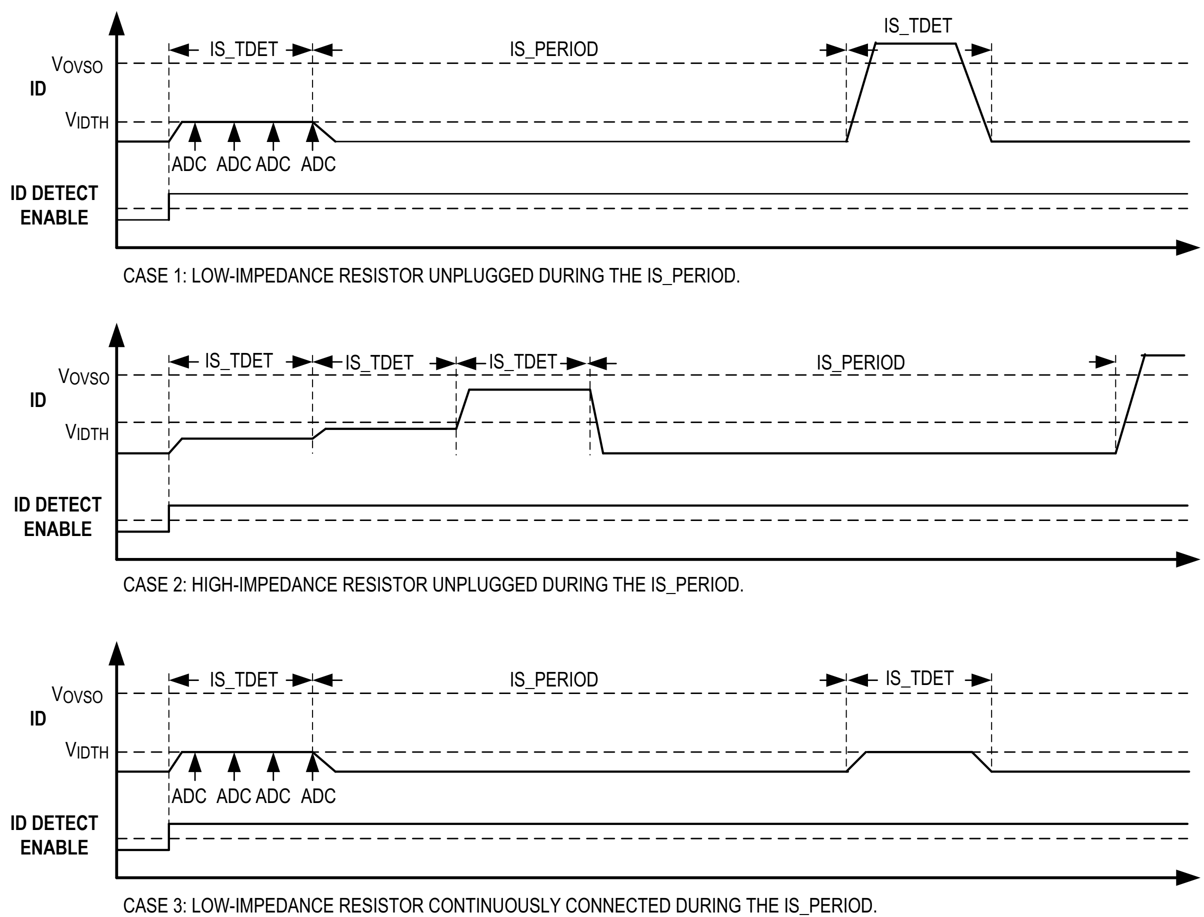


Figure 1. Current Source On-Time Timing Diagram (IS_INIT_SET = 0)

Detailed Description

The MAX20330A is a universal ID detection IC that detects the ID resistor values when it is enabled. The device automatically adjusts the detection current to check the wide range of the ID resistor values while keeping the average supply current low. The device can be used in many different applications such as accessory detection, secure factory mode, connector wet detection, etc.

$\overline{EN}$ pin and ENb Bit

The MAX20330A is enabled by $\overline{EN}$ pin and ENb bit. ENb bit is defaulted to 0. The ID check is enabled when $\overline{EN}$ goes low after debounce time (100ms, typ).

All the registers are reset to default values when the device enters shutdown.

$\overline{EN}$ (pin)	ENb (I^2C)	STATUS
1	0	Shutdown
1	1	Shutdown
0	0	Active
0	1	Shutdown

36VDC (40V Abs Max) Withstanding

The MAX20330A can withstand the DC voltage up to 40V on ID pin. If 40V input is expected, it is recommended to use the external TVS that clamps the surge to 40V or below.

Factory Mode

When the MAX20330A determines that the final ADC value is within the range of the factory resistor value in the preset I^2C registers, it enables the factory mode check. The factory mode can be enabled or disabled by the I^2C register bit FM_ENb.

The factory mode starts when the MAX20330A finds the ADC resistor value is within the factory resistor value range. Then the device must find out that the ID pin is biased with the voltage higher than 2.7V (typ). The factory ID resistor must be present for at least the total period equals to the sum of 2xIS_TDET and IS_PERIOD. There is no limit how long the resistor can be present until the ID is biased by the factory mode power supply. The factory mode is cancelled either the ID resistor changes prior to the presence of the factory mode power supply presence or removing of the factory bias voltage. Also set ENb bit in I^2C register high cancels the factory mode.

3.5mm Moisture Detection Application

The MAX20330A can be used to determine the faulty insertion of the jack due to a wrong impedance detection of the connector by moisture intrusion. The ACC_DET interrupt can be used to identify the valid accessory insertion and disconnect detection of the accessory.

The accessory detection threshold can be adjusted for issuing the proper accessory detection interrupt based on a valid jack impedance.

Thermal Shutdown

Thermal shutdown circuitry protects the devices from overheating. When the junction temperature exceeds +125°C (typ), the THERM_SHDN bit and interrupt are on.

Application Information

I^2C Interface

When in I^2C mode, the MAX20330A operates as a slave device that sends and receives data through an I^2C-compatible 2-wire interface. The interface uses a serial data line (SDA) and a serial clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX20330A and generates the SCL clock that synchronizes the data transfer. The SDA line operates as both an input and an open-drain output. A pullup resistor is required on SDA. The SCL line operates only as an input. A pullup resistor is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output. Each transmission consists of a START condition sent by a master, followed by the MAX20330A 7-bit slave address plus R/$\overline{W}$ bit, a register address byte, one or more data bytes, and finally a STOP condition (Figure 2).

Start and Stop Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high (Figure 3). When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

Bit Transfer

One data bit is transferred during each clock pulse (Figure 4). The data on SDA must remain stable while SCL is high. Changes in SDA while SCK is high and stable are considered control signals (see *Start and Stop Conditions*).

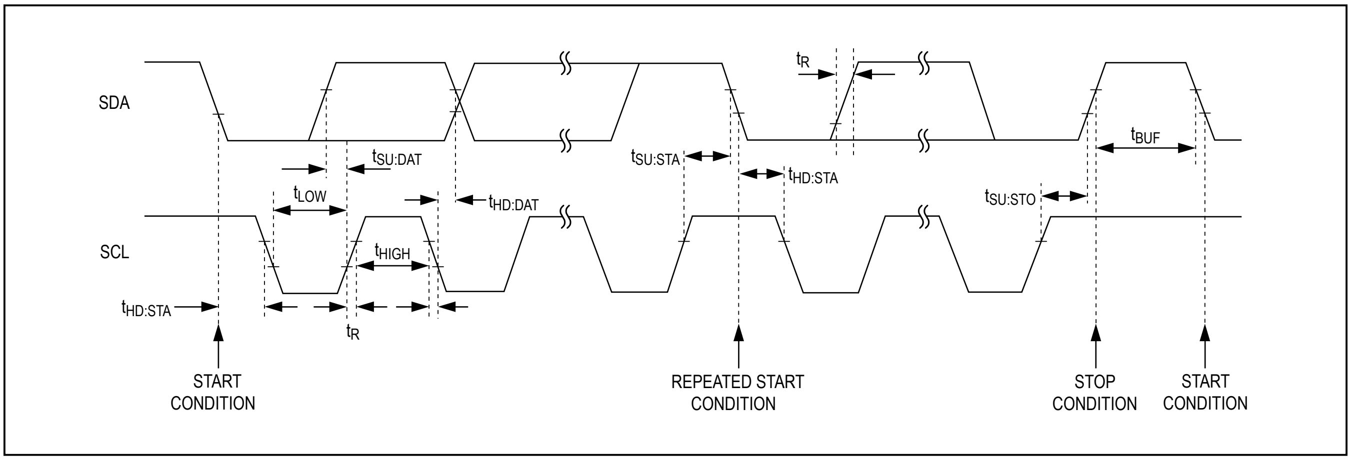


Figure 2. I²C Interface Timing Details

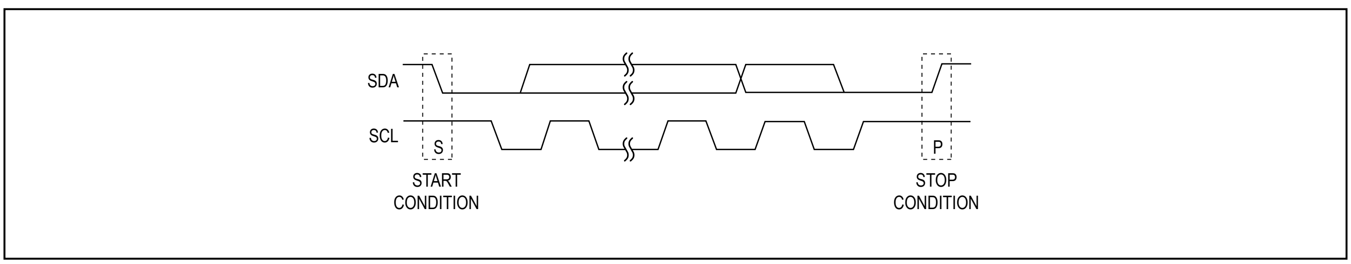


Figure 3. Start and Stop Conditions

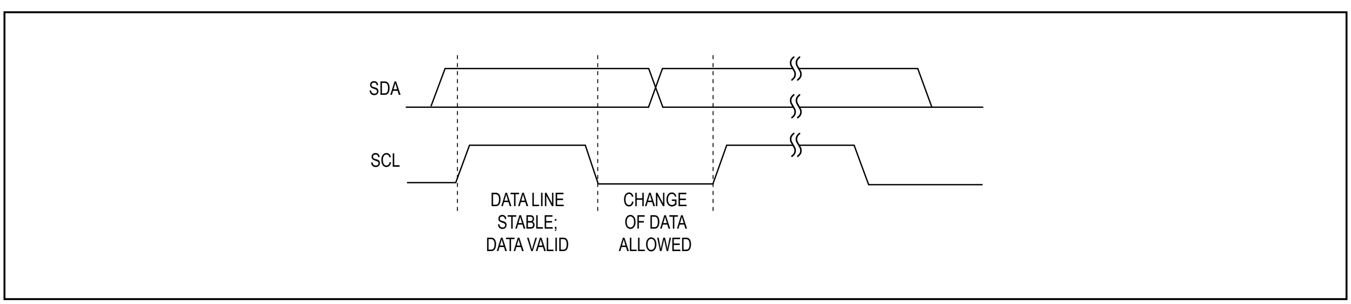


Figure 4. Bit Transfer

Acknowledge

The acknowledge bit is a clocked 9th bit (Figure 5), which the recipient uses to handshake receipt of each byte of data. Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse. The SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX20330A, it generates the acknowledge bit because the device is the recipient. When the device is transmitting to the master, the master generates the acknowledge bit because the master is the recipient. If the device did not pull SDA low, a not acknowledge is indicated.

Slave Address

The MAX20330A features a 7-bit slave address: 1010 111. The bit following a 7-bit slave address is the R/$\overline{W}$ bit, which is low for a write command and high for a read command.

Bus Reset

The MAX20330A resets the bus with the I2C start condition for reads. When the R/$\overline{W}$ bit is set to 1, the device transmits data to the master, thus the master is reading from the device.

Format for Writing

A write to the MAX20330A comprises the transmission of the slave address with the R/$\overline{W}$ bit set to zero, followed by at least 1 byte of information. The first byte of information is the register address or command byte. The register address determines which register of the device is to be written by the next byte, if received. If a STOP (P) condition is detected after the register address is received, then the device takes no further action beyond storing the register address. Any bytes received after the register address are data bytes. The first data byte goes into the register selected by the register address and subsequent data bytes go into subsequent registers (Figure 6). If multiple data bytes are transmitted before a STOP condition, these bytes are stored in subsequent registers because the register addresses autoincrement (Figure 7).

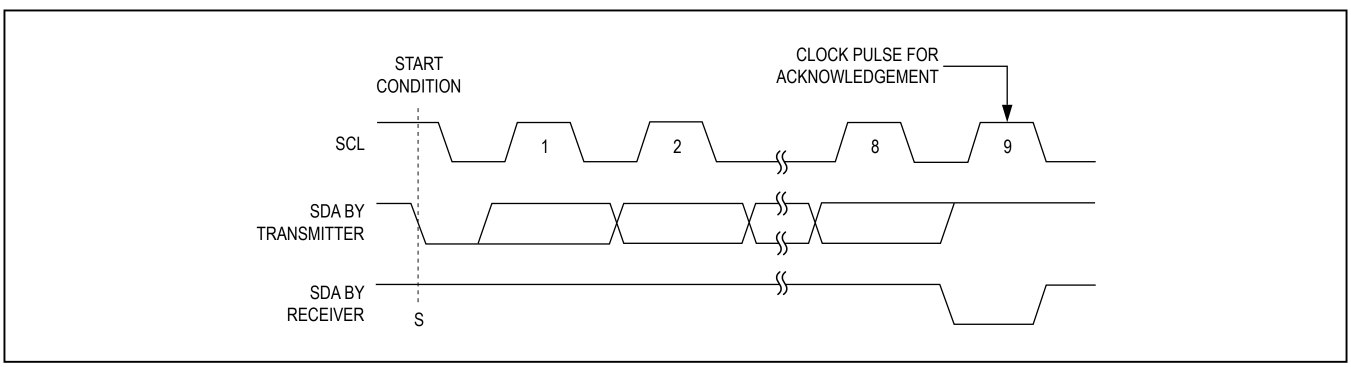


Figure 5. Acknowledge

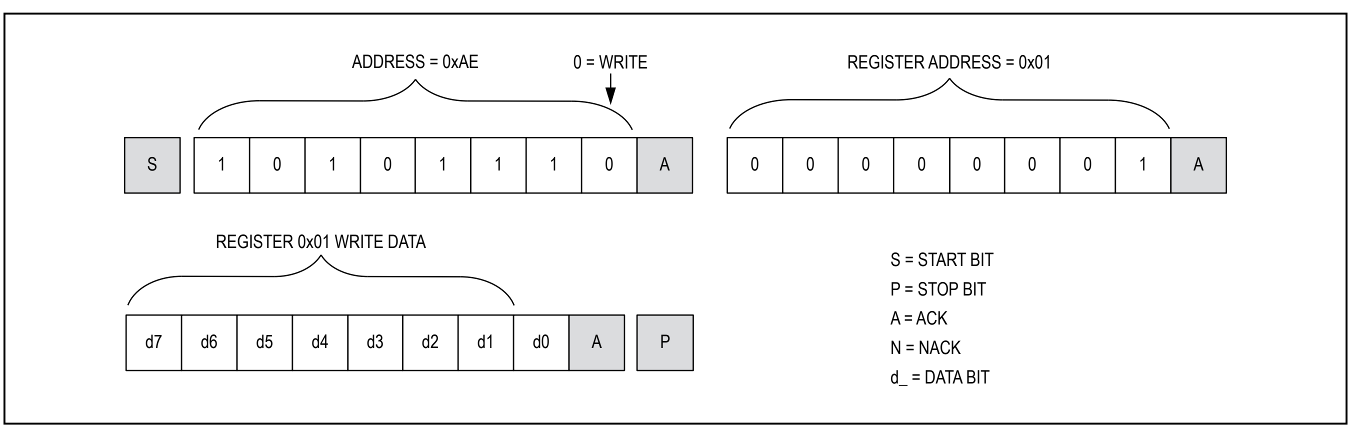


Figure 6. Format for I2C Write

Format for Reading

The MAX20330A is read using the internally stored register address as an address pointer, the same way the stored register address is used as an address pointer for a write. The pointer autoincrements after each data byte is read using the same rules as for a write. Thus, a read is initiated by first configuring the register address by performing a write (Figure 8). The master can now read consecutive bytes from the device, with the first data byte being read from the register addressed pointed by the previously written register address (Figure 9). Once the master sounds a NACK, the MAX20330A stops sending valid data.

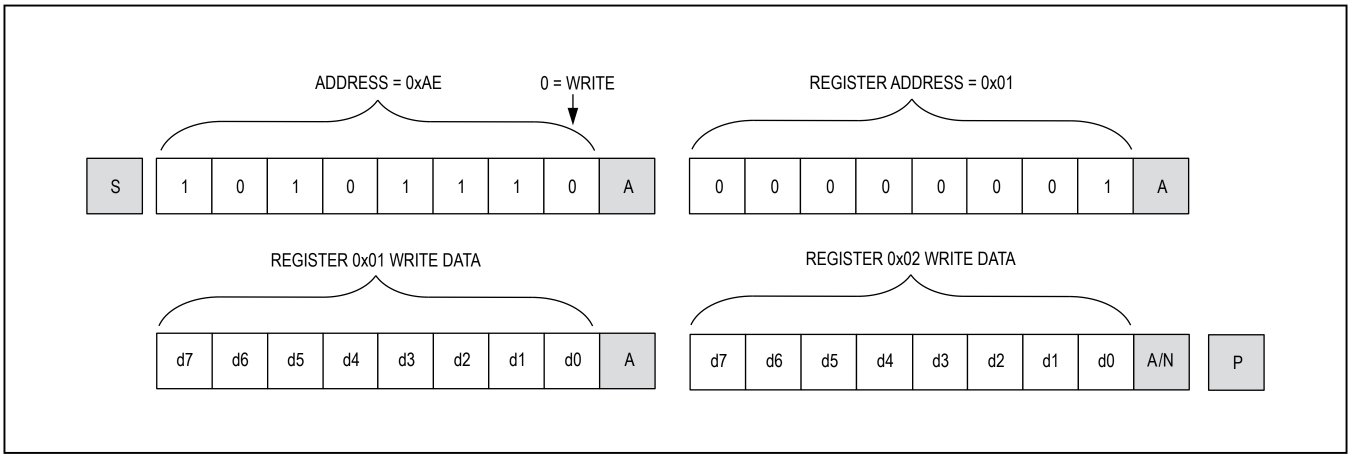


Figure 7. Format for Writing to Multiple Registers

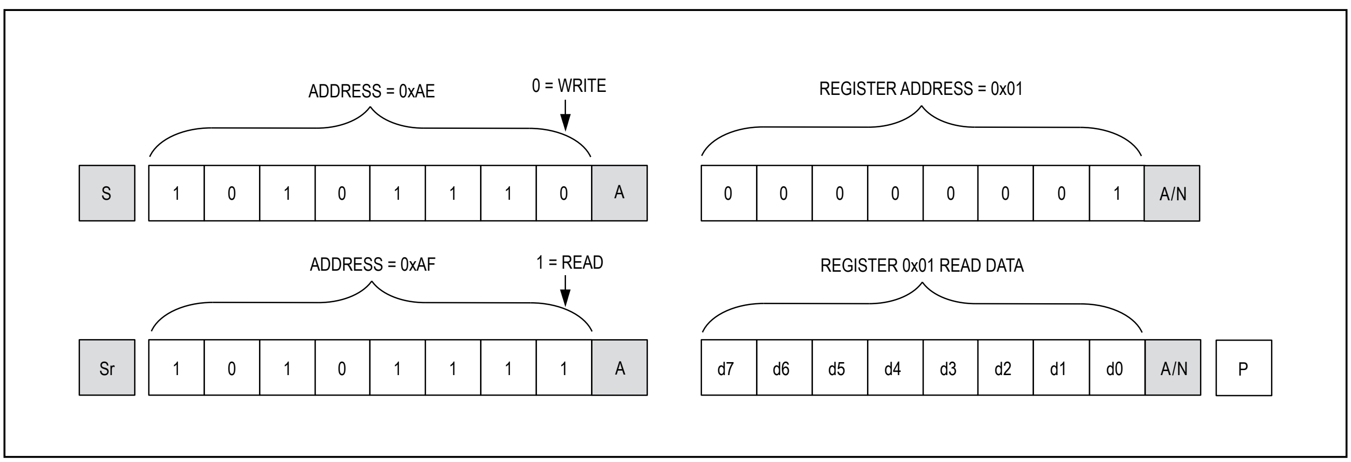


Figure 8. Format for Reads (Repeated Start)

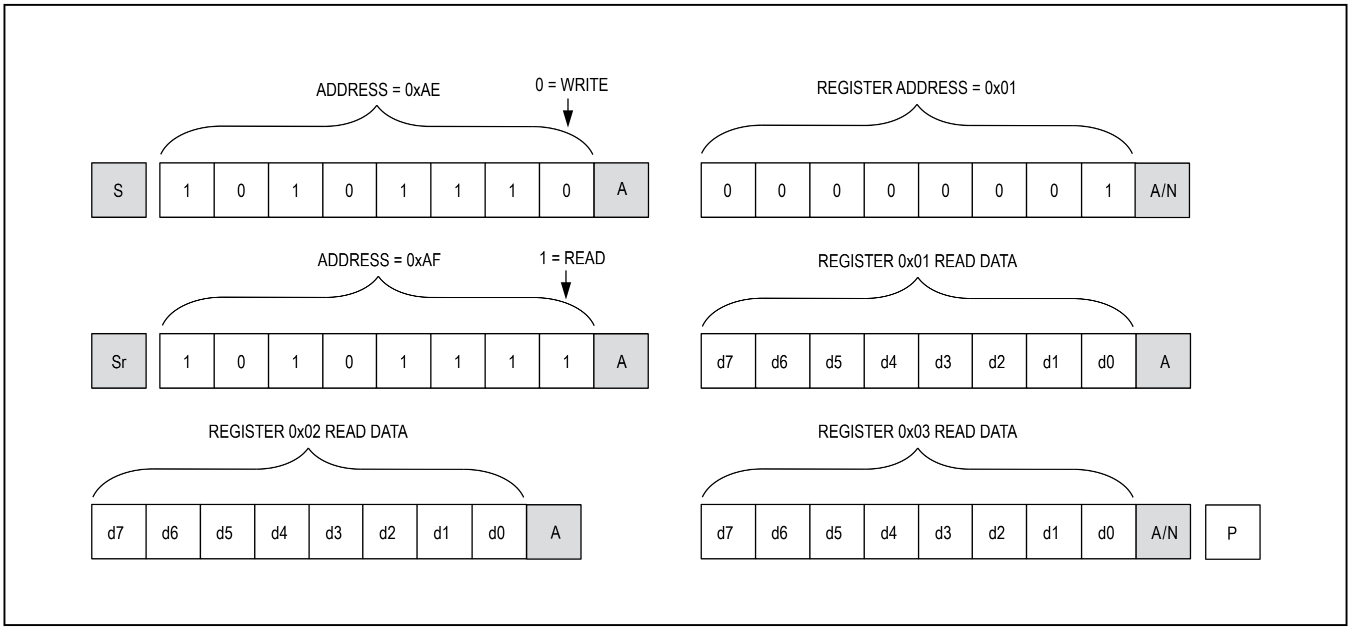
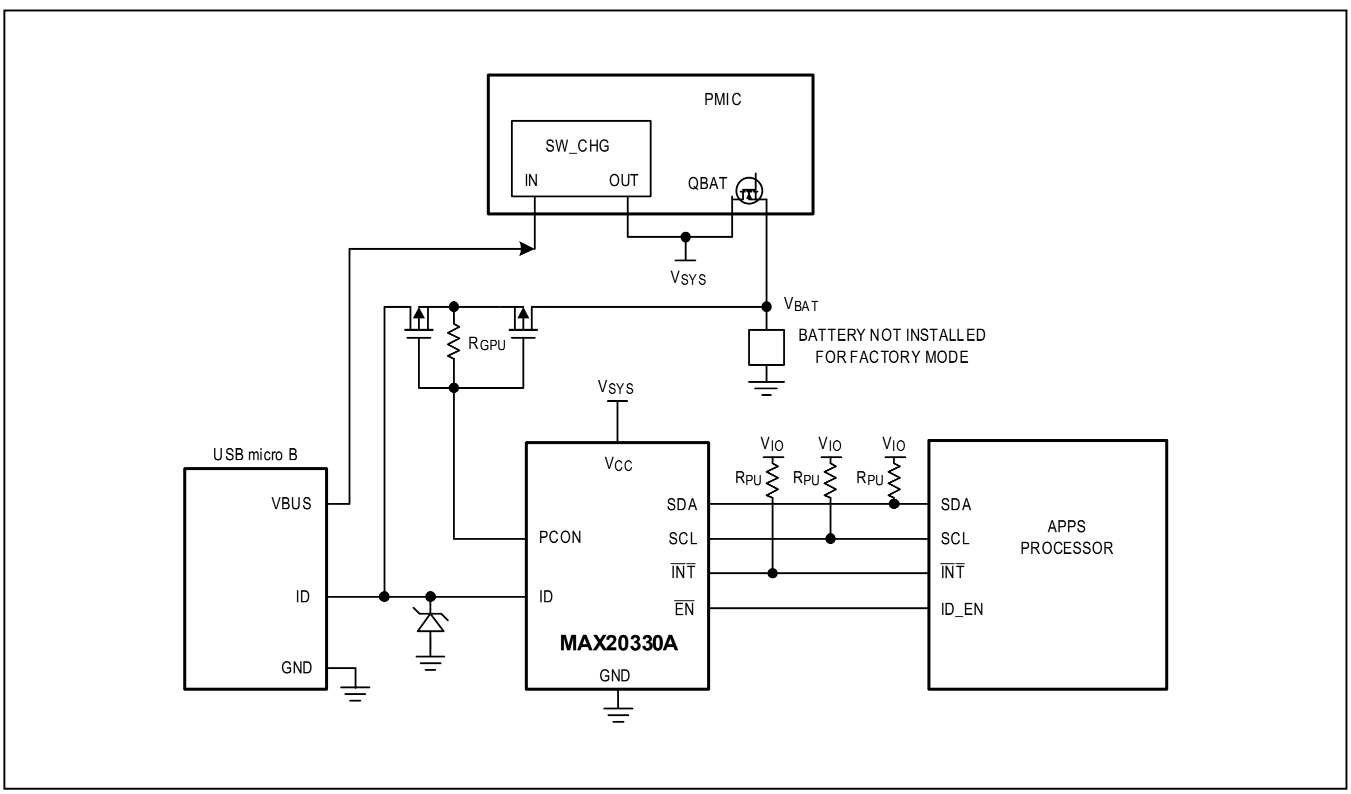
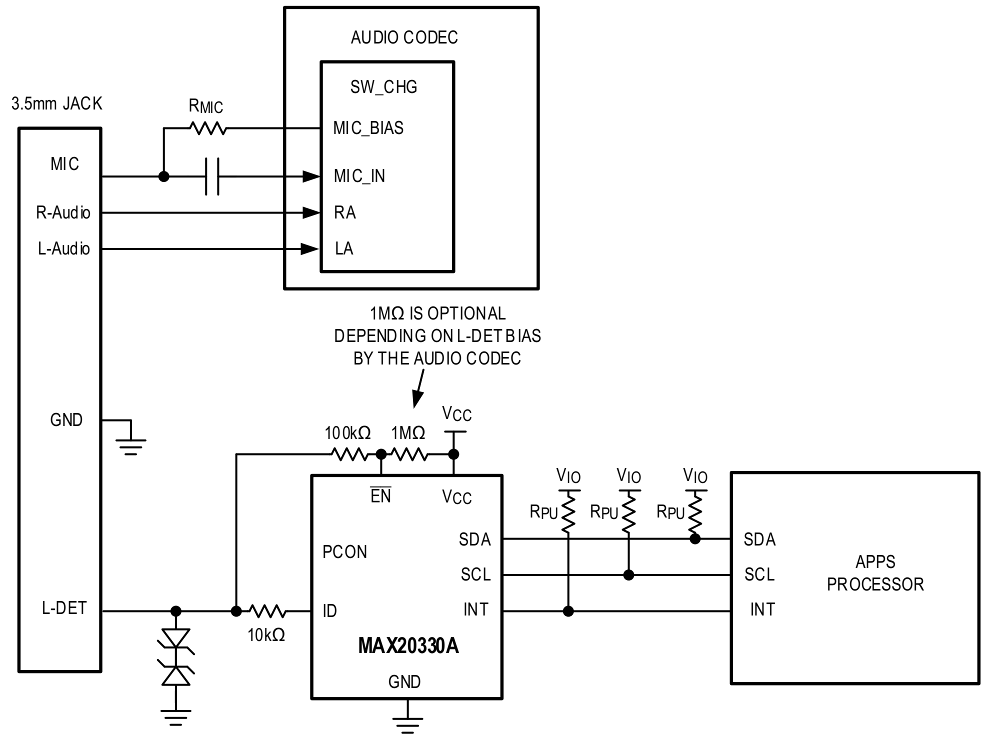


Figure 9. Format for Reading Multiple Registers

Typical Application Circuits



Typical Application Circuits (continued)



Ordering Information

PART	TOP MARK	TEMP RANGE	PIN-PACKAGE
MAX20330AEWA+T	CB	-40°C TO +85°C	8 WLP

+ Denotes lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 WLP	W81B1+1	21-100229	Refer to Application Note 1891

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/18	Initial release	—
1	6/18	Updated Table 2	12

